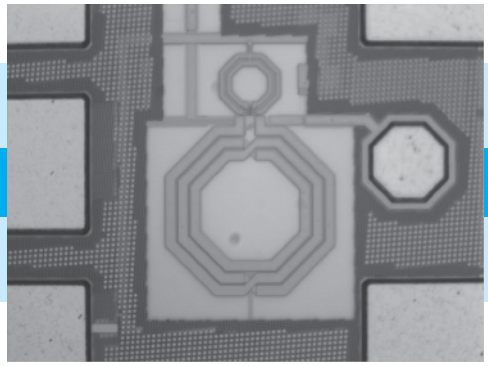

6

Nuevo enfoque: primero leo todo, dsp anoto

Physics of MOS Transistors

Today's field of microelectronics is dominated by a type of device called the metal-oxide-semiconductor field-effect transistor (MOSFET). Conceived in the 1930s but first realized in the 1960s, MOSFETs (also called MOS devices) offer unique properties that have led to the revolution of the semiconductor industry. This revolution has culminated in microprocessors having 100 million transistors, memory chips containing billions of transistors, and sophisticated communication circuits providing tremendous signal processing capability.

Our treatment of MOS devices and circuits follows the same procedure as that taken in Chapters 2 and 3 for *pn* junctions. In this chapter, we analyze the structure and operation of MOSFETs, seeking models that prove useful in circuit design. In Chapter 7, we utilize the models to study MOS amplifier topologies. The outline below illustrates the sequence of concepts covered in this chapter.

Operation of MOSFETs
- MOS Structure
- Operation in Triode Region
- Operation in Saturation
- I/V Characteristics

➤

MOS Device Models
- Large–Signal Model
- Small–Signal Model

➤

PMOS Devices
- Structure
- Models

6.1 STRUCTURE OF MOSFET

Recall from Chapter 5 that any voltage-controlled current source can provide signal amplification. MOSFETs also behave as such controlled sources but their characteristics are different from those of bipolar transistors.

In order to arrive at the structure of the MOSFET, we begin with a simple geometry consisting of a conductive (e.g., metal) plate, an insulator ("dielectric"), and a doped

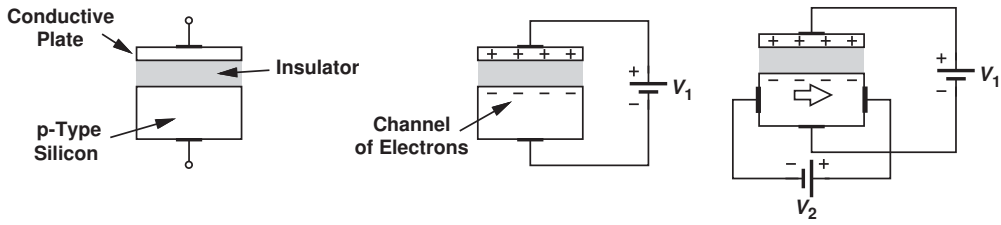

Figure 6.1 (a) Hypothetical semiconductor device, (b) operation as a capacitor, (c) current flow as a result of potential difference.

piece of silicon. Illustrated in Fig. 6.1(a), such a structure operates as a capacitor because the *p*-type silicon is somewhat conductive, "mirroring" any charge deposited on the top plate.

What happens if a potential difference is applied as shown in Fig. 6.1(b)? As positive charge is placed on the top plate, it attracts negative charge, e.g., electrons, from the piece of silicon. (Even though doped with acceptors, the *p*-type silicon does contain a small number of electrons.) We therefore observe that a "channel" of *free* electrons may be created at the interface between the insulator and the piece of silicon, potentially serving as a good conductive path if the electron density is sufficiently high. The key point here is that the density of electrons in the channel *varies* with V_1, as evident from $Q = CV$, where C denotes the capacitance between the two plates.

The dependence of the electron density upon V_1 leads to an interesting property: if, as depicted in Fig. 6.1(c), we allow a current to flow from left to right through the silicon material, V_1 can *control* the current by adjusting the resistivity of the channel. (Note that the current prefers to take the path of least resistance, thus flowing primarily through the channel rather than through the entire body of silicon.) This will serve our objective of building a voltage-controlled current source.

Equation $Q = CV$ suggests that, to achieve a strong control of Q by V, the value of C must be maximized, for example, by *reducing* the thickness of the dielectric layer separating the two plates.[1] The ability of silicon fabrication technology to produce extremely thin but uniform dielectric layers (with thicknesses below 20 Å today) has proven essential to the rapid advancement of microelectronic devices.

The foregoing thoughts lead to the MOSFET structure shown in Fig. 6.2(a) as a candidate for an amplifying device. Called the "gate" (G), the top conductive plate resides on a thin dielectric (insulator) layer, which itself is deposited on the underlying *p*-type silicon "substrate." To allow current flow through the silicon material, two contacts are attached to the substrate through two heavily-doped *n*-type regions because direct connection of metal to the substrate would not produce a good "ohmic" contact.[2] These two terminals are called "source" (S) and "drain" (D) to indicate that the former can *provide* charge carriers and the latter can *absorb* them. Figure 6.2(a) reveals that the device is symmetric with respect to S and D; i.e., depending on the voltages applied to the device, either of

[1]The capacitance between two plates is given by $\epsilon A/t$, where ϵ is the "dielectric constant" (also called the "permitivity"), A is the area of each plate, and t is the dielectric thickness.

[2]Used to distinguish it from other types of contacts such as diodes, the term "ohmic" contact emphasizes bi-directional current flow—as in a resistor.

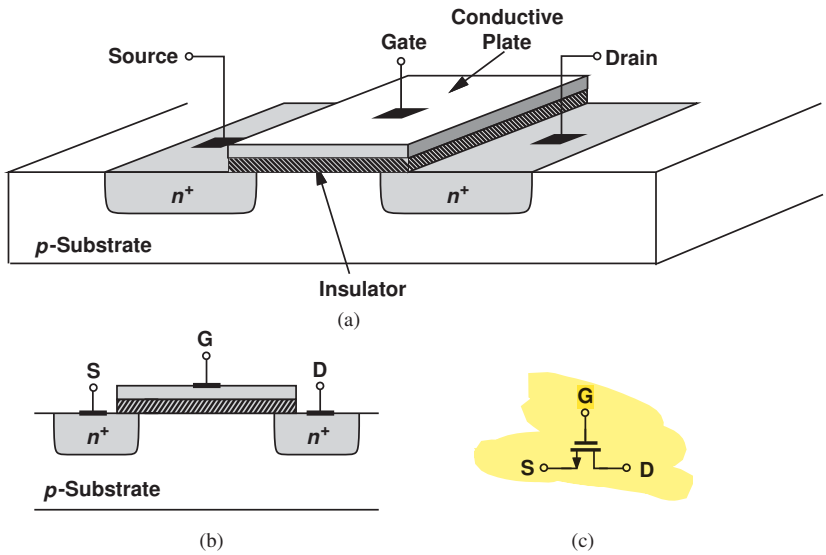

Figure 6.2 (a) Structure of MOSFET, (b) side view, (c) circuit symbol.

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these two terminals can drain the charge carriers from the other. As explained in Section 6.2, with *n*-type source/drain and *p*-type substrate, this transistor operates with electrons rather than holes and is therefore called an *n*-type MOS (NMOS) device. (The *p*-type counterpart is studied in Section 6.4.) We draw the device as shown in Fig. 6.2(b) for simplicity. Figure 6.2(c) depicts the circuit symbol for an NMOS transistor, wherein the arrow signifies the source terminal.

Before delving into the operation of the MOSFET, let us consider the types of materials used in the device. The gate plate must serve as a good conductor and was in fact realized by metal (aluminum) in the early generations of MOS technology. However, it was discovered that noncrystalline silicon ("polysilicon" or simply "poly") with heavy doping (for low resistivity) exhibits better fabrication and physical properties. Thus, today's MOSFETs employ polysilicon gates.

The dielectric layer sandwiched between the gate and the substrate plays a critical role in the performance of transistors and is created by growing silicon dioxide (or simply

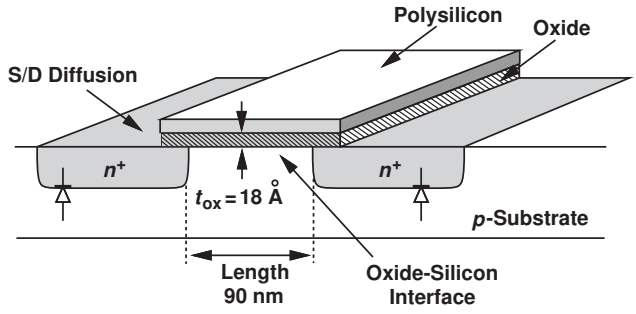

Figure 6.3 Typical dimensions of today's MOSFETs.

"oxide") on top of the silicon area. The n^+ regions are sometimes called source/drain "diffusion," referring to a fabrication method used in early days of microelectronics. We should also remark that these regions in fact form *diodes* with the *p*-type substrate (Fig. 6.3). As explained later, proper operation of the transistor requires that these junctions remain reverse-biased. Thus, only the depletion region capacitance associated with the two diodes must be taken into account. Figure 6.3 shows some of the device dimensions in today's state-of-the-art MOS technologies. The oxide thickness is denoted by t_{ox}.

6.2 OPERATION OF MOSFET

This section deals with a multitude of concepts related to MOSFETs. The outline is shown in Fig. 6.4.

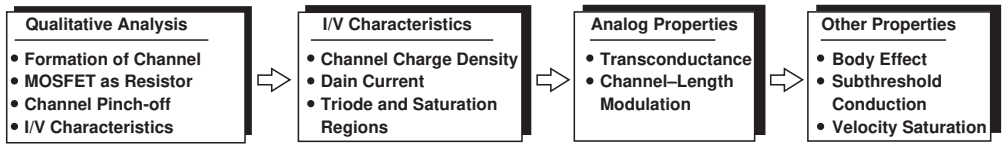

Figure 6.4 Outline of concepts to be studied.

6.2.1 Qualitative Analysis

Our study of the simple structures shown in Figs. 6.1 and 6.2 suggests that the MOSFET may conduct current between the source and drain if a channel of electrons is created by making the gate voltage sufficiently positive. Moreover, we expect that the magnitude of the current can be controlled by the gate voltage. Our analysis will indeed confirm these conjectures while revealing other subtle effects in the device. Note that the gate terminal draws no (low-frequency) current as it is insulated from the channel by the oxide.

La idea es siempre la misa: fuente de corriente controlada por tensión

Dentro del MOS hay como un capacitor, q' a altas frecuencias no a ser un corto

Since the MOSFET contains three terminals,[3] we may face many combinations of terminal voltages and currents. Fortunately, with the (low-frequency) gate current being zero, the only current of interest is that flowing between the source and the drain. We must study the dependence of this current upon the gate voltage (e.g., for a constant drain voltage) and upon the drain voltage (e.g., for a constant gate voltage). These concepts become clearer below.

Did you know?

The concept of MOSFET was proposed by Julius Edgar Lilienfeld in 1925, decades before the invention of the bipolar transistor. But why did it take until the 1960s for the MOS transistor to be successfully fabricated? The critical issue was the oxide-silicon interface. In initial attempts, this interface contained many "surface states," trapping the charge carriers and leading to poor conduction. As semiconductor technology advanced and "clean rooms" were invented for fabrication, the oxide could be grown on silicon with almost no surface states, yielding a high transconductance.

Let us first consider the arrangement shown in Fig. 6.5(a), where the source and drain are grounded and the gate voltage is varied. This circuit does not appear particularly useful but it gives us a great deal of insight. Recall from Fig. 6.1(b) that, as V_G rises, the positive charge on the gate must be mirrored by negative charge in the substrate. While we stated in Section 6.1 that electrons are attracted to the interface, in reality, another phenomenon precedes the formation of the channel. As V_G increases from zero, the positive charge on the gate *repels* the holes in the substrate, thereby exposing negative ions and creating a depletion region [Fig. 6.5(b)].[4]

[3]The substrate acts as a fourth terminal, but we ignore that for now.

[4]Note that this depletion region contains only one immobile charge polarity, whereas the depletion region in a *pn* junction consists of two areas of negative and positive ions on the two sides of the junction.

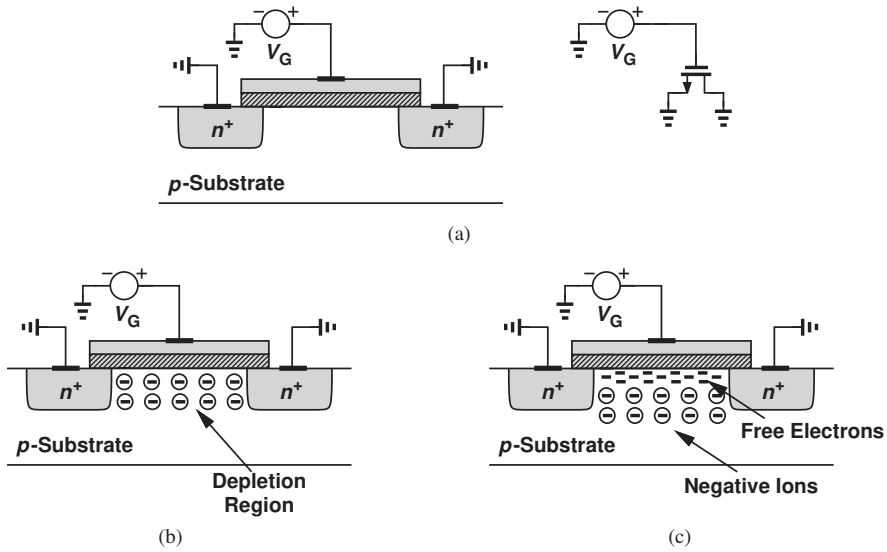

Figure 6.5 (a) MOSFET with gate voltage, (b) formation of depletion region, (c) formation of channel.

Note that the device still acts as a capacitor—positive charge on the gate is mirrored by negative charge in the substrate—but no channel of *mobile* charge is created yet. Thus, no current can flow from the source to the drain. We say the MOSFET is off.

Can the source-substrate and drain-substrate junctions carry current in this mode? To avoid this effect, the substrate itself is also tied to zero, ensuring that these diodes are not forward-biased. For simplicity, we do not show this connection in the diagrams.

What happens as V_G increases? To mirror the charge on the gate, more negative ions are exposed and the depletion region under the oxide becomes deeper. Does this mean the transistor never turns on?! Fortunately, if V_G becomes sufficiently positive, free electrons are attracted to the oxide-silicon interface, forming a conductive channel [Fig. 6.5(c)]. We say the MOSFET is on. The gate potential at which the channel begins to appear is called the "threshold voltage," V_{TH}, and falls in the range of 300 mV to 500 mV. Note that the electrons are readily provided by the n^+ source and drain regions, and need not be supplied by the substrate.

It is interesting to recognize that the gate terminal of the MOSFET draws no (low-frequency) current. Resting on top of the oxide, the gate remains insulated from other terminals and simply operates as a plate of a capacitor.

MOSFET as a Variable Resistor The conductive channel between S and D can be viewed as a resistor. Furthermore, since the density of electrons in the channel must increase as V_G becomes more positive (why?), the value of this resistor *changes* with the gate voltage. Conceptually illustrated in Fig. 6.6, such a voltage-dependent resistor proves extremely useful in analog and digital circuits.

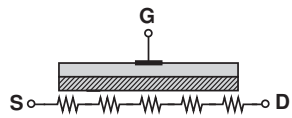

Figure 6.6 MOSFET viewed as a voltage-dependent resistor.

Example 6.1

In the vicinity of a wireless base station, the signal received by a cellphone may become very strong, possibly "saturating" the circuits and prohibiting proper operation. Devise a variable-gain circuit that lowers the signal level as the cellphone approaches the base station.

Solution

A MOSFET can form a voltage-controlled attenuator along with a resistor as shown in Fig. 6.7.

Since

$$\frac{v_{out}}{v_{in}} = \frac{R_1}{R_M + R_1}, \tag{6.1}$$

the output signal becomes smaller as V_{cont} falls because the density of electrons in the channel decreases and R_M rises. MOSFETs are commonly utilized as voltage-dependent resistors in "variable-gain amplifiers."

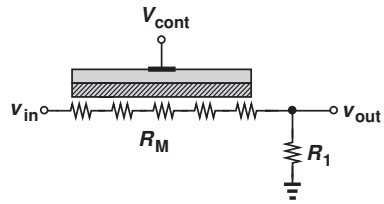

Figure 6.7 Use of MOSFET to adjust signal levels.

Exercise What happens to R_M if the channel length is doubled?

In the arrangement of Fig. 6.5(c), no current flows between S and D because the two terminals are at the same potential. We now raise the drain voltage as shown in Fig. 6.8(a) and examine the drain current (= source current). If $V_G < V_{TH}$, no channel exists, the device is off, and $I_D = 0$ regardless of the value of V_D. On the other hand, if $V_G > V_{TH}$, then $I_D > 0$ [Fig. 6.8(b)]. In fact, the source-drain path may act as a simple resistor, yielding the I_D-V_D characteristic shown in Fig. 6.8(c). The slope of the characteristic is equal to $1/R_{on}$, where R_{on} denotes the "on-resistance" of the transistor.[5]

Our brief treatment of the MOS I-V characteristics thus far points to two different views of the operation: in Fig. 6.8(b), V_G is varied while V_D remains constant whereas in Fig. 6.8(c), V_D is varied while V_G remains constant. Each view provides valuable insight into the operation of the transistor.

How does the characteristic of Fig. 6.8(b) change if V_G increases? The higher density of electrons in the channel lowers the on-resistance, yielding a *greater* slope. Depicted in Fig. 6.8(d), the resulting characteristics strengthen the notion of voltage-dependent resistance.

[5]The term "on-resistance" always refers to that between the source and drain, as no resistance exists between the gate and other terminals.

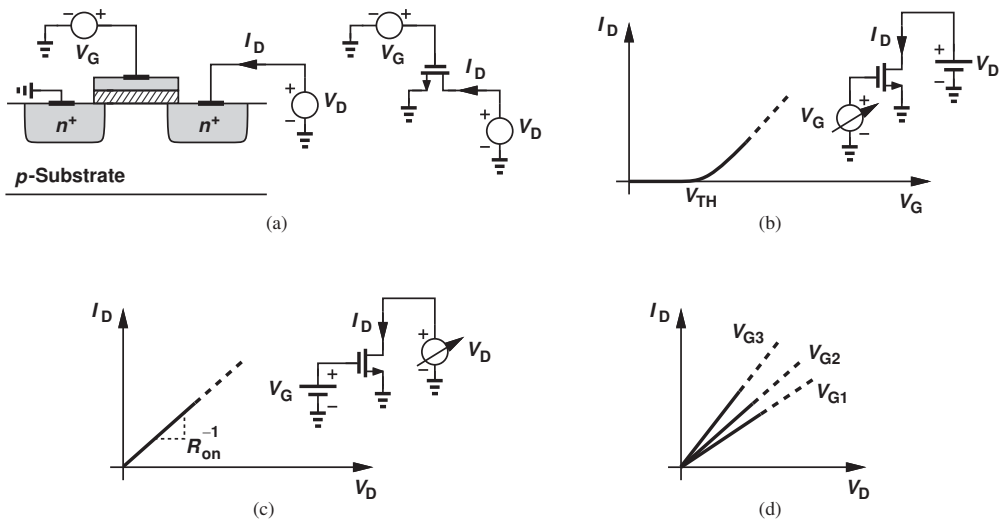

Figure 6.8 (a) MOSFET with gate and drain voltages, (b) I_D-V_G characteristic, (c) I_D-V_D characteristic, (d) I_D-V_D characteristics for various gate voltages.

Recall from Chapter 2 that charge flow in semiconductors occurs by diffusion or drift. How about the transport mechanism in a MOSFET? Since the voltage source tied to the drain creates an electric field along the channel, the current results from the *drift* of charge.

The I_D-V_G and I_D-V_D characteristics shown in Figs. 6.8(b) and (c), respectively, play a central role in our understanding of MOS devices. The following example reinforces the concepts studied thus far.

Example 6.2 Sketch the I_D-V_G and I_D-V_D characteristics for (a) different channel lengths, and (b) different oxide thicknesses.

Solution As the channel length increases, so does the on-resistance.[6] Thus, for $V_G > V_{TH}$, the drain current begins with lesser values as the channel length increases [Fig. 6.9(a)]. Similarly, I_D exhibits a smaller slope as a function of V_D [Fig. 6.9(b)]. It is therefore desirable to *minimize* the channel length so as to achieve large drain currents—an important trend in the MOS technology development.

Buscamos canales cortos y anchos (W/L grande)

How does the oxide thickness, t_{ox}, affect the I-V characteristics? As t_{ox} increases, the capacitance between the gate and the silicon substrate *decreases*. Thus, from $Q = CV$, we note that a given voltage results in *less* charge on the gate and hence a lower electron density in the channel. Consequently, the device suffers from a *higher* on-resistance, producing less drain current for a given gate voltage [Fig. 6.9(c)] or drain voltage [Fig. 6.9(d)]. For this reason, the semiconductor industry has continued to reduce the gate oxide thickness.

[6] Recall that the resistance of a conductor is proportional to the length.

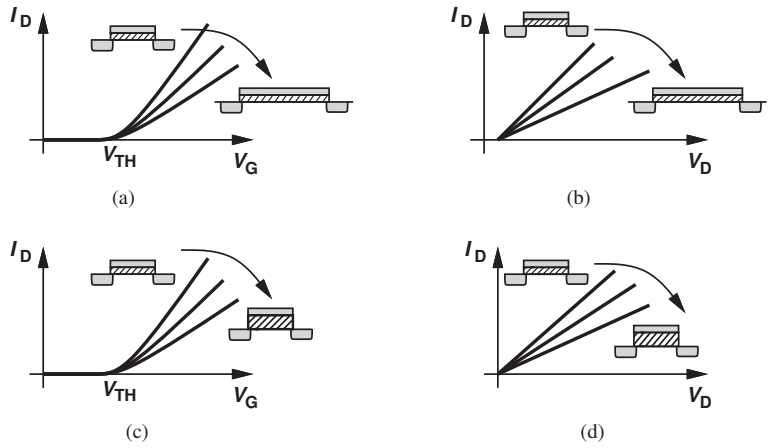

Figure 6.9 (a) I_D-V_G characteristics for different channel lengths, (b) I_D-V_D characteristics for different channel lengths, (c) I_D-V_G characteristics for different oxide thicknesses, (d) I_D-V_D characteristics for different oxide thicknesses.

Exercise The current conduction in the channel is in the form of drift. If the mobility falls at high temperatures, what can we say about the on-resistance as the temperature goes up?

While both the length and the oxide thickness affect the performance of MOSFETs, only the former is under the circuit designer's control, i.e., it can be specified in the "layout" of the transistor. The latter, on the other hand, is defined during fabrication and remains constant for all transistors in a given generation of the technology.

Another MOS parameter controlled by circuit designers is the *width* of the transistor, the dimension perpendicular to the length [Fig. 6.10(a)]. We therefore observe that

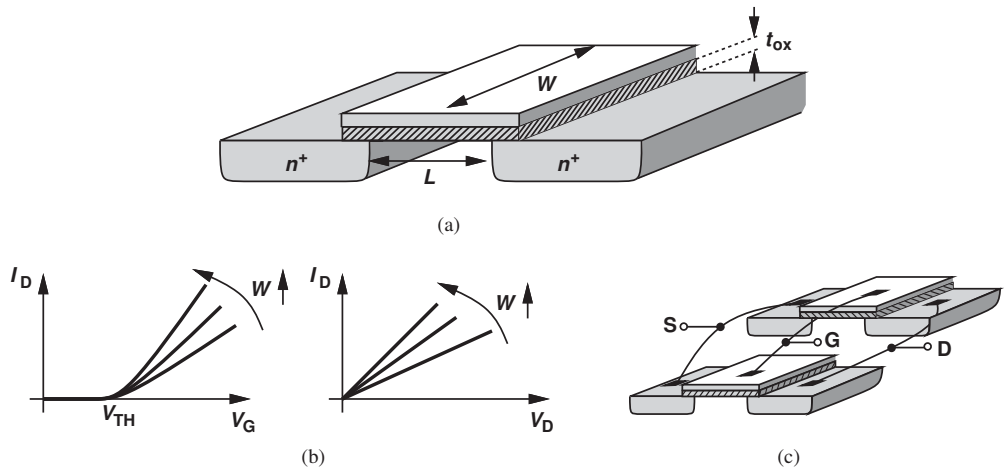

Figure 6.10 (a) Dimensions of a MOSFET (W and L are under circuit designer's control), (b) I_D characteristics for different values of W, (c) equivalence to devices in parallel.

"lateral" dimensions such as L and W can be chosen by circuit designers whereas "vertical" dimensions such as t_{ox} cannot.

How does the gate width impact the I-V characteristics? As W increases, so does the width of the channel, thus *lowering* the resistance between the source and the drain[7] and yielding the trends depicted in Fig. 6.10(b). From another perspective, a wider device can be viewed as two narrower transistors *in parallel*, producing a high drain current [Fig. 6.10(c)]. We may then surmise that W must be maximized, but we must also note that the total gate capacitance increases with W, possibly limiting the speed of the circuit. Thus, the width of each device in the circuit must be chosen carefully.

$W \uparrow \Rightarrow C \uparrow \Rightarrow |Z_C| \downarrow$ ⇒ A frecuencias no tan altas se empieza a notar el capacitor. Ojo al piojo con W

Llevo 20' de lectura. A morfar y dsp. Sigo.

Channel Pinch-Off Our qualitative study of the MOSFET thus far implies that the device acts as a voltage-dependent resistor if the gate voltage exceeds V_{TH}. In reality, however, the transistor operates as a *current source* if the drain voltage is sufficiently positive. To understand this effect, we make two observations: (1) to form a channel, the potential difference between the gate and the oxide-silicon interface must exceed V_{TH}; (2) if the drain voltage remains higher than the source voltage, then the voltage at each point along the channel with respect to ground increases as we go from the source towards the drain. Illustrated in Fig. 6.11(a), this effect arises from the gradual voltage drop along the channel resistance. Since the gate voltage is constant (because the gate is conductive but carries no current in any direction), and since the potential at the oxide-silicon interface rises from the source to the drain, the potential difference *between* the gate and the oxide-silicon interface *decreases* along the x-axis [Fig. 6.11(b)]. The density of electrons in the channel follows the same trend, falling to a minimum at $x = L$.

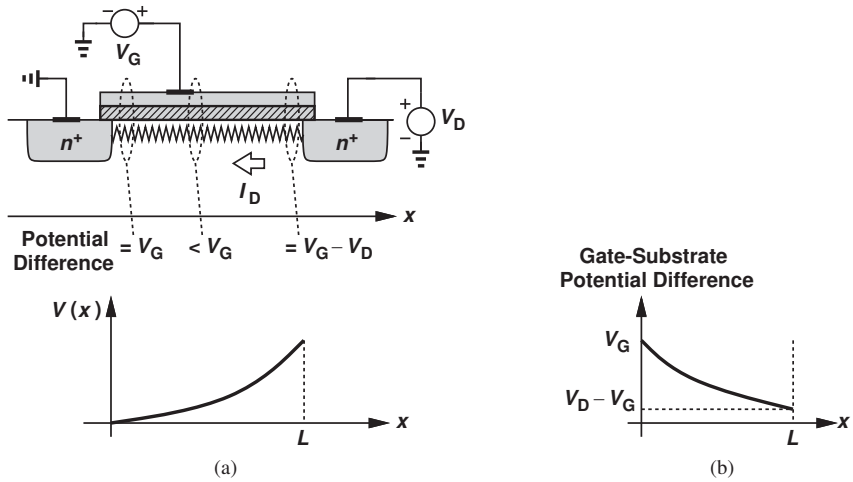

Figure 6.11 (a) Channel potential variation, (b) gate-substrate voltage difference along the channel.

[7]Recall that the resistance of a conductor is inversely proportional to the cross section area, which itself is equal to the product of the width and thickness of the conductor.

WTF

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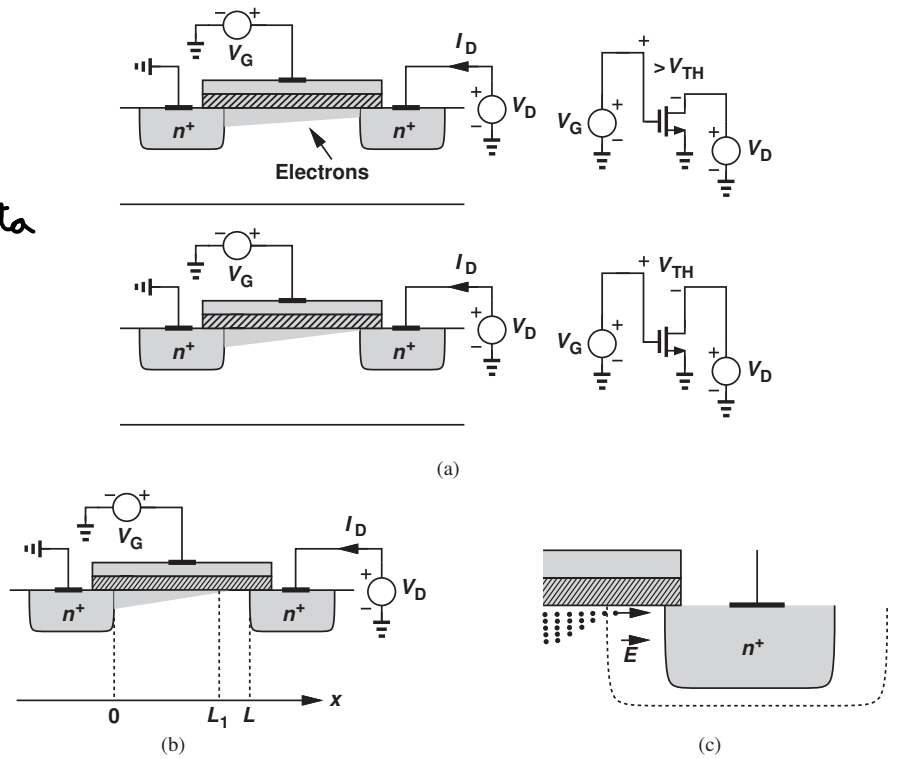


Figure 6.12 (a) Pinchoff, (b) variation of length with drain voltage, (c) detailed operation near the drain.

From these observations, we conclude that, if the drain voltage is high enough to produce $V_G - V_D \leq V_{TH}$, then the channel ceases to exist near the drain. We say the gate-substrate potential difference is not sufficient at $x = L$ to attract electrons and the channel is "pinched off" [Fig. 6.12(a)].

What happens if V_D rises even higher than $V_G - V_{TH}$? Since $V(x)$ now goes from 0 at $x = 0$ to $V_D > V_G - V_{TH}$ at $x = L$, the voltage difference between the gate and the substrate falls to V_{TH} at some point $L_1 < L$ [Fig. 6.12(b)]. The device therefore contains no channel between L_1 and L. Does this mean the transistor cannot conduct current? No, the device still conducts: as illustrated in Fig. 6.12(c), once the electrons reach the end of the channel, they experience the high electric field in the depletion region surrounding the drain junction and are rapidly swept to the drain terminal. Nonetheless, as shown in the next section, the drain voltage no longer affects the current significantly, and the MOSFET acts as a constant current source—similar to a bipolar transistor in the forward active region. Note that the source-substrate and drain-substrate junctions carry no current.

6.2.2 Derivation of I-V Characteristics

With the foregoing qualitative study, we can now formulate the behavior of MOSFETs in terms of their terminal voltages.

Channel Charge Density Our derivations require an expression for the channel charge (i.e., free electrons) per unit *length*, also called the "charge density." From $Q = CV$, we note

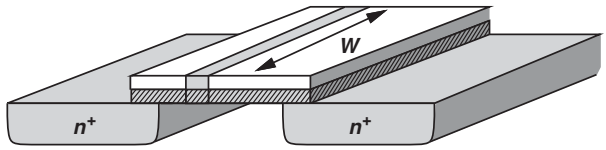


Figure 6.13 Illustration of capacitance per unit length.

that if C is the gate capacitance per unit length and V the voltage difference between the gate and the channel, then Q is the desired charge density. Denoting the gate capacitance per unit *area* by C_{ox} (expressed in F/m^2 or fF/μm^2), we write $C = WC_{ox}$ to account for the width of the transistor (Fig. 6.13). Moreover, we have $V = V_{GS} - V_{TH}$ because no mobile charge exists for $V_{GS} < V_{TH}$. (Hereafter, we denote both the gate and drain voltages with respect to the source.) It follows that

$$Q = WC_{ox}(V_{GS} - V_{TH}). \tag{6.2}$$

Note that Q is expressed in coulomb/meter. Now recall from Fig. 6.11(a) that the channel voltage varies along the length of the transistor, and the charge density falls as we go from the source to the drain. Thus, Eq. (6.2) is valid only near the source terminal, where the channel potential remains close to zero. As shown in Fig. 6.14, we denote the channel potential at x by $V(x)$ and write

$$Q(x) = WC_{ox}[V_{GS} - V(x) - V_{TH}], \tag{6.3}$$

noting that $V(x)$ goes from zero to V_D if the channel is not pinched off.

Drain Current What is the relationship between the mobile charge density and the current? Consider a bar of semiconductor having a uniform charge density (per unit length) equal to Q and carrying a current I (Fig. 6.15). Note from Chapter 2 that (1) I is given by the total charge that passes through the cross section of the bar in one second, and (2) if the carriers move with a velocity of v m/s, then the charge enclosed in v meters along the bar passes through the cross section in one second. Since the charge enclosed in v meters is equal to $Q \cdot v$, we have

$$I = Q \cdot v. \tag{6.4}$$

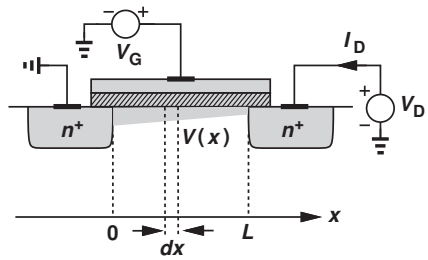


Figure 6.14 Device illustration for calculation of drain current.

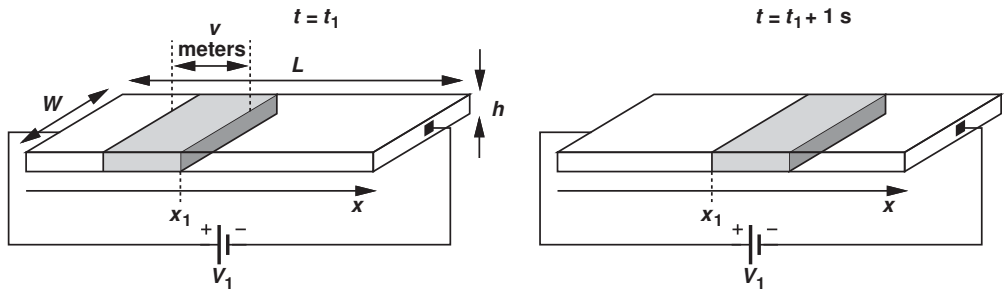


Figure 6.15 Relationship between charge velocity and current.

As explained in Chapter 2,

$$v = -\mu_n E, \tag{6.5}$$

$$= +\mu_n \frac{dV}{dx}, \tag{6.6}$$

where dV/dx denotes the derivative of the voltage at a given point. Combining Eqs. (6.3), (6.4), and (6.6), we obtain

$$I_D = WC_{ox}[V_{GS} - V(x) - V_{TH}]\mu_n \frac{dV(x)}{dx}. \tag{6.7}$$

Interestingly, since I_D must remain constant along the channel (why?), $V(x)$ and dV/dx must vary such that the product of $V_{GS} - V(x) - V_{TH}$ and dV/dx is independent of x.

While it is possible to solve the above differential equation to obtain $V(x)$ in terms of I_D (and the reader is encouraged to do that), our immediate need is to find an expression for I_D in terms of the terminal voltages. To this end, we write

$$\int_{x=0}^{x=L} I_D \, dx = \int_{V(x)=0}^{V(x)=V_{DS}} \mu_n C_{ox} W[V_{GS} - V(x) - V_{TH}] \, dV. \tag{6.8}$$

That is,

$$I_D = \frac{1}{2}\mu_n C_{ox} \frac{W}{L} \left[2(V_{GS} - V_{TH})V_{DS} - V_{DS}^2\right]. \tag{6.9}$$

We now examine this important equation from different perspectives to gain more insight. First, the linear dependence of I_D upon μ_n, C_{ox}, and W/L is to be expected: a higher mobility yields a greater current for a given drain-source voltage; a higher gate oxide capacitance leads to a larger electron density in the channel for a given gate-source voltage; and a larger W/L (called the device "aspect ratio") is equivalent to placing more transistors in parallel [Fig. 6.10(c)]. Second, for a constant V_{GS}, I_D varies *parabolically* with V_{DS} (Fig. 6.16), reaching a maximum of

$$I_{D,max} = \frac{1}{2}\mu_n C_{ox} \frac{W}{L}(V_{GS} - V_{TH})^2 \tag{6.10}$$

at $V_{DS} = V_{GS} - V_{TH}$. It is common to write W/L as the ratio of two values e.g., $5\,\mu$m/$0.18\,\mu$m (rather than 27.8) to emphasize the choice of W and L. While only the

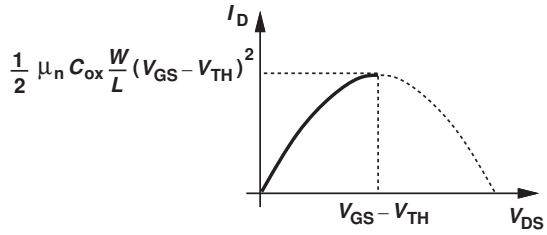


Figure 6.16 Parabolic I_D-V_{DS} characteristic.

ratio appears in many MOS equations, the individual values of W and L also become critical in most cases. For example, if both W and L are doubled, the ratio remains unchanged but the gate capacitance increases.

Example 6.3

Plot the I_D-V_{DS} characteristics for different values of V_{GS}.

Solution

As V_{GS} increases, so do $I_{D,max}$ and $V_{GS} - V_{TH}$. Illustrated in Fig. 6.17, the characteristics exhibit maxima that follow a parabolic shape themselves because $I_{D,max} \propto (V_{GS} - V_{TH})^2$.

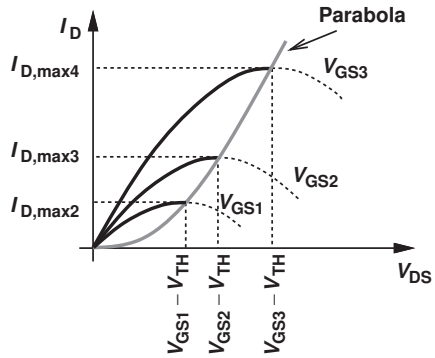


Figure 6.17 MOS characteristics for different gate-source voltages.

Exercise What happens to the above plots if t_{ox} is halved?

The nonlinear relationship between I_D and V_{DS} reveals that the transistor *cannot* generally be modeled as a simple linear resistor. However, if $V_{DS} \ll 2(V_{GS} - V_{TH})$, Eq. (6.9) reduces to:

$$I_D \approx \mu_n C_{ox} \frac{W}{L}(V_{GS} - V_{TH})V_{DS}, \tag{6.11}$$

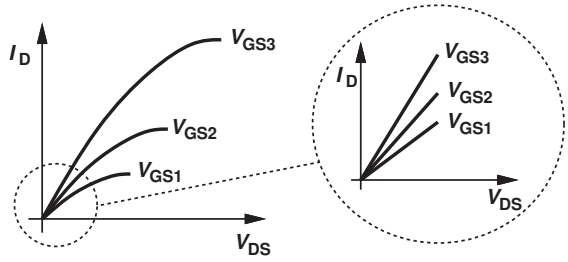


Figure 6.18 Detailed characteristics for small V_{DS}.

exhibiting a linear I_D-V_{DS} behavior for a given V_{GS}. In fact, the equivalent on-resistance is given by V_{DS}/I_D:

$$R_{on} = \frac{1}{\mu_n C_{ox} \dfrac{W}{L}(V_{GS} - V_{TH})}. \tag{6.12}$$

From another perspective, at small V_{DS} (near the origin), the parabolas in Fig. 6.17 can be approximated by straight lines having different slopes (Fig. 6.18).

As predicted in Section 6.2.1, Eq. (6.12) suggests that the on-resistance can be controlled by the gate-source voltage. In particular, for $V_{GS} = V_{TH}$, $R_{on} = \infty$, i.e., the device can operate as an electronic switch.

Example 6.4

A cordless telephone incorporates a single antenna for reception and transmission. Explain how the system must be configured.

Solution

The system is designed so that the phone receives for half of the time and transmits for the other half. Thus, the antenna is alternately connected to the receiver and the transmitter in regular intervals, e.g., every 20 ms (Fig. 6.19). An electronic antenna switch is therefore necessary here.[8]

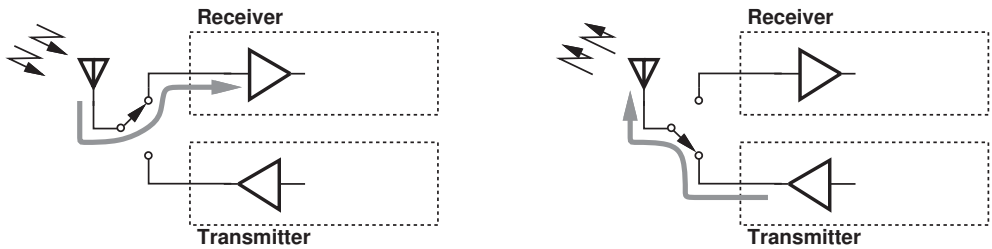


Figure 6.19 Role of antenna switch in a cordless phone.

Exercise Some systems employ two antennas, each of which receives and transmits signals. How many switches are needed?

[8]Some cellphones operate in the same manner.

In most applications, it is desirable to achieve a low on-resistance for MOS switches. The circuit designer must therefore maximize W/L and V_{GS}. The following example illustrates this point.

Example 6.5

In the cordless phone of Example 6.4, the switch connecting the transmitter to the antenna must negligibly attenuate the signal, e.g., by no more than 10%. If $V_{DD} = 1.8$ V, $\mu_n C_{ox} = 100\,\mu$A/V^2, and $V_{TH} = 0.4$ V, determine the minimum required aspect ratio of the switch. Assume the antenna can be modeled as a 50-Ω resistor.

Solution As depicted in Fig. 6.20, we wish to ensure

$$\frac{V_{out}}{V_{in}} \geq 0.9 \tag{6.13}$$

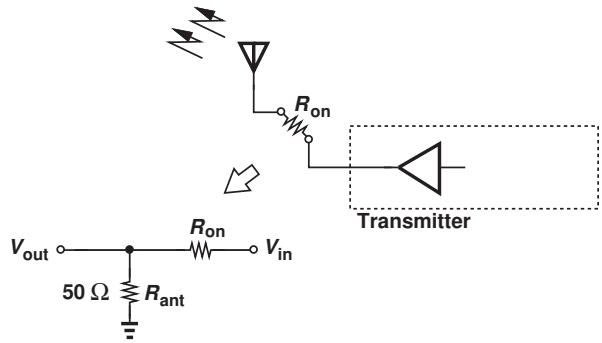


Figure 6.20 Signal degradation due to on-resistance of antenna switch.

and hence

$$R_{on} \leq 5.6\,\Omega. \tag{6.14}$$

Setting V_{GS} to the maximum value, V_{DD}, we obtain from Eq. (6.12),

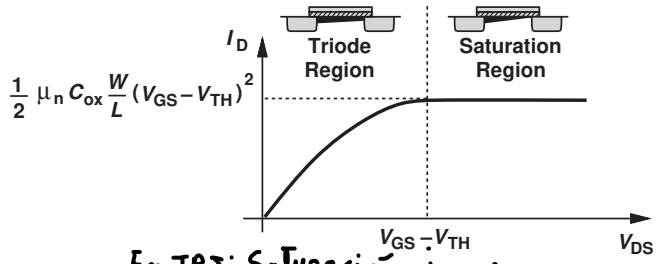
$$\frac{W}{L} \geq 1276. \tag{6.15}$$

(Since wide transistors introduce substantial capacitance in the signal path, this choice of W/L may still attenuate high-frequency signals.)

Exercise What W/L is necessary if V_{DD} drops to 1.2 V?

Triode and Saturation Regions Equation (6.9) expresses the drain current in terms of the device terminal voltages, implying that the current begins to *fall* for $V_{DS} > V_{GS} - V_{TH}$. We say the device operates in the "triode region" (also called the "linear region") if $V_{DS} < V_{GS} - V_{TH}$ (the rising section of the parabola). We also use the term "deep triode region" for $V_{DS} \ll 2(V_{GS} - V_{TH})$, where the transistor operates as a resistor.

Nota que nada que ver: a veces la tensión se comporta como un vector, no? Vce = extremo (c) menos origen (e) Y sí mi rey, eso es lo q significa una diferencia de potencial xd



En TBJ: Saturación ; MAD
($V_{CE}<0{,}7V$), ($V_{CE}>0{,}7$)

Figure 6.21 Overall MOS characteristic.

Saturación: Por más V_{DS} q' enclufe, I_D no crece

In reality, the drain current reaches "saturation," that is, becomes *constant* for $V_{DS} > V_{GS} - V_{TH}$ (Fig. 6.21). To understand why, recall from Fig. 6.12 that the channel experiences pinch-off if $V_{DS} = V_{GS} - V_{TH}$. Thus, further increase in V_{DS} simply shifts the pinch-off point slightly toward the drain. Also, recall that Eqs. (6.7) and (6.8) are valid only where channel charge exists. It follows that the integration in Eq. (6.8) must encompass only the channel, i.e., from $x = 0$ to $x = L_1$ in Fig. 6.12(b), and be modified to

$$\int_{x=0}^{x=L_1} I_D\,dx = \int_{V(x)=0}^{V(x)=V_{GS}-V_{TH}} \mu_n C_{ox} W[V_{GS} - V(x) - V_{TH}]\,dV. \qquad (6.16)$$

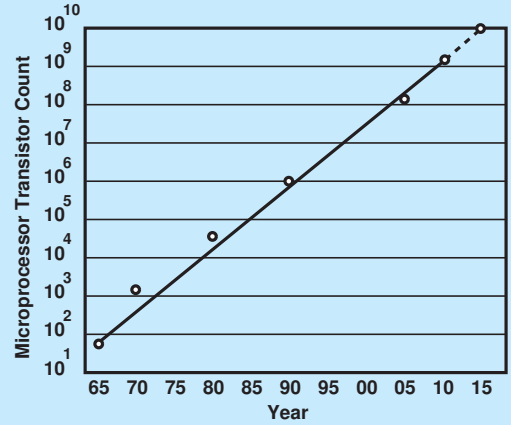
Note that the upper limits correspond to the channel pinch-off point. In particular, the integral on the right-hand side is evaluated up to $V_{GS} - V_{TH}$ rather than V_{DS}. Consequently,

$$I_D = \frac{1}{2}\mu_n C_{ox}\frac{W}{L_1}(V_{GS} - V_{TH})^2, \qquad (6.17)$$

a result independent of V_{DS} and identical to $I_{D,max}$ in Eq. (6.10) if we assume $L_1 \approx L$. Called the "overdrive voltage," the quantity $V_{GS} - V_{TH}$ plays a key role in MOS circuits. MOSFETs are sometimes called "square-law" devices to emphasize the relationship between I_D and the overdrive. For the sake of brevity, we hereafter denote L_1 with L.

Did you know?

The explosive growth of MOS technology is attributed to two factors: the ability to shrink the dimensions of the MOS device (W, L, t_{ox}, etc.) and the ability to integrate a greater number of MOS devices on a chip each year. The latter trend was predicted by one of Intel's founders, Gordon Moore, in 1965. He observed that the number of transistors per chip doubled every two years. Indeed, starting with 50 devices per chip in 1965, we now have reached tens of billions on memory chips and several billion on microprocessor chips. Can you think of any other product in human history that has grown so much so fast (except for Bill Gates' wealth)?

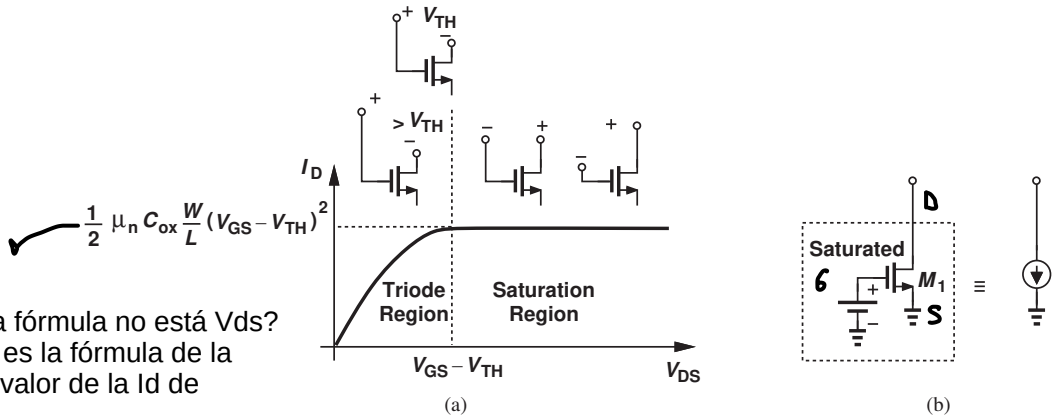


Moore's Law: transistor count per chip throughout the years.

The I-V characteristic of Fig. 6.21 resembles that of bipolar devices, with the triode and saturation regions in MOSFETs appearing similar to saturation and forward active regions in bipolar transistors, respectively. It is unfortunate that the term "saturation" refers to completely different regions in MOS and bipolar I-V characteristics.

BAUH moment ←

We employ the conceptual illustration in Fig. 6.22 to determine the region of operation. Note that the gate-drain potential difference suits this purpose and we need not compute the gate-source and gate-drain voltages separately.



Por qué en esta fórmula no está Vds? Que tarado, no es la fórmula de la parábola, es el valor de la Id de saturación

Figure 6.22 Illustration of triode and saturation regions based on the gate and drain voltages.

Exhibiting a "flat" current in the saturation region, a MOSFET can operate as a current source having a value given by Eq. (6.17). Furthermore, the square-law dependence of I_D upon $V_{GS} - V_{TH}$ suggests that the device can act as a voltage-controlled current source.

Example 6.6

Calculate the bias current of M_1 in Fig. 6.23. Assume $\mu_n C_{ox} = 100\,\mu\text{A/V}^2$ and $V_{TH} = 0.4$ V. If the gate voltage increases by 10 mV, what is the change in the drain voltage?

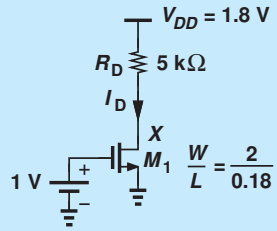


Figure 6.23 Simple MOS circuit.

Solution

It is unclear a priori in which region M_1 operates. Let us assume M_1 is saturated and proceed. Since $V_{GS} = 1$ V,

$$I_D = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{GS} - V_{TH})^2 \tag{6.18}$$

$$= 200\,\mu\text{A}. \tag{6.19}$$

We must check our assumption by calculating the drain potential:

$$V_X = V_{DD} - R_D I_D \tag{6.20}$$

$$= 0.8\,\text{V}. \tag{6.21}$$

The drain voltage is lower than the gate voltage, but by less than V_{TH}. The illustration in Fig. 6.22 therefore indicates that M_1 indeed operates in saturation.

If the gate voltage increases to 1.01 V, then

$$I_D = 206.7\,\mu\text{A}, \tag{6.22}$$

lowering V_X to

$$V_X = 0.766\,\text{V}. \tag{6.23}$$

Fortunately, M_1 is still saturated. The 34-mV change in V_X reveals that the circuit can *amplify* the input.

Exercise What choice of R_D places the transistor at the edge of the triode region?

Comparación MOSFET vs. TBJ

It is instructive to identify several points of contrast between bipolar and MOS devices. (1) A bipolar transistor with $V_{BE} = V_{CE}$ resides at the edge of the active region whereas a MOSFET approaches the edge of saturation if its drain voltage falls below its gate voltage by V_{TH}. (2) Bipolar devices exhibit an exponential I_C-V_{BE} characteristic while MOSFETs display a square-law dependence. That is, the former provide a greater transconductance than the latter (for a given bias current). (3) In bipolar circuits, most transistors have the same dimensions and hence the same I_S, whereas in MOS circuits, the aspect ratio of each device may be chosen differently to satisfy the design requirements. (4) The gate of MOSFETs draws no bias current.[9]

$V_D < V_{G-th}$

(Con S = GND)

Example 6.7

Determine the value of W/L in Fig. 6.23 that places M_1 at the edge of saturation and calculate the drain voltage change for a 1-mV change at the gate. Assume $V_{TH} = 0.4\,\text{V}$.

Solution

With $V_{GS} = +1\,\text{V}$, the drain voltage must fall to $V_{GS} - V_{TH} = 0.6\,\text{V}$ for M_1 to enter the triode region. That is,

$$I_D = \frac{V_{DD} - V_{DS}}{R_D} \tag{6.24}$$

$$= 240\,\mu\text{A}. \tag{6.25}$$

Since I_D scales linearly with W/L,

$$\left.\frac{W}{L}\right|_{max} = \frac{240\,\mu\text{A}}{200\,\mu\text{A}} \cdot \frac{2}{0.18} \tag{6.26}$$

$$= \frac{2.4}{0.18}. \tag{6.27}$$

If V_{GS} increases by 1 mV,

$$I_D = 248.04\,\mu\text{A}, \tag{6.28}$$

changing V_X by

$$\Delta V_X = \Delta I_D \cdot R_D \tag{6.29}$$

$$= 4.02\,\text{mV}. \tag{6.30}$$

The voltage gain is thus equal to 4.02 in this case.

Exercise Repeat the above example if R_D is doubled.

[9]New generations of MOSFETs suffer from gate "leakage" current, but we neglect this effect here.

Example 6.8

Calculate the maximum allowable gate voltage in Fig. 6.24 if M_1 must remain saturated.

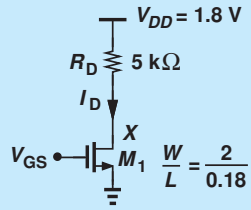


Figure 6.24 Simple MOS circuit.

Solution At the edge of saturation, $V_{GS} - V_{TH} = V_{DS} = V_{DD} - R_D I_D$. Substituting for I_D from Eq. (6.17) gives

$$V_{GS} - V_{TH} = V_{DD} - \frac{R_D}{2}\mu_n C_{ox}\frac{W}{L}(V_{GS} - V_{TH})^2, \tag{6.31}$$

and hence

$$V_{GS} - V_{TH} = \frac{-1 + \sqrt{1 + 2R_D V_{DD}\mu_n C_{ox}\frac{W}{L}}}{R_D \mu_n C_{ox}\frac{W}{L}}. \tag{6.32}$$

Thus,

$$V_{GS} = \frac{-1 + \sqrt{1 + 2R_D V_{DD}\mu_n C_{ox}\frac{W}{L}}}{R_D \mu_n C_{ox}\frac{W}{L}} + V_{TH}. \tag{6.33}$$

Exercise Calculate the value of V_{GS} if $\mu_n C_{ox} = 100\,\mu\text{A/V}^2$ and $V_{TH} = 0.4$.

6.2.3 Channel-Length Modulation

In our study of the pinch-off effect, we observed that the point at which the channel vanishes in fact moves toward the source as the drain voltage increases. In other words, the value of L_1 in Fig. 6.12(b) varies with V_{DS} to some extent. Called "channel-length modulation" and illustrated in Fig. 6.25, this phenomenon yields a larger drain current as V_{DS} increases because $I_D \propto 1/L_1$ in Eq. (6.17). Similar to the Early effect in bipolar devices,

Como en tbj, no es del todo cierto que la corriente de salida (Id) no dependa de la tensión de salida (Vds)

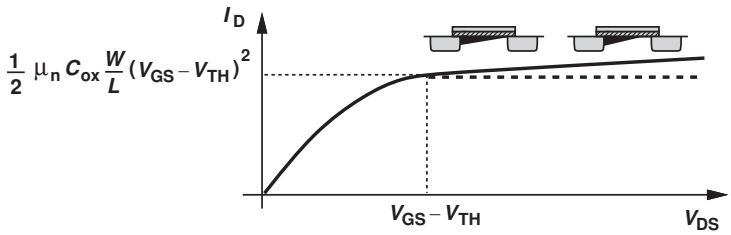


Figure 6.25 Variation of I_D in saturation region.

channel-length modulation results in a finite output impedance given by the inverse of the I_D-V_{DS} slope in Fig. 6.25.

To account for channel-length modulation, we assume L is constant, but multiply the right-hand side of Eq. (6.17) by a corrective term:

$$I_D = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{GS} - V_{TH})^2(1 + \lambda V_{DS}), \tag{6.34}$$

where λ is called the "channel-length modulation coefficient." While only an approximation, this linear dependence of I_D upon V_{DS} still provides a great deal of insight into the circuit design implications of channel-length modulation.

Unlike the Early effect in bipolar devices (Chapter 4), the amount of channel-length modulation is under the circuit designer's control. This is because λ is inversely proportional to L: for a longer channel, the *relative* change in L (and hence in I_D) for a given change in V_{DS} is smaller (Fig. 6.26).[10] (By contrast, the base width of bipolar devices cannot be adjusted by the circuit designer, yielding a constant Early voltage for all transistors in a given technology.)

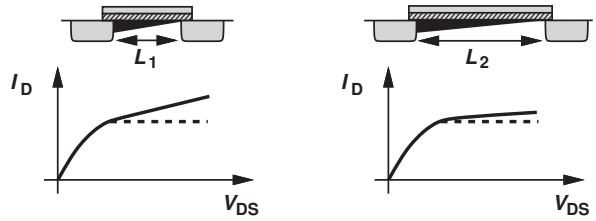


Figure 6.26 Channel-length modulation.

Example 6.9

A MOSFET carries a drain current of 1 mA with $V_{DS} = 0.5$ V in saturation. Determine the change in I_D if V_{DS} rises to 1 V and $\lambda = 0.1\ \text{V}^{-1}$. What is the device output impedance?

Solution

We write

$$I_{D1} = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{GS} - V_{TH})^2(1 + \lambda V_{DS1}) \tag{6.35}$$

$$I_{D2} = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{GS} - V_{TH})^2(1 + \lambda V_{DS2}) \tag{6.36}$$

and hence

$$I_{D2} = I_{D1}\frac{1 + \lambda V_{DS2}}{1 + \lambda V_{DS1}}. \tag{6.37}$$

With $I_{D1} = 1$ mA, $V_{DS1} = 0.5$ V, $V_{DS2} = 1$ V, and $\lambda = 0.1\ \text{V}^{-1}$,

$$I_{D2} = 1.048\ \text{mA}. \tag{6.38}$$

[10]Since different MOSFETs in a circuit may be sized for different λ's, we do not define a quantity similar to the Early voltage here.

The change in I_D is therefore equal to 48 μA, yielding an output impedance of

$$r_O = \frac{\Delta V_{DS}}{\Delta I_D} \tag{6.39}$$

$$= 10.42\,\text{k}\Omega. \tag{6.40}$$

Exercise Does W affect the above results?

The above example reveals that channel-length modulation limits the output impedance of MOS current sources. The same effect was observed for bipolar current sources in Chapters 4 and 5.

Example 6.10 Assuming $\lambda \propto 1/L$, calculate ΔI_D and r_O in Example 6.9 if both W and L are doubled.

Solution In Eqs. (6.35) and (6.36), W/L remains unchanged but λ drops to 0.05 V^{-1}. Thus,

$$I_{D2} = I_{D1}\frac{1+\lambda V_{DS2}}{1+\lambda V_{DS1}} \tag{6.41}$$

$$= 1.024\,\text{mA}. \tag{6.42}$$

That is, $\Delta I_D = 24\,\mu$A and

$$r_O = 20.84\,\text{k}\Omega. \tag{6.43}$$

Exercise What output impedance is achieved if W and L are quadrupled and I_D is halved?

6.2.4 MOS Transconductance

As a voltage-controlled current source, a MOS transistor can be characterized by its transconductance:

$$g_m = \frac{\partial I_D}{\partial V_{GS}}. \tag{6.44}$$

SALIDA

Entrada

This quantity serves as a measure of the "strength" of the device: a higher value corresponds to a greater change in the drain current for a given change in V_{GS}. Using Eq. (6.17) for the saturation region, we have

$$g_m = \mu_n C_{ox}\frac{W}{L}(V_{GS} - V_{TH}), \tag{6.45}$$

concluding that (1) g_m is linearly proportional to W/L for a given $V_{GS} - V_{TH}$, and (2) g_m is linearly proportional to $V_{GS} - V_{TH}$ for a given W/L. Also, substituting for $V_{GS} - V_{TH}$ from Eq. (6.17), we obtain

$$g_m = \sqrt{2\mu_n C_{ox}\frac{W}{L}I_D}. \tag{6.46}$$

TABLE 6.1 Various dependencies of g_m.

$\frac{W}{L}$ Constant $V_{GS} - V_{TH}$ Variable	$\frac{W}{L}$ Variable $V_{GS} - V_{TH}$ Constant	$\frac{W}{L}$ Variable $V_{GS} - V_{TH}$ Constant
$g_m \propto \sqrt{I_D}$	$g_m \propto I_D$	$g_m \propto \sqrt{\frac{W}{L}}$
$g_m \propto V_{GS} - V_{TH}$	$g_m \propto \frac{W}{L}$	$g_m \propto \frac{1}{V_{GS} - V_{TH}}$

¿contradictorio?

(Eq. 6.45) (Eq. 6.46)

That is, (1) g_m is proportional to $\sqrt{W/L}$ for a given I_D, and (2) g_m is proportional to $\sqrt{I_D}$ for a given W/L. Moreover, dividing Eq. (6.45) by (6.17) gives

$$g_m = \frac{2I_D}{V_{GS} - V_{TH}}, \tag{6.47}$$

revealing that (1) g_m is linearly proportional to I_D for a given $V_{GS} - V_{TH}$, and (2) g_m is inversely proportional to $V_{GS} - V_{TH}$ for a given I_D. Summarized in Table 6.1, these dependencies prove critical in understanding performance trends of MOS devices and have no counterpart in bipolar transistors.[11] Among these three expressions for g_m, Eq. (6.46) is more frequently used because I_D may be predetermined by power dissipation requirements.

Example 6.11 For a MOSFET operating in saturation, how do g_m and $V_{GS} - V_{TH}$ change if both W/L and I_D are doubled?

Solution Equation (6.46) indicates that g_m is also doubled. Moreover, Eq. (6.17) suggests that the overdrive remains constant. These results can be understood intuitively if we view the doubling of W/L and I_D as shown in Fig. 6.27. Indeed, if V_{GS} remains constant and the width of the device is doubled, it is as if two transistors carrying equal currents are placed in parallel, thereby doubling the transconductance. The reader can show that this trend applies to any type of transistor.

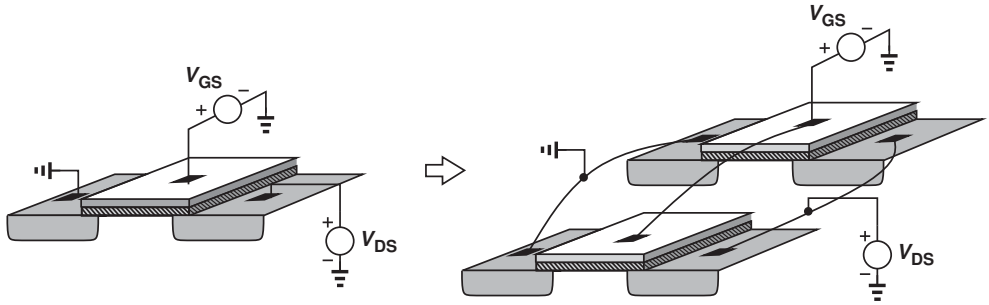


Figure 6.27 Equivalence of a wide MOSFET to two in parallel.

Exercise How do g_m and $V_{GS} - V_{TH}$ change if only W and I_D are doubled?

[11] There is some resemblance between the second column and the behavior of $g_m = I_C/V_T$. If the bipolar transistor width is increased while V_{BE} remains constant, then both I_C and g_m increase linearly.

6.2.5 Velocity Saturation*

Recall from Section 2.1.3 that at high electric fields, carrier mobility degrades, eventually leading to a *constant* velocity. Owing to their very short channels (e.g., 0.1 μm), modern MOS devices experience velocity saturation even with drain-source voltages as low as 1 V. As a result, the I/V characteristics no longer follow the square-law behavior.

Let us examine the derivations in Section 6.2.2 under velocity saturation conditions. Denoting the saturated velocity by v_{sat}, we have

$$I_D = v_{sat} \cdot Q \tag{6.48}$$

$$= v_{sat} \cdot WC_{ox}(V_{GS} - V_{TH}). \tag{6.49}$$

Interestingly, I_D now exhibits a *linear* dependence on $V_{GS} - V_{TH}$ and no dependence on L.[12] We also recognize that

$$g_m = \frac{\partial I_D}{\partial V_{GS}} \tag{6.50}$$

$$= v_{sat} WC_{ox}, \tag{6.51}$$

a quantity independent of L and I_D.

6.2.6 Other Second-Order Effects

Body Effect In our study of MOSFETs, we have assumed that both the source and the substrate (also called the "bulk" or the "body") are tied to ground. However, this condition need not hold in all circuits. For example, if the source terminal rises to a positive voltage while the substrate is at zero, then the source-substrate junction remains reverse-biased and the device still operates properly.

Figure 6.28 illustrates this case. The source terminal is tied to a potential V_S with respect to ground while the substrate is grounded through a p^+ contact.[13] The dashed line added to the transistor symbol indicates the substrate terminal. We denote the voltage difference between the source and the substrate (the bulk) by V_{SB}.

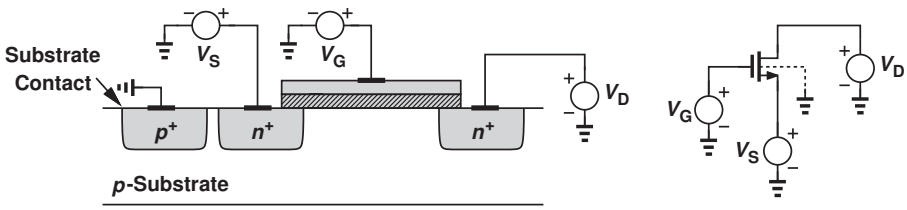


Figure 6.28 Body effect.

*This section can be skipped in a first reading.

[12]Of course, if L is increased substantially, while V_{DS} remains constant, then the device experiences less velocity saturation and Eq. (6.49) is not accurate.

[13]The p^+ island is necessary to achieve an "ohmic" contact with low resistance.

An interesting phenomenon occurs as the source-substrate potential difference departs from zero: the threshold voltage of the device *changes*. In particular, as the source becomes more positive with respect to the substrate, V_{TH} *increases*. Called "body effect," this phenomenon is formulated as

Un reconfortante galeraso

$$V_{TH} = V_{TH0} + \gamma(\sqrt{|2\phi_F + V_{SB}|} - \sqrt{|2\phi_F|}), \tag{6.52}$$

where V_{TH0} denotes the threshold voltage with $V_{SB} = 0$ (as studied earlier), and γ and ϕ_F are technology-dependent parameters having typical values of $0.4\sqrt{\text{V}}$ and 0.4 V, respectively.

Example 6.12 In the circuit of Fig. 6.28, assume $V_S = 0.5$ V, $V_G = V_D = 1.4$ V, $\mu_n C_{ox} = 100\,\mu\text{A/V}^2$, $W/L = 50$, and $V_{TH0} = 0.6$ V. Determine the drain current if $\lambda = 0$.

Solution Since the source-body voltage, $V_{SB} = 0.5$ V, Eq. (6.52) and the typical values for γ and ϕ_F yield

$$V_{TH} = 0.698 \text{ V}. \tag{6.53}$$

Also, with $V_G = V_D$, the device operates in saturation (why?) and hence

$$I_D = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_G - V_S - V_{TH})^2 \tag{6.54}$$

$$= 102\,\mu\text{A}. \tag{6.55}$$

Exercise Sketch the drain current as a function of V_S as V_S goes from zero to 1 V.

Body effect manifests itself in some analog and digital circuits and is studied in more advanced texts. We neglect body effect in this book.

Curioso. Canal inducido/Canal preformado?

Subthreshold Conduction The derivation of the MOS I-V characteristic has assumed that the transistor abruptly turns on as V_{GS} reaches V_{TH}. In reality, formation of the channel is a gradual effect, and the device conducts a small current even for $V_{GS} < V_{TH}$. Called "subthreshold conduction," this effect has become a critical issue in modern MOS devices and is studied in more advanced texts.

6.3 MOS DEVICE MODELS

With our study of MOS I-V characteristics in the previous section, we now develop models that can be used in circuit analysis and design.

6.3.1 Large-Signal Model

For arbitrary voltage and current levels, we must resort to Eqs. (6.9) and (6.34) to express the device behavior:

$$I_D = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}[2(V_{GS} - V_{TH})V_{DS} - V_{DS}^2] \quad \text{Triode Region} \tag{6.56}$$

$$I_D = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{GS} - V_{TH})^2(1 + \lambda V_{DS}) \quad \text{Saturation Region} \tag{6.57}$$

Una fuente de corriente ideal no depende de la tensión entre sus terminales, así que el transistor en triodo NO es una fuente de corriente ideal. En saturación tampoco, a menos que se desprecie el EMLC

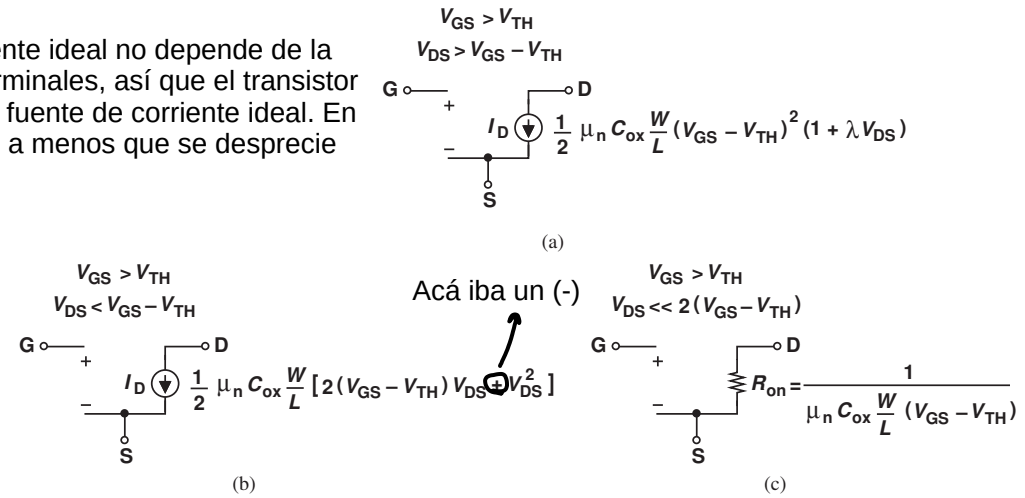


Figure 6.29 MOS models for (a) saturation region, (b) triode region, (c) deep triode region.

In the saturation region, the transistor acts as a voltage-controlled current source, lending itself to the model shown in Fig. 6.29(a). Note that I_D does depend on V_{DS} and is therefore not an ideal current source. For $V_{DS} < V_{GS} - V_{TH}$, the model must reflect the triode region, but it can still incorporate a voltage-controlled current source, as depicted in Fig. 6.29(b). Finally, if $V_{DS} \ll 2(V_{GS} - V_{TH})$, the transistor can be viewed as a voltage-controlled resistor [Fig. 6.29(c)]. In all three cases, the gate remains an open circuit to represent the zero gate current.

Example 6.13

Sketch the drain current of M_1 in Fig. 6.30(a) versus V_1 as V_1 varies from zero to V_{DD}. Assume $\lambda = 0$.

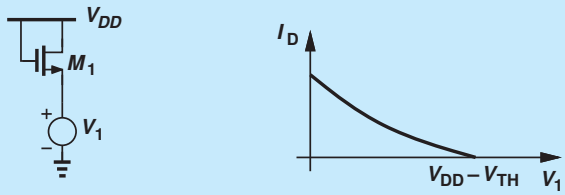


Figure 6.30 (a) Simple MOS circuit, (b) variation of I_D with V_1.

Solution Noting that the device operates in saturation (why?), we write

$$I_D = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{GS} - V_{TH})^2 \tag{6.58}$$

$$= \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{DD} - V_1 - V_{TH})^2. \tag{6.59}$$

At $V_1 = 0$, $V_{GS} = V_{DD}$ and the device carries maximum current. As V_1 rises, V_{GS} falls and so does I_D. If V_1 reaches $V_{DD} - V_{TH}$, V_{GS} drops to V_{TH}, turning the transistor off. The drain current thus varies as illustrated in Fig. 6.30(b). Note that, owing to body effect, V_{TH} *varies* with V_1 if the substrate is tied to ground.

Exercise Repeat the above example if the gate of M_1 is tied to a voltage equal to 1.5 V and $V_{DD} = 2$ V.

6.3.2 Small-Signal Model

If the bias currents and voltages of a MOSFET are only slightly disturbed by signals, the nonlinear, large-signal models can be reduced to linear, small-signal representations. The development of the model proceeds in a manner similar to that in Chapter 4 for bipolar devices. Of particular interest to us in this book is the small-signal model for the saturation region.

Viewing the transistor as a voltage-controlled current source, we draw the basic model as in Fig. 6.31(a), where $i_D = g_m v_{GS}$ and the gate remains open. To represent channel-length modulation, i.e., variation of i_D with v_{DS}, we add a resistor as in Fig. 6.31(b):

$$r_O = \left(\frac{\partial I_D}{\partial V_{DS}}\right)^{-1} \tag{6.60}$$

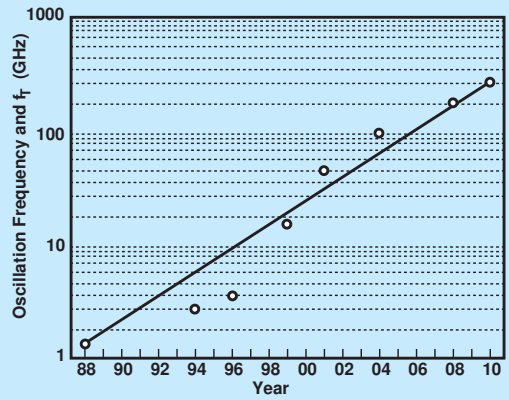
$$= \frac{1}{\left[\frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{GS} - V_{TH})^2\right]\lambda}. \tag{6.61}$$

Since channel-length modulation is relatively small, the denominator of Eq. (6.61) can be approximated as $I_D \cdot \lambda$, yielding

$$r_O \approx \frac{1}{\lambda I_D}. \tag{6.62}$$

Did you know?

In addition to integrating a larger number of transistors per chip, MOS technology has also benefited tremendously from "scaling," i.e., the reduction of the transistors' dimensions. The minimum channel length has fallen from about 10 μm to about 25 nm today and the speed of MOSFETs has improved by more than 4 orders of magnitude. For example, the clock frequency of Intel's microprocessors has risen from 100 kHz to 4 GHz. But have analog circuits taken advantage of the scaling as well? Yes, indeed. Plotted below is the frequency of MOS oscillators as a function of time over the past three decades.



MOS oscillator frequency as a function of time.

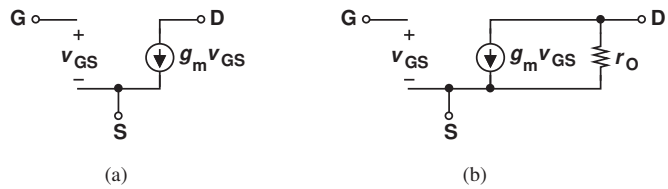


Figure 6.31 (a) Small-signal model of MOSFET, (b) inclusion of channel-length modulation.

Example 6.14

A MOSFET is biased at a drain current of 0.5 mA. If $\mu_n C_{ox} = 100\,\mu\text{A/V}^2$, $W/L = 10$, and $\lambda = 0.1\,\text{V}^{-1}$, calculate its small-signal parameters.

Solution

We have

$$g_m = \sqrt{2\mu_n C_{ox}\frac{W}{L}I_D} \tag{6.63}$$

$$= \frac{1}{1\,\text{k}\Omega}. \tag{6.64}$$

Also,

$$r_O = \frac{1}{\lambda I_D} \tag{6.65}$$

$$= 20\,\text{k}\Omega. \tag{6.66}$$

This means that the intrinsic gain, $g_m r_O$ (Chapter 4), is equal to 20 for this choice of device dimensions and bias current.

Exercise Repeat the above example if W/L is doubled.

6.4 PMOS TRANSISTOR

Having seen both *npn* and *pnp* bipolar transistors, the reader may wonder if a *p*-type counterpart exists for MOSFETs. Indeed, as illustrated in Fig. 6.32(a), changing the doping polarities of the substrate and the S/D areas results in a "PMOS" device. The channel now consists of *holes* and is formed if the gate voltage is *below* the source potential by one threshold voltage. That is, to turn the device on, $V_{GS} < V_{TH}$, where V_{TH} itself is negative. Following the conventions used for bipolar devices, we draw the PMOS device as in Fig. 6.32(b), with the source terminal identified by the arrow and placed

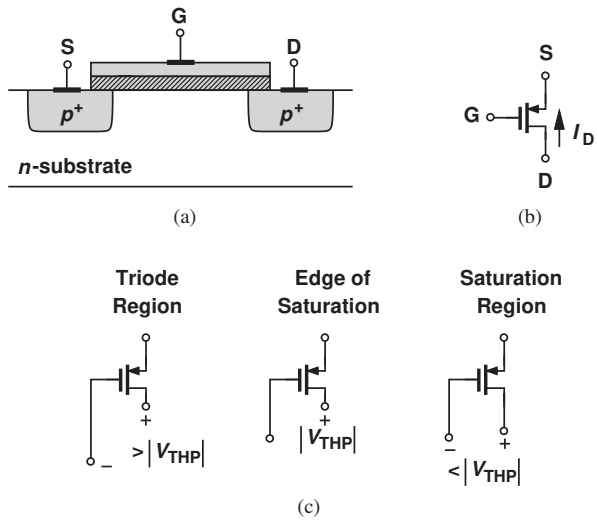


Figure 6.32 (a) Structure of PMOS device, (b) PMOS circuit symbol, (c) illustration of triode and saturation regions based on gate and drain voltages.

on top to emphasize its higher potential. The transistor operates in the triode region if the drain voltage is near the source potential, approaching saturation as V_D falls to $V_G - V_{TH} = V_G + |V_{TH}|$. Figure 6.32(c) conceptually illustrates the gate-drain voltages required for each region of operation. We say that if V_{DS} of a PMOS (NMOS) device is sufficiently negative (positive), then it is in saturation.

Example 6.15

In the circuit of Fig. 6.33, determine the region of operation of M_1 as V_1 goes from V_{DD} to zero. Assume $V_{DD} = 2.5$ V and $|V_{TH}| = 0.5$ V.

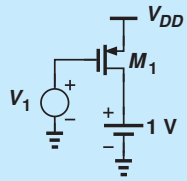


Figure 6.33 Simple PMOS circuit.

Solution

For $V_1 = V_{DD}$, $V_{GS} = 0$ and M_1 is off. As V_1 falls and approaches $V_{DD} - |V_{TH}|$, the gate-source potential is negative enough to form a channel of holes, turning the device on. At this point, $V_G = V_{DD} - |V_{TH}| = +2$ V while $V_D = +1$ V; i.e., M_1 is saturated [Fig. 6.32(c)]. As V_1 falls further, V_{GS} becomes more negative and the transistor current rises. For $V_1 = +1\text{ V} - |V_{TH}| = 0.5$ V, M_1 is at the edge of the triode region. As V_1 goes below 0.5 V, the transistor enters the triode region further.

Formulas del P-Mos

En P(+) mos, ID < 0
En N(-) mos, ID>0

Todo al revés
Una vez más, uno entrega corriente y el otro la absorbe

The voltage and current polarities in PMOS devices can prove confusing. Using the current direction shown in Fig. 6.32(b), we express I_D in the saturation region as

$$I_{D,sat} = -\frac{1}{2}\mu_p C_{ox}\frac{W}{L}(V_{GS} - V_{TH})^2(1 - \lambda V_{DS}), \tag{6.67}$$

where λ is multiplied by a negative sign.[14] In the triode region,

$$I_{D,tri} = -\frac{1}{2}\mu_p C_{ox}\frac{W}{L}\left[2(V_{GS} - V_{TH})V_{DS} - V_{DS}^2\right]. \tag{6.68}$$

Alternatively, both equations can be expressed in terms of absolute values:

$$|I_{D,sat}| = \frac{1}{2}\mu_p C_{ox}\frac{W}{L}(|V_{GS}| - |V_{TH}|)^2(1 + \lambda|V_{DS}|) \tag{6.69}$$

$$|I_{D,tri}| = \frac{1}{2}\mu_p C_{ox}\frac{W}{L}\left[2(|V_{GS}| - |V_{TH}|)|V_{DS}| - V_{DS}^2\right]. \tag{6.70}$$

The small-signal model of PMOS transistor is identical to that of NMOS devices (Fig. 6.31). The following example illustrates this point.

[14] To make this equation more consistent with that of NMOS devices [Eq. (6.34)], we can define λ itself to be negative and express I_D as $(1/2)\mu_p C_{ox}(W/L)(V_{GS} - V_{TH})^2(1 + \lambda V_{DS})$. But a negative λ carries little physical meaning.

Example 6.16

For the configurations shown in Fig. 6.34(a), determine the small-signal resistances R_X and R_Y. Assume $\lambda \neq 0$.

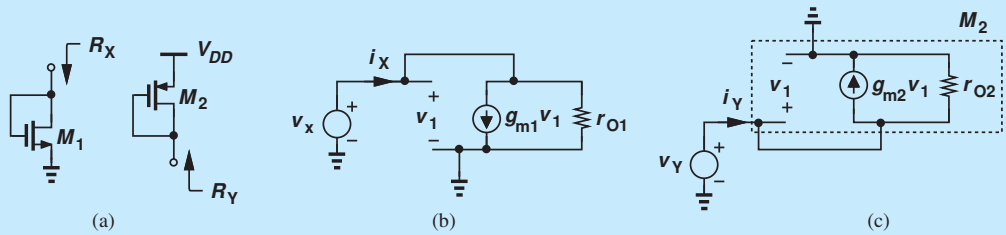


Figure 6.34 (a) Diode-connected NMOS and PMOS devices, (b) small-signal model of (a), (c) small-signal model of (b).

Solution For the NMOS version, the small-signal equivalent appears as depicted in Fig. 6.34(b), yielding

$$R_X = \frac{v_X}{i_X} \tag{6.71}$$

$$= \left(g_{m1}v_X + \frac{v_X}{r_{O1}}\right)\frac{1}{i_X} \tag{6.72}$$

$$= \frac{1}{g_{m1}} || r_{O1}. \tag{6.73}$$

For the PMOS version, we draw the equivalent as shown in Fig. 6.34(c) and write

$$R_Y = \frac{v_Y}{i_Y} \tag{6.74}$$

$$= \left(g_{m2}v_Y + \frac{v_Y}{r_{O1}}\right)\frac{1}{i_Y} \tag{6.75}$$

$$= \frac{1}{g_{m2}} || r_{O2}. \tag{6.76}$$

In both cases, the small-signal resistance is equal to $1/g_m$ if $\lambda \to 0$.

In analogy with their bipolar counterparts [Fig. 4.44(a)], the structures shown in Fig. 6.34(a) are called "diode-connected" devices and act as two-terminal components: we will encounter many applications of diode-connected devices in Chapters 9 and 10.

Owing to the lower mobility of holes (Chapter 2), PMOS devices exhibit a poorer performance than NMOS transistors. For example, Eq. (6.46) indicates that the transconductance of a PMOS device is lower for a given drain current. We therefore prefer to use NMOS transistors wherever possible.

→ NMOS > PMOS, r_{O1} r_{O2}, x_d son iguales pero al cuadrado

6.5 CMOS TECHNOLOGY

Is it possible to build both NMOS and PMOS devices on the same wafer? Figures 6.2(a) and 6.32(a) reveal that the two require *different* types of substrate. Fortunately, a *local* n-type substrate can be created in a p-type substrate, thereby accommodating PMOS transistors.

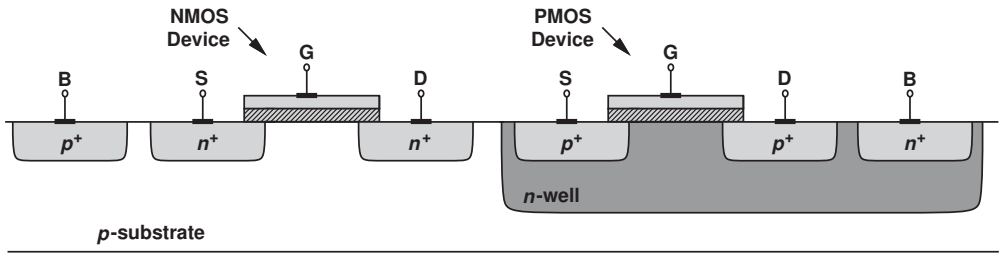


Figure 6.35 CMOS technology.

As illustrated in Fig. 6.35, an "*n*-well" encloses a PMOS device while the NMOS transistor resides in the *p*-substrate.

Called "complementary MOS" (CMOS) technology, the above structure requires more complex processing than simple NMOS or PMOS devices. In fact, the first few generations of MOS technology contained only NMOS transistors,[15] and the higher cost of CMOS processes seemed prohibitive. However, many significant advantages of complementary devices eventually made CMOS technology dominant and NMOS technology obsolete.

6.6 COMPARISON OF BIPOLAR AND MOS DEVICES

Having studied the physics and operation of bipolar and MOS transistors, we can now compare their properties. Table 6.2 shows some of the important aspects of each device. Note that the exponential I_C-V_{BE} dependence of bipolar devices accords them a higher transconductance for a given bias current.

$g_m(\text{TBJ}) \gg g_m(\text{MOS})$

TABLE 6.2 Comparison of bipolar and MOS transistors.

Bipolar Transistor	MOSFET
Exponential Characteristic	Quadratic Characteristic
Active: $V_{CB} > 0$	Saturation: $V_{DS} > V_{GS} - V_{TH}$ (NMOS)
Saturation: $V_{CB} < 0$	Triode: $V_{DS} < V_{GS} - V_{TH}$ (NMOS)
Finite Base Current	Zero Gate Current
Early Effect	Channel-Length Modulation
Diffusion Current	Drift Current
—	Voltage-Dependent Resistor

Terminé de leer 1h y 20 min.

6.7 CHAPTER SUMMARY

- A voltage-dependent current source can form an amplifier along with a load resistor. MOSFETs are electronic devices that can operate as voltage-dependent current sources.
- A MOSFET consists of a conductive plate (the "gate") atop a semiconductor substrate and two junctions ("source" and "drain") in the substrate. The gate controls the current flow from the source to the drain. The gate draws nearly zero current because an insulating layer separates it from the substrate.

Cuánto me lleva hacer el apunte? Si me lleva más de 40 min, no hice más rápido que antes

Actualización: Tardé más de una hora xd

[15]The first Intel microprocessor, the 4004, was realized in NMOS technology.

- As the gate voltage rises, a depletion region is formed in the substrate under the gate area. Beyond a certain gate-source voltage (the "threshold voltage"), mobile carriers are attracted to the oxide-silicon interface and a channel is formed.
- If the drain-source voltage is small, the device operates a voltage-dependent resistor.
- As the drain voltage rises, the charge density near the drain falls. If the drain voltage reaches one threshold below the gate voltage, the channel ceases to exist near the drain, leading to "pinch-off."
- MOSFETs operate in the "triode" region if the drain voltage is more than one threshold below the gate voltage. In this region, the drain current is a function of V_{GS} and V_{DS}. The current is also proportional to the device aspect ratio, W/L.
- MOSFETs enter the "saturation region" if channel pinch-off occurs, i.e., the drain voltage is less than one threshold below the gate volatge. In this region, the drain current is proportional to $(V_{GS} - V_{TH})^2$.
- MOSFETs operating in the saturation region behave as current sources and find wide application in microelectronic circuits.
- As the drain voltage exceeds $V_{GS} - V_{TH}$ and pinch-off occurs, the drain end of the channel begins to move toward the source, reducing the effective length of the device. Called "channel-length modulation," this effect leads to variation of drain current in the saturation region. That is, the device is not an ideal current source.
- A measure of the small-signal performance of voltage-dependent current sources is the "transconductance," defined as the change in the output current divided by the change in the input voltage. The transconductance of MOSFETs can be expressed by one of three equations in terms of the bias voltages and currents.
- Operation across different regions and/or with large swings exemplifies "large-signal behavior." If the signal swings are sufficiently small, the MOSFET can be represented by a small-signal model consisting of a *linear* voltage-dependent current source and an output resistance.
- The small-signal model is derived by making a small change in the voltage difference between two terminals while the the other voltages remain constant.
- The small-signal models of NMOS and PMOS devices are identical.
- NMOS and PMOS transistors are fabricated on the same substrate to create CMOS technology.

PROBLEMS

In the following problems, unless otherwise stated, assume $\mu_n C_{ox} = 200\,\mu\text{A/V}^2$, $\mu_p C_{ox} = 100\,\mu\text{A/V}^2$, and $V_{TH} = 0.4\,\text{V}$ for NMOS devices and $-0.4\,\text{V}$ for PMOS devices.

Sec. 6.2 Operation of MOSFET

*6.1. Two identical MOSFETs are placed in series as shown in Fig. 6.36. If both devices operate as resistors, explain intuitively why this combination is equivalent to a single transistor, M_{eq}. What are the width and length of M_{eq}?

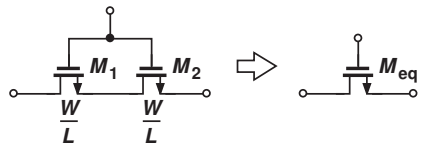


Figure 6.36

6.2. Referring to Fig. 6.11 and assuming that $V_D > 0$,
(a) Sketch the electron density in the channel as a function of x.
(b) Sketch the local resistance of the channel (per unit length) as a function of x.

6.3. Calculate the total charge stored in the channel of an NMOS device if $C_{ox} = 10\,\text{fF}/\mu\text{m}^2$, $W = 5\,\mu\text{m}$, $L = 0.1\,\mu\text{m}$, and $V_{GS} - V_{TH} = 1\,\text{V}$. Assume $V_{DS} = 0$.

*6.4. Consider a MOSFET experiencing pinch-off near the drain. Equation (6.4) indicates that the charge density and carrier velocity must change in opposite directions if the current remains constant. How can this relationship be interpreted at the pinch-off point, where the charge density approaches zero?

6.5. Assuming I_D is constant, solve Eq. (6.7) to obtain an expression for $V(x)$. Plot both $V(x)$ and dV/dx as a function of x for different values of W or V_{TH}.

*6.6. The drain current of a MOSFET in the triode region is expressed as

$$I_D = \mu_n C_{ox} \frac{W}{L}\left[(V_{GS} - V_{TH})V_{DS} - \frac{1}{2}V_{DS}^2\right]. \tag{6.77}$$

Suppose the values of $\mu_n C_{ox}$ and W/L are unknown. Is it possible to determine these quantities by applying different values of $V_{GS} - V_{TH}$ and V_{DS} and measuring I_D?

6.7. An NMOS device carries 1 mA with $V_{GS} - V_{TH} = 0.6\,\text{V}$ and 1.6 mA with $V_{GS} - V_{TH} = 0.8\,\text{V}$. If the device operates in the triode region, calculate V_{DS} and W/L.

*6.8. Compute the transconductance of a MOSFET operating in the triode region. Define $g_m = \partial I_D/\partial V_{GS}$ for a constant V_{DS}. Explain why $g_m = 0$ for $V_{DS} = 0$.

6.9. For a MOS transistor biased in the triode region, we can define an incremental drain-source resistance as

$$r_{DS,tri} = \left(\frac{\partial I_D}{\partial V_{DS}}\right)^{-1}. \tag{6.78}$$

Derive an expression for this quantity.

6.10. We wish to use an NMOS transistor as a variable resistor with $R_{on} = 500\,\Omega$ at $V_{GS} = 1\,\text{V}$ and $R_{on} = 400\,\Omega$ at $V_{GS} = 1.5\,\text{V}$. Explain why this is not possible.

6.11. An NMOS device operating with a small drain-source voltage serves as a resistor. If the supply voltage is 1.8 V, what is the minimum on-resistance that can be achieved with $W/L = 20$?

6.12. It is possible to define an "intrinsic time constant" for a MOSFET operating as a resistor:

$$\tau = R_{on}C_{GS}, \tag{6.79}$$

where $C_{GS} = WLC_{ox}$. Obtain an expression for τ and explain what the circuit designer must do to minimize the time constant.

6.13. In the circuit of Fig. 6.37, M_1 serves as an electronic switch. If $V_{in} \approx 0$, determine W/L such that the circuit attenuates the signal by only 5%. Assume $V_G = 1.8\,\text{V}$ and $R_L = 100\,\Omega$.

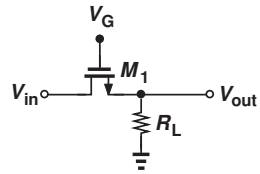


Figure 6.37

6.14. In the circuit of Fig. 6.37, the input is a small sinusoid superimposed on a dc level: $V_{in} = V_0\cos\omega t + V_1$, where V_0 is on the order of a few millivolts.
(a) For $V_1 = 0$, obtain W/L in terms of R_L and other parameters so that $V_{out} = 0.95V_{in}$.
(b) Repeat part (a) for $V_1 = 0.5\,\text{V}$. Compare the results.

6.15. For an NMOS device, plot I_D as a function of V_{GS} for different values of V_{DS}.

6.16. In Fig. 6.17, explain why the peaks of the parabolas lie on a parabola themselves.

6.17. For MOS devices with very short channel lengths, the square-law behavior is not valid, and we may instead write:

$$I_D = WC_{ox}(V_{GS} - V_{TH})v_{sat}, \tag{6.80}$$

where v_{sat} is a relatively *constant* velocity. Determine the transconductance of such a device.

6.18. Advanced MOS devices do not follow the square-law behavior expressed by Eq. (6.17). A somewhat better approximation is:

$$I_D = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{GS} - V_{TH})^{\alpha}, \qquad (6.81)$$

where α is less than 2. Determine the transconductance of such a device.

*__6.19.__ Determine the region of operation of M_1 in each of the circuits shown in Fig. 6.38.

*__6.20.__ Determine the region of operation of M_1 in each of the circuits shown in Fig. 6.39.

6.21. Two current sources realized by identical MOSFETs (Fig. 6.40) match to within 1%, i.e., $0.99I_{D2} < I_{D1} < 1.01I_{D2}$. If $V_{DS1} = 0.5\,\text{V}$ and $V_{DS2} = 1\,\text{V}$, what is the maximum tolerable value of λ?

6.22. Assume $\lambda = 0$, compute W/L of M_1 in Fig. 6.41 such that the device operates at the edge of saturation.

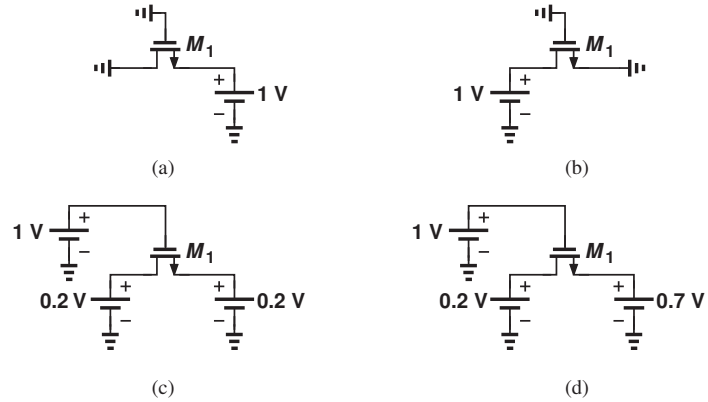


Figure 6.38

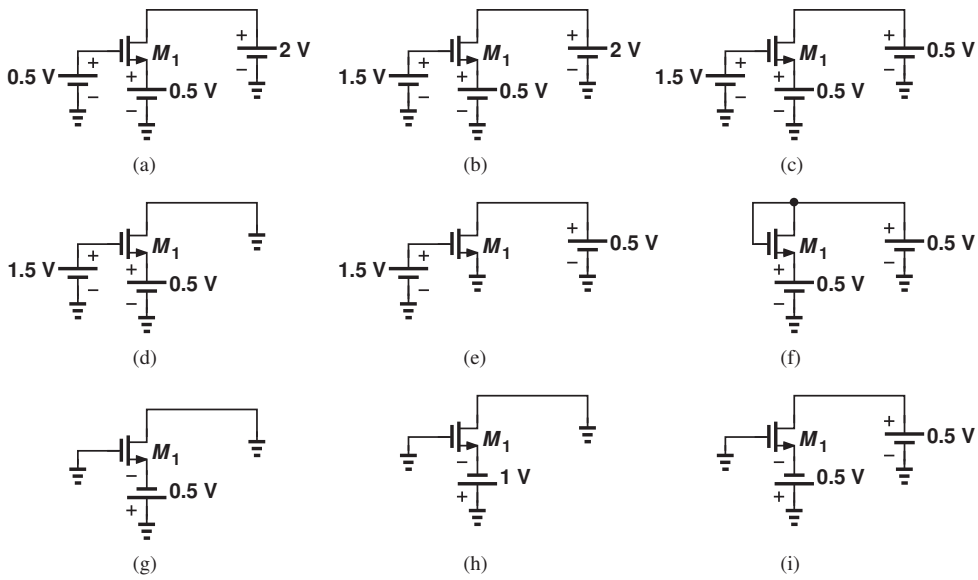


Figure 6.39

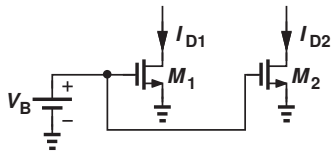


Figure 6.40

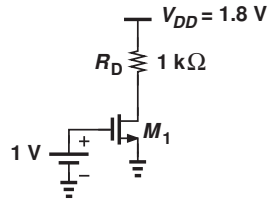


Figure 6.41

6.23. Using the value of W/L found in Problem 6.22, explain what happens if the gate oxide thickness is doubled due to a manufacturing error.

6.24. In the Fig. 6.42 ,what is the minimum allowable value of V_{DD} if M_1 must not enter the triode region? Assume $\lambda = 0$.

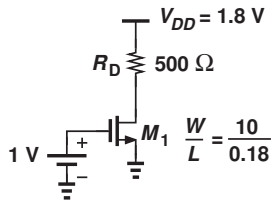


Figure 6.42

6.25. Calculate the bias current of M_1 in Fig. 6.43 if $\lambda = 0$.

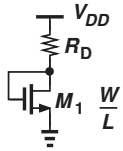


Figure 6.43

6.26. Compute the value of W/L for M_1 in Fig. 6.44 for a bias current of I_1. Assume $\lambda = 0$.

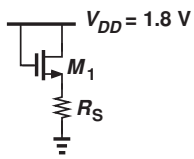


Figure 6.44

*6.27. In Fig. 6.45, derive a relationship among the circuit parameters that guarantees M_1 operates at the edge of saturation. Assume $\lambda = 0$.

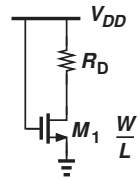


Figure 6.45

**6.28. Sketch I_X as a function of V_X for the circuits shown in Fig. 6.46. Assume V_X goes from 0 to $V_{DD} = 1.8$ V. Also, $\lambda = 0$. Determine at what value of V_X the device changes its region of operation.

6.29. Assuming $W/L = 10/0.18$ $\lambda = 0.1\ \text{V}^{-1}$, and $V_{DD} = 1.8$ V, calculate the drain current of M_1 in Fig. 6.47.

6.30. In the circuit of Fig. 6.48, $W/L = 20/0.18$ and $\lambda = 0.1\ \text{V}^{-1}$. What value of V_B places the transistor at the edge of saturation?

6.31. An NMOS device operating in saturation with $\lambda = 0$ must provide a transconductance of $1/(50\ \Omega)$.

(a) Determine W/L if $I_D = 0.5$ mA.

(b) Determine W/L if $V_{GS} - V_{TH} = 0.5$ V.

(c) Determine I_D if $V_{GS} - V_{TH} = 0.5$ V.

**6.32. Determine how the transconductance of a MOSFET (operating in saturation) changes if

(a) W/L is doubled but I_D remains constant.

(b) $V_{GS} - V_{TH}$ is doubled but I_D remains constant.

(c) I_D is doubled but W/L remains constant.

(d) I_D is doubled but $V_{GS} - V_{TH}$ remains constant.

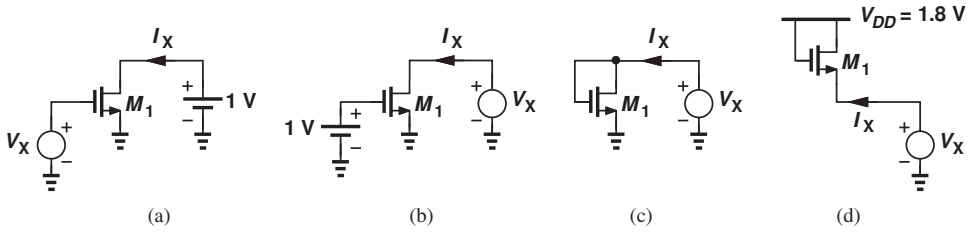


Figure 6.46

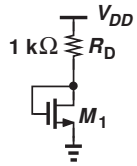


Figure 6.47

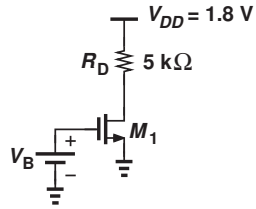


Figure 6.48

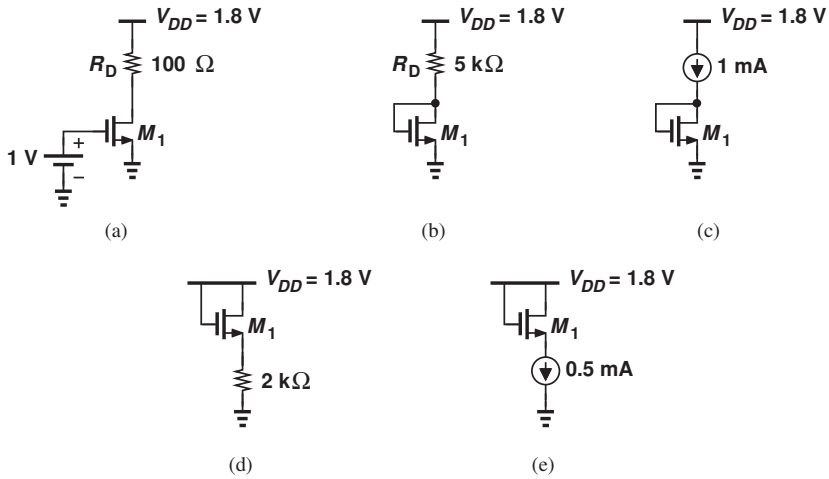


Figure 6.49

6.33. The "intrinsic gain" of a MOSFET operating in saturation is defined as $g_m r_O$. Derive an expression for $g_m r_O$ and plot the result as a function of I_D. Assume V_{DS} is constant.

6.34. If $\lambda = 0.1\,\text{V}^{-1}$ and $W/L = 20/0.18$, construct the small-signal model of each of the circuits shown in Fig. 6.49.

*__6.35.__ Assuming a constant V_{DS}, plot the intrinsic gain, $g_m r_O$, of a MOSFET
(a) as a function of $V_{GS} - V_{TH}$ if I_D is constant.
(b) as a function of I_D if $V_{GS} - V_{TH}$ is constant.

6.36. An NMOS device with $\lambda = 0.1\,\text{V}^{-1}$ must provide a $g_m r_O$ of 20 with $V_{DS} = 1.5\,\text{V}$. Determine the required value of W/L if $I_D = 0.5\,\text{mA}$.

6.37. Repeat Problem 6.36 for $\lambda = 0.2\,\text{V}^{-1}$.

6.38. Construct the small-signal model of the circuits depicted in Fig. 6.50. Assume all transistors operate in saturation and $\lambda \neq 0$.

Sec. 6.4 PMOS Transistor

*__6.39.__ Determine the region of operation of M_1 in each circuit shown in Fig. 6.51.

*__6.40.__ Determine the region of operation of M_1 in each circuit shown in Fig. 6.52.

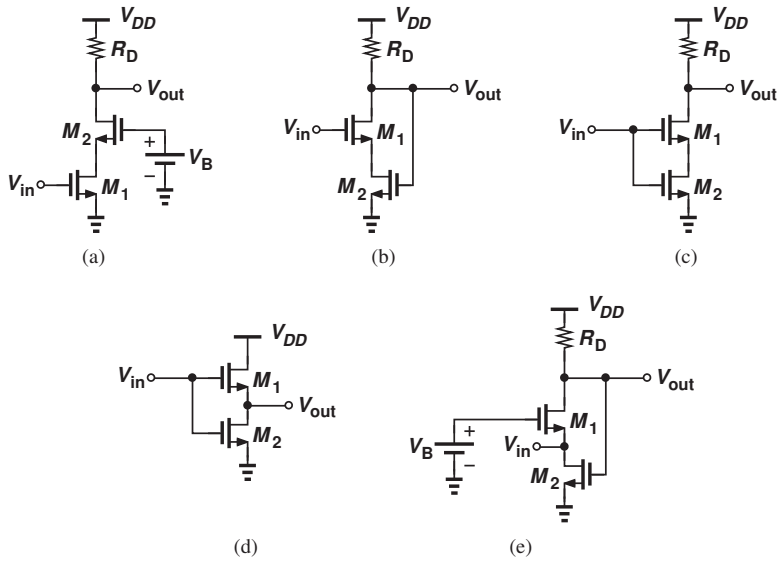


Figure 6.50

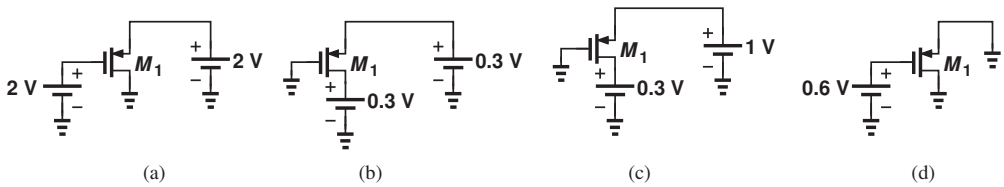


Figure 6.51

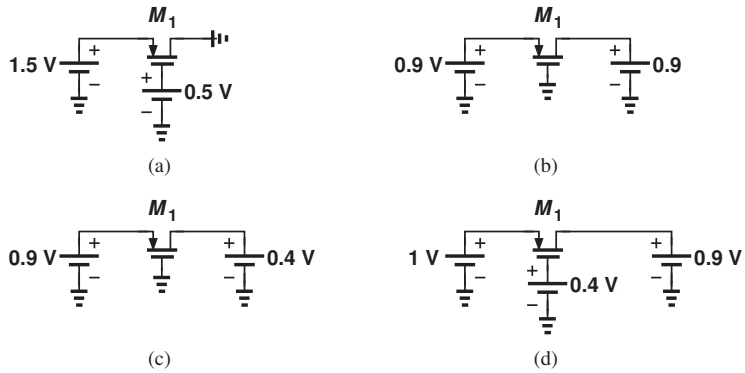


Figure 6.52

6.41. If $\lambda = 0$, what value of W/L places M_1 at the edge of saturation in Fig. 6.53?

6.42. With the value of W/L obtained in Problem 6.41, what happens if V_B changes to $+0.8$ V?

6.43. If $W/L = 10/0.18$ and $\lambda = 0$, determine the operating point of M_1 in each circuit depicted in Fig. 6.54.

6.44. Sketch I_X as a function of V_X for the circuits shown in Fig. 6.55. Assume V_X goes from 0 to $V_{DD} = 1.8$ V. Also, $\lambda = 0$. Determine at what value of V_X the device changes its region of operation.

6.45. Construct the small-signal model of each circuit shown in Fig. 6.56 if all of the transistors operate in saturation and $\lambda \neq 0$.

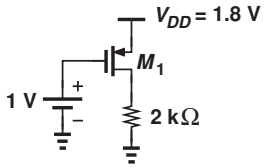


Figure 6.53

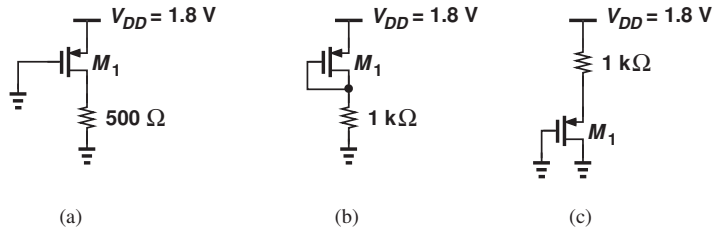


Figure 6.54

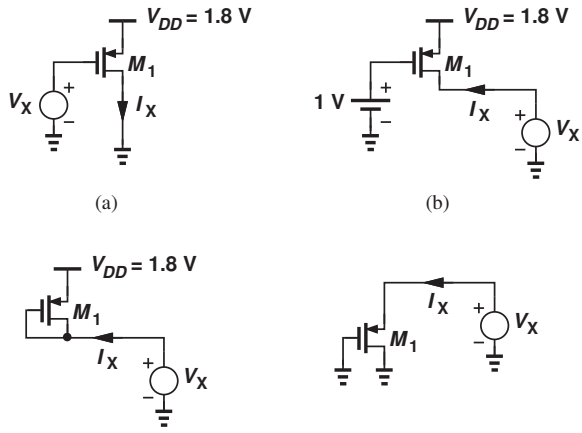


Figure 6.55

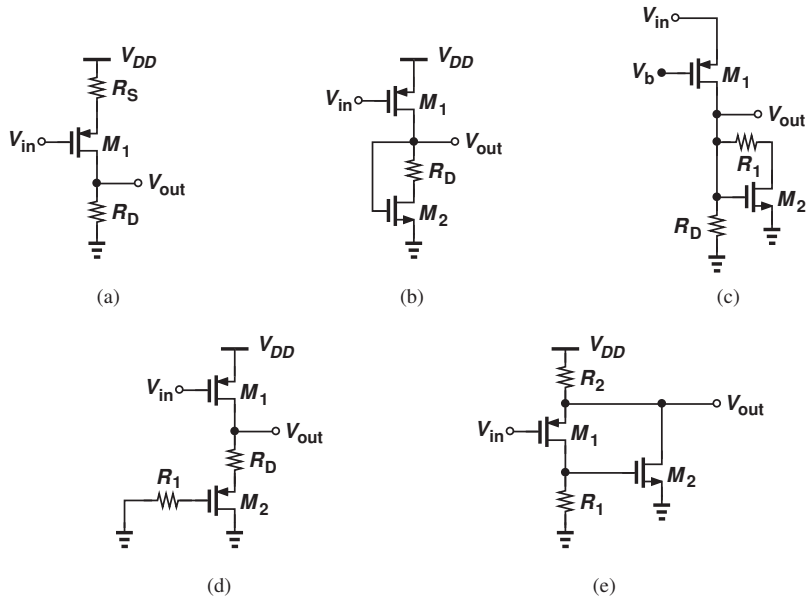


Figure 6.56

**6.46. Consider the circuit depicted in Fig. 6.57, where M_1 and M_2 operate in saturation and exhibit channel-length modulation coefficients λ_n and λ_p, respectively.

(a) Construct the small-signal equivalent circuit and explain why M_1 and M_2 appear in "parallel."

(b) Determine the small-signal voltage gain of the circuit.

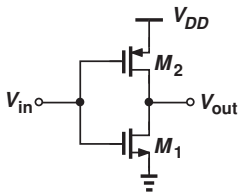


Figure 6.57

SPICE PROBLEMS

In the following problems, use the MOS models and source/drain dimensions given in Appendix A. Assume the substrates of NMOS and PMOS devices are tied to ground and V_{DD}, respectively.

6.47. For the circuit shown in Fig. 6.58, plot V_X as a function of I_X for $0 < I_X < 3$ mA. Explain the sharp change in V_X as I_X exceeds a certain value.

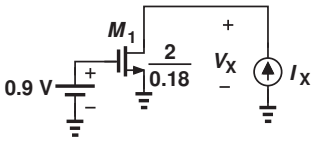


Figure 6.58

6.48. Plot the input/output characteristic of the stage shown in Fig. 6.59 for $0 < V_{in} < 1.8$ V. At what value of V_{in} does the slope (gain) reach a maximum?

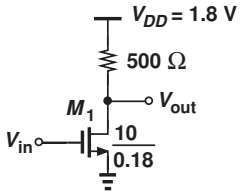


Figure 6.59

6.49. For the arrangements shown in Fig. 6.60, plot I_D as a function of V_X as V_X varies from 0 to 1.8 V. Can we say these two arrangements are equivalent?

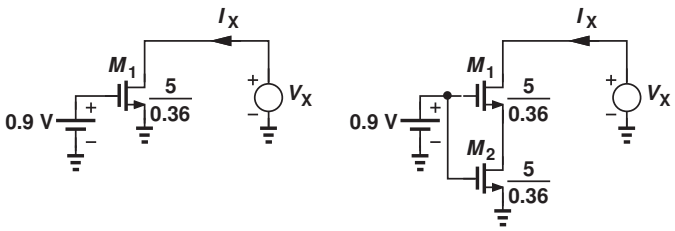


Figure 6.60

6.50. Plot I_X as a function of V_X for the arrangement depicted in Fig. 6.61 as V_X varies from 0 to 1.8 V. Can you explain the behavior of the circuit?

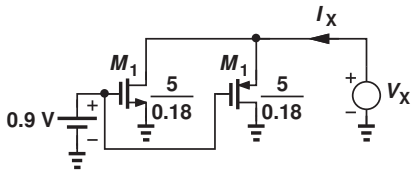


Figure 6.61

6.51. Repeat Problem 6.50 for the circuit illustrated in Fig. 6.62.

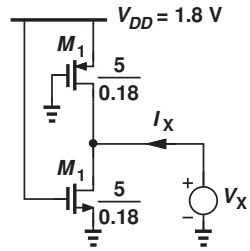


Figure 6.62