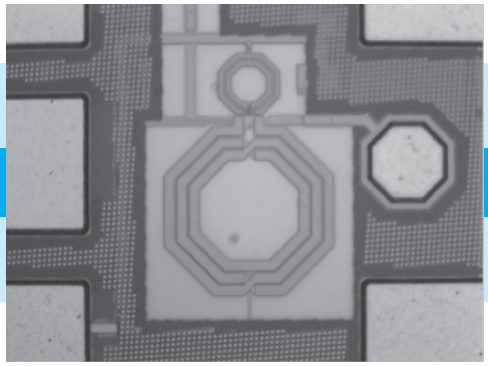


7

CMOS Amplifiers

Este fin de semana ya leí 4 capítulos de este libro, pero lo quiero terminar ya x favor

Most CMOS amplifiers have identical bipolar counterparts and can therefore be analyzed in the same fashion. Our study in this chapter parallels the developments in Chapter 5, identifying both similarities and differences between CMOS and bipolar circuit topologies. It is recommended that the reader review Chapter 5, specifically, Section 5.1. We assume the reader is familiar with concepts such as I/O impedances, biasing, and dc and small-signal analysis. The outline of the chapter is shown below.

General Concepts
- Biasing of MOS Stages
- Realization of Current Sources

➤

MOS Amplifiers
- Common–Source Stage
- Common–Gate Stage
- Source Follower

7.1 GENERAL CONSIDERATIONS

7.1.1 MOS Amplifier Topologies

Recall from Section 5.3 that the nine possible circuit topologies using a bipolar transistor in fact reduce to three useful configurations. The similarity of bipolar and MOS small-signal models (i.e., a voltage-controlled current source) suggests that the same must hold for MOS amplifiers. In other words, we expect three basic CMOS amplifiers: the "common-source" (CS) stage, the "common-gate" (CG) stage, and the "source follower."

7.1.2 Biasing

Depending on the application, MOS circuits may incorporate biasing techniques that are quite different from those described in Chapter 5 for bipolar stages. Most of these techniques are beyond the scope of this book and some methods are studied in Chapter 5. Nonetheless, it is still instructive to apply some of the biasing concepts of Chapter 5 to MOS stages.

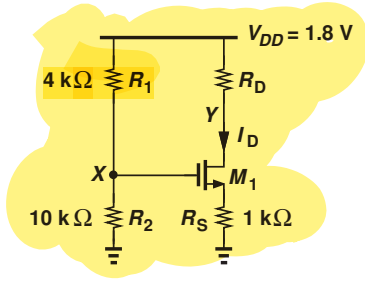


Figure 7.1 MOS stage with biasing.

Consider the circuit shown in Fig. 7.1, where the gate voltage is defined by R_1 and R_2. We assume M_1 operates in saturation. Also, in most bias calculations, we can neglect channel-length modulation. Noting that the gate current is zero, we have

$$V_X = \frac{R_2}{R_1 + R_2} V_{DD}. \tag{7.1}$$

No está el problema de aproximar $I_B \cong 0$

Since $V_X = V_{GS} + I_D R_S$,

$$\frac{R_2}{R_1 + R_2} V_{DD} = V_{GS} + I_D R_S. \tag{7.2}$$

Also,

$$I_D = \frac{1}{2} \mu_n C_{ox} \frac{W}{L} (V_{GS} - V_{TH})^2. \tag{7.3}$$

Equations (7.2) and (7.3) can be solved to obtain I_D and V_{GS}, either by iteration or by finding I_D from Eq. (7.2) and replacing for it in Eq. (7.3):

$$\left(\frac{R_2}{R_1 + R_2} V_{DD} - V_{GS} \right) \frac{1}{R_S} = \frac{1}{2} \mu_n C_{ox} \frac{W}{L} (V_{GS} - V_{TH})^2. \tag{7.4}$$

That is,

$$V_{GS} = -(V_1 - V_{TH}) + \sqrt{(V_1 - V_{TH})^2 - V_{TH}^2 + \frac{2R_2}{R_1 + R_2} V_1 V_{DD}}, \tag{7.5}$$

$$= -(V_1 - V_{TH}) + \sqrt{V_1^2 + 2V_1 \left(\frac{R_2 V_{DD}}{R_1 + R_2} - V_{TH} \right)}, \tag{7.6}$$

where

$$V_1 = \frac{1}{\mu_n C_{ox} \frac{W}{L} R_S}. \tag{7.7}$$

Desventaja del MOS: no podés asumir Vgs=0,7V, tenés que resolver esta cuadrática del orto. Aguanten las exponenciales

This value of V_{GS} can then be substituted in Eq. (7.2) to obtain I_D. Of course, V_Y must exceed $V_X - V_{TH}$ to ensure operation in the saturation region.

Example 7.1

Determine the bias current of M_1 in Fig. 7.1 assuming $V_{TH} = 0.5\,\text{V}$, $\mu_n C_{ox} = 100\,\mu\text{A/V}^2$, $W/L = 5/0.18$, and $\lambda = 0$. What is the maximum allowable value of R_D for M_1 to remain in saturation?

Solution We have

$$V_X = \frac{R_2}{R_1 + R_2} V_{DD} \tag{7.8}$$

$$= 1.286\,\text{V}. \tag{7.9}$$

With an initial guess $V_{GS} = 1\,\text{V}$, the voltage drop across R_S can be expressed as $V_X - V_{GS} = 286\,\text{mV}$, yielding a drain current of 286 μA. Substituting for I_D in Eq. (7.3) gives the new value of V_{GS} as

$$V_{GS} = V_{TH} + \sqrt{\frac{2I_D}{\mu_n C_{ox} \dfrac{W}{L}}} \tag{7.10}$$

$$= 0.954\,\text{V}. \tag{7.11}$$

Consequently,

$$I_D = \frac{V_X - V_{GS}}{R_S} \tag{7.12}$$

$$= 332\,\mu\text{A}, \tag{7.13}$$

and hence

$$V_{GS} = 0.989\,\text{V}. \tag{7.14}$$

This gives $I_D = 297\,\mu$A.

As seen from the iterations, the solutions converge more slowly than those encountered in Chapter 5 for bipolar circuits. This is due to the quadratic (rather than exponential) I_D-V_{GS} dependence. We may therefore utilize the exact result in Eq. (7.6) to avoid lengthy calculations. Since $V_1 = 0.36\,\text{V}$,

$$V_{GS} = 0.974\,\text{V} \tag{7.15}$$

and

$$I_D = \frac{V_X - V_{GS}}{R_S} \tag{7.16}$$

$$= 312\,\mu\text{A}. \tag{7.17}$$

The maximum allowable value of R_D is obtained if $V_Y = V_X - V_{TH} = 0.786\,\text{V}$. That is,

$$R_D = \frac{V_{DD} - V_Y}{I_D} \tag{7.18}$$

$$= 3.25\,\text{k}\Omega. \tag{7.19}$$

Exercise What is the value of R_2 that places M_1 at the edge of saturation?

Example 7.2

In the circuit of Example 7.1, assume M_1 is in saturation and $R_D = 2.5\,\text{k}\Omega$ and compute (a) the maximum allowable value of W/L and (b) the minimum allowable value of R_S (with $W/L = 5/0.18$). Assume $\lambda = 0$.

Solution

(a) As W/L becomes larger, M_1 can carry a larger current for a given V_{GS}. With $R_D = 2.5\,\text{k}\Omega$ and $V_X = 1.286\,\text{V}$, the maximum allowable value of I_D is given by

$$I_D = \frac{V_{DD} - V_Y}{R_D} \tag{7.20}$$

$$= 406\,\mu\text{A}. \tag{7.21}$$

The voltage drop across R_S is then equal to 406 mV, yielding $V_{GS} = 1.286\,\text{V} - 0.406\,\text{V} = 0.88\,\text{V}$. In other words, M_1 must carry a current of 406 μA with $V_{GS} = 0.88\,\text{V}$:

$$I_D = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{GS} - V_{TH})^2 \tag{7.22}$$

$$406\,\mu\text{A} = (50\,\mu\text{A/V}^2)\frac{W}{L}(0.38\,\text{V})^2; \tag{7.23}$$

thus,

$$\frac{W}{L} = 56.2. \tag{7.24}$$

(b) With $W/L = 5/0.18$, the minimum allowable value of R_S gives a drain current of 406 μA. Since

$$V_{GS} = V_{TH} + \sqrt{\frac{2I_D}{\mu_n C_{ox}\dfrac{W}{L}}} \tag{7.25}$$

$$= 1.041\,\text{V}, \tag{7.26}$$

the voltage drop across R_S is equal to $V_X - V_{GS} = 245\,\text{mV}$. It follows that

$$R_S = \frac{V_X - V_{GS}}{I_D} \tag{7.27}$$

$$= 604\,\Omega. \tag{7.28}$$

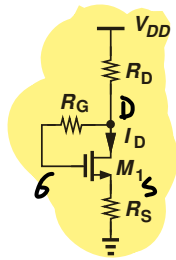
Exercise Repeat the above example if $V_{TH} = 0.35\,\text{V}$.

The self-biasing technique of Fig. 5.22 can also be applied to MOS amplifiers. Depicted in Fig. 7.2, the circuit can be analyzed by noting that M_1 is in saturation (why?) and the voltage drop across R_G is zero. Thus,

$$I_D R_D + V_{GS} + R_S I_D = V_{DD}. \tag{7.29}$$

Finding V_{GS} from this equation and substituting it in Eq. (7.3), we have

$$I_D = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}[V_{DD} - (R_S + R_D)I_D - V_{TH}]^2, \tag{7.30}$$



Nota : $-V_{GD} = V_{DS}$

Figure 7.2 Self-biased MOS stage.

la cuadrática más feadel tu vida

where channel-length modulation is neglected. It follows that

$$(R_S + R_D)^2 I_D^2 - 2\left[(V_{DD} - V_{TH})(R_S + R_D) + \frac{1}{\mu_n C_{ox}\frac{W}{L}}\right] I_D + (V_{DD} - V_{TH})^2 = 0. \tag{7.31}$$

a b c

Example 7.3

Calculate the drain current of M_1 in Fig. 7.3 if $\mu_n C_{ox} = 100\,\mu\text{A/V}^2$, $V_{TH} = 0.5\,\text{V}$, and $\lambda = 0$. What value of R_D is necessary to reduce I_D by a factor of two?

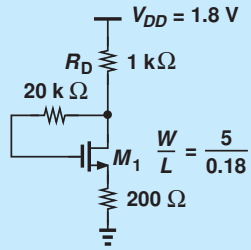


Figure 7.3 Example of self-biased MOS stage.

Solution Equation (7.31) gives

$$I_D = 556\,\mu\text{A}. \tag{7.32}$$

To reduce I_D to 278 μA, we solve Eq. (7.31) for R_D:

$$R_D = 2.867\,\text{k}\Omega. \tag{7.33}$$

Exercise Repeat the above example if V_{DD} drops to 1.2 V.

7.1.3 Realization of Current Sources

MOS transistors operating in saturation can act as current sources. As illustrated in Fig. 7.4(a), an NMOS device serves as a current source with one terminal tied to ground, i.e., it draws current from node X to ground. On the other hand, a PMOS transistor

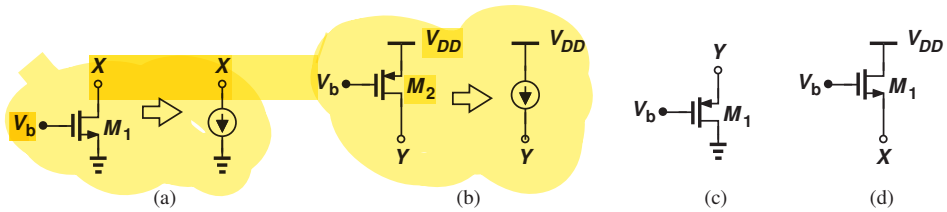


Figure 7.4 (a) NMOS device operating as a current source, (b) PMOS device operating as a current source, (c) PMOS topology not operating as a current source, (d) NMOS topology not operating as a current source.

Uno da, el otro chupa, if you know what i mean

[Fig. 7.4(b)] draws current from V_{DD} to node Y. If $\lambda = 0$, these currents remain independent of V_X or V_Y (so long as the transistors are in saturation).

¿?

It is important to understand that only the *drain* terminal of a MOSFET can draw a dc current and still present a high impedance. Specifically, NMOS or PMOS devices configured as shown in Figs. 7.4(c) and (d) do *not* operate as current sources because variation of V_X or V_Y directly changes the gate-source voltage of each transistor, thus changing the drain current considerably. From another perspective, the small-signal model of these two structures is identical to that of the diode-connected devices in Fig. 6.34, revealing a small-signal impedance of only $1/g_m$ (if $\lambda = 0$) rather than infinity.

7.2 COMMON-SOURCE STAGE

7.2.1 CS Core

Shown in Fig. 7.5(a), the basic CS stage is similar to the common-emitter topology, with the input applied to the gate and the output sensed at the drain. For small signals, M_1 converts the input voltage variations to proportional drain current changes, and R_D transforms the drain currents to the output voltage. If channel-length modulation is neglected, the small-signal model in Fig. 7.5(b) yields $v_{in} = v_1$ and $v_{out} = -g_m v_1 R_D$. That is,

$$\frac{v_{out}}{v_{in}} = -g_m R_D, \tag{7.34}$$

a result similar to that obtained for the common emitter stage in Chapter 5.

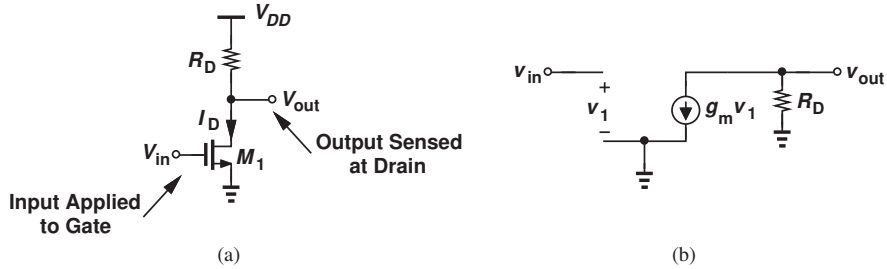


Figure 7.5 (a) Common-source stage, (b) small-signal mode.

The voltage gain of the CS stage is also limited by the supply voltage. Since $g_m = \sqrt{2\mu_n C_{ox}(W/L)I_D}$, we have

$$A_v = -\sqrt{2\mu_n C_{ox}\frac{W}{L}I_D}R_D, \tag{7.35}$$

concluding that if I_D or R_D is increased, so is the voltage drop across R_D ($= I_D R_D$).[1] For M_1 to remain in saturation,

$$V_{DD} - R_D I_D > V_{GS} - V_{TH}, \tag{7.36}$$

that is,

$$R_D I_D < V_{DD} - (V_{GS} - V_{TH}). \tag{7.37}$$

Example 7.4

Calculate the small-signal voltage gain of the CS stage shown in Fig. 7.6 if $I_D = 1\,\text{mA}$, $\mu_n C_{ox} = 100\,\mu\text{A/V}^2$, $V_{TH} = 0.5\,\text{V}$, and $\lambda = 0$. Verify that M_1 operates in saturation.

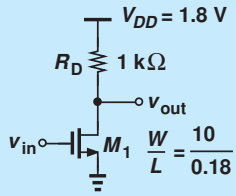


Figure 7.6 Example of CS stage.

Solution

We have

$$g_m = \sqrt{2\mu_n C_{ox}\frac{W}{L}I_D} \tag{7.38}$$

$$= \frac{1}{300\,\Omega}. \tag{7.39}$$

Thus,

$$A_v = -g_m R_D \tag{7.40}$$

$$= 3.33. \tag{7.41}$$

To check the operation region, we first determine the gate-source voltage:

$$V_{GS} = V_{TH} + \sqrt{\frac{2I_D}{\mu_n C_{ox}\frac{W}{L}}} \tag{7.42}$$

$$= 1.1\,\text{V}. \tag{7.43}$$

[1] It is possible to raise the gain to some extent by increasing W, but "subthreshold conduction" eventually limits the transconductance. This concept is beyond the scope of this book.

The drain voltage is equal to $V_{DD} - R_D I_D = 0.8\,\text{V}$. Since $V_{GS} - V_{TH} = 0.6\,\text{V}$, the device indeed operates in saturation and has a margin of 0.2 V with respect to the triode region. For example, if R_D is doubled with the intention of doubling A_v, then M_1 enters the triode region and its transconductance drops.

Exercise What value of V_{TH} places M_1 at the edge of saturation?

Since the gate terminal of MOSFETs draws a zero current (at very low frequencies), we say the CS amplifier provides a current gain of infinity. By contrast, the current gain of a common-emitter stage is equal to β.

Let us now compute the I/O impedances of the CS amplifier. Since the gate current is zero (at low frequencies),

$$R_{in} = \infty, \tag{7.44}$$

a point of contrast to the CE stage (whose R_{in} is equal to r_π). The high input impedance of the CS topology plays a critical role in many analog circuits.

The similarity between the small-signal equivalents of CE and CS stages indicates that the output impedance of the CS amplifier is simply equal to

$$R_{out} = R_D. \tag{7.45}$$

This is also seen from Fig. 7.7.

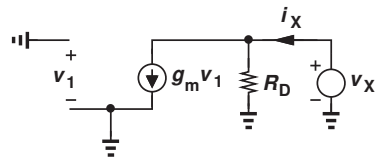


Figure 7.7 Output impedance of CS stage.

In practice, channel-length modulation may not be negligible, especially if R_D is large. The small-signal model of CS topology is therefore modified as shown in Fig. 7.8, revealing that

$$A_v = -g_m(R_D \| r_O) \tag{7.46}$$

$$R_{in} = \infty \tag{7.47}$$

$$R_{out} = R_D \| r_O. \tag{7.48}$$

In other words, channel-length modulation and the Early effect impact the CS and CE stages, respectively, in a similar manner.

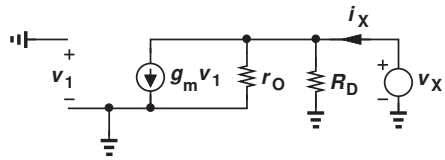
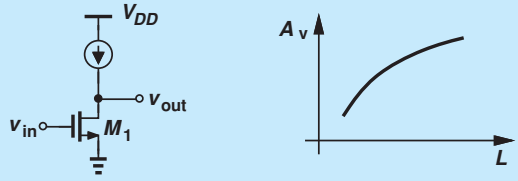


Figure 7.8 Effect of channel-length modulation on CS stage.

Example 7.5

Assuming M_1 operates in saturation, determine the voltage gain of the circuit depicted in Fig. 7.9(a) and plot the result as a function of the transistor channel length while other parameters remain constant.



(a) (b)

Figure 7.9 (a) CS stage with ideal current source as a load, (b) gain as a function of device channel length.

Solution

The ideal current source presents an infinite small-signal resistance, allowing the use of Eq. (7.46) with $R_D = \infty$:

$$A_v = -g_m r_O. \tag{7.49}$$

This is the highest voltage gain that a single transistor can provide. Writing $g_m = \sqrt{2\mu_n C_{ox}(W/L)I_D}$ and $r_O = (\lambda I_D)^{-1}$, we have

$$|A_v| = \frac{\sqrt{2\mu_n C_{ox}\dfrac{W}{L}}}{\lambda\sqrt{I_D}}. \tag{7.50}$$

This result may imply that $|A_v|$ falls as L increases, but recall from Chapter 6 that $\lambda \propto L^{-1}$:

$$|A_v| \propto \sqrt{\frac{2\mu_n C_{ox} WL}{I_D}}. \tag{7.51}$$

Consequently, $|A_v|$ increases with L [Fig. 7.9(b)].

Exercise Repeat the above example if a resistor of value R_1 is tied between the gate and drain of M_1.

7.2.2 CS Stage With Current-Source Load

As seen in the above example, the trade-off between the voltage gain and the voltage headroom can be relaxed by replacing the load resistor with a current source. The observations made in relation to Fig. 7.4(b) therefore suggest the use of a PMOS device as the load of an NMOS CS amplifier [Fig. 7.10(a)].

Let us determine the small-signal gain and output impedance of the circuit. Having a constant gate-source voltage, M_2 simply behaves as a resistor equal to its

Did you know?

The intrinsic gain, $g_m r_O$, of MOSFETs has fallen with technology scaling, i.e., as the minimum channel length has gone from about 10 μm in the 1960s to 25 nm today. Due to severe channel-length modulation, the intrinsic gain of these short-channel devices is on the order of 5 to 10, making it difficult to achieve a high voltage gain in many analog circuits. This issue has prompted extensive research on analog design using low-gain building blocks. For example, the analog-to-digital converter that digitizes the image in your camera may need an op amp with a gain of 4,000 but must now be designed with a gain of only 20.

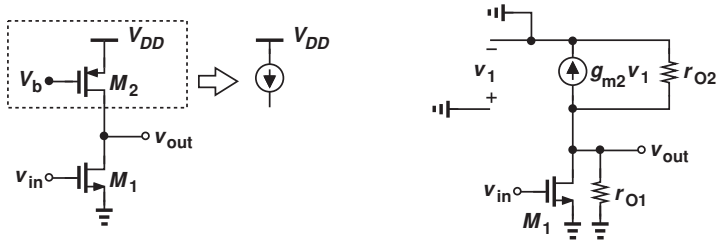


Figure 7.10 (a) CS stage using a PMOS device as a current source, (b) small-signal model.

output impedance [Fig. 7.10(b)] because $v_1 = 0$ and hence $g_{m2}v_1 = 0$. Thus, the drain node of M_1 sees both r_{O1} and r_{O2} to ac ground. Equations (7.46) and (7.48) give

$$A_v = -g_{m1}(r_{O1}||r_{O2}) \tag{7.52}$$

$$R_{out} = r_{O1}||r_{O2}. \tag{7.53}$$

Example 7.6

Figure 7.11 shows a PMOS CS stage using an NMOS current source load. Compute the voltage gain of the circuit.

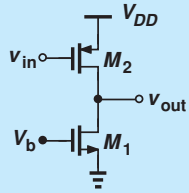


Figure 7.11 CS stage using an NMOS device as current source.

Solution Transistor M_2 generates a small-signal current equal to $g_{m2}v_{in}$, which then flows through $r_{O1}||r_{O2}$, producing $v_{out} = -g_{m2}v_{in}(r_{O1}||r_{O2})$. Thus,

$$A_v = -g_{m2}(r_{O1}||r_{O2}). \tag{7.54}$$

Exercise Calculate the gain if the circuit drives a loads resistance equal to R_L.

7.2.3 CS Stage With Diode-Connected Load

In some applications, we may use a diode-connected MOSFET as the drain load. Illustrated in Fig. 7.12(a), such a topology exhibits only a moderate gain due to the relatively low impedance of the diode-connected device (Section 7.1.3). With $\lambda = 0$, M_2 acts as a small-signal resistance equal to $1/g_{m2}$, and Eq. (7.34) yields

$$A_v = -g_{m1} \cdot \frac{1}{g_{m2}} \tag{7.55}$$

$$= -\frac{\sqrt{2\mu_n C_{ox}(W/L)_1 I_D}}{\sqrt{2\mu_n C_{ox}(W/L)_2 I_D}} \tag{7.56}$$

$$= -\sqrt{\frac{(W/L)_1}{(W/L)_2}}. \tag{7.57}$$

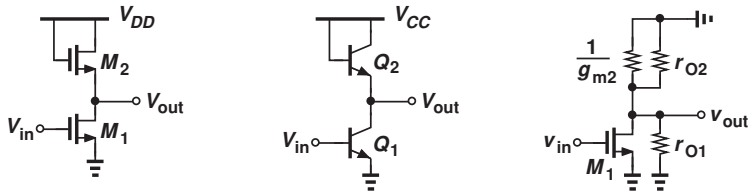


Figure 7.12 (a) MOS stage using a diode-connected load, (b) bipolar counterpart, (c) simplified circuit of (a).

Interestingly, the gain is given by the dimensions of M_1 and M_2 and remains independent of process parameters μ_n and C_{ox} and the drain current, I_D.

The reader may wonder why we did not consider a common-emitter stage with a diode-connected load in Chapter 5. Shown in Fig. 7.12(b), such a circuit is not used because it provides a voltage gain of only unity:

$$A_v = -g_{m1} \cdot \frac{1}{g_{m2}} \tag{7.58}$$

$$= -\frac{I_{C1}}{V_T} \cdot \frac{1}{I_{C2}/V_T} \tag{7.59}$$

$$\approx -1. \tag{7.60}$$

The contrast between Eqs. (7.57) and (7.60) arises from a fundamental difference between MOS and bipolar devices: transconductance of the former depends on device dimensions whereas that of the latter does not.

A more accurate expression for the gain of the stage in Fig. 7.12(a) must take channel-length modulation into account. As depicted in Fig. 7.12(c), the resistance seen at the drain is now equal to $(1/g_{m2})||r_{O2}||r_{O1}$, and hence

$$A_v = -g_{m1}\left(\frac{1}{g_{m2}}||r_{O2}||r_{O1}\right). \tag{7.61}$$

Similarly, the output resistance of the stage is given by

$$R_{out} = \frac{1}{g_{m2}}||r_{O2}||r_{O1}. \tag{7.62}$$

Example 7.7

Determine the voltage gain of the circuit shown in Fig. 7.13(a) if $\lambda \neq 0$.

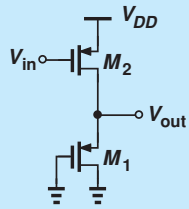


Figure 7.13 CS stage with diode-connected PMOS device.

Solution This stage is similar to that in Fig. 7.12(a), but with NMOS devices changed to PMOS transistors: M_1 serves as a common-source device and M_2 as a diode-connected load. Thus,

$$A_v = -g_{m2}\left(\frac{1}{g_{m1}}||r_{O1}||r_{O2}\right). \tag{7.63}$$

Exercise Repeat the above example if the gate of M_1 is tied to a constant voltage equal to 0.5 V.

7.2.4 CS Stage With Degeneration → otra vez sopa

Recall from Chapter 5 that a resistor placed in series with the emitter of a bipolar transistor alters characteristics such as gain, I/O impedances, and linearity. We expect similar results for a degenerated CS amplifier.

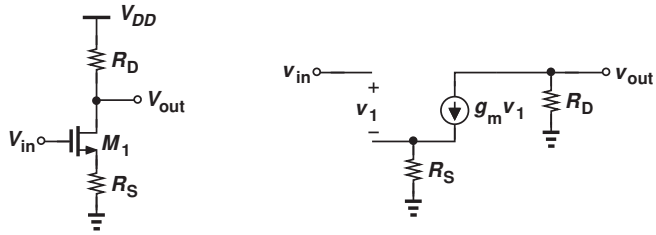


Figure 7.14 (a) CS stage with degeneration, (b) small-signal model.

Figure 7.14 depicts the stage along with its small-signal equivalent (if $\lambda = 0$). As with the bipolar counterpart, the degeneration resistor sustains a fraction of the input voltage change. From Fig. 7.14(b), we have

$$v_{in} = v_1 + g_m v_1 R_S \tag{7.64}$$

and hence

$$v_1 = \frac{v_{in}}{1 + g_m R_S}. \tag{7.65}$$

Since $g_m v_1$ flows through R_D, $v_{out} = -g_m v_1 R_D$ and

$$\frac{v_{out}}{v_{in}} = -\frac{g_m R_D}{1 + g_m R_S} \tag{7.66}$$

$$= -\frac{R_D}{\frac{1}{g_m} + R_S}, \tag{7.67}$$

a result identical to that expressed by Eq. (5.157) for the bipolar counterpart.

otra vez, cae la ganancia. ¿Qué se gana? ¿Se estabiliza mejor?

Example 7.8 Compute the voltage gain of the circuit shown in Fig. 7.15(a) if $\lambda = 0$.

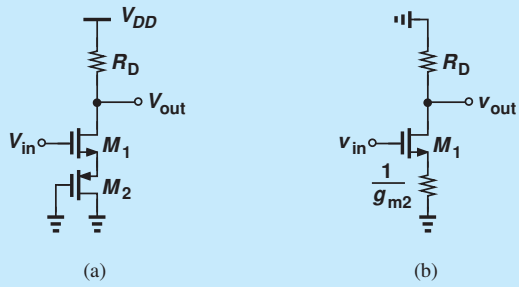


Figure 7.15 (a) Example of CS stage with degeneration, (b) simplified circuit.

Solution Transistor M_2 serves as a diode-connected device, presenting an impedance of $1/g_{m2}$ [Fig. 7.15(b)]. The gain is therefore given by Eq. (7.67) if R_S is replaced with $1/g_{m2}$:

$$A_v = -\frac{R_D}{\frac{1}{g_{m1}} + \frac{1}{g_{m2}}}. \tag{7.68}$$

Exercise What happens if $\lambda \neq 0$ for M_2?

In parallel with the developments in Chapter 5, we may study the effect of a resistor appearing in series with the gate (Fig. 7.16). However, since the gate current is zero (at low frequencies), R_G sustains no voltage drop and does not affect the voltage gain or the I/O impedances.

→ A TU PUTISIMA CASA TBJ

Effect of Transistor Output Impedance As with the bipolar counterparts, the inclusion of the transistor output impedance complicates the analysis and is studied in Problem 7.32. Nonetheless, the output impedance of the degenerated CS stage plays a critical role in analog design and is worth studying here.

Figure 7.17 shows the small-signal equivalent of the circuit. Since R_S carries a current equal to i_X (why?), we have $v_1 = -i_X R_S$. Also, the current through r_O is equal to

→ Por el gate no se va a ir

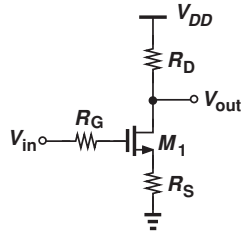


Figure 7.16 CS stage with gate resistance.

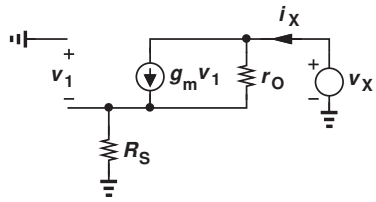


Figure 7.17 Output impedance of CS stage with degeneration.

$i_X - g_m v_1 = i_X - g_m(-i_X R_S) = i_X + g_m i_X R_S$. Adding the voltage drops across r_O and R_S and equating the result to v_X, we have

$$r_O(i_X + g_m i_X R_S) + i_X R_S = v_X, \tag{7.69}$$

and hence

$$\frac{v_X}{i_X} = r_O(1 + g_m R_S) + R_S \tag{7.70}$$

$$= (1 + g_m r_O) R_S + r_O \tag{7.71}$$

$$\approx g_m r_O R_S + r_O. \tag{7.72}$$

factor de multiplicación

Alternatively, we observe that the model in Fig. 7.17 is similar to its bipolar counterpart in Fig. 5.46(a) but with $r_\pi = \infty$. Letting $r_\pi \to \infty$ in Eqs. (5.196) and (5.197) yields the same results as above. As expected from our study of the bipolar degenerated stage, the MOS version also exhibits a "boosted" output impedance.

Example 7.9

Compute the output resistance of the circuit in Fig. 7.18(a) if M_1 and M_2 are identical.

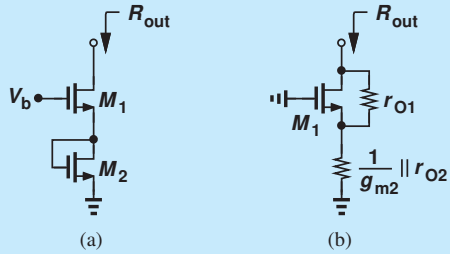


Figure 7.18 (a) Example of CS stage with degeneration, (b) simplified circuit.

Solution The diode-connected device M_2 can be represented by a small-signal resistance of $(1/g_{m2})||r_{O2} \approx 1/g_{m2}$. Transistor M_1 is degenerated by this resistance, and from Eq. (7.70):

$$R_{out} = r_{O1}\left(1 + g_{m1}\frac{1}{g_{m2}}\right) + \frac{1}{g_{m2}} \tag{7.73}$$

which, since $g_{m1} = g_{m2} = g_m$, reduces to

$$R_{out} = 2r_{O1} + \frac{1}{g_m} \tag{7.74}$$

$$\approx 2r_{O1}. \tag{7.75}$$

Exercise Do the results remain unchanged if M_2 is replaced with a diode-connected PMOS device?

Example 7.10 Determine the output resistance of the circuit in Fig. 7.19(a) and compare the result with that in the above example. Assume M_1 and M_2 are in saturation.

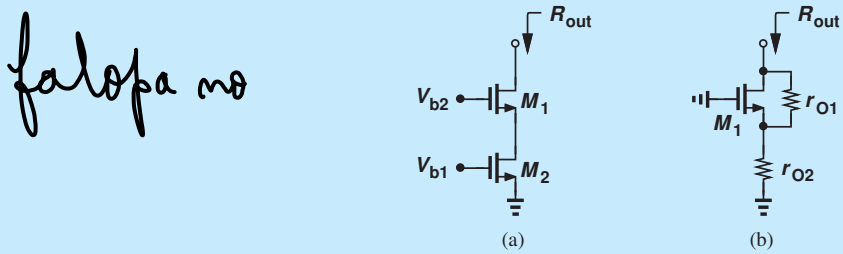


Figure 7.19 (a) Example of CS stage with degeneration, (b) simplified circuit.

Solution With its gate-source voltage fixed, transistor M_2 operates as a current source, introducing a resistance of r_{O2} from the source of M_1 to ground [Fig. 7.19(b)].

Equation (7.71) can therefore be written as

$$R_{out} = (1 + g_{m1}r_{O1})r_{O2} + r_{O1} \tag{7.76}$$

$$\approx g_{m1}r_{O1}r_{O2} + r_{O1}. \tag{7.77}$$

Assuming $g_{m1}r_{O2} \gg 1$ (which is valid in practice), we have

$$R_{out} \approx g_{m1}r_{O1}r_{O2}. \tag{7.78}$$

We observe that this value is quite higher than that in Eq. (7.75).

Exercise Repeat the above example for the PMOS counterpart of the circuit.

7.2.5 CS Core With Biasing

The effect of the simple biasing network shown in Fig. 7.1 is similar to that analyzed for the bipolar stage in Chapter 5. Depicted in Fig. 7.20(a) along with an input coupling capacitor (assumed a short circuit), such a circuit no longer exhibits an infinite input impedance:

$$R_{in} = R_1 || R_2. \tag{7.79}$$

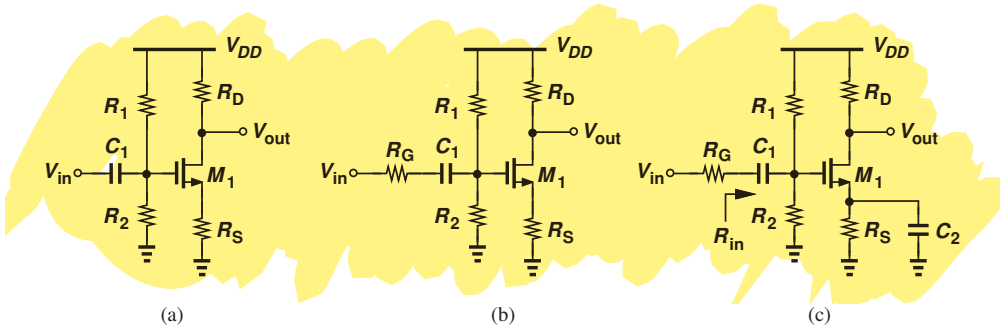


Figure 7.20 (a) CS stage with input coupling capacitor, (b) inclusion of gate resistance, (c) use of bypass capacitor.

Thus, if the circuit is driven by a finite source impedance [Fig. 7.20(b)], the voltage gain falls to

$$A_v = \frac{R_1||R_2}{R_G + R_1||R_2} \cdot \frac{-R_D}{\dfrac{1}{g_m} + R_S}, \tag{7.80}$$

where λ is assumed to be zero.

As mentioned in Chapter 5, it is possible to utilize degeneration for bias point stability but eliminate its effect on the small-signal performance by means of a bypass capacitor [Fig. 7.20(c)]. Unlike the case of bipolar realization, this does not alter the input impedance of the CS stage:

$$R_{in} = R_1||R_2, \tag{7.81}$$

but raises the voltage gain:

$$A_v = -\frac{R_1||R_2}{R_G + R_1||R_2} g_m R_D. \tag{7.82}$$

Example 7.11

Design the CS stage of Fig. 7.20(c) for a voltage gain of 5, an input impedance of 50 kΩ, and a power budget of 5 mW. Assume $\mu_n C_{ox} = 100\,\mu\text{A/V}^2$, $V_{TH} = 0.5\,\text{V}$, $\lambda = 0$, and $V_{DD} = 1.8\,\text{V}$. Also, assume a voltage drop of 400 mV across R_S.

Solution

The power budget along with $V_{DD} = 1.8\,\text{V}$ implies a maximum supply current of 2.78 mA. As an initial guess, we allocate 2.7 mA to M_1 and the remaining 80 μA to R_1 and R_2. It follows that

$$R_S = 148\,\Omega. \tag{7.83}$$

As with typical design problems, the choice of g_m and R_D is somewhat flexible so long as $g_m R_D = 5$. However, with I_D known, we must ensure a reasonable value for V_{GS}, e.g., $V_{GS} = 1\,\text{V}$. This choice yields

$$g_m = \frac{2I_D}{V_{GS} - V_{TH}} \tag{7.84}$$

$$= \frac{1}{92.6\,\Omega}, \tag{7.85}$$

and hence

$$R_D = 463\,\Omega. \tag{7.86}$$

Writing

$$I_D = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{GS} - V_{TH})^2 \tag{7.87}$$

gives

$$\frac{W}{L} = 216. \tag{7.88}$$

With $V_{GS} = 1$ V and a 400-mV drop across R_S, the gate voltage reaches 1.4 V, requiring that

$$\frac{R_2}{R_1 + R_2}V_{DD} = 1.4\,\text{V}, \tag{7.89}$$

which, along with $R_{in} = R_1||R_2 = 50\,\text{k}\Omega$, yields

$$R_1 = 64.3\,\text{k}\Omega \tag{7.90}$$

$$R_2 = 225\,\text{k}\Omega. \tag{7.91}$$

We must now check to verify that M_1 indeed operates in saturation. The drain voltage is given by $V_{DD} - I_D R_D = 1.8\,\text{V} - 1.25\,\text{V} = 0.55\,\text{V}$. Since the gate voltage is equal to 1.4 V, the gate-drain voltage difference exceeds V_{TH}, driving M_1 into the triode region!

How did our design procedure lead to this result? For the given I_D, we have chosen an excessively large R_D, i.e., an excessively small g_m (because $g_m R_D = 5$), even though V_{GS} is reasonable. We must therefore increase g_m so as to allow a lower value for R_D. For example, suppose we halve R_D and double g_m by increasing W/L by a factor of four:

$$\frac{W}{L} = 864 \tag{7.92}$$

$$g_m = \frac{1}{46.3\,\Omega}. \tag{7.93}$$

The corresponding gate-source voltage is obtained from (7.84):

$$V_{GS} = 250\,\text{mV}, \tag{7.94}$$

yielding a gate voltage of 650 mV.

Is M_1 in saturation? The drain voltage is equal to $V_{DD} - R_D I_D = 1.17\,\text{V}$, a value higher than the gate voltage minus V_{TH}. Thus, M_1 operates in saturation.

Exercise Repeat the above example for a power budget of 3 mW and $V_{DD} = 1.2$ V.

7.3 COMMON-GATE STAGE

Shown in Fig. 7.21, the CG topology resembles the common-base stage studied in Chapter 5. Here, if the input rises by a small value, ΔV, then the gate-source voltage of M_1 *decreases* by the same amount, thereby lowering the drain current by $g_m \Delta V$ and

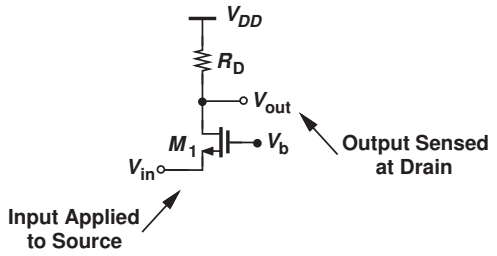


Figure 7.21 Common-gate stage.

raising V_{out} by $g_m \Delta V R_D$. That is, the voltage gain is positive and equal to

$$A_v = g_m R_D. \tag{7.95}$$

The CG stage suffers from voltage headroom-gain trade-offs similar to those of the CB topology. In particular, to achieve a high gain, a high I_D or R_D is necessary, but the drain voltage, $V_{DD} - I_D R_D$, must remain above $V_b - V_{TH}$ to ensure M_1 is saturated.

Example 7.12

A microphone having a dc level of zero drives a CG stage biased at $I_D = 0.5\,\text{mA}$. If $W/L = 50$, $\mu_n C_{ox} = 100\,\mu\text{A/V}^2$, $V_{TH} = 0.5\,\text{V}$, and $V_{DD} = 1.8\,\text{V}$, determine the maximum allowable value of R_D and hence the maximum voltage gain. Neglect channel-length modulation.

Solution

With W/L known, the gate-source voltage can be determined from

$$I_D = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{GS} - V_{TH})^2 \tag{7.96}$$

as

$$V_{GS} = 0.947\,\text{V}. \tag{7.97}$$

For M_1 to remain in saturation,

$$\underbrace{V_{DD} - I_D R_D}_{V_D} > V_b - V_{TH} \tag{7.98}$$

and hence

$$R_D < 2.71\,\text{k}\Omega. \tag{7.99}$$

Also, the above value of W/L and I_D yield $g_m = (447\,\Omega)^{-1}$ and

$$A_v \leq 6.06. \tag{7.100}$$

Figure 7.22 summarizes the allowable signal levels in this design. The gate voltage can be generated using a resistive divider similar to that in Fig. 7.20(a).

Exercise If a gain of 10 is required, what value should be chosen for W/L?

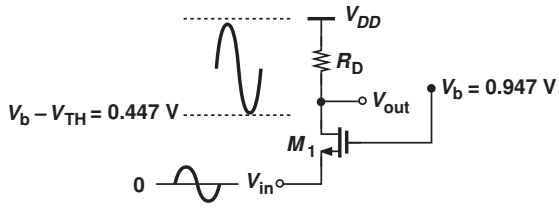


Figure 7.22 Signal levels in CG stage.

We now compute the I/O impedances of the CG stage, expecting to obtain results similar to those of the CB topology. Neglecting channel-length modulation for now, we have from Fig. 7.23(a) $v_1 = -v_X$ and

$$i_X = -g_m v_1 \tag{7.101}$$

$$= g_m v_X. \tag{7.102}$$

That is,

$$R_{in} = \frac{1}{g_m}, \tag{7.103}$$

a relatively *low* value. Also, from Fig. 7.23(b), $v_1 = 0$ and hence

$$R_{out} = R_D, \tag{7.104}$$

an expected result because the circuits of Figs. 7.23(b) and 7.7 are identical.

Did you know?

The common-gate stage is sometimes used as a low-noise RF amplifier, e.g., at the input of your WiFi receiver. This topology is attractive because its low input impedance allows simple "impedance matching" with the antenna. However, with the reduction of the intrinsic gain, $g_m r_O$, as a result of scaling, the input impedance, R_{in}, is now too high! It can be shown that with channel-length modulation

$$R_{in} = \frac{R_D + r_O}{1 + g_m r_O}$$

which reduces to $1/g_m$ if $g_m r_O \gg 1$ and $R_D \ll r_O$. Since neither of these conditions holds anymore, the CG stage presents new challenges to RF designers.

Let us study the behavior of the CG stage in the presence of a finite source impedance (Fig. 7.24) but still with $\lambda = 0$. In a manner similar to that depicted in Chapter 5 for the CB topology, we write

$$v_X = \frac{\dfrac{1}{g_m}}{\dfrac{1}{g_m} + R_S} v_{in} \tag{7.105}$$

$$= \frac{1}{1 + g_m R_S} v_{in}. \tag{7.106}$$

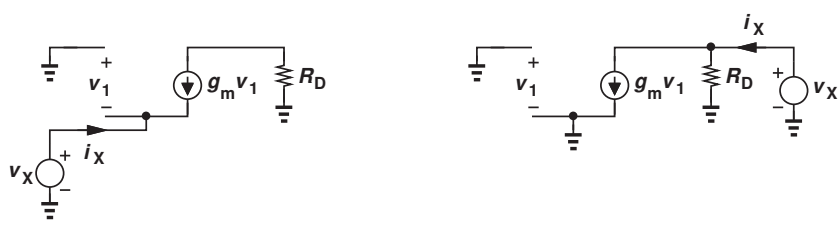


Figure 7.23 (a) Input and (b) output impedances of CG stage.

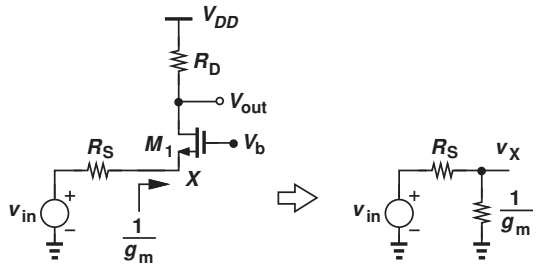


Figure 7.24 Simplification of CG stage with signal source resistance.

Thus,

$$\frac{v_{out}}{v_{in}} = \frac{v_{out}}{v_X} \cdot \frac{v_X}{v_{in}} \tag{7.107}$$

$$= \frac{g_m R_D}{1 + g_m R_S} \tag{7.108}$$

$$= \frac{R_D}{\frac{1}{g_m} + R_S}. \tag{7.109}$$

The gain is therefore equal to that of the degenerated CS stage except for a negative sign.

In contrast to the common-source stage, the CG amplifier exhibits a current gain of unity: the current provided by the input voltage source simply flows through the channel and emerges from the drain node.

The analysis of the common-gate stage in the general case, i.e., including both channel-length modulation and a finite source impedance, is beyond the scope of this book (Problem 7.42). However, we can make two observations. First, a resistance appearing in series with the gate terminal [Fig. 7.25(a)] does not alter the gain or I/O impedances (at low frequencies) because it sustains a zero potential drop—as if its value were zero. Second, the output resistance of the CG stage in the general case [Fig. 7.25(b)] is identical to that of the degenerated CS topology:

$$R_{out} = (1 + g_m r_O) R_S + r_O. \tag{7.110}$$

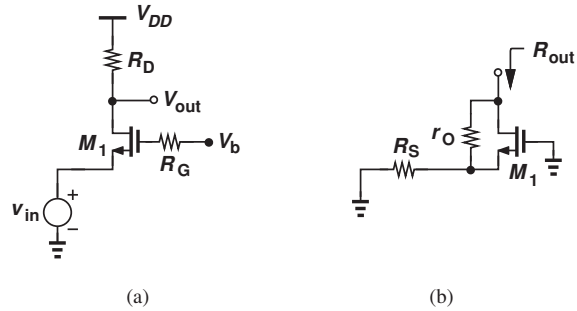


Figure 7.25 (a) CG stage with gate resistance, (b) output resistance of CG stage.

Example 7.13

For the circuit shown in Fig. 7.26(a), calculate the voltage gain if $\lambda = 0$ and the output impedance if $\lambda > 0$.

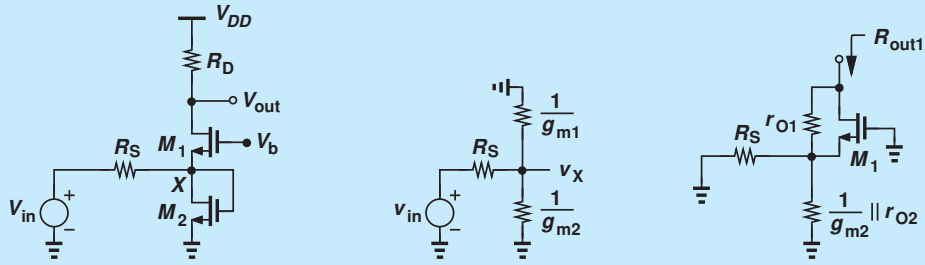


Figure 7.26 (a) Example of CG stage, (b) equivalent input network, (c) calculation of output resistance.

Solution We first compute v_X/v_{in} with the aid of the equivalent circuit depicted in Fig. 7.26(b):

$$\frac{v_X}{v_{in}} = \frac{\dfrac{1}{g_{m2}} \Big\| \dfrac{1}{g_{m1}}}{\dfrac{1}{g_{m2}} \Big\| \dfrac{1}{g_{m1}} + R_S} \tag{7.111}$$

$$= \frac{1}{1 + (g_{m1} + g_{m2})R_S}. \tag{7.112}$$

Noting that $v_{out}/v_X = g_{m1}R_D$, we have

$$\frac{v_{out}}{v_{in}} = \frac{g_{m1}R_D}{1 + (g_{m1} + g_{m2})R_S}. \tag{7.113}$$

To compute the output impedance, we first consider R_{out1}, as shown in Fig. 7.26(c), which from Eq. (7.110) is equal to

$$R_{out1} = (1 + g_{m1}r_{O1}) \left(\frac{1}{g_{m2}} || r_{O2} || R_S \right) + r_{O1} \tag{7.114}$$

$$\approx g_{m1}r_{O1} \left(\frac{1}{g_{m2}} || R_S \right) + r_{O1}. \tag{7.115}$$

The overall output impedance is then given by

$$R_{out} = R_{out1} || R_D \tag{7.116}$$

$$\approx \left[g_{m1}r_{O1} \left(\frac{1}{g_{m2}} || R_S \right) + r_{O1} \right] \Big\| R_D. \tag{7.117}$$

Exercise Calculate the output impedance if the gate of M_2 is tied to a constant voltage.

7.3.1 CG Stage With Biasing

Following our study of the CB biasing in Chapter 5, we surmise the CG amplifier can be biased as shown in Fig. 7.27. Providing a path for the bias current to ground, resistor R_3 lowers the input impedance—and hence the voltage gain—if the signal source exhibits a finite output impedance, R_S.

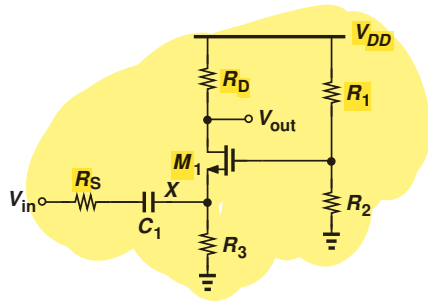


Figure 7.27 CG stage with biasing.

Since the impedance seen to the right of node X is equal to $R_3||(1/g_m)$, we have

$$\frac{v_{out}}{v_{in}} = \frac{v_X}{v_{in}} \cdot \frac{v_{out}}{v_X} \tag{7.118}$$

$$= \frac{R_3||(1/g_m)}{R_3||(1/g_m) + R_S} \cdot g_m R_D, \tag{7.119}$$

where channel-length modulation is neglected. As mentioned earlier, the voltage divider consisting of R_1 and R_2 does not affect the small-signal behavior of the circuit (at low frequencies).

Example 7.14

Design the common-gate stage of Fig. 7.27 for the following parameters: $v_{out}/v_{in} = 5$, $R_S = 0$, $R_3 = 500\ \Omega$, $1/g_m = 50\ \Omega$, power budget $= 2$ mW, $V_{DD} = 1.8$ V. Assume $\mu_n C_{ox} = 100\ \mu\text{A/V}^2$, $V_{TH} = 0.5$ V, and $\lambda = 0$.

Solution

From the power budget, we obtain a total supply current of 1.11 mA. Allocating 10 μA to the voltage divider, R_1 and R_2, we leave 1.1 mA for the drain current of M_1. Thus, the voltage drop across R_3 is equal to 550 mV.

We must now compute two interrelated parameters: W/L and R_D. A larger value of W/L yields a greater g_m, allowing a lower value of R_D. As in Example 7.11, we choose an initial value for V_{GS} to arrive at a reasonable guess for W/L. For example, if $V_{GS} = 0.8$ V, then $W/L = 244$, and $g_m = 2I_D/(V_{GS} - V_{TH}) = (136.4\ \Omega)^{-1}$, dictating $R_D = 682\ \Omega$ for $v_{out}/v_{in} = 5$.

Let us determine whether M_1 operates in saturation. The gate voltage is equal to V_{GS} plus the drop across R_3, amounting to 1.35 V. On the other hand, the drain voltage is given by $V_{DD} - I_D R_D = 1.05$ V. Since the drain voltage exceeds $V_G - V_{TH}$, M_1 is indeed in saturation.

The resistive divider consisting of R_1 and R_2 must establish a gate voltage equal to 1.35 V while drawing 10 μA:

$$\frac{V_{DD}}{R_1 + R_2} = 10\,\mu\text{A} \tag{7.120}$$

$$\frac{R_2}{R_1 + R_2} V_{DD} = 1.35\,\text{V}. \tag{7.121}$$

It follows that $R_1 = 45\,\text{k}\Omega$ and $R_2 = 135\,\text{k}\Omega$.

Exercise If W/L cannot exceed 100, what voltage gain can be achieved?

Example 7.15 Suppose in Example 7.14, we wish to minimize W/L (and hence transistor capacitances). What is the minimum acceptable value of W/L?

Solution For a given I_D, as W/L decreases, $V_{GS} - V_{TH}$ increases. Thus, we must first compute the maximum allowable V_{GS}. We impose the condition for saturation as

$$V_{DD} - I_D R_D > V_{GS} + V_{R3} - V_{TH}, \tag{7.122}$$

where V_{R3} denotes the voltage drop across R_3, and set $g_m R_D$ to the required gain:

$$\frac{2I_D}{V_{GS} - V_{TH}} R_D = A_v. \tag{7.123}$$

Eliminating R_D from Eqs. (7.122) and (7.123) gives:

$$V_{DD} - \frac{A_v}{2}(V_{GS} - V_{TH}) > V_{GS} - V_{TH} + V_{R3} \tag{7.124}$$

and hence

$$V_{GS} - V_{TH} < \frac{V_{DD} - V_{R3}}{\frac{A_v}{2} + 1}. \tag{7.125}$$

In other words,

$$W/L > \frac{2I_D}{\mu_n C_{ox}\left(2\dfrac{V_{DD} - V_{R3}}{A_v + 2}\right)^2}. \tag{7.126}$$

It follows that

$$W/L > 172.5. \tag{7.127}$$

Exercise Repeat the above example for $A_v = 10$.

7.4 SOURCE FOLLOWER

The MOS counterpart of the emitter follower is called the "source follower" (or the "common-drain" stage) and shown in Fig. 7.28. The amplifier senses the input at the gate and produces the output at the source, with the drain tied to V_{DD}. The circuit's behavior is similar to that of the bipolar counterpart.

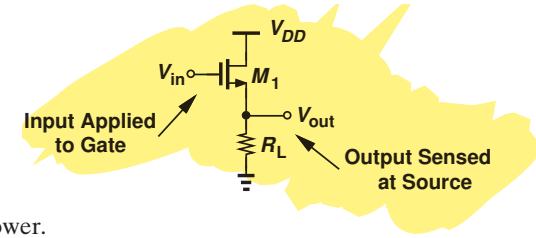


Figure 7.28 Source follower.

7.4.1 Source Follower Core

If the gate voltage of M_1 in Fig. 7.28 is raised by a small amount, ΔV_{in}, the gate-source voltage tends to increase, thereby raising the source current and hence the output voltage. Thus, V_{out} "follows" V_{in}. Since the dc level of V_{out} is lower than that of V_{in} by V_{GS}, we say the follower can serve as a "level shift" circuit. From our analysis of emitter followers in Chapter 5, we expect this topology to exhibit a subunity gain, too.

Figure 7.29(a) depicts the small-signal equivalent of the source follower, including channel-length modulation. Recognizing that r_O appears in parallel with R_L, we have

$$g_m v_1 (r_O || R_L) = v_{out}. \tag{7.128}$$

Also,

$$v_{in} = v_1 + v_{out}. \tag{7.129}$$

It follows that

$$\frac{v_{out}}{v_{in}} = \frac{g_m (r_O || R_L)}{1 + g_m (r_O || R_L)} \tag{7.130}$$

$$= \frac{r_O || R_L}{\dfrac{1}{g_m} + r_O || R_L}. \tag{7.131}$$

The voltage gain is therefore positive and less than unity. It is desirable to maximize R_L (and r_O).

As with emitter followers, we can view the above result as voltage division between a resistance equal to $1/g_m$ and another equal to $r_O || R_L$ [Fig. 7.29(b)]. Note, however, that a resistance placed in series with the gate does not affect Eq. (7.131) (at low frequencies) because it sustains a zero drop.

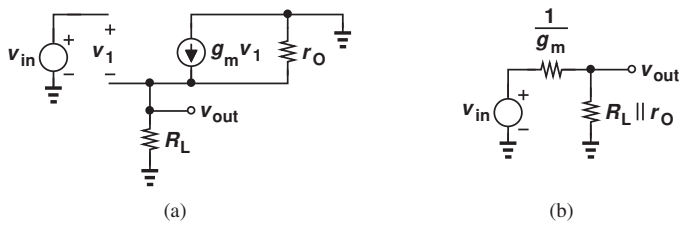


Figure 7.29 (a) Small-signal equivalent of source follower, (b) simplified circuit.

Example 7.16

A source follower is realized as shown in Fig. 7.30(a), where M_2 serves as a current source. Calculate the voltage gain of the circuit.

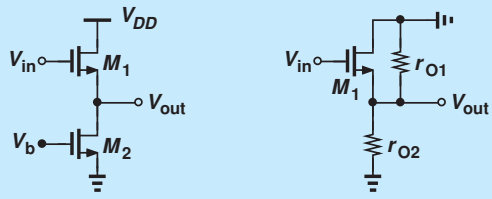


Figure 7.30 (a) Follower with ideal current source, (b) simplified circuit.

Solution

Since M_2 simply presents an impedance of r_{O2} from the output node to ac ground [Fig. 7.30(b)], we substitute $R_L = r_{O2}$ in Eq. (7.131):

$$A_v = \frac{r_{O1}||r_{O2}}{\dfrac{1}{g_{m1}} + r_{O1}||r_{O2}}. \tag{7.132}$$

If $r_{O1}||r_{O2} \gg 1/g_{m1}$, then $A_v \approx 1$.

Exercise

Repeat the above example if a resistance of value R_S is placed in series with the source of M_2.

Example 7.17

Design a source follower to drive a 50-Ω load with a voltage gain of 0.5 and a power budget of 10 mW. Assume $\mu_n C_{ox} = 100\,\mu\text{A/V}^2$, $V_{TH} = 0.5$ V, $\lambda = 0$, and $V_{DD} = 1.8$ V.

Solution

With $R_L = 50\,\Omega$ and $r_O = \infty$ in Fig. 7.28, we have

$$A_v = \frac{R_L}{\dfrac{1}{g_m} + R_L} \tag{7.133}$$

and hence

$$g_m = \frac{1}{50\,\Omega}. \tag{7.134}$$

The power budget and supply voltage yield a maximum supply current of 5.56 mA. Using this value for I_D in $g_m = \sqrt{2\mu_n C_{ox}(W/L)I_D}$ gives

$$W/L = 360. \tag{7.135}$$

Exercise

What voltage gain can be achieved if the power budget is raised to 15 mW?

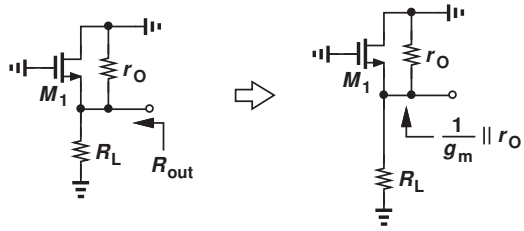


Figure 7.31 Output resistance of source follower.

It is instructive to compute the output impedance of the source follower.[2] As illustrated in Fig. 7.31, R_{out} consists of the resistance seen looking up into the source in parallel with that seen looking down into R_L. With $\lambda \neq 0$, the former is equal to $(1/g_m)||r_O$, yielding

Nota: $R_{IN} = \infty$

$$R_{out} = \frac{1}{g_m} ||r_O||R_L \tag{7.136}$$

$$\approx \frac{1}{g_m} ||R_L. \tag{7.137}$$

In summary, the source follower exhibits a very high input impedance and a relatively low output impedance, thereby providing buffering capability.

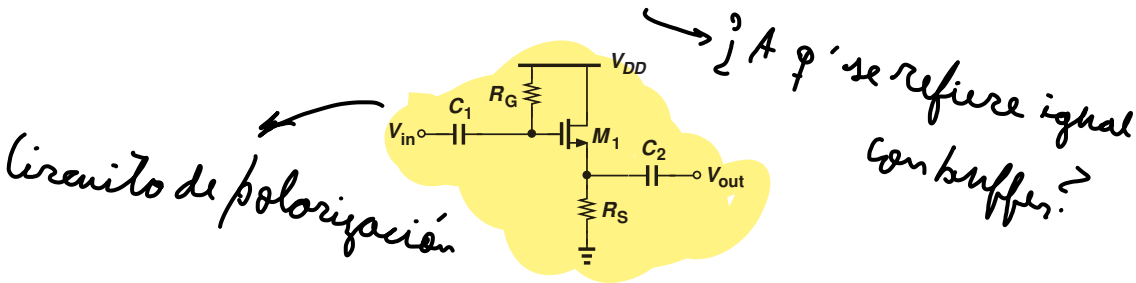


Figure 7.32 Source follower with input and output coupling capacitors.

7.4.2 Source Follower With Biasing

$I_G = 0$

$V_{DG} = 0$

The biasing of source followers is similar to that of emitter followers (Chapter 5). Figure 7.32 depicts an example where R_G establishes a dc voltage equal to V_{DD} at the gate of M_1 (why?) and R_S sets the drain bias current. Note that M_1 operates in saturation because the gate and drain voltages are equal. Also, the input impedance of the circuit has dropped from infinity to R_G.

Let us compute the bias current of the circuit. With a zero voltage drop across R_G, we have

$$V_{GS} + I_D R_S = V_{DD}. \tag{7.138}$$

[2]The input impedance is infinite at low frequencies.

Neglecting channel-length modulation, we write

$$I_D = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{GS} - V_{TH})^2 \tag{7.139}$$

$$= \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{DD} - I_D R_S - V_{TH})^2. \tag{7.140}$$

Puta cuadrática de mierda ↑

The resulting quadratic equation can be solved to obtain I_D.

Example 7.18

Design the source follower of Fig. 7.32 for a drain current of 1 mA and a voltage gain of 0.8. Assume $\mu_n C_{ox} = 100\,\mu\text{A/V}^2$, $V_{TH} = 0.5\,\text{V}$, $\lambda = 0$, $V_{DD} = 1.8\,\text{V}$, and $R_G = 50\,\text{k}\Omega$.

Solution

The unknowns in this problem are V_{GS}, W/L, and R_S. The following three equations can be formed:

$$I_D = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{GS} - V_{TH})^2 \tag{7.141}$$

$$I_D R_S + V_{GS} = V_{DD} \tag{7.142}$$

$$A_v = \frac{R_S}{\dfrac{1}{g_m} + R_S}. \tag{7.143}$$

If g_m is written as $2I_D/(V_{GS} - V_{TH})$, then Eqs. (7.142) and (7.143) do not contain W/L and can be solved to determine V_{GS} and R_S. With the aid of Eq. (7.142), we write Eq. (7.143) as

$$A_v = \frac{R_S}{\dfrac{V_{GS} - V_{TH}}{2I_D} + R_S} \tag{7.144}$$

$$= \frac{2I_D R_S}{V_{GS} - V_{TH} + 2I_D R_S} \tag{7.145}$$

$$= \frac{2I_D R_S}{V_{DD} - V_{TH} + I_D R_S}. \tag{7.146}$$

Thus,

$$R_S = \frac{V_{DD} - V_{TH}}{I_D}\frac{A_v}{2 - A_v} \tag{7.147}$$

$$= 867\,\Omega. \tag{7.148}$$

and

$$V_{GS} = V_{DD} - I_D R_S \tag{7.149}$$

$$= V_{DD} - (V_{DD} - V_{TH})\frac{A_v}{2 - A_v} \tag{7.150}$$

$$= 0.933\,\text{V}. \tag{7.151}$$

It follows from Eq. (7.141) that

$$\frac{W}{L} = 107. \tag{7.152}$$

Exercise What voltage gain can be achieved if W/L cannot exceed 50?

Equation (7.140) reveals that the bias current of the source follower varies with the supply voltage. To avoid this effect, integrated circuits bias the follower by means of a current source (Fig. 7.33).

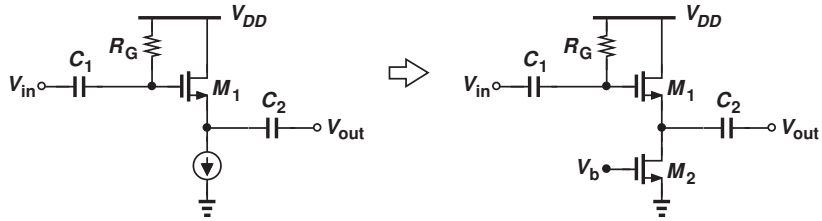


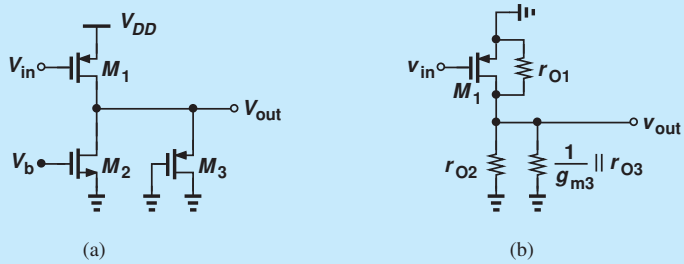
Figure 7.33 Source follower with biasing.

7.5 SUMMARY AND ADDITIONAL EXAMPLES

In this chapter, we have studied three basic CMOS building blocks, namely, the common-source stage, the common-gate stage, and the source follower. As observed throughout the chapter, the small-signal behavior of these circuits is quite similar to that of their bipolar counterparts, with the exception of the high impedance seen at the gate terminal. We have noted that the biasing schemes are also similar, with the quadratic I_D-V_{GS} relationship supplanting the exponential I_C-V_{BE} characteristic.

In this section, we consider a number of additional examples to solidify the concepts introduced in this chapter, emphasizing analysis by inspection.

Example 7.19 Calculate the voltage gain and output impedance of the circuit shown in Fig. 7.34(a).



(a) (b)

Figure 7.34 (a) Example of CS stage, (b) simplified circuit.

Solution We identify M_1 as a common-source device because it senses the input at its gate and generates the output at its drain. Transistors M_2 and M_3 therefore act as the load, with the former serving as a current source and the latter as a diode-connected device. Thus, M_2 can be replaced with a small-signal resistance equal to r_{O2}, and M_3 with another equal to $(1/g_{m3})||r_{O3}$. The circuit now reduces to that depicted in Fig. 7.34(b), yielding

$$A_v = -g_{m1}\left(\frac{1}{g_{m3}}||r_{O1}||r_{O2}||r_{O3}\right) \tag{7.153}$$

and

$$R_{out} = \frac{1}{g_{m3}}||r_{O1}||r_{O2}||r_{O3}. \tag{7.154}$$

Note that $1/g_{m3}$ is dominant in both expressions.

Exercise Repeat the above example if M_2 is converted to a diode-connected device.

Example 7.20 Compute the voltage gain of the circuit shown in Fig. 7.35(a). Neglect channel-length modulation in M_1.

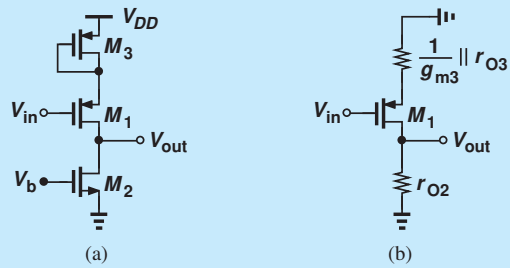


Figure 7.35 (a) Example of CS stage, (b) simplified circuit.

Solution Operating as a CS stage and degenerated by the diode-connected device M_3, transistor M_1 drives the current-source load, M_2. Simplifying the amplifier to that in Fig. 7.35(b), we have

$$A_v = -\frac{r_{O2}}{\dfrac{1}{g_{m1}} + \dfrac{1}{g_{m3}}||r_{O3}}. \tag{7.155}$$

Exercise Repeat the above example if the gate of M_3 is tied to a constant voltage.

Example 7.21

Determine the voltage gain of the amplifiers illustrated in Fig. 7.36. For simplicity, assume $r_{O1} = \infty$ in Fig. 7.36(b).

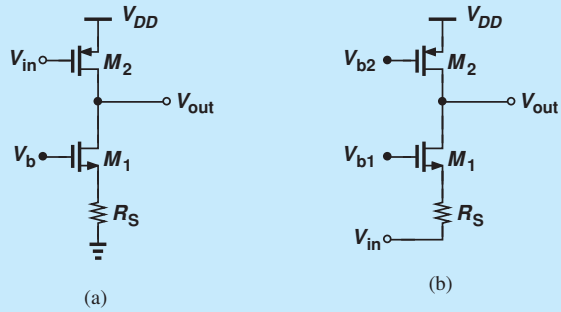


Figure 7.36 Examples of (a) CS and (b) CG stages.

Solution

Degenerated by R_S, transistor M_1 in Fig. 7.36(a) presents an impedance of $(1 + g_{m1}r_{O1})R_S + r_{O1}$ to the drain of M_2. Thus the total impedance seen at the drain is equal to $[(1 + g_{m1}r_{O1})R_S + r_{O1}]||r_{O2}$, giving a voltage gain of

$$A_v = -g_{m2}\{[(1 + g_{m1}r_{O1})R_S + r_{O1}]||r_{O1}\}. \tag{7.156}$$

In Fig. 7.36(b), M_1 operates as a common-gate stage and M_2 as the load, obtaining Eq. (7.109):

$$A_{v2} = \frac{r_{O2}}{\dfrac{1}{g_{m1}} + R_S}. \tag{7.157}$$

Exercise Replace R_S wit a diode-connected device and repeat the analysis.

Example 7.22

Calculate the voltage gain of the circuit shown in Fig. 7.37(a) if $\lambda = 0$.

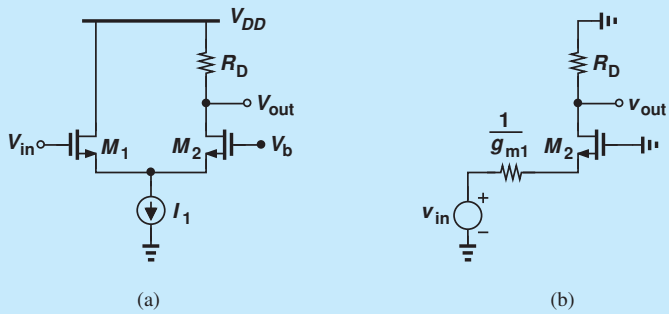


Figure 7.37 (a) Example of a composite stage, (b) simplified circuit.

Solution In this circuit, M_1 operates as a source follower and M_2 as a CG stage (why?). A simple method of analyzing the circuit is to replace v_{in} and M_1 with a Thevenin equivalent. From Fig. 7.29(b), we derive the model depicted in Fig. 7.37(b). Thus,

$$A_v = \frac{R_D}{\frac{1}{g_{m1}} + \frac{1}{g_{m2}}}. \tag{7.158}$$

Exercise What happens if a resistance of value R_1 is placed in series with the drain of M_1?

Example 7.23 The circuit of Fig. 7.38 produces two outputs. Calculate the voltage gain from the input to Y and to X. Assume $\lambda = 0$ for M_1.

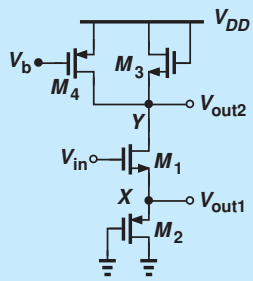


Figure 7.38 Example of composite stage.

Solution For V_{out1}, the circuit serves as a source follower. The reader can show that if $r_{O1} = \infty$, then M_3 and M_4 do not affect the source follower operation. Exhibiting a small-signal impedance of $(1/g_{m2})||r_{O2}$, transistor M_2 acts as a load for the follower, yielding from Eq. (7.131)

$$\frac{v_{out1}}{v_{in}} = \frac{\frac{1}{g_{m2}}||r_{O2}}{\frac{1}{g_{m2}}||r_{O2} + \frac{1}{g_{m1}}}. \tag{7.159}$$

For V_{out2}, M_1 operates as a degenerated CS stage with a drain load consisting of the diode-connected device M_3 and the current source M_4. This load impedance is equal to $(1/g_{m3})||r_{O3}||r_{O4}$, resulting in

$$\frac{v_{out2}}{v_{in}} = -\frac{\frac{1}{g_{m3}}||r_{O3}||r_{O4}}{\frac{1}{g_{m1}} + \frac{1}{g_{m2}}||r_{O2}}. \tag{7.160}$$

Exercise Which one of the two gains is higher? Explain intuitively why.

7.6 CHAPTER SUMMARY

- The impedances seen looking into the gate, drain, and source of a MOSFET are equal to infinity, r_O (with source grounded), and $1/g_m$ (with gate grounded), respectively.
- In order to obtain the required small-signal MOS parameters such as g_m and r_O, the transistor must be "biased," i.e., carry a certain drain current and sustain certain gate-source and drain-source voltages. Signals simply perturb these conditions.
- Biasing techniques establish the required gate voltage by means of a resistive path to the supply rails or the output node (self-biasing).
- With a single transistor, only three amplifier topologies are possible: common-source and common-gate stages and source followers.
- The CS stage provides a moderate voltage gain, a high input impedance, and a moderate output impedance.
- Source degeneration improves the linearity but lowers the voltage gain.
- Source degeneration raises the output impedance of CS stages considerably.
- The CG stage provides a moderate voltage gain, a low input impedance, and a moderate output impedance.
- The voltage gain expressions for CS and CG stages are similar but for a sign.
- The source follower provides a voltage gain less than unity, a high input impedance, and a low output impedance, serving as a good voltage buffer.

xq hay degeneración acá, si no dependo de beta?

Buffer, xq si tengo una tensión que no quiero que se pierda en algún lado, pongo un seguidor para que la tensión la imponga la batería (Vcc) y sea igual a la de entrada. Ponele.
Una hora para leer este cap. Bien. A ver si llego a escribir en 1h tmb.

PROBLEMS

In the following problems, unless otherwise stated, assume $\mu_n C_{ox} = 200\,\mu\text{A/V}^2$, $\mu_p C_{ox} = 100\,\mu\text{A/V}^2$, $\lambda = 0$, and $V_{TH} = 0.4$ V for NMOS devices and -0.4 V for PMOS devices.

Sec. 7.1.2 Biasing

7.1. In the circuit of Fig. 7.39, determine the maximum allowable value of W/L if M_1 must remain in saturation. Assume $\lambda = 0$.

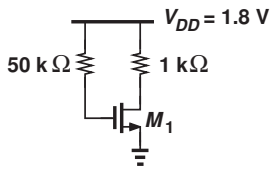


Figure 7.39

7.2. We wish to design the circuit of Fig. 7.40 for a drain current of 1 mA. If $W/L = 20/0.18$, compute R_1 and R_2 such that the input impedance is at least 20 kΩ.

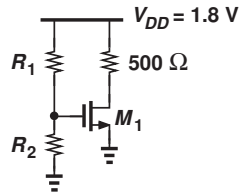


Figure 7.40

7.3. Consider the circuit shown in Fig. 7.41. Calculate the maximum transconductance that M_1 can provide (without going into the triode region.)

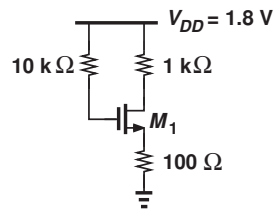


Figure 7.41

7.4. The circuit of Fig. 7.42 must be designed for a voltage drop of 200 mV across R_S.
(a) Calculate the minimum allowable value of W/L if M_1 must remain in saturation.
(b) What are the required values of R_1 and R_2 if the input impedance must be at least 30 kΩ?

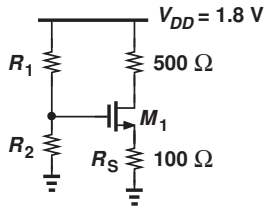


Figure 7.42

7.5. Consider the circuit depicted in Fig. 7.43, where $W/L = 20/0.18$. Assuming the current flowing through R_2 is one-tenth of I_{D1}, calculate the values of R_1 and R_2 so that $I_{D1} = 0.5$ mA.

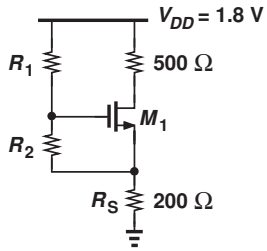


Figure 7.43

7.6. The self-biased stage of Fig. 7.44 must be designed for a drain current of 1 mA. If M_1 is to provide a transconductance of $1/(100\ \Omega)$, calculate the required value of R_D.

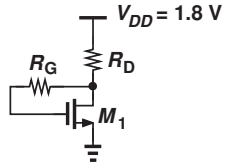


Figure 7.44

7.7. We wish to design the stage in Fig. 7.45 for a drain current of 0.5 mA. If $W/L = 50/0.18$, calculate the values of R_1 and R_2 such that these resistors carry a current equal to one-tenth of I_{D1}.

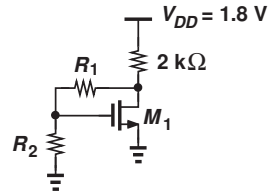


Figure 7.45

*__7.8.__ Due to a manufacturing error, a parasitic resistor, R_P has appeared in the circuit of Fig. 7.46. We know that circuit samples free from this error exhibit $V_{GS} = V_{DS} + 100$ mV whereas defective samples exhibit $V_{GS} = V_{DS} + 50$ mV. Determine the values of W/L and R_P.

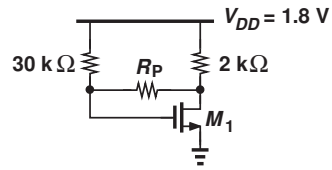


Figure 7.46

*__7.9.__ Due to a manufacturing error, a parasitic resistor, R_P has appeared in the circuit of Fig. 7.47. We know that circuit samples free from this error exhibit $V_{GS} = V_{DS}$ whereas defective samples exhibit $V_{GS} = V_{DS} + V_{TH}$. Determine the values of W/L and R_P if the drain current is 1 mA without R_P.

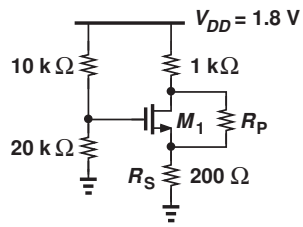


Figure 7.47

Sec. 7.1.3 Realization of Current Sources

7.10. In the circuit of Fig. 7.48, M_1 and M_2 have lengths equal to 0.25 μm and $\lambda = 0.1\ \text{V}^{-1}$. Determine W_1 and W_2 such that $I_X = 2I_Y = 1$ mA. Assume $V_{DS1} = V_{DS2} = V_B = 0.8$ V. What is the output resistance of each current source?

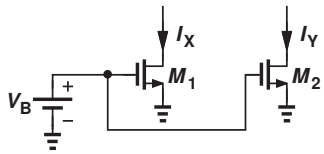


Figure 7.48

7.11. An NMOS current source must be designed for an output resistance of 20 kΩ and an output current of 0.5 mA. What is the maximum tolerable value of λ?

7.12. The two current sources in Fig. 7.49 must be designed for $I_X = I_Y = 0.5$ mA. If $V_{B1} = 1$ V, $V_{B2} = 1.2$ V, $\lambda = 0.1\ \text{V}^{-1}$, and $L_1 = L_2 = 0.25\ \mu$m, calculate W_1 and W_2. Compare the output resistances of the two current sources.

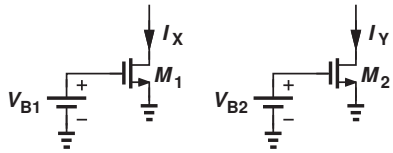


Figure 7.49

7.13. Consider the circuit shown in Fig. 7.50, where $(W/L)_1 = 10/0.18$ and $(W/L)_2 = 30/0.18$. If $\lambda = 0.1\ \text{V}^{-1}$, calculate V_B such that $V_X = 0.9$ V.

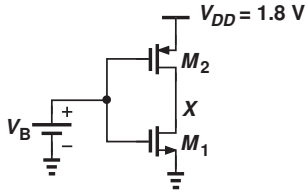


Figure 7.50

7.14. In the circuit of Fig. 7.51, M_1 and M_2 serve as current sources. Calculate I_X and I_Y if $V_B = 1$ V and $W/L = 20/0.25$. How are the output resistances of M_1 and M_2 related?

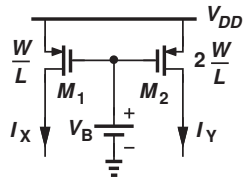


Figure 7.51

*7.15. A student mistakenly uses the circuit of Fig. 7.52 as a current source. If $W/L = 10/0.25$, $\lambda = 0.1\ \text{V}^{-1}$, $V_{B1} = 0.2$ V, and V_X has a dc level of 1.2 V, calculate the impedance seen at the source of M_1.

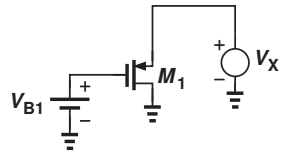


Figure 7.52

**7.16. In the circuit of Fig. 7.53, $(W/L)_1 = 5/0.18$, $(W/L)_2 = 10/0.18$, $\lambda_1 = 0.1\ \text{V}^{-1}$, and $\lambda_2 = 0.15\ \text{V}^{-1}$.

(a) Determine V_B such that $I_{D1} = |I_{D2}| = 0.5$ mA for $V_X = 0.9$ V.

(b) Now sketch I_X as a function of V_X as V_X goes from 0 to V_{DD}.

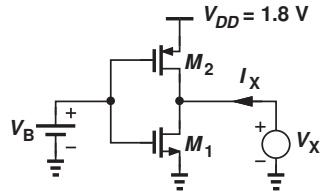


Figure 7.53

Sec. 7.2 Common-Source Stage

7.17. In the common-source stage of Fig. 7.54, $W/L = 30/0.18$ and $\lambda = 0$.

(a) What gate voltage yields a drain current of 0.5 mA? (Verify that M_1 operates in saturation.)

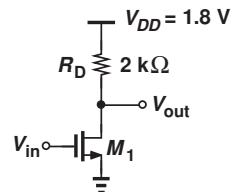


Figure 7.54

(b) With such a drain bias current, calculate the voltage gain of the stage.

7.18. The circuit of Fig. 7.54 is designed with $W/L = 20/0.18$, $\lambda = 0$, and $I_D = 0.25$ mA.
(a) Compute the required gate bias voltage.
(b) With such a gate voltage, how much can W/L be increased while M_1 remains in saturation? What is the maximum voltage gain that can be achieved as W/L increases?

7.19. We wish to design the stage of Fig. 7.55 for a voltage gain of 5 with $W/L \leq 20/0.18$. Determine the required value of R_D if the power dissipation must not exceed 1 mW.

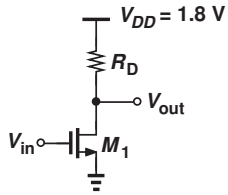


Figure 7.55

7.20. The CS stage of Fig. 7.56 must provide a voltage gain of 10 with a bias current of 0.5 mA. Assume $\lambda_1 = 0.1\ \text{V}^{-1}$, and $\lambda_2 = 0.15\ \text{V}^{-1}$.
(a) Compute the required value of $(W/L)_1$.
(b) If $(W/L)_2 = 20/0.18$, calculate the required value of V_B.

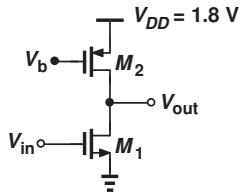


Figure 7.56

7.21. In the stage of Fig. 7.56, M_2 has a long length so that $\lambda_2 \ll \lambda_1$. Calculate the voltage gain if $\lambda_1 = 0.1\ \text{V}^{-1}$, $(W/L)_1 = 20/0.18$, and $I_D = 1$ mA.

****7.22.** The circuit of Fig. 7.56 is designed for a bias current of I_1 with certain dimensions for M_1 and M_2. If the width and the length of both transistors are doubled, how does the voltage gain change? Consider two cases: (a) the bias current remains constant, or (b) the bias current is doubled.

7.23. The CS stage depicted in Fig. 7.57 must achieve a voltage gain of 15 at a bias current of 0.5 mA. If $\lambda_1 = 0.15\ \text{V}^{-1}$ and $\lambda_2 = 0.05\ \text{V}^{-1}$, determine the required value of $(W/L)_2$.

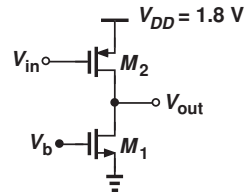


Figure 7.57

7.24. Explain which one of the topologies shown in Fig. 7.58 is preferred.

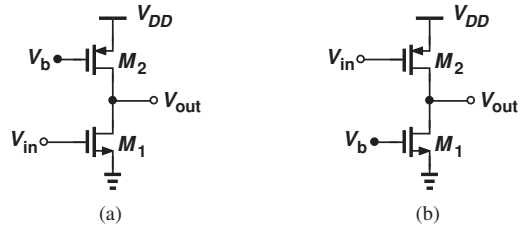


Figure 7.58

7.25. We wish to design the circuit shown in Fig. 7.59 for a voltage gain of 3. If $(W/L)_1 = 20/0.18$, determine $(W/L)_2$. Assume $\lambda = 0$.

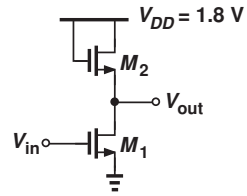


Figure 7.59

7.26. In the circuit of Fig. 7.59, $(W/L)_1 = 10/0.18$ and $I_{D1} = 0.5$ mA.
(a) If $\lambda = 0$, determine $(W/L)_2$ such that M_1 operates at the edge of saturation.
(b) Now calculate the voltage gain.
(c) Explain why this choice of $(W/L)_2$ yields the maximum gain.

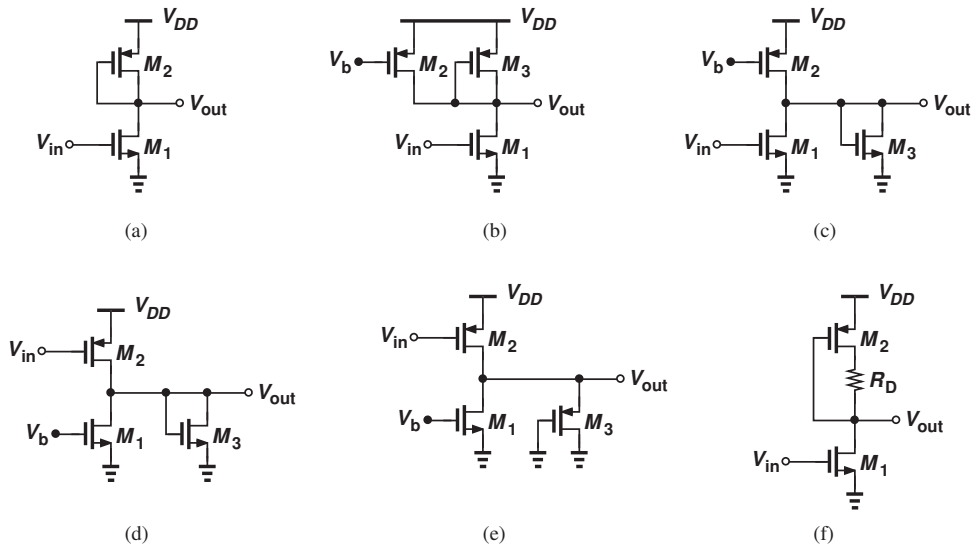


Figure 7.60

7.27. The CS stage of Fig. 7.59 must achieve a voltage gain of 5.
(a) If $(W/L)_2 = 2/0.18$, compute the required value of $(W/L)_1$.
(b) What is the maximum allowable bias current if M_1 must operate in saturation?

****7.28.** If $\lambda \neq 0$, determine the voltage gain of the stages shown in Fig. 7.60.

***7.29.** In the circuit of Fig. 7.61, determine the gate voltage such that M_1 operates at the edge of saturation. Assume $\lambda = 0$.

***7.30.** The degenerated CS stage of Fig. 7.61 must provide a voltage gain of 4 with a bias current of 1 mA. Assume a drop of 200 mV across R_S and $\lambda = 0$.

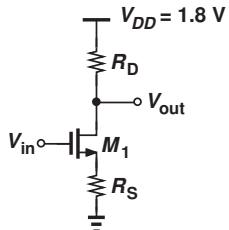


Figure 7.61

(a) If $R_D = 1\,\text{k}\Omega$, determine the required value of W/L. Does the transistor operate in saturation for this choice of W/L?
(b) If $W/L = 50/0.18$, determine the required value of R_D. Does the transistor operate in saturation for this choice of R_D?

****7.31.** Calculate the voltage gain of the circuits depicted in Fig. 7.62. Assume $\lambda = 0$.

****7.32.** Consider a degenerated CS stage with $\lambda > 0$. Assuming $g_m r_O \gg 1$, calculate the voltage gain of the circuit.

***7.33.** Determine the output impedance of each circuit shown in Fig. 7.63. Assume $\lambda \neq 0$.

7.34. The CS stage of Fig. 7.64 carries a bias current of 1 mA. If $R_D = 1\,\text{k}\Omega$ and $\lambda = 0.1\,\text{V}^{-1}$, compute the required value of W/L for a gate voltage of 1 V. What is the voltage gain of the circuit?

7.35. Repeat Problem 7.34 with $\lambda = 0$ and compare the results.

7.36. An adventurous student decides to try a new circuit topology wherein the input is applied to the drain and the output is sensed at the source (Fig. 7.65). Assume $\lambda \neq 0$, determine the voltage gain of the circuit and discuss the result.

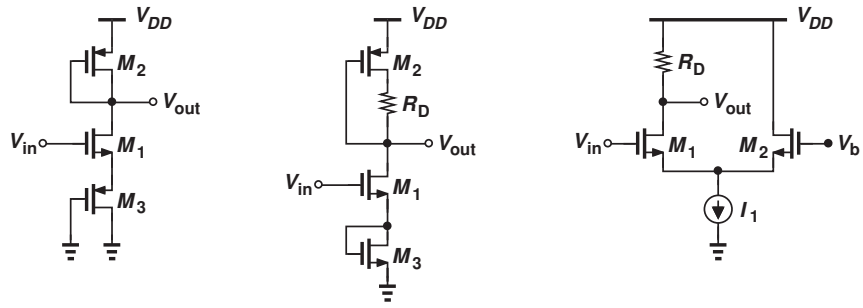


Figure 7.62

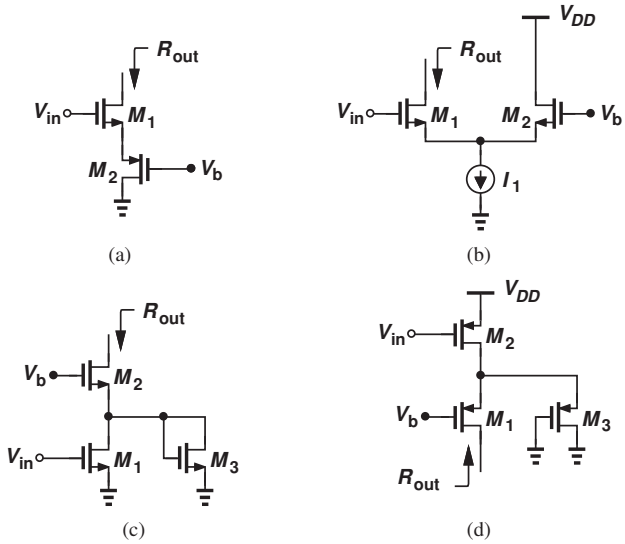


Figure 7.63

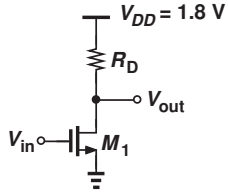


Figure 7.64

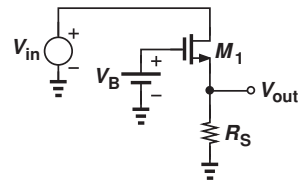


Figure 7.65

7.37. In the common-source stage depicted in Fig. 7.66, the drain current of M_1 is defined by the ideal current source I_1 and remains independent of R_1 and R_2 (why?). Suppose $I_1 = 1$ mA, $R_D = 500\,\Omega$, $\lambda = 0$, and C_1 is very large.

(a) Compute the value of W/L to obtain a voltage gain of 5.

(b) Choose the values of R_1 and R_2 to place the transistor 200 mV away from the triode region while $R_1 + R_2$ draws no more than 0.1 mA from the supply.

(c) With the values found in (b), what happens if W/L is twice that found in (a)? Consider both the bias conditions (e.g., whether M_1 comes closer to the triode region) and the voltage gain.

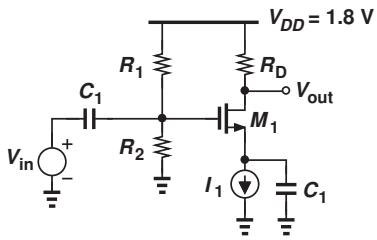


Figure 7.66

7.38. Consider the CS stage shown in Fig. 7.67, where I_1 defines the bias current of M_1 and C_1 is very large.

(a) If $\lambda = 0$ and $I_1 = 1$ mA, what is the maximum allowable value of R_D for M, to remain in saturation?

(b) With the value found in (a), determine W/L to obtain a voltage gain of 5.

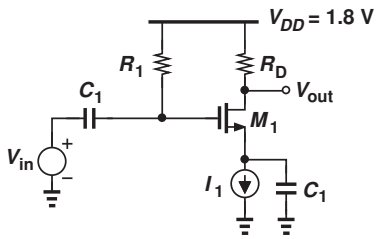


Figure 7.67

Sec. 7.3 Common-Gate Stage

7.39. The common-gate stage shown in Fig. 7.68 must provide a voltage gain of 4 and an input impedance of 50 Ω. If $I_D = 0.5$ mA, and $\lambda = 0$, determine the values of R_D and W/L.

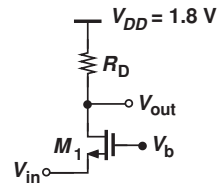


Figure 7.68

7.40. Suppose in Fig. 7.68, $I_D = 0.5$ mA, $\lambda = 0$, and $V_b = 1$ V. Determine the values of W/L and R_D for an input impedance of 50 Ω and maximum voltage gain (while M_1 remains in saturation).

7.41. The CG stage depicted in Fig. 7.69 must provide an input impedance of 50 Ω and an output impedance of 500 Ω. Assume $\lambda = 0$.

(a) What is the maximum allowable value of I_D?

(b) With the value obtained in (a), calculate the required value of W/L.

(c) Compute the voltage gain.

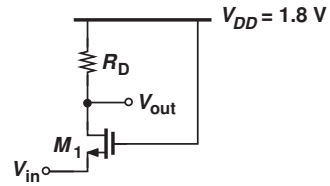


Figure 7.69

*__7.42.__ A CG stage with a source resistance of R_S employs a MOSFET with $\lambda > 0$. Assuming $g_m r_O \gg 1$, calculate the voltage gain of the circuit.

7.43. The CG amplifier shown in Fig. 7.70 is biased by means of $I_1 = 1$ mA. Assume $\lambda = 0$ and C_1 is very large.

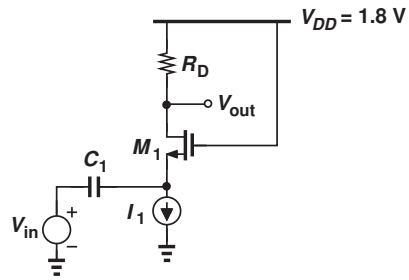


Figure 7.70

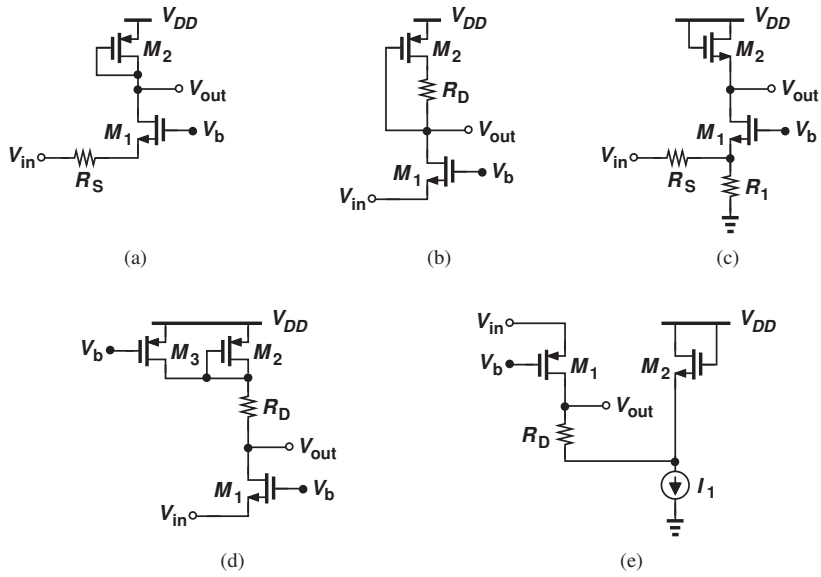


Figure 7.71

(a) What value of R_D places the transistor M_1 100 mV away from the triode region?

(b) What is the required W/L if the circuit must provide a voltage gain of 5 with the value of R_D obtained in (a)?

*7.44. Determine the voltage gain of each stage depicted in Fig. 7.71. Assume $\lambda = 0$.

7.45. Consider the circuit of Fig. 7.72, where a common-source stage (M_1 and R_{D1}) is followed by a common-gate stage (M_2 and R_{D2}).

(a) Writing $v_{out}/v_{in} = (v_X/v_{in})(v_{out}/v_X)$ and assuming $\lambda = 0$, compute the overall voltage gain.

(b) Simplify the result obtained in (a) if $R_{D1} \to \infty$. Explain why this result is to be expected.

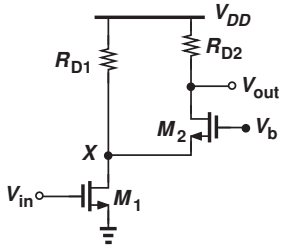


Figure 7.72

7.46. Repeat Problem 7.45 for the circuit shown in Fig. 7.73.

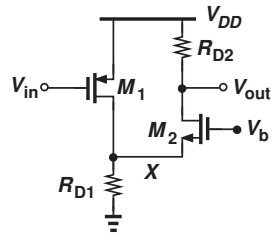


Figure 7.73

7.47. Assuming $\lambda = 0$, calculate the voltage gain of the circuit shown in Fig. 7.74. Explain why this stage is *not* a common-gate amplifier.

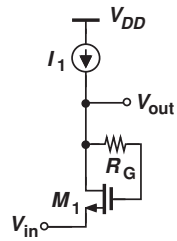


Figure 7.74

7.48. Calculate the voltage gain of the stage depicted in Fig. 7.75. Assume $\lambda = 0$ and the capacitors are very large.

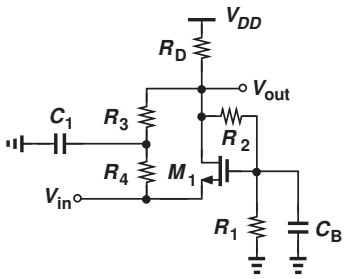


Figure 7.75

Sec. 7.4 Source Follower

7.49. The source follower shown in Fig. 7.76 is biased through R_G. Calculate the voltage gain if $W/L = 20/0.18$ and $\lambda = 0.1\ \text{V}^{-1}$.

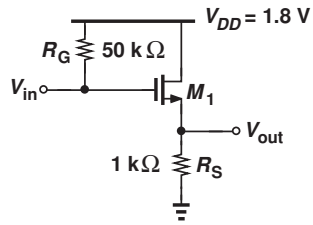


Figure 7.76

7.50. We wish to design the source follower shown in Fig. 7.77 for a voltage gain of 0.8. If $W/L = 30/0.18$ and $\lambda = 0$, determine the required gate bias voltage.

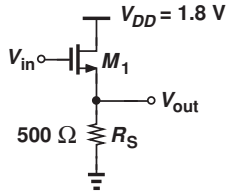


Figure 7.77

7.51. The source follower of Fig. 7.77 is to be designed with a maximum bias gate voltage of 1.8 V. Compute the required value of W/L for a voltage gain of 0.8 if $\lambda = 0$.

7.52. The source follower depicted in Fig. 7.78 employs a current source. Determine the values of I_1 and W/L if the circuit must provide an output impedance less than 100 Ω with $V_{GS} = 0.9$ V. Assume $\lambda = 0$.

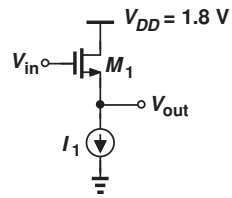


Figure 7.78

7.53. The circuit of Fig. 7.78 must exhibit an output impedance of less than 50 Ω with a power budget of 2 mW. Determine the required value of W/L. Assume $\lambda = 0$.

7.54. We wish to design the source follower of Fig. 7.79 for a voltage gain of 0.8 with a power budget of 3 mW. Compute the required value of W/L. Assume C_1 is very large and $\lambda = 0$.

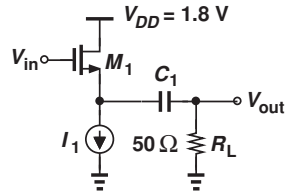


Figure 7.79

*7.55. Determine the voltage gain of the stages shown in Fig. 7.80. Assume $\lambda \neq 0$.

*7.56. Consider the circuit shown in Fig. 7.81, where a source follower (M_1 and I_1) precedes a common-gate stage (M_2 and R_D).

(a) Writing $v_{out}/v_{in} = (v_X/v_{in})(v_{out}/v_X)$, compute the overall voltage gain.

(b) Simplify the result obtained in (a) if $g_{m1} = g_{m2}$.

Design Problems

In the following problems, unless otherwise stated, assume $\lambda = 0$.

7.57. Design the CS stage shown in Fig. 7.82 for a voltage gain of 5 and an output impedance of 1 kΩ. Bias the transistor so that it operates 100 mV away from the triode region. Assume the capacitors are very large and $R_D = 10\ \text{k}\Omega$.

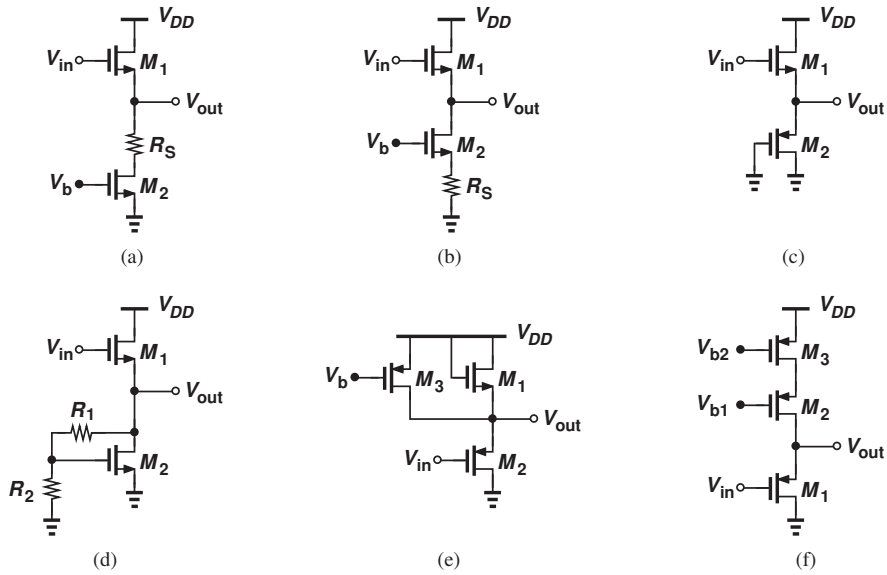


Figure 7.80

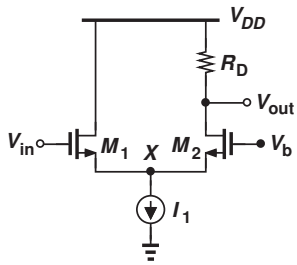


Figure 7.81

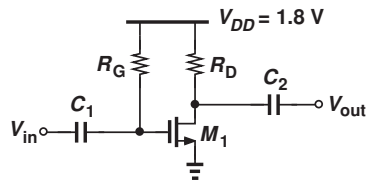


Figure 7.82

7.58. The CS amplifier of Fig. 7.82 must be designed for a voltage gain of 5 with a power budget of 2 mW. If $R_D I_D = 1$ V, determine the required value of W/L. Make the same assumptions as those in Problem 7.57.

7.59. We wish to design the CS stage of Fig. 7.82 for maximum voltage gain but with $W/L \leq 50/0.18$ and a maximum output impedance of 500 Ω. Determine the required current. Make the same assumptions as those in Problem 7.57.

7.60. The degenerated stage depicted in Fig. 7.83 must provide a voltage gain of 4 with a power budget of 2 mW while the voltage drop across R_S is equal to 200 mV. If the overdrive voltage of the transistor must not exceed 300 mV and $R_1 + R_2$ must consume less than than 5% of the allocated power, design the circuit. Make the same assumptions as those in Problem 7.57.

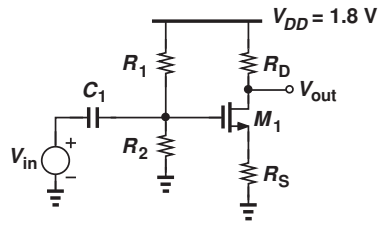


Figure 7.83

7.61. Design the circuit of Fig. 7.83 for a voltage gain of 5 and a power budget of 6 mW. Assume the voltage drop across R_S is equal to the overdrive voltage of the transistor and $R_D = 200$ Ω.

7.62. The circuit shown in Fig. 7.84 must provide a voltage gain of 6, with C_S serving as a low impedance at the frequencies of interest. Assuming a power budget of 2 mW and an input impedance of 20 kΩ, design the circuit such that M_1 operates 200 mV away from the triode region. Select the values of C_1 and C_S so that their impedance is negligible at 1 MHz.

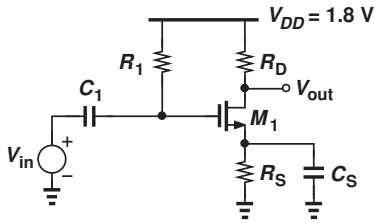


Figure 7.84

7.63. In the circuit of Fig. 7.85, M_2 serves as a current source. Design the stage for a voltage gain of 20 and a power budget of 2 mW. Assume $\lambda = 0.1\ \text{V}^{-1}$ for both transistors and the maximum allowable level at the output is 1.5 V (i.e., M_2 must remain in saturation if $V_{out} \leq 1.5$ V).

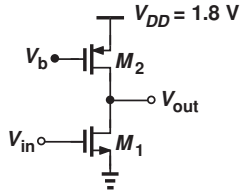


Figure 7.85

7.64. Consider the circuit shown in Fig. 7.86, where C_B is very large and $\lambda_n = 0.5\lambda_p = 0.1\ \text{V}^{-1}$.

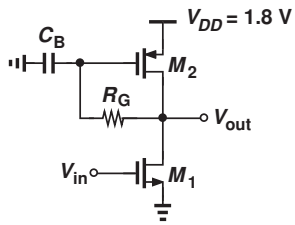


Figure 7.86

(a) Calculate the voltage gain.

(b) Design the circuit for a voltage gain of 15 and a power budget of 3 mW. Assume $R_G \approx 10(r_{O1} \| r_{O2})$ and the dc level of the output must be equal to $V_{DD}/2$.

7.65. The CS stage of Fig. 7.87 incorporates a degenerated PMOS current source. The degeneration must raise the output impedance of the current source to about $10r_{O1}$ such that the voltage gain remains nearly equal to the intrinsic gain of M_1. Assume $\lambda = 0.1\ \text{V}^{-1}$ for both transistors and a power budget of 2 mW.

(a) If $V_B = 1$ V, determine the values of $(W/L)_2$ and R_S so that the impedance seen looking into the drain of M_2 is equal to $10r_{O1}$.

(b) Determine $(W/L)_1$ to achieve a voltage gain of 30.

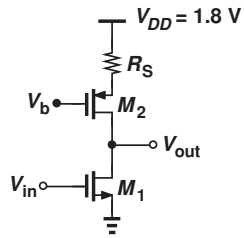


Figure 7.87

7.66. Assuming a power budget of 1 mW and an overdrive of 200 mV for M_1, design the circuit shown in Fig. 7.88 for a voltage gain of 4.

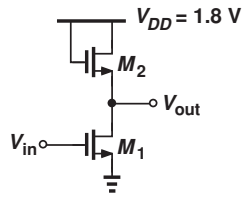


Figure 7.88

7.67. Design the common-gate stage depicted in Fig. 7.89 for an input impedance of 50 Ω and a voltage gain of 5. Assume a power budget of 3 mW.

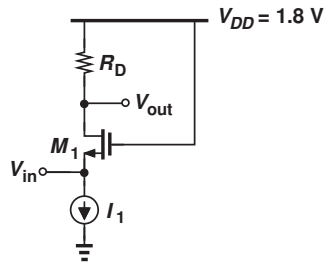


Figure 7.89

7.68. Design the circuit of Fig. 7.90 such that M_1 operates 100 mV away from the triode region while providing a voltage gain of 4. Assume a power budget of 2 mW.

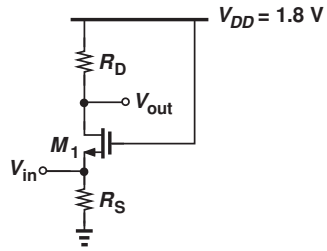


Figure 7.90

7.69. Figure 7.91 shows a self-biased common-gate stage, where $R_G \approx 10R_D$ and C_G serves as a low impedance so that the voltage gain is still given by $g_m R_D$. Design the circuit for a power budget of 5 mW and a voltage gain of 5. Assume $R_S \approx 10/g_m$ so that the input impedance remains approximately equal to $1/g_m$.

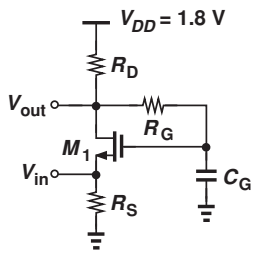


Figure 7.91

7.70. Design the CG stage shown in Fig. 7.92 such that it can accommodate an output swing of 500 mV_{pp}, i.e., V_{out} can fall below its bias value by 250 mV without driving M_1 into the triode region. Assume a voltage gain of 4 and an input impedance of 50 Ω. Select $R_S \approx 10/g_m$ and $R_1 + R_2 = 20\,k\Omega$. (Hint: since M_1 is biased 250 mV away from the triode region, we have $R_S I_D + V_{GS} - V_{TH} + 250\,mV = V_{DD} - I_D R_D$.)

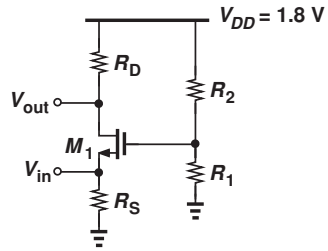


Figure 7.92

7.71. Design the source follower depicted in Fig. 7.93 for a voltage gain of 0.8 and a power budget of 2 mW. Assume the output dc level is equal to $V_{DD}/2$ and the input impedance exceeds 10 kΩ.

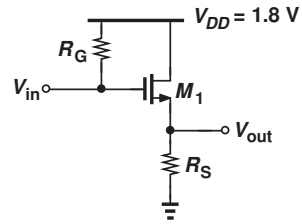


Figure 7.93

7.72. Consider the source follower shown in Fig. 7.94. The circuit must provide a voltage gain of 0.6 at 100 MHz. Design the circuit such that the dc voltage at node X is equal to $V_{DD}/2$. Assume the input impedance exceeds 20 kΩ.

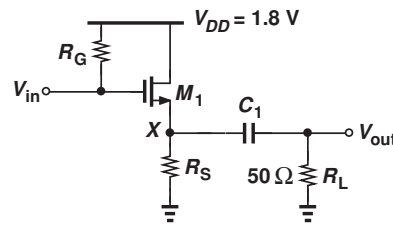


Figure 7.94

7.73. In the source follower of Fig. 7.95, M_2 serves as a current source. The circuit must operate with a power budget of 3 mW, a voltage gain of 0.9, and a minimum allowable output of 0.3 V (i.e., M_2 must remain in saturation if $V_{DS2} \geq 0.3$ V). Assuming $\lambda = 0.1\ \text{V}^{-1}$ for both transistors, design the circuit.

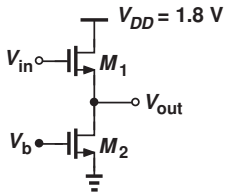


Figure 7.95

SPICE PROBLEMS

In the following problems, use the MOS models and source/drain dimensions given in Appendix A. Assume the substrates of NMOS and PMOS devices are tied to ground and V_{DD}, respectively.

7.74. In the circuit of Fig. 7.96, I_1 is an ideal current source equal to 1 mA.

(a) Using hand calculations, determine $(W/L)_1$ such that $g_{m1} = (100\ \Omega)^{-1}$.

(b) Select C_1 for an impedance of $\approx 100\ \Omega$ ($\ll 1$ kΩ) at 50 MHz.

(c) Simulate the circuit and obtain the voltage gain and output impedance at 50 MHz.

(d) What is the change in the gain if I_1 varies by $\pm 20\%$?

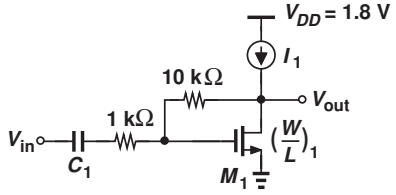


Figure 7.96

7.75. The source follower of Fig. 7.97 employs a bias current source, M_2.

(a) What value of V_{in} places M_2 at the edge of saturation?

(b) What value of V_{in} places M_1 at the edge of saturation?

(c) Determine the voltage gain if V_{in} has a dc value of 1.5 V.

(d) What is the change in the gain if V_b changes by ± 50 mV?

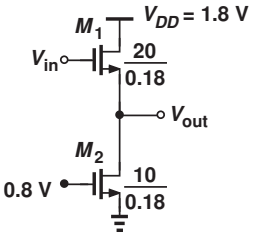


Figure 7.97

7.76. Figure 7.98 depicts a cascade of a source follower and a common-gate stage. Assume $V_b = 1.2$ V and $(W/L)_1 = (W/L)_2 = 10\ \mu\text{m}/0.18\ \mu\text{m}$.

(a) Determine the voltage gain if V_{in} has a dc value of 1.2 V.

(b) Verify that the gain drops if the dc value of V_{in} is higher or lower than 1.2 V.

(c) What dc value at the input reduces the gain by 10% with respect to that obtained in (a)?

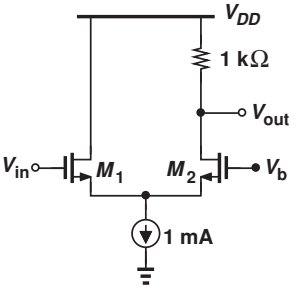


Figure 7.98

7.77. Consider the CS stage shown in Fig. 7.99, where M_2 operates as a resistor.

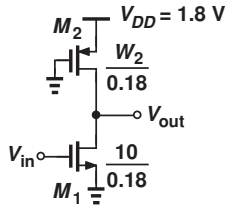


Figure 7.99

(a) Determine W_2 such that an input dc level of 0.8 V yields an output dc level of 1 V. What is the voltage gain under these conditions?

(b) What is the change in the gain if the mobility of the NMOS device varies by ±10%? Can you explain this result using the expressions derived in Chapter 6 for the transconductance?

7.78. Repeat Problem 7.77 for the circuit illustrated in Fig. 7.100 and compare the sensitivities to the mobility.

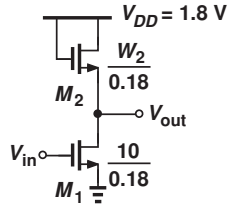


Figure 7.100