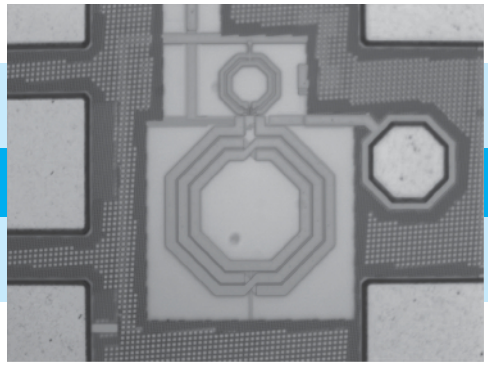


11

Frequency Response

The need for operating circuits at increasingly higher speeds has always challenged designers. From radar and television systems in the 1940s to gigahertz microprocessors today, the demand to push circuits to higher frequencies has required a solid understanding of their speed limitations.

In this chapter, we study the effects that limit the speed of transistors and circuits, identifying topologies that better lend themselves to high-frequency operation. We also develop skills for deriving transfer functions of circuits, a critical task in the study of stability and frequency compensation (12). We assume bipolar transistors remain in the active mode and MOSFETs in the saturation region. The outline is shown below.

Fundamental Concepts
- Bode's Rules
- Association of Poles with Nodes
- Miller's Theorem

➤

High-Frequency Models of Transistors
- Bipolar Model
- MOS Model
- Transit Frequency

➤

Frequency Response of Circuits
- CE/CS Stages
- CB/CG Stages
- Followers
- Cascode Stage
- Differential Pair

11.1 FUNDAMENTAL CONCEPTS

11.1.1 General Considerations

What do we mean by "frequency response?" Illustrated in Fig. 11.1(a), the idea is to apply a sinusoid at the input of the circuit and observe the output while the input frequency is varied. As exemplified by Fig. 11.1(a), the circuit may exhibit a high gain at low frequencies but a "roll-off" as the frequency increases. We plot the magnitude of the gain as in Fig. 11.1(b) to represent the circuit's behavior at all frequencies of interest. We may loosely call f_1 the useful bandwidth of the circuit. Before investigating the cause of this roll-off,

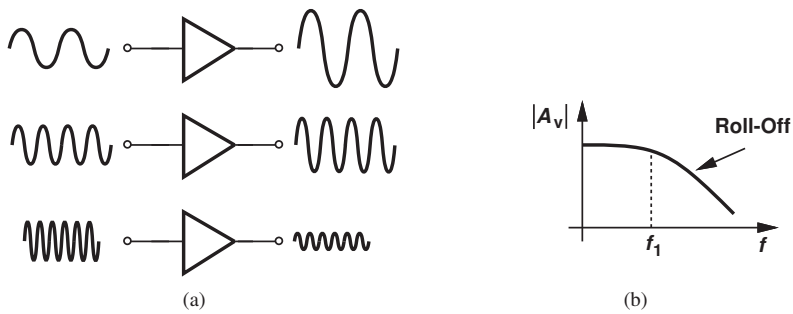


Figure 11.1 (a) Conceptual test of frequency response, (b) gain roll-off with frequency.

we must ask: why is frequency response important? The following examples illustrate the issue.

Example 11.1 Explain why people's voices over the phone sound different from their voices in face-to-face conversation.

Solution The human voice contains frequency components from 20 Hz to 20 kHz [Fig. 11.2(a)]. Thus, circuits processing the voice must accommodate this frequency range. Unfortunately, the phone system suffers from a limited bandwidth, exhibiting the frequency response shown in Fig. 11.2(b). Since the phone suppresses frequencies above 3.5 kHz, each person's voice is altered. In high-quality audio systems, on the other hand, the circuits are designed to cover the entire frequency range.

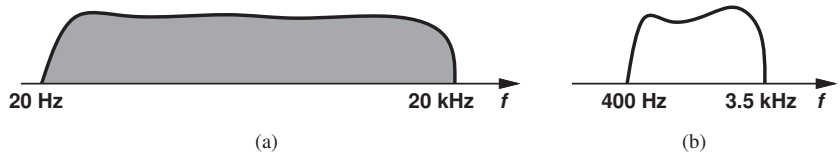


Figure 11.2

Exercise Whose voice does the phone system alter more, men's or women's?

Example 11.2 When you record your voice and listen to it, it sounds somewhat different from the way you hear it directly when you speak. Explain why?

Solution During recording, your voice propagates through the air and reaches the audio recorder. On the other hand, when you speak and listen to your own voice simultaneously, your voice propagates not only through the air but also from your mouth through your skull to your ear. Since the frequency response of the path through your skull is different

from that through the air (i.e., your skull passes some frequencies more easily than others), the way you hear your own voice is different from the way other people hear your voice.

Exercise Explain what happens to your voice when you have a cold.

Example 11.3 Video signals typically occupy a bandwidth of about 5 MHz. For example, the graphics card delivering the video signal to the display of a computer must provide at least 5 MHz of bandwidth. Explain what happens if the bandwidth of a video system is insufficient.

Solution With insufficient bandwidth, the "sharp" edges on a display become "soft," yielding a fuzzy picture. This is because the circuit driving the display is not fast enough to abruptly change the contrast from, e.g., complete white to complete black from one pixel to the next. Figures 11.3(a) and (b) illustrate this effect for a high-bandwidth and low-bandwidth driver, respectively. (The display is scanned from left to right.)

(a) (b)

Figure 11.3

Exercise What happens if the display is scanned from top to bottom?

What causes the gain roll-off in Fig. 11.1? As a simple example, let us consider the low-pass filter depicted in Fig. 11.4(a). At low frequencies, C_1 is nearly open and the current through R_1 nearly zero; thus, $V_{out} = V_{in}$. As the frequency increases, the impedance of C_1 falls and the voltage divider consisting of R_1 and C_1 attenuates V_{in} to a greater extent. The circuit therefore exhibits the behavior shown in Fig. 11.4(b).

As a more interesting example, consider the common-source stage illustrated in Fig. 11.5(a), where a load capacitance, C_L, appears at the output. At low frequencies, the signal current produced by M_1 prefers to flow through R_D because the impedance of

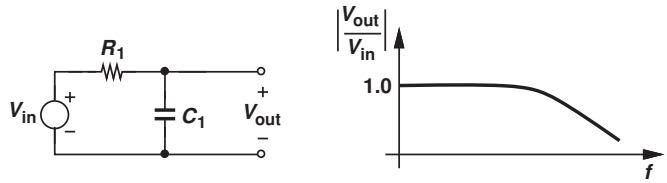
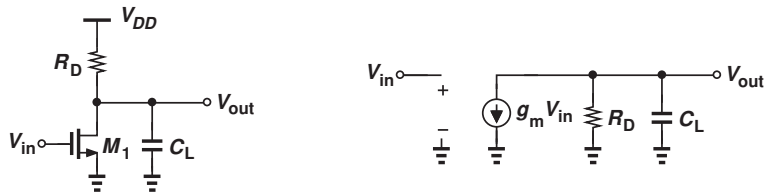


Figure 11.4 (a) Simple low-pass filter, and (b) its frequency response.



(a) (b)

Figure 11.5 (a) CS stage with load capacitance, (b) small-signal model of the circuit.

C_L, $1/(C_L s)$, remains high. At high frequencies, on the other hand, C_L "steals" some of the signal current and shunts it to ground, leading to a lower voltage swing at the output. In fact, from the small-signal equivalent circuit of Fig. 11.5(b),[1] we note that R_D and C_L are in parallel and hence:

$$V_{out} = -g_m V_{in} \left(R_D || \frac{1}{C_L s} \right). \tag{11.1}$$

That is, as the frequency increases, the parallel impedance falls and so does the amplitude of V_{out}.[2] The voltage gain therefore drops at high frequencies.

The reader may wonder why we use *sinusoidal* inputs in our study of frequency response. After all, an amplifier may sense a voice or video signal that bears no resemblance to sinusoids. Fortunately, such signals can be viewed as a summation of many sinusoids with different frequencies (and phases). Thus, responses such as that in Fig. 11.5(b) prove useful so long as the circuit remains linear and hence superposition can be applied.

11.1.2 Relationship Between Transfer Function and Frequency Response

We know from basic circuit theory that the transfer function of a circuit can be written as

$$H(s) = A_0 \frac{\left(1 + \dfrac{s}{\omega_{z1}}\right)\left(1 + \dfrac{s}{\omega_{z2}}\right)\cdots}{\left(1 + \dfrac{s}{\omega_{p1}}\right)\left(1 + \dfrac{s}{\omega_{p2}}\right)\cdots}, \tag{11.2}$$

where A_0 denotes the low-frequency gain because $H(s) \to A_0$ as $s \to 0$. The frequencies ω_{zj} and ω_{pj} represent the zeros and poles of the transfer function, respectively. If the input to the circuit is a sinusoid of the form $x(t) = A \cos(2\pi ft) = A \cos \omega t$, then the output can be expressed as

$$y(t) = A|H(j\omega)|\cos[\omega t + \angle H(j\omega)], \tag{11.3}$$

[1] Channel-length modulation is neglected here.

[2] We use upper-case letters for frequency-domain quantities (Laplace transforms) even though they denote small-signal values.

where $H(j\omega)$ is obtained by making the substitution $s = j\omega$. Called the "magnitude" and the "phase," $|H(j\omega)|$ and $\angle H(j\omega)$ respectively reveal the frequency response of the circuit. In this chapter, we are primarily concerned with the former. Note that f (in Hz) and ω (in radians per second) are related by a factor of 2π. For example, we may write $\omega = 5 \times 10^{10}$ rad/s $= 2\pi(7.96\,\text{GHz})$.

Example 11.4

Determine the transfer function and frequency response of the CS stage shown in Fig. 11.5(a).

Solution

From Eq. (11.1), we have

$$H(s) = \frac{V_{out}}{V_{in}}(s) = -g_m\left(R_D \| \frac{1}{C_L s}\right) \tag{11.4}$$

$$= \frac{-g_m R_D}{R_D C_L s + 1}. \tag{11.5}$$

For a sinusoidal input, we replace $s = j\omega$ and compute the magnitude of the transfer function:[3]

$$\left|\frac{V_{out}}{V_{in}}\right| = \frac{g_m R_D}{\sqrt{R_D^2 C_L^2 \omega^2 + 1}}. \tag{11.6}$$

As expected, the gain begins at $g_m R_D$ at low frequencies, rolling off as $R_D^2 C_L^2 \omega^2$ becomes comparable with unity. At $\omega = 1/(R_D C_L)$,

$$\left|\frac{V_{out}}{V_{in}}\right| = \frac{g_m R_D}{\sqrt{2}}. \tag{11.7}$$

Since $20 \log \sqrt{2} \approx 3$ dB, we say the -3 dB bandwidth of the circuit is equal to $1/(R_D C_L)$ (Fig. 11.6).

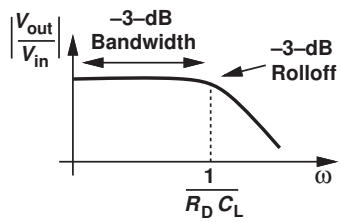


Figure 11.6

Exercise Derive the above results if $\lambda \neq 0$.

[3]The magnitude of the complex number $a + jb$ is equal to $\sqrt{a^2 + b^2}$.

Example 11.5

Consider the common-emitter stage shown in Fig. 11.7. Derive a relationship among the gain, the −3 dB bandwidth, and the power consumption of the circuit. Assume $V_A = \infty$.

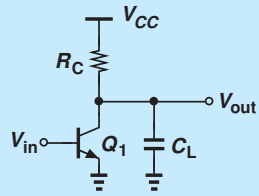


Figure 11.7

Solution

In a manner similar to the CS topology of Fig. 11.5(a), the bandwidth is given by $1/(R_C C_L)$, the low-frequency gain by $g_m R_C = (I_C/V_T)R_C$, and the power consumption by $I_C \cdot V_{CC}$. For the highest performance, we wish to maximize both the gain and the bandwidth (and hence the product of the two) and minimize the power dissipation. We therefore define a "figure of merit" as

$$\frac{\text{Gain} \times \text{Bandwidth}}{\text{Power Consumption}} = \frac{\frac{I_C}{V_T} R_C \times \frac{1}{R_C C_L}}{I_C \cdot V_{CC}} \tag{11.8}$$

$$= \frac{1}{V_T \cdot V_{CC}} \frac{1}{C_L}. \tag{11.9}$$

Thus, the overall performance can be improved by lowering (a) the temperature;[4] (b) V_{CC} but at the cost of limiting the voltage swings; or (c) the load capacitance. In practice, the load capacitance receives the greatest attention. Equation (11.9) becomes more complex for CS stages (Problem 11.15).

Exercise Derive the above results if $V_A < \infty$.

Example 11.6

Explain the relationship between the frequency response and step response of the simple low-pass filter shown in Fig. 11.4(a).

Solution

To obtain the transfer function, we view the circuit as a voltage divider and write

$$H(s) = \frac{V_{out}}{V_{in}}(s) = \frac{\frac{1}{C_1 s}}{\frac{1}{C_1 s} + R_1} \tag{11.10}$$

$$= \frac{1}{R_1 C_1 s + 1}. \tag{11.11}$$

[4]For example, by immersing the circuit in liquid nitrogen ($T = 77$ K), but requiring that the user carry a tank around!

The frequency response is determined by replacing s with $j\omega$ and computing the magnitude:

$$|H(s = j\omega)| = \frac{1}{\sqrt{R_1^2 C_1^2 \omega^2 + 1}}. \tag{11.12}$$

The -3 dB bandwidth is equal to $1/(R_1C_1)$.

The circuit's response to a step of the form $V_0 u(t)$ is given by

$$V_{out}(t) = V_0 \left(1 - \exp \frac{-t}{R_1 C_1}\right) u(t). \tag{11.13}$$

The relationship between Eqs. (11.12) and (11.13) is that, as R_1C_1 increases, the bandwidth *drops* and the step response becomes *slower*. Figure 11.8 plots this behavior, revealing that a narrow bandwidth results in a sluggish time response. This observation explains the effect seen in Fig. 11.3(b): since the signal cannot rapidly jump from low (white) to high (black), it spends some time at intermediate levels (shades of gray), creating "fuzzy" edges.

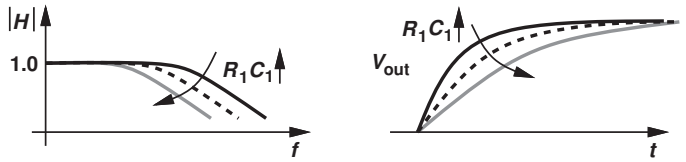


Figure 11.8

Exercise At what frequency does $|H|$ fall by a factor of two?

11.1.3 Bode's Rules

The task of obtaining $|H(j\omega)|$ from $H(s)$ and plotting the result is somewhat tedious. For this reason, we often utilize Bode's rules (approximations) to construct $|H(j\omega)|$ rapidly. Bode's rules for $|H(j\omega)|$ are as follows:

- As ω passes each pole frequency, the slope of $|H(j\omega)|$ *decreases* by 20 dB/dec. (A slope of 20 dB/dec simply means a tenfold change in H for a tenfold increase in frequency);
- As ω passes each zero frequency, the slope of $|H(j\omega)|$ *increases* by 20 dB/dec.[5]

Example 11.7 Construct the Bode plot of $|H(j\omega)|$ for the CS stage depicted in Fig. 11.5(a).

Solution Equation (11.5) indicates a pole frequency of

$$|\omega_{p1}| = \frac{1}{R_D C_L}. \tag{11.14}$$

[5]Complex poles may result in sharp peaks in the frequency response, an effect neglected in Bode's approximation.

The magnitude thus begins at $g_m R_D$ at low frequencies and remains flat up to $\omega = |\omega_{p1}|$. At this point, the slope changes from zero to -20 dB/dec. Figure 11.9 illustrates the result. In contrast to Fig. 11.5(b), the Bode approximation ignores the 3 dB roll-off at the pole frequency—but it greatly simplifies the algebra. As evident from Eq. (11.6), for $R_D^2 C_L^2 \omega^2 \gg 1$, Bode's rule provides a good approximation.

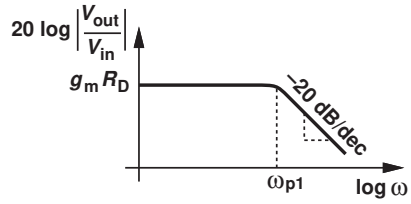


Figure 11.9

Exercise Construct the Bode plot for $g_m = (150\ \Omega)^{-1}$, $R_D = 2\ \text{k}\Omega$, and $C_L = 100\ \text{fF}$.

11.1.4 Association of Poles with Nodes

The poles of a circuit's transfer function play a central role in the frequency response. The designer must therefore be able to identify the poles *intuitively* so as to determine which parts of the circuit appear as the "speed bottleneck."

The CS topology studied in Example 11.4 serves as a good example for identifying poles by inspection. Equation (11.5) reveals that the pole frequency is given by the inverse of the product of the total resistance seen between the output node and ground and the total capacitance seen between the output node and ground. Applicable to many circuits, this observation can be generalized as follows: if node j in the signal path exhibits a small-signal resistance of R_j to ground and a capacitance of C_j to ground, then it contributes a pole of magnitude $(R_j C_j)^{-1}$ to the transfer function.

Did you know?

Bode's rules are an example of "necessity is mother of invention." While working on electronic filters and equalizers at Bell Labs in the 1930s, Hendrik Bode, like other researchers in the field, faced the problem of determining the stability of complex circuits and systems. With no computers or even calculators available, the engineers of that era had to perform lengthy hand calculations for this purpose. Bode thus came up with his approximations of the frequency response and, as seen in Chapter 12, a simple method of studying the stability of feedback systems.

Example 11.8

Determine the poles of the circuit shown in Fig. 11.10. Assume $\lambda = 0$.

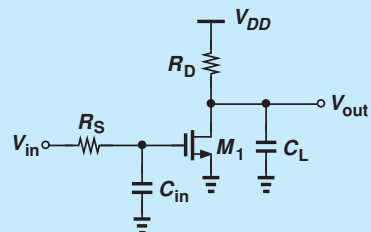


Figure 11.10

Solution Setting V_{in} to zero, we recognize that the gate of M_1 sees a resistance of R_S and a capacitance of C_{in} to ground. Thus,

$$|\omega_{p1}| = \frac{1}{R_S C_{in}}. \tag{11.15}$$

We may call ω_{p1} the "input pole" to indicate that it arises in the input network. Similarly, the "output pole" is given by

$$|\omega_{p2}| = \frac{1}{R_D C_L}. \tag{11.16}$$

Since the low-frequency gain of the circuit is equal to $-g_m R_D$, we can readily write the magnitude of the transfer function as:

$$\left|\frac{V_{out}}{V_{in}}\right| = \frac{g_m R_D}{\sqrt{\left(1+\omega^2/\omega_{p1}^2\right)\left(1+\omega^2\omega_{p2}^2\right)}}. \tag{11.17}$$

Exercise If $\omega_{p1} = \omega_{p2}$, at what frequency does the gain drop by 3 dB?

Example 11.9 Compute the poles of the circuit shown in Fig. 11.11. Assume $\lambda = 0$.

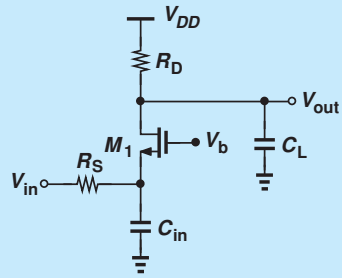


Figure 11.11

Solution With $V_{in} = 0$, the small-signal resistance seen at the source of M_1 is given by $R_S||(1/g_m)$, yielding a pole at

$$\omega_{p1} = \frac{1}{\left(R_S||\dfrac{1}{g_m}\right)C_{in}}. \tag{11.18}$$

The output pole is given by $\omega_{p2} = (R_D C_L)^{-1}$.

Exercise How do we choose the value of R_D such that the output pole frequency is ten times the input pole frequency?

The reader may wonder how the foregoing technique can be applied if a node is loaded with a "floating" capacitor, i.e., a capacitor whose other terminal is also connected to a node in the signal path (Fig. 11.12). In general, we cannot utilize this technique and must

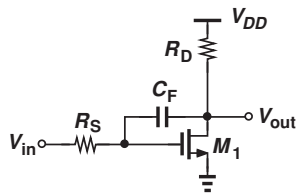


Figure 11.12 Circuit with floating capacitor.

write the circuit's equations and obtain the transfer function. However, an approximation given by "Miller's theorem" can simplify the task in some cases.

11.1.5 Miller's Theorem

Our above study and the example in Fig. 11.12 make it desirable to obtain a method that "transforms" a floating capacitor to two *grounded* capacitors, thereby allowing association of one pole with each node. Miller's theorem is such a method. Miller's theorem, however, was originally conceived for another reason. In the late 1910s, John Miller had observed that parasitic capacitances appearing between the input and output of an amplifier may drastically lower the input impedance. He then proposed an analysis that led to the theorem.

Consider the general circuit shown in Fig. 11.13(a), where the floating impedance, Z_F, appears between nodes 1 and 2. We wish to transform Z_F to two grounded impedances as depicted in Fig. 11.13(b), while ensuring all of the currents and voltages in the circuit remain unchanged. To determine Z_1 and Z_2, we make two observations: (1) the current drawn by Z_F from node 1 in Fig. 11.13(a) must be equal to that drawn by Z_1 in Fig. 11.13(b); and (2) the current injected to node 2 in Fig. 11.13(a) must be equal to that injected by Z_2 in Fig. 11.13(b). (These requirements guarantee that the circuit does not "feel" the transformation.) Thus,

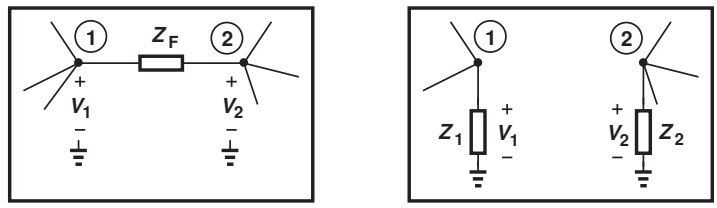
$$\frac{V_1 - V_2}{Z_F} = \frac{V_1}{Z_1} \tag{11.19}$$

$$\frac{V_1 - V_2}{Z_F} = -\frac{V_2}{Z_2}. \tag{11.20}$$

Denoting the voltage gain from node 1 to node 2 by A_v, we obtain

$$Z_1 = Z_F \frac{V_1}{V_1 - V_2} \tag{11.21}$$

$$= \frac{Z_F}{1 - A_v} \tag{11.22}$$



(a) (b)

Figure 11.13 (a) General circuit including a floating impedance, (b) equivalent of (a) as obtained from Miller's theorem.

and

$$Z_2 = Z_F \frac{-V_2}{V_1 - V_2} \tag{11.23}$$

$$= \frac{Z_F}{1 - \dfrac{1}{A_v}}. \tag{11.24}$$

Called Miller's theorem, the results expressed by Eqs. (11.22) and (11.24) prove extremely useful in analysis and design. In particular, Eq. (11.22) suggests that the floating impedance is *reduced* by a factor of $1 - A_v$ when "seen" at node 1.

As an important example of Miller's theorem, let us assume Z_F is a single capacitor, C_F, tied between the input and output of an inverting amplifier [Fig. 11.14(a)]. Applying Eq. (11.22), we have

$$Z_1 = \frac{Z_F}{1 - A_v} \tag{11.25}$$

$$= \frac{1}{(1 + A_0)C_F s}, \tag{11.26}$$

where the substitution $A_v = -A_0$ is made. What type of impedance is Z_1? The $1/s$ dependence suggests a capacitor of value $(1 + A_0)C_F$, as if C_F is "amplified" by a factor of $1 + A_0$. In other words, a capacitor C_F tied between the input and output of an inverting amplifier with a gain of A_0 raises the *input capacitance* by an amount equal to $(1 + A_0)C_F$. We say such a circuit suffers from "Miller multiplication" of the capacitor.

The effect of C_F at the *output* can be obtained from Eq. (11.24):

$$Z_2 = \frac{Z_F}{1 - \dfrac{1}{A_v}} \tag{11.27}$$

$$= \frac{1}{\left(1 + \dfrac{1}{A_0}\right)C_F s}, \tag{11.28}$$

which is close to $(C_F s)^{-1}$ if $A_0 \gg 1$. Figure 11.14(b) summarizes these results.

The Miller multiplication of capacitors can also be explained intuitively. Suppose the input voltage in Fig. 11.14(a) goes up by a small amount ΔV. The output then goes *down* by $A_0 \Delta V$. That is, the voltage across C_F increases by $(1 + A_0)\Delta V$, requiring that the input provide a proportional charge. By contrast, if C_F were not a floating capacitor and its right plate voltage did not change, it would experience only a voltage change of ΔV and require less charge.

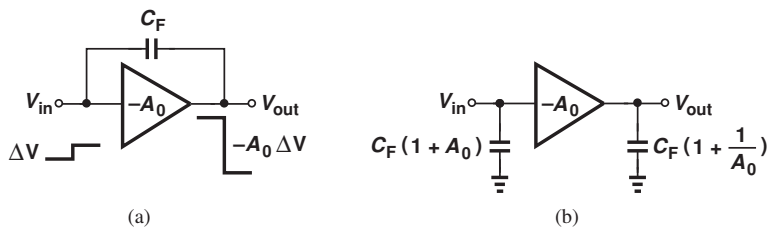
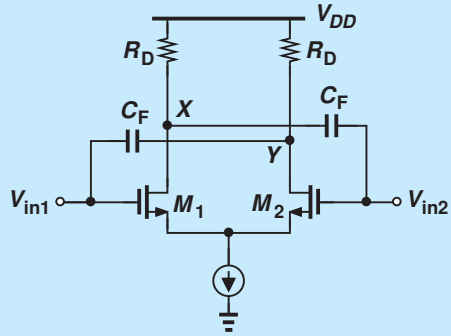


Figure 11.14 (a) Inverting circuit with floating capacitor, (b) equivalent circuit as obtained from Miller's theorem.

The above study points to the utility of Miller's theorem for conversion of floating capacitors to grounded capacitors. The following example demonstrates this principle.

Did you know?

The Miller effect was discovered by John Miller in 1919. In his original paper, Miller observes that "the apparent input capacity can become a number of times greater than the actual capacities between the tube electrodes." (Back then, capacitance and capacitor were called "capacity" and "condensor," respectively.) A curious effect with respect to Miller multiplication is that, if the amplifier gain is *positive* and greater than unity, then we obtain a *negative* input capacitance, $(1 - A_v)C_F$. Does this happen? Yes, indeed. Shown below is a circuit realizing a negative capacitance. Since the gain from V_{in1} to V_Y (and from V_{in2} to V_X) is positive, C_F can be multiplied by a negative number. This technique is used in many high-speed circuits to partially cancel the effect of undesired (positive) capacitances.



Circuit with negative input capacitance.

Example 11.10

Estimate the pole of the circuit shown in Fig. 11.15(a). Assume $\lambda = 0$.

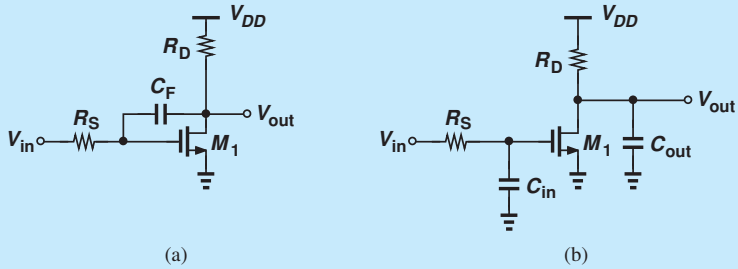


Figure 11.15

Solution

Noting that M_1 and R_D constitute an inverting amplifier having a gain of $-g_m R_D$, we utilize the results in Fig. 11.14(b) to write:

$$C_{in} = (1 + A_0)C_F \tag{11.29}$$

$$= (1 + g_m R_D)C_F \tag{11.30}$$

and

$$C_{out} = \left(1 + \frac{1}{g_m R_D}\right)C_F, \tag{11.31}$$

thereby arriving at the topology depicted in Fig. 11.15(b). From our study in Example 11.8, we have:

$$\omega_{in} = \frac{1}{R_S C_{in}} \tag{11.32}$$

$$= \frac{1}{R_S(1 + g_m R_D)C_F} \tag{11.33}$$

and

$$\omega_{out} = \frac{1}{R_D C_{out}} \tag{11.34}$$

$$= \frac{1}{R_D\left(1 + \frac{1}{g_m R_D}\right) C_F}. \tag{11.35}$$

Why does the circuit in (a) have one pole but that in (b) two? This is explained below.

Exercise Calculate C_{in} if $g_m = (150\ \Omega)^{-1}$, $R_D = 2\ \text{k}\Omega$, and $C_F = 80\ \text{fF}$.

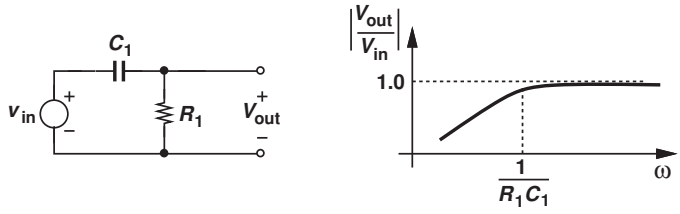
The reader may find the above example somewhat inconsistent. Miller's theorem requires that the floating impedance and the voltage gain be computed *at the same frequency* whereas Example 11.10 uses the *low-frequency* gain, $g_m R_D$, even for the purpose of finding high-frequency poles. After all, we know that the existence of C_F lowers the voltage gain from the gate of M_1 to the output at high frequencies. Owing to this inconsistency, we call the procedure in Example 11.10 the "Miller approximation." Without this approximation, i.e., if A_0 is expressed in terms of circuit parameters at the frequency of interest, application of Miller's theorem would be no simpler than direct solution of the circuit's equations. Due to the approximation, the circuit in the above example exhibits two poles.

Another artifact of Miller's approximation is that it may eliminate a *zero* of the transfer function. We return to this issue in Section 11.4.3.

The general expression in Eq. (11.22) can be interpreted as follows: an impedance tied between the input and output of an inverting amplifier with a gain of A_v is lowered by a factor of $1 + A_v$ if seen at the input (with respect to ground). This reduction of impedance (hence increase in capacitance) is called "Miller effect." For example, we say Miller effect raises the input capacitance of the circuit in Fig. 11.15(a) to $(1 + g_m R_D)C_F$.

11.1.6 General Frequency Response

Our foregoing study indicates that capacitances in a circuit tend to lower the voltage gain at high frequencies. It is possible that capacitors reduce the gain at *low* frequencies as well. As a simple example, consider the high-pass filter shown in Fig. 11.16(a), where the voltage



(a) (b)

Figure 11.16 (a) Simple high-pass filter, and (b) its frequency response.

division between C_1 and R_1 yields

$$\frac{V_{out}}{V_{in}}(s) = \frac{R_1}{R_1 + \dfrac{1}{C_1 s}} \tag{11.36}$$

$$= \frac{R_1 C_1 s}{R_1 C_1 s + 1}, \tag{11.37}$$

and hence

$$\left|\frac{V_{out}}{V_{in}}\right| = \frac{R_1 C_1 \omega}{\sqrt{R_1^2 C_1^2 \omega_1^2 + 1}}. \tag{11.38}$$

Plotted in Fig. 11.16(b), the response exhibits a roll-off as the frequency of operation falls *below* $1/(R_1C_1)$. As seen from Eq. (11.37), this roll-off arises because the zero of the transfer function occurs at the origin.

The low-frequency roll-off may prove undesirable. The following example illustrates this point.

Example 11.11

Figure 11.17 depicts a source follower used in a high-quality audio amplifier. Here, R_i establishes a gate bias voltage equal to V_{DD} for M_1, and I_1 defines the drain bias current. Assume $\lambda = 0$, $g_m = 1/(200\,\Omega)$, and $R_1 = 100$ kΩ. Determine the minimum required value of C_1 and the maximum tolerable value of C_L.

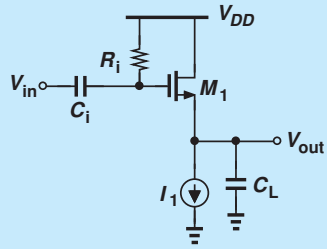


Figure 11.17

Solution

Similar to the high-pass filter of Fig. 11.16, the input network consisting of R_i and C_i attenuates the signal at low frequencies. To ensure that audio components as low as 20 Hz experience a small attenuation, we set the corner frequency $1/(R_iC_i)$ to $2\pi \times (20\,\text{Hz})$, thus obtaining

$$C_i = 79.6\,\text{nF}. \tag{11.39}$$

This value is, of course, much too large to be integrated on a chip. Since Eq. (11.38) reveals a 3 dB attenuation at $\omega = 1/(R_iC_i)$, in practice we must choose even a larger capacitor if a lower attenuation is desired.

The load capacitance creates a pole at the output node, lowering the gain at high frequencies. Setting the pole frequency to the upper end of the audio range, 20 kHz, and recognizing that the resistance seen from the output node to ground is equal to $1/g_m$, we have

$$\omega_{p,out} = \frac{g_m}{C_L} \tag{11.40}$$

$$= 2\pi \times (20\,\text{kHz}), \tag{11.41}$$

and hence

$$C_L = 39.8\,\text{nF}. \tag{11.42}$$

An efficient driver, the source follower can tolerate a very large load capacitance (for the audio band).

Exercise Repeat the above example if I_1 and the width of M_1 are halved.

Why did we use capacitor C_i in the above example? Without C_i, the circuit's gain would not fall at low frequencies, and we would not need perform the above calculations. Called a "coupling" capacitor, C_i allows the signal frequencies of interest to pass through the circuit while blocking the dc content of V_{in}. In other words, C_i isolates the bias conditions of the source follower from those of the *preceding* stage. Figure 11.18(a) illustrates an example in which a CS stage precedes the source follower. The coupling capacitor permits independent bias voltages at nodes X and Y. For example, V_Y can be chosen relatively low (placing M_2 near the triode region) to allow a large drop across R_D, thereby maximizing the voltage gain of the CS stage (why?).

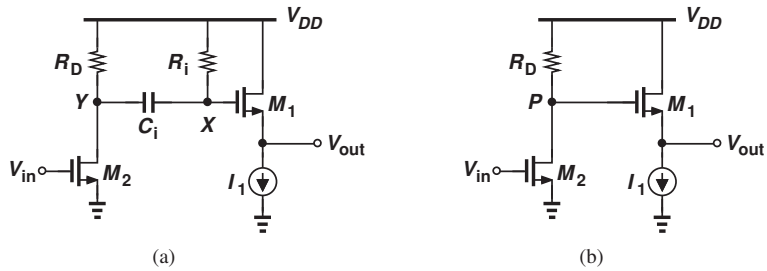


Figure 11.18 Cascade of CS stage and source follower with (a) capacitor coupling and (b) direct coupling.

To convince the reader that capacitive coupling proves essential in Fig. 11.18(a), we consider the case of "direct coupling" [Fig. 11.18(b)] as well. Here, to maximize the voltage gain, we wish to set V_P just above $V_{GS2} - V_{TH2}$, e.g., 200 mV. On the other hand, the gate of M_2 must reside at a voltage of at least $V_{GS1} + V_{I1}$, where V_{I1} denotes the minimum voltage required by I_1. Since $V_{GS1} + V_{I1}$ may reach 600-700 mV, the two stages are quite incompatible in terms of their bias points, necessitating capacitive coupling.

Capacitive coupling (also called "ac coupling") is more common in discrete circuit design due to the large capacitor values required in many applications (e.g., C_i in the above audio example). Nonetheless, many integrated circuits also employ capacitive coupling, especially at low supply voltages, if the necessary capacitor values are no more than a few picofarads.

Figure 11.19 shows a typical frequency response and the terminology used to refer to its various attributes. We call ω_L the lower corner or lower "cut-off" frequency and ω_H the upper corner or upper cut-off frequency. Chosen to accommodate the signal frequencies of interest, the band between ω_L and ω_H is called the "midband range" and the corresponding gain the "midband gain."

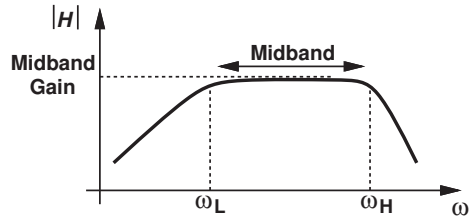


Figure 11.19 Typical frequency response.

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11.2 HIGH-FREQUENCY MODELS OF TRANSISTORS

The speed of many circuits is limited by the capacitances within each transistor. It is therefore necessary to study these capacitances carefully.

11.2.1 High-Frequency Model of Bipolar Transistor

Recall from Chapter 4 that the bipolar transistor consists of two *pn* junctions. The depletion region associated with the junctions[6] gives rise to a capacitance between base and emitter, denoted by C_{je}, and another between base and collector, denoted by C_μ [Fig. 11.20(a)]. We may then add these capacitances to the small-signal model to arrive at the representation shown in Fig. 11.20(b).

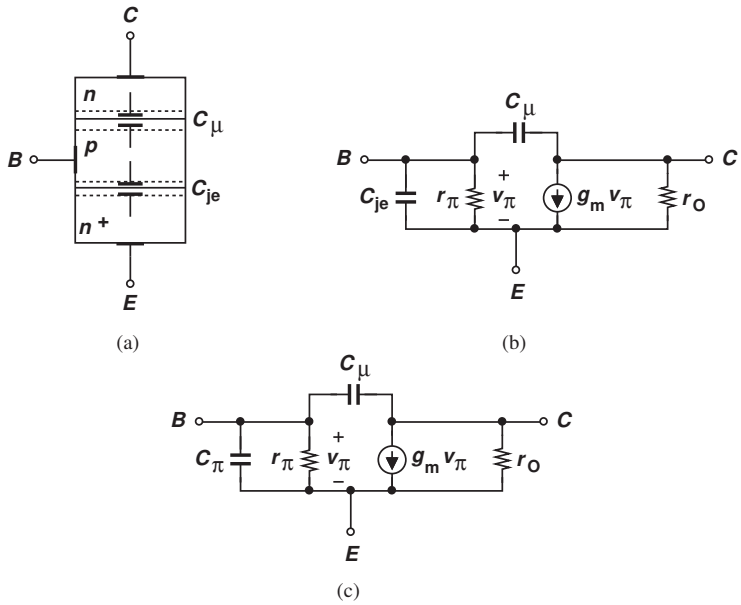


Figure 11.20 (a) Structure of bipolar transistor showing junction capacitances, (b) small-signal model with junction capacitances, (c) complete model accounting for base charge.

Unfortunately, this model is incomplete because the base-emitter junction exhibits another effect that must be taken into account. As explained in Chapter 4, the operation of the transistor requires a (nonuniform) charge profile in the base region to allow the

[6] As mentioned in Chapter 4, both forward-biased and reversed-biased junctions contain a depletion region and hence a capacitance associated with it.

diffusion of carriers toward the collector. In other words, if the transistor is suddenly turned on, proper operation does not begin until enough charge carriers enter the base region and *accumulate* so as to create the necessary profile. Similarly, if the transistor is suddenly turned off, the charge carriers stored in the base must be *removed* for the collector current to drop to zero.

The above phenomenon is quite similar to charging and discharging a capacitor: to change the collector current, we must change the base charge profile by injecting or removing some electrons or holes. Modeled by a second capacitor between the base and emitter, C_b, this effect is typically more significant than the depletion region capacitance. Since C_b and C_{je} appear in parallel, they are lumped into one and denoted by C_π [Fig. 11.20(c)].

In integrated circuits, the bipolar transistor is fabricated atop a grounded substrate [Fig. 11.21(a)]. The collector-substrate junction remains reverse-biased (why?), exhibiting a junction capacitance denoted by C_{CS}. The complete model is depicted in Fig. 11.21(b). We hereafter employ this model in our analysis. In modern integrated-circuit bipolar transistors, C_{je}, C_μ, and C_{CS} are on the order of a few femtofarads for the smallest allowable devices.

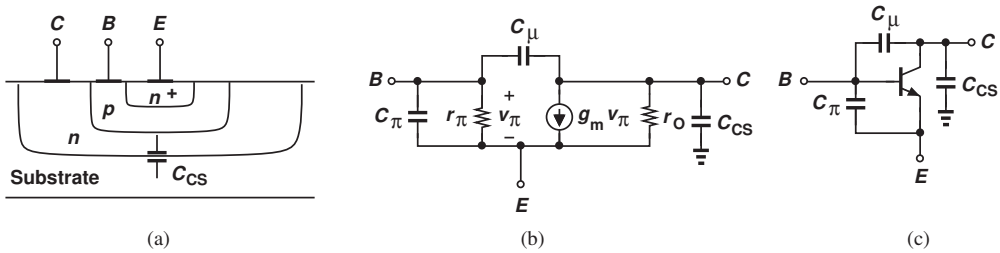


Figure 11.21 (a) Structure of an integrated bipolar transistor, (b) small-signal model including collector-substrate capacitance, (c) device symbol with capacitances shown explicitly.

In the analysis of frequency response, it is often helpful to first draw the transistor capacitances on the circuit diagram, simplify the result, and then construct the small-signal equivalent circuit. We may therefore represent the transistor as shown in Fig. 11.21(c).

Example 11.12

Identify all of the capacitances in the circuit shown in Fig. 11.22(a).

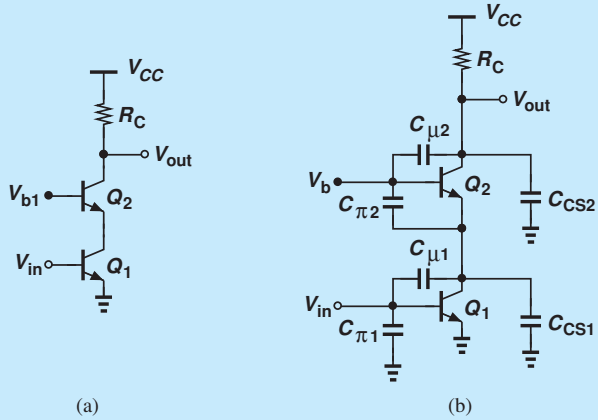


Figure 11.22

Solution From Fig. 11.21(b), we add the three capacitances of each transistor as depicted in Fig. 11.22(b). Interestingly, C_{CS1} and $C_{\pi 2}$ appear in parallel, and so do $C_{\mu 2}$ and C_{CS2}.

Exercise Construct the small-signal equivalent circuit of the above cascode.

11.2.2 High-Frequency Model of MOSFET

Our study of the MOSFET structure in Chapter 6 revealed several capacitive components. We now study these capacitances in the device in greater detail.

Illustrated in Fig. 11.23(a), the MOSFET displays three prominent capacitances: one between the gate and the channel (called the "gate oxide capacitance" and given by WLC_{ox}), and two associated with the reverse-biased source-bulk and drain-bulk junctions. The first component presents a modeling difficulty because the transistor model does not contain a "channel." We must therefore decompose this capacitance into one between the gate and the source and another between the gate and the drain [Fig. 11.23(b)]. The exact partitioning of this capacitance is beyond the scope of this book, but, in the saturation region, C_1 is about 2/3 of the gate-channel capacitance whereas $C_2 \approx 0$.

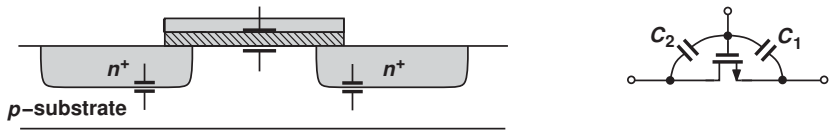


Figure 11.23 (a) Structure of MOS device showing various capacitances, (b) partitioning of gate-channel capacitance between source and drain.

Two other capacitances in the MOSFET become critical in some circuits. Shown in Fig. 11.24, these components arise from both the physical overlap of the gate with source/drain areas[7] and the fringe field lines between the edge of the gate and the top of the S/D regions. Called the gate-drain or gate-source "overlap" capacitance, this (symmetric) effect persists even if the MOSFET is off.

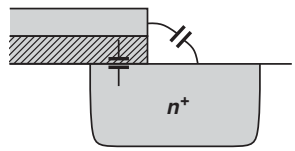


Figure 11.24 Overlap capacitance between gate and drain (or source).

We now construct the high-frequency model of the MOSFET. Depicted in Fig. 11.25(a), this representation consists of: (1) the capacitance between the gate and source, C_{GS} (including the overlap component); (2) the capacitance between the gate and drain (including the overlap component); (3) the junction capacitances between the source and bulk and the drain and bulk, C_{SB} and C_{DB}, respectively. (We assume the bulk remains at ac ground.)

[7] As mentioned in Chapter 6, the S/D areas protrude under the gate during fabrication.

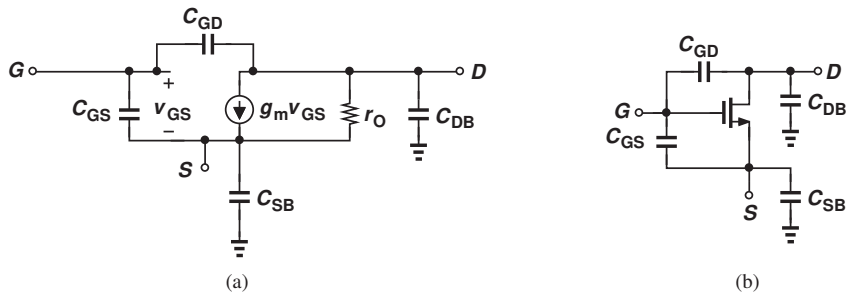


Figure 11.25 (a) High-frequency model of MOSFET, (b) device symbol with capacitances shown explicitly.

As mentioned in Section 11.2.1, we often draw the capacitances on the transistor symbol [Fig. 11.25(b)] before constructing the small-signal model.

Example 11.13

Identify all of the capacitances in the circuit of Fig. 11.26(a).

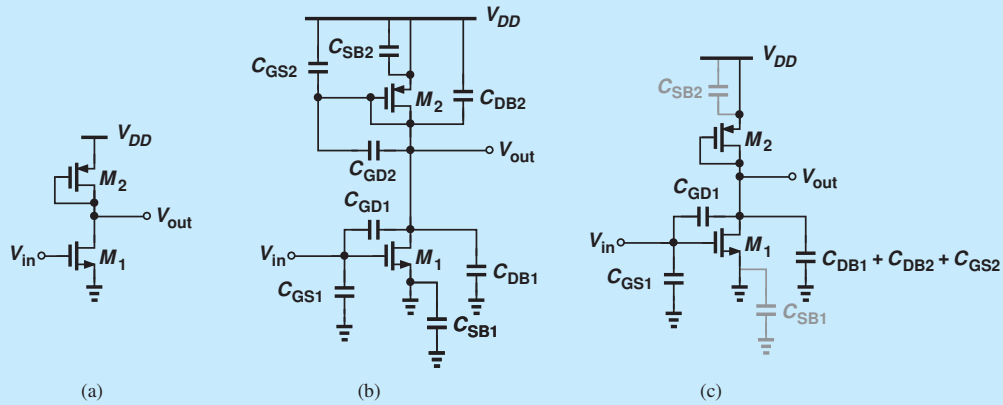


Figure 11.26

Solution

Adding the four capacitances of each device from Fig. 11.25, we arrive at the circuit in Fig. 11.26(b). Note that C_{SB1} and C_{SB2} are shorted to ac ground on both ends, C_{GD2} is shorted "out," and C_{DB1}, C_{DB2}, and C_{GS2} appear in parallel at the output node. The circuit therefore reduces to that in Fig. 11.26(c).

Exercise

Noting that M_2 is a diode-connected device, construct the small-signal equivalent circuit of the amplifier.

11.2.3 Transit Frequency

With various capacitances surrounding bipolar and MOS devices, is it possible to define a quantity that represents the ultimate speed of the transistor? Such a quantity would prove useful in comparing different types or generations of transistors as well as in predicting the performance of circuits incorporating the devices.

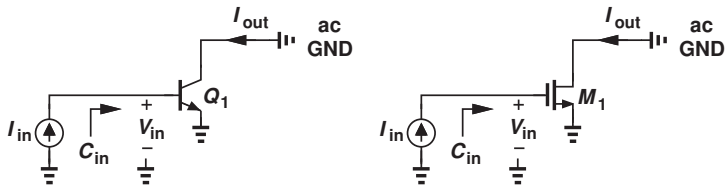


Figure 11.27 Conceptual setup for measurement of f_T of transistors.

A measure of the intrinsic speed of transistors[8] is the "transit" or "cut-off" frequency, f_T, defined as the frequency at which the small-signal *current gain* of the device falls to unity. Illustrated in Fig. 11.27 (without the biasing circuitry), the idea is to inject a sinusoidal current into the base or gate and measure the resulting collector or drain current while the input frequency, f_{in}, is increased. We note that, as f_{in} increases, the input capacitance of the device lowers the input impedance, Z_{in}, and hence the input voltage $V_{in} = I_{in}Z_{in}$ and the output current. We neglect C_μ and C_{GD} here (but take them into account in Problem 11.26). For the bipolar device in Fig. 11.27(a),

$$Z_{in} = \frac{1}{C_\pi s} || r_\pi. \tag{11.43}$$

Since $I_{out} = g_m I_{in} Z_{in}$,

$$\frac{I_{out}}{I_{in}} = \frac{g_m r_\pi}{r_\pi C_\pi s + 1} \tag{11.44}$$

$$= \frac{\beta}{r_\pi C_\pi s + 1}. \tag{11.45}$$

At the transit frequency, $\omega_T (= 2\pi f_T)$, the magnitude of the current gain falls to unity:

$$r_\pi^2 C_\pi^2 \omega_T^2 = \beta^2 - 1 \tag{11.46}$$

$$\approx \beta^2. \tag{11.47}$$

That is,

$$\omega_T \approx \frac{g_m}{C_\pi}. \tag{11.48}$$

The transit frequency of MOSFETs is obtained in a similar fashion. We therefore write:

$$2\pi f_T \approx \frac{g_m}{C_\pi} \quad \text{or} \quad \frac{g_m}{C_{GS}}. \tag{11.49}$$

Note that the collector-substrate or drain-bulk capacitance does not affect f_T owing to the ac ground established at the output.

Modern bipolar and MOS transistors boast f_T's above 100 GHz. Of course, the speed of complex circuits using such devices is quite lower.

Example 11.14

The minimum channel length of MOSFETs has been scaled from 1 μm in the late 1980s to 65 nm today. Also, the inevitable reduction of the supply voltage has reduced the gate-source overdive voltage from about 400 mV to 100 mV. By what factor has the f_T of MOSFETs increased?

[8] By "intrinsic" speed, we mean the performance of the device *by itself*, without any other limitations imposed or enhancements provided by the circuit.

Solution It can proved (Problem 11.28) that

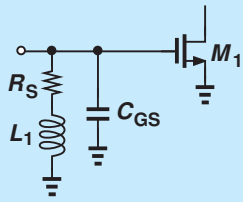
$$2\pi f_T = \frac{3}{2}\frac{\mu_n}{L^2}(V_{GS} - V_{TH}). \tag{11.50}$$

Thus, the transit frequency has increased by approximately a factor of 59. For example, if $\mu_n = 400\ \text{cm}^2/(\text{V}\cdot\text{s})$, then 65 nm devices having an overdrive of 100 mV exhibit an f_T of 226 GHz.

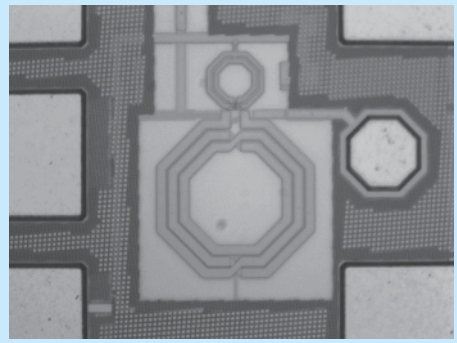
Exercise Determine the f_T if the channel length is scaled down to 45 nm but the mobility degrades to $300\ \text{cm}^2/(\text{V}\cdot\text{s})$.

Did you know?

If the f_T of 65 nm MOSFETs is around 220 GHz, is it possible to operate such a device at a higher frequency? Yes, indeed. The key is to use inductors to cancel the effect of capacitors. Suppose as shown in Fig. (a), we place inductor L_1 in parallel with C_{GS}. (Realized as a metal spiral on the chip, the inductor has some resistance, R_S.) At the resonance frequency, $\omega_O = 1/\sqrt{L_1 C_{GS}}$, the parallel combination reduces to a single resistor, almost as if M_1 had no gate-source capacitance! For this reason, the use of on-chip inductors has become common in high-frequency design. Figure (b) shows the chip photograph of a 300 GHz oscillator designed by the author in 65 nm technology. Such high frequencies find application in medical imaging.



(a)



(b)

(a) Use of resonance to cancel transistor capacitance, (b) chip photograph of a 300 GHz CMOS oscillator.

11.3 ANALYSIS PROCEDURE

We have thus far seen a number of concepts and tools that help us study the frequency response of circuits. Specifically, we have observed that:

- The frequency response refers to the magnitude of the transfer function of a system.[9]
- Bode's approximation simplifies the task of plotting the frequency response if the poles and zeros are known.

[9]In a more general case, the frequency response also includes the phase of the transfer function, as studied in Chapter 12.

- In many cases, it is possible to associate a pole with each node in the signal path.
- Miller's theorem proves helpful in decomposing floating capacitors into grounded elements.
- Bipolar and MOS devices exhibit various capacitances that limit the speed of circuits.

In order to methodically analyze the frequency response of various circuits, we prescribe the following steps:

1. Determine which capacitors impact the low-frequency region of the response and compute the low-frequency cut-off. In this calculation, the transistor capacitances can be neglected as they typically impact only the high-frequency region.
2. Calculate the midband gain by replacing the above capacitors with short circuits while still neglecting the transistor capacitances.
3. Identify and add to the circuit the capacitances contributed by each transistor.
4. Noting ac grounds (e.g., the supply voltage or constant bias voltages), merge the capacitors that are in parallel and omit those that play no role in the circuit.
5. Determine the high-frequency poles and zeros by inspection or by computing the transfer function. Miller's theorem may prove useful here.
6. Plot the frequency response using Bode's rules or exact calculations.

We now apply this procedure to various amplifier topologies.

11.4 FREQUENCY RESPONSE OF CE AND CS STAGES

11.4.1 Low-Frequency Response

As mentioned in Section 11.1.6, the gain of amplifiers may fall at low frequencies due to certain capacitors in the signal path. Let us consider a general CS stage with its input bias network and an input coupling capacitor [Fig. 11.28(a)]. At low frequencies, the transistor capacitances negligibly affect the frequency response, leaving only C_i as the frequency-dependent component. We write $V_{out}/V_{in} = (V_{out}/V_X)(V_X/V_{in})$, neglect channel-length modulation, and note that both R_1 and R_2 are tied between X and ac ground. Thus, $V_{out}/V_X = -R_D/(R_S + 1/g_m)$ and

$$\frac{V_X}{V_{in}}(s) = \frac{R_1||R_2}{R_1||R_2 + \dfrac{1}{C_i s}} \tag{11.51}$$

$$= \frac{(R_1||R_2)C_i s}{(R_1||R_2)C_i s + 1}. \tag{11.52}$$

Similar to the high-pass filter of Fig. 11.16, this network attenuates the low frequencies, dictating that the lower cut-off be chosen below the lowest signal frequency, $f_{sig,min}$ (e.g., 20 Hz in audio applications):

$$\frac{1}{2\pi[(R_1||R_2)C_i]} < f_{sig,min}. \tag{11.53}$$

In applications demanding a greater midband gain, we place a "bypass" capacitor in parallel with R_S [Fig. 11.28(b)] so as to remove the effect of degeneration at midband frequencies. To quantify the role of C_b, we place its impedance, $1/(C_b s)$, in parallel with R_S

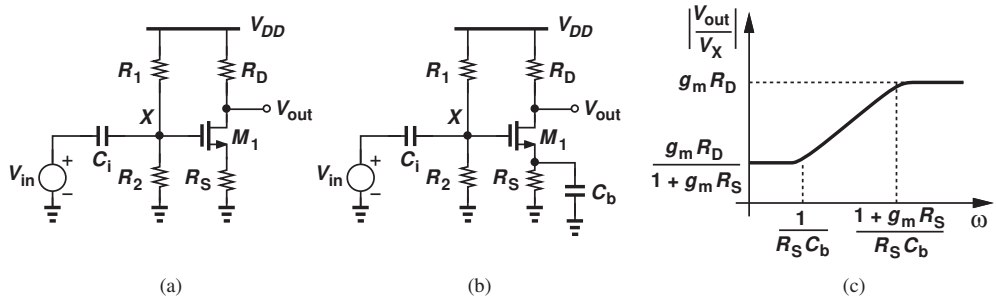


Figure 11.28 (a) CS stage with input coupling capacitor, (b) effect of bypassed degeneration, (c) frequency response with bypassed degeneration.

in the midband gain expression:

$$\frac{V_{out}}{V_X}(s) = \frac{-R_D}{R_S || \dfrac{1}{C_b s} + \dfrac{1}{g_m}} \tag{11.54}$$

$$= \frac{-g_m R_D (R_S C_b s + 1)}{R_S C_b s + g_m R_S + 1}. \tag{11.55}$$

Figure 11.28(c) shows the Bode plot of the frequency response in this case. At frequencies well below the zero, the stage operates as a degenerated CS amplifier, and at frequencies well above the pole, the circuit experiences no degeneration. Thus, the pole frequency must be chosen significantly smaller than the lowest signal frequency of interest.

The above analysis can also be applied to a CE stage. Both types exhibit low-frequency roll-off due to the input coupling capacitor and the degeneration bypass capacitor.

11.4.2 High-Frequency Response

Consider the CE and CS amplifiers shown in Fig. 11.29(a), where R_S may represent the output impedance of the preceding stage, i.e., it is not added deliberately. Identifying the capacitances of Q_1 and M_1, we arrive at the complete circuits depicted in Fig. 11.29(b), where the source-bulk capacitance of M_1 is grounded on both ends. The small-signal equivalents of these circuits differ by only r_π [Fig. 11.29(c)],[10] and can be reduced to one if V_{in}, R_S and r_π are replaced with their Thevenin equivalent [Fig. 11.29(d)]. In practice, $R_S \ll r_\pi$ and hence $R_{Thev} \approx R_S$. Note that the output resistance of each transistor would simply appear in parallel with R_L.

With this unified model, we now study the high-frequency response, first applying Miller's approximation to develop insight and then performing an accurate analysis to arrive at more general results.

11.4.3 Use of Miller's Theorem

With C_{XY} tied between two floating nodes, we cannot simply associate one pole with each node. However, following Miller's approximation as in Example 11.10, we can decompose

[10]The Early effect and channel-length modulation are neglected here.

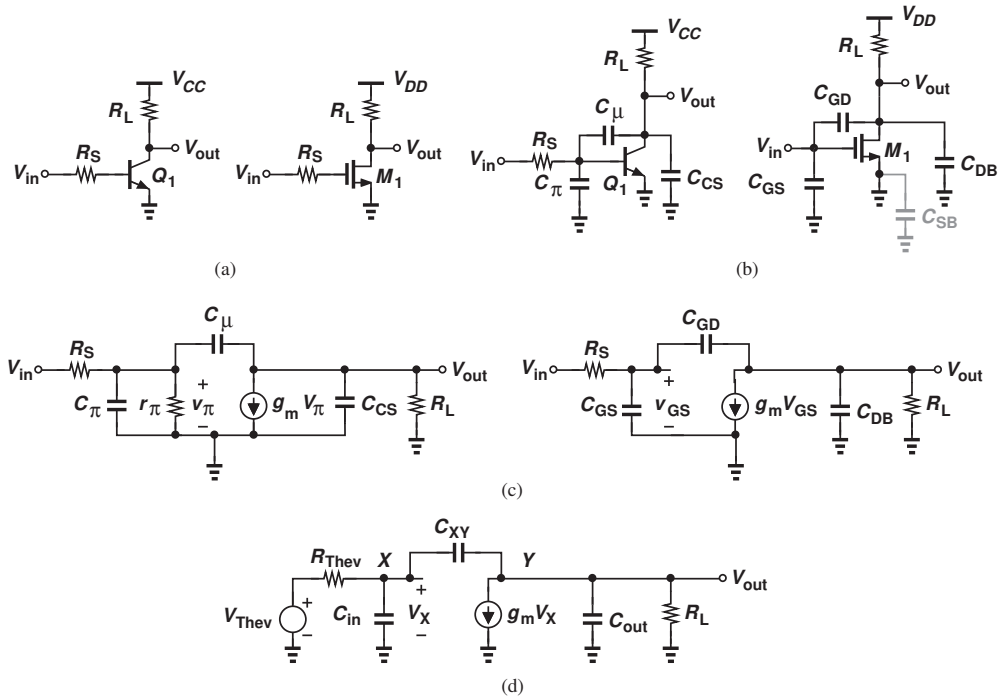
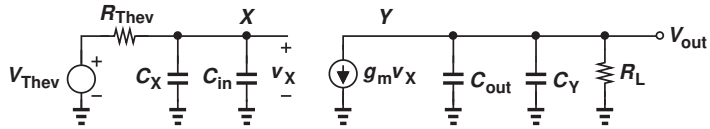


Figure 11.29 (a) CE and CS stages, (b) inclusion of transistor capacitances, (c) small-signal equivalents, (d) unified model of both circuits.

C_{XY} into two grounded components (Fig. 11.30):

$$C_X = (1 + g_m R_L) C_{XY} \tag{11.56}$$

$$C_Y = \left(1 + \frac{1}{g_m R_L}\right) C_{XY}. \tag{11.57}$$



CE Stage	CS Stage
$V_{Thev} = V_{in} \dfrac{r_\pi}{r_\pi + R_S}$	$V_{Thev} = V_{in}$
$R_{Thev} = R_S \parallel r_\pi$	$R_{Thev} = R_S$
$C_X = C_\mu (1 + g_m R_L)$	$C_X = C_{GD} (1 + g_m R_L)$
$C_Y = C_\mu \left(1 + \dfrac{1}{g_m R_L}\right)$	$C_Y = C_{GD} \left(1 + \dfrac{1}{g_m R_L}\right)$

Figure 11.30 Parameters in unified model of CE and CS stages with Miller's approximation.

Now, each node sees a resistance and capacitances only to ground. In accordance with our notations in Section 11.1, we write

$$|\omega_{p,in}| = \frac{1}{R_{Thev}[C_{in} + (1 + g_m R_L)C_{XY}]} \tag{11.58}$$

$$|\omega_{p,out}| = \frac{1}{R_L\left[C_{out} + \left(1 + \frac{1}{g_m R_L}\right)C_{XY}\right]}. \tag{11.59}$$

If $g_m R_L \gg 1$, the capacitance at the output node is simply equal to $C_{out} + C_{XY}$.

The intuition gained from the application of Miller's theorem proves invaluable. The input pole is approximately given by the source resistance, the base-emitter or gate-source capacitance, and the *Miller multiplication* of the base-collector or gate-drain capacitance. The Miller multiplication makes it undesirable to have a high gain in the circuit. The output pole is roughly determined by the load resistance, the collector-substrate or drain-bulk capacitance, and the base-collector or gate-drain capacitance.

Example 11.15

In the CE stage of Fig. 11.29(a), $R_S = 200\,\Omega$, $I_C = 1$ mA, $\beta = 100$, $C_\pi = 100$ fF, $C_\mu = 20$ fF, and $C_{CS} = 30$ fF.

(a) Calculate the input and output poles if $R_L = 2\,\text{k}\Omega$. Which node appears as the speed bottleneck (limits the bandwidth)?

(b) Is it possible to choose R_L such that the output pole limits the bandwidth?

Solution

(a) Since $r_\pi = 2.6\,\text{k}\Omega$, we have $R_{Thev} = 186\,\Omega$. Fig. 11.30 and Eqs. (11.58) and (11.59) thus give

$$|\omega_{p,in}| = 2\pi \times (516\,\text{MHz}) \tag{11.60}$$

$$|\omega_{p,out}| = 2\pi \times (1.59\,\text{GHz}). \tag{11.61}$$

We observe that the Miller effect multiplies C_μ by a factor of 78, making its contribution much greater than that of C_π. As a result, the input pole limits the bandwidth.

(b) We must seek such a value of R_L that yields $|\omega_{p,in}| > \omega_{p,out}|$:

$$\frac{1}{(R_S||r_\pi)[C_\pi + (1 + g_m R_L)C_\mu]} > \frac{1}{R_L\left[C_{CS} + \left(1 + \frac{1}{g_m R_L}\right)C_\mu\right]}. \tag{11.62}$$

If $g_m R_L \gg 1$, then we have

$$[C_{CS} + C_\mu - g_m(R_S||r_\pi)C_\mu]R_L > (R_S||r_\pi)C_\pi. \tag{11.63}$$

With the values assumed in this example, the left-hand side is negative, implying that no solution exists. The reader can prove that this holds even if $g_m R_L$ is not much greater than unity. Thus, the input pole remains the speed bottleneck here.

Exercise Repeat the above example if $I_C = 2$ mA and $C_\pi = 180$ fF.

Example 11.16

An electrical engineering student designs the CS stage of Fig. 11.29(a) for a certain low-frequency gain and high-frequency response. Unfortunately, in the layout phase, the student uses a MOSFET half as wide as that in the original design. Assuming that the bias current is also halved, determine the gain and the poles of the circuit.

Solution

Both the width and the bias current of the transistor are halved, and so is its transconductance (why?). The small-signal gain, $g_m R_L$, is therefore halved.

Reducing the transistor width by a factor of two also lowers all of the capacitances by the same factor. From Fig. 11.30 and Eqs. (11.58) and (11.59), we can express the poles as

$$|\omega_{p,in}| = \frac{1}{R_S\left[\frac{C_{in}}{2} + \left(1 + \frac{g_m R_L}{2}\right)\frac{C_{XY}}{2}\right]} \tag{11.64}$$

$$|\omega_{p,out}| = \frac{1}{R_L\left[\frac{C_{out}}{2} + \left(1 + \frac{2}{g_m R_L}\right)\frac{C_{XY}}{2}\right]}, \tag{11.65}$$

where C_{in}, g_m, C_{XY} and C_{out} denote the parameters corresponding to the original device width. We observe that $\omega_{p,in}$ has risen in magnitude by more than a factor of two, and $\omega_{p,out}$ by approximately a factor of two (if $g_m R_L \gg 2$). In other words, the gain is halved and the bandwidth is roughly doubled, suggesting that the gain-bandwidth product is approximately constant.

Exercise

What happens if both the width and the bias current are twice their nominal values?

11.4.4 Direct Analysis

The use of Miller's theorem in the previous section provides a quick and intuitive perspective on the performance. However, we must carry out a more accurate analysis so as to understand the limitations of Miller's approximation in this case.

The circuit of Fig. 11.29(d) contains two nodes and can therefore be solved by writing two KCLs. That is,[11]

$$\text{At Node } X\text{: } (V_{out} - V_X)C_{XY}s = V_X C_{in}s + \frac{V_X - V_{Thev}}{R_{Thev}} \tag{11.66}$$

$$\text{At Node } Y\text{: } (V_X - V_{out})C_{XY}s = g_m V_X + V_{out}\left(\frac{1}{R_L} + C_{out}s\right). \tag{11.67}$$

We compute V_X from Eq. (11.67):

$$V_X = V_{out}\frac{C_{XY}s + \frac{1}{R_L} + C_{out}s}{C_{XY}s - g_m} \tag{11.68}$$

[11] Recall that we denote frequency-domain quantities with upper-case letters.

and substitute the result in Eq. (11.66) to arrive at

$$V_{out}C_{XY}s - \left(C_{XY}s + C_{in}s + \frac{1}{R_{Thev}}\right)\frac{C_{XY}s + \dfrac{1}{R_L} + C_{out}s}{C_{XY}s - g_m}V_{out} = \frac{-V_{Thev}}{R_{Thev}}. \tag{11.69}$$

It follows that

$$\frac{V_{out}}{V_{Thev}}(s) = \frac{(C_{XY}s - g_m)R_L}{as^2 + bs + 1}, \tag{11.70}$$

where

$$a = R_{Thev}R_L(C_{in}C_{XY} + C_{out}C_{XY} + C_{in}C_{out}) \tag{11.71}$$

$$b = (1 + g_mR_L)C_{XY}R_{Thev} + R_{Thev}C_{in} + R_L(C_{XY} + C_{out}). \tag{11.72}$$

Note from Fig. 11.30 that for a CE stage, Eq. (11.70) must be multiplied by $r_\pi/(R_S + r_\pi)$ to obtain V_{out}/V_{in}—without affecting the location of the poles and the zero.

Let us examine the above results carefully. The transfer function exhibits a zero at

$$\omega_z = \frac{g_m}{C_{XY}}. \tag{11.73}$$

(The Miller approximation fails to predict this zero.) Since C_{XY} (i.e., the base-collector or the gate-drain overlap capacitance) is relatively small, the zero typically appears at very high frequencies and hence is unimportant.[12]

As expected, the system contains two poles given by the values of s that force the denominator to zero. We can solve the quadratic $as^2 + bs + 1 = 0$ to determine the poles but the results provide little insight. Instead, we first make an interesting observation in regard to the quadratic denominator: if the poles are given by ω_{p1} and ω_{p2}, we can write

$$as^2 + bs + 1 = \left(\frac{s}{\omega_{p1}} + 1\right)\left(\frac{s}{\omega_{p2}} + 1\right) \tag{11.74}$$

$$= \frac{s^2}{\omega_{p1}\omega_{p2}} + \left(\frac{1}{\omega_{p1}} + \frac{1}{\omega_{p2}}\right)s + 1. \tag{11.75}$$

Now suppose one pole is much farther from the origin than the other: $\omega_{p2} \gg \omega_{p1}$. (This is called the "dominant pole" approximation to emphasize that ω_{p1} dominates the frequency response). Then, $\omega_{p1}^{-1} + \omega_{p2}^{-1} \approx \omega_{p1}^{-1}$, i.e.,

$$b = \frac{1}{\omega_{p1}}, \tag{11.76}$$

and from Eq. (11.72),

$$|\omega_{p1}| = \frac{1}{(1 + g_mR_L)C_{XY}R_{Thev} + R_{Thev}C_{in} + R_L(C_{XY} + C_{out})}. \tag{11.77}$$

How does this result compare with that obtained using the Miller approximation? Equation (11.77) does reveal the Miller effect of C_{XY} but it also contains the additional term $R_L(C_{XY} + C_{out})$ [which is close to the output time constant predicted by Eq. (11.59)].

[12] As explained in more advanced courses, this zero does become problematic in the internal circuitry of op amps.

To determine the "nondominant" pole, ω_{p2}, we recognize from Eqs. (11.75) and (11.76) that

$$|\omega_{p2}| = \frac{b}{a} \tag{11.78}$$

$$= \frac{(1+g_m R_L)C_{XY}R_{Thev} + R_{Thev}C_{in} + R_L(C_{XY}+C_{out})}{R_{Thev}R_L(C_{in}C_{XY} + C_{out}C_{XY} + C_{in}C_{out})}. \tag{11.79}$$

Example 11.17

Using the dominant-pole approximation, compute the poles of the circuit shown in Fig. 11.31(a). Assume both transistors operate in saturation and $\lambda \neq 0$.

Solution

Noting that C_{SB1}, C_{GS2}, and C_{SB2} do not affect the circuit (why?), we add the remaining capacitances as depicted in Fig. 11.31(b), simplifying the result as illustrated in Fig. 11.31(c), where

$$C_{in} = C_{GS1} \tag{11.80}$$

$$C_{XY} = C_{GD1} \tag{11.81}$$

$$C_{out} = C_{DB1} + C_{GD2} + C_{DB2}. \tag{11.82}$$

It follows from Eqs. (11.77) and (11.79) that

$$\omega_{p1} \approx \frac{1}{[1+g_{m1}(r_{O1}||r_{O2})]C_{XY}R_S + R_S C_{in} + (r_{O1}||r_{O2})(C_{XY}+C_{out})} \tag{11.83}$$

$$\omega_{p2} \approx \frac{[1+g_{m1}(r_{O1}||r_{O2})]C_{XY}R_S + R_S C_{in} + (r_{O1}||r_{O2})(C_{XY}+C_{out})}{R_S(r_{O1}||r_{O2})(C_{in}C_{XY} + C_{out}C_{XY} + C_{in}C_{out})}. \tag{11.84}$$

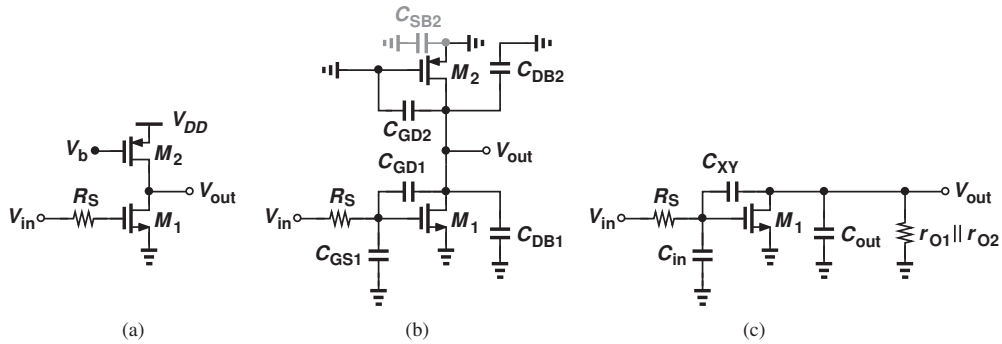


Figure 11.31

Exercise Repeat the above example if $\lambda \neq 0$.

Example 11.18

In the CS stage of Fig. 11.29(a), we have $R_S = 200\,\Omega, C_{GS} = 250$ fF, $C_{GD} = 80$ fF, $C_{DB} = 100$ fF, $g_m = (150\,\Omega)^{-1}$, $\lambda = 0$, and $R_L = 2$ kΩ. Plot the frequency response with the aid of (a) Miller's approximation, (b) the exact transfer function, (c) the dominant-pole approximation.

Solution (a) With $g_m R_L = 13.3$, Eqs. (11.58) and (11.59) yield

$$|\omega_{p,in}| = 2\pi \times (571\ \text{MHz}) \tag{11.85}$$

$$|\omega_{p,out}| = 2\pi \times (428\ \text{MHz}). \tag{11.86}$$

(b) The transfer function in Eq. (11.70) gives a zero at $g_m/C_{GD} = 2\pi \times (13.3\ \text{GHz})$. Also, $a = 2.12 \times 10^{-20}\ \text{s}^{-2}$ and $b = 6.39 \times 10^{-10}$ s. Thus,

$$|\omega_{p1}| = 2\pi \times (264\ \text{MHz}) \tag{11.87}$$

$$|\omega_{p2}| = 2\pi \times (4.53\ \text{GHz}). \tag{11.88}$$

Note the large error in the values predicted by Miller's approximation. This error arises because we have multiplied C_{GD} by the midband gain $(1 + g_m R_L)$ rather than the gain at high frequencies.[13]

(c) The results obtained in part (b) predict that the dominant-pole approximation produces relatively accurate results as the two poles are quite far apart. From Eqs. (11.77) and (11.79), we have

$$|\omega_{p1}| = 2\pi \times (249\ \text{MHz}) \tag{11.89}$$

$$|\omega_{p2}| = 2\pi \times (4.79\ \text{GHz}). \tag{11.90}$$

Figure 11.32 plots the results. The low-frequency gain is equal to 22 dB $\approx$ 13 and the -3 dB bandwidth predicted by the exact equation is around 250 MHz.

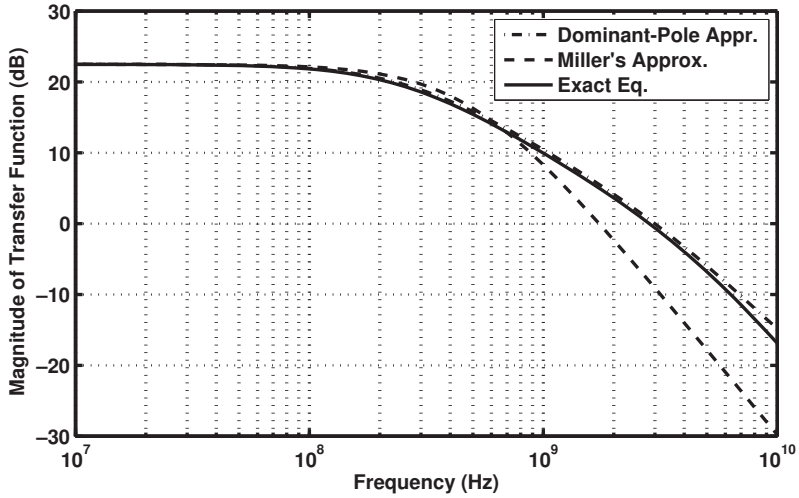


Figure 11.32

Exercise Repeat the above example if the device width (and hence its capacitances) and the bias current are halved.

11.4.5 Input Impedance

The high-frequency input impedances of the CE and CS amplifiers determine the ease with which these circuits can be driven by other stages. Our foregoing analysis of

[13]The large discrepancy between $|\omega_{p,out}|$ and $|\omega_{p2}|$ results from an effect called "pole splitting" and is studied in more advanced courses.

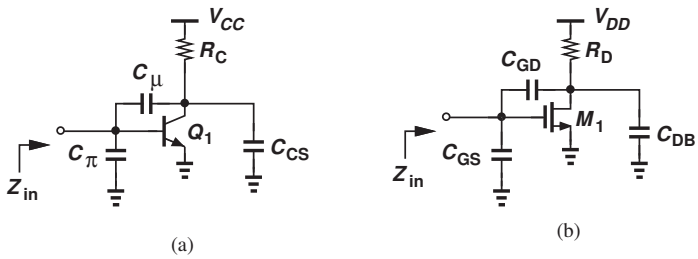


Figure 11.33 Input impedance of (a) CE and (b) CS stages.

the frequency response and particularly the Miller approximation readily yields this impedance.

As illustrated in Fig. 11.33(a), the input impedance of a CE stage consists of two parallel components: $C_\pi + (1 + g_m R_D)C_\mu$ and r_π.[14] That is,

$$Z_{in} \approx \frac{1}{[C_\pi + (1 + g_m R_D)C_\mu]s} || r_\pi . \tag{11.91}$$

Similarly, the MOS counterpart exhibits an input impedance given by

$$Z_{in} \approx \frac{1}{[C_{GS} + (1 + g_m R_D)C_{GD}]s} . \tag{11.92}$$

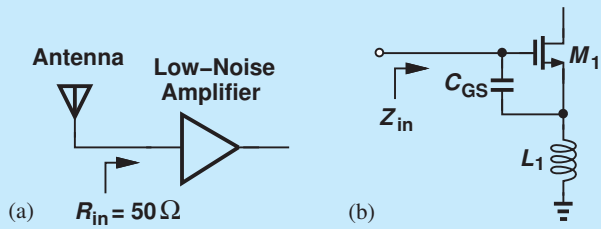
With a high voltage gain, the Miller effect may substantially lower the input impedance at high frequencies.

Did you know?

Most RF receivers incorporate a common-source or common-emitter amplifier at their front end. This "low-noise" amplifier must present an input resistance of 50 Ω so as to "match" the impedance of the antenna [Fig. (a)]. But how could a CS stage have such a low input resistance? A clever technique is to add an inductor in series with the source of the transistor [Fig. (b)]. It can be shown that the input impedance is given by

$$Z_{in}(s) = \frac{1}{C_{GS}s} + L_1 s + \frac{L_1 g_m}{C_{GS}} .$$

Note that the last term is a real quantity, representing a resistance. Proper choice of L_1, g_m, and C_{GS} provides a value of 50 Ω. Next time you turn on your cell phone or your GPS, you may be receiving an RF signal through an inductively-degenerated CS amplifier.



Input impedance matching in a receiver.

[14] In calculation of the input impedance, the output impedance of the preceding stage (denoted by R_S) is excluded.

11.5 FREQUENCY RESPONSE OF CB AND CG STAGES

11.5.1 Low-Frequency Response

As with CE and CS stages, the use of capacitive coupling leads to low-frequency roll-off in CB and CG amplifiers. Consider the CB circuit depicted in Fig. 11.34(a), where I_1 defines the bias current of Q_1 and V_b is chosen to ensure operation in the forward active region (V_b is less than the collector bias voltage). How large should C_i be? Since C_i appears in series with R_S, we replace R_S with $R_S + (C_i s)^{-1}$ in the midband gain expression, $R_C/(R_S + 1/g_m)$, and write the resulting transfer function as

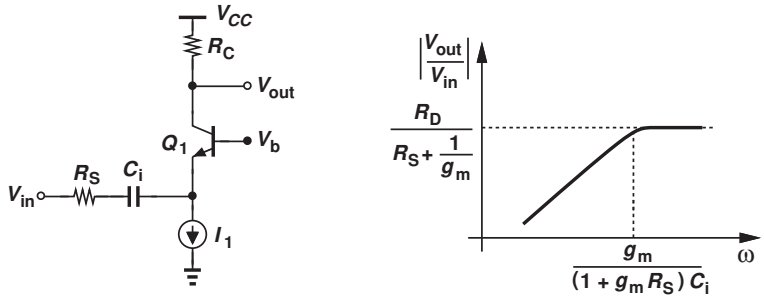
$$\frac{V_{out}}{V_{in}}(s) = \frac{R_C}{R_S + (C_i s)^{-1} + 1/g_m} \tag{11.93}$$

$$= \frac{g_m R_C C_i s}{(1 + g_m R_S) C_i s + g_m}. \tag{11.94}$$

Equation (11.93) implies that the signal does not "feel" the effect of C_i if $|(C_i s)^{-1}| \ll R_S + 1/g_m$. From another perspective, Eq. (11.94) yields the response shown in Fig. 11.34(b), revealing a pole at

$$|\omega_p| = \frac{g_m}{(1 + g_m R_S) C_i} \tag{11.95}$$

and suggesting that this pole must remain quite lower than the minimum signal frequency of interest. These two conditions are equivalent.



(a) (b)

Figure 11.34 (a) CB stage with input capacitor coupling, (b) resulting frequency response.

11.5.2 High-Frequency Response

We know from Chapters 5 and 7 that CB and CG stages exhibit a relatively low input impedance ($\approx 1/g_m$). The high-frequency response of these circuits does not suffer from Miller effect, an important advantage in some cases.

Consider the stages shown in Fig. 11.35, where $r_O = \infty$ and the transistor capacitances are included. Since V_b is at ac ground, we note that (1) C_π and $C_{GS} + C_{SB}$ go to ground; (2) C_{CS} and C_μ of Q_1 appear in parallel to ground, and so do C_{GD} and C_{DB} of M_1; (3) no capacitance appears between the input and output networks, avoiding the Miller effect. In fact, with all of the capacitances seeing ground at one of their terminals, we can readily associate one pole with each node. At node X, the total resistance seen to ground is given

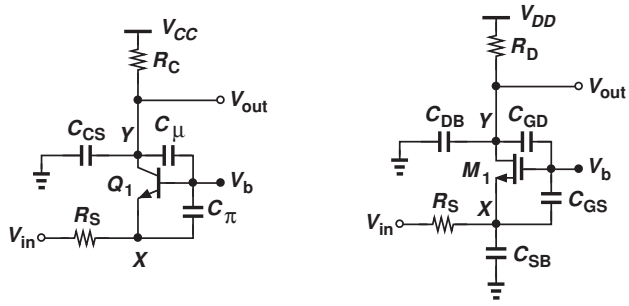


Figure 11.35 (a) CB and (b) CG stages including transistor capacitances.

by $R_S||(1/g_m)$, yielding

$$|\omega_{p,X}| = \frac{1}{\left(R_S||\dfrac{1}{g_m}\right)C_X}, \tag{11.96}$$

where $C_X = C_\pi$ or $C_{GS} + C_{SB}$. Similarly, at Y,

$$|\omega_{p,Y}| = \frac{1}{R_L C_Y}, \tag{11.97}$$

where $C_Y = C_\mu + C_{CS}$ or $C_{GD} + C_{DB}$.

It is interesting to note that the "input" pole magnitude is on the order of the f_T of the transistor: C_X is equal to C_π or roughly equal to C_{GS} while the resistance seen to ground is less than $1/g_m$. For this reason, the input pole of the CB/CG stage rarely creates a speed bottleneck.[15]

Example 11.19

Compute the poles of the circuit shown in Fig. 11.36(a). Assume $\lambda = 0$.

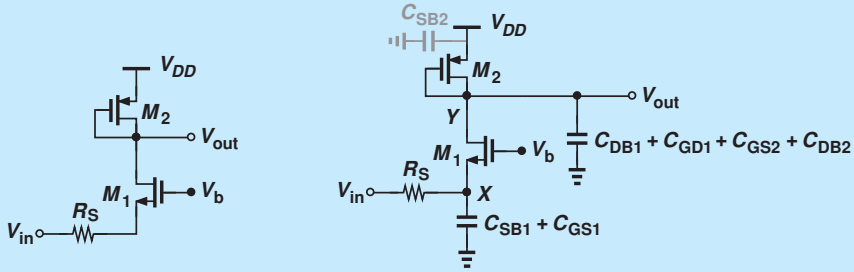


Figure 11.36

Solution

Noting that C_{GD2} and C_{SB2} play no role in the circuit, we add the device capacitances as depicted in Fig. 11.36(b). The input pole is thus given by

$$|\omega_{p,X}| = \frac{1}{\left(R_S\left\|\dfrac{1}{g_{m1}}\right.\right)(C_{SB1} + C_{GD1})}. \tag{11.98}$$

[15] One exception is encountered in radio-frequency circuits (e.g., cellphones), where the input capacitance becomes undesirable.

Since the small-signal resistance at the output node is equal to $1/g_{m2}$, we have

$$|\omega_{p,Y}| = \frac{1}{\frac{1}{g_{m2}}(C_{DB1} + C_{GD1} + C_{GS2} + C_{DB2})}. \tag{11.99}$$

Exercise Repeat the above example if M_2 operates as a current source, i.e., its gate is connected to a constant voltage.

Example 11.20

The CS stage of Example 11.18 is reconfigured to a common-gate amplifier (with R_S tied to the source of the transistor). Plot the frequency response of the circuit.

Solution

With the values given in Example 11.18 and noting that $C_{SB} = C_{DB}$,[16] we obtain from Eqs. (11.96) and (11.97),

$$|\omega_{p,in}| = 2\pi \times (5.31\ \text{GHz}) \tag{11.100}$$

$$|\omega_{p,out}| = 2\pi \times (442\ \text{MHz}). \tag{11.101}$$

With no Miller effect, the input pole has dramatically risen in magnitude. The output pole, however, limits the bandwidth. Also, the low-frequency gain is now equal to $R_D/(R_S + 1/g_m) = 5.7$, more than a factor of two lower than that of the CS stage. Figure 11.37 plots the result. The low-frequency gain is equal to 15 dB ≈ 5.7 and the -3 dB bandwidth is around 450 MHz.

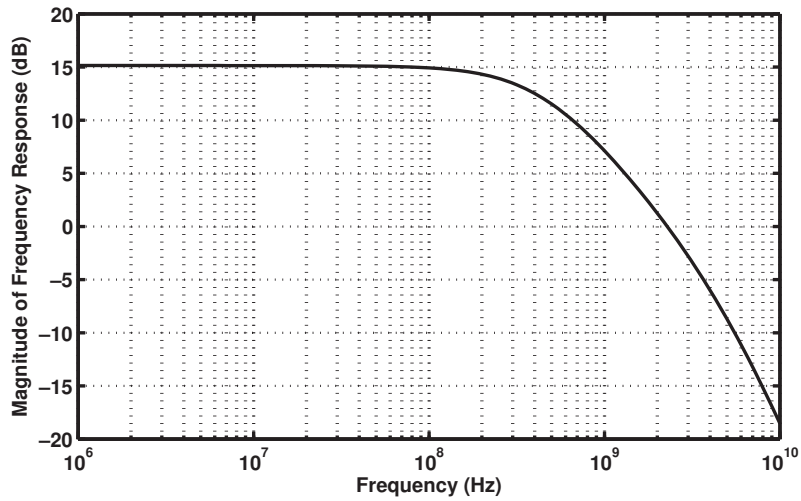


Figure 11.37

Exercise Repeat the above example if the CG amplifier drives a load capacitance of 150 fF.

[16] In reality, the junction capacitances C_{SB} and C_{DB} sustain different reverse bias voltages and are therefore not quite equal.

11.6 FREQUENCY RESPONSE OF FOLLOWERS

The low-frequency response of followers is similar to that studied in Example 11.11 and that of CE/CS stages. We thus study the high-frequency behavior here.

In Chapters 5 and 7, we noted that emitter and source followers provide a high input impedance and a relatively low output impedance while suffering from a sub-unity (positive) voltage gain. Emitter followers, and occasionally source followers, are utilized as buffers and their frequency characteristics are of interest.

Figure 11.38 illustrates the stages with relevant capacitances. The emitter follower is loaded with C_L to create both a more general case and greater similarity between the bipolar and MOS counterparts. We observe that each circuit contains two grounded capacitors and one floating capacitor. While the latter may be decomposed using Miller's approximation, the resulting analysis is beyond the scope of this book. We therefore perform a direct analysis by writing the circuit's equations. Since the bipolar and MOS versions in Fig. 11.38 differ by only r_π, we first analyze the emitter follower and subsequently let r_π (or β) approach infinity to obtain the transfer function of the source follower.

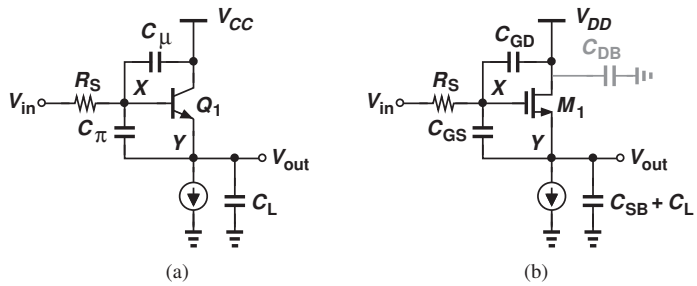


Figure 11.38 (a) Emitter follower and (b) source follower including transistor capacitances.

Consider the small-signal equivalent shown in Fig. 11.39. Recognizing that $V_X = V_{out} + V_\pi$ and the current through the parallel combination of r_π and C_π is given by $V_\pi/r_\pi + V_\pi C_\pi s$, we write a KCL at node X:

$$\frac{V_{out} + V_\pi - V_{in}}{R_S} + (V_{out} + V_\pi)C_\mu s + \frac{V_\pi}{r_\pi} + V_\pi C_\pi s = 0, \tag{11.102}$$

and another at the output node:

$$\frac{V_\pi}{r_\pi} + V_\pi C_\pi s + g_m V_\pi = V_{out} C_L s. \tag{11.103}$$

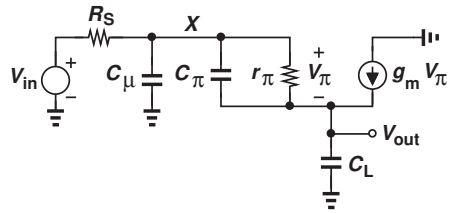


Figure 11.39 Small-signal equivalent of emitter follower.

The latter gives

$$V_\pi = \frac{V_{out} C_L s}{\frac{1}{r_\pi} + g_m + C_\pi s}, \tag{11.104}$$

which, upon substitution in Eq. (11.102) and with the assumption $r_\pi \gg g_m^{-1}$, leads to

$$\frac{V_{out}}{V_{in}} = \frac{1 + \frac{C_\pi}{g_m} s}{as^2 + bs + 1}, \tag{11.105}$$

where

$$a = \frac{R_S}{g_m}(C_\mu C_\pi + C_\mu C_L + C_\pi C_L) \tag{11.106}$$

$$b = R_S C_\mu + \frac{C_\pi}{g_m} + \left(1 + \frac{R_S}{r_\pi}\right)\frac{C_L}{g_m}. \tag{11.107}$$

The circuit thus exhibits a zero at

$$|\omega_z| = \frac{g_m}{C_\pi}, \tag{11.108}$$

which, from Eq. (11.49), is near the f_T of the transistor. The poles of the circuit can be computed using the dominant-pole approximation described in Section 11.4.4. In practice, however, the two poles do not fall far from each other, necessitating direct solution of the quadratic denominator.

The above results also apply to the source follower if $r_\pi \to \infty$ and corresponding capacitance substitutions are made (C_{SB} and C_L are in parallel):

$$\frac{V_{out}}{V_{in}} = \frac{1 + \frac{C_{GS}}{g_m} s}{as^2 + bs + 1}, \tag{11.109}$$

where

$$a = \frac{R_S}{g_m}[C_{GD}C_{GS} + C_{GD}(C_{SB} + C_L) + C_{GS}(C_{SB} + C_L)] \tag{11.110}$$

$$b = R_S C_{GD} + \frac{C_{GD} + C_{SB} + C_L}{g_m}. \tag{11.111}$$

Example 11.21

A source follower is driven by a resistance of 200 Ω and drives a load capacitance of 100 fF. Using the transistor parameters given in Example 11.18, plot the frequency response of the circuit.

Solution

The zero occurs at $g_m/C_{GS} = 2\pi \times (4.24\ \text{GHz})$. To compute the poles, we obtain a and b from Eqs. (11.110) and (11.111), respectively:

$$a = 2.58 \times 10^{-21}\ \text{s}^{-2} \tag{11.112}$$

$$b = 5.8 \times 10^{-11}\ \text{s}. \tag{11.113}$$

The two poles are then equal to

$$\omega_{p1} = 2\pi[-1.79\,\text{GHz} + j(2.57\,\text{GHz})] \tag{11.114}$$

$$\omega_{p2} = 2\pi[-1.79\,\text{GHz} - j(2.57\,\text{GHz})]. \tag{11.115}$$

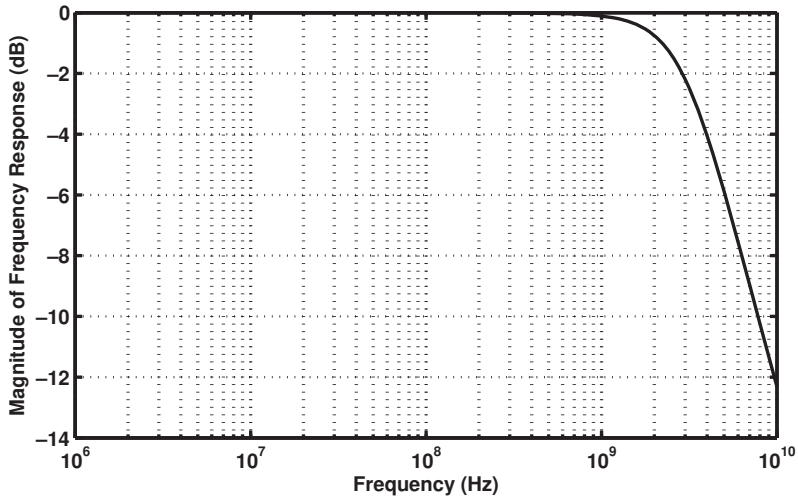


Figure 11.40

With the values chosen here, the poles are complex. Figure 11.40 plots the frequency response. The −3 dB bandwidth is approximately equal to 3.5 GHz.

Exercise For what value of g_m do the two poles become real and equal?

Example 11.22 Determine the transfer function of the source follower shown in Fig. 11.41(a), where M_2 acts as a current source.

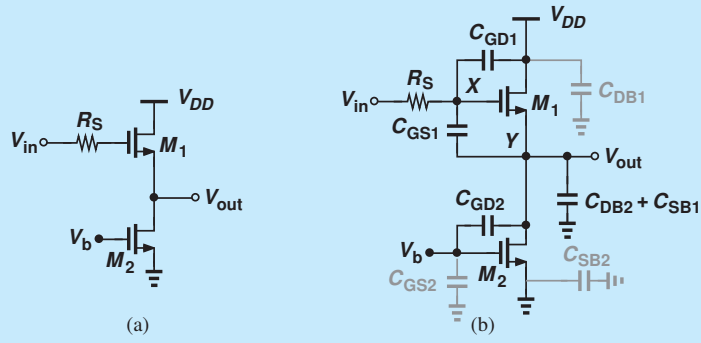


Figure 11.41

Solution Noting that C_{GS2} and C_{SB2} play no role in the circuit, we include the transistor capacitances as illustrated in Fig. 11.41(b). The result resembles that in Fig. 11.38, but with C_{GD2} and

C_{DB2} appearing in parallel with C_{SB1}. Thus, Eq. (11.109) can be rewritten as

$$\frac{V_{out}}{V_{in}}(s) = \frac{1 + \dfrac{C_{GS1}}{g_{m1}}s}{as^2 + bs + 1}, \tag{11.116}$$

where

$$a = \frac{R_S}{g_{m1}}[C_{GD1}C_{GS1} + (C_{GD1} + C_{GS1})(C_{SB1} + C_{GD2} + C_{DB2})] \tag{11.117}$$

$$b = R_S C_{GD1} + \frac{C_{GD1} + C_{SB1} + C_{GD2} + C_{DB2}}{g_{m1}}. \tag{11.118}$$

Exercise Assuming M_1 and M_2 are identical and using the transistor parameters given in Example 11.18, calculate the pole frequencies.

11.6.1 Input and Output Impedances

In Chapter 5, we observed that the input resistance of the emitter follower is given by $r_\pi + (\beta + 1)R_L$, where R_L denotes the load resistance. Also, in Chapter 7, we noted that the source follower input resistance approaches infinity at low frequencies. We now employ an approximate but intuitive analysis to obtain the input capacitance of followers.

Consider the circuits shown in Fig. 11.42, where C_π and C_{GS} appear between the input and output and can therefore be decomposed using Miller's theorem. Since the low-frequency gain is equal to

$$A_v = \frac{R_L}{R_L + \dfrac{1}{g_m}}, \tag{11.119}$$

we note that the "input" component of C_π or C_{GS} is expressed as

$$C_X = (1 - A_v)C_{XY} \tag{11.120}$$

$$= \frac{1}{1 + g_m R_L}C_{XY}. \tag{11.121}$$

Interestingly, the input capacitance of the follower contains only a *fraction* of C_π or C_{GS}, depending on how large $g_m R_L$ is. Of course, C_μ or C_{GD} directly adds to this value to yield the total input capacitance.

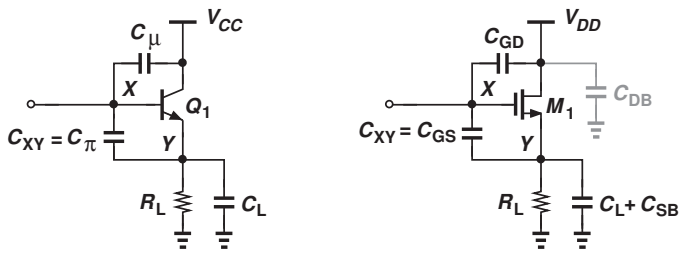


Figure 11.42 Input impedance of (a) emitter follower and (b) source follower.

Example 11.23

Estimate the input capacitance of the follower shown in Fig. 11.43. Assume $\lambda \neq 0$.

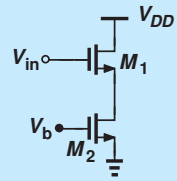


Figure 11.43

Solution

From Chapter 7, the low-frequency gain of the circuit can be written as

$$A_v = \frac{r_{O1}||r_{O2}}{r_{O1}||r_{O2} + \dfrac{1}{g_{m1}}}. \tag{11.122}$$

Also, from Fig. 11.42(b), the capacitance appearing between the input and output is equal to C_{GS1}, thereby providing

$$C_{in} = C_{GD1} + (1 - A_v)C_{GS1} \tag{11.123}$$

$$= C_{GD1} + \frac{1}{1 + g_{m1}(r_{O1}||r_{O2})}C_{GS1}. \tag{11.124}$$

For example, if $g_{m1}(r_{O1}||r_{O2}) \approx 10$, then only 9% of C_{GS1} appears at the input.

Exercise Repeat the above example if $\lambda = 0$.

Let us now turn our attention to the output impedance of followers. Our study of the emitter follower in Chapter 5 revealed that the output resistance is equal to $R_S/(\beta + 1) + 1/g_m$. Similarly, Chapter 7 indicated an output resistance of $1/g_m$ for the source follower. At high frequencies, these circuits display an interesting behavior.

Consider the followers depicted in Fig. 11.44(a), where other capacitances and resistances are neglected for the sake of simplicity. As usual, R_S represents the output resistance of a preceding stage or device. We first compute the output impedance of the emitter follower and subsequently let $r_\pi \to \infty$ to determine that of the source follower. From the

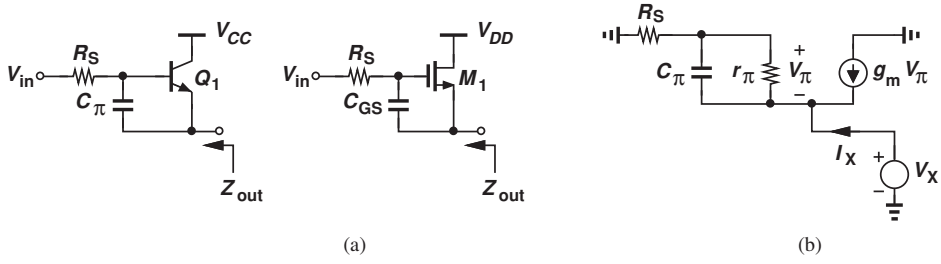


Figure 11.44 (a) Output impedance of emitter and source followers, (b) small-signal model.

equivalent circuit in Fig. 11.44(b), we have

$$(I_X + g_m V_\pi)\left(r_\pi \left\| \frac{1}{C_\pi s}\right.\right) = -V_\pi \tag{11.125}$$

and also

$$(I_X + g_m V_\pi)R_S - V_\pi = V_X. \tag{11.126}$$

Finding V_π from Eq. (11.125)

$$V_\pi = -I_X \frac{r_\pi}{r_\pi C_\pi s + \beta + 1} \tag{11.127}$$

and substituting in Eq. (11.126), we obtain

$$\frac{V_X}{I_X} = \frac{R_S r_\pi C_\pi s + r_\pi + R_S}{r_\pi C_\pi s + \beta + 1}. \tag{11.128}$$

As expected, at low frequencies $V_X/I_X = (r_\pi + R_S)/(\beta + 1) \approx 1/g_m + R_S/(\beta + 1)$. On the other hand, at very high frequencies, $V_X/I_X = R_S$, a meaningful result considering that C_π becomes a short circuit.

The two extreme values calculated above for the output impedance of the emitter follower can be used to develop greater insight. Plotted in Fig. 11.45, the magnitude of this impedance *falls* with ω if $R_S < 1/g_m + R_S/(\beta + 1)$ or *rises* with ω if $R_S > 1/g_m + R_S/(\beta + 1)$. In analogy with the impedance of capacitors and inductors, we say Z_{out} exhibits a capacitive behavior in the former case and an inductive behavior in the latter.

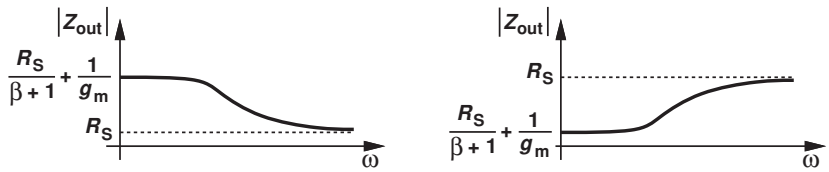


Figure 11.45 Output impedance of emitter follower as a function of frequency for (a) small R_S and (b) large R_S.

Which case is more likely to occur in practice? Since a follower serves to *reduce* the driving impedance, it is reasonable to assume that the follower low-frequency output impedance is *lower* than R_S.[17] Thus, the inductive behavior is more commonly encountered. (It is even possible that the inductive output impedance leads to oscillation if the follower sees a certain amount of load capacitance.)

The above development can be extended to source followers by factoring r_π from the numerator and denominator of Eq. (11.128) and letting r_π and β approach infinity:

$$\frac{V_X}{I_X} = \frac{R_S C_{GS} s + 1}{C_{GS} s + g_m}, \tag{11.129}$$

where $(\beta + 1)/r_\pi$ is replaced with g_m, and C_π with C_{GD}. The plots of Fig. 11.45 are redrawn for the source follower in Fig. 11.46, displaying a similar behavior.

[17] If the follower output resistance is *greater* than R_S, then it is better to omit the follower!

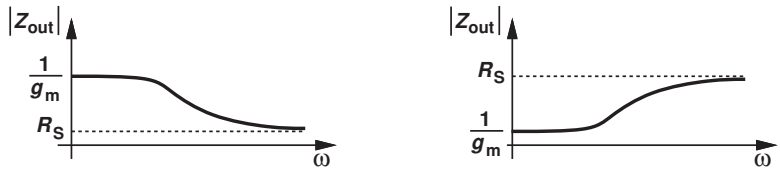


Figure 11.46 Output impedance of source follower as a function of frequency for (a) small R_S and (b) large R_S.

The inductive impedance seen at the output of followers proves useful in the realization of "active inductors."

Example 11.24

Figure 11.47 depicts a two-stage amplifier consisting of a CS circuit and a source follower. Assuming $\lambda \neq 0$ for M_1 and M_2 but $\lambda = 0$ for M_3, and neglecting all capacitances except C_{GS3}, compute the output impedance of the amplifier.

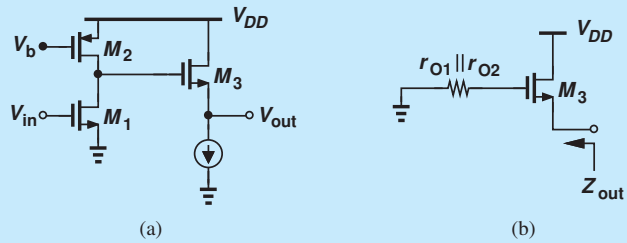


Figure 11.47

Solution

The source impedance seen by the follower is equal to the output resistance of the CS stage, which is equal to $r_{O1}||r_{O2}$. Assuming $R_S = r_{O1}||r_{O2}$ in Eq. (11.129), we have

$$\frac{V_X}{I_X} = \frac{(r_{O1}||r_{O2})C_{GS3}s + 1}{C_{GS3}s + g_{m3}}. \tag{11.130}$$

Exercise Determine Z_{out} in the above example if $\lambda \neq 0$ for M_1-M_3.

11.7 FREQUENCY RESPONSE OF CASCODE STAGE

Our analysis of the CE/CS stage in Section 11.4 and the CB/CG stage in Section 11.5 reveals that the former provides a relatively high input resistance but suffers from Miller effect whereas the latter exhibits a relatively low input resistance but is free from Miller effect. We wish to combine the desirable properties of the two topologies, obtaining a circuit with a relatively high input resistance and no or little Miller effect. Indeed, this thought process led to the invention of the cascode topology in the 1940s.

Consider the cascodes shown in Fig. 11.48. As mentioned in Chapter 9, this structure can be viewed as a CE/CS transistor, Q_1 or M_1, followed by a CB/CG device, Q_2 or M_2. As

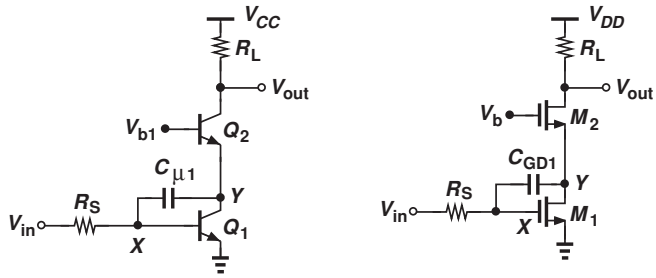
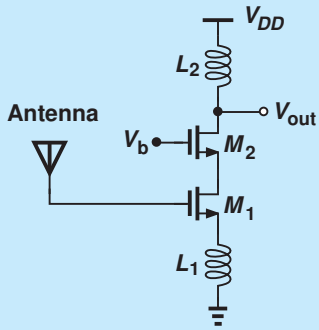


Figure 11.48 (a) Bipolar and (b) MOS cascode stages.

Did you know?

In addition to reducing Miller multiplication of C_μ or C_{GD}, the cascode structure provides a higher output impedance, a higher voltage gain, and greater stability. By stability, we mean the tendency of the amplifier not to oscillate. Since C_μ or C_{GD} returns a fraction of the output signal to the input, it can cause instability in high-frequency amplifiers. For this reason, we commonly use the cascode topology at the front end of RF receivers, often with inductive degeneration as shown below.



Use of cascode in a cellphone low-noise amplifier.

such, the circuit still exhibits a relatively high (for Q_1) or infinite (for M_1) input resistance while providing a voltage gain equal to $g_{m1}R_L$.[18] But, how about the Miller multiplication of $C_{\mu 1}$ or C_{GD1}? We must first compute the voltage gain from node X to node Y. Assuming $r_O = \infty$ for all transistors, we recognize that the impedance seen at Y is equal to $1/g_{m2}$, yielding a small-signal gain of

$$A_{v,XY} = \frac{v_Y}{v_X} \tag{11.131}$$

$$= -\frac{g_{m1}}{g_{m2}}. \tag{11.132}$$

In the bipolar cascode, $g_{m1} = g_{m2}$ (why?), resulting in a gain of -1. In the MOS counterpart, M_1 and M_2 need not be identical, but g_{m1} and g_{m2} are comparable because of their relatively weak dependence upon W/L. We therefore say the gain from X to Y remains near -1 in most practical cases, concluding that the Miller effect of $C_{XY} = C_{\mu 1}$ or C_{GD1} is given by

$$C_X = (1 - A_{v,XY})C_{XY} \tag{11.133}$$

$$\approx 2C_{XY}. \tag{11.134}$$

This result stands in contrast to that expressed by Eq. (11.56), suggesting that the cascode transistor breaks the trade-off between the gain and the input capacitance due to Miller effect.

Let us continue our analysis and estimate the poles of the cascode topology with the aid of Miller's approximation. Illustrated in Fig. 11.49 is the bipolar cascode along with the transistor capacitances. Note that the effect of $C_{\mu 1}$ at Y is also equal to $(1 - A_{v,XY}^{-1})C_{\mu 1} = 2C_{\mu 1}$.

[18] The voltage division between R_S and $r_{\pi 1}$ lowers the gain slightly in the bipolar circuit.

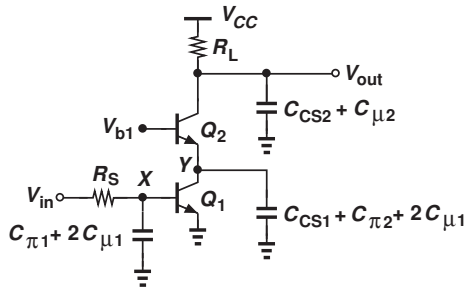


Figure 11.49 Bipolar cascode including transistor capacitances.

Associating one pole with each node gives

$$|\omega_{p,X}| = \frac{1}{(R_S||r_{\pi 1})(C_{\pi 1} + 2C_{\mu 1})} \tag{11.135}$$

$$|\omega_{p,Y}| = \frac{1}{\dfrac{1}{g_{m2}}(C_{CS1} + C_{\pi 2} + 2C_{\mu 1})} \tag{11.136}$$

$$|\omega_{p,out}| = \frac{1}{R_L(C_{CS2} + C_{\mu 2})}. \tag{11.137}$$

It is interesting to note that the pole at node Y falls near the f_T of Q_2 if $C_{\pi 2} \gg C_{CS1} + 2C_{\mu 1}$. Even for comparable values of $C_{\pi 2}$ and $C_{CS1} + 2C_{\mu 1}$, we can say this pole is on the order of $f_T/2$, a frequency typically much higher than the signal bandwidth. For this reason, the pole at node Y often has negligible effect on the frequency response of the cascode stage.

The MOS cascode is shown in Fig. 11.50 along with its capacitances after the use of Miller's approximation. Since the gain from X to Y in this case may not be equal to -1, we use the actual value, $-g_{m1}/g_{m2}$, to arrive at a more general solution. Associating one pole with each node, we have

$$|\omega_{p,X}| = \frac{1}{R_S\left[C_{GS1} + \left(1 + \dfrac{g_{m1}}{g_{m2}}\right)C_{GD1}\right]} \tag{11.138}$$

$$|\omega_{p,Y}| = \frac{1}{\dfrac{1}{g_{m2}}\left[C_{DB1} + C_{GS2} + \left(1 + \dfrac{g_{m2}}{g_{m1}}\right)C_{GD1} + C_{SB2}\right]} \tag{11.139}$$

$$|\omega_{p,out}| = \frac{1}{R_L(C_{DB2} + C_{GD2})}. \tag{11.140}$$

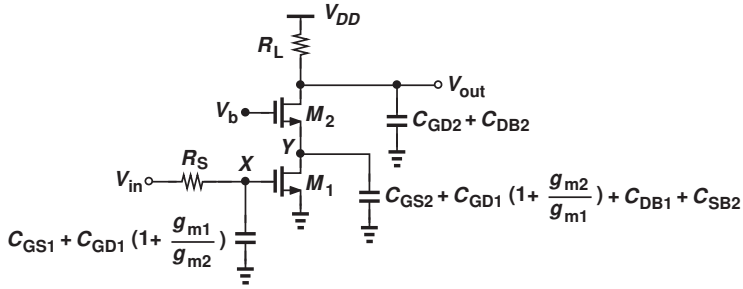


Figure 11.50 MOS cascode including transistor capacitances.

We note that $\omega_{p,Y}$ is still in the range of $f_T/2$ if C_{GS2} and $C_{DB1} + (1 + g_{m2}/g_{m1})C_{GD1}$ are comparable.

Example 11.25

The CS stage studied in Example 11.18 is converted to a cascode topology. Assuming the two transistors are identical, estimate the poles, plot the frequency response, and compare the results with those of Example 11.18. Assume $C_{DB} = C_{SB}$.

Solution

Using the values given in Example 11.18, we write from Eqs. (11.138), (11.139), and (11.140):

$$|\omega_{p,X}| = 2\pi \times (1.95\ \text{GHz}) \tag{11.141}$$

$$|\omega_{p,Y}| = 2\pi \times (1.73\ \text{GHz}) \tag{11.142}$$

$$|\omega_{p,out}| = 2\pi \times (442\ \text{MHz}). \tag{11.143}$$

Note that the pole at node Y is significantly lower than $f_T/2$ in this particular example. Compared with the Miller approximation results obtained in Example 11.18, the input pole has risen considerably. Compared with the exact values derived in that example, the cascode bandwidth (442 MHz) is nearly twice as large. Figure 11.51 plots the frequency response of the cascode stage.

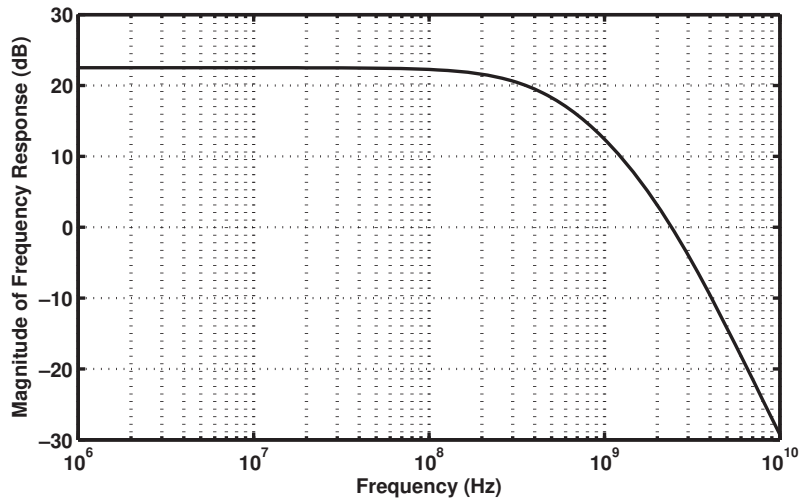


Figure 11.51

Exercise

Repeat the above example if the width of M_2 and hence all of its capacitances are doubled. Assume $g_{m2} = (100\ \Omega)^{-1}$.

Example 11.26

In the cascode shown in Fig. 11.52, transistor M_3 serves as a constant current source, allowing M_1 to carry a larger current than M_2. Estimate the poles of the circuit, assuming $\lambda = 0$.

Solution Transistor M_3 contributes C_{GD3} and C_{DB3} to node Y, thus lowering the corresponding pole magnitude. The circuit contains the following poles:

$$|\omega_{p,X}| = \frac{1}{R_S\left[C_{GS1} + \left(1 + \frac{g_{m1}}{g_{m2}}\right)C_{GD1}\right]} \tag{11.144}$$

$$|\omega_{p,Y}| = \frac{1}{\frac{1}{g_{m2}}\left[C_{DB1} + C_{GS2} + \left(1 + \frac{g_{m2}}{g_{m1}}\right)C_{GD1} + C_{GD3} + C_{DB3} + C_{SB2}\right]} \tag{11.145}$$

$$|\omega_{p,out}| = \frac{1}{R_L(C_{DB2} + C_{GD2})}. \tag{11.146}$$

Note that $\omega_{p,X}$ also reduces in magnitude because the addition of M_3 lowers I_{D2} and hence g_{m2}.

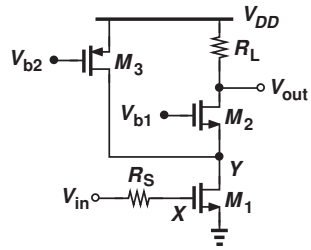


Figure 11.52

Exercise Calculate the pole frequencies in the above example using the transistor parameters given in Example 11.18 for M_1-M_3.

From our studies of the cascode topology in Chapter 9 and in this chapter, we identify two important, distinct attributes of this circuit: (1) the ability to provide a high output impedance and hence serve as a good current source and/or high-gain amplifier; (2) the reduction of the Miller effect and hence better high-frequency performance. Both of these properties are exploited extensively.

11.7.1 Input and Output Impedances

The foregoing analysis of the cascode stage readily provides estimates for the I/O impedances. From Fig. 11.49, the input impedance of the bipolar cascode is given by

$$Z_{in} = r_{\pi 1} \left\| \frac{1}{(C_{\pi 1} + 2C_{\mu 1})s}, \right. \tag{11.147}$$

where Z_{in} does not include R_S. The output impedance is equal to

$$Z_{out} = R_L \left\| \frac{1}{(C_{\mu 2} + C_{CS2})s}, \right. \tag{11.148}$$

where the Early effect is neglected. Similarly, for the MOS stage shown in Fig. 11.50, we have

$$Z_{in} = \frac{1}{\left[C_{GS1} + \left(1 + \frac{g_{m1}}{g_{m2}}\right)C_{GD1}\right]s} \tag{11.149}$$

$$Z_{out} = \frac{1}{R_L(C_{GD2} + C_{DB2})}, \tag{11.150}$$

where it is assumed $\lambda = 0$.

If R_L is large, the output resistance of the transistors must be taken into account. This calculation is beyond the scope of this book.

11.8 FREQUENCY RESPONSE OF DIFFERENTIAL PAIRS

The half-circuit concept introduced in Chapter 10 can also be applied to the high-frequency model of differential pairs, thus reducing the circuit to those studied above.

Figure 11.53(a) depicts two bipolar and MOS differential pairs along with their capacitances. For small differential inputs, the half circuits can be constructed as shown in

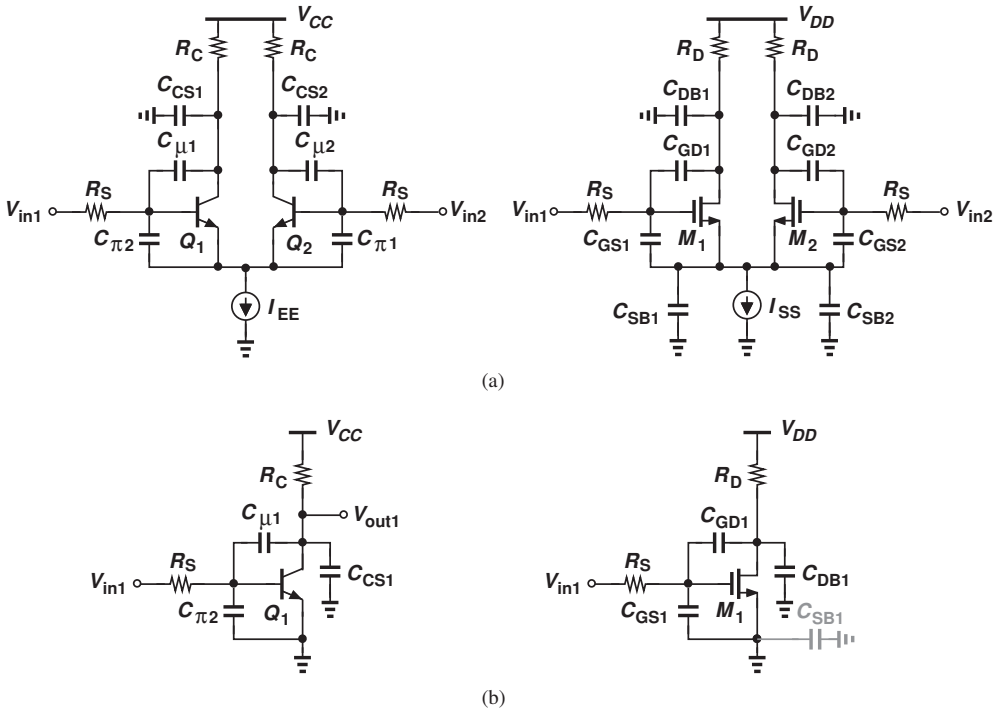


Figure 11.53 (a) Bipolar and MOS differential pairs including transistor capacitances, (b) half circuits.

Fig. 11.53(b). The transfer function is therefore given by Eq. (11.70):

$$\frac{V_{out}}{V_{Thev}}(s) = \frac{(C_{XY}s - g_m)R_L}{as^2 + bs + 1}, \tag{11.151}$$

where the same notation is used for various parameters. Similarly, the input and output impedances (from each node to ground) are equal to those in Eqs. (11.91) and (11.92), respectively.

Example 11.27

A differential pair employs cascode devices to lower the Miller effect [Fig. 11.54(a)]. Estimate the poles of the circuit.

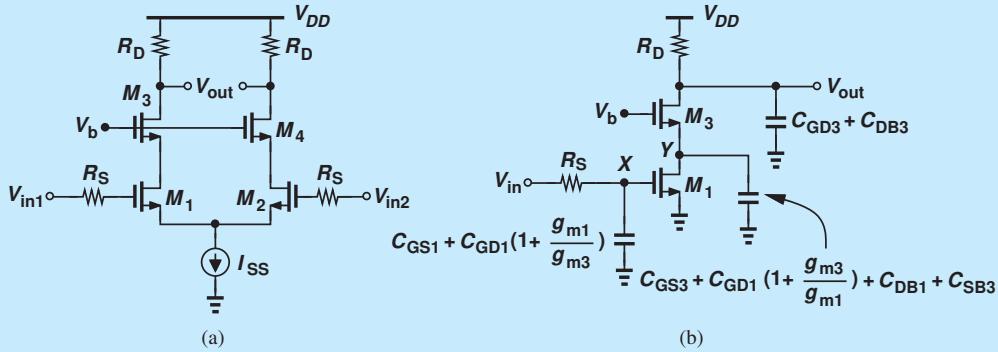


Figure 11.54

Solution

Employing the half circuit shown in Fig. 11.54(b), we utilize the results obtained in Section 11.7:

$$|\omega_{p,X}| = \frac{1}{R_S\left[C_{GS1} + \left(1 + \frac{g_{m1}}{g_{m3}}\right)C_{GD1}\right]} \tag{11.152}$$

$$|\omega_{p,Y}| = \frac{1}{\frac{1}{g_{m3}}\left[C_{DB1} + C_{GS3} + \left(1 + \frac{g_{m3}}{g_{m1}}\right)C_{GD1} + C_{SB3}\right]} \tag{11.153}$$

$$|\omega_{p,out}| = \frac{1}{R_L(C_{DB3} + C_{GD3})}. \tag{11.154}$$

Exercise

Calculate the pole frequencies using the transistor parameters given in Example 11.18. Assume the width and hence the capacitances of M_3 are twice those of M_1. Also, $g_{m3} = \sqrt{2}g_{m1}$.

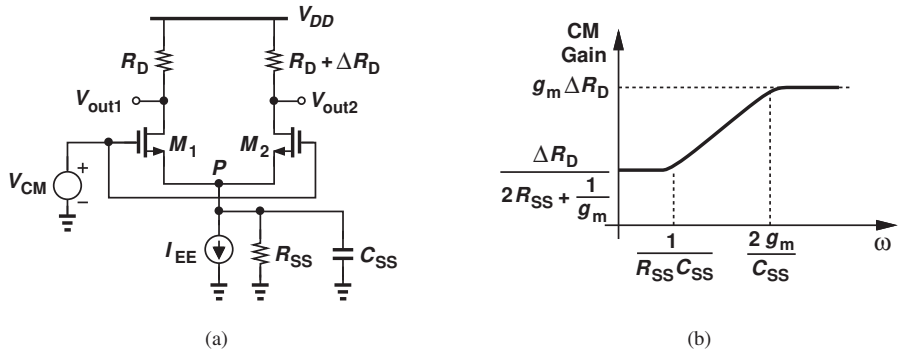


Figure 11.55 (a) Differential pair with parasitic capacitance at the tail node, (b) CM frequency response.

11.8.1 Common-Mode Frequency Response*

The CM response studied in Chapter 10 included no transistor capacitances. At high frequencies, capacitances may *raise* the CM gain (and lower the differential gain), thus degrading the common-mode rejection ratio.

Let us consider the MOS differential pair shown in Fig. 11.55(a), where a finite capacitance appears between node P and ground. Since C_{SS} shunts R_{SS}, we expect the total impedance between P and ground to fall at high frequencies, leading to a higher CM gain. In fact, we can simply replace R_{SS} with $R_{SS}||[1/(C_{SS}s)]$ in Eq. (10.186):

$$\left|\frac{\Delta V_{out}}{\Delta V_{CM}}\right| = \frac{\Delta R_D}{\dfrac{1}{g_m} + 2\left(R_{SS}\left\|\dfrac{1}{C_{SS}s}\right.\right)} \tag{11.155}$$

$$= \frac{g_m \Delta R_D (R_{SS}C_{SS} + 1)}{R_{SS}C_{SS}s + 2g_m R_{SS} + 1}. \tag{11.156}$$

Since R_{SS} is typically quite large, $2g_m R_{SS} \gg 1$, yielding the following zero and pole frequencies:

$$|\omega_z| = \frac{1}{R_{SS}C_{SS}} \tag{11.157}$$

$$|\omega_p| = \frac{2g_m}{C_{SS}}, \tag{11.158}$$

and the Bode approximation plotted in Fig. 11.55(b). The CM gain indeed rises dramatically at high frequencies—by a factor of $2g_m R_{SS}$ (why?).

Figure 11.56 depicts the transistor capacitances that constitute C_{SS}. For example, M_3 is typically a wide device so that it can operate with a small V_{DS}, thereby adding large capacitances to node P.

*This section can be skipped in a first reading.

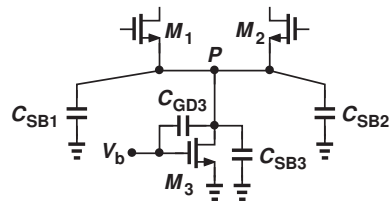


Figure 11.56 Transistor capacitance contributions to the tail node.

11.9 ADDITIONAL EXAMPLES

Example 11.28

The amplifier shown in Fig. 11.57(a) incorporates capacitive coupling both at the input and between the two stages. Determine the low-frequency cut-off of the circuit. Assume $I_S = 5 \times 10^{-16}$ A, $\beta = 100$, and $V_A = \infty$.

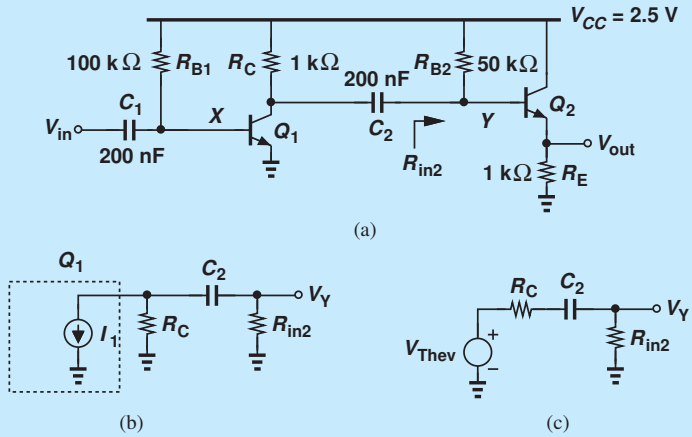


Figure 11.57

Solution

We must first compute the operating point and small-signal parameters of the circuit. From Chapter 5, we begin with an estimate of for V_{BE1}, e.g., 800 mV, and express the base current of Q_1 as $(V_{CC} - V_{BE1})/R_{B1}$ and hence

$$I_{C1} = \beta \frac{V_{CC} - V_{BE1}}{R_{B1}} \tag{11.159}$$

$$= 1.7\,\text{mA}. \tag{11.160}$$

It follows that $V_{BE1} = V_T \ln(I_{C1}/I_{S1}) = 748$ mV and $I_{C1} = 1.75$ mA. Thus, $g_{m1} = (14.9\,\Omega)^{-1}$ and $r_{\pi 1} = 1.49$ kΩ. For Q_2, we have

$$V_{CC} = I_{B2}R_{B2} + V_{BE2} + R_E I_{C2}, \tag{11.161}$$

and therefore

$$I_{C2} = \frac{V_{CC} - V_{BE2}}{R_{B2}/\beta + R_E} \tag{11.162}$$

$$= 1.13\,\text{mA}, \tag{11.163}$$

where it is assumed $V_{BE2} \approx 800$ mV. Iteration yields $I_{C2} = 1.17$ mA. Thus, $g_{m2} = (22.2\,\Omega)^{-1}$ and $r_{\pi 2} = 2.22$ kΩ.

Let us now consider the first stage by itself. Capacitor C_1 forms a high-pass filter along with the input resistance of the circuit, R_{in1}, thus attenuating low frequencies. Since $R_{in1} = r_{\pi 2}||R_{B1}$, the low-frequency cut-off of this stage is equal to

$$\omega_{L1} = \frac{1}{(r_{\pi 1}||R_{B1})C_1} \tag{11.164}$$

$$= 2\pi \times (542\ \text{Hz}). \tag{11.165}$$

The second coupling capacitor also creates a high-pass response along with the input resistance of the second stage, $R_{in2} = R_{B2}||[r_{\pi 2} + (\beta + 1)R_E]$. To compute the cut-off frequency, we construct the simplified interface shown in Fig. 11.57(b) and determine V_Y/I_1. In this case, it is simpler to replace I_1 and R_C with a Thevenin equivalent, Fig. 11.57(c), where $V_{Thev} = -I_1 R_C$. We now have

$$\frac{V_Y}{V_{Thev}}(s) = \frac{R_{in2}}{R_C + \dfrac{1}{C_2 s} + R_{in2}}, \tag{11.166}$$

obtaining a pole at

$$\omega_{L2} = \frac{1}{(R_C + R_{in2})C_2} \tag{11.167}$$

$$= \pi \times (22.9\ \text{Hz}). \tag{11.168}$$

Since $\omega_{L2} \ll \omega_{L1}$, we conclude that ω_{L1} "dominates" the low-frequency response, i.e., the gain drops by 3 dB at ω_{L1}.

Exercise Repeat the above example if $R_E = 500\ \Omega$.

Example 11.29

The circuit of Fig. 11.58(a) is an example of amplifiers realized in integrated circuits. It consists of a degenerated stage and a self-biased stage, with moderate values for

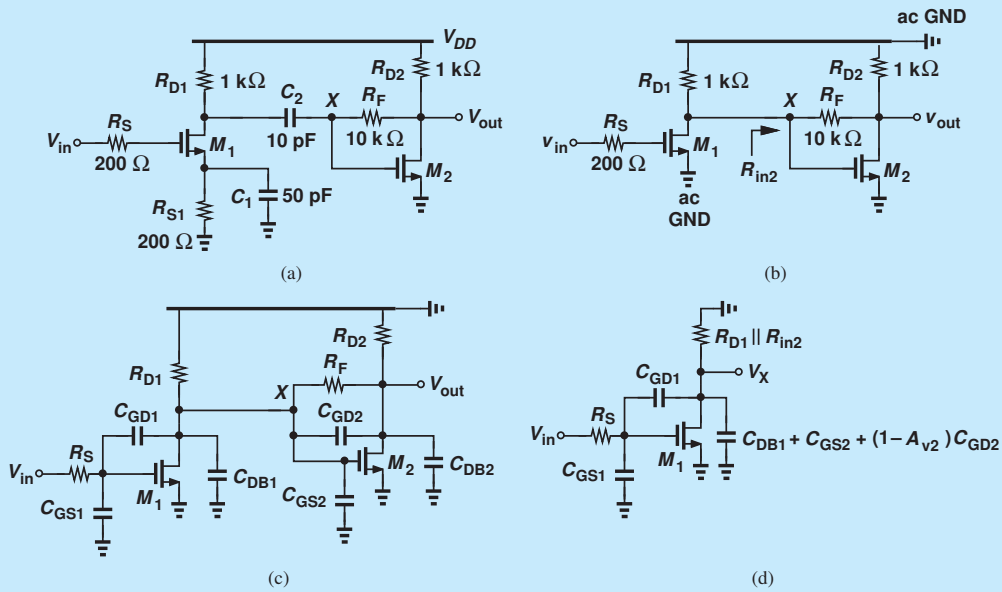


Figure 11.58

C_1 and C_2. Assuming M_1 and M_2 are identical and have the same parameters as those given in Example 11.18, plot the frequency response of the amplifier.

Solution

Low-Frequency Behavior We begin with the low-frequency region and first consider the role of C_1. From Eq. (11.55) and Fig. 11.28(c), we note that C_1 contributes a low-frequency cut-off at

$$\omega_{L1} = \frac{g_{m1}R_{S1} + 1}{R_{S1}C_1} \tag{11.169}$$

$$= 2\pi \times (37.1\,\text{MHz}). \tag{11.170}$$

A second low-frequency cut-off is contributed by C_2 and the input resistance of the second stage, R_{in2}. This resistance can be calculated with the aid of Miller's theorem:

$$R_{in2} = \frac{R_F}{1 - A_{v2}}, \tag{11.171}$$

where A_{v2} denotes the voltage gain from X to the output. Since $R_F \gg R_{D2}$, we have $A_{v2} \approx -g_{m2}R_{D2} = -6.67$,[19] obtaining $R_{in2} = 1.30\,\text{k}\Omega$. Using an analysis similar to that in the previous example, the reader can show that

$$\omega_{L2} = \frac{1}{(R_{D1} + R_{in2})C_2} \tag{11.172}$$

$$= 2\pi \times (6.92\,\text{MHz}). \tag{11.173}$$

Since ω_{L1} remains well above ω_{L2}, the cut-off is dominated by the former.

Midband Behavior In the next step, we compute the midband gain. At midband frequencies, C_1 and C_2 act as a short circuit and the transistor capacitances play a negligible role, allowing the circuit to be reduced to that in Fig. 11.58(b). We note that $v_{out}/v_{in} = (v_X/v_{in})(v_{out}/v_X)$ and recognize that the drain of M_1 sees two resistances to ac ground: R_{D1} and R_{in2}. That is,

$$\frac{v_X}{v_{in}} = -g_{m1}(R_{D1}||R_{in2}) \tag{11.174}$$

$$= -3.77. \tag{11.175}$$

The voltage gain from node X to the output is approximately equal to $-g_{m2}R_{D2}$ because $R_F \gg R_{D2}$.[20] The overall midband gain is therefore roughly equal to 25.1.

High-Frequency Behavior To study the response of the amplifier at high frequencies, we insert the transistor capacitances, noting that C_{SB1} and C_{SB2} play no role because the source terminals of M_1 and M_2 are at ac ground. We thus arrive at the simplified topology shown in Fig. 11.58(c), where the overall transfer function is given by $V_{out}/V_{in} = (V_X/V_{in})(V_{out}/V_X)$.

[19] With this estimate of the gain, we can express the Miller effect of R_F at the output as $R_F/(1 - A_{v2}^{-1}) \approx 8.7\,\text{k}\Omega$, place this resistance in parallel with R_{L2}, and write $A_{v2} = -g_{m2}(R_{D2}||8.7\,\text{k}\Omega) = -5.98$. But we continue without this iteration for simplicity.

[20] If not, then the circuit must be solved using a complete small-signal equivalent.

How do we compute V_X/V_{in} in the presence of the loading of the second stage? The two capacitances C_{DB1} and C_{GS2} are in parallel, but how about the effect of R_F and C_{GD2}? We apply Miller's approximation to both components so as to convert them to grounded elements. The Miller effect of R_F was calculated above to be equivalent to $R_{in2} = 1.3\,\text{k}\Omega$. The Miller multiplication of C_{GD2} is given by $(1 - A_{v2})C_{GD2} = 614$ fF. The first stage can now be drawn as illustrated in Fig. 11.58(d), lending itself to the CS analysis performed in Section 11.4. The zero is given by $g_{m1}/C_{GD1} = 2\pi \times (13.3\,\text{GHz})$. The two poles can be calculated from Eqs. (11.70), (11.71), and (11.72):

$$|\omega_{p1}| = 2\pi \times (242\,\text{MHz}) \tag{11.176}$$

$$|\omega_{p2}| = 2\pi \times (2.74\,\text{GHz}). \tag{11.177}$$

The second stage contributes a pole at its output node. The Miller effect of C_{GD2} at the output is expressed as $(1 - A_{v2}^{-1})C_{GD2} \approx 1.15C_{GD2} = 92$ fF. Adding C_{DB2} to this value yields the output pole as

$$|\omega_{p3}| = \frac{1}{R_{L2}(1.15C_{GD2} + C_{DB2})} \tag{11.178}$$

$$= 2\pi \times (0.829\,\text{GHz}). \tag{11.179}$$

We observe that ω_{p1} dominates the high-frequency response. Figure 11.59 plots the overall response. The midband gain is about 26 dB ≈ 20, around 20% lower than the calculated result. This is primarily due to the use of Miller approximation for R_F. Also, the "useful" bandwidth can be defined from the lower -3 dB cut-off (≈ 40 MHz) to the upper -3 dB cut-off (≈ 300 MHz) and is almost one decade wide. The gain falls to unity at about 2.3 GHz.

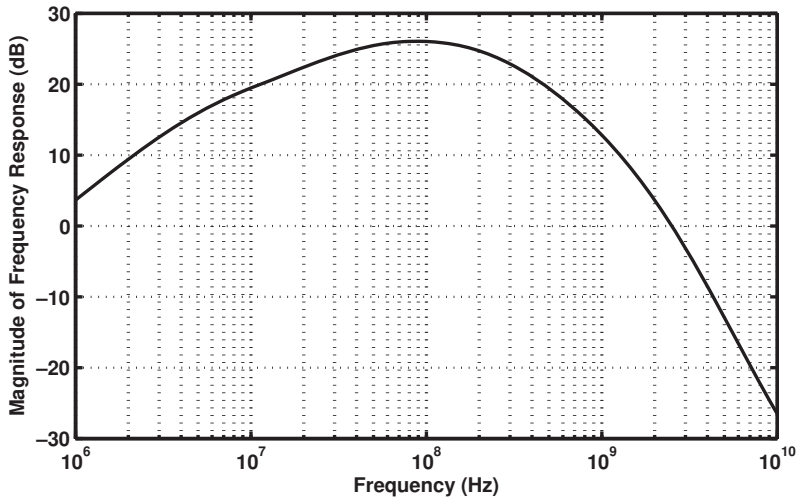


Figure 11.59

11.10 CHAPTER SUMMARY

- The speed of circuits is limited by various capacitances that the transistors and other components contribute to each node.
- The speed can be studied in the time domain (e.g., by applying a step) or in the frequency domain (e.g., by applying a sinusoid). The frequency response of a circuit corresponds to the latter test.
- As the frequency of operation increases, capacitances exhibit a lower impedance, reducing the gain. The gain thus rolls off at high signal frequencies.
- To obtain the frequency response, we must derive the transfer function of the circuit. The magnitude of the transfer function indicates how the gain varies with frequency.
- Bode's rules approximate the frequency response if the poles and zeros are known.
- A capacitance tied between the input and output of an inverting amplifier appears at the input with a factor equal to one minus the gain of the amplifier. This is called the Miller effect.
- In many circuits, it is possible to associate a pole with each node, i.e., calculate the pole frequency as the inverse of the product of the capacitance and resistance seen between the node and ac ground.
- Miller's theorem allows a floating impedance to be decomposed into to grounded impedances.
- Owing to coupling or degeneration capacitors, the frequency response may also exhibit roll-off as the frequency falls to very low values.
- Bipolar and MOS transistors contain capacitances between their terminals and from some terminals to ac ground. When solving a circuit, these capacitances must be identified and the resulting circuit simplified.
- The CE and CS stages exhibit a second-order transfer function and hence two poles. Miller's approximation indicates an input pole that embodies Miller multiplication of the base-collector or gate-drain capacitance.
- If the two poles of a circuit are far from each other, the "dominant-pole approximation" can be used to find a simple expression for each pole frequency.
- The CB and CG stages do not suffer from the Miller effect and achieve a higher speed than CE/CS stages, but their lower input impedance limits their applicability.
- Emitter and source followers provide a wide bandwidth. Their output impedance, however, can be inductive, causing instability in some cases.
- To benefit from the higher input impedance of CE/CS stages but reduce the Miller effect, a cascode stage can be used.
- The differential frequency response of differential pairs is similar to that of CE/CS stages.

PROBLEMS

Sec. 11.1.2 Transfer Function and Frequency Response

11.1. In the circuit of Fig. 11.60, we wish to achieve a -3-dB bandwidth of 1 GHz with a load capacitance of 2 pF. What is the maximum (low-frequency) gain that can be achieved with a power dissipation of 2 mW? Assume $V_{CC} = 2.5$ V and neglect the Early effect and other capacitances.

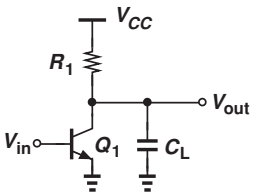


Figure 11.60

11.2. In the amplifier of Fig. 11.61, $R_D = 1$ kΩ and $C_L = 1$ pF. Neglecting channel-length modulation and other capacitances, determine the frequency at which the gain falls by 10% (≈1 dB).

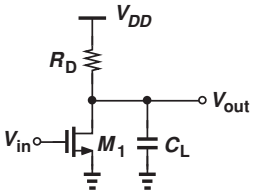


Figure 11.61

11.3. Determine the -3 dB bandwidth of the circuits shown in Fig. 11.62. Assume $V_A = \infty$ but $\lambda > 0$. Neglect other capacitances.

Sec. 11.1.3 Bode's Rules

11.4. Construct the Bode plot of $|V_{out}/V_{in}|$ for the stages depicted in Fig. 11.62.

11.5. A circuit contains two coincident (i.e., equal) poles at ω_{p1}. Construct the Bode plot of $|V_{out}/V_{in}|$.

11.6. An amplifier exhibits two poles at 100 MHz and 10 GHz and a zero at 1 GHz. Construct the Bode plot of $|V_{out}/V_{in}|$.

11.7. An ideal integrator contains a pole at the origin, i.e., $\omega_p = 0$. Construct the Bode plot of $|V_{out}/V_{in}|$. What is the gain of the circuit at arbitrarily *low* frequencies?

11.8. An ideal differentiator provides a zero at the origin, i.e., $\omega_z = 0$. Construct the Bode plot of $|V_{out}/V_{in}|$. What is the gain of the circuit at arbitrarily *high* frequencies?

11.9. Figure 11.63 illustrates a cascade of two identical CS stages. Neglecting channel-length modulation and other capacitances, construct the Bode plot of $|V_{out}/V_{in}|$. Note that $V_{out}/V_{in} = (V_X/V_{in})(V_{out}/V_X)$.

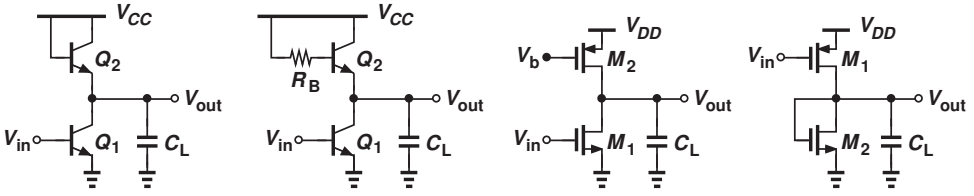


Figure 11.62

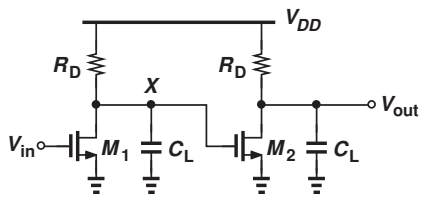


Figure 11.63

*11.10. In Problem 11.9, derive the transfer function of the circuit, substitute $s = j\omega$, and obtain an expression for $|V_{out}/V_{in}|$. Determine the -3 dB bandwidth of the circuit.

*11.11. Due to a manufacturing error, a parasitic resistance R_p has appeared in series with the source of M_1 in Fig. 11.64. Assuming $\lambda = 0$ and neglecting other capacitances, determine the input and output poles of the circuit.

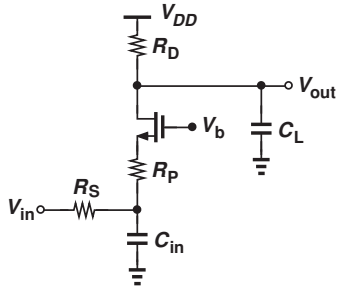


Figure 11.64

*11.12. Consider the circuit shown in Fig. 11.65. Derive the transfer function assuming $\lambda > 0$ but neglecting other capacitances. Explain why the circuit operates as an ideal integrator if $\lambda \to 0$.

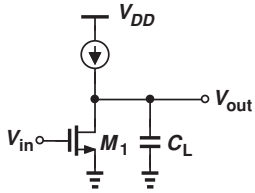


Figure 11.65

11.13. Repeat Problem 11.12 for the circuit shown in Fig. 11.66.

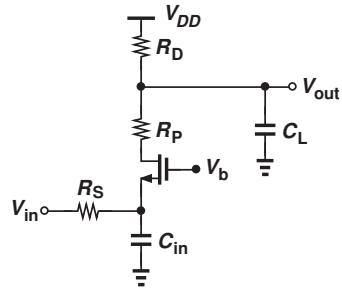


Figure 11.66

11.14. Repeat Problem 11.12 for the CS stage depicted in Fig. 11.67.

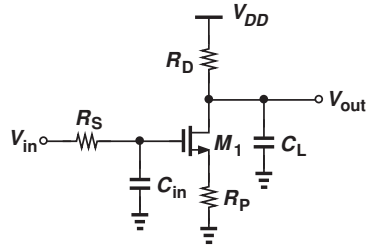


Figure 11.67

*11.15. Derive a relationship for the figure of merit defined by Eq. (11.8) for a CS stage. Consider only the load capacitance.

Sec. 11.1.5 Miller's Theorem

11.16. Apply Miller's theorem to resistor R_F in Fig. 11.68 and estimate the voltage gain of the circuit. Assume $V_A = \infty$ and R_F is large enough to allow the approximation $v_{out}/v_X = -g_m R_C$.

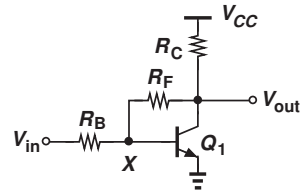


Figure 11.68

11.17. Repeat Problem 11.16 for the source follower in Fig. 11.69. Assume $\lambda = 0$ and R_F is large enough to allow the approximation $v_{out}/v_X = R_L/(R_L + g_m^{-1})$.

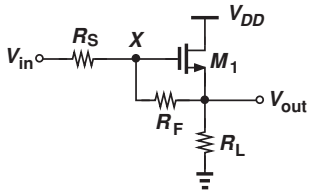


Figure 11.69

****11.18.** Consider the common-base stage illustrated in Fig. 11.70, where the output resistance of Q_1 is drawn explicitly. Utilize Miller's theorem to estimate the gain. Assume r_O is large enough to allow the approximation $v_{out}/v_X = g_m R_C$.

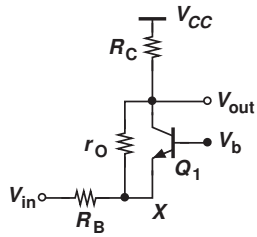


Figure 11.70

***11.19.** Using Miller's theorem, estimate the input capacitance of the circuit depicted in Fig. 11.71. Assume $\lambda > 0$ but neglect other capacitances. What happens if $\lambda \to 0$?

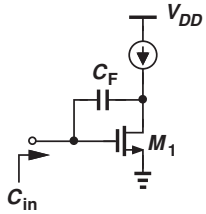


Figure 11.71

11.20. Repeat Problem 11.19 for the source follower shown in Fig. 11.72.

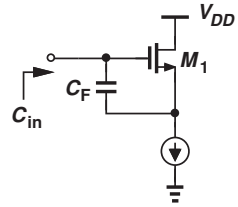


Figure 11.72

***11.21.** Using Miller's theorem, explain how the common-base stage illustrated in Fig. 11.73 provides a *negative* input capacitance. Assume $V_A = \infty$ and neglect other capacitances.

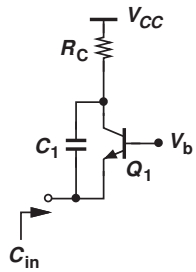


Figure 11.73

11.22. Use Miller's theorem to estimate the input and output poles of the circuit shown in Fig. 11.74. Assume $V_A = \infty$ and neglect other capacitances. Note that the circuit in fact has only one pole.

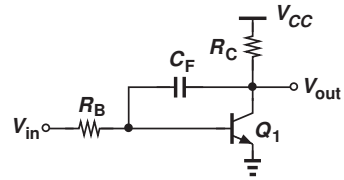


Figure 11.74

**11.23. Repeat Problem 11.22 for the circuit in Fig. 11.75.

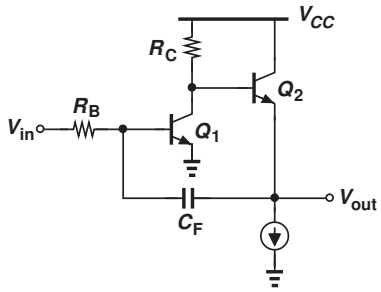


Figure 11.75

Sec. 11.2 High-Frequency Models of Transistors

**11.24. For the bipolar circuits depicted in Fig. 11.76, identify all of the transistor capacitances and determine which ones are in parallel and which ones are grounded on both ends.

**11.25. For the MOS circuits shown in Fig. 11.77, identify all of the transistor capacitances and determine which ones are in parallel and which ones are grounded on both ends.

**11.26. In arriving at Eq. (11.49) for the f_T of transistors, we neglected C_μ and C_{GD}. Repeat the derivation without this approximation.

**11.27. It can be shown that, if the minority carriers injected by the emitter into the base take τ_F seconds to cross the base region, then $C_b = g_m \tau_F$.

(a) Writing $C_\pi = C_b + C_{je}$, assuming that C_{je} is independent of the bias current, and using Eq. (11.49), derive an expression for the f_T of bipolar transistors in terms of the collector bias current.

(b) Sketch f_T as a function of I_C.

*11.28. It can be shown that $C_{GS} \approx (2/3)WLC_{ox}$ for a MOSFET operating in saturation. Using Eq. (11.49), prove that

$$2\pi f_T = \frac{3}{2}\frac{\mu_n}{L^2}(V_{GS} - V_{TH}). \qquad (11.180)$$

Note that f_T increases with the overdrive voltage.

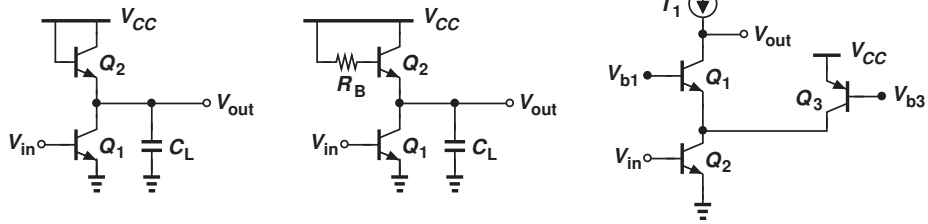


Figure 11.76

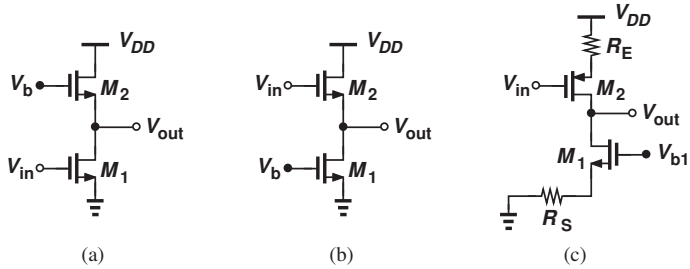


Figure 11.77

*11.29. Having solved Problem 11.28 successfully, a student attempts a different substitution for g_m: $2I_D/(V_{GS} - V_{TH})$, arriving at

$$2\pi f_T = \frac{3}{2}\frac{2I_D}{WLC_{ox}}\frac{1}{V_{GS} - V_{TH}}. \quad (11.181)$$

This result suggests that f_T *decreases* as the overdrive voltage increases! Explain this apparent discrepancy between Eqs. (11.180) and (11.181).

*11.30. Using Eq. (11.49) and the results of Problems 11.28 and 11.29, plot the f_T of a MOSFET (a) as a function of W for a constant I_D, (b) as a function of I_D for a constant W. Assume L remains constant in both cases.

*11.31. Using Eq. (11.49) and the results of Problems 11.28 and 11.29, plot the f_T of a MOSFET (a) as a function of $V_{GS} - V_{TH}$ for a constant I_D, (b) as a function of I_D for a constant $V_{GS} - V_{TH}$. Assume L remains constant in both cases.

*11.32. Using Eq. (11.49) and the results of Problems 11.28 and 11.29, plot the f_T of a MOSFET (a) as a function of W for a constant $V_{GS} - V_{TH}$, (b) as a function of $V_{GS} - V_{TH}$ for a constant W. Assume L remains constant in both cases.

*11.33. We wish to halve the overdrive voltage of a transistor so as to provide a greater voltage headroom in a circuit. Determine the change in the f_T if (a) I_D is constant and W is increased, or (b) W is constant and I_D is decreased. Assume L is constant.

*11.34. In order to lower channel-length modulation in a MOSFET, we double the device length. (a) How should the device width be adjusted to maintain the same overdrive voltage and the same drain current? (b) How do these changes affect the f_T of the transistor?

11.35. Using Miller's theorem, determine the input and output poles of the CE and CS stages depicted in Fig. 11.29(a) while including the output impedance of the transistors.

Sec. 11.4 Frequency Response of CE and CS Stage

11.36. The common-emitter stage of Fig. 11.78 employs a current-source load to achieve a high gain (at low frequencies). Assuming $V_A < \infty$ and using Miller's theorem, determine the input and output poles and hence the transfer function of the circuit.

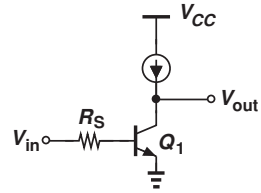


Figure 11.78

11.37. Repeat Problem 11.36 for the stage shown in Fig. 11.79.

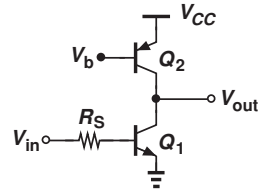


Figure 11.79

*11.38. Assuming $\lambda > 0$ and using Miller's theorem, determine the input and output poles of the stages depicted in Fig. 11.80.

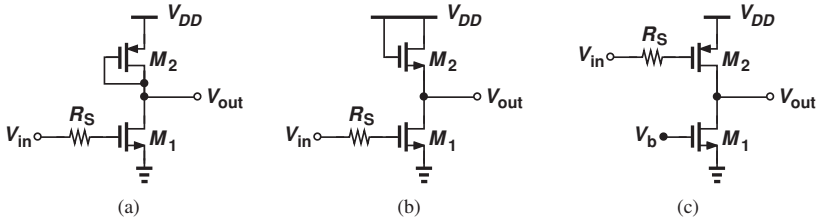


Figure 11.80

11.39. In the CS stage of Fig. 11.29(a), $R_S = 200\,\Omega$, $R_D = 1$ kΩ, $I_{D1} = 1$ mA, $C_{GS} = 50$ fF, $C_{GD} = 10$ fF, $C_{DB} = 15$ fF, and $V_{GS} - V_{TH} = 200$ mV. Determine the poles of the circuit using (a) Miller's approximation, and (b) the transfer function given by Eq. (11.70). Compare the results.

11.40. Consider the amplifier shown in Fig. 11.81, where $V_A = \infty$. Determine the poles of the circuit using (a) Miller's approximation, and (b) the transfer function expressed by Eq. (11.70). Compare the results.

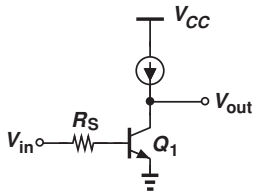


Figure 11.81

11.41. Repeat Problem 11.40 but use the dominant-pole approximation. How do the results compare?

*__11.42.__ Determine the input and output impedances of the stage depicted in Fig. 11.82 without using Miller's theorem. Assume $V_A = \infty$.

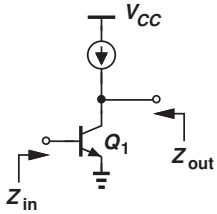


Figure 11.82

*__11.43.__ The circuit depicted in Fig. 11.83 is called an "active inductor." Neglecting other capacitances and assuming $\lambda = 0$, compute Z_{in}. Use Bode's rule to plot $|Z_{in}|$ as a function of frequency and explain why it exhibits inductive behavior.

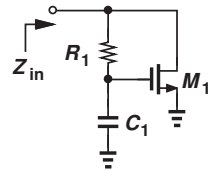


Figure 11.83

**__11.44.__ Compute the transfer function of the circuit shown in Fig. 11.84 without using Miller's theorem. Assume $\lambda > 0$.

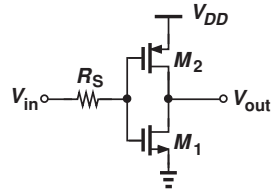


Figure 11.84

*__11.45.__ Calculate the input impedance of the stage illustrated in Fig. 11.85 without using Miller's theorem. Assume $\lambda = 0$.

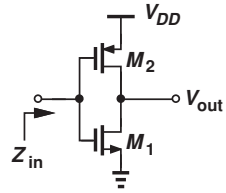


Figure 11.85

Sec. 11.5 Frequency Response of CB and CG Stages

11.46. Determine the transfer function of the circuits shown in Fig. 11.86. Assume $\lambda = 0$ for M_1.

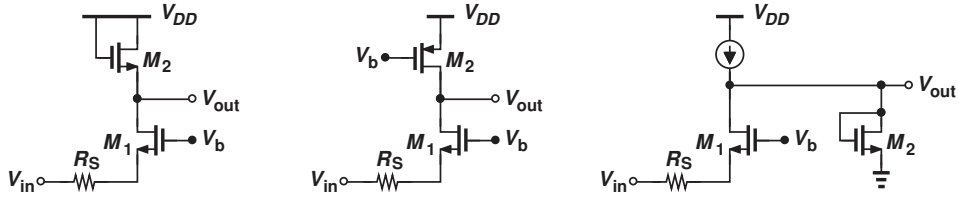


Figure 11.86

Sec. 11.6 Frequency Response of Followers

11.47. Consider the source follower shown in Fig. 11.87, where the current source is mistakenly replaced with a diode-connected device. Taking into account only C_{GS1}, compute the input capacitance of the circuit. Assume $\lambda \neq 0$.

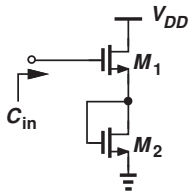


Figure 11.87

11.48. Determine the output impedance of the emitter follower depicted in Fig. 11.88, including C_μ and other capacitances. Sketch $|Z_{out}|$ as a function of frequency. Assume $V_A = \infty$.

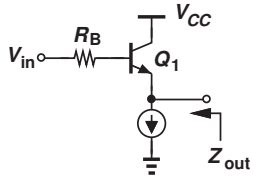


Figure 11.88

Sec. 11.7 Frequency Response of Cascode Stage

11.49. In the cascode of Fig. 11.89, Q_3 serves as a constant current source, providing 75% of the bias current of Q_1. Assuming $V_A = \infty$ and using Miller's theorem, determine the poles of the circuit. Is Miller's effect more or less significant here than in the standard cascode topology of Fig. 11.48(a)?

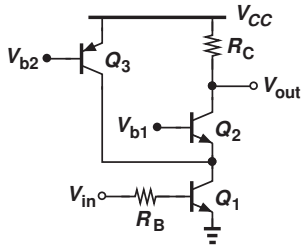


Figure 11.89

11.50. Due to manufacturing error, a parasitic resistor R_p has appeared in the cascode stage of Fig. 11.90. Assuming $\lambda = 0$ and using Miller's theorem, determine the poles of the circuit.

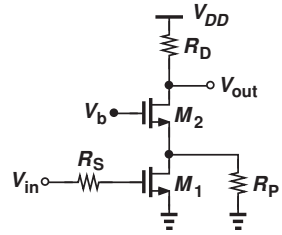


Figure 11.90

11.51. In analogy with the circuit of Fig. 11.89, a student constructs the stage depicted in Fig. 11.91 but mistakenly uses an NMOS device for M_3. Assuming $\lambda = 0$ and using Miller's theorem, compute the poles of the circuit.

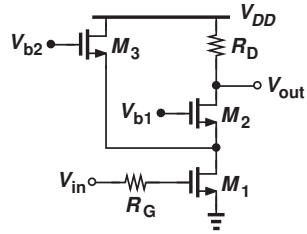


Figure 11.91

Design Problems

11.52. Using the results obtained in Problems 11.9 and 11.10, design the two-stage amplifier of Fig. 11.63 for a total voltage gain of 20 and a -3 dB bandwidth of 1 GHz. Assume each stage carries a bias current of 1 mA, $C_L = 50$ fF, and $\mu_n C_{ox} = 100\ \mu$A/V^2.

11.53. We wish to design the CE stage of Fig. 11.92 for an input pole at 500 MHz and an output pole at 2 GHz. Assuming $I_C = 1$ mA, $C_\pi = 20$ fF, $C_\mu = 5$ fF, $C_{CS} = 10$ fF, and $V_A = \infty$, and using Miller's theorem, determine the values of R_B and R_C such that the (low-frequency) voltage gain is maximized. You may need to use iteration.

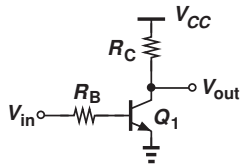


Figure 11.92

11.54. Repeat Problem 11.53 with the additional assumption that the circuit must drive a load capacitance of 20 fF.

11.55. We wish to design the common-base stage of Fig. 11.93 for a -3 dB bandwidth of 10 GHz. Assume $I_C = 1$ mA, $V_A = \infty$, $R_S = 50\,\Omega$, $C_\pi = 20$ fF, $C_\mu = 5$ fF, and $C_{CS} = 20$ fF. Determine the maximum allowable value of R_C and hence the maximum achievable gain. (Note that the input and output poles may affect the bandwidth.)

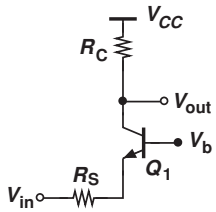


Figure 11.93

11.56. The emitter follower of Fig. 11.94 must be designed for an input capacitance of less than 50 fF. If $C_\mu = 10$ fF, $C_\pi = 100$ fF, $V_A = \infty$, and $I_C = 1$ mA, what is the minimum tolerable value of R_L?

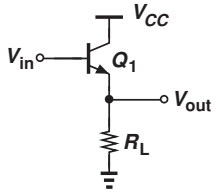


Figure 11.94

11.57. An NMOS source follower must drive a load resistance of 100 Ω with a voltage gain of 0.8. If $I_D = 1$ mA, $\mu_n C_{ox} = 100\,\mu\text{A/V}^2$, $C_{ox} = 12$ fF/μm^2, and $L = 0.18\,\mu$m, what is the minimum input capacitance that can be achieved? Assume $\lambda = 0$, $C_{GD} \approx 0$, $C_{SB} \approx 0$, and $C_{GS} = (2/3)WLC_{ox}$.

11.58. We wish to design the MOS cascode of Fig. 11.95 for an input pole of 5 GHz and an output pole of 10 GHz. Assume M_1 and M_2 are identical, $I_D = 0.5$ mA, $C_{GS} = (2/3)WLC_{ox}$, $C_{ox} = 12$ fF/μm^2, $\mu_n C_{ox} = 100\,\mu\text{A/V}^2$, $\lambda = 0$, $L = 0.18\,\mu$m, and $C_{GD} = C_0 W$, where $C_0 = 0.2$fF/μm denotes the gate-drain capacitance per unit width. Determine the maximum allowable values of R_G, R_D, and the voltage gain. Use Miller's approximation for C_{GD1}. Assume an overdrive voltage of 200 mV for each transistor.

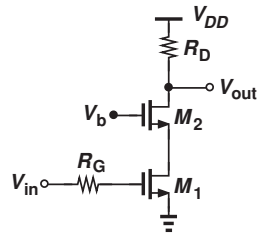


Figure 11.95

11.59. Repeat Problem 11.58 if $W_2 = 4W_1$ so as to reduce the Miller multiplication of C_{GD1}.

SPICE PROBLEMS

In the following problems, use the MOS device models given in Appendix A. For bipolar transistors, assume $I_{S,npn} = 5 \times 10^{-16}$ A, $\beta_{npn} = 100$, $V_{A,npn} = 5$ V, $I_{S,pnp} = 8 \times 10^{-16}$ A, $\beta_{pnp} = 50$, $V_{A,pnp} = 3.5$ V. Also, SPICE models the effect of charge storage in the base by a parameter called $\tau_F = C_b/g_m$. Assume $\tau_F(tf) = 20$ ps.

11.60. In the two-stage amplifier shown in Fig. 11.96, $W/L = 10\ \mu$m$/0.18\ \mu$m for M_1-M_4.

(a) Select the input dc level to obtain an output dc level of 0.9 V.

(b) Plot the frequency response and compute the low-frequency gain and the −3 dB bandwidth.

(c) Repeat (a) and (b) for $W = 20\ \mu$m and compare the results.

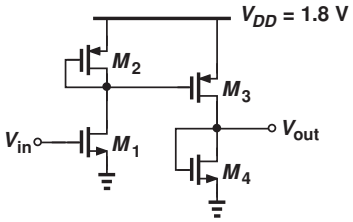


Figure 11.96

11.61. The circuit of Fig. 11.97 must drive a load capacitance of 100 fF.

(a) Select the input dc level to obtain an output dc level of 1.2 V.

(b) Plot the frequency response and compute the low-frequency gain and the −3 dB bandwidth.

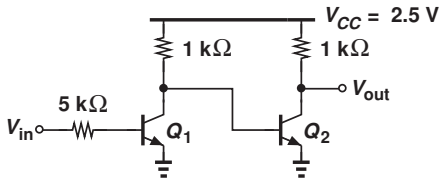


Figure 11.97

11.62. The self-biased stage depicted in Fig. 11.98 must drive a load capacitance of 50 fF with a maximum gain-bandwidth product (= midband gain × unity-gain bandwidth). Assuming $R_1 = 500\ \Omega$ and $L_1 = 0.18\ \mu$m, determine W_1, R_F, and R_D.

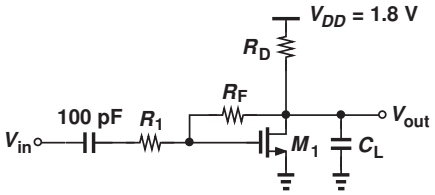


Figure 11.98

11.63. Repeat Problem 11.62 for the circuit shown in Fig. 11.99. (Determine R_F and R_C.)

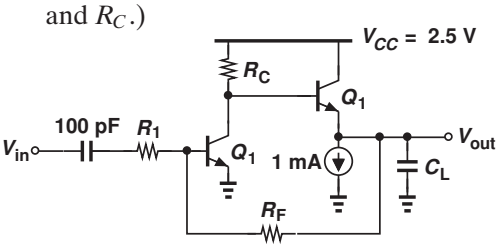


Figure 11.99

11.64. The two-stage amplifier shown in Fig. 11.100 must achieve a maximum gain-bandwidth product while driving $C_L = 50$ fF. Assuming M_1-M_4 have a width of W and a length of 0.18 μm, determine R_F and W.

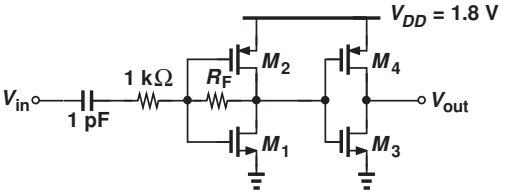


Figure 11.100