Contents

CHAPTER 1 Models for Integrated-Circuit Active				1.5.2	Comparison of Operating Regions of Bipolar and MOS Transistors 45	
Devi	ces 1			1.5.3	Decomposition of Gate-Source	
1.1	Introduction 1				Voltage 47	
1.2	Depletion Region of a pn Junction 1			1.5.4	Threshold Temperature Dependence 47	
	1.2.1 1.2.2	Depletion-Region Capacitance 5 Junction Breakdown 6		1.5.5	MOS Device Voltage Limitations 48	
1.3		Large-Signal Behavior of Bipolar Transistors 8			Small-Signal Models of MOS Transistors 49	
	1.3.1 Large-Signal Models in the			1.6.1	Transconductance 50	
	1.3.2	Forward-Active Region 8		1.6.2	Intrinsic Gate-Source and Gate-Drain Capacitance 51	
	1.5.2	Large-Signal Characteristics in the Forward-Active Region 14		1.6.3	Input Resistance 52	
				1.6.4	Output Resistance 52	
	1.3.3	Saturation and Inverse-Active Regions 16		1.6.5	Basic Small-Signal Model of the MOS Transistor 52	
	1.3.4			1.6.6	Body Transconductance 53	
	1.3.5	Dependence of Transistor Current Gain β_F on Operating Conditions 23		1.6.7	Parasitic Elements in the Small-Signal Model 54	
1.4	Small Trans	-Signal Models of Bipolar	1.7	1.6.8	MOS Transistor Frequency Response 55	
	1.4.1	Transconductance 26		Short-Channel Effects in MOS		
	1.4.2			Trans	istors 59	
	1.4.2	Input Resistance 28		1.7.1	Velocity Saturation from the Horizontal Field 59	
	1.4.4	Output Resistance 29		1.7.2	Transconductance and Transition	
	1.4.5	Basic Small-Signal Model of the		1.7.2	Frequency 63	
	1.4.6	Bipolar Transistor 30 Collector-Base Resistance 30		1.7.3	Mobility Degradation from the Vertical Field 65	
	1.4.7	Parasitic Elements in the	1.8	Waals	Inversion in MOS Transistors 65	
	1.1.7	Small-Signal Model 31	1.6	1.8.1	Drain Current in Weak Inversion 66	
	1.4.8	Specification of Transistor Frequency Response 34		1.8.2	Transconductance and Transition Frequency in Weak Inversion 69	
1.5	Large-Signal Behavior of Metal-Oxide-Semiconductor			Substrate Current Flow in MOS Transistors 71		
	1.5.1	Field-Effect Transistors 38 1.5.1 Transfer Characteristics of MOS Devices 38			nary of Active-Device neters 73	

viii Contents

	MOS, and BiCMOS d-Circuit Technology 78	 2.9 Active Devices in MOS Integrated Circuits 131 2.9.1 <i>n</i>-Channel Transistors 131
2.1 Intr	oduction 78	2.9.2 <i>p</i> -Channel Transistors 144
2.2 Bas	ic Processes in Integrated-Circuit	2.9.3 Depletion Devices 144
	rication 79	2.9.4 Bipolar Transistors 145
2.2.	Electrical Resistivity of Silicon 79	2.10 Passive Components in MOS
2.2.2	2 Solid-State Diffusion 80	Technology 146
2.2.3	1	2.10.1 Resistors 146
2.2	Layers 82	2.10.2 Capacitors in MOS Technology 148
2.2.4 2.2.5	8 T 3	2.10.3 Latchup in CMOS Technology 151
2.2.0	-	2.11 BiCMOS Technology 152
2.2.3	•	2.12 Heterojunction Bipolar Transistors 153
2.2.8		2.13 Interconnect Delay 156
	h-Voltage Bipolar grated-Circuit Fabrication 88	2.14 Economics of Integrated-Circuit Fabrication 156
	ranced Bipolar Integrated-Circuit	2.14.1 Yield Considerations in
	rication 92	Integrated-Circuit Fabrication 157
2.5 Act	ive Devices in Bipolar Analog	2.14.2 Cost Considerations in Integrated-Circuit Fabrication 159
Inte	grated Circuits 95	A.2.1 SPICE Model-Parameter Files 162
2.5.		A.2.1 STICE Woder-1 manifeld Titles 102
2.5.7	96	CHAPTER 3
2.5.2	2 Integrated-Circuit <i>pnp</i> Transistors 107	Single-Transistor and Multiple-Transistor Amplifiers 169
	sive Components in Bipolar	3.1 Device Model Selection for
	grated Circuits 115	Approximate Analysis of Analog
2.6.1		Circuits 170
2.6.2	2 Epitaxial and Epitaxial Pinch Resistors 119	3.2 Two-Port Modeling of Amplifiers 171
2.6.3		3.3 Basic Single-Transistor Amplifier
2.6.4		Stages 173
2.6.5	5 Junction Diodes 122	3.3.1 Common-Emitter Configuration 174
	difications to the Basic Bipolar	3.3.2 Common-Source Configuration 178
	cess 123	3.3.3 Common-Base Configuration 182
2.7.2 2.7.2		3.3.4 Common-Gate Configuration 185
2.1.2	High-Performance Active Devices	3.3.5 Common-Base and Common-Gate Configurations with Finite r_0 187
2.7.3		3.3.5.1 Common-Base and Common-Gate Input Resistance 187
2.8 MO	S Integrated-Circuit Fabrication Vma	3.3.5.2 Common-Base and
127	k .	Common-Gate Output
	rafa	Choes Xg/ Resistance 189
	•	

ix

3.3.6	Common-Collector Configuration (Emitter Follower) 191			3.5.6.8	Offset Voltage Drift in the Source-Coupled Pair 236		
3.3.7	Common-Drain Configuration (Source Follower) 194			3.5.6.9	Small-Signal Characteristics of Unbalanced Differential Amplifiers 237		
3.3.8	Common-Emitter Amplifier with Emitter Degeneration 196	A.3.1			tatistics and the Gaussian		
3.3.9	Common-Source Amplifier with Source Degeneration 199		Distribution 244				
Multi	ple-Transistor Amplifier Stages	CHAP					
201				-	ctive Loads, and		
3.4.1	The CC-CE, CC-CC, and Darlington	Refe	rence	s 251			
	Configurations 201	4.1	Introd	luction	251		
3.4.2	The Cascode Configuration 205 3.4.2.1 The Bipolar Cascode 205	4.2	Current Mirrors 251				
	3.4.2.1 The Bipolar Cascode 203 3.4.2.2 The MOS Cascode 207		4.2.1	General	Properties 251		
3.4.3	The Active Cascode 210		4.2.2	Simple	Current Mirror 253		
				4.2.2.1	Bipolar 253		
3.4.4	The Super Source Follower 212	lt al		4.2.2.2	MOS 255		
Diffe	rential Pairs 214 rimes en la test	ian	4.2.3		Current Mirror with Beta		
3.5.1	The dc Transfer Characteristic of an 41				258		
	Emitter-Coupled Pair 214				Bipolar 258		
3.5.2	The dc Transfer Characteristic with			4.2.3.2			
	Emitter Degeneration 216		4.2.4		Current Mirror with		
3.5.3	The dc Transfer Characteristic of a			_	ration 260		
	Source-Coupled Pair 217				Bipolar 260 MOS 261		
3.5.4	Introduction to the Small-Signal		125				
	Analysis of Differential Amplifiers		4.2.5		e Current Mirror 261 Bipolar 261		
	220				MOS 264		
3.5.5	Small-Signal Characteristics of		4.2.6		Current Mirror 272		
	Balanced Differential Amplifiers		7.2.0		Bipolar 272		
	223				MOS 275		
3.5.6	Device Mismatch Effects in	4.3	Activ	e Loads	276		
	Differential Amplifiers 229	1.3					
	3.5.6.1 Input Offset Voltage and Current 230		4.3.1		ion 276		
	3.5.6.2 Input Offset Voltage of the		4.3.2		on-Emitter-Common-Source		
	Emitter-Coupled Pair 230			-	er with Complementary		
	3.5.6.3 Offset Voltage of the				277		
	Emitter-Coupled Pair:		4.3.3		on-Emitter–Common-Source		
	Approximate Analysis 231			-	er with Depletion Load 280		
	3.5.6.4 Offset Voltage Drift in the		4.3.4		on-Emitter-Common-Source		
	Emitter-Coupled Pair 233			•	er with Diode-Connected		
	3.5.6.5 Input Offset Current of the			Load			
	Emitter-Coupled Pair 233		4.3.5		ntial Pair with Current-Mirror		
	3.5.6.6 Input Offset Voltage of the Source-Coupled Pair 234				285 - Large Signal Analysis 285		
	3.5.6.7 Offset Voltage of the			4.3.5.1	Large-Signal Analysis 285 Small-Signal Analysis 286		
	Source-Coupled Pair:				Common-Mode Rejection		
	Approximate Analysis 235			2.3.0	Ratio 291		

3.4

3.5

4.4	Voltag	ge and C	Surrent References 297		5.3.1		
	4.4.1		nrrent Biasing 297 Bipolar Widlar Current		5.3.2	Follower 353 Distortion in the Source Follower	
			Source 297			355	
		4.4.1.2	MOS Widlar Current Source 300	5.4	Class	B Push–Pull Output Stage 359	
		4.4.1.3	Bipolar Peaking Current Source 301		5.4.1	Transfer Characteristic of the Class B Stage 360	
		4.4.1.4	MOS Peaking Current Source 302		5.4.2	Power Output and Efficiency of the Class B Stage 362	
	4.4.2		Insensitive Biasing 303 Widlar Current Sources		5.4.3	Practical Realizations of Class B Complementary Output Stages 366	
		4.4.0.0	304		5.4.4	All-npn Class B Output Stage 373	
			Current Sources Using Other Voltage Standards 305 Self-Biasing 307		5.4.5	Quasi-Complementary Output Stages 376	
	4.4.3		0		5.4.6	Overload Protection 377	
	7.7.3	Temperature-Insensitive Biasing 315		5.5	CMO	S Class AB Output Stages 379	
		4.4.3.1	Band-Gap-Referenced		5.5.1	Common-Drain Configuration 380	
		4422	Bias Circuits in Bipolar Technology 315 Road Con Referenced		5.5.2	Common-Source Configuration with Error Amplifiers 381	
		4.4.3.2	Band-Gap-Referenced Bias Circuits in CMOS Technology 321		5.5.3	Alternative Configurations 388 5.5.3.1 Combined Common-Drain Common-Source	
A.4.1	Mirro A.4.1.	ning Cor rs 325 1 Bipola 2 MOS	ar 325			Configuration 388 5.5.3.2 Combined Common-Drain Common-Source Configuration with High	
A.4.2	Pair w A.4.2.	ith Acti 1 Bipol				Swing 390 5.5.3.3 Parallel Common-Source Configuration 390	
	A.4.2.2 MOS 332 APTER 5			CHAPTER 6 Operational Amplifiers with Single-Ended Outputs 400			
Outp	ut Sta	ges 3	41	6.1	Appli	cations of Operational Amplifiers	
5.1	Introd	luction	341		401		
5.2	The Emitter Follower as an Output Stage				6.1.1	Basic Feedback Concepts 401	
	341				6.1.2	Inverting Amplifier 402	
	5.2.1		r Characteristics of the Follower 341		6.1.3	Noninverting Amplifier 404	
	5.2.2		Output and Efficiency 344		6.1.4	Differential Amplifier 404	
	5.2.3		-Follower Drive		6.1.5	Nonlinear Analog Operations 405	
	3.2.3		ments 351		6.1.6	Integrator, Differentiator 406	
	5.2.4		ignal Properties of the Follower 352		6.1.7	Internal Amplifiers 407 6.1.7.1 Switched-Capacitor Amplifier 407	
5.3	The S 353	ource F	ollower as an Output Stage			6.1.7.2 Switched-Capacitor Integrator 412	

хi

6.2	Deviations from Ideality in Real Operational Amplifiers 415			CHAPTER 7 Frequency Response of Integrated			
	6.2.1	6.2.1 Input Bias Current 415		Circuits 490			
	6.2.2	Input Offset Current 416	7.1	Introd	luction 490		
	6.2.3	Input Offset Voltage 416	7.2	Singl	e-Stage Amplifiers 490		
	6.2.4 6.2.5	Common-Mode Input Range 416 Common-Mode Rejection Ratio (CMRR) 417		7.2.1	Single-Stage Voltage Amplifiers and the Miller Effect 490 7.2.1.1 The Bipolar Differential		
	6.2.6	Power-Supply Rejection Ratio (PSRR) 418			Amplifier: Differential- Mode Gain 495		
	6.2.7	Input Resistance 420			7.2.1.2 The MOS Differential Amplifier: Differential-		
	6.2.8	Output Resistance 420			Mode Gain 499		
	6.2.9	Frequency Response 420		7.2.2	Frequency Response of the		
	6.2.10	Operational-Amplifier Equivalent Circuit 420			Common-Mode Gain for a Differential Amplifier 501		
6.3		Basic Two-Stage MOS Operational Amplifiers 421			Frequency Response of Voltage Buffers 503		
	6.3.1	Input Resistance, Output Resistance, and Open-Circuit Voltage Gain 422			7.2.3.1 Frequency Response of the Emitter Follower 5057.2.3.2 Frequency Response of the		
	6.3.2	Output Swing 423			Source Follower 511		
	6.3.3	Input Offset Voltage 424		7.2.4	Frequency Response of Current		
	6.3.4	Common-Mode Rejection Ratio 427			Buffers 514 7.2.4.1 Common-Base Amplifier		
	6.3.5	Common-Mode Input Range 427			Frequency Response 516		
	6.3.6	Power-Supply Rejection Ratio (PSRR) 430			7.2.4.2 Common-Gate Amplifier Frequency Response 517		
	6.3.7 6.3.8	Effect of Overdrive Voltages 434 Layout Considerations 435	7.3	Multistage Amplifier Frequency Response 518			
6.4		Stage MOS Operational Amplifiers		7.3.1	Dominant-Pole Approximation 518		
	with (h Cascodes 438		7.3.2	Zero-Value Time Constant Analysis 519		
6.5		OS Telescopic-Cascode Operational uplifiers 439		7.3.3	Cascode Voltage-Amplifier Frequency Response 524		
6.6		Folded-Cascode Operational ifiers 442		7.3.4 7.3.5	Cascode Frequency Response 527 Frequency Response of a Current		
6.7	MOS Ampl	Active-Cascode Operational ifiers 446		7.3.3	Mirror Loading a Differential Pair 534		
6.8	Bipol	ar Operational Amplifiers 448		7.3.6	Short-Circuit Time Constants 536		
	6.8.1	.1 The dc Analysis of the NE5234 7 Operational Amplifier 452			vsis of the Frequency Response of E5234 Op Amp 539		
	6.8.2	Transistors that Are Normally Off 467		7.4.1	High-Frequency Equivalent Circuit of the NE5234 539		
	6.8.3	Small-Signal Analysis of the NE5234 Operational Amplifier 469		7.4.2	Calculation of the -3-dB Frequency of the NE5234 540		
	6.8.4	Calculation of the Input Offset Voltage and Current of the NE5234 477		7.4.3	Nondominant Poles of the NE5234 542		

xii Contents

7.5		n Between Frequency Res ne Response 542	sponse	9.3	Instab 626	ility and the Nyquist Criterion	
				9.4	Comp	ensation 633	
CHAP	ER 8 back	552			9.4.1	Theory of Compensation 633	
					9.4.2	Methods of Compensation 637	
8.1 8.2		eedback Equation 553 ensitivity 555			9.4.3	Two-Stage MOS Amplifier Compensation 643	
8.3		of Negative Feedback on on 555			9.4.4	Compensation of Single-Stage CMOS Op Amps 650	
8.4	Feedba	ck Configurations 557			9.4.5	Nested Miller Compensation 654	
	8.4.1	Series-Shunt Feedback 557		9.5	Root-	Locus Techniques 664	
		Shunt-Shunt Feedback 560 Shunt-Series Feedback 561			9.5.1	Root Locus for a Three-Pole Transfer Function 665	
	8.4.4	Series-Series Feedback 562			9.5.2	Rules for Root-Locus Construction 667	
8.5		al Configurations and the ling 563	Effect		9.5.3	Root Locus for Dominant-Pole Compensation 676	
		Shunt-Shunt Feedback 563 Series-Series Feedback 569	ı		9.5.4	Root Locus for Feedback-Zero Compensation 677	
	8.5.3	Series-Shunt Feedback 579		9.6	Slew	Rate 681	
		Shunt-Series Feedback 583 Summary 587			9.6.1	Origin of Slew-Rate Limitations 681	
8.6		Stage Feedback 587			9.6.2	Methods of Improving Slew-Rate in Two-Stage Op Amps 685	
		Local Series-Series Feedback Local Series-Shunt Feedback			9.6.3	Improving Slew-Rate in Bipolar Op Amps 687	
8.7	The Vol Circuit	tage Regulator as a Feedb	oack		9.6.4	Improving Slew-Rate in MOS Op Amps 688	
8.8	Feedbac Ratio	ck Circuit Analysis Using 599	Return		9.6.5	Effect of Slew-Rate Limitations on Large-Signal Sinusoidal	
		Closed-Loop Gain Using Ret Ratio 601	urn	A O 1	A male	Performance 692	
	8.8.2	8.8.2 Closed-Loop Impedance Formula			-	sis in Terms of Return-Ratio eters 693	
	8.8.3	Jsing Return Ratio 607 Summary—Return-Ratio Ana 512	alysis	A.9.2	Roots	of a Quadratic Equation 694	
8.9		ng Input and Output Ports	in	CHAPTER 10 Nonlinear Analog Circuits 704			
				10.1 Introduction 704			
Frequ	CHAPTER 9 Frequency Response and Stability of			10.2	Analog	Multipliers Employing the Transistor 704	
Feed	back A	mplifiers 624			10.2.1 The Emitter-Coupled Pair as a S		
9.1	Introduction 624			•	Multiplier 704		
9.2		n Between Gain and Band back Amplifiers 624	lwidth	1		The dc Analysis of the Gilbert Multiplier Cell 706	

	10.2.3 The Gilbert Cell as an Analog Multiplier 708		11.6.2 Effect of Practical Feedback on Noise Performance 765	
	10.2.4 A Complete Analog Multiplier 71110.2.5 The Gilbert Multiplier Cell as a	11.7	Noise Performance of Other Transistor Configurations 771	
	Balanced Modulator and Phase Detector 712		11.7.1 Common-Base Stage Noise Performance 771	
10.3	Phase-Locked Loops (PLL) 716		11.7.2 Emitter-Follower Noise	
	10.3.1 Phase-Locked Loop Concepts 716		Performance 773	
	10.3.2 The Phase-Locked Loop in the Locked Condition 718		11.7.3 Differential-Pair Noise Performance 773	
	10.3.3 Integrated-Circuit Phase-Locked	11.8	Noise in Operational Amplifiers 776	
10.1	Loops 727	11.9	Noise Bandwidth 782	
10.4	Nonlinear Function Synthesis 731	11.10	Noise Figure and Noise Temperature 786	
CHAP	e in Integrated Circuits 736		11.10.1 Noise Figure 786	
	_		11.10.2 Noise Temperature 790	
11.1	Introduction 736		•	
11.2	Sources of Noise 736	CHAPT	TED 12	
	11.2.1 Shot Noise 736		Differential Operational	
	11.2.2 Thermal Noise 740		olifiers 796	
	11.2.3 Flicker Noise (1/f Noise) 741	12.1	Introduction 796	
	11.2.4 Burst Noise (<i>Popcorn Noise</i>) 742	12.2	Properties of Fully Differential	
11.2	11.2.5 Avalanche Noise 743		Amplifiers 796	
11.3	Noise Models of Integrated-Circuit Components 744	12.3	Small-Signal Models for Balanced Differential Amplifiers 799	
	11.3.1 Junction Diode 744	12.4	Common-Mode Feedback 804	
	11.3.2 Bipolar Transistor 745	12.1	12.4.1 Common-Mode Feedback at Low	
	11.3.3 MOS Transistor 746		Frequencies 805	
	11.3.4 Resistors 747		12.4.2 Stability and Compensation	
	11.3.5 Capacitors and Inductors 747		Considerations in a CMFB	
11.4	Circuit Noise Calculations 748		Loop 810	
	11.4.1 Bipolar Transistor Noise Performance 750	12.5	CMFB Circuits 811	
	11.4.2 Equivalent Input Noise and the		12.5.1 CMFB Using Resistive Divider and Amplifier 812	
11.5	Minimum Detectable Signal 754 Equivalent Input Noise Generators 756		12.5.2 CMFB Using Two Differential Pairs 816	
11.5	11.5.1 Bipolar Transistor Noise Generators		12.5.3 CMFB Using Transistors in the	
	757		Triode Region 819	
	11.5.2 MOS Transistor Noise Generators		12.5.4 Switched-Capacitor CMFB 821	
	762	12.6	Fully Differential Op Amps 823	
11.6	Effect of Feedback on Noise Performance 764		12.6.1 A Fully Differential Two-Stage Op Amp 823	
	11.6.1 Effect of Ideal Feedback on Noise Performance 764		12.6.2 Fully Differential Telescopic Cascode Op Amp 833	

xiv Symbol Convention

12.6.3 Fully Differential Folded-Cascode Op Amp 83412.6.4 A Differential Op Amp with Two

Differential Input Stages 835

- 12.6.5 Neutralization 835
- 12.7 Unbalanced Fully Differential Circuits
- 12.8 Bandwidth of the CMFB Loop 844

- 12.9 Analysis of a CMOS Fully Differential Folded-Cascode Op Amp 845
 - 12.9.1 DC Biasing 848
 - 12.9.2 Low-Frequency Analysis 850
 - 12.9.3 Frequency and Time Responses in a Feedback Application 856

Index 871

Symbol Convention

Unless otherwise stated, the following symbol convention is used in this book. Bias or dc quantities, such as transistor collector current I_C and collector-emitter voltage V_{CE} , are represented by uppercase symbols with uppercase subscripts. Small-signal quantities, such as the incremental change in transistor collector current i_c , are represented by lowercase symbols with lowercase subscripts. Elements such as transconductance g_m in small-signal equivalent circuits are represented in the same way. Finally, quantities such as total collector current I_c , which represent the sum of the bias quantity and the signal quantity, are represented by an uppercase symbol with a lowercase subscript.