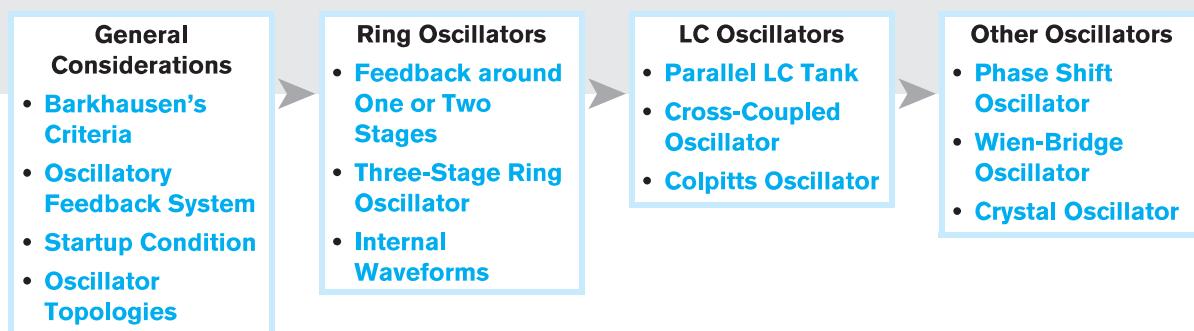


13

Oscillators

Most of our studies in previous chapters have focused on the analysis and design of amplifiers. In this chapter, we turn our attention to another important class of analog circuits, namely, oscillators. From your laptop computer to your cell phone, today's electronic devices use oscillators for numerous purposes, and pose interesting challenges. For example, the clock driving a 3 GHz microprocessor is generated by an on-chip oscillator running at 3 GHz. Also, a WiFi transceiver employs a 2.4 GHz or 5 GHz on-chip oscillator to generate a "carrier." Shown below is the outline of the chapter. The reader is encouraged to review Chapter 12 before delving into oscillators.



13.1 GENERAL CONSIDERATIONS

We know from previous chapters that an amplifier *senses* a signal and reproduces it at the output, perhaps with some gain. An oscillator, on the other hand, *generates* a signal, typically a periodic one. For example, the clock in a microprocessor resembles a square wave (Fig. 13.1).

How can a circuit generate a periodic output without an input? Let us return to our study of amplifier stability in Chapter 12 and recall that a negative-feedback circuit can

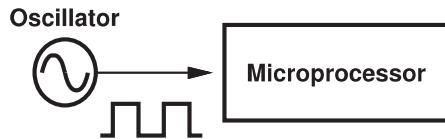


Figure 13.1 High-speed oscillator driving a microprocessor.

oscillate if Barkhausen's criteria are met. That is, as shown in Fig. 13.2, we have

Did you know?

The most commonplace use of oscillators is in (electronic) watches. A crystal oscillator (studied later in this chapter) runs at a precise frequency of 32,768 ($= 2^{15}$) Hz. This frequency is then divided down by means of a 15-bit counter to generate a 1-Hz square waveform, providing the "time base." This waveform shows the seconds on the watch. It is also divided by 60 and another 60 to count the minutes and the hours, respectively. A great challenge in early electronic watches was to design these counters for a very low power consumption so that the watch battery would last a few months.

$$\frac{Y}{X}(s) = \frac{H(s)}{1 + H(s)}, \quad (13.1)$$

which goes to infinity at a frequency of ω_1 if $H(s = j\omega_1) = -1$, or, equivalently, $|H(j\omega_1)| = 1$ and $\angle H(j\omega_1) = 180^\circ$. We may therefore view an oscillator as a badly-designed feedback amplifier! The key point here is that the signal traveling around the loop experiences so much phase shift (i.e., delay) that, upon reaching the subtractor, it actually *enhances* X . With enough loop gain, the circuit continues to amplify X indefinitely, generating an infinitely large output waveform from a finite swing at X .

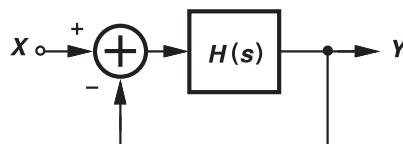


Figure 13.2 Feedback system for oscillation study.

It is important not to confuse the *frequency-dependent* 180° phase shift stipulated by Barkhausen with the 180° phase shift necessary for negative feedback. As depicted in Fig. 13.3(a), the loop contains one net signal inversion (the negative sign at the input of the adder) so as to ensure negative feedback *and* another 180° of phase shift at ω_1 . In other words, the *total* phase shift around the loop reaches 360° at ω_1 [Fig. 13.3(b)].

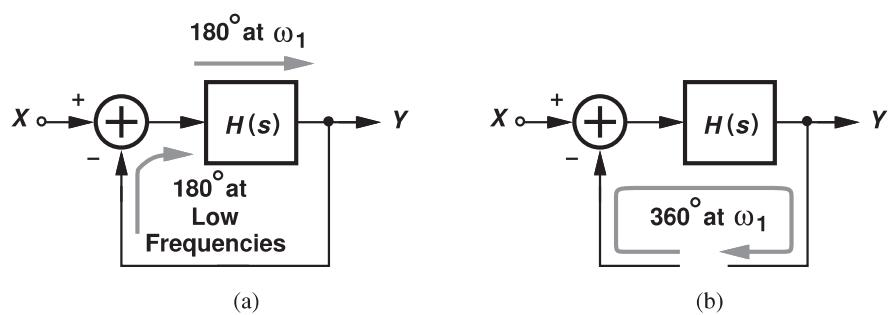


Figure 13.3 (a) Phase shift around an oscillator loop, (b) alternative view.

We must now answer two urgent questions. First, where does X come from? (We just stated that oscillators do not have an input.) In practice, X comes from the noise of the devices within the loop. Transistors and resistors in the oscillator produce noise at all frequencies, providing the “seed” for oscillation at ω_1 . Second, does the output amplitude really go to infinity? No, in reality, saturation or nonlinear effects in the circuit limit the output swing. After all, if the supply voltage is 1.5 V, it would be difficult to produce a swing greater than this amount.¹ For example, consider the conceptual arrangement shown in Fig. 13.4, where a common-source stage provides amplification within $H(s)$. As the output swing grows, at some point M_1 enters the triode region and its transconductance falls. Consequently, the loop gain decreases, eventually approaching the barely acceptable value, unity.

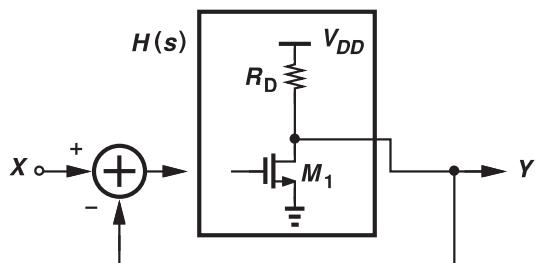


Figure 13.4 Feedback loop containing a common-source stage.

**Example
13.1**

An oscillator employs a differential pair [Fig. 13.5(a)]. Explain what limits the output amplitude.

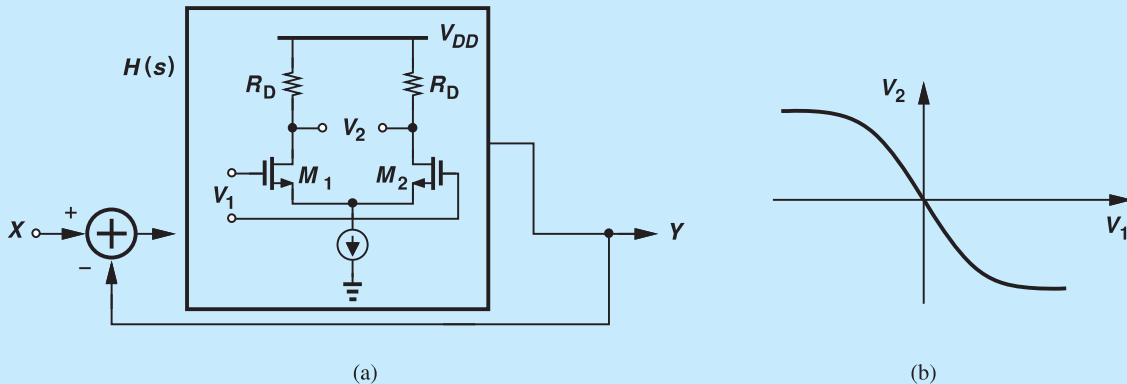


Figure 13.5

Solution

As the input swing to the differential pair grows, the circuit begins to experience saturation [Fig. 13.5(b)]. (Recall the large-signal behavior of differential pairs in Chapter 10.) Thus, the gain of the differential pair (i.e., the slope of the input-output characteristic) drops and so does the loop gain. The oscillation amplitude growth ceases at some point. In fact, if V_1 is large enough, the tail current is steered completely to the left or to the right, allowing V_2 to swing from $-I_{SS}R_D$ to $+I_{SS}R_D$. This is the maximum oscillation amplitude.

Exercise

Repeat the above example for a bipolar differential pair.

¹But some oscillators can generate an output swing about twice the supply voltage.

TABLE 13.1 Summary of various oscillator topologies and their applications.

Oscillator Topology	LC Oscillators					
	Ring Oscillator	Cross-Coupled Oscillator	Colpitts Oscillator	Phase Shift Oscillator	Wien-Bridge Oscillator	Crystal Oscillator
Implementation	Integrated	Integrated	Discrete or Integrated	Discrete	Discrete	Discrete or Integrated
Typical Frequency Range	Up to Several Gigahertz	Up to Hundreds of Gigahertz	Up to Tens of Gigahertz	Up to a Few Megahertz	Up to a Few Megahertz	Up to About 100 MHz
Application	Microprocessors and Memories	Wireless Transceivers	Stand-Alone oscillators	Prototype Design	Prototype Design	Precise Reference

Startup Condition From the first Barkhausen criterion, we may design the circuit for a unity loop gain at the desired oscillation frequency, ω_1 . This is called the oscillation “startup condition.” However, this choice places the circuit at the edge of failure: a slight change in the temperature, process, or supply voltage may drop the loop gain below 1. For this and other reasons, the loop gain is usually quite larger than unity. (In fact, the design typically begins with the required output voltage swing rather than the loop gain.)

What aspects of an oscillator design are important? Depending on the application, the specifications include the frequency of oscillation, output amplitude, power consumption, and complexity. In some cases, the “noise” in the output waveform is also critical.

Oscillators can be realized as either integrated or discrete circuits. The topologies are quite different in the two cases but still rely on Barkhausen’s criteria. We study both types here. It is helpful to first take a glance at the various types of oscillators studied in this chapter. Table 13.1 summarizes the topologies and some of their attributes.

13.2

RING OSCILLATORS

Most microprocessors and memories incorporate CMOS “ring oscillators.” As the name implies, the circuit consists of a number of stages in a ring, but to understand the underlying principles, we must take a few steps back.

Let us place a common-source amplifier in a negative-feedback loop and see if it oscillates. As shown in Fig. 13.6(a), we tie the output to the input. The feedback (at low frequencies) is negative because the stage has a voltage gain of $-g_m R_D$ (if $\lambda = 0$). Now, consider the small-signal model [Fig. 13.6(b)]. Does this circuit oscillate? Of the two Barkhausen’s criteria, the loop gain requirement, $|H(j\omega_1)| = 1$, appears possible. But how about the phase requirement? Neglecting C_{GD1} , we observe that the circuit’s capacitances merge into one at node X , forming a single (open-loop) pole with R_D : $\omega_{p,X} = -(R_D C_L)^{-1}$. Unfortunately, a single pole can provide a maximum phase shift of -90° (at $\omega = \infty$). That is, the frequency-dependent phase shift of the open-loop transfer function, $H(s)$, does not exceed -90° , prohibiting oscillation. From the perspective of Fig. 13.3(b), the *total* phase shift around the loop cannot reach 360° .

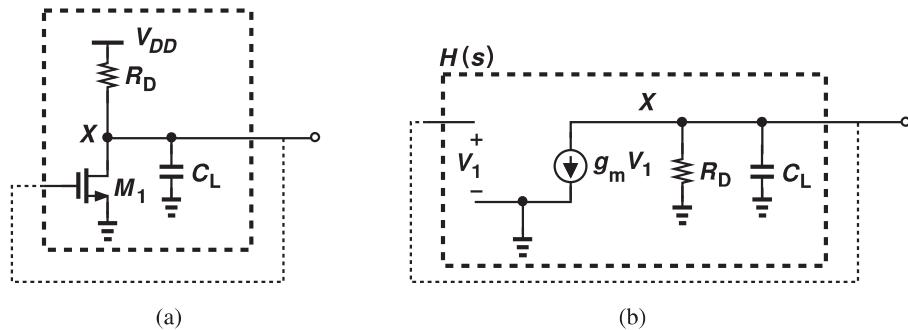


Figure 13.6 (a) Hypothetical oscillator using a single CS stage, (b) equivalent circuit of (a).

This brief analysis suggests that we should increase the delay or phase shift around the loop. For example, let us cascade *two* CS stages (Fig. 13.7). Now, the open-loop circuit contains two poles, exhibiting a maximum phase shift of 180° . Do we have an oscillator? No, not yet; each CS stage provides a phase shift of -90° only at $\omega = \infty$, but no *gain* at this frequency. That is, we still cannot meet both of Barkhausen's criteria at the same frequency.

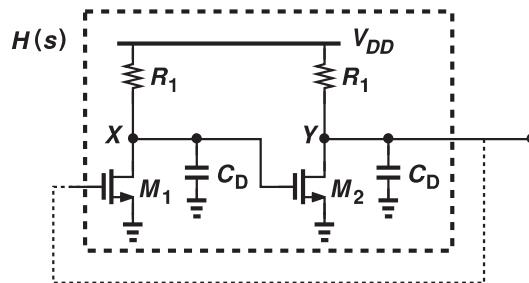


Figure 13.7 Feedback loop using two CS stages.

By now, we see the trend and postulate that we must insert one more CS stage in the loop, as shown in the “ring oscillator” of Fig. 13.8.² Each pole must provide a phase shift of only 60° (or -60°). Since the phase shift for a pole at $R_D C_D$ is equal to $-\tan^{-1}(R_D C_D \omega)$,

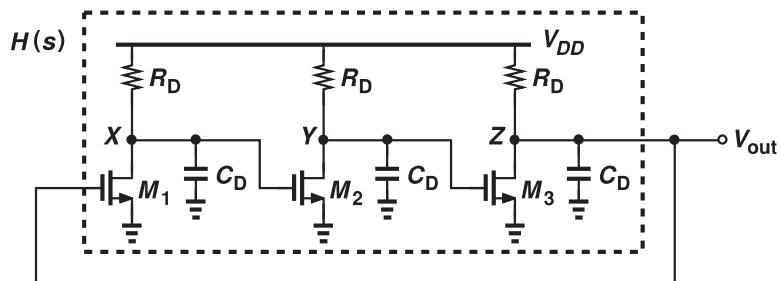


Figure 13.8 Simple three-stage ring oscillator.

²We neglect C_{GD} here.

we have

$$-\tan^{-1}(R_D C_D \omega_1) = -60^\circ, \quad (13.2)$$

obtaining an oscillation frequency of

$$\omega_1 = \frac{\sqrt{3}}{R_D C_D}. \quad (13.3)$$

The reader is encouraged to apply the perspective of Fig. 13.3(b) and prove that the total phase shift around the loop is 360° at ω_1 . The startup condition is calculated by setting $H(s)$ at $s = j\omega_1$ equal to unity. If $\lambda = 0$, the transfer function of each stage is given by $-g_m R_D / (1 + R_D C_D s)$. We replace s with $j\omega_1$, find the magnitude of the transfer function, raise it to the third power (for three identical stages), and equate the result to 1:

$$\left(\frac{g_m R_D}{\sqrt{1 + R_D^2 C_D^2 \omega_1^2}} \right)^3 = 1. \quad (13.4)$$

It follows that

$$g_m R_D = \sqrt{1 + R_D^2 C_D^2 \omega_1^2} \quad (13.5)$$

$$= 2, \quad (13.6)$$

indicating that the *low-frequency* gain of each stage must exceed 2 to ensure oscillation startup.

**Example
13.2**

A student runs a transient SPICE simulation on the ring oscillator of Fig. 13.8 but observes that all three drain voltages are equal and the circuit does not oscillate. Explain why. Assume that the stages are identical.

Solution

At the beginning of a transient simulation, SPICE computes the dc operating points for all of the devices. With identical stages, SPICE finds equal drain voltages as one solution of the network and retains it. Thus, the three drain voltages remain at the same value indefinitely. In the actual circuit, on the other hand, the electronic noise of the devices perturbs these voltages, initiating oscillation. (The transient simulation in SPICE does not include device noise.) In order to “kick” the circuit in SPICE, we can apply an initial condition of, say, 0 to node X . As a result, $V_Y = V_{DD}$, and $V_Z \approx 0$, forcing V_X to rise toward V_{DD} . Thus, SPICE cannot find an equilibrium point and is forced to allow oscillation.

Exercise

What happens if the ring contains four identical stages and we apply an initial condition of zero to one of the nodes?

Another type of ring oscillator can be conceived as follows. Suppose we replace the load resistors in Fig. 13.8 with PMOS current sources as shown in Fig. 13.9(a). The circuit still satisfies our foregoing derivations if we substitute $r_{Op} || r_{On}$ for R_D .³ But let us change

³We assume all of the transistors are in saturation, which is not quite correct when the drain voltage comes close to ground or V_{DD} .

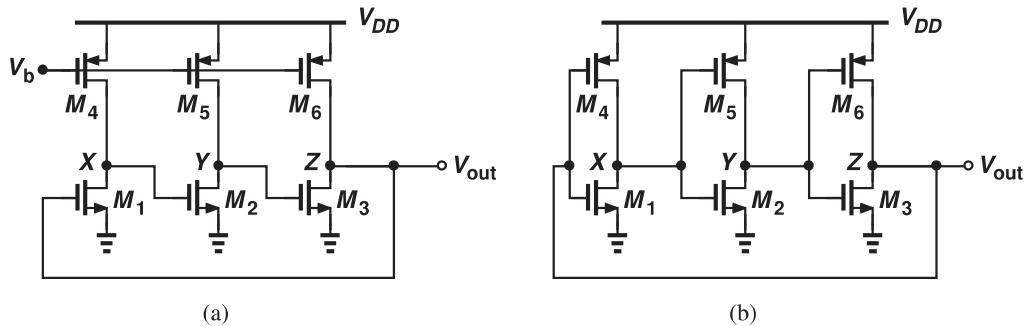


Figure 13.9 Ring oscillators using (a) CS stages with PMOS loads, (b) CMOS inverters.

each PMOS current source to an *amplifying* device by connecting its gate to the input of the corresponding stage [Fig. 13.9(b)]. Each stage is now a CMOS inverter (a basic building block in logic design), providing a voltage gain of $-(g_{mp} + g_{mn})(r_{Op}||r_{On})$ if both transistors are in saturation. This type of ring oscillator finds use in many applications. Note the transistors themselves contribute capacitance to each node, limiting the speed.

The operation of the inverter-based ring oscillator can also be studied from a different perspective. If V_X starts at zero, we have $V_Y = V_{DD}$ and $V_Z = 0$. Thus, the first stage wants to raise V_X to V_{DD} . Since each stage has some phase shift (delay), the circuit oscillates such that the three voltages toggle between 0 and V_{DD} consecutively (Fig. 13.10). First, V_X rises; after some delay, V_Y falls; after another delay, V_Z rises; finally, with some delay, V_X falls. If each inverter has a delay of T_D seconds, the overall oscillation period is equal to $6T_D$ and hence the output frequency is given by $1/(6T_D)$.

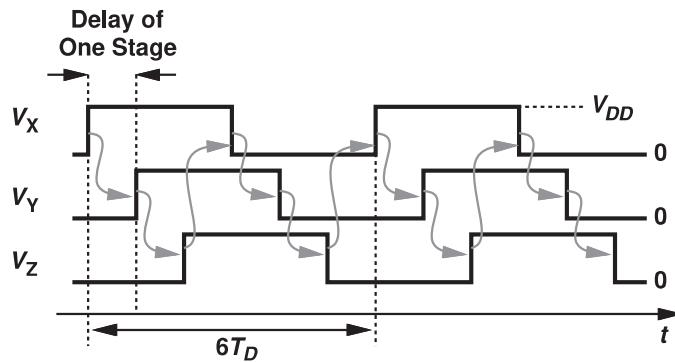


Figure 13.10 Ring oscillator waveforms.

**Example
13.3**

Can we cascade four inverters to implement a four-stage ring oscillator?

Solution No, we cannot. Consider the ring in Fig. 13.11 and suppose the circuit begins with $V_X = 0$. Thus, $V_Y = V_{DD}$, $V_Z = 0$, and $V_W = V_{DD}$. Since the first stage senses a *high input*, it happily retains its low output indefinitely. Note that all of the transistors are either off or in deep triode region (with zero drain current), yielding a zero loop gain and violating Barkhausen's first criterion. We say the circuit is "latched up." In general, a single-ended ring having an even number of inverters experiences latch-up.

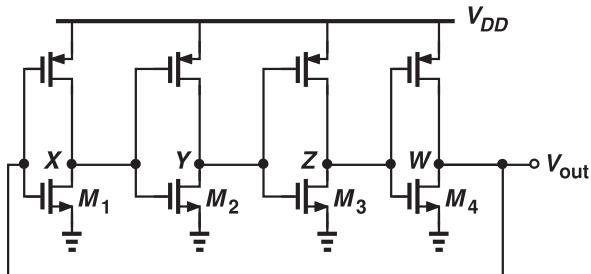


Figure 13.11

How fast can ring oscillators run? The gate delay in 40-nm CMOS technology is about 8 ps. Thus, a three-stage ring can oscillate at frequencies as high as 20 GHz. Their simplicity makes ring oscillators a popular choice in many integrated circuits. For example, memories, microprocessors, and some communication systems employ ring oscillators for on-chip clock generation.

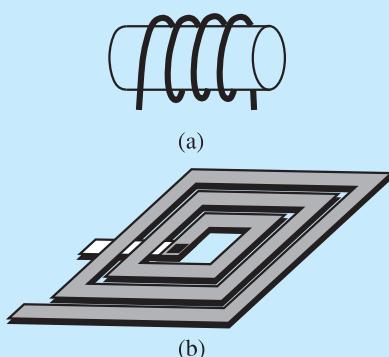
13.3

LC OSCILLATORS

Another class of oscillators employs inductors and capacitors to define the oscillation frequency. Called “LC oscillators,” these circuits can be realized in both integrated and discrete forms but with different topologies and design constraints. We begin with integrated LC oscillators.

Did you know?

A tough challenge in the design of integrated LC oscillators has been the realization of on-chip inductors. While discrete inductors can readily extend in three dimensions [Fig. (a)], integrated devices must be preferably based on a “planar” (two-dimensional) structure. Figure (b) shows a “spiral” inductor commonly employed in integrated circuits. The spiral is made of the metal layer (copper or aluminum) that is used for on-chip wiring.



(a) Simple three-dimensional inductor,
(b) integrated spiral inductor.

Why LC oscillators? Why not just ring oscillators? LC oscillators offer two advantages that have made them popular, especially in radio-frequency and wireless transceivers: they can operate faster than ring oscillators (the author has developed one that reaches 300 GHz in 65 nm CMOS technology), and they exhibit less noise (although we have not studied noise in this book). Unfortunately, LC oscillators are more difficult to design and occupy a larger chip area than ring oscillators. As our first step, let us return to some concepts from basic circuit theory.

13.3.1 Parallel LC Tanks

Shown in Fig. 13.12, an ideal parallel LC tank provides an impedance given by

$$Z_1(s) = (L_1 s) \parallel \frac{1}{C_1 s} \quad (13.7)$$

$$= \frac{L_1 s}{L_1 C_1 s^2 + 1}. \quad (13.8)$$

For a sinusoidal input current or voltage, we have $s = j\omega$ and

$$Z_1(j\omega) = \frac{j L_1 \omega}{1 - L_1 C_1 \omega^2}, \quad (13.9)$$

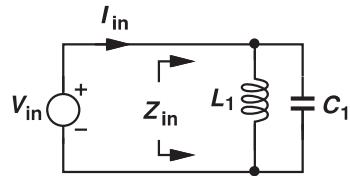


Figure 13.12 Impedance of a parallel LC tank.

observing that the impedance goes to infinity at $\omega_1 = 1/\sqrt{L_1 C_1}$. That is, even though the voltage applied to the tank, V_{in} , varies sinusoidally with time, no net current flows into the tank. How does this happen? At $\omega = \omega_1$, the inductor and the capacitor exhibit equal and opposite impedances [$jL_1\omega_1$ and $1/(jC_1\omega_1)$, respectively], canceling each other and yielding an open circuit. In other words, the current required by L_1 is exactly provided by C_1 . We say the tank “resonates” at $\omega = \omega_1$.

Example 13.4

Sketch the magnitude and phase of $Z_1(j\omega)$ as a function of frequency.

Solution We have

$$|Z_1(j\omega)| = \frac{L_1\omega}{|1 - L_1 C_1 \omega^2|}, \quad (13.10)$$

obtaining the plot in Fig. 13.13(a). As for the phase, we note from Eq. (13.9) that if $\omega < \omega_1$, then $1 - L_1 C_1 \omega^2 > 0$ and $\angle Z_1(j\omega) = \angle(jL_1\omega) = +90^\circ$ [Fig. 13.13(b)]. On the other hand, if $\omega > \omega_1$, then $1 - L_1 C_1 \omega^2 < 0$ and hence $\angle Z_1(j\omega) = \angle(jL_1\omega_1) - 180^\circ = -90^\circ$. We roughly say the tank has an inductive behavior for $\omega < \omega_1$ and a capacitive behavior for $\omega > \omega_1$.

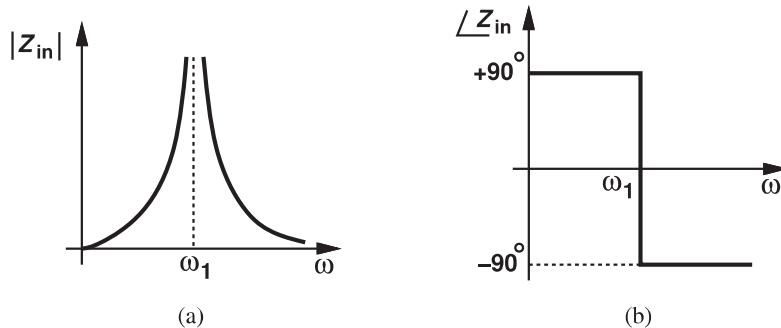


Figure 13.13

Exercise

Determine $|Z_1|$ at $\omega = \omega_1/2$ and $\omega = 2\omega_1/2$.

In practice, the impedance of a parallel LC tank does not go to infinity at the resonance frequency. To understand this point, we recognize that the wire forming the inductor has a finite *resistance*. As illustrated in Fig. 13.14(a), when L_1 carries current, its wire resistance, R_1 , heats up, dissipating energy. Thus, V_{in} must replenish this energy in every cycle, and $Z_2 < \infty$ even at resonance. The circuit is now called a “lossy tank” to emphasize the loss of energy within the inductor’s resistance.

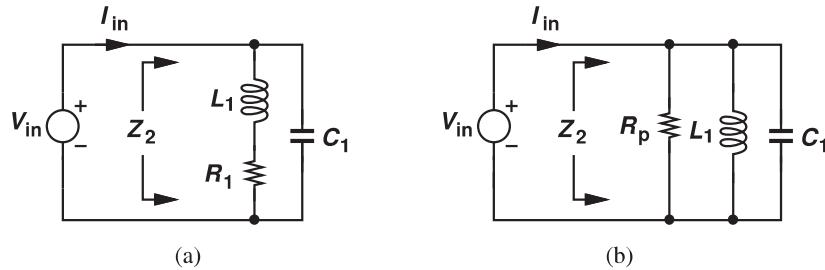


Figure 13.14 (a) Impedance of lossy tank, (b) equivalent circuit of (a).

In the analysis of LC oscillators, we prefer to model the loss of the tank by a parallel resistance, R_p [Fig. 13.14(b)]. Are the two circuits in Fig. 13.14 equivalent? They cannot be equivalent at all frequencies: at $\omega \approx 0$, L_1 is a short circuit and C_1 is open, yielding $Z_2 = R_1$ in Fig. 13.14(a) but $Z_2 = 0$ in Fig. 13.14(b). But for a narrow range around the resonance frequency, the two models can be equivalent. The proof and derivations are outlined in Problem 13.23 for the interested reader, but we present the final result here: for the two tanks to be approximately equivalent, we must have

$$R_p = \frac{L_1^2 \omega^2}{R_1}. \quad (13.11)$$

Note that an ideal inductor exhibits $R_1 = 0$ and hence $R_p = \infty$. The following example illustrates how the parallel model simplifies the analysis.

**Example
13.5**

Plot the magnitude and phase of $Z_2(s)$ in Fig. 13.14(b) as a function of frequency.

Solution We have

$$Z_2(s) = R_p || (L_1 s) || \frac{1}{C_1 s} \quad (13.12)$$

$$= \frac{R_p L_1 s}{R_p L_1 C_1 s^2 + L_1 s + R_p}. \quad (13.13)$$

At $s = j\omega$,

$$Z_2(j\omega) = \frac{j R_p L_1 \omega}{R_p (1 - L_1 C_1 \omega^2) + j L_1 \omega}. \quad (13.14)$$

At $\omega_1 = 1/\sqrt{L_1 C_1}$, we have $Z_2(j\omega_1) = R_p$, an expected result because the inductor and capacitor impedances still cancel each other. Since Z_2 reduces to a single resistance at ω_1 , $\angle Z_2(j\omega_1) = 0$. We also note that (1) at very low frequencies, $j L_1 \omega$ is very small, dominating the parallel combination, i.e., $Z_2 \approx j L_1 \omega$, and (2) at very high frequencies, $1/(j C_1 \omega)$ is very small and hence $Z_2 \approx 1/(j C_1 \omega)$. Thus, $|Z_2|$ and $\angle Z_2$ follow the general behaviors shown in Fig. 13.15.

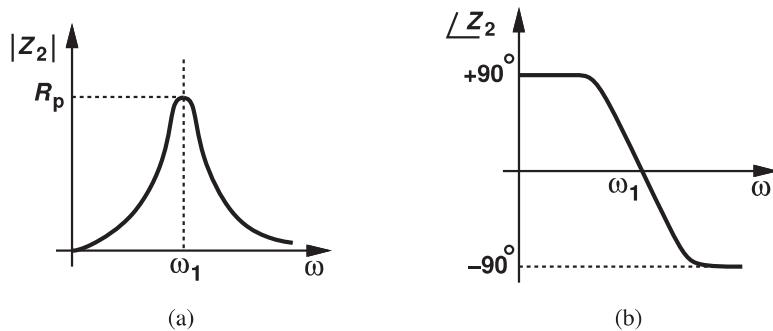


Figure 13.15 Magnitude and phase of lossy tank.

Exercise Determine $|Z_2|$ at $\omega = \omega_1/2$ and $\omega = 2\omega_1/2$.

Example 13.6

Suppose we apply an initial voltage of V_0 across the capacitor in an isolated parallel tank. Study the behavior of the circuit in the time domain if the tank is ideal or lossy.

Solution

As illustrated in Fig. 13.16(a) for the ideal tank, the capacitor begins to discharge through the inductor, i.e., the electric energy is transformed to magnetic energy. When $V_{out} = 0$, only L_1 carries energy in the form of a current. This current now continues to charge C_1 toward $-V_0$. This transfer of energy between C_1 and L_1 repeats and the tank oscillates indefinitely.

With a lossy tank [Fig. 13.16(b)], on the other hand, a nonzero output voltage causes current flow through R_p and hence dissipation of energy. Thus, the tank loses some energy in every cycle, producing a decaying oscillatory output. To construct an oscillator, we must somehow cancel this decay.

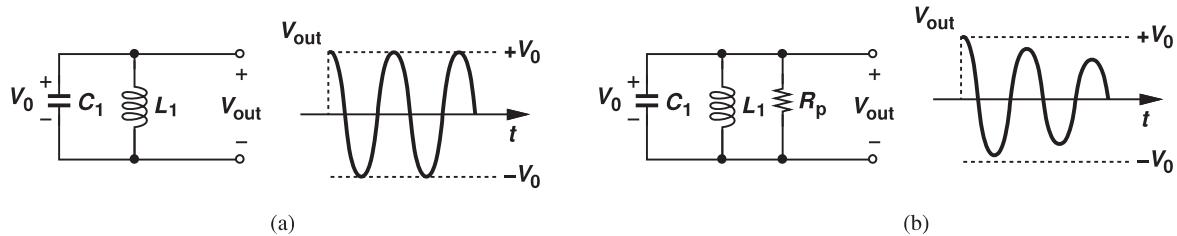


Figure 13.16 Time-domain behavior of (a) ideal, and (b) lossy tanks.

Exercise Calculate the maximum energy stored in L_1 in Fig. 13.16(a).

With our basic understanding of the parallel LC tank, we can now incorporate it in amplifying stages and oscillators.

13.3.2 Cross-Coupled Oscillator

In our study of CMOS amplifiers, we have considered common-source stages with resistor or current-source loads. Now, let us construct a common-source stage using a parallel LC tank as its load [Fig. 13.17(a)]. We wish to analyze the frequency response of this “tuned” amplifier. Denoting the tank impedance by Z_2 and neglecting channel-length modulation,⁴ we have

$$\frac{V_{out}}{V_{in}} = -g_m Z_2(s), \quad (13.15)$$

where $Z_2(s)$ is given by Eq. (13.13). Using the plots of $|Z_2|$ and $\angle Z_2$ in Fig. 13.15, we can sketch $|V_{out}/V_{in}|$ and $\angle(V_{out}/V_{in})$ as shown in Fig. 13.17(b). Note $\angle(V_{out}/V_{in})$ is obtained by shifting $\angle Z_2$ by 180° (up or down) to account for the negative sign in $-g_m Z_2(s)$. The CS stage thus exhibits a gain that reaches a maximum of $g_m R_p$ at resonance and approaches zero at very low or very high frequencies. The phase shift at ω_1 is equal to 180° because the load reduces to a resistor at resonance.

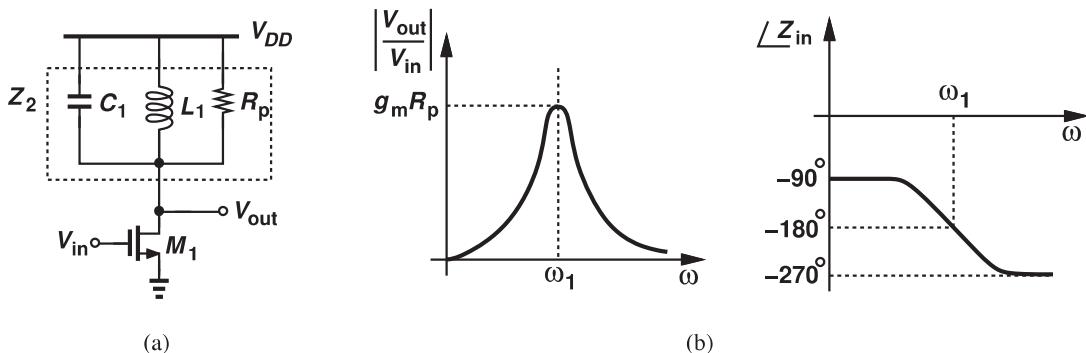


Figure 13.17 (a) CS stage with a tank load, (b) magnitude and phase plots of the stage.

Does the CS stage of Fig. 13.17(a) oscillate if we tie its output to its input? As illustrated in Fig. 13.3(b), the total phase shift around the loop must reach 360° at a finite frequency, but Fig. 13.17(b) reveals that this is not possible. We therefore insert one more CS stage in the loop and try again [Fig. 13.18(a)]. For a total phase shift of 360° , each stage must provide 180° , which is possible at $\omega = \omega_1$ in Fig. 13.17(b). Thus, the circuit oscillates at ω_1 if the loop gain at this frequency is sufficient. Since each stage has a voltage gain of $g_m R_p$ at ω_1 , Barkhausen’s loop gain criterion translates to

$$(g_m R_p)^2 \geq 1. \quad (13.16)$$

Stated more accurately, the startup condition emerges as $g_m(R_p || r_O) \geq 1$. With identical stages, the oscillator of Fig. 13.18 generates differential signals at nodes X and Y [Fig. 13.18(b)] (why?), a useful property for integrated-circuit applications.

A critical issue in the above topology is that the bias current of the transistors is poorly defined. Since no current mirror or other means of proper biasing are used, the drain currents of M_1 and M_2 vary with process, supply voltage, and temperature. For example, if the transistors’ threshold voltage is lower than the nominal value, then the peak value of

⁴The output resistance of M_1 can be simply absorbed in R_p .

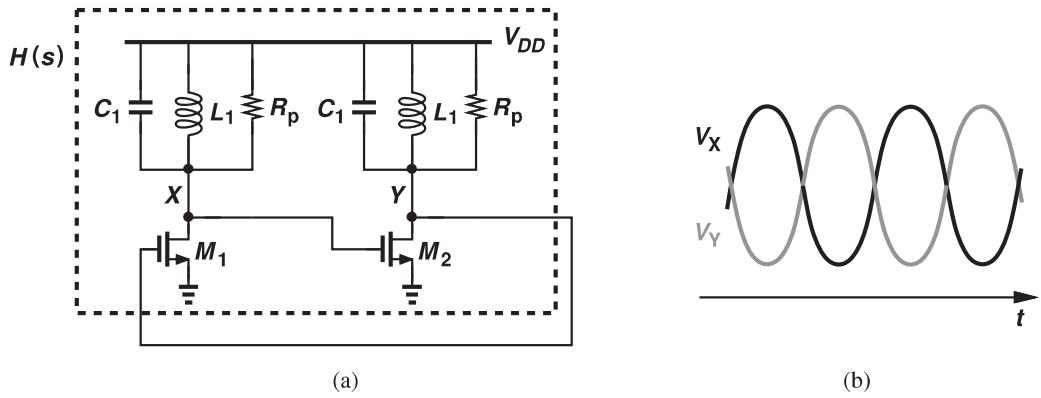


Figure 13.18 (a) Two LC-load CS stages in a loop, (b) oscillation waveforms.

V_X yields a greater overdrive voltage for M_2 and hence a larger drain current. To resolve this issue, we first note that the gate of each device is tied to the drain of the other and redraw the circuit as shown in Fig. 13.19(a). Now, M_1 and M_2 almost resemble a differential pair whose output is fed back to its input. Let us then add a tail current source as illustrated in Fig. 13.19(b), ensuring that the total bias current of M_1 and M_2 is equal to I_{SS} . We usually redraw this circuit as shown in Fig. 13.19(c).

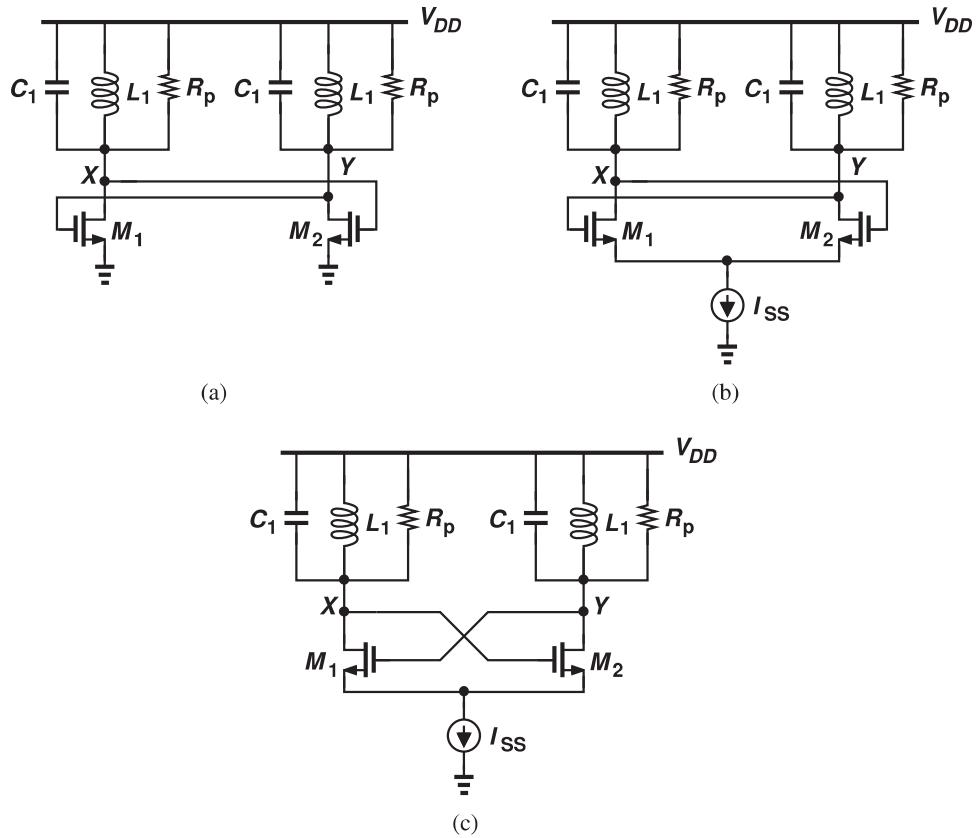


Figure 13.19 Different drawings of the cross-coupled oscillator.

The “cross-coupled” oscillator of Fig. 13.19(c) is the most popular and robust LC oscillator used in integrated circuits. The carrier frequency in your cell phone and in its GPS receiver is very likely generated by such a topology.

Example 13.7

Plot the drain currents of M_1 and M_2 in Fig. 13.19(c) if the voltage swings at X and Y are large.

Solution

Let us first consider the differential pair in Fig. 13.20(a). With large input voltage swings, the entire current is steered to the left or to the right [Fig. 13.20(b)]. The circuit of Fig. 13.19(b), too, exhibits the same behavior, producing drain currents that swing between zero and I_{SS} [Fig. 13.20(c)].

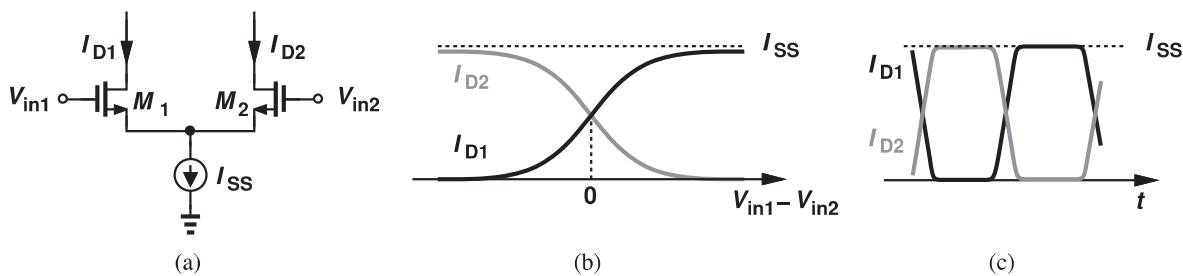


Figure 13.20

Exercise Redraw the cross-coupled oscillator with PMOS transistors.

Our study of ring and cross-coupled oscillators points to a general procedure for the analysis of oscillators: open the feedback loop (while including the effect of I/O impedances as in Chapter 12), determine the transfer function around the loop (similar to the loop gain), and equate the phase of this result to 360° and its magnitude to unity. In the next section, we apply this procedure to the Colpitts oscillator.

13.3.3 Colpitts Oscillator

The Colpitts topology employs only one transistor and finds wide application in discrete design. This is because (high-frequency) discrete transistors are more expensive than passive discrete devices. (In integrated circuits, on the other hand, transistors are the least expensive because they occupy the smallest area.) Since bipolar transistors are much more common in discrete design than are MOSFETs, we analyze a bipolar Colpitts oscillator here.

How can we construct an oscillator using only one transistor? We observed in Figs. 13.6(a) and 13.17(a) that a common-source (or common-emitter) stage cannot serve this purpose. But how about a common-gate (or common-base) stage? Depicted in Fig. 13.21(a), the Colpitts oscillator resembles a common-base topology whose output (the collector voltage) is fed back to its input (the emitter node). Current source I_1 defines the bias current of Q_1 , and V_b ensures Q_1 is in the forward active region. As with the cross-coupled oscillator, resistor R_p models the loss of the inductor. This resistor can also

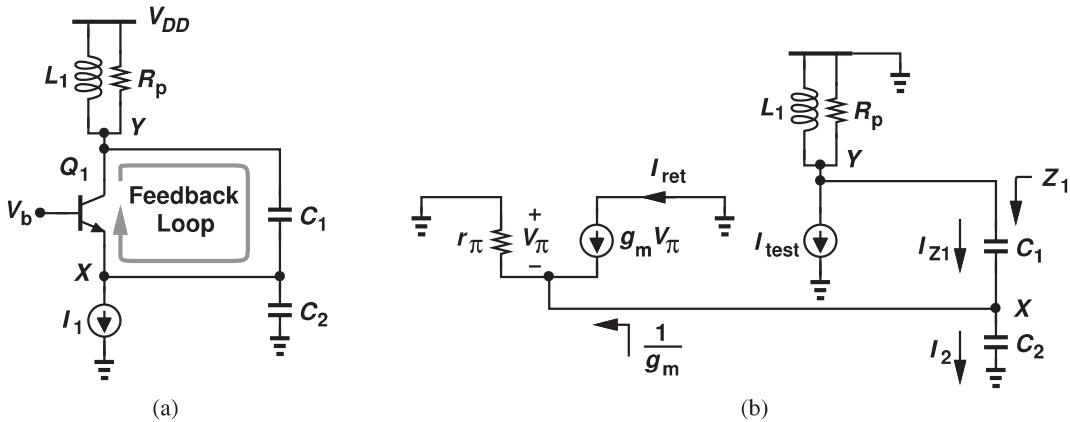


Figure 13.21 (a) Colpitts oscillator, (b) open-loop equivalent of (a).

model the input resistance of the subsequent stage, e.g., r_π if the oscillator drives a simple common-emitter stage.

In order to analyze the Colpitts oscillator, we wish to break the feedback loop. Neglecting the Early effect, we note that Q_1 in Fig. 13.21(a) operates as an ideal voltage-dependent current source, injecting its small-signal current into node Y . We therefore break the loop at the collector as shown in Fig. 13.21(b), where an independent current source I_{test} is drawn from Y , and the current returned by the transistor, I_{ret} , is measured as the quantity of interest. The transfer function I_{ret}/I_{test} must exhibit a phase of 360° and a magnitude of at least unity at the frequency of oscillation.

We observe that I_{test} is divided between $(L_1 s) \parallel R_p = L_1 s R_p / (L_1 s + R_p)$ and Z_1 , which is given by

$$Z_1 = \frac{1}{C_1 s} + \frac{1}{g_m} \parallel \frac{1}{C_2 s} \quad (13.17)$$

$$= \frac{1}{C_1 s} + \frac{1}{C_2 s + g_m}. \quad (13.18)$$

That is, the current flowing through C_1 is equal to

$$I_{Z1} = -I_{test} \frac{\frac{L_1 s R_p}{L_1 s + R_p}}{\frac{L_1 s R_p}{L_1 s + R_p} + \frac{1}{C_1 s} + \frac{1}{C_2 s + g_m}}. \quad (13.19)$$

This current is now multiplied by the parallel combination of $1/(C_2 s)$ and $1/g_m$ to yield V_X . Since $I_{ret} = g_m V_\pi = -g_m V_X$, we have

$$\frac{I_{ret}}{I_{test}}(s) = \frac{g_m R_p L_1 C_1 s^2}{L_1 C_1 C_2 R_p s^3 + [g_m R_p L_1 C_1 + L_1(C_1 + C_2)]s^2 + [g_m L_1 + R_p(C_1 + C_2)]s + g_m R_p}. \quad (13.20)$$

We now equate this transfer function to unity (which is equivalent to setting its phase to 360° and its magnitude to 1) and cross-multiply, obtaining:

$$L_1 C_1 C_2 R_p s^3 + L_1(C_1 + C_2)s^2 + [g_m L_1 + R_p(C_1 + C_2)]s + g_m R_p = 0. \quad (13.21)$$

At the oscillation frequency, $s = j\omega_1$, both the real and imaginary parts of the right-hand side must drop to zero:

$$-L_1(C_1 + C_2)\omega_1^2 + g_m R_p = 0 \quad (13.22)$$

$$-L_1C_1C_2R_p\omega_1^3 + [g_m L_1 + R_p(C_1 + C_2)]\omega_1 = 0. \quad (13.23)$$

From the second equation, we obtain the oscillation frequency:

$$\omega_1^2 = \frac{(C_1 + C_2)}{L_1C_2C_2} + \frac{g_m}{R_pC_1C_2}. \quad (13.24)$$

The second term on the right is typically negligible, yielding

$$\omega_1^2 \approx \frac{1}{L_1 \frac{C_1C_2}{C_1 + C_2}}. \quad (13.25)$$

That is, the oscillation occurs at the resonance of L_1 and the series combination of C_1 and C_2 . Using this result in Eq. (13.23) gives the startup condition:

$$g_m R_p = \frac{(C_1 + C_2)^2}{C_1C_2}. \quad (13.26)$$

The transistor must thus provide sufficient transconductance to satisfy or exceed this requirement. Since the right-hand side is minimum if $C_1 = C_2$, we conclude that $g_m R_p$ must be at least equal to 4.

**Example
13.8**

Compare the startup conditions of cross-coupled and Colpitts oscillators.

Solution

We note from Eq. (13.16) that the cross-coupled topology requires a minimum $g_m R_p$ of 1, i.e., it can tolerate a lossier inductor than the Colpitts oscillator can. (Also, note that the Colpitts topology provides only a single-ended output.)

Exercise

How much is the dc voltage at node Y in Fig. 13.21(a)? Can you sketch the oscillation waveform at this node?

Where is the output node in the oscillator of Fig. 13.21(a)? The output can be sensed at node Y , in which case the input resistance of the next stage (e.g., r_π) shunts R_p , requiring a greater g_m to satisfy the startup condition. Alternatively, the output can be sensed at the emitter (Fig. 13.22). This is usually preferable in discrete design because (1) discrete inductors have a low loss (a high equivalent R_p) and are therefore sensitive to resistive loading, and (2) with only R_{in} loading the emitter (and $R_p \rightarrow \infty$), the startup condition is modified to:

$$g_m R_{in} = 1 \quad (13.27)$$

Derived in Problem 13.37, this more relaxed condition simplifies the design of the oscillator. For example, the oscillator can drive a lower load resistance in this case than when the load is tied to the collector. It is important to note that most textbooks derive Eq. (13.27) as the startup condition, which holds only if R_p is very large (the inductor has a low loss).

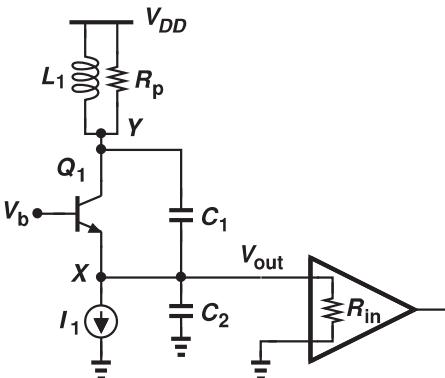


Figure 13.22 Colpitts oscillator driving next stage at its emitter.

13.4

PHASE SHIFT OSCILLATOR

In our development of ring oscillators in Section 13.2, we created sufficient phase shift by cascading three *active* stages. Alternatively, we can cascade passive sections along with a single amplifier to achieve the same goal. Shown in Fig. 13.23(a) is a “phase shift oscillator” based on this principle. We expect that the three RC sections can provide a phase shift of 180° at the frequency of interest even if the amplifier itself contributes negligible phase. Nonetheless, the signal attenuation introduced by the passive stages must be compensated by the amplifier to fulfill the startup condition.⁵

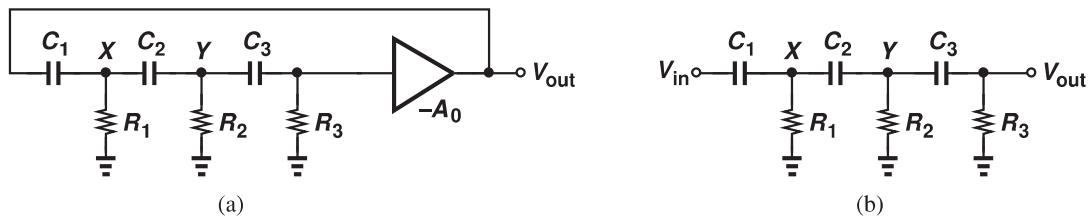


Figure 13.23 (a) Phase shift oscillator, (b) phase shift network.

Let us first compute the transfer function of the passive network shown in Fig. 13.23(b), assuming that $C_1 = C_2 = C_3 = C$ and $R_1 = R_2 = R_3 = R$. Beginning from the output, we write the current through R_3 as V_{out}/R and hence

$$V_Y = \frac{V_{out}}{R} \frac{1}{Cs} + V_{out}. \quad (13.28)$$

Dividing V_Y by R_2 and multiplying it by $1/(C_2 s)$, we have the voltage drop across C_2 and thus

$$V_X = \frac{V_Y}{R_2} \frac{1}{Cs} + V_Y \quad (13.29)$$

$$= \left(\frac{1}{RCs} + 1 \right)^2 V_{out}. \quad (13.30)$$

⁵Note that the bottom terminal of R_S must in fact be tied to a bias voltage that is proper for the amplifier.

Finally,

$$V_{in} = \left(\frac{1}{RCs} + 1 \right)^3 V_{out} \quad (13.31)$$

and hence

$$\frac{V_{out}}{V_{in}} = \frac{(RCs)^3}{(RCs + 1)^3}. \quad (13.32)$$

At $s = j\omega_1$,

$$\angle \frac{V_{out}}{V_{in}} = 3 \times 90^\circ - 3\tan^{-1}(RC\omega_1). \quad (13.33)$$

For oscillation to occur at ω_1 , this phase must reach 180° :

$$\tan^{-1}(RC\omega_1) = 30^\circ. \quad (13.34)$$

It follows that

$$\omega_1 = \frac{1}{\sqrt{3}RC}. \quad (13.35)$$

For the startup condition to hold, we multiply the magnitude of Eq. (13.32) by the gain of the amplifier and equate the result to unity:

$$\frac{ARC\omega_1}{\sqrt{R^2C^2\omega_1^2 + 1}} = 1. \quad (13.36)$$

That is, the gain of the amplifier must be at least:

$$A = 2. \quad (13.37)$$

The phase shift oscillator is occasionally used in discrete design as it requires only one amplifying stage. This topology does not find wide application in integrated circuits because its output noise is quite high.

Example 13.9

Design the phase shift oscillator using an op amp.

Solution

We must configure the op amp as an *inverting* amplifier. Figure 13.24(a) shows an example. Here, however, resistor R_4 appears between node Z and a virtual ground, equivalently shunting resistor R_3 . Thus, for our foregoing derivations to apply, we must choose $R_3||R_4 = R_2 = R_1 = R$. In fact, we may simply allow R_3 to be infinity and R_4 to be equal to R , arriving at the topology depicted in Fig. 13.24(b).

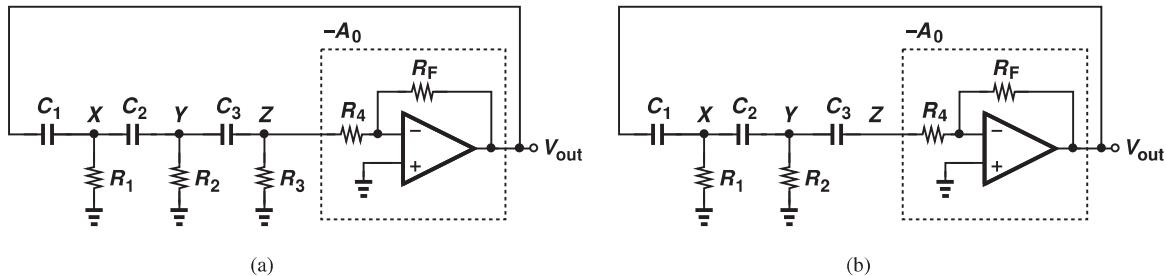


Figure 13.24

Exercise How should R_F/R_4 be chosen to obtain a loop gain of 1 at the frequency of oscillation?

What determines the oscillation amplitude in the circuit of Fig. 13.24(b)? If the loop gain at ω_1 is greater than unity, the amplitude grows until the op amp output swings from one supply rail to the other. Owing to the saturation of the op amp, the output waveform resembles a square wave rather than a sinusoid, an undesirable effect in some applications. Moreover, the saturation tends to slow down the op amp response, limiting the maximum oscillation frequency. For these reasons, one may opt to define (“stabilize”) the oscillation amplitude by additional means. For example, as illustrated in Fig. 13.25(a), we can replace the feedback resistor with two “anti-parallel” diodes. The output now swings by one diode drop ($V_{D,on} = 700$ to 800 mV) below and above its average value.

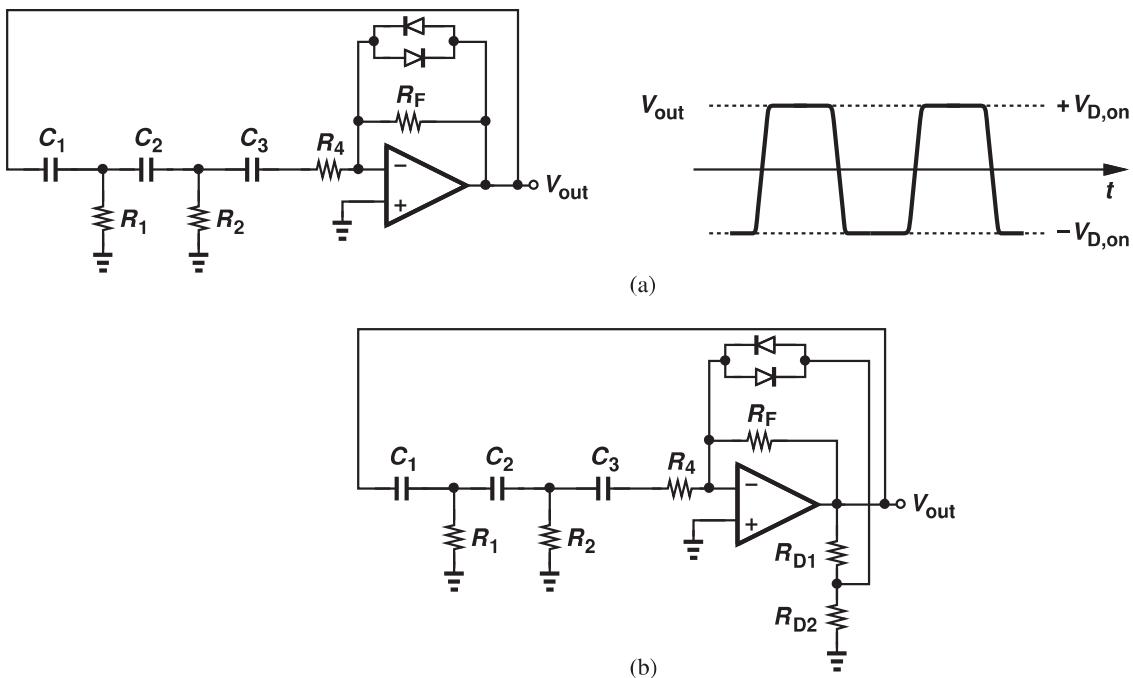


Figure 13.25 (a) Use of diodes to limit the output swing, (b) alternative topology providing larger output swing.

The oscillation amplitude obtained above may prove inadequate in many applications. We must therefore modify the feedback network such that the diodes turn on only when V_{out} reaches a larger, predetermined value. To this end, we divide V_{out} down and feed the result to the diodes [Fig. 13.25(b)]. Assuming a constant-voltage model for D_1 and D_2 , we observe that one diode turns on when

$$V_{out} \frac{R_{D2}}{R_{D2} + R_{D1}} = V_{D,on}, \quad (13.38)$$

and hence

$$V_{out} = \left(1 + \frac{R_{D1}}{R_{D2}}\right) V_{D,on}. \quad (13.39)$$

13.5 WIEN-BRIDGE OSCILLATOR

The Wien-bridge oscillator is another topology sometimes used in discrete design as it requires only one amplifying stage. Unlike the phase shift oscillator, however, the Wien-bridge configuration employs a passive feedback network with *zero* phase shift rather than 180° phase shift. The amplifier must therefore provide a *positive* gain so that the total phase shift at the frequency of oscillation is equal to zero (or 360°).

Did you know?

In 1939, two young Stanford graduates named William Hewlett and David Packard used the Wien-bridge oscillator to design a sound generator for the soundtrack of the Disney movie *Fantasia*. History has it that Hewlett and Packard borrowed \$500 from their advisor, Fredrick Terman, to construct and sell eight of these generators to Disney. Thus began the company known today as HP. For the first several decades, HP designed and manufactured only test equipment, e.g., oscilloscopes, signal generators, power supplies, etc.

Let us first construct a simple passive network with zero phase shift at a *single* frequency. Shown in Fig. 13.26(a) is an example. If $R_1 = R_2 = R$ and $C_1 = C_2 = C$, we have

$$\frac{V_{out}}{V_{in}}(s) = \frac{\frac{R}{RCs + 1}}{\frac{R}{RCs + 1} + \frac{1}{Cs} + R} \quad (13.40)$$

$$= \frac{RCs}{R^2C^2s^2 + 3RCs + 1}. \quad (13.41)$$

The phase thus emerges as

$$\angle \frac{V_{out}}{V_{in}}(s = j\omega) = \frac{\pi}{2} - \tan^{-1} \frac{3RC\omega}{1 - R^2C^2\omega^2}, \quad (13.42)$$

falling to zero at

$$\omega_1 = \frac{1}{RC}. \quad (13.43)$$

We now place this network around an op amp as illustrated in Fig. 13.26(b). Denoting the gain of the non-inverting amplifier by A , we multiply the magnitude of Eq. (13.41) by A and equate the result to unity:

$$\left| \frac{ARCj\omega}{1 - R^2C^2\omega^2 + 3jRC\omega} \right| = 1. \quad (13.44)$$

At ω_1 , this equation yields

$$A = 3. \quad (13.45)$$

That is, we choose $R_{F1} \geq 2R_{F2}$.

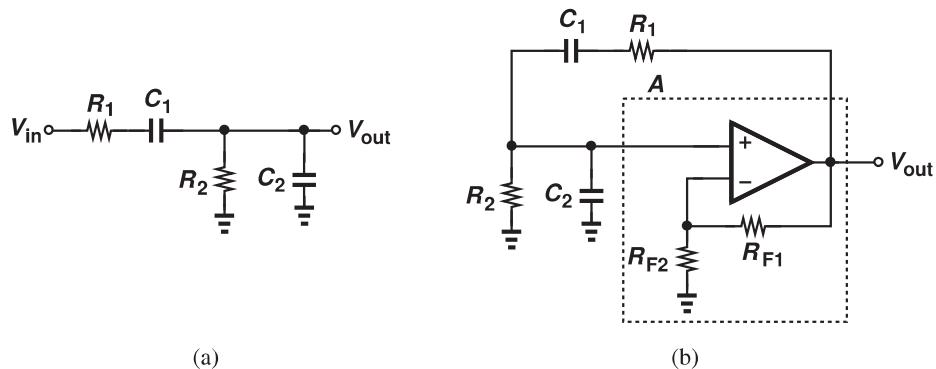


Figure 13.26 (a) Phase shift network, (b) Wien-bridge oscillator.

To avoid uncontrolled amplitude growth, the Wien-bridge oscillator can incorporate diodes in the gain definition network, R_{F1} and R_{F2} . As depicted in Fig. 13.27, two anti-parallel diodes can be inserted in series with R_{F1} so as to create strong feedback as $|V_{out}|$ exceeds $V_{D.on}$. If larger amplitudes are desired, resistor R_{F3} can be added to divide V_{out} and apply the result to the diodes.

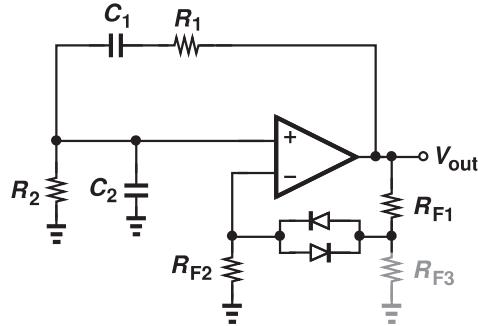


Figure 13.27 Addition of diodes to limit output swing of Wien-bridge oscillator.

13.6

CRYSTAL OSCILLATORS

The oscillators studied thus far do not offer a precise output frequency. For example, as the temperature varies, so does the value of the capacitances in each circuit, creating a drift in the oscillation frequency. Many applications, on the other hand, demand a precise clock frequency. If the oscillator frequency in your watch departs from 2^{15} Hz by 0.1%, the time reading will be 10 minutes off after one week.

For high-precision applications, we employ “crystal oscillators.” A crystal is made of a piezoelectric material such as quartz and it mechanically vibrates at a certain frequency if subjected to a voltage difference. Crystals are attractive as a frequency “reference” for three reasons. (1) Given by the physical dimensions of the crystal, the vibration frequency is extremely stable with temperature, varying by only a few parts per million (ppm) for a 1° change, (2) the crystal can be cut with relative ease in the factory so as to produce a precise vibration frequency, e.g., with an error of 10–20 ppm.⁶ (3) Crystals exhibit a very low loss, behaving almost like an ideal LC tank. That is, an electric impulse applied to the crystal makes it vibrate for thousands of cycles before the oscillation decays.

Our treatment of crystal oscillators in this section proceeds as follows. First, we derive a circuit model for the crystal, concluding that it behaves as a lossy LC tank. Next, we develop an active circuit that provides a *negative* resistance. Finally, we attach the crystal to such a circuit so as to form an oscillator.

13.6.1 Crystal Model

For circuit design, we need an electrical model of the crystal. Figure 13.28(a) shows the circuit symbol and the typical impedance characteristic of a crystal. The impedance falls to nearly zero at ω_1 and rises to a very *high* value at ω_2 . Let us construct an RLC circuit model to represent this behavior. Since the impedance is close to zero at ω_1 , we envision a *series* resonance at this frequency [Fig. 13.28(b)]: if $jL_1\omega + 1/(jC_1\omega) = 0$ at $\omega = \omega_1$, then

⁶Crystals with an error of a few ppm are also available but at a higher cost.

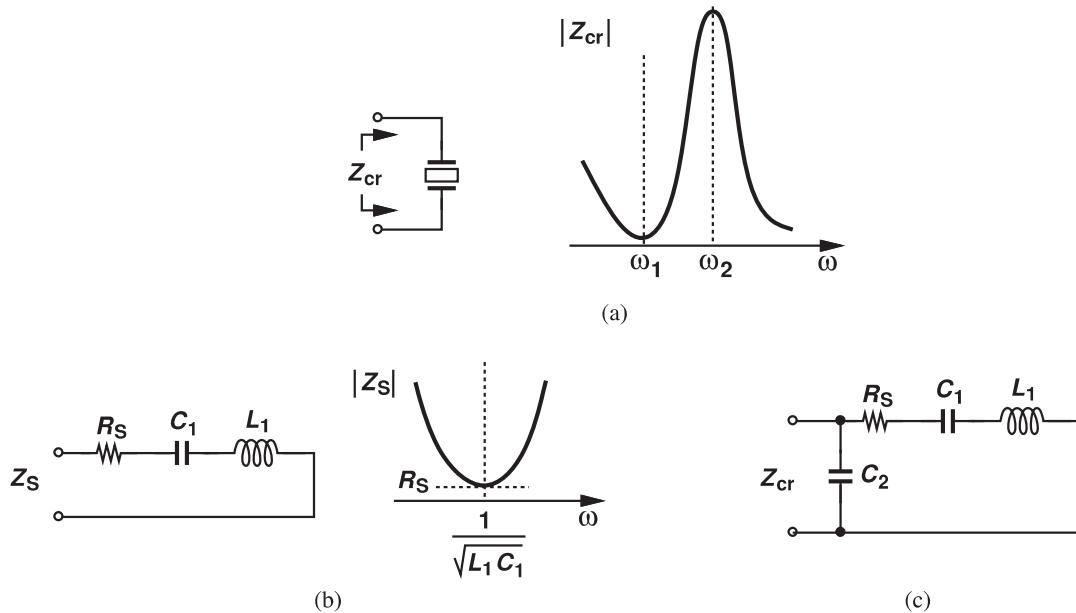


Figure 13.28 (a) Symbol and impedance of a crystal, (b) circuit model for series resonance, (c) complete model.

the impedance reduces to R_S , which is usually a small resistance. That is, Z_S can model the crystal in the vicinity of ω_1 .

Around ω_2 , the device experiences *parallel* resonance—as seen earlier in LC oscillators. We can therefore place a capacitance in parallel with Z_S as shown in Fig. 13.28(c). To determine ω_2 in terms of the circuit parameters, we neglect R_S and write

$$Z_{cr}(j\omega) = Z_S(j\omega) \parallel \frac{1}{jC_2\omega} \quad (13.46)$$

$$\approx \frac{1 - L_1 C_1 \omega^2}{j\omega(C_1 + C_2 - L_1 C_1 C_2 \omega^2)}. \quad (13.47)$$

We note that Z_{cr} goes to infinity at

$$\omega_2 = \frac{1}{\sqrt{L_1 \frac{C_1 C_2}{C_1 + C_2}}}. \quad (13.48)$$

In practice, ω_1 and ω_2 are very close, i.e.,

$$\frac{1}{\sqrt{L_1 C_1}} \approx \frac{1}{\sqrt{L_1 \frac{C_1 C_2}{C_1 + C_2}}} \quad (13.49)$$

and hence

$$C_1 \approx \frac{C_1 C_2}{C_1 + C_2}. \quad (13.50)$$

It follows that

$$C_2 \gg C_1. \quad (13.51)$$

**Example
13.10**

If $C_2 \gg C_1$, find a relation between the series and parallel resonance frequencies.

Solution We have

$$\frac{\omega_2}{\omega_1} = \sqrt{\frac{C_1 + C_2}{C_2}} \quad (13.52)$$

$$\approx 1 + \frac{C_1}{2C_2}. \quad (13.53)$$

Exercise Derive an expression for ω_2/ω_1 if R_S is not neglected.

13.6.2 Negative-Resistance Circuit

In order to arrive at a popular crystal oscillator topology, we must first devise a circuit that provides a *negative* (small-signal) input resistance. Consider the topology shown in Fig. 13.29(a), where the bias network of M_1 is omitted for simplicity. Let us obtain Z_{in} with the aid of the arrangement in Fig. 13.29(b), neglecting channel-length modulation and other capacitances. Upon flowing through C_A , I_X generates a gate-source voltage for M_1 . Thus, the drain current is given by

$$I_1 = -\frac{I_X}{C_{AS}} g_m. \quad (13.54)$$

Since C_B carries a current equal to $I_X - I_1$, it sustains a voltage equal to $(I_X - I_1)/C_{BS} = [I_X + g_m I_X / (C_{AS})] / (C_{BS})$. Writing a KVL around C_A , V_X and C_B , we eventually obtain

$$V_X = \frac{I_X}{C_{AS}} + \frac{I_X}{C_{BS}} + \frac{g_m I_X}{C_A C_{BS} s^2}. \quad (13.55)$$

That is,

$$Z_{in}(s) = \frac{1}{C_{AS}} + \frac{1}{C_{BS}} + \frac{g_m}{C_A C_{BS} s^2}. \quad (13.56)$$

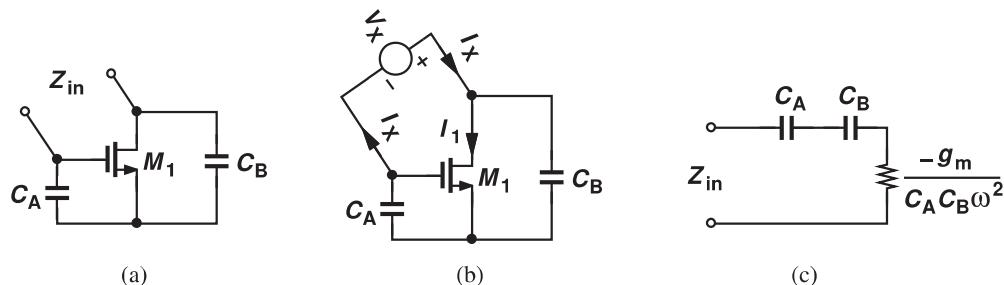


Figure 13.29 (a) Circuit providing negative resistance, (b) setup for impedance measurement, (c) equivalent impedance.

For a sinusoidal input, $s = j\omega$, and

$$Z_{in}(j\omega) = \frac{1}{jC_A\omega} + \frac{1}{jC_B\omega} - \frac{g_m}{C_A C_B \omega^2}. \quad (13.57)$$

What do the three terms in this equation signify? The first two represent two capacitors in series. The third, on the other hand, is *real*, i.e., a resistance, and *negative* [Fig. 13.29(c)]. A small-signal negative resistance simply means that if the voltage across the device increases, the current through it *decreases*.

A negative resistance can help sustain oscillation. To understand this point, consider a lossy parallel LC tank [Fig. 13.30(a)]. As explained previously, an initial condition on the capacitor leads to a decaying oscillation because R_p dissipates energy in every cycle. Let us now place a negative resistance in parallel with R_p [Fig. 13.30(b)]. We choose $|-R_1| = R_p$, obtaining $(-R_1) \parallel R_p = \infty$. Since R_1 and R_p cancel, the tank consisting of L_1 and C_1 sees no net loss, as if the tank were *lossless*. In other words, since the energy lost by R_p in every cycle is replenished by the active circuit, the oscillation continues indefinitely.

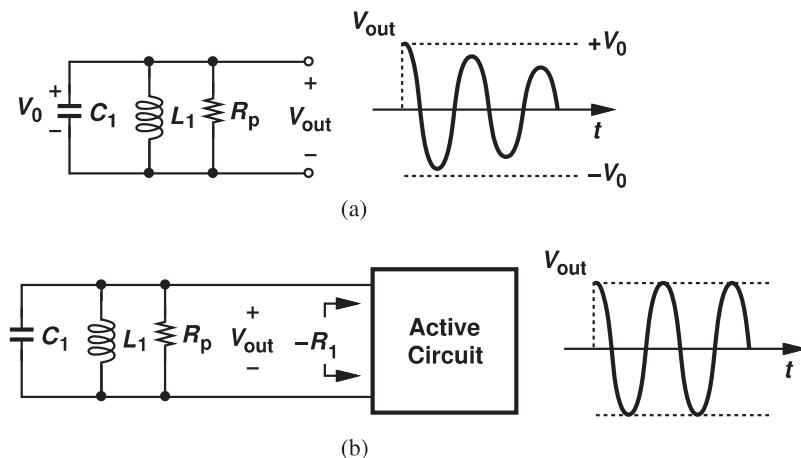


Figure 13.30 (a) Time response of a lossy LC tank, (b) use of a negative resistance to cancel the loss of the tank.

Did you know?

Crystal oscillators provide a very precise and stable output frequency. But what if we need a variable frequency? For example, the microprocessor in your laptop runs at a high clock frequency if heavy computation is necessary but switches to a low clock frequency to save power if there is little computation demand. How can such a clock be generated? This task is accomplished using a “phase-locked loop,” a circuit that multiplies the crystal frequency by a programmable factor. For example, with a crystal frequency of 10 MHz and a multiplication factor ranging from 10 to 300, the microprocessor can run at a clock frequency of 100 MHz to 3 GHz.

What happens if $|-R_1| < R_p$? Then, $(-R_1) \parallel R_p$ is still negative, allowing the oscillation amplitude to grow until nonlinear mechanisms in the active circuit limit the amplitude (Section 13.1).

13.6.3 Crystal Oscillator Implementation

We now attach a crystal to a negative resistance to form an oscillator [Fig. 13.31(a)]. Replacing the crystal with its electrical model and the negative-resistance circuit with its equivalent network, we arrive at Fig. 13.31(b). Of course, to benefit from the precise resonance frequency of the crystal, we must choose C_A and C_B so as to *minimize* their effect on the oscillation frequency. As evident from Fig. 13.31(b), this occurs if $C_A C_B / (C_A + C_B)$ is much *smaller* than the crystal impedance, Z_{cr} . However, if C_A and C_B are excessively large, then the

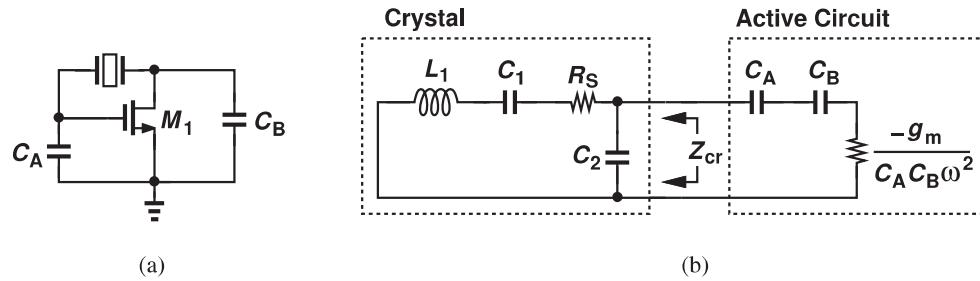


Figure 13.31 (a) Use of negative resistance to cancel loss of crystal, (b) equivalent circuit.

negative resistance, $-g_m/(C_A C_B \omega^2)$, is not “strong” enough to cancel the crystal loss. In typical designs, C_A and C_B are chosen 10 to 20 times smaller than C_2 .

The analysis of the basic crystal oscillator in Fig. 13.31 is somewhat beyond the scope of this book and is outlined in Problem 13.51 for the interested reader. It can be shown that the circuit oscillates at the crystal’s parallel resonance frequency if

$$L_1 C_1 \omega^2 - 1 \leq g_m R_S \frac{C_1 C_2}{C_A C_B}. \quad (13.58)$$

The crystal data sheet specifies L_1 , C_1 , C_2 , and R_S . The designer must choose C_A , C_B , and g_m properly.

We must now add bias elements to the circuit. Unlike parallel LC tanks, a crystal does not provide a path for the bias current or voltage. (Recall the series capacitance, C_1 , in the crystal model.) For example, the stages in Fig. 13.32(a) do not operate properly because the drain bias current of M_A is zero and the gate bias voltage of M_B is not defined. We

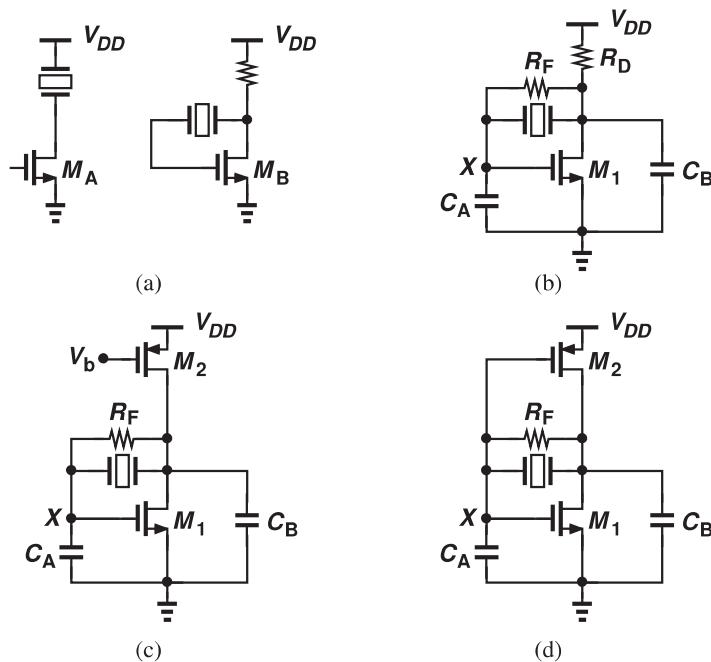


Figure 13.32 (a) Stages with no dc bias path, (b) simple biasing of a crystal oscillator, (c) biasing using a PMOS current source, (d) inverter-based crystal oscillator.

can add a feedback resistor as shown in Fig. 13.32(b) to realize a self-biased stage. Note that R_F must be very large (tens of kilohms) to contribute negligible loss. We can replace R_D with a current source [Fig. 13.32(c)]. Now the current source can be transformed to an *amplifying* device if its gate is tied to node X [Fig. 13.32(d)].

The circuit of Fig. 13.32(d) merits several remarks. First, both transistors are biased in saturation before oscillation begins (why?). Second, for small-signal operation, M_1 and M_2 appear in parallel, providing a total transconductance of $g_{m1} + g_{m2}$. Third, M_1 and M_2 can be viewed as a CMOS inverter (Chapter 16) that is biased at its trip point. This oscillator topology is popular in integrated circuits, with the inverter placed on the chip and the crystal off the chip.

The circuit of Fig. 13.32(d) may exhibit a tendency to oscillate at higher harmonics of the crystal's parallel resonance frequency. For example, if this resonance frequency is 20 MHz, the circuit may oscillate at 40 MHz. To avoid this issue, a low-pass filter must be inserted in the feedback loop so as to suppress the gain at higher frequencies. As illustrated in Fig. 13.33, we place resistor R_1 in series with the feedback network. The pole frequency, $1/(2\pi R_1 C_B)$, is typically chosen slightly above the oscillation frequency.

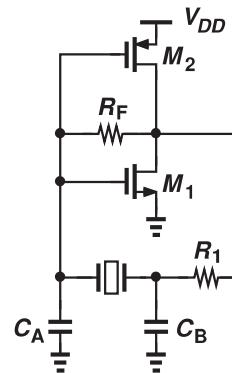


Figure 13.33 Complete crystal oscillator including low-pass filter to avoid higher modes.

In discrete circuit design, a high-speed CMOS inverter may not be available. An alternative topology using a single bipolar transistor can be derived from the circuit of Fig. 13.31(a) as shown in Fig. 13.34(a). To bias the transistor, we add a large resistor from the collector to the base and an inductor from the collector to V_{CC} [Fig. 13.34(b)]. We wish L_1 to provide the bias current of Q_1 but not affect the oscillation frequency. Thus, we choose L_1 large enough that $L_1\omega$ is a high impedance (approximately an open circuit).

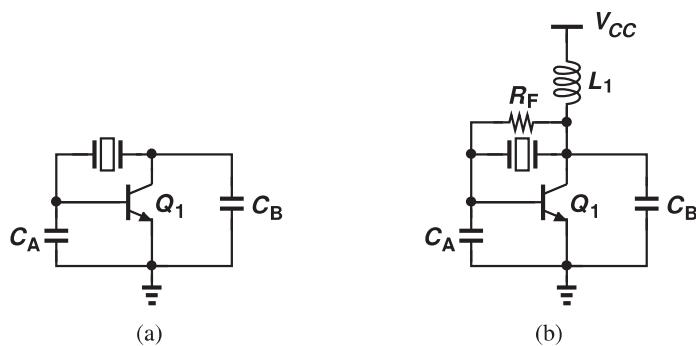


Figure 13.34 Crystal oscillator using a bipolar device.

An inductor playing such a role is called a “radio-frequency choke” (RFC). Note that this circuit reduces to that in Fig. 13.34(a) if R_F and L_1 are large.

13.7

CHAPTER SUMMARY

- An oscillator can be viewed as a negative-feedback system with so much phase shift (delay) in the loop that the feedback becomes positive at the oscillation frequency.
- The magnitude of the loop gain must exceed unity at the oscillation frequency. This is called the “startup condition.”
- The voltage swing in an oscillator is determined by saturation or nonlinear behavior of the devices.
- Ring oscillators consist of multiple identical gain stages in a loop and find wide application in integrated circuits, e.g., microprocessors and memories.
- The impedance of a parallel LC tank exhibits a zero phase at resonance. A lossy tank reduces to a single resistor at this frequency.
- If two common-source stages having resonant loads are placed in a feedback loop, an oscillator is formed.
- The cross-coupled LC oscillator is extensively used in high-frequency integrated circuits, e.g., WiFi transceivers. This topology provides a differential output.
- The Colpitts LC oscillator employs a single transistor and finds application in high-frequency discrete design. This topology provides a single-ended output.
- For low to moderate frequencies, the phase shift and Wien-bridge oscillators are used in discrete design. They can be readily implemented by means of op amps.
- For precise and stable frequencies, crystal oscillators can be used. Such circuits serve as the “reference frequency” in many applications, e.g., microprocessors, memories, wireless transceivers, etc.

PROBLEMS

Sec. 13.1 Oscillation Conditions

- 13.1.** A negative-feedback system is shown in Fig. 13.35. Under what conditions does the system oscillate?

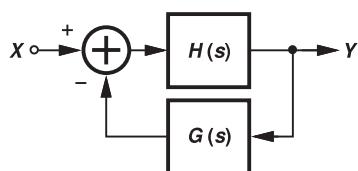


Figure 13.35

- 13.2.** A negative-feedback system is shown in Fig. 13.36. Under what conditions does the system oscillate?

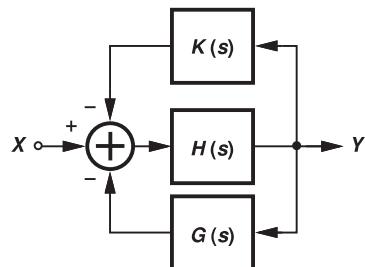


Figure 13.36

- 13.3.** Consider the simple common-emitter stage shown in Fig. 13.37. Explain why this circuit does not oscillate.

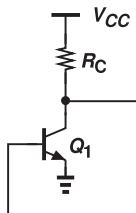


Figure 13.37

- 13.4.** A differential pair is placed in a negative-feedback loop as shown in Fig. 13.38. Can this circuit oscillate? Explain.

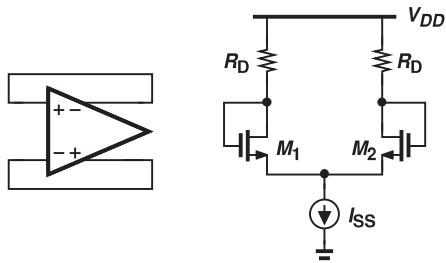


Figure 13.38

- *13.5.** Explain what happens if the polarity of feedback is changed in the circuit of Fig. 13.38, i.e., the gate of M_1 is tied to the drain of M_2 and vice versa.

- *13.6.** A differential pair followed by source followers is placed in a negative-feedback loop as illustrated in Fig. 13.39. Consider only the capacitances shown in the circuit. Can this circuit oscillate? Explain.

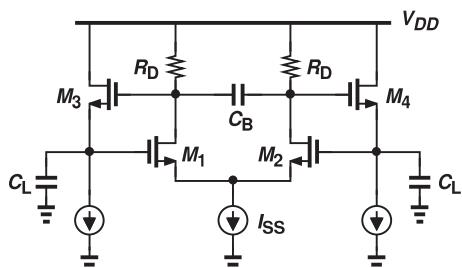


Figure 13.39

- **13.7.** We insert two resistors in series with the gates of M_1 and M_2 in Fig. 13.39. Taking into account C_{GS1} and C_{GS2} in addition to the other four capacitors, explain whether the circuit can oscillate.

Sec. 13.2 Ring Oscillators

- 13.8.** Suppose in the ring oscillator of Fig. 13.8, the value of R_D is doubled. How do the oscillation frequency and startup condition change?

- *13.9.** Suppose in the ring oscillator of Fig. 13.8, the value of C_D is doubled. How do the oscillation frequency and startup condition change?

- *13.10.** In the ring oscillator of Fig. 13.8, we assume C_D arises from C_{GS} and neglect other capacitances. If the width and bias current of each transistor are doubled and R_D is halved, what happens to the oscillation frequency?

- 13.11.** The supply voltage of the ring oscillator of Fig. 13.8 is gradually reduced. Explain why the oscillation eventually ceases.

- *13.12.** Derive the oscillation frequency and startup condition for the ring oscillator of Fig. 13.8 if the number of stages is increased to five.

- *13.13.** Derive the oscillation frequency and startup condition for the ring oscillator of Fig. 13.9(a). Consider only the C_{GS} of the NMOS transistors and assume all transistors are in saturation.

- 13.14.** Suppose the bias voltage, V_b , in Fig. 13.9(a) is gradually raised to reduce the bias current of each stage. Does the circuit have a lower or higher tendency to oscillate? (Hint: as the bias current decreases, I_O rises more rapidly than g_m falls.)

- *13.15.** Derive the oscillation frequency and startup condition for the ring oscillator of Fig. 13.9(b). Consider the C_{GS} of both NMOS and PMOS transistors and assume all transistors are in saturation.

- 13.16.** Draw the large-signal waveforms of Fig. 13.10 for a five-stage ring oscillator similar to the circuit of Fig. 13.9(b).

- 13.17.** A ring oscillator is sometimes used to provide *multiple* outputs with different phases. What is the phase difference between consecutive nodes in the circuit of Fig. 13.9(b)? (Hint: consider the waveforms in Fig. 13.10.)
- 13.18.** A ring oscillator employs N stages. What is the phase difference between the consecutive outputs of the circuit?

Sec. 13.3 LC Oscillators

- 13.19.** Repeat the plots in Fig. 13.13 if both L_1 and C_1 in Fig. 13.12 are doubled.
- 13.20.** In the circuit of Fig. 13.12, assume $V_{in}(t) = V_0 \cos \omega_{int} t$. Plot $I_{in}(t)$ if ω_{in} is slightly below ω_1 or above ω_1 . (Hint: consider the magnitude and phase response in Fig. 13.13.)
- 13.21.** Compute $Z_2(s)$ in the tank of Fig. 13.14(a). Compute the pole frequencies.
- 13.22.** Determine the pole frequencies of $Z_2(s)$ in Eq. (13.13) and sketch their locations on the complex plane as R_p goes from infinity to a small value.
- ***13.23.** In this problem, we wish to determine how the tank in Fig. 13.14(a) can be transformed to that in Fig. 13.14(b). Compute the impedance of each tank at a frequency $s = j\omega$ and equate the two impedances. Now, equate their real parts and do the same with their imaginary parts. Also, assume $L_1\omega/R_1 \gg 1$. (We say the inductor has a high quality factor, Q .) Determine the value of R_p .
- 13.24.** Explain qualitatively what happens to the plots in Fig. 13.15 if R_p is doubled.
- 13.25.** Sketch the instantaneous power dissipated by R_p in Fig. 13.16(b) as a function of time. Can you predict what we will obtain if we integrate the area under this plot?
- 13.26.** In the CS stage of Fig. 13.17(a), $V_{in} = V_0 \cos \omega_1 t + V_1$, where $\omega_1 = 1/\sqrt{L_1 C_1}$ and V_1 is a bias value. Plot V_{out} as a function of time. (Hint: what is the dc value of the output when the input is just equal to V_1 ?)
- 13.27.** Explain qualitatively what happens to the plots in Fig. 13.17(b) if R_p is doubled.
- ****13.28.** In the circuit of Fig. 13.18(a), we break the loop at the gate of M_1 and apply an input as shown in Fig. 13.40. Suppose $V_{in} = V_0 \cos \omega_1 t + V_1$, where ω_1 is the resonance frequency of each tank and V_1 is a bias voltage. Plot the waveforms at nodes X and Y .
- 13.29.** Suppose the LC oscillator of Fig. 13.18(a) is realized with *ideal* tanks, i.e., $R_p = \infty$. Taking channel-length modulation into account, determine the startup condition.
- ***13.30.** Suppose the two tanks in the oscillator of Fig. 13.18(a) have slightly different resonance frequencies. Can you roughly predict the oscillation frequency? (Hint: consider the open-loop frequency response.)
- 13.31.** Explain why the circuit of Fig. 13.19(c) does not oscillate if the tanks are replaced with resistors.
- 13.32.** If we increase C_1 in the Colpitts oscillator of Fig. 13.21(a), do we relax or tighten the startup condition?
- 13.33.** What happens if $C_2 = 0$ in the Colpitts oscillator of Fig. 13.21(a)?
- ****13.34.** Repeat the analysis of the Colpitts oscillator but by breaking the loop at the emitter of Q_1 . The equivalent circuit is shown in Fig. 13.41. Note that the loading seen at the emitter, $1/g_m$, is included in parallel with C_2 .
- 13.35.** Repeat the analysis of the Colpitts oscillator while including r_o of Q_1 but assuming $R_p = \infty$.

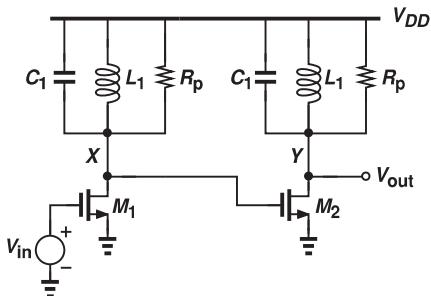


Figure 13.40

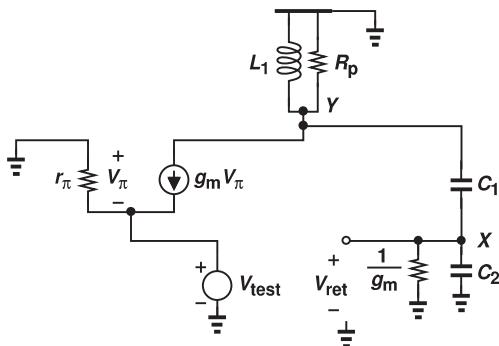


Figure 13.41

- 13.36.** Repeat the analysis of the Colpitts oscillator while assuming an output resistance, R_1 , for I_1 but neglecting R_p .
- 13.37.** Derive Eq. (13.27) if $R_p = \infty$. You can use the equivalent circuit of Fig. 13.21(b) and tie R_{in} from X to ground.

Sec. 13.4 and 13.5 Phase Shift and Wien Bridge Oscillators

- 13.38.** In the oscillator of Fig. 13.23(a), we have $R_1 = R_2 = R_3 = R$, $C_1 = C_2 = C_3 = C$, and $V_{out} = V_0 \cos \omega_0 t$, where $\omega_0 = 1/(RC)$. Plot the waveforms at X and Y . Assume $A_0 = 2$.
- 13.39.** A student decides to employ three *low-pass* sections to create the phase shift necessary in a phase shift oscillator (Fig. 13.42). If $R_1 = R_2 = R_3 = R$ and $C_1 = C_2 = C_3 = C$, repeat the analysis for this circuit.

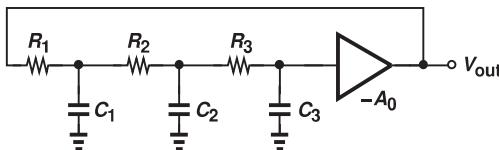


Figure 13.42

- 13.40.** Compare the oscillation frequency and startup condition of the phase shift oscillator with those of a three-stage ring oscillator.
- 13.41.** Suppose a phase shift oscillator incorporates *four* high-pass sections with equal

resistors and capacitors. Derive the oscillation frequency and the startup condition for such a circuit.

- *13.42.** Can the circuit shown in Fig. 13.43 oscillate? Explain. Assume $R_1 = R_2 = R_3 = R$ and $C_1 = C_2 = C_3 = C$.

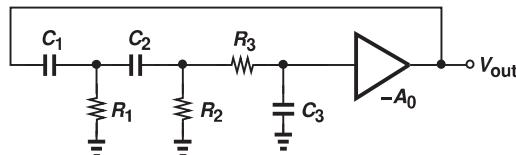


Figure 13.43

- 13.43.** Consider the oscillator of Fig. 13.23(a) and assume the amplifier contains a pole, i.e., $A(s) = A_0/(1 + s/\omega_0)$. Also, assume the phase shift network contains only two high-pass sections with $R_1 = R_2 = R$ and $C_1 = C_2 = C$. Can ω_0 be chosen such that this circuit oscillates?
- 13.44.** In the circuit of Fig. 13.26(a), $R_1 = R_2 = R$ and $C_1 = C_2 = C$. If $V_{in} = V_0 \cos \omega_0 t$, where $\omega_0 = 1/(RC)$, plot V_{out} as a function of time.
- *13.45.** A student decides to modify the Wien oscillator of Fig. 13.26(b) as shown in Fig. 13.44. Can this circuit oscillate? Explain.

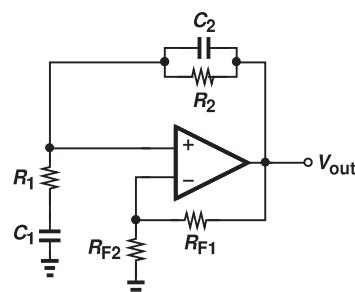


Figure 13.44

Sec. 13.6 Crystal Oscillators

- 13.46.** Derive an expression for Z_S in Fig. 13.28(b) if $s = j\omega$.
- 13.47.** Sketch the real and imaginary parts of Z_{in} in Fig. 13.29(c) as a function of frequency.

- 13.48.** Suppose the negative-resistance circuit of Fig. 13.29(a) employs a bipolar transistor rather than a MOSFET. Determine Z_{in} and the equivalent circuit.
- 13.49.** Determine Z_{in} in Fig. 13.29(a) if channel-length modulation is not neglected. Can you construct a simple equivalent circuit for Z_{in} such as that in Fig. 13.29(c)?
- 13.50.** Suppose capacitor C_1 in Fig. 13.30(a) begins with an initial condition of V_0 . Derive an equation for V_{out} assuming that R_p is large. (A large R_p means the tank has a high quality factor, Q).
- **13.51.** We wish to determine the startup condition for the crystal oscillator of Fig. 13.31(b).
- Prove that Z_{cr} is given by the following equation at the parallel resonance frequency:
- $$Z_{cr}(j\omega_2) = \frac{L_1 C_1 \omega_2^2 - 1}{R_s C_1 C_2 \omega_2^2} + \frac{1}{jC_2 \omega_2}. \quad (13.59)$$
- Now, cancel the real part of $Z_{cr}(j\omega_2)$ by the negative resistance and prove Eq. (13.58).
- **13.52.** Repeat Problem 13.51 if channel-length modulation is not neglected.

Design Problems

In the following problems, unless otherwise stated, assume $\mu_n C_{ox} = 2\mu_p C_{ox} = 100 \text{ } \mu\text{A/V}^2$, $\lambda_n = 0.5 \lambda_p = 0.1 \text{ V}^{-1}$, $V_{THN} = 0.3 \text{ V}$, and $V_{THP} = -0.35 \text{ V}$.

- 13.53.** In Fig. 13.8, $R_D = 1 \text{ k}\Omega$. Design the circuit for a power budget of 3 mW and a frequency of 1 GHz. Assume $V_{DD} = 1.5 \text{ V}$ and $\lambda = 0$.
- 13.54.** In the circuit of Fig. 13.9(a), $V_{DD} - V_b = 0.6 \text{ V}$.
- Choose W/L of the PMOS devices for a bias current of 1 mA.
- 13.55.** (a) Choose W/L of the NMOS devices to meet the startup condition, $g_m N(r_{ON}) || r_{OP} = 2$.
- (b) A 10 nH inductor has a series resistance of 10Ω . Determine the equivalent parallel resistance, R_p , at 1 GHz.
- 13.56.** (a) Design a 1 GHz cross-coupled oscillator using this inductor with a power budget of 2 mW and $V_{DD} = 1.5 \text{ V}$. Choose W/L of the two transistors such that 95% of the tail current is steered to the left or to the right for $|V_X - V_Y| = 500 \text{ mV}$. For simplicity, assume each transistor contributes a capacitance of $1.5 \times W \text{ fF}$, where W is in microns.
- (b) A 20 nH inductor has a series resistance of 15Ω . Compute the equivalent parallel resistance, R_p , at 2 GHz.
- 13.57.** Design the phase shift oscillator of Fig. 13.24 for a frequency of 10 MHz, assuming an ideal op amp and $C_1 = C_2 = C_3 = 1 \text{ nF}$.
- 13.58.** Design the Wien bridge oscillator of Fig. 13.26(b) for a frequency of 10 MHz, assume an ideal op amp and $C_1 = C_2 = 1 \text{ nF}$.
- 13.59.** (a) A crystal with a parallel resonance frequency at 10 MHz has $C_2 = 100 \text{ pF}$, $C_1 = 10 \text{ pF}$ [Fig. 13.28(c)]. Determine the value of L_1 .
- (b) Suppose the crystal series resistance is equal to 5Ω . Design the oscillator of Fig. 13.32(d) for a frequency of 10 MHz. Neglect the transistor capacitances and assume $C_A = C_B = 20 \text{ pF}$, $(W/L)_2 = 2(W/L)_1$, and $V_{DD} = 1.2 \text{ V}$.

SPICE PROBLEMS

In the following problems, use the MOS device models given in Appendix A. For bipolar transistors, assume $I_S = 5 \times 10^{-16}$ A, $\beta = 100$, and $V_A = 5$ V. Also, assume a supply voltage of 1.8 V. (In SPICE, one node of the oscillators must be initialized near zero or V_{DD} to ensure startup.)

- 13.60.** Simulate the oscillator of Fig. 13.8 with $W/L = 10/0.18$ and $C_D = 20$ fF. Choose the value of R_D so that the circuit barely oscillates. Compare the value of $g_m R_D$ with the theoretical minimum of 2. Plot the voltage swings at X , Y , and Z and measure their phase difference.
- 13.61.** Repeat Problem 13.60 but choose R_D equal to four times the minimum acceptable value. How much is the voltage swing in this case? Does the frequency decrease by a factor of 4?
- 13.62.** Simulate the oscillator of Fig. 13.9(a) with $(W/L)_N = 10/0.18$ and $(W/L)_P = 15/0.18$. Choose V_b to obtain a bias current of 0.5 mA in each branch.
- Measure the oscillation frequency.
 - Now, change V_b by ± 100 mV and measure the oscillation frequency. Such a circuit is called a voltage-controlled oscillator (VCO).
- 13.63.** Repeat Problem 13.62 with five stages in the ring and compare the oscillation frequencies with the previous case. Do they decrease by a ratio of 5 to 3?
- 13.64.** Simulate the ring oscillator of Fig. 13.9(b) in two cases.
- Choose $(W/L)_P = 2(W/L)_N = 20/0.18$.
 - Choose $(W/L)_P = 2(W/L)_N = 10/0.18$. Which case yields a higher oscillation frequency?
- 13.65.** We wish to design the circuit of Fig. 13.9(b) for the highest oscillation frequency. Begin with $(W/L)_N = (W/L)_P = 5/0.18$ and decrease the width of the transistors in $0.5 \mu\text{m}$ steps. Plot the oscillation frequency as a function of W .
- 13.66.** We can construct a *four-stage* ring oscillator if we employ differential pairs rather than inverters. Simulate a ring comprising four identical differential pairs with $W/L = 10/0.18$, a tail current of 0.5 mA, and a load resistor of 1 k Ω . Choose the feedback to be *negative* at low frequencies. Plot the waveforms provided by the four stages and measure their phase difference.
- 13.67.** Simulate the cross-coupled oscillator of Fig. 13.19(c) with $W/L = 10/0.18$, $I_{SS} = 1$ mA, and $L_1 = 10$ nH. Place a resistance of 10 Ω in series with each inductor (and exclude R_p) and add enough capacitance from X and Y to ground so as to obtain an oscillation frequency of 1 GHz. Plot the output voltages and the drain currents of M_1 and M_2 as a function of time. What is the minimum value of I_{SS} to sustain oscillation?
- 13.68.** Design and simulate the Colpitts oscillator of Fig. 13.21(a) with $L_1 = 10$ nH, $V_b = 1.2$ V, and $I_1 = 1$ mA. Choose R_p such that $Q = R_p/(L_1\omega) = 10$ at 2 GHz. Also, select the value of $C_1 = C_2$ for an oscillation frequency of 2 GHz. Plot the waveforms at the collector and emitter of Q_1 .
- 13.69.** In Problem 13.68, reduce I_1 in steps of 0.1 mA until the oscillation ceases. Compare the minimum required I_1 with the theoretical value predicted by Eq. (13.26).