

Current Mirrors, Active Loads, and References

4.1 Introduction

Current mirrors made by using active devices have come to be widely used in analog integrated circuits both as biasing elements and as load devices for amplifier stages. The use of current mirrors in biasing can result in superior insensitivity of circuit performance to variations in power supply and temperature. Current mirrors are frequently more economical than resistors in terms of the die area required to provide bias current of a certain value, particularly when the required value of bias current is small. When used as a load element in transistor amplifiers, the high incremental resistance of the current mirror results in high voltage gain at low power-supply voltages.

The first section of this chapter describes the general properties of current mirrors and compares various bipolar and MOS mirrors to each other using these properties. The next section deals with the use of current mirrors as load elements in amplifier stages. The last section shows how current mirrors are used to construct references that are insensitive to variations in supply and temperature. Finally, the appendix analyzes the effects of device mismatch.

4.2 Current Mirrors

$$I_o = K I_i \text{ (independent of } V_{in} \text{ & } V_{out})$$

4.2.1 General Properties

A current mirror is an element with at least three terminals, as shown in Fig. 4.1. The common terminal is connected to a power supply, and the input current source is connected to the input terminal. Ideally, the output current is equal to the input current multiplied by a desired current gain. If the gain is unity, the input current is reflected to the output, leading to the name *current mirror*. Under ideal conditions, the current-mirror gain is independent of input frequency, and the output current is independent of the voltage between the output and common terminals. Furthermore, the voltage between the input and common terminals is ideally zero because this condition allows the entire supply voltage to appear across the input current source, simplifying its transistor-level design. More than one input and/or output terminals are sometimes used.

In practice, real transistor-level current mirrors suffer many deviations from this ideal behavior. For example, the gain of a real current mirror is never independent of the input frequency. The topic of frequency response is covered in Chapter 7, and mainly dc and low-frequency ac signals are considered in the rest of this chapter. Deviations from ideality that will be considered in this chapter are listed below.

1. One of the most important deviations from ideality is the variation of the current-mirror output current with changes in voltage at the output terminal. This effect is characterized

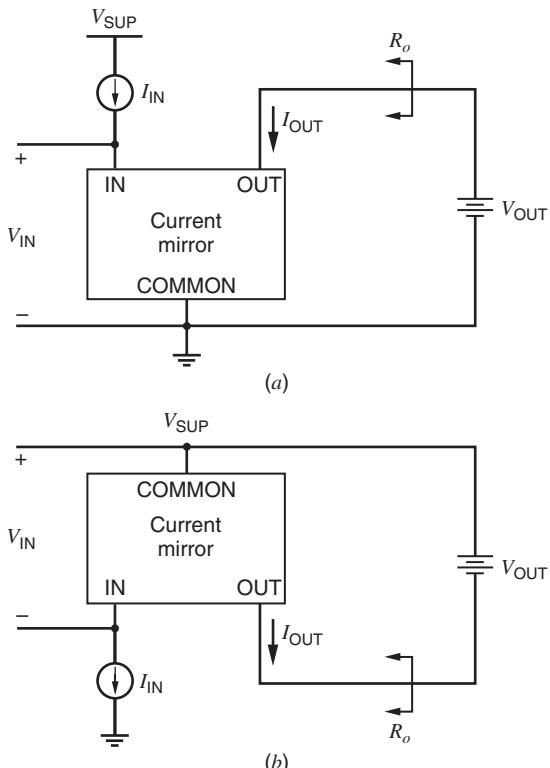


Figure 4.1 Current-mirror block diagrams referenced to (a) ground and (b) the positive supply.

by the small-signal output resistance, R_o , of the current mirror. A Norton-equivalent model of the output of the current mirror includes R_o in parallel with a current source controlled by the input current. The output resistance directly affects the performance of many circuits that use current mirrors. For example, the common-mode rejection ratio of the differential amplifier depends directly on this resistance, as does the gain of the active-load circuits. Increasing the output resistance reduces the dependence of the output current on the output voltage and is therefore desirable. Generally speaking, the output resistance increases in practical circuits when the output current decreases. Unfortunately, decreasing the output current also decreases the maximum operating speed. Therefore, when comparing the output resistance of two current mirrors, they should be compared at identical output currents.

2. Another important error source is the gain error, which is the deviation of the gain of a current mirror from its ideal value. The gain error is separated into two parts: (1) the systematic gain error and (2) the random gain error. The systematic gain error, ϵ , is the gain error that arises even when all matched elements in the mirror are perfectly matched and will be calculated for each of the current mirrors presented in this section. The random gain error is the gain error caused by unintended mismatches between matched elements.
3. When the input current source is connected to the input terminal of a real current mirror, it creates a positive voltage drop, V_{IN} , that reduces the voltage available across the input current source. **Minimizing V_{IN} is important** because it simplifies the design of the input current source, especially in low-supply applications. To reduce V_{IN} , current mirrors sometimes have more than one input terminal. In that case, we will calculate an input voltage for each input terminal. An example is the MOS high-swing cascode current mirror considered in Section 4.2.5.

4. A positive output voltage, V_{OUT} , is required in practice to make the output current depend mainly on the input current. This characteristic is summarized by the minimum voltage across the output branch, $V_{\text{OUT}(\min)}$, that allows the output device(s) to operate in the active region. Minimizing $V_{\text{OUT}(\min)}$ maximizes the range of output voltages for which the current-mirror output resistance is almost constant, which is important in applications where current mirrors are used as active loads in amplifiers (especially with low power-supply voltages). This topic is covered in Section 4.3. When current mirrors have more than one output terminal, each output must be biased above its $V_{\text{OUT}(\min)}$ to make the corresponding output current depend mainly on the input current.

In later sections, the performance of various current mirrors will be compared to each other through these four parameters: R_o , ϵ , V_{IN} , and $V_{\text{OUT}(\min)}$. *¿y la ganancia de corriente?*

4.2.2 Simple Current Mirror

4.2.2.1 Bipolar

The simplest form of a current mirror consists of two transistors. Fig. 4.2 shows a bipolar version of this mirror. Transistor Q_1 is diode connected, forcing its collector-base voltage to zero. In this mode, the collector-base junction is off in the sense that no injection takes place there, and Q_1 operates in the forward-active region. Assume that Q_2 also operates in the forward-active region and that both transistors have infinite output resistance. Then I_{OUT} is controlled by V_{BE2} , which is equal to V_{BE1} by KVL. A KVL equation is at the heart of the operation of all current mirrors. Neglecting junction leakage currents,

$$V_{BE2} = V_T \ln \frac{I_{C2}}{I_{S2}} = V_{BE1} = V_T \ln \frac{I_{C1}}{I_{S1}} \quad (4.1)$$

where $V_T = kT/q$ is the thermal voltage and I_{S1} and I_{S2} are the transistor saturation currents. From (4.1),

$$I_{C2} = \frac{I_{S2}}{I_{S1}} I_{C1} \quad (4.2)$$

If the transistors are identical, $I_{S1} = I_{S2}$ and (4.2) shows that the current flowing in the collector of Q_1 is mirrored to the collector of Q_2 . KCL at the collector of Q_1 yields

$$I_{\text{IN}} - I_{C1} - \frac{I_{C1}}{\beta_F} - \frac{I_{C2}}{\beta_F} = 0 \quad (4.3)$$

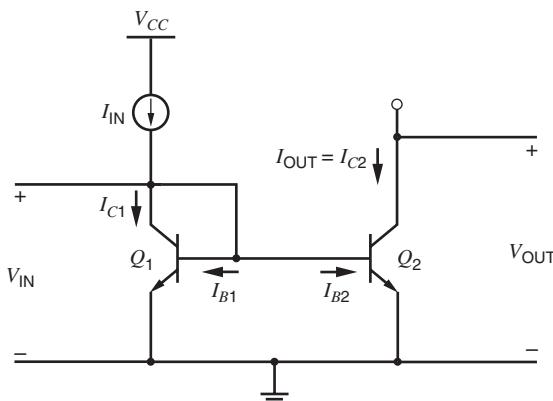


Figure 4.2 A simple bipolar current mirror.

Therefore, with identical transistors,

$$I_{\text{OUT}} = I_{C2} = I_{C1} = \frac{I_{\text{IN}}}{1 + \frac{2}{\beta_F}} = \frac{\beta}{\beta + 2} I_{\text{IN}} \quad (4.4)$$

If β_F is large, the base currents are small and

$$I_{\text{OUT}} = I_{C1} \simeq I_{\text{IN}} \quad (4.5)$$

Thus for identical devices Q_1 and Q_2 , the gain of the current mirror is approximately unity. This result holds for both dc and low-frequency ac currents. Above the 3-dB frequency of the mirror, however, the base current increases noticeably because the impedance of the base-emitter capacitance decreases, reducing the gain of the current mirror. Frequency response is studied in Chapter 7. The rest of this section considers dc currents only.

In practice, the devices need not be identical. Then from (4.2) and (4.3),

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$$I_{\text{OUT}} = \frac{I_{S2}}{I_{S1}} I_{C1} = \left(\frac{I_{S2}}{I_{S1}} I_{\text{IN}} \right) \left(\frac{1}{1 + \frac{1 + (I_{S2}/I_{S1})}{\beta_F}} \right) \quad (4.6)$$

When $I_{S2} = I_{S1}$, (4.6) is the same as (4.4). Since the saturation current of a bipolar transistor is proportional to its emitter area, the first term in (4.6) shows that the gain of the current mirror can be larger or smaller than unity because the emitter areas can be ratioed. If the desired current-mirror gain is a rational number, M/N , the area ratio is usually set by connecting M identical devices called *units* in parallel to form Q_2 and N units in parallel to form Q_1 to minimize mismatch arising from lithographic effects in forming the emitter regions. However, area ratios greater than about five to one consume a large die area dominated by the area of the larger of the two devices. Thus other methods described in later sections are preferred for the generation of large current ratios. The last term in (4.6) accounts for error introduced by finite β_F . Increasing I_{S2}/I_{S1} increases the magnitude of this error by increasing the base current of Q_2 compared to that of Q_1 .

In writing (4.1) and (4.2), we assumed that the collector currents of the transistors are independent of their collector-emitter voltages. If a transistor is biased in the forward-active region, its collector current actually increases slowly with increasing collector-emitter voltage. Fig. 4.3 shows an output characteristic for Q_2 . The output resistance of the current mirror at any given operating point is the reciprocal of the slope of the output characteristic at that point. In the forward-active region,

$$R_o = r_{o2} = \frac{V_A}{I_{C2}} \quad (4.7)$$

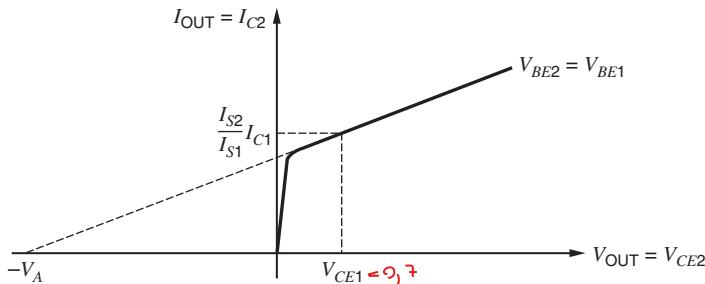


Figure 4.3 *npn* output characteristic.

The point where $V_{CE2} = V_{CE1}$ and $V_{BE2} = V_{BE1}$ is labeled on the characteristic. Because the collector current is controlled by the base-emitter and collector-emitter voltages, $I_{C2} = (I_{S2}/I_{S1})I_{C1}$ at this point. If the slope of the characteristic in saturation is constant, the variation in I_{C2} for changes in V_{CE2} can be predicted by a straight line that goes through the labeled point. As described in Chapter 1, extrapolation of the output characteristic in the forward-active region back to the V_{CE2} axis gives an intercept at $-V_A$, where V_A is the Early voltage. If $V_A \gg V_{CE1}$, the slope of the straight line is about equal to $(I_{S2}/I_{S1})(I_{C1}/V_A)$. Therefore,

COMO $V_{CE1} = 0$, $\gamma V_{CE2} > V_{CE1}$

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EE hace q' I_{C2} crezga

$$I_{OUT} = \frac{I_{S2}}{I_{S1}} I_{C1} \left(1 + \frac{V_{CE2} - V_{CE1}}{V_A} \right) = \frac{\frac{I_{S2}}{I_{S1}} I_{IN} \left(1 + \frac{V_{CE2} - V_{CE1}}{V_A} \right)}{1 + \frac{1 + (I_{S2}/I_{S1})}{\beta_F}} \quad (4.8)$$

Since the ideal gain of the current mirror is I_{S2}/I_{S1} , the systematic gain error, ϵ , of the current mirror can be calculated from (4.8).

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$$\epsilon = \left(\frac{1 + \frac{V_{CE2} - V_{CE1}}{V_A}}{1 + \frac{1 + (I_{S2}/I_{S1})}{\beta_F}} \right) - 1 \approx \frac{V_{CE2} - V_{CE1}}{V_A} - \frac{1 + (I_{S2}/I_{S1})}{\beta_F} \quad (4.9)$$

The first term in (4.9) stems from finite output resistance and the second term from finite β_F . If $V_{CE2} > V_{CE1}$, the polarities of the two terms are opposite. Since the two terms are independent, however, cancellation is unlikely in practice. The first term dominates when the difference in the collector-emitter voltages and β_F are large. For example, with identical transistors and $V_A = 130$ V, if the collector-emitter voltage of Q_1 is held at $V_{BE(on)}$, and if the collector-emitter voltage of Q_2 is 30 V, then the systematic gain error $(30 - 0.6)/130 - 2/200 \approx 0.22$. Thus for a circuit operating at a power-supply voltage of 30 V, the current-mirror currents can differ by more than 20 percent from those values calculated by assuming that the transistor output resistance and β_F are infinite. Although the first term in (4.9) stems from finite output resistance, it does not depend on r_{o2} directly but instead on the collector-emitter and Early voltages. The Early voltage is independent of the bias current, and

$$V_{IN} = V_{CE1} = V_{BE1} = V_{BE(on)} \quad (4.10)$$

Since $V_{BE(on)}$ is proportional to the natural logarithm of the collector current, V_{IN} changes little with changes in bias current. Therefore, changing the bias current in a current mirror changes systematic gain error mainly through changes in V_{CE2} .

Finally, the minimum output voltage required to keep Q_2 in the forward-active region is

$$V_{OUT(min)} = V_{CE2(sat)} \quad (4.11)$$

4.2.2.2 MOS

Figure 4.4 shows an MOS version of the simple current mirror. The drain-gate voltage of M_1 is zero; therefore, the channel does not exist at the drain, and the transistor operates in the saturation or active region if the threshold is positive. Although the principle of operation for MOS transistors does not involve forward biasing any diodes, M_1 is said to be *diode connected* in an analogy to the bipolar case. Assume that M_2 also operates in the active region and that both transistors have infinite output resistance. Then I_{D2} is controlled by V_{GS2} , which is equal to V_{GS1} by KVL. A KVL equation is at the heart of the operation of all current mirrors. As described in Section 1.5.3, the gate-source voltage of a given MOS transistor is usually

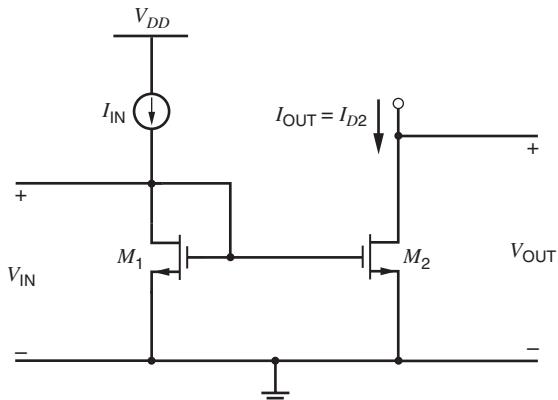


Figure 4.4 A simple MOS current mirror.

separated into two parts: the threshold V_t and the overdrive V_{ov} . Assuming square-law behavior as in (1.157), the overdrive for M_2 is

$$V_{ov2} = V_{GS2} - V_t = \sqrt{\frac{2I_{D2}}{k'(W/L)_2}} \quad (4.12)$$

Since the transconductance parameter k' is proportional to mobility, and since mobility falls with increasing temperature, the overdrive rises with temperature. In contrast, Section 1.5.4 shows that the threshold falls with increasing temperature. From KVL and (1.157),

$$V_{GS2} = V_t + \sqrt{\frac{2I_{D2}}{k'(W/L)_2}} = V_{GS1} = V_t + \sqrt{\frac{2I_{D1}}{k'(W/L)_1}} \quad (4.13)$$

Equation 4.13 shows that the overdrive of M_2 is equal to that of M_1 .

$$V_{ov2} = V_{ov1} = V_{ov} \quad (4.14)$$

If the transistors are identical, $(W/L)_2 = (W/L)_1$, and therefore

$$I_{OUT} = I_{D2} = I_{D1} \quad (4.15)$$

Equation 4.15 shows that the current that flows in the drain of M_1 is mirrored to the drain of M_2 . Since $\beta_F \rightarrow \infty$ for MOS transistors, (4.15) and KCL at the drain of M_1 yield

$$I_{OUT} = I_{D1} = I_{IN} \quad (4.16)$$

Thus for identical devices operating in the active region with infinite output resistance, the gain of the current mirror is unity. This result holds when the gate currents are zero; that is, (4.16) is at least approximately correct for dc and low-frequency ac currents. As the input frequency increases, however, the gate currents of M_1 and M_2 increase because each transistor has a nonzero gate-source capacitance. The part of the input current that flows into the gate leads does not flow into the drain of M_1 and is not mirrored to M_2 ; therefore, the gain of the current mirror decreases as the frequency of the input current increases. The rest of this section considers dc currents only.

In practice, the devices need not be identical. Then from (4.13) and (4.16),

$$I_{OUT} = \frac{(W/L)_2}{(W/L)_1} I_{D1} = \frac{(W/L)_2}{(W/L)_1} I_{IN} \quad (4.17)$$

Equation 4.17 shows that the gain of the current mirror can be larger or smaller than unity because the transistor sizes can be ratioed. To ratio the transistor sizes, either the widths or the lengths can be made unequal in principle. In practice, however, the lengths of M_1 and M_2 are rarely made unequal. The lengths that enter into (4.17) are the effective channel lengths given by (2.35). Equation 2.35 shows that the effective channel length of a given transistor differs from its drawn length by offset terms stemming from the depletion region at the drain and lateral diffusion at the drain and source. Since the offset terms are independent of the drawn length, a ratio of two effective channel lengths is equal to the drawn ratio only if the drawn lengths are identical. As a result, a ratio of unequal channel lengths depends on process parameters that may not be well controlled in practice. Similarly, Section 2.9.1 shows that the effective width of a given transistor differs from the drawn width because of lateral oxidation resulting in a *bird's beak*. Therefore, a ratio of unequal channel widths will also be process dependent. In many applications, however, the shortest channel length allowed in a given technology is selected for most transistors to maximize speed and minimize area. In contrast, the drawn channel widths are usually many times larger than the minimum dimensions allowed in a given technology. Therefore, to minimize the effect of the offset terms when the current-mirror gain is designed to differ from unity, the widths are ratioed rather than the lengths in most practical cases. If the desired current-mirror gain is a rational number, M/N , the ratio is usually set by connecting M identical devices called *units* in parallel to form M_2 and N units in parallel to form M_1 to minimize mismatch arising from lithographic effects in forming the gate regions. As in the bipolar case, ratios greater than about five to one consume a large die area dominated by the area of the larger of the two devices. Thus other methods described in later sections are preferred for the generation of large current ratios.

In writing (4.13) and (4.15), we assumed that the drain currents of the transistors are independent of their drain-source voltages. If a transistor is biased in the active region, its drain current actually increases slowly with increasing drain-source voltage. Figure 4.5 shows an output characteristic for M_2 . The output resistance of the current mirror at any given operating point is the reciprocal of the slope of the output characteristic at that point. In the active region,

$$R_o = r_{o2} = \frac{V_A}{I_{D2}} = \frac{1}{\lambda I_{D2}} \quad (4.18)$$

The point where $V_{DS2} = V_{DS1}$ and $V_{GS2} = V_{GS1}$ is labeled on the characteristic. Because the drain current is controlled by the gate-source and drain-source voltages, $I_{D2} = [(W/L)_2/(W/L)_1]I_{D1}$ at this point. If the slope of the characteristic in saturation is constant, the variation in I_{D2} for changes in V_{DS2} can be predicted by a straight line that goes through the

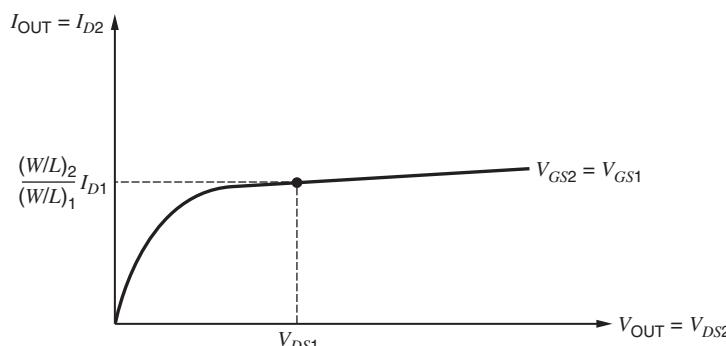


Figure 4.5 Output characteristic of simple MOS current mirror.

labeled point. As described in Chapter 1, extrapolation of the output characteristic in the active region back to the V_{DS2} axis gives an intercept at $-V_A = -1/\lambda$, where V_A is the Early voltage. If $V_A \gg V_{DS1}$, the slope of the straight line is about equal to $[(W/L)_2/(W/L)_1][I_{D1}/V_A]$. Therefore,

$$I_{\text{OUT}} = \frac{(W/L)_2}{(W/L)_1} I_{\text{IN}} \left(1 + \frac{V_{DS2} - V_{DS1}}{V_A} \right) \quad (4.19)$$

Since the ideal gain of the current mirror is $(W/L)_2/(W/L)_1$, the systematic gain error, ϵ , of the current mirror can be calculated from (4.19).

$$\epsilon = \frac{V_{DS2} - V_{DS1}}{V_A} \quad (4.20)$$

For example, if the drain-source voltage of M_1 is held at 1.2 V, and if the drain-source voltage of M_2 is 5 V, then the systematic gain error is $(5 - 1.2)/10 \simeq 0.38$ with $V_A = 10$ V. Thus for a circuit operating at a power-supply voltage of 5 V, the current-mirror currents can differ by more than 35 percent from those values calculated by assuming that the transistor output resistance is infinite. Although ϵ stems from finite output resistance, it does not depend on r_{o2} directly but instead on the drain-source and Early voltages. Since the Early voltage is independent of the bias current, this observation shows that changing the input bias current in a current mirror changes systematic gain error mainly through changes to the drain-source voltages.

For the simple MOS current mirror, the input voltage is

$$V_{\text{IN}} = V_{GS1} = V_t + V_{ov1} = V_t + V_{ov} \quad (4.21)$$

With square-law behavior, the overdrive in (4.21) is proportional to the square root of the input current. In contrast, (4.10) shows that the entire V_{IN} in a simple bipolar mirror is proportional to the natural logarithm of the input current. Therefore, for a given change in the input current, the variation in V_{IN} in a simple MOS current mirror is generally larger than in its bipolar counterpart.

Finally, the minimum output voltage required to keep M_2 in the active region is

$$V_{\text{OUT(min)}} = V_{ov2} = V_{ov} = \sqrt{\frac{2I_{\text{OUT}}}{k'(W/L)_2}} \quad (4.22)$$

Equation 4.22 predicts that $V_{\text{OUT(min)}}$ depends on the transistor geometry and can be made arbitrarily small in a simple MOS mirror, unlike in the bipolar case. However, if the overdrive predicted by (4.22) is less than $2nV_T$, where n is defined in (1.247) and V_T is a thermal voltage, the result is invalid except to indicate that the transistors operate in weak inversion. At room temperature with $n = 1.5$, $2nV_T \simeq 78$ mV. If the transistors operate in weak inversion,

$$V_{\text{OUT(min)}} \simeq 3V_T \quad (4.23)$$

as shown in Fig. 1.43.¹

4.2.3 Simple Current Mirror with Beta Helper

4.2.3.1 Bipolar

In addition to the variation in output current due to finite output resistance, the second term in (4.9) shows that the collector current I_{C2} differs from the input current because of finite β_F . To reduce this source of error, an additional transistor can be added, as shown in Fig. 4.6. If Q_1 and Q_3 are identical, the emitter current of transistor Q_2 is

$$I_{E2} = -\frac{I_{C1}}{\beta_F} - \frac{I_{C3}}{\beta_F} = -\frac{2}{\beta_F} I_{C1} \quad (4.24)$$

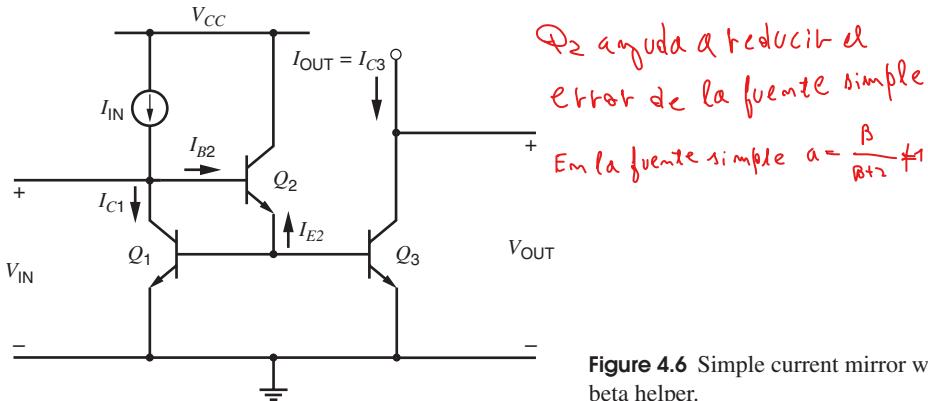


Figure 4.6 Simple current mirror with beta helper.

where I_E , I_C , and I_B are defined as positive when flowing into the transistor, and where we have neglected the effects of finite output resistance. The base current of transistor Q_2 is equal to

$$I_{B2} = -\frac{I_{E2}}{\beta_F + 1} = \frac{2}{\beta_F(\beta_F + 1)} I_{C1} \quad (4.25)$$

Finally, KCL at the collector of Q_1 gives

$$I_{IN} - I_{C1} - \frac{2}{\beta_F(\beta_F + 1)} I_{C1} = 0 \quad (4.26)$$

Since I_{C1} and I_{C3} are equal when Q_1 and Q_3 are identical,

$$I_{OUT} = I_{C3} = \frac{I_{IN}}{1 + \frac{2}{\beta_F(\beta_F + 1)}} \simeq I_{IN} \left(1 - \frac{2}{\beta_F(\beta_F + 1)}\right) \quad (4.27)$$

Equation 4.27 shows that the systematic gain error from finite β_F has been reduced by a factor of $[\beta_F + 1]$, which is the current gain of emitter follower Q_2 . As a result, Q_2 is often referred to as a *beta helper*.

Although the beta helper has little effect on the output resistance and the minimum output voltage of the current mirror, it increases the input voltage by the base-emitter voltage of Q_2 :

PRECIO A PAGAR: V_{IN} ← $V_{IN} = V_{BE1(on)} + V_{BE2(on)}$ (4.28)

If multiple emitter followers are cascaded to further reduce the gain error arising from finite β_F , V_{IN} increases by an extra base-emitter voltage for each additional emitter follower, posing one limit to the use of cascaded emitter followers.

Current mirrors often use a beta helper when they are constructed with *pnp* transistors because the value of β_F for *pnp* transistors is usually less than for *npn* transistors. Another application of the beta-helper configuration is in current mirrors with multiple outputs. An example with two independent outputs is shown in Fig. 4.7. At first, ignore Q_2 and imagine that Q_1 is simply diode connected. Also, let $R_1 = R_3 = R_4 = 0$ here. (The effects of nonzero resistances will be considered in Section 4.2.4.) Then the gain from the input to each output is primarily determined by the area ratios I_{S3}/I_{S1} and I_{S4}/I_{S1} . Because the bases of three instead of two transistors are connected together, the total base current is increased here, which increases the gain error from the input to either output arising from finite β_F . Furthermore, the

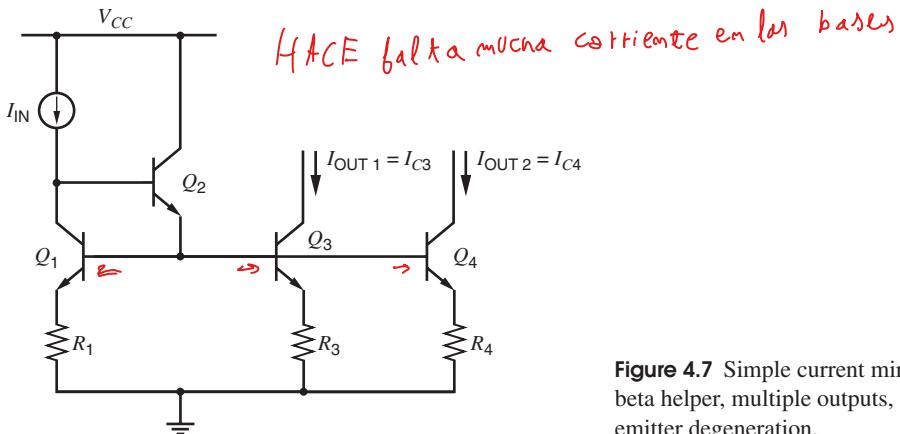


Figure 4.7 Simple current mirror with beta helper, multiple outputs, and emitter degeneration.

gain errors worsen as the number of independent outputs increases. Since the beta helper, Q_2 , reduces the gain error from the input to each output by a factor of $[\beta_F + 1]$, it is often used in bipolar current mirrors with multiple outputs.

4.2.3.2 MOS

Since $\beta_F \rightarrow \infty$ for an MOS transistor, beta helpers are not used in simple MOS current mirrors to reduce the systematic gain error. However, a beta-helper configuration can increase the bandwidth of MOS and bipolar current mirrors.

4.2.4 Simple Current Mirror with Degeneration

4.2.4.1 Bipolar

The performance of the simple bipolar transistor current mirror of Fig. 4.6 can be improved by the addition of emitter degeneration as shown in Fig. 4.7 for a current mirror with two independent outputs. The purpose of the emitter resistors is twofold. First, Appendix A.4.1 shows that the matching between I_{IN} and outputs I_{C3} and I_{C4} can be greatly improved by using emitter degeneration. Second, as shown in Section 3.3.8, the use of emitter degeneration boosts the output resistance of each output of the current mirror. Transistors Q_1 and Q_2 combine to present a very low resistance at the bases of Q_3 and Q_4 . Therefore, from (3.99), the small-signal output resistance seen at the collectors of Q_3 and Q_4 is

$$R_o \simeq r_o(1 + g_m R_E) \quad (4.29)$$

if $r_\pi \gg R_E$. Taking Q_3 as an example and using $g_{m3} = I_{C3}/V_T$, we find

$$R_o \simeq r_{o3} \left(1 + \frac{I_{C3} R_3}{V_T} \right) \quad (4.30)$$

This increase in the output resistance for a given output current also decreases the component of systematic gain error that stems from finite output resistance by the same factor. From (4.9) and (4.30) with infinite β_F ,

$$\epsilon \simeq \frac{V_{CE2} - V_{CE1}}{V_A \left(1 + \frac{I_{C3} R_3}{V_T} \right)} \quad (4.31)$$

The quantity $I_{C3}R_3$ is just the dc voltage drop across R_3 . If this quantity is 260 mV, for example, then R_o is about $10r_o$ at room temperature, and ϵ is reduced by a factor of about eleven. Unfortunately, this improvement in R_o is limited by corresponding increases in the input and minimum output voltages of the mirror:

$$V_{IN} \simeq V_{BE1(on)} + V_{BE2(on)} + I_{IN}R_1 \quad (4.32)$$

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$$V_{OUT(min)} = V_{CE3(sat)} + I_{C3}R_3 \quad (4.33)$$

The emitter areas of Q_1 , Q_3 , and Q_4 may be matched or ratioed. For example, if we want $I_{OUT1} = I_{IN}$ and $I_{OUT2} = 2I_{IN}$, we would make Q_3 identical to Q_1 , and Q_4 consist of two copies of Q_1 connected in parallel so that $I_{S4} = 2I_{S1}$. In addition, we could make $R_3 = R_1$, and R_4 consist of two copies of R_1 connected in parallel so that $R_4 = R_1/2$. Note that all the dc voltage drops across R_1 , R_3 , and R_4 would then be equal. Using KVL around the loop including Q_1 and Q_4 and neglecting base currents, we find

$$I_{C1}R_1 + V_T \ln \frac{I_{C1}}{I_{S1}} = I_{C4}R_4 + V_T \ln \frac{I_{C4}}{I_{S4}} \quad (4.34)$$

V_{BE1}

from which

$$I_{OUT2} = I_{C4} = \frac{1}{R_4} \left(I_{IN}R_1 + V_T \ln \frac{I_{IN} I_{S4}}{I_{C4} I_{S1}} \right) \quad (4.35)$$

Since $I_{S4} = 2I_{S1}$, the solution to (4.35) is

$$I_0 = \frac{R_1}{R_4} I_{IN} + \frac{V_T}{R_4} \ln \left(2 \frac{I_{IN}}{I_0} \right)$$

Anuló el logaritmo, pero ??

$$I_{OUT2} = \frac{R_1}{R_4} I_{IN} = 2I_{IN} \quad (4.36)$$

because the last term in (4.35) goes to zero. If we make the voltage drops $I_{IN}R_1$ and $I_{C4}R_4$ much greater than V_T , the current-mirror gain to the Q_4 output is determined primarily by the resistor ratio R_4/R_1 , and only to a secondary extent by the emitter area ratio, because the natural log term in (4.35) varies slowly with its argument.

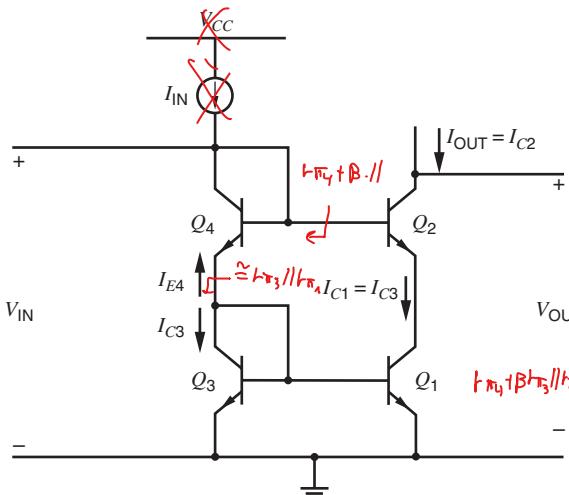
4.2.4.2 MOS

Source degeneration is rarely used in MOS current mirrors because, in effect, MOS transistors are inherently controlled resistors. Thus, matching in MOS current mirrors is improved simply by increasing the gate areas of the transistors.^{2,3,4} Furthermore, the output resistance can be increased by increasing the channel length. To increase the output resistance while keeping the current and $V_{GS} - V_t$ constant, the W/L ratio must be held constant. Therefore, the channel width must be increased as much as the length, and the price paid for the improved output resistance is that increased chip area is consumed by the current mirror.

4.2.5 Cascode Current Mirror

4.2.5.1 Bipolar

Section 3.4.2 shows that the cascode connection achieves a very high output resistance. Since this is a desirable characteristic for a current mirror, exploring the use of cascodes for high-performance current mirrors is natural. A bipolar-transistor current mirror based on the cascode connection is shown in Fig. 4.8. Transistors Q_3 and Q_1 form a simple current mirror, and emitter resistances can be added to improve the matching. Transistor Q_2 acts as the common-base part of the cascode and transfers the collector current of Q_1 to the output while presenting a high



CASCODE:

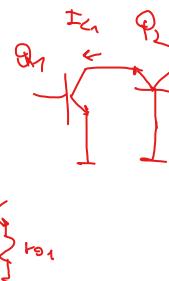


Figure 4.8 Cascode current mirror with bipolar transistors.

output resistance. Transistor Q_4 acts as a diode level shifter and biases the base of Q_2 so that Q_1 operates in the forward-active region with $V_{CE1} \simeq V_{CE3} = V_{BE3(on)}$. If we assume that the small-signal resistances of diodes Q_3 and Q_4 are small, a direct application of (3.98) with $R_E = r_{o1}$ concludes that

$$\begin{aligned} R_o &\simeq r_o (1 + \beta_m h_{FE}/R_E) = \\ &= r_o (1 + \frac{\beta_m R_E}{1 + \frac{\beta_m R_E}{\beta}}) \xrightarrow{(3.98)} R_o = r_{o2} \left(1 + \frac{\beta_m r_{o1}}{1 + \frac{\beta_m r_{o1}}{\beta_0}} \right) \simeq \beta_0 r_{o2} \end{aligned} \quad (4.37)$$

because $\beta_m r_{o1} \simeq \beta_0 r_{o1} \gg \beta_0$. This calculation assumes that almost all of the small-signal current that flows into the collector of Q_2 flows out its base because the small-signal resistance connected to the emitter of Q_2 is much greater than that connected to its base. A key problem with this calculation, however, is that it ignores the effect of the simple current mirror formed by Q_3 and Q_1 . Let i_{b2} and i_{e2} represent increases in the base and emitter currents flowing out of Q_2 caused by increasing output voltage. Then the simple mirror forces $i_{e2} \simeq i_{b2}$. As a result, the variation in the collector current of Q_2 splits into two equal parts and half flows in $r_{\pi2}$. A small-signal analysis shows that R_o in (4.37) is reduced by half to

$$R_o \simeq \frac{\beta_0 r_{o2}}{2} \quad (4.38)$$

Thus, the cascode configuration boosts the output resistance by approximately $\beta_0/2$. For $\beta_0 = 100$, $V_A = 130$ V, and $I_{C2} = 1$ mA,

$$R_o = \frac{\beta_0 V_A}{2 I_{C2}} = \frac{100(130)}{2 \text{ mA}} = 6.5 \text{ M}\Omega \quad (4.39)$$

In this calculation of output resistance, we have neglected the effects of r_μ . Although this assumption is easy to justify in the case of the simple current mirror, it must be reexamined here because the output resistance is so high. The collector-base resistance r_μ results from modulation of the base-recombination current as a consequence of the Early effect, as described in Chapter 1. For a transistor whose base current is composed entirely of base-recombination current, the percentage change in base current when V_{CE} is changed at a constant V_{BE} would equal that of the collector current, and r_μ would be equal to $\beta_0 r_o$. In this case, the effect of

r_μ would be to reduce the output resistance of the cascode current mirror given in (4.38) by a factor of 1.5.

In actual integrated-circuit *npn* transistors, however, only a small percentage of the base current results from recombination in the base. Since only this component is modulated by the Early effect, the observed values of r_μ are a factor of 10 or more larger than $\beta_0 r_o$. Therefore, r_μ has a negligible effect here with *npn* transistors. On the other hand, for lateral *pnp* transistors, the feedback resistance r_μ is much smaller than for *npn* transistors because most of the base current results from base-region recombination. The actual value of this resistance depends on a number of process and device-geometry variables, but observed values range from 2 to 5 times $\beta_0 r_o$. Therefore, for a cascode current mirror constructed with lateral *pnp* transistors, the effect of r_μ on the output resistance can be significant. Furthermore, when considering current mirrors that give output resistances higher than $\beta_0 r_o$, the effects of r_μ must be considered.

In the cascode current mirror, the base of Q_1 is connected to a low-resistance point because Q_3 is diode connected. As a result, feedback from $r_{\mu 1}$ is greatly attenuated and has negligible effect on the output resistance. On the other hand, if the resistance from the base of Q_1 to ground is increased while all other parameters are held constant, local feedback from $r_{\mu 1}$ significantly affects the base-emitter voltage of Q_1 and reduces the output resistance. In the limit where the resistance from the base of Q_1 to ground becomes infinite, Q_1 acts as if it were diode connected. Local feedback is considered in Chapter 8.

The input voltage of the cascode current mirror is

$$V_{IN} = V_{BE3} + V_{BE4} = 2V_{BE(on)} \quad (4.40)$$

Although V_{IN} is higher here than in (4.10) for a simple current mirror, the increase becomes a limitation only if the power-supply voltage is reduced to nearly two diode drops.

The minimum output voltage for which the output resistance is given by (4.38) must allow both Q_1 and Q_2 to be biased in the forward-active region. Since $V_{CE1} \approx V_{CE3} = V_{BE(on)}$,

$$V_{OUT(min)} = V_{CE1} + V_{CE2(sat)} \approx V_{BE(on)} + V_{CE2(sat)} \quad (4.41)$$

Comparing (4.41) and (4.11) shows that the minimum output voltage for a cascode current mirror is higher than for a simple current mirror by a diode drop. This increase poses an important limitation on the minimum supply voltage when the current mirror is used as an active load for an amplifier.

Since $V_{CE1} \approx V_{CE3}$, $I_{C1} \approx I_{C3}$, and the systematic gain error arising from finite transistor output resistance is almost zero. A key limitation of the cascode current mirror, however, is that the systematic gain error arising from finite β_F is worse than for a simple current mirror. From KCL at the collector of Q_3 ,

$$-I_{E4} = I_{C3} + \frac{2I_{C3}}{\beta_F} \quad \begin{matrix} \text{Los nodos de los} \\ \text{Colectores son} \end{matrix} \quad (4.42)$$

From KCL at the collector of Q_4 ,

$$I_{IN} = -I_{E4} + \frac{I_{C2}}{\beta_F} \quad \begin{matrix} \text{importantes} \end{matrix} \quad (4.43)$$

The collector current of Q_2 is

$$I_{C2} = \frac{\beta_F}{\beta_F + 1} I_{C3} \quad (4.44)$$

Substituting (4.42) and (4.44) into (4.43) gives

$$I_{IN} = I_{C3} + \frac{2I_{C3}}{\beta_F} + \frac{I_{C3}}{\beta_F + 1} \quad (4.45)$$

Rearranging (4.45) to find I_{C3} and substituting back into (4.44) gives

$$I_{\text{OUT}} = I_{C2} = \left(\frac{\beta_F}{\beta_F + 1} \right) \left(\frac{I_{\text{IN}}}{1 + \frac{2}{\beta_F} + \frac{1}{\beta_F + 1}} \right) \quad (4.46)$$

Equation 4.46 can be rearranged to give

$$I_{\text{OUT}} = I_{\text{IN}} \left(1 - \frac{4\beta_F + 2}{\beta_F^2 + 4\beta_F + 2} \right) \quad (4.47)$$

Equation 4.47 shows that the systematic gain error is

$$\epsilon = -\frac{4\beta_F + 2}{\beta_F^2 + 4\beta_F + 2} \quad (4.48)$$

When $\beta_F \gg 1$, (4.48) simplifies to

$$\epsilon \simeq -\frac{4}{\beta_F + 4} \quad \begin{array}{l} \text{? Peor error que la} \\ \text{fuente simple?} \end{array} \quad (4.49)$$

In contrast, the systematic gain error stemming from finite β_F in a simple current mirror with identical transistors is about $-2/\beta_F$, which is less in magnitude than (4.49) predicts for a cascode current mirror if $\beta_F > 4$. This limitation of a cascode current mirror is overcome by the Wilson current mirror described in Section 4.2.6.

4.2.5.2 MOS → LARGA CORRIENTE DE SALIDA

The cascode current mirror is widely used in MOS technology, where it does not suffer from finite β_F effects. Figure 4.9 shows the simplest form. From (3.107), the small-signal output resistance is

Con $\beta = \infty$ cualquiera hace una fuente de corriente

$$R_o = r_{o2}[1 + (g_{m2} + g_{mb2})r_{o1}] + r_{o1} \quad (4.50)$$

As shown in the previous section, the bipolar cascode current mirror cannot realize an output resistance larger than $\beta_0 r_o / 2$ because β_0 is finite and nonzero small-signal base current flows in the cascode transistor. In contrast, the MOS cascode is capable of realizing arbitrarily high output resistance by increasing the number of stacked cascode devices because $\beta_0 \rightarrow \infty$ for MOS transistors. However, the MOS substrate leakage current described in Section 1.9 can create a resistive shunt to ground from the output node, which can dominate the output resistance for $V_{\text{OUT}} > V_{\text{OUT(min)}}$.⁵

EXAMPLE

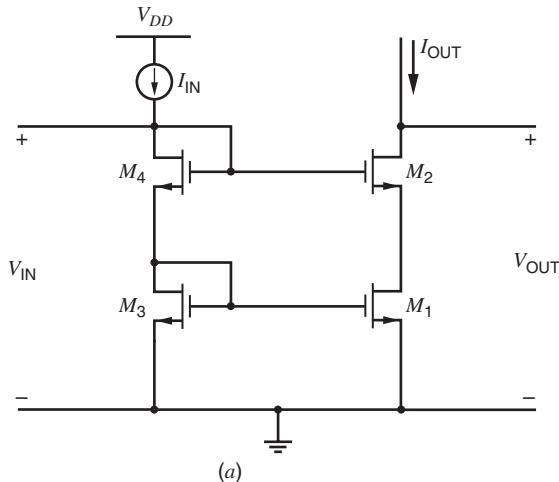
Find the output resistance of the double-cascode current mirror shown in Fig. 4.10. Assume all the transistors operate in the active region with $I_D = 10 \mu\text{A}$, $V_A = 50 \text{ V}$, and $g_{mr_o} = 50$. Neglect body effect.

The output resistance of each transistor is

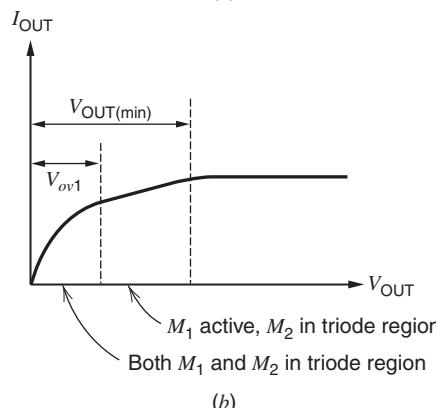
$$r_o = \frac{V_A}{I_D} = \frac{50 \text{ V}}{10 \mu\text{A}} = 5 \text{ M}\Omega$$

From (4.50), looking into the drain of M_2 :

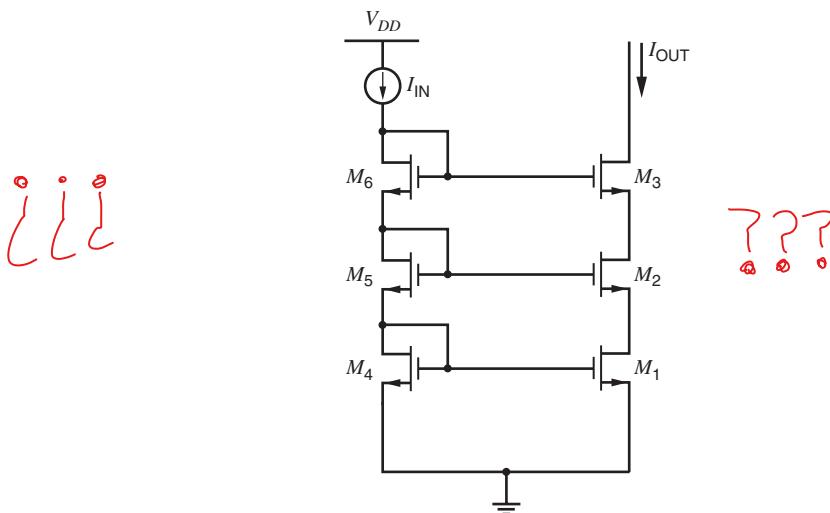
$$R_{o2} = r_{o2}(1 + g_{m2}r_{o1}) + r_{o1} \quad (4.51)$$



(a)



(b)

Figure 4.9 (a) Cascode current mirror using MOS transistors. (b) I-V characteristic.**Figure 4.10** Example of a double-cascode current mirror.

Similarly, looking into the drain of M_3 :

$$R_o = r_{o3}[1 + g_{m3}R_{o2}] + R_{o2} \quad (4.52)$$

Each cascode stage increases the output resistance by a factor of about $(1 + g_m r_o)$. Therefore,

$$R_o \simeq r_o(1 + g_m r_o)^2 \simeq 5(51)^2 \text{ M}\Omega \simeq 13 \text{ G}\Omega \quad (4.53)$$

With such a large output resistance, other parasitic leakage paths, such as the substrate leakage path, could be comparable to this resistance in practice.

From KVL in Fig. 4.9,

$$V_{DS1} = V_{GS3} + V_{GS4} - V_{GS2} \quad (4.54)$$

Since $V_{DS3} = V_{GS3}$, (4.54) shows that $V_{DS1} = V_{DS3}$ when $V_{GS2} = V_{GS4}$. Under this condition, the systematic gain error of the cascode current mirror is zero because M_1 and M_3 are identically biased, and because $\beta_F \rightarrow \infty$ for MOS transistors. In practice, V_{GS2} is not exactly equal to V_{GS4} even with perfect matching unless $V_{\text{OUT}} = V_{\text{IN}}$ because of channel-length modulation. As a result, $V_{DS1} \simeq V_{DS3}$ and

$$\epsilon \simeq 0 \quad (4.55)$$

The input voltage of the MOS cascode current mirror in Fig. 4.9 is

$$\begin{aligned} V_{\text{IN}} &= V_{GS3} + V_{GS4} \\ &= V_{t3} + V_{ov3} + V_{t4} + V_{ov4} \end{aligned} \quad (4.56)$$

The input voltage here includes two gate-source drops, each composed of threshold and overdrive components. Ignoring the body effect and assuming the transistors all have equal overdrives,

$$V_{\text{IN}} = 2V_t + 2V_{ov} \quad (4.57)$$

Also, adding extra cascode levels increases the input voltage by another threshold and another overdrive component for each additional cascode. Furthermore, the body effect increases the threshold of all transistors with $V_{SB} > 0$. Together, these facts increase the difficulty of designing the input current source for low power-supply voltages.

When M_1 and M_2 both operate in the active region, $V_{DS1} \simeq V_{DS3} = V_{GS3}$. For M_2 to operate in the active region, $V_{DS2} > V_{ov2}$ is required. Therefore, the minimum output voltage for which M_1 and M_2 operate in the active region is

$$\begin{aligned} V_{\text{OUT(min)}} &= V_{DS1} + V_{ov2} \\ &\simeq V_{GS3} + V_{ov2} = V_t + V_{ov3} + V_{ov2} \end{aligned} \quad (4.58)$$

If the transistors all have equal overdrives,

$$V_{\text{OUT(min)}} \simeq V_t + 2V_{ov} \quad (4.59)$$

On the other hand, M_2 operates in the triode region if $V_{\text{OUT}} < V_{\text{OUT(min)}}$, and both M_1 and M_2 operate in the triode region if $V_{\text{OUT}} < V_{ov1}$. These results are shown graphically in Fig. 4.9b.

Although the overdrive term in (4.59) can be made small by using large values of W for a given current, the threshold term represents a significant loss of voltage swing when the current mirror is used as an active load in an amplifier. The threshold term in (4.59) stems from the biasing of the drain-source voltage of M_1 so that

$$V_{DS1} = V_{\text{IN}} - V_{GS2} \quad (4.60)$$

Ignoring the body effect and assuming that M_1 - M_4 all operate in the active region with equal overdrives,

$$V_{DS1} = V_t + V_{ov} \quad (4.61)$$

Therefore, the drain-source voltage of M_1 is a threshold larger than necessary to operate M_1 in the active region. To reduce V_{DS1} , the voltage from the gate of M_2 to ground can be level shifted down by a threshold as shown in Fig. 4.11a. In practice, a source follower is used to implement the level shift, as shown in Fig. 4.11b.⁶ Transistor M_5 acts as the source follower and is biased by the output of the simple current mirror M_3 and M_6 . Because the gate-source voltage of M_5 is greater than its threshold by the overdrive, however, the drain-source voltage of M_1 would be zero with equal thresholds and overdrives on all transistors. To bias M_1 at the

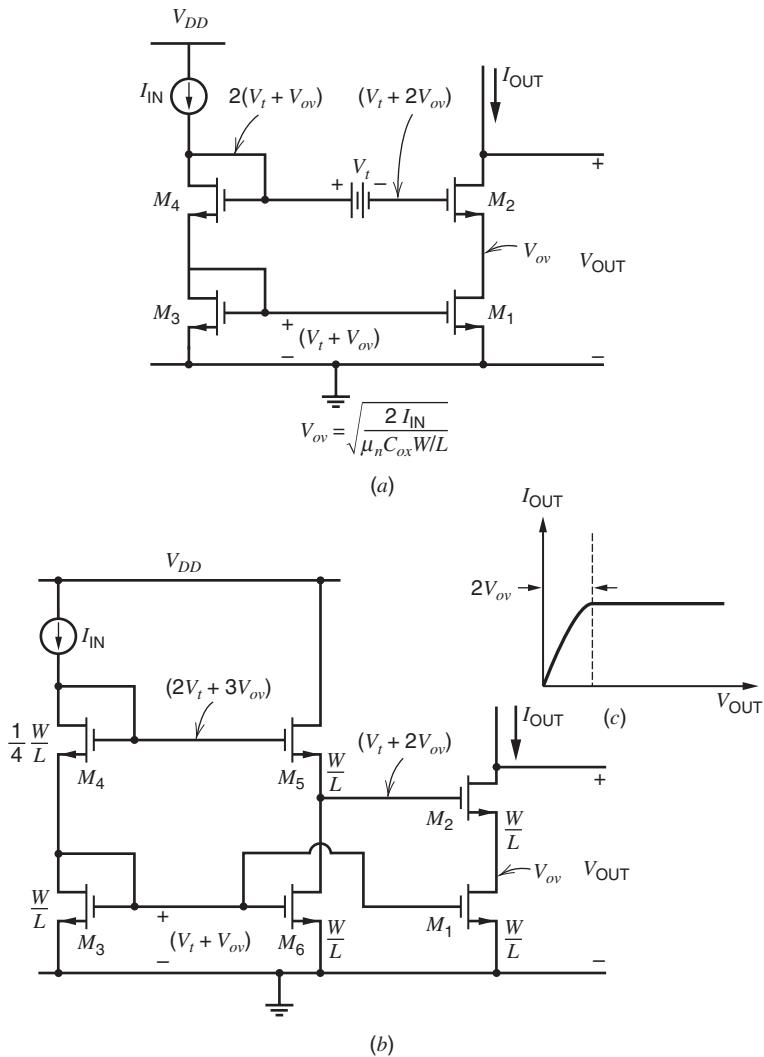


Figure 4.11 (a) MOS cascode current mirror with improved biasing for maximum voltage swing. (b) Practical implementation. (c) I-V characteristic.

boundary between the active and triode regions,

$$V_{DS1} = V_{ov} \quad (4.62)$$

is required. Therefore, the overdrive on M_4 is doubled by reducing its W/L by a factor of four to satisfy (4.62). As a result, the threshold term in (4.59) is eliminated and

$$V_{OUT(min)} \simeq 2V_{ov} \quad (4.63)$$

Because the minimum output voltage does not contain a threshold component, the range of output voltages for which M_1 and M_2 both operate in the active region is significantly improved. Therefore, the current mirror in Fig. 4.11 places much less restriction on the range of output voltages that can be achieved in an amplifier using this current mirror as an active load than the mirror in Fig. 4.9. For this reason, the mirror in Fig. 4.11 is called a *high-swing cascode current mirror*. This type of level shifting to reduce $V_{OUT(min)}$ can also be applied to bipolar circuits.

The output resistance of the high-swing cascode current mirror is the same as in (4.50) when both M_1 and M_2 operate in the active region. However, the input voltage and the systematic gain error are worsened compared to the cascode current mirror without level shift. The input voltage is still given by (4.56), but the overdrive component of the gate-source voltage of M_4 has increased by a factor of two because its W/L has been reduced by a factor of four. Therefore,

$$V_{IN} = 2V_t + 3V_{ov} \quad (4.64)$$

Since M_3 and M_1 form a simple current mirror with unequal drain-source voltages, the systematic gain error is

$$\epsilon = \frac{V_{DS1} - V_{DS3}}{V_A} \simeq \frac{V_{ov1} - (V_t + V_{ov1})}{V_A} = -\frac{V_t}{V_A} \quad (4.65)$$

The negative sign in (4.65) shows that $I_{OUT} < I_{IN}$. For example, if $I_{IN} = 100 \mu A$, $V_t = 1 V$, and $V_A = 10 V$, $\epsilon \simeq -0.1$, which means that $I_{OUT} \simeq 90 \mu A$.

In practice, $(W/L)_4 < (1/4)(W/L)$ is usually selected for two reasons. First, MOS transistors display an indistinct transition from the triode to active regions. Therefore, increasing the drain-source voltage of M_1 by a few hundred millivolts above V_{ov1} is usually required to realize the incremental output resistance predicted by (4.50). Second, although the body effect was not considered in this analysis, it tends to reduce the drain-source voltage on M_1 , which is determined by the following KVL loop

$$V_{DS1} = V_{GS3} + V_{GS4} - V_{GS5} - V_{GS2} \quad (4.66)$$

Each of the gate-source voltage terms in (4.66) contains a threshold component. Since the source-body voltage of M_5 is higher than that of M_4 , $V_{t5} > V_{t4}$. Also, $V_{t2} > V_{t3}$ because the source-body voltage of M_2 is higher than that of M_3 . Simulations with high-accuracy models are usually required to find the optimum $(W/L)_4$.

One drawback of the current mirror in Fig. 4.11 is that the input current is mirrored to a new branch to do the level shift. Combining the input branches eliminates the possibility of mismatch between the two branch currents and may reduce the power dissipation. In a single combined input branch, some element must provide a voltage drop equal to the desired difference between the gate voltages of M_1 and M_2 . To bias M_1 at the edge of the active region, the required voltages from the gates M_1 and M_2 to ground are $V_t + V_{ov}$ and $V_t + 2V_{ov}$, respectively. Therefore, the desired difference in the gate voltages is V_{ov} . This voltage difference can be developed across the drain to the source of a transistor deliberately operated in the triode region, as shown in Fig. 4.12a.⁷ Since M_6 is diode connected, it operates

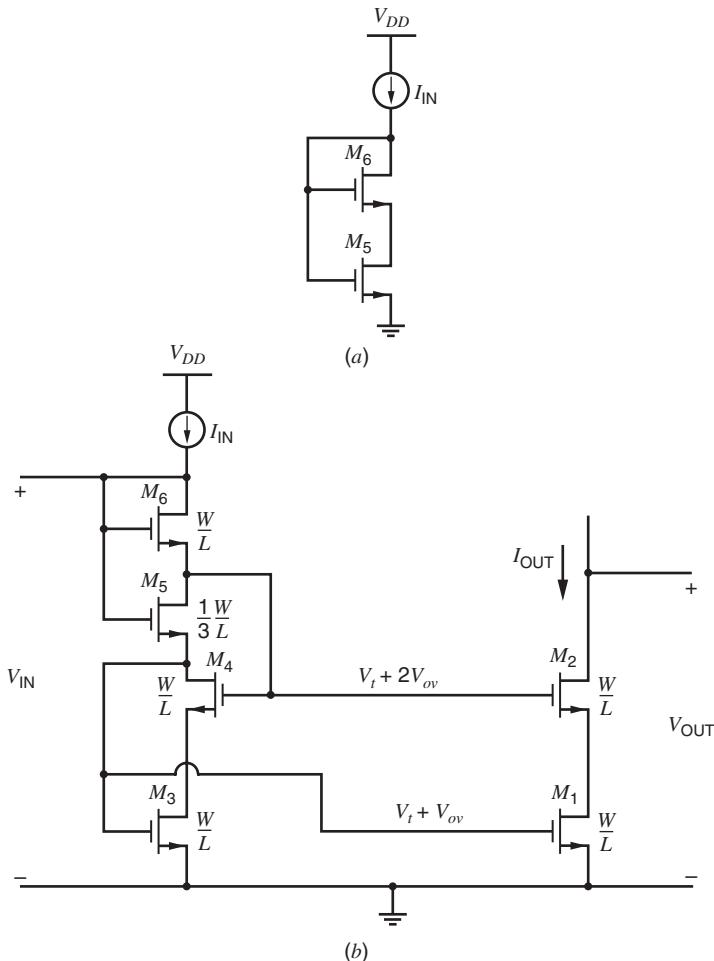


Figure 4.12 (a) Circuit that forces M_5 to operate in the triode region. (b) Sooch cascode current mirror using the circuit in (a).

in the active region as long as the input current and threshold are positive. However, since the gate-source voltage of M_6 is equal to the gate-drain voltage of M_5 , a channel exists at the drain of M_5 when it exists at the source of M_6 . In other words, M_6 forces M_5 to operate in the triode region.

To use the circuit in Fig. 4.12a in a current mirror, we would like to choose the aspect ratios of the transistors so that the drain-source voltage of M_5 is V_{ov} . Since M_6 operates in the active region,

$$I_{IN} = \frac{k'}{2} \left(\frac{W}{L} \right)_6 (V_{GS6} - V_t)^2 \quad (4.67)$$

Since M_5 operates in the triode region,

$$I_{IN} = \frac{k'}{2} \left(\frac{W}{L} \right)_5 (2(V_{GSS5} - V_t)V_{DS5} - (V_{DS5})^2) \quad (4.68)$$

The goal is to set

$$V_{DS5} = V_{ov} \quad (4.69)$$

when

$$V_{GS6} = V_t + V_{ov} \quad (4.70)$$

From (4.69) and (4.70),

$$V_{GS5} = V_{GS6} + V_{DS5} = V_t + 2V_{ov} \quad (4.71)$$

Substituting (4.68) - (4.71) into (4.67) gives

$$\frac{k'}{2} \left(\frac{W}{L} \right)_6 (V_{ov})^2 = \frac{k'}{2} \left(\frac{W}{L} \right)_5 \left(2(2V_{ov})V_{ov} - (V_{ov})^2 \right) \quad (4.72)$$

Equation 4.72 can be simplified to

$$\left(\frac{W}{L} \right)_5 = \frac{1}{3} \left(\frac{W}{L} \right)_6 \quad (4.73)$$

The circuit of Fig. 4.12a is used in the current mirror of Fig. 4.12b,⁷ which is called the *Sooch* cascode current mirror after its inventor. At first, ignore transistor M_4 and assume that M_3 is simply diode connected. The difference between the voltages to ground from the gates of M_1 and M_2 is set by the drain-source voltage of M_5 . By choosing equal aspect ratios for all devices except M_5 , whose aspect ratio is given by (4.73), the drain-source voltage of M_5 is V_{ov} and M_1 is biased at the edge of the active region. The output resistance, minimum output voltage, input voltage, and systematic gain error are the same as in (4.50), (4.63), (4.64), and (4.65) respectively.

Now we will consider the effect of transistor M_4 . The purpose of M_4 is to set the drain-source voltage of M_3 equal to that of M_1 . Without M_4 , these drain-source voltages differ by a threshold, causing nonzero systematic gain error. With M_4 ,

$$V_{DS3} = V_{G2} - V_{GS4} \quad (4.74)$$

where

$$V_{G2} = V_{GS3} + V_{DS5} \quad (4.75)$$

Ignoring channel-length modulation,

$$V_{G2} = (V_t + V_{ov}) + V_{ov} = V_t + 2V_{ov} \quad (4.76)$$

Ignoring the body effect and assuming that M_4 operates in the active region,

$$V_{GS4} = V_t + V_{ov} \quad (4.77)$$

Then substituting (4.76) and (4.77) into (4.74) gives

$$V_{DS3} = V_{ov} \quad (4.78)$$

If M_2 also operates in the active region under these conditions, $V_{DS3} = V_{DS1}$. As a result, the systematic gain error is

$$\epsilon = 0 \quad (4.79)$$

Therefore, the purpose of M_4 is to equalize the drain-source voltages of M_3 and M_1 to reduce the systematic gain error.

For M_4 to operate in the active region, $V_{DS4} > V_{ov}$ is required. Since

$$V_{DS4} = V_{GS3} - V_{DS3} = (V_t + V_{ov}) - V_{ov} = V_t \quad (4.80)$$

Equation 4.80 shows that M_4 operates in the active region if $V_t > V_{ov}$. Although this condition is usually satisfied, a low threshold and/or high overdrive may cause M_4 to operate in the triode region. If this happens, the gate-source voltage of M_4 depends strongly on its drain-source voltage, increasing the systematic gain error. Since increasing temperature causes the threshold to decrease, but the overdrive to increase, checking the region of operation of M_4 in simulation at the maximum expected operating temperature is important in practice.

The main limitation of the high-swing cascode current mirrors just presented, is that the input voltage is large. In Fig. 4.11, the input voltage is the sum of the gate-source voltages of M_3 and M_4 and is given by (4.64) ignoring body effect. In Fig. 4.12, the input voltage is

$$\begin{aligned} V_{IN} &= V_{GS3} + V_{DS5} + V_{GS6} \\ &= V_t + V_{ov} + V_{ov} + V_t + V_{ov} \\ &= 2V_t + 3V_{ov} \end{aligned} \quad (4.81)$$

Equation 4.81 shows that the input voltage of the high-swing cascode current mirror in Fig. 4.12 is the same as in (4.64) for Fig. 4.11. The large input voltages may limit the minimum power-supply voltage because a transistor-level implementation of the input current source requires some nonzero drop for proper operation. With threshold voltages of about 1 V, the cascode current mirrors in Figs. 4.11 and 4.12 can operate properly for power-supply voltages greater than about 3 V. Below about 2 V, however, reduced thresholds or a new configuration is required. Reducing the magnitude of the threshold for all transistors increases the difficulty in turning off transistors that are used as switches. This problem can be overcome by using low-threshold devices in the current mirror and high-threshold devices as switches, but this solution increases process complexity and cost. Therefore, circuit techniques to reduce the input voltage are important to minimize cost.

To reduce the input voltage, the input branch can be split into two branches, as shown in Fig. 4.13. If M_1 and M_2 are biased in the active region, the output resistance is still given by (4.50). Also, the minimum output voltage for which (4.50) applies is still given by (4.63). Furthermore, if M_4 operates in the active region, the drain-source voltage of M_3 is equal to that of M_1 , and the systematic gain error is still zero as in (4.79).

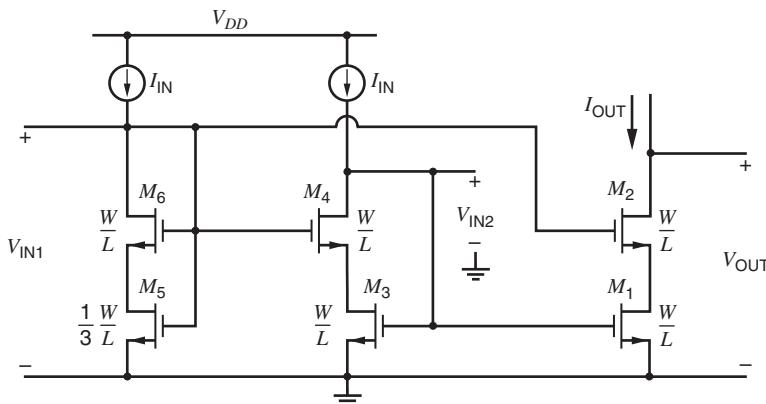


Figure 4.13 MOS high-swing current mirror with two input branches.

Since the mirror in Fig. 4.13 has two input branches, an input voltage can be calculated for each:

$$V_{IN1} = V_{DS5} + V_{GS6} = V_t + 2V_{ov} \quad (4.82)$$

$$V_{IN2} = V_{GS3} = V_t + V_{ov} \quad (4.83)$$

Both V_{IN1} and V_{IN2} are less than the input voltage given in (4.64) for Fig. 4.12b by more than a threshold, allowing the input current sources to operate properly with power-supply voltages greater than about 2 V, assuming thresholds of about 1 V.

Finally, in Fig. 4.13, the drain-source voltage of M_5 is only used to bias the source of M_6 . Therefore, M_5 and M_6 can be collapsed into one diode-connected transistor whose source is grounded. Call this replacement transistor M_7 . The aspect ratio of M_7 should be a factor of four smaller than the aspect ratios of M_1-M_4 to maintain the bias conditions as in Fig. 4.13. In practice, the aspect ratio of M_7 is further reduced to bias M_1 past the edge of the active region and to overcome a mismatch in the thresholds of M_7 and M_2 caused by body effect.

4.2.6 Wilson Current Mirror

4.2.6.1 Bipolar

The main limitation of the bipolar cascode current mirror is that the systematic gain error stemming from finite β_F was large, as given in (4.49). To overcome this limitation, the Wilson current mirror can be used as shown in Fig. 4.14a.⁸ This circuit uses negative feedback through Q_1 , activating Q_3 to reduce the base-current error and raise the output resistance. (See Chapter 8.)

From a qualitative standpoint, the difference between the input current and I_{C3} flows into the base of Q_2 . This base current is multiplied by $(\beta_F + 1)$ and flows in the diode-connected transistor Q_1 , which causes current of the same magnitude to flow in Q_3 . A feedback path is thus formed that regulates I_{C3} so that it is nearly equal to the input current, reducing the systematic gain error caused by finite β_F . Similarly, when the output voltage increases, the collector current of Q_2 also increases, in turn increasing the collector current of Q_1 . As a result, the collector current of Q_3 increases, which reduces the base current of Q_2 . The decrease in the base current of Q_2 caused by negative feedback reduces the original change in the collector current of Q_2 and increases the output resistance.

To find the output resistance of the Wilson current mirror when all transistors operate in the active region, we will analyze the small-signal model shown in Fig. 4.14b, in which a

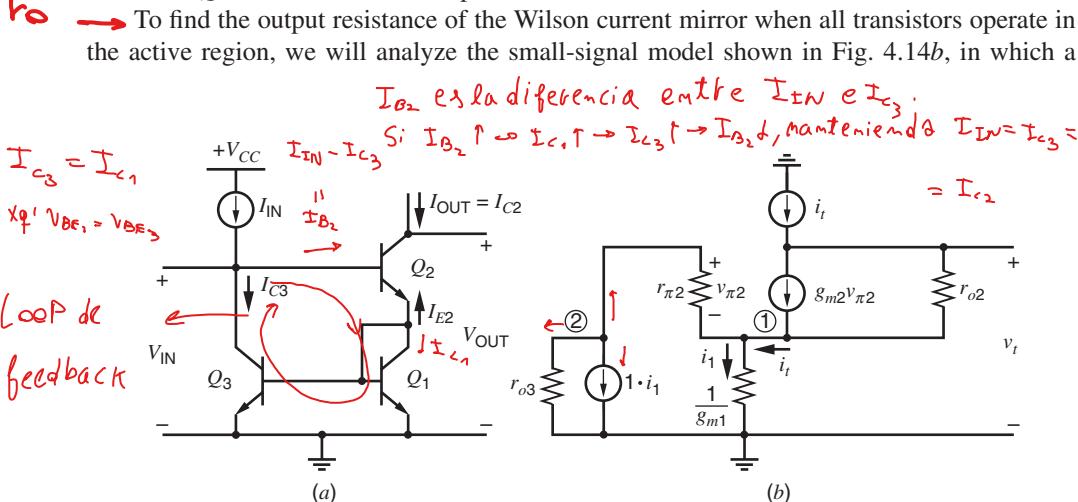


Figure 4.14 (a) Bipolar Wilson current mirror. (b) Small-signal model.

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test current source i_t is applied at the output. Transistors Q_1 and Q_3 form a simple current mirror. Since Q_1 is diode connected, the small-signal resistance from the base of Q_1 to ground is $(1/g_{m1})||r_{\pi1}||r_{\pi3}||r_{o1}$. Assume that an unknown current i_1 flows in this resistance. When $g_{m1}r_{\pi1} \gg 1$, $g_{m1}r_{\pi3} \gg 1$, and $g_{m1}r_{o1} \gg 1$, this resistance is approximately equal to $1/g_{m1}$. Transistor Q_3 could be modeled as a voltage-controlled current source of value $g_{m3}v_{\pi3}$ in parallel with r_{o3} . Since $v_{\pi3} = v_{\pi1} \approx i_1/g_{m1}$, the voltage-controlled current source in the model for Q_3 can be replaced by a current-controlled current source of value $(g_{m3}/g_{m1})(i_1) = 1(i_1)$, as shown in Fig. 4.14b. This model represents the behavior of the simple current mirror directly: The input current i_1 is mirrored to the output by the current-controlled current source.

Using this model, the resulting voltage v_t is

$$v_t = \frac{i_1}{g_{m1}} + (i_t - g_{m2}v_{\pi2})r_{o2} \quad (4.84)$$

To find the relationship between i_1 and $v_{\pi2}$, note that the voltage across r_{o3} is $(i_1/g_{m1} + v_{\pi2})$ and use KCL at node ② in Fig. 4.14b to show that

$$\frac{v_{\pi2}}{r_{\pi2}} + i_1 + \frac{\frac{i_1}{g_{m1}} + v_{\pi2}}{r_{o3}} = 0 \quad (4.85)$$

Rearranging (4.85) gives

$$v_{\pi2} = -i_1 r_{\pi2} \left(\frac{1 + \frac{1}{g_{m1}r_{o3}}}{1 + \frac{r_{\pi2}}{r_{o3}}} \right) \quad (4.86)$$

To find the relationship between i_1 and i_t , use KCL at node ① in Fig. 4.14b to show that

$$i_t = i_1 - \frac{v_{\pi2}}{r_{\pi2}} \quad (4.87)$$

Substituting (4.86) into (4.87) and rearranging gives

$$i_1 = \frac{i_t}{1 + \left(\frac{1 + \frac{1}{g_{m1}r_{o3}}}{1 + \frac{r_{\pi2}}{r_{o3}}} \right)} \quad (4.88)$$

Substituting (4.88) into (4.86) and rearranging gives

$$v_{\pi2} = -i_t r_{\pi2} \left(\frac{1 + \frac{1}{g_{m1}r_{o3}}}{2 + \frac{r_{\pi2}}{r_{o3}} + \frac{1}{g_{m1}r_{o3}}} \right) \quad (4.89)$$

Substituting (4.88) and (4.89) into (4.84) and rearranging gives

$$R_o = \frac{v_t}{i_t} = \frac{1}{g_{m1} \left[1 + \left(\frac{1 + \frac{1}{g_{m1}r_{o3}}}{1 + \frac{r_{\pi2}}{r_{o3}}} \right) \right]} + r_{o2} + \frac{g_{m2}r_{\pi2}r_{o2} \left(1 + \frac{1}{g_{m1}r_{o3}} \right)}{2 + \frac{r_{\pi2}}{r_{o3}} + \frac{1}{g_{m1}r_{o3}}} \quad (4.90)$$

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If $r_{o3} \rightarrow \infty$, the small-signal current that flows in the collector of Q_3 is equal to i_1 and (4.90) reduces to

$$\text{Simplifica todo} \quad R_o = \frac{1}{g_m 1(2)} + r_{o2} + \frac{g_m 2 r_{\pi 2} r_{o2}}{2} \simeq \frac{\beta_0 r_{o2}}{2} \quad (4.91)$$

This result is the same as (4.38) for the cascode current mirror. In the cascode current mirror, the small-signal current that flows in the base of Q_2 is mirrored through Q_3 to Q_1 so that the small-signal base and emitter currents leaving Q_2 are approximately equal. On the other hand, in the Wilson current mirror, the small-signal current that flows in the emitter of Q_2 is mirrored through Q_1 to Q_3 and then flows in the base of Q_2 . Although the cause and effect relationship here is opposite of that in a cascode current mirror, the output resistance is unchanged because the small-signal base and emitter currents leaving Q_2 are still forced to be equal. Therefore, the small-signal collector current of Q_2 that flows because of changes in the output voltage still splits into two equal parts with half flowing in $r_{\pi 2}$.

For the purpose of dc analysis, we assume that $V_A \rightarrow \infty$ and that the transistors are identical. Then the input voltage is

$$V_{IN} = V_{CE3} = V_{BE1} + V_{BE2} = 2V_{BE(on)} \quad (4.92)$$

which is the same as in (4.40) for a cascode current mirror. Also, the minimum output voltage for which both transistors in the output branch operate in the forward-active region is

$$V_{OUT(min)} = V_{CE1} + V_{CE2(sat)} = V_{BE(on)} + V_{CE2(sat)} \quad (4.93)$$

The result in (4.93) is the same as in (4.41) for a cascode current mirror.

To find the systematic gain error, start with KCL at the collector of Q_1 to show that

$$-I_{E2} = I_{C1} + I_{B1} + I_{B3} = I_{C1} \left(1 + \frac{1}{\beta_F} \right) + \frac{I_{C3}}{\beta_F} \quad (4.94)$$

Since we assumed that the transistors are identical and $V_A \rightarrow \infty$,

$$I_{C3} = I_{C1} \quad (4.95)$$

Substituting (4.95) into (4.94) gives

$$-I_{E2} = I_{C1} \left(1 + \frac{2}{\beta_F} \right) \quad (4.96)$$

Using (4.96), the collector current of Q_2 is then

$$I_{C2} = -I_{E2} \left(\frac{\beta_F}{1 + \beta_F} \right) = I_{C1} \left(1 + \frac{2}{\beta_F} \right) \left(\frac{\beta_F}{1 + \beta_F} \right) \quad (4.97)$$

Rearranging (4.97) we obtain

$$I_{C1} = I_{C2} \left[\frac{1}{\left(1 + \frac{2}{\beta_F} \right) \left(\frac{\beta_F}{1 + \beta_F} \right)} \right] \quad (4.98)$$

From KCL at the base of Q_2 ,

$$I_{C3} = I_{IN} - \frac{I_{C2}}{\beta_F} \quad (4.99)$$

Inserting (4.98) and (4.99) into (4.95), we find that

$$I_{\text{OUT}} = I_{C2} = I_{\text{IN}} \left(1 - \frac{2}{\beta_F^2 + 2\beta_F + 2} \right) = \frac{I_{\text{IN}}}{1 + \frac{2}{\beta_F (\beta_F + 2)}} \quad (4.100)$$

In the configuration shown in Fig. 4.14a, the systematic gain error arising from finite output resistance is not zero because Q_3 and Q_1 operate with collector-emitter voltages that differ by the base-emitter voltage of Q_2 . With finite V_A and finite β_F ,

$$\begin{aligned} I_{\text{OUT}} &\simeq I_{\text{IN}} \left(1 - \frac{2}{\beta_F^2 + 2\beta_F + 2} \right) \left(1 + \frac{V_{CE1} - V_{CE3}}{V_A} \right) \\ &\simeq I_{\text{IN}} \left(1 - \frac{2}{\beta_F^2 + 2\beta_F + 2} \right) \left(1 - \frac{V_{BE2}}{V_A} \right) \end{aligned} \quad (4.101)$$

Therefore, the systematic gain error is

$$\epsilon \simeq - \left(\frac{2}{\beta_F^2 + 2\beta_F + 2} + \frac{V_{BE2}}{V_A} \right) \quad (4.102)$$

Comparing (4.102) to (4.49) shows two key points. First, the systematic gain error arising from finite β_F in a Wilson current mirror is much less than in a cascode current mirror. Second, the systematic gain error arising from finite output resistance is worse in the Wilson current mirror shown in Fig. 4.14a than in the cascode current mirror shown in Fig. 4.9. However, this limitation is not fundamental because it can be overcome by introducing a new diode-connected transistor between the collector of Q_3 and the base of Q_2 to equalize the collector-emitter voltages of Q_3 and Q_1 .

4.2.6.2 MOS

Wilson current mirrors are also used in MOS technology, as shown in Fig. 4.15. Ignoring M_4 , the circuit operation is essentially identical to the bipolar case with $\beta_F \rightarrow \infty$. One way to calculate the output resistance is to let $r_{\pi 2} \rightarrow \infty$ in (4.90), which gives

$$R_o = \frac{1}{g_{m1}} + r_{o2} + g_{m2}r_{o2} \left(1 + \frac{1}{g_{m1}r_{o3}} \right) r_{o3} \simeq (1 + g_{m2}r_{o3})r_{o2} \quad (4.103)$$

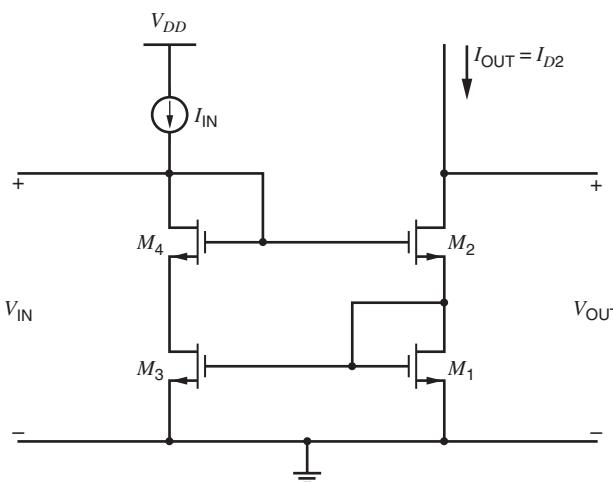


Figure 4.15 Improved MOS Wilson current mirror with an additional device such that the drain voltages of M_1 and M_3 are equal.

Since the calculation in (4.103) is based on the small-signal model for the bipolar Wilson current mirror in Fig. 4.14b, it ignores the body effect in transistor M_2 . Repeating the analysis with a body-effect generator in parallel with r_{o2} gives

$$R_o \simeq (2 + g_{m2}r_{o3})r_{o2} \quad (4.104)$$

The body effect on M_2 has little effect on (4.104) because M_1 is diode connected and therefore the voltage from the source of M_2 to ground is almost constant.

Although $\beta_F \rightarrow \infty$ for MOS transistors, the systematic gain error is not zero without M_4 because the drain-source voltage of M_3 differs from that of M_1 by the gate-source voltage of M_2 . Therefore, without M_4 ,

$$\epsilon = \frac{V_{DS1} - V_{DS3}}{V_A} = -\frac{V_{GS2}}{V_A} \quad (4.105)$$

Transistor M_4 is inserted in series with M_3 to equalize the drain-source voltages of M_3 and M_1 so that

$$\epsilon \simeq 0 \quad (4.106)$$

With M_4 , the output resistance is still given by (4.104) if all transistors operate in the active region. Also, insertion of M_4 does not change either the minimum output voltage for which (4.104) applies or the input voltage. Ignoring body effect and assuming equal overdrives on all transistors, the minimum output voltage is

$$V_{OUT(\min)} = V_{GS1} + V_{ov2} = V_t + 2V_{ov} \quad (4.107)$$

Under the same conditions, the input voltage is

$$V_{IN} = V_{GS1} + V_{GS2} = 2V_t + 2V_{ov} \quad (4.108)$$

4.3 Active Loads

4.3.1 Motivation

In differential amplifiers of the type described in Chapter 3, resistors are used as the load elements. For example, consider the differential amplifier shown in Fig. 3.45. For this circuit, the differential-mode (dm) voltage gain is

$$A_{dm} = -g_m R_C \quad (4.109)$$

Large gain is often desirable because it allows negative feedback to make the gain with feedback insensitive to variations in the parameters that determine the gain without feedback. This topic is covered in Chapter 8. In Chapter 9, we will show that the required gain should be obtained in as few stages as possible to minimize potential problems with instability. Therefore, maximizing the gain of each stage is important.

Multiplying the numerator and denominator of (4.109) by I gives

$$A_{dm} = -\frac{I(R_C)}{I/g_m} \quad (4.110)$$

With bipolar transistors, let I represent the collector current I_C of each transistor in the differential pair. From (1.91), (4.110) can be rewritten as

$$A_{dm} = -\frac{I_C R_C}{V_T} \quad (4.111)$$

To achieve large voltage gain, (4.111) shows that the $I_C R_C$ product must be made large, which in turn requires a large power-supply voltage. Furthermore, large values of resistance are required when low current is used to limit the power dissipation. As a result, the required die area for the resistors can be large.

A similar situation occurs in MOS amplifiers with resistive loads. Let I represent the drain current I_D of each transistor in the differential pair, and let the resistive loads be R_D . From (1.157) and (1.180), (4.110) can be rewritten as

$$A_{dm} = -\frac{I_D R_D}{(V_{GS} - V_t)/2} = -\frac{2I_D R_D}{V_{ov}} \quad (4.112)$$

Equation 4.112 shows that the $I_D R_D$ product must be increased to increase the gain with constant overdrive. As a result, a large power supply is usually required for large gain, and large resistance is usually required to limit power dissipation. Also, since the overdrive is usually much larger than the thermal voltage, comparing (4.111) and (4.112) shows that the gain of an MOS differential pair is usually much less than the gain of its bipolar counterpart with equal resistive drops. This result stems from the observation that bipolar transistors provide much more transconductance for a given current than MOS transistors provide.

If the power-supply voltage is only slightly larger than the drop on the resistors, the range of common-mode input voltages for which the input transistors would operate in the active region would be severely restricted in both bipolar and MOS amplifiers. To overcome this problem and provide large gain without large power-supply voltages or resistances, the r_o of a transistor can be used as a load element.⁹ Since the load element in such a circuit is a transistor instead of a resistor, the load element is said to be *active* instead of *passive*.

4.3.2 Common-Emitter–Common-Source Amplifier with Complementary Load

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A common-emitter amplifier with *pnp* current-mirror load is shown in Fig. 4.16a. The common-source counterpart with a *p*-channel MOS current-mirror load is shown in Fig. 4.16b. In both cases, there are two output variables: the output voltage, V_{out} , and the output current, I_{out} . The relationship between these variables is governed by both the input transistor and the load transistor. From the standpoint of the input transistor T_1 ,

$$I_{out} = I_{c1} \quad \text{or} \quad I_{out} = I_{d1} \quad (4.113)$$

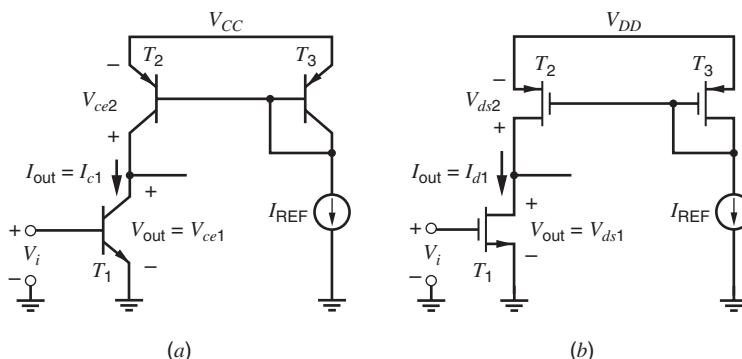


Figure 4.16 (a) Common-emitter amplifier with active load. (b) Common-source amplifier with active load.

and

$$V_{\text{out}} = V_{ce1} \quad \text{or} \quad V_{\text{out}} = V_{ds1} \quad (4.114)$$

Equations 4.113 and 4.114 show that the output I - V characteristics of T_1 can be used directly in the analysis of the relationship between the output variables. Since the input voltage is the base-emitter voltage of T_1 in Fig. 4.16a and the gate-source voltage of T_1 in Fig. 4.16b, the input voltage is the parameter that determines the particular curve in the family of output characteristics under consideration at any point, as shown in Fig. 4.17a.

In contrast, the base-emitter or gate-source voltage of the load transistor T_2 is fixed by diode-connected transistor T_3 . Therefore, only one curve in the family of output I - V characteristics needs to be considered for the load transistor, as shown in Fig. 4.17b. From the standpoint of the load transistor,

$$I_{\text{out}} = -I_{c2} \quad \text{or} \quad I_{\text{out}} = -I_{d2} \quad (4.115)$$

and

$$V_{\text{out}} = V_{CC} + V_{ce2} \quad \text{or} \quad V_{\text{out}} = V_{DD} + V_{ds2} \quad (4.116)$$

Equation 4.115 shows that the output characteristic of the load transistor should be mirrored along the horizontal axis to plot in the same quadrant as the output characteristics of the input

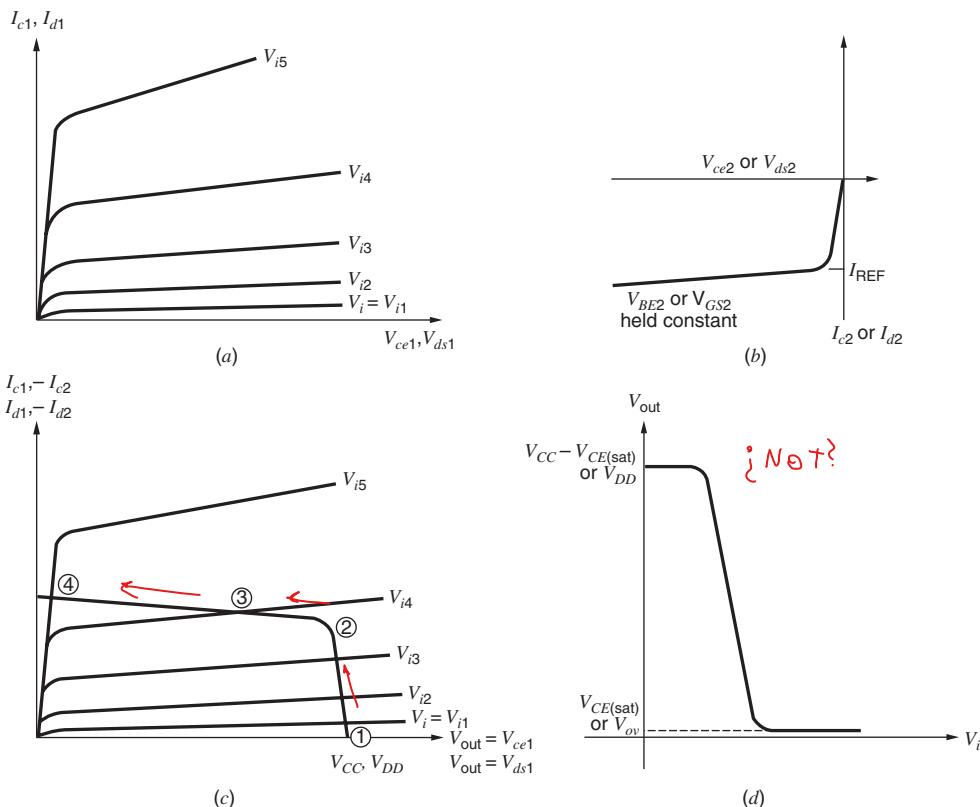


Figure 4.17 (a) I - V characteristics of the input transistor. (b) I - V characteristic of the active load. (c) I - V characteristics with load characteristic superimposed. (d) dc transfer characteristic of common-emitter or common-source amplifier with current-mirror load.

transistor. Equation 4.116 shows that the load curve should be shifted to the right by an amount equal to the power-supply voltage.

We now consider the dc transfer characteristic of the circuits. Initially, assume that $V_i = 0$. Then the input transistor is turned off, and the load is saturated in the bipolar case and linear in the MOS case, corresponding to point ① in Fig. 4.17c. As V_i is increased, the input transistor eventually begins to conduct current but the load remains saturated or linear until point ② is reached. Here the load enters the active region and a small further increase in V_i moves the operating point through point ③ to point ④, where the input transistor saturates in the bipolar case or enters the linear region in the MOS case. The change in V_i required to move from point ② to point ④ is small because the slopes of the output I - V characteristics in the active region are small for both transistors. The transfer curve (V_{out} as a function of V_i) is sketched in Fig. 4.17d.

A key point of this analysis is that the slope of the output characteristic is not constant, which is important because the slope is the gain of the amplifier. Since the gain of the amplifier depends on the input voltage, the amplifier is nonlinear in general, causing distortion to appear in the amplifier output. For low V_i , the output is high and the gain is low because the load transistor does not operate in the active region. Similarly, for large V_i , the output is low and the gain is low because the input transistor does not operate in the active region. To minimize distortion while providing gain, the amplifier should be operated in the intermediate region of V_i , where all transistors operate in the active region. The range of outputs for which all transistors operate in the active region should be maximized to use the power-supply voltage to the maximum extent. The active loads in Fig. 4.16 maintain high incremental output resistance as long as the drop across the load is more than $V_{OUT(min)}$ of the current mirror, which is $|V_{CE2(sat)}|$ in the bipolar case and $|V_{ov2}|$ in the MOS case here. Therefore, minimizing $V_{OUT(min)}$ of the mirror maximizes the range of outputs over which the amplifier provides high and nearly constant gain. In contrast, an ideal passive load requires a large voltage drop to give high gain, as shown in (4.111) and (4.112). As a result, the range of outputs for which the gain is high and nearly constant is much less than with an active load. *→ ventaja de la C.A.*

The gain at any output voltage can be found by finding the slope in Fig. 4.17d. In general, this procedure requires writing equations for the various curves in all of Fig. 4.17. Although this process is required to study the nonlinear behavior of the circuits, it is so complicated analytically that it is difficult to carry out for more than just a couple of transistors at a time. Furthermore, after completing such a large-signal analysis, the results are often so complicated that the effects of the key parameters are difficult to understand, increasing the difficulty of designing with these results. Since we are ultimately interested in being able to analyze and design circuits with a large number of transistors, we will concentrate on the small-signal analysis, which is much simpler to carry out and interpret than the large-signal analysis. Unfortunately, the small-signal analysis provides no information about nonlinearity because it assumes that all transistor parameters are constant.

The primary characteristics of interest in the small-signal analysis here are the voltage gain and output resistance when both devices operate in the active region. The small-signal equivalent circuit is shown in Fig. 4.18. It is drawn for the bipolar case but applies for the MOS case as well when $r_{\pi 1} \rightarrow \infty$ and $r_{\pi 2} \rightarrow \infty$ because $\beta_0 \rightarrow \infty$. Since I_{REF} in Fig. 4.16 is assumed constant, the large-signal base-emitter or gate-source voltage of the load transistor is constant. Therefore, the small-signal base-emitter or gate-source voltage of the load transistor, v_2 , is zero. As a result, the small-signal voltage-controlled current $g_{m2}v_2 = 0$. To find the output resistance of the amplifier, we set the input to zero. Therefore, $v_1 = 0$ and $g_{m1}v_1 = 0$, and the output resistance is

$$R_o = r_{o1} || r_{o2} \quad (4.117)$$

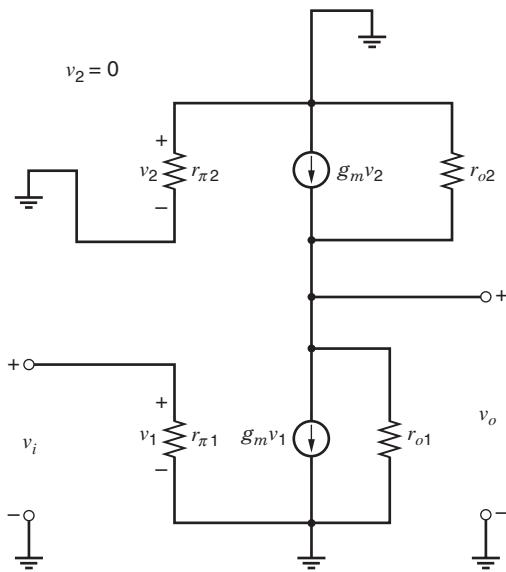


Figure 4.18 Small-signal equivalent circuit for common-emitter amplifier with active load.

Equation 4.117 together with (1.112) and (1.194) show that the output resistance is inversely proportional to the current in both the bipolar and MOS cases.

Since $v_2 = 0$, $g_{m1}v_1$ flows in $r_{o1}||r_{o2}$ and

$$A_v = -g_{m1}(r_{o1}||r_{o2}) \quad (4.118)$$

Substituting (1.91) and (1.112) into (4.118) gives for the bipolar case,

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$$A_v = -\frac{1}{\frac{V_T}{V_{A1}} + \frac{V_T}{V_{A2}}} \quad (4.119)$$

Equation 4.119 shows that the gain is independent of the current in the bipolar case because the transconductance is proportional to the current while the output resistance is inversely proportional to the current. Typical values for this voltage gain are in the 1000 to 2000 range. Therefore, the actively loaded bipolar stage provides very high voltage gain.

In contrast, (1.180) shows that the transconductance is proportional to the square root of the current in the MOS case assuming square-law operation. Therefore, the gain in (4.118) is inversely proportional to the square root of the current. With channel lengths less than 1 μm , however, the drain current is almost linearly related to the gate-source voltage, as shown in (1.224). Therefore, the transconductance is almost constant, and the gain is inversely proportional to the current with very short channel lengths. Furthermore, typical values for the voltage gain in the MOS case are between 10 and 100, which is much less than with bipolar transistors.

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4.3.3 Common-Emitter-Common-Source Amplifier with Depletion Load

Actively loaded gain stages using MOS transistors can be realized in processes that include only *n*-channel or only *p*-channel transistors if depletion devices are available. A depletion transistor is useful as a load element because it behaves like a current source when the transistor operates in the active region with the gate shorted to the source.

The I - V characteristic of an n -channel MOS depletion-load transistor is illustrated in Fig. 4.19. Neglecting body effect, the device exhibits a very high output resistance (equal to the device r_o) as long as the device operates in the active region. When the body effect is included, the resistance seen across the device drops to approximately $1/g_{mb}$. A complete gain stage is shown in Fig. 4.20 together with its dc transfer characteristic. The small-signal equivalent model when both transistors operate in the active region is shown in Fig. 4.21. From this circuit, we find that the gain is

$$\frac{v_o}{v_i} = -g_{m1} \left(r_{o1} || r_{o2} || \frac{1}{g_{mb2}} \right) \simeq -\frac{g_{m1}}{g_{mb2}} \quad (4.120)$$

For a common-source amplifier with a depletion load, rearranging (4.120) and using (1.180) and (1.200) gives

$$\frac{v_o}{v_i} \simeq -\frac{g_{m1}}{\frac{g_{mb2}}{g_{m2}}} = -\frac{1}{\chi} \sqrt{\frac{(W/L)_1}{(W/L)_2}} \quad (4.121)$$

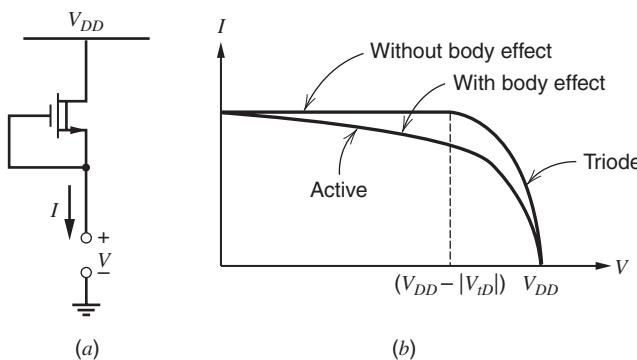


Figure 4.19 (a) n -channel depletion-mode load transistor. (b) I - V characteristic.

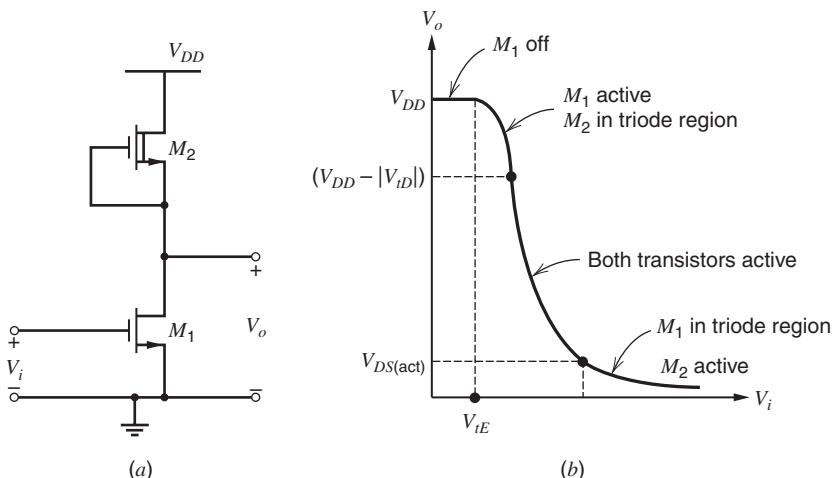


Figure 4.20 (a) Common-source amplifier with depletion-mode transistor load. (b) dc transfer characteristic.

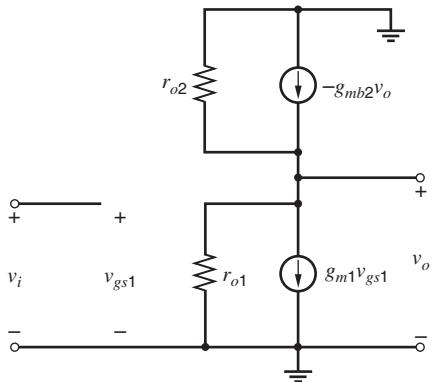


Figure 4.21 Small-signal equivalent circuit of the common-source amplifier with depletion load, including the body effect in the load and the channel-length modulation in the load and the common-source device.

From (1.196) and (1.141),

$$\frac{1}{\chi} = 2\sqrt{2\phi_f C_{ox}} \sqrt{\frac{1 + V_{SB}/(2\phi_f)}{2q\epsilon N_A}} \quad (4.122)$$

Since χ depends on $V_o = V_{SB}$, the incremental voltage gain varies with output voltage, giving the slope variation shown in the active region of Fig. 4.20b.

Equation 4.120 applies for either a common-emitter or common-source driver with a depletion MOS load. If this circuit is implemented in a *p*-well CMOS technology, M_2 can be built in an isolated well, which can be connected to the source of M_2 . Since this connection sets the source-body voltage in the load transistor to zero, it eliminates the body effect. Setting $g_{mb2} = 0$ in (4.120) gives

$$\frac{v_o}{v_i} = -g_m r_{o1} || r_{o2} \quad (4.123)$$

Although the gain predicted in (4.123) is much higher than in (4.120), this connection reduces the bandwidth of the amplifier because it adds extra capacitance (from the well of M_2 to the substrate of the integrated circuit) to the amplifier output node.

4.3.4 Common-Emitter-Common-Source Amplifier with Diode-Connected Load

In this section, we examine the common-emitter/source amplifier with diode-connected load as shown in MOS form in Fig. 4.22. Since the load is diode connected, the load resistance is no more than the reciprocal of the transconductance of the load. As a result, the gain of this circuit is low, and it is often used in wideband amplifiers that require low gain.

For input voltages that are less than one threshold voltage, transistor M_1 is off and no current flows in the circuit. When the input voltage exceeds a threshold, transistor M_1 turns on, and the circuit provides amplification. Assume that both transistors operate in the active region. From (1.157), the drain currents of M_1 and M_2 are

$$I_1 = \frac{k'}{2} \left(\frac{W}{L} \right)_1 (V_{gs1} - V_{t1})^2 \quad (4.124)$$

and

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$$I_2 = \frac{k'}{2} \left(\frac{W}{L} \right)_2 (V_{gs2} - V_{t2})^2 \quad (4.125)$$

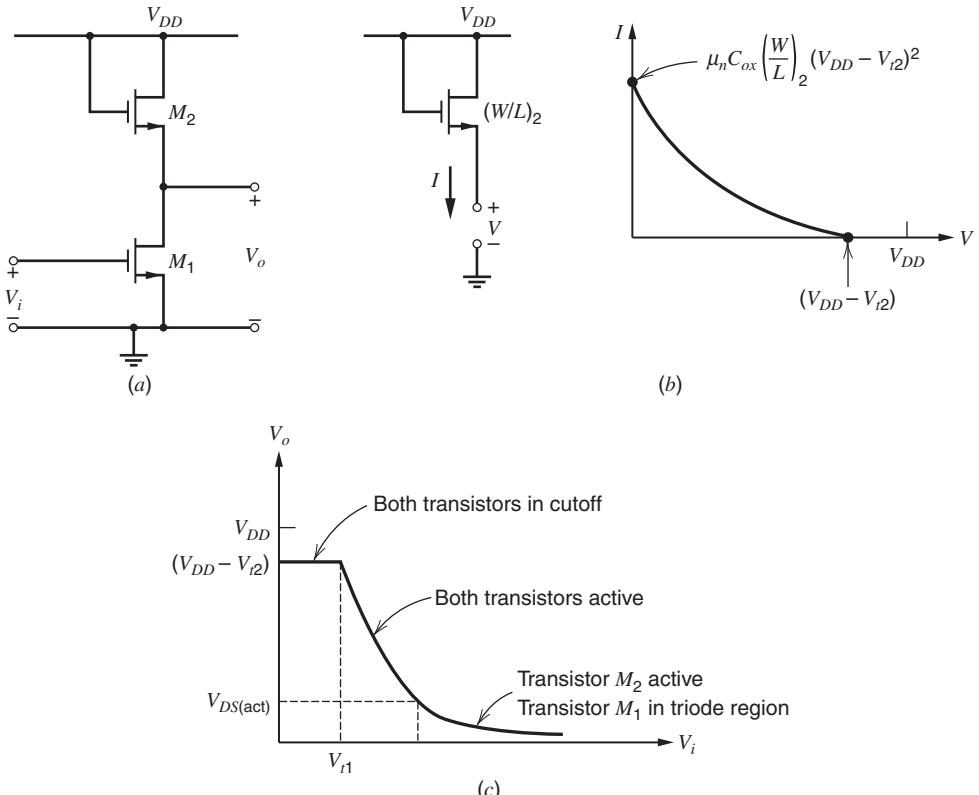


Figure 4.22 (a) Common-source amplifier with enhancement-mode load. (b) I-V characteristic of load transistor. (c) Transfer characteristic of the circuit.

From KVL in Fig. 4.22,

$$V_o = V_{DD} - V_{gs2} \quad (4.126)$$

Solving (4.125) for V_{gs2} and substituting into (4.126) gives

Mirá el circuito, q il

$$V_o = V_{DD} - V_{t2} - \sqrt{\frac{2I_2}{k'(W/L)_2}} \quad (4.127)$$

Since $I_2 = I_1$, (4.127) can be rewritten as

$$V_o = V_{DD} - V_{t2} - \sqrt{\frac{2I_1}{k'(W/L)_2}} \quad (4.128)$$

Substituting (4.124) into (4.128) with $V_{gs1} = V_i$ gives

$$V_o = V_{DD} - V_{t2} - \sqrt{\frac{(W/L)_1}{(W/L)_2} (V_i - V_{t1})} \quad (4.129)$$

Equation 4.129 shows that the slope of the transfer characteristic is the square root of the aspect ratios, assuming that the thresholds are constant. Since the slope of the transfer characteristic is the gain of the amplifier, the gain is constant and the amplifier is linear for a wide range

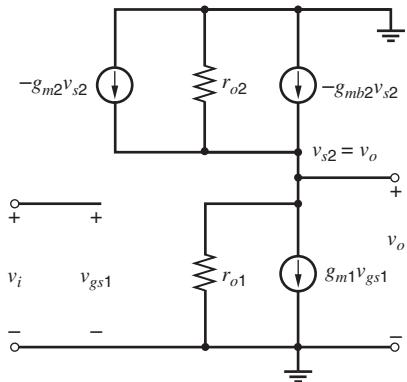


Figure 4.23 Small-signal equivalent circuit for the common-source amplifier with enhancement-mode load, including output resistance and body effect in the load.

of inputs if the thresholds are constant. This amplifier is useful in implementing broadband, low-gain amplifiers with high linearity.

Equation 4.129 holds when both transistors operate in the active region and when channel-length modulation and body effect are negligible. In practice, the requirement that both transistors operate in the active region leads to an important performance limitation in enhancement-load inverters. The load device remains in the active region only if the drain-source voltage of the load is at least a threshold voltage. For output voltages more positive than $V_{DD} - V_{T2}$, the load transistor enters the cutoff region and carries no current. Therefore, the amplifier is incapable of producing an output more positive than one threshold voltage below the positive supply. Also, in practice, channel-length modulation and body effect reduce the gain as shown in the following small-signal analysis.

The small-signal voltage gain can be determined by using the small-signal equivalent circuit of Fig. 4.23, in which both the body effect and the output resistance of the two transistors have been included. From KCL at the output node,

$$g_m1 v_i + \frac{v_o}{r_{o1}} + \frac{v_o}{r_{o2}} + g_m2 v_o + g_{mb2} v_o = 0 \quad (4.130)$$

Rearranging (4.130) gives

$$\begin{aligned} \frac{v_o}{v_i} &= -g_m1 \left(\frac{1}{g_m2} \left| \frac{1}{g_{mb2}} \right| |r_{o1}| |r_{o2}| \right) \\ &= -\frac{g_m1}{g_m2} \left(\frac{1}{1 + \frac{g_{mb2}}{g_m2} + \frac{1}{g_m2 r_{o1}} + \frac{1}{g_m2 r_{o2}}} \right) \end{aligned} \quad (4.131)$$

If $g_m2/g_{mb2} \gg 1$, $g_m2 r_{o1} \gg 1$, and $g_m2 r_{o2} \gg 1$,

$$\frac{v_o}{v_i} \simeq -\frac{g_m1}{g_m2} = -\sqrt{\frac{(W/L)_1}{(W/L)_2}} \quad (4.132)$$

as in (4.129). For practical device geometries, this relationship limits the maximum voltage gain to values on the order of 10 to 20.

The bipolar counterpart of the circuit in Fig. 4.22 is a common-emitter amplifier with a diode-connected load. The magnitude of its gain would be approximately equal to the ratio of the transconductances, which would be unity. However, the current that would flow in this circuit would be extremely large for inputs greater than $V_{be(on)}$ because the collector current in a bipolar transistor is an exponential function of its base-emitter voltage. To limit the current

but maintain unity gain, equal-value resistors can be placed in series with the emitter of each transistor. Alternatively, the input transistors can be replaced by a differential pair, where the current is limited by the tail current source. In this case, emitter degeneration is used in the differential pair to increase the range of inputs for which all transistors operate in the active region, as in Fig. 3.49. In contrast, source degeneration is rarely used in MOS differential pairs because their transconductance and linear range can be controlled through the device aspect ratios.

4.3.5 Differential Pair with Current-Mirror Load

4.3.5.1 Large-Signal Analysis

A straightforward application of the active-load concept to the differential pair would yield the circuit shown in Fig. 4.24a. Assume at first that all *n*-channel transistors are identical

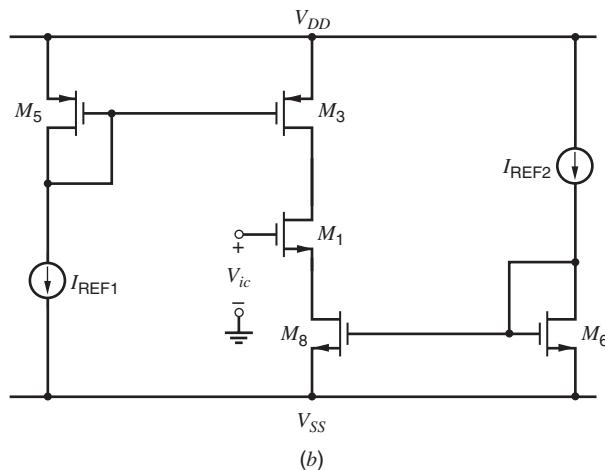
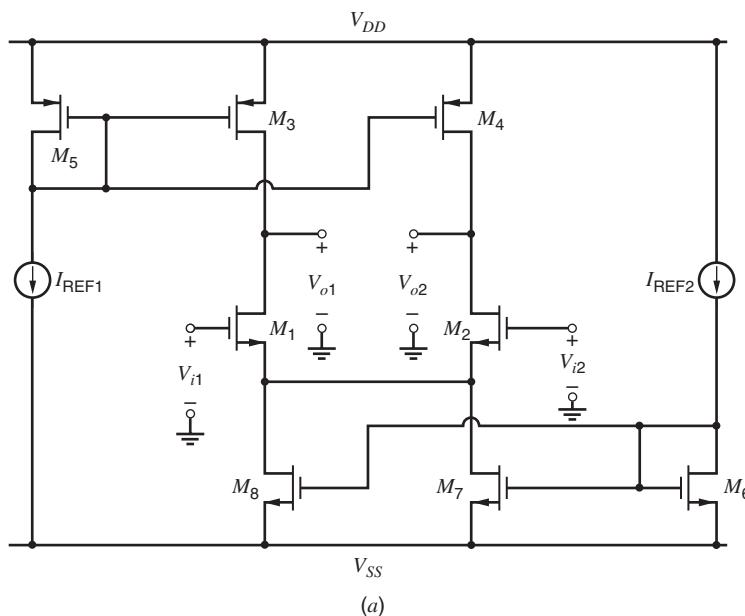


Figure 4.24 (a) Differential pair with active load. (b) Common-mode half circuit for differential pair with active load.

and that all *p*-channel transistors are identical. Then the differential-mode half circuit for this differential pair is just a common-source amplifier with an active-load, as in Fig. 4.16*b*. Thus the differential-mode voltage gain is large when all the transistors are biased in the active region. The circuit as it stands, however, has the drawback that the quiescent value of the common-mode output voltage is very sensitive to changes in the drain currents of M_3 , M_4 , M_7 , and M_8 . As a result, some transistors may operate in or near the triode region, reducing the differential gain or the range of outputs for which the differential gain is high.

This fact is illustrated by the dc common-mode half-circuit shown in Fig. 4.24*b*. In the common-mode half circuit, the combination of M_1 , M_6 , and M_8 form a cascode current mirror, which is connected to the simple current mirror formed by M_3 and M_5 . If all transistors operate in the active region, M_3 pushes down a current about equal to I_{REF1} , and M_8 pulls down a current about equal to I_{REF2} . KCL requires that the current in M_3 must be equal to the current in M_8 . If $I_{REF2} = I_{REF1}$, KCL can be satisfied while all transistors operate in the active region. In practice, however, I_{REF2} is not exactly equal to I_{REF1} , and the current mirrors contain nonzero mismatch, causing changes in the common-mode output to satisfy KCL. Since the output resistance of each current mirror is high, the required change in the common-mode output voltage can be large even for a small mismatch in reference currents or transistors, and one or more transistors can easily move into or near the triode region. For example, suppose that the current pushed down by M_3 when it operates in the active region is more than the current pulled down by M_8 when it operates in the active region. Then the common-mode output voltage must rise to reduce the current in M_3 . If the common-mode output voltage rises within V_{ov3} of V_{DD} , M_3 operates in the triode region. Furthermore, even if all the transistors continue to be biased in the active region, any change in the common-mode output voltage from its desired value reduces the range of outputs for which the differential gain is high.

Since M_1 and M_2 act as cascodes for M_7 and M_8 , shifts in the common-mode input voltage have little effect on the common-mode output unless the inputs become low enough that M_7 and M_8 are forced to operate in the triode region. Therefore, feedback to the inputs of the circuit in Fig. 4.24*a* is not usually adequate to overcome the common-mode bias problem. Instead, this problem is usually overcome in practice through the use of a separate common-mode feedback circuit, which either adjusts the sum of the currents in M_3 and M_4 to be equal to the sum of the currents in M_7 and M_8 or vice versa for a given common-mode output voltage. This topic is covered in Chapter 12.

An alternative approach that avoids the need for common-mode feedback is shown in Fig. 4.25. For simplicity in the bipolar circuit shown in Fig. 4.25*a*, assume that $\beta_F \rightarrow \infty$. The circuit in Fig. 4.25*b* is the MOS counterpart of the bipolar circuit in Fig. 4.25*a* because each *npn* and *pnp* transistor has been replaced by *n*-channel and *p*-channel MOS transistors, respectively. Then under ideal conditions in both the bipolar and MOS circuits, the active load is a current mirror that forces the current in its output transistor T_4 to equal the current in its input transistor T_3 . Since the sum of the currents in both transistors of the active load must equal I_{TAIL} by KCL, $I_{TAIL}/2$ flows in each side of the active load. Therefore, these circuits eliminate the common-mode bias problem by allowing the currents in the active load to be set by the tail current source. Furthermore, these circuits each provide a single output with much better rejection of common-mode input signals than a standard resistively loaded differential pair with the output taken off one side only. Although these circuits can be analyzed from a large-signal standpoint, we will concentrate on the small-signal analysis for simplicity.

4.3.5.2 Small-Signal Analysis

We will analyze the low-frequency small-signal behavior of the bipolar circuit shown in Fig. 4.25*a* because these results cover both the bipolar and MOS cases by letting $\beta_0 \rightarrow \infty$ and $r_\pi \rightarrow \infty$. Key parameters of interest in this circuit include the small-signal

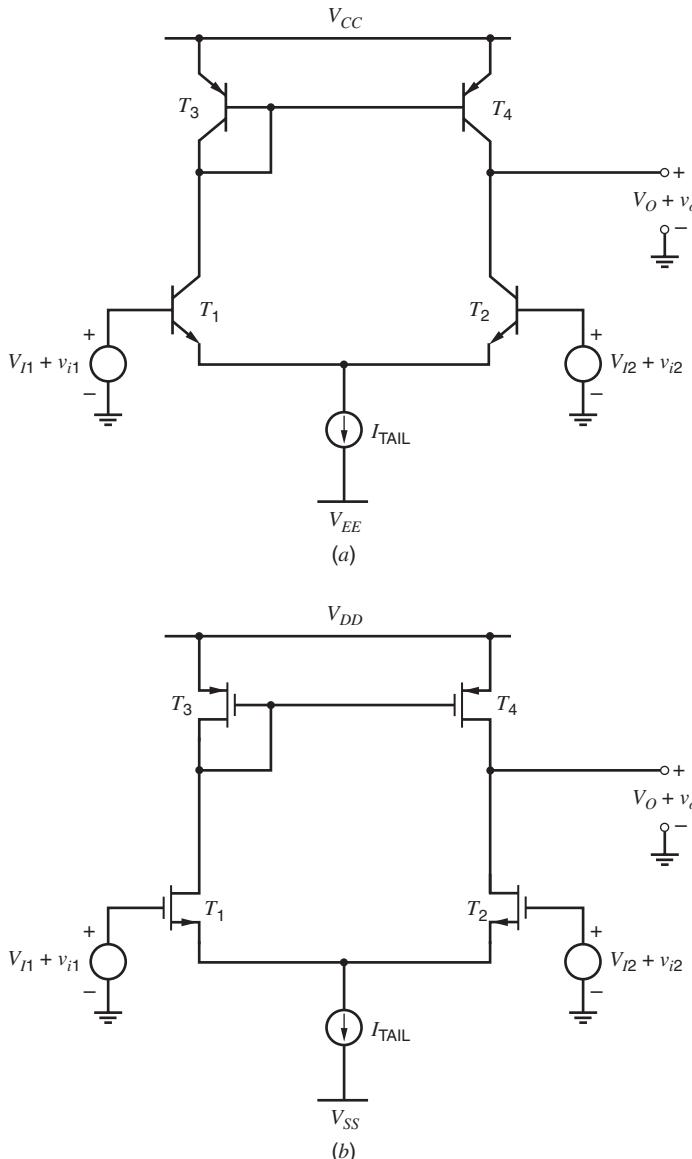


Figure 4.25 (a) Emitter-coupled pair with current-mirror load. (b) Source-coupled pair with current-mirror load (MOS counterpart).

transconductance and output resistance. (The product of these two quantities gives the small-signal voltage gain with no load.) Since only one transistor in the active load is diode connected, the circuit is not symmetrical and a half-circuit approach is not useful. Therefore, we will analyze the small-signal model of this circuit directly. Assume that all transistors operate in the active region with $r_\mu \rightarrow \infty$ and $r_b = 0$. Let r_{tail} represent the output resistance of the tail current source I_{TAIL} . The resulting small-signal circuit is shown in Fig. 4.26a.

Since T_3 and T_4 form a current mirror, we expect the mirror output current to be approximately equal to the mirror input current. Therefore, we will write

$$g_{m4}v_3 = i_3(1 - \epsilon_m) \quad (4.133)$$

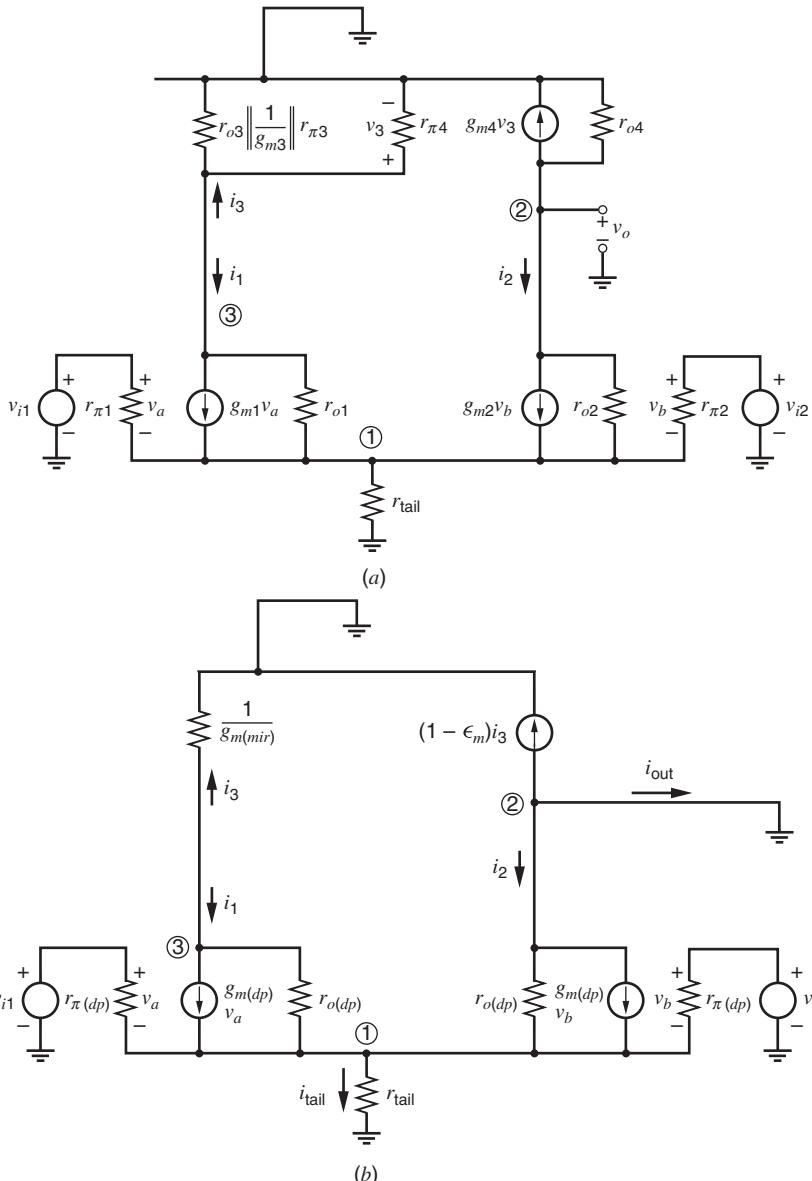


Figure 4.26 (a) Small-signal equivalent circuit, differential pair with current-mirror load. (b) Simplified drawing of small-signal model of differential pair with current-mirror load.

where \$\epsilon_m\$ is the systematic gain error of the current mirror calculated from small-signal parameters. Let \$r_3\$ represent the total resistance connected between the base or gate of \$T_3\$ and the power supply. Then \$r_3\$ is the parallel combination of \$1/g_{m3}\$, \$r_{\pi3}\$, \$r_{\pi4}\$, and \$r_{o3}\$. Under the simplifying assumptions that \$\beta_0 \gg 1\$ and \$g_{mr} \gg 1\$, this parallel combination is approximately equal to \$1/g_{m3}\$. Then the drop across \$r_{\pi4}\$ is

$$v_3 = i_3 r_3 \simeq \frac{i_3}{g_{m3}} \quad (4.134)$$

We will also assume that the two transistors in the differential pair match perfectly and operate with equal dc currents, as do the two transistors in the current-mirror load. Then \$g_{m(dp)} = g_{m1}\$

$= g_{m2}$, $g_{m(mir)} = g_{m3} = g_{m4}$, $r_{\pi(dp)} = r_{\pi1} = r_{\pi2}$, $r_{\pi(mir)} = r_{\pi3} = r_{\pi4}$, $r_{o(dp)} = r_{o1} = r_{o2}$, and $r_{o(mir)} = r_{o3} = r_{o4}$. From (4.134), the resulting voltage-controlled current $g_{m4}v_3$ is

$$g_{m4}v_3 = g_{m(mir)}v_3 \simeq g_{m(mir)} \frac{i_3}{g_{m(mir)}} = i_3 \quad (4.135)$$

Equations 4.133 and 4.135 show that $\epsilon_m \simeq 0$ and thus the active load acts as a current mirror in a small-signal sense, as expected. Using (4.133), the small-signal circuit is redrawn in Fig. 4.26b with the output grounded to find the transconductance. Note that r_{o4} is omitted because it is attached to a small-signal ground on both ends.

From KCL at node ①,

$$(v_{i1} - v_1 + v_{i2} - v_1) \left(\frac{1}{r_{\pi(dp)}} + g_{m(dp)} \right) + \frac{v_3 - v_1}{r_{o(dp)}} - \frac{v_1}{r_{o(dp)} || r_{tail}} = 0 \quad (4.136)$$

where v_1 and v_3 are the voltages to ground from nodes ① and ③. To complete an exact small-signal analysis, KCL equations could also be written at nodes ② and ③, and these KCL equations plus (4.136) could be solved simultaneously. However, this procedure is complicated algebraically and leads to an equation that is difficult to interpret. To simplify the analysis, we will assume at first that $r_{tail} \rightarrow \infty$ and $r_{o(dp)} \rightarrow \infty$ since the transistors are primarily controlled by their base-emitter or gate-source voltages. Then from (4.136)

$$v_1 = \frac{v_{i1} + v_{i2}}{2} = v_{ic} \quad (4.137)$$

where v_{ic} is the common-mode component of the input. Let $v_{id} = v_{i1} - v_{i2}$ represent the differential-mode component of the input. Then $v_{i1} = v_{ic} + v_{id}/2$ and $v_{i2} = v_{ic} - v_{id}/2$, and the small-signal collector or drain currents

$$i_1 = g_{m(dp)}(v_{i1} - v_1) = \frac{g_{m(dp)}v_{id}}{2} \quad (4.138)$$

and

$$i_2 = g_{m(dp)}(v_{i2} - v_1) = -\frac{g_{m(dp)}v_{id}}{2} \quad (4.139)$$

With a resistive load and a single-ended output, only i_2 flows in the output. Therefore, the transconductance for a differential-mode (dm) input with a passive load is

$$G_m[dm] = \frac{i_{out}}{v_{id}} \Big|_{v_{out}=0} = -\frac{i_2}{v_{id}} = \frac{g_{m(dp)}}{2} \quad (4.140)$$

On the other hand, with the active loads in Fig. 4.25, not only i_2 but also most of i_3 flows in the output because of the action of the current mirror, as shown by (4.135). Therefore, the output current in Fig. 4.26b is

$$i_{out} = -(1 - \epsilon_m)i_3 - i_2 \quad (4.141)$$

Assume at first that the current mirror is ideal so that $\epsilon_m = 0$. Then since $i_3 = -i_1$, substituting (4.138) and (4.139) in (4.141) gives

$$i_{out} = g_{m(dp)}v_{id} \quad (4.142)$$

Therefore, with an active load,

$$G_m[dm] = \frac{i_{out}}{v_{id}} \Big|_{v_{out}=0} = g_{m(dp)} \quad (4.143)$$

Equation 4.143 applies for both the bipolar and MOS amplifiers shown in Fig. 4.25. Comparing (4.140) and (4.143) shows that the current-mirror load doubles the differential transconductance

compared to the passive-load case. This result stems from the fact that the current mirror creates a second signal path to the output. (The first path is through the differential pair.) Although frequency response is not analyzed in this chapter, note that the two signal paths usually have different frequency responses, which is often important in high-speed applications.

The key assumptions that led to (4.142) and (4.143) are that the current mirror is ideal so $\epsilon_m = 0$ and that $r_{tail} \rightarrow \infty$ and $r_{o(dp)} \rightarrow \infty$. Under these assumptions, the output current is independent of the common-mode input. In practice, none of these assumptions is exactly true, and the output current depends on the common-mode input. However, this dependence is small because the active load greatly enhances the common-mode rejection ratio of this stage, as shown in Section 4.3.5.3.

Another important parameter of the differential pair with active load is the output resistance. The output resistance is calculated using the circuit of Fig. 4.27, in which a test voltage source v_t is applied at the output while the inputs are connected to small-signal ground. The resulting current i_t has four components. The current in r_{o4} is

$$i_{t1} = \frac{v_t}{r_{o4}} \quad (4.144)$$

The resistance in the emitter or source lead of T_2 is r_{tail} in parallel with the resistance seen looking into the emitter or source of T_1 , which is approximately $1/g_{m1}$. Thus, using (3.99) for a transistor with degeneration, we find that the effective output resistance looking into the collector or drain of T_2 is

$$R_{o2} \simeq r_{o2} \left(1 + g_{m2} \frac{1}{g_{m1}} \right) = 2r_{o2} \quad (4.145)$$

Hence

$$i_{t2} + i_{t4} \simeq \frac{v_t}{2r_{o2}} \quad (4.146)$$

If $r_{tail} \gg 1/g_{m1}$, this current flows into the emitter or source of T_1 , and is mirrored to the output with a gain of approximately unity to produce

$$i_{t3} \simeq i_{t2} + i_{t4} \simeq \frac{v_t}{2r_{o2}} \quad (4.147)$$

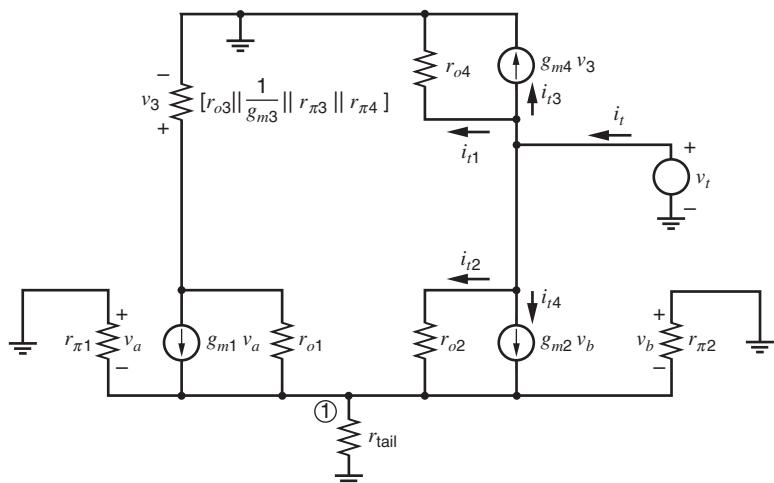


Figure 4.27 Circuit for calculation of the output resistance of the differential pair with current-mirror load.

Thus

$$i_t = i_{t1} + i_{t2} + i_{t3} + i_{t4} \simeq v_t \left(\frac{1}{r_{o4}} + \frac{1}{r_{o2}} \right) \quad (4.148)$$

Since $r_{o2} = r_{o(dp)}$ and $r_{o4} = r_{o(mir)}$,

$$R_o = \frac{v_t}{i_t} \Big|_{\substack{v_{i1}=0 \\ v_{i2}=0}} \simeq \frac{1}{\frac{1}{r_{o(dp)}} + \frac{1}{r_{o(mir)}}} = r_{o(dp)} || r_{o(mir)} \quad (4.149)$$

The result in (4.149) applies for both the bipolar and MOS amplifiers shown in Fig. 4.25. In multistage bipolar amplifiers, the low-frequency gain of the loaded circuit is likely to be reduced by the input resistance of the next stage because the output resistance is high. In contrast, low-frequency loading is probably not an issue in multistage MOS amplifiers because the next stage has infinite input resistance if the input is the gate of an MOS transistor.

Finally, although the source-coupled pair has infinite input resistance, the emitter-coupled pair has finite input resistance because β_0 is finite. If the effects of the r_o of T_2 and T_4 are neglected, the differential input resistance of the actively loaded emitter-coupled pair is simply $2r_{\pi(dp)}$ as in the resistively loaded case. In practice, however, the asymmetry of the circuit together with the high voltage gain cause feedback to occur through the output resistance of T_2 to node (1). This feedback causes the input resistance to differ slightly from $2r_{\pi(dp)}$.

In summary, the actively loaded differential pair is capable of providing differential-to-single-ended conversion, that is, the conversion from a differential voltage to a voltage referenced to the ground potential. The high output resistance of the circuit requires that the next stage must have high input resistance if the large gain is to be realized. A small-signal two-port equivalent circuit for the stage is shown in Fig. 4.28.

4.3.5.3 Common-Mode Rejection Ratio

In addition to providing high voltage gain, the circuits in Fig. 4.25 provide conversion from a differential input signal to an output signal that is referenced to ground. Such a conversion is required in all differential-input, single-ended output amplifiers.

The simplest differential-to-single-ended converter is a resistively loaded differential pair in which the output is taken from only one side, as shown in Fig. 4.29a. In this case, $A_{dm} > 0$, $A_{cm} < 0$, and the output is

$$v_o = -\frac{v_{od}}{2} + v_{oc} = -\frac{A_{dm}v_{id}}{2} + A_{cm}v_{ic} \quad (4.150)$$

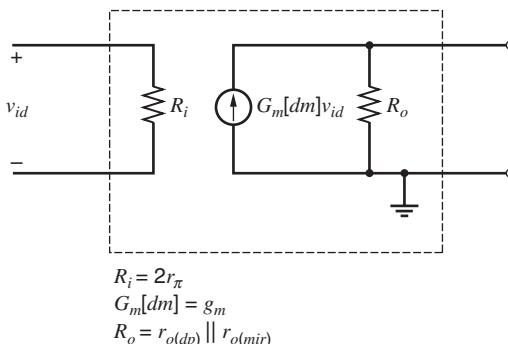


Figure 4.28 Two-port representation of small-signal properties of differential pair with current-mirror load. The effects of asymmetrical input resistance have been neglected.

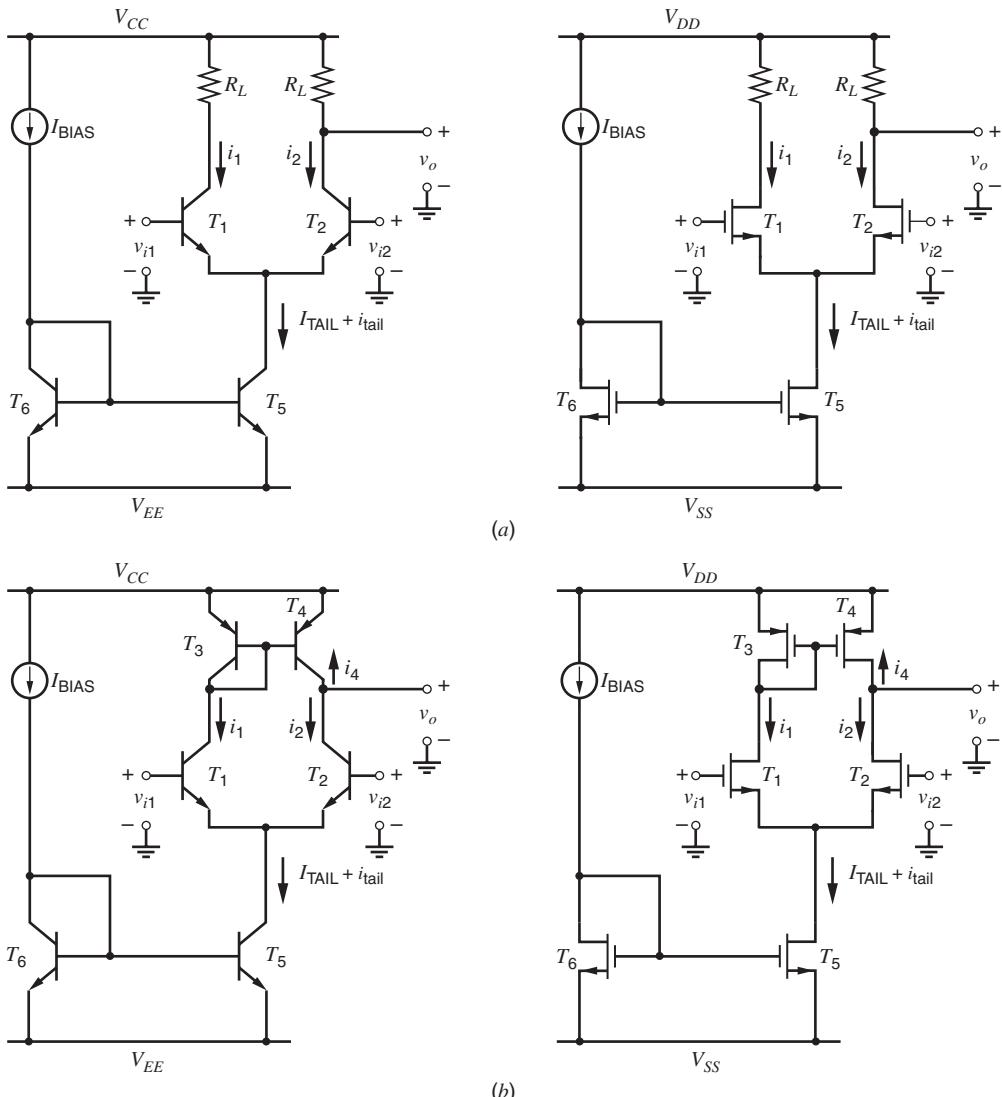


Figure 4.29 Differential-to-single-ended conversion (a) resistively loaded differential pairs and (b) actively loaded differential pairs.

$$v_o = -\frac{A_{dm}}{2} \left(v_{id} - \frac{2A_{cm}}{A_{dm}} v_{ic} \right) = -\frac{A_{dm}}{2} \left(v_{id} + 2 \left| \frac{A_{cm}}{A_{dm}} \right| v_{ic} \right) \quad (4.151)$$

$$= -\frac{A_{dm}}{2} \left(v_{id} + \frac{2v_{ic}}{\text{CMRR}} \right) \quad (4.152)$$

Thus, common-mode signals at the input will cause changes in the output voltage. The common-mode rejection ratio (CMRR) is

$$\text{CMRR} = \left| \frac{A_{dm}}{A_{cm}} \right| = \left| \frac{G_m[\text{dm}]R_o}{G_m[\text{cm}]R_o} \right| = \left| \frac{G_m[\text{dm}]}{G_m[\text{cm}]} \right| \quad (4.153)$$

where the common-mode (cm) transconductance is

$$G_m[cm] = \left. \frac{i_{out}}{v_{ic}} \right|_{v_{out}=0} \quad (4.154)$$

Since the circuits in Fig. 4.29a are symmetrical, a common-mode half circuit can be used to find $G_m[cm]$. The common-mode half circuit is a common-emitter/source amplifier with degeneration. From (3.93) and (3.104),

$$G_m[cm] = -\frac{i_2}{v_{ic}} \simeq -\frac{g_{m(dp)}}{1 + g_{m(dp)}(2r_{tail})} \quad (4.155)$$

where $g_{m(dp)} = g_{m1} = g_{m2}$ and r_{tail} represents the output resistance of the tail current source T_5 . The negative sign appears in (4.155) because the output current is defined as positive when it flows from the output terminal into the small-signal ground to be consistent with the differential case, as in Fig. 4.26b. Equation 4.155 applies for both the bipolar and MOS cases if the base current is ignored in the bipolar case, the body effect is ignored in the MOS case, and r_{o1} and r_{o2} are ignored in both cases. Substituting (4.140) and (4.155) into (4.153) gives

$$\text{CMRR} = \frac{1 + 2g_{m(dp)}r_{tail}}{2} \simeq g_{m(dp)}r_{tail} = g_{m1}r_{o5} \quad (4.156)$$

Equation 4.156 shows that the common-mode rejection ratio here is about half that in (3.193) because the outputs in Fig. 4.29 are taken only from one side of each differential pair instead of from both sides, reducing the differential-mode gain by a factor of two. The result in (4.156) applies for both the bipolar and MOS amplifiers shown in Fig. 4.29a. Because g_{mr_o} is much higher for bipolar transistors than MOS transistors, the CMRR of a bipolar differential pair with resistive load is much higher than that of its MOS counterpart.

On the other hand, the active-load stages shown in Fig 4.29b have common-mode rejection ratios much superior to those of the corresponding circuits in Fig. 4.29a. Assume that the outputs in Fig. 4.29b are connected to small-signal ground to allow calculation of the common-mode transconductance. The small-signal model is the same as shown in Fig. 4.26b with $v_{i1} = v_{i2} = v_{ic}$. For simplicity, let $\beta_0 \rightarrow \infty$ and $r_\pi \rightarrow \infty$ at first. As with a resistive load, changes in the common-mode input will cause changes in the tail bias current i_{tail} because the output resistance of T_5 is finite. If we assume that the currents in the differential-pair transistors are controlled only by the base-emitter or gate-source voltages, the change in the current in T_1 and T_2 is

$$i_1 = i_2 = \frac{i_{tail}}{2} \quad (4.157)$$

If $\epsilon_m = 0$, the gain of the current mirror is unity. Then substituting (4.157) into (4.141) with $i_3 = -i_1$ gives

$$i_{out} = -i_3 - i_2 = i_1 - i_2 = 0 \quad (4.158)$$

As a result,

$$G_m[cm] = \left. \frac{i_{out}}{v_{ic}} \right|_{v_{out}=0} = 0 \quad (4.159)$$

Therefore,

$$\text{CMRR} \rightarrow \infty \quad (4.160)$$

The common-mode rejection ratio in (4.160) is infinite because the change in the current in T_4 cancels that in T_2 even when r_{tail} is finite under these assumptions.

The key assumptions that led to (4.160) are that $r_{o(dp)} \rightarrow \infty$ so $i_1 = i_2$ and that the current mirror is ideal so $\epsilon_m = 0$. In practice, the currents in the differential-pair transistors are not

only controlled by their base-emitter or gate-source voltages, but also to some extent by their collector-emitter or drain-source voltages. As a result, i_1 is not exactly equal to i_2 because of finite $r_{o(dp)}$ in T_1 and T_2 . Furthermore, the gain of the current mirror is not exactly unity, which means that ϵ_m is not exactly zero in practice because of finite $r_{o(mir)}$ in T_3 and T_4 . Finite β_0 also affects the systematic gain error of the current mirror when bipolar transistors are used. For these reasons, the common-mode rejection ratio is finite in practice. However, the use of the active load greatly improves the common-mode rejection ratio compared to the resistive load case, as we will show next.

Suppose that

$$i_1 = i_2(1 - \epsilon_d) \quad (4.161)$$

where ϵ_d can be thought of as the gain error in the differential pair. Substituting (4.161) into (4.141) with $i_3 = -i_1$ gives

$$i_{\text{out}} = i_1(1 - \epsilon_m) - i_2 = i_2((1 - \epsilon_d)(1 - \epsilon_m) - 1) \quad (4.162)$$

Rearranging (4.162) gives

$$i_{\text{out}} = -i_2(\epsilon_d + \epsilon_m - \epsilon_d\epsilon_m) \quad (4.163)$$

If $\epsilon_d \ll 1$ and $\epsilon_m \ll 1$, the product term $\epsilon_d\epsilon_m$ is a second-order error and can be neglected. Therefore,

$$i_{\text{out}} \simeq -i_2(\epsilon_d + \epsilon_m) \quad (4.164)$$

Substituting (4.164) into (4.154) gives

$$G_m[\text{cm}] \simeq -\left(\frac{i_2}{v_{ic}}\right)(\epsilon_d + \epsilon_m) \quad (4.165)$$

Equation 4.165 applies for the active-load circuits shown in Fig. 4.29b; however, the first term has approximately the same value as in the passive-load case. Therefore, we will substitute (4.155) into (4.165), which gives

$$G_m[\text{cm}] \simeq -\left(\frac{g_{m(dp)}}{1 + g_{m(dp)}(2r_{\text{tail}})}\right)(\epsilon_d + \epsilon_m) \quad (4.166)$$

Substituting (4.166) and (4.143) into (4.153) gives

$$\text{CMRR} = \left| \frac{G_m[\text{dm}]}{G_m[\text{cm}]} \right| \simeq \frac{1 + 2g_{m(dp)}r_{\text{tail}}}{(\epsilon_d + \epsilon_m)} \quad (4.167)$$

Comparing (4.167) and (4.156) shows that the active load improves the common-mode rejection ratio by a factor of $2/(\epsilon_d + \epsilon_m)$. The factor of 2 in the numerator of this expression stems from the increase in the differential transconductance, and the denominator stems from the decrease in the common-mode transconductance.

To find ϵ_d , we will refer to Fig. 4.26b with $v_{i1} = v_{i2} = v_{ic}$. First, we write

$$i_1 = g_{m(dp)}(v_{ic} - v_1) + \frac{v_3 - v_1}{r_{o(dp)}} \quad (4.168)$$

and

$$i_2 = g_{m(dp)}(v_{ic} - v_1) - \frac{v_1}{r_{o(dp)}} \quad (4.169)$$

Substituting (4.134) and $i_3 = -i_1$ into (4.168) gives

$$i_1 \simeq g_{m(dp)}(v_{ic} - v_1) - \frac{v_1}{r_{o(dp)}} - \frac{i_1}{g_{m(mir)}r_{o(dp)}} \quad (4.170)$$

Equation 4.170 can be rearranged to give

$$\left(\frac{1 + g_{m(mir)}r_{o(dp)}}{g_{m(mir)}r_{o(dp)}} \right) i_1 \simeq g_{m(dp)}(v_{ic} - v_1) - \frac{v_1}{r_{o(dp)}} \quad (4.171)$$

Substituting (4.169) into (4.171) gives

$$i_1 \simeq \left(\frac{g_{m(mir)}r_{o(dp)}}{1 + g_{m(mir)}r_{o(dp)}} \right) i_2 \quad (4.172)$$

Substituting (4.161) into (4.172) gives

$$\epsilon_d \simeq \frac{1}{1 + g_{m(mir)}r_{o(dp)}} \quad (4.173)$$

To find ϵ_m , we will again refer to Fig. 4.26b with $v_{i1} = v_{i2} = v_{ic}$. In writing (4.134), we assumed that $r_3 \simeq 1/g_{m3}$. We will now reconsider this assumption and write

$$r_3 = \frac{1}{g_{m3}} ||r_{\pi 3}||r_{\pi 4}||r_{o3} \quad (4.174)$$

We will still assume that the two transistors in the differential pair match perfectly and operate with equal dc currents, as do the two transistors in the active load. Then (4.174) can be rewritten as

$$r_3 = \frac{r_{\pi(mir)}r_{o(mir)}}{r_{\pi(mir)} + 2r_{o(mir)} + g_{m(mir)}r_{\pi(mir)}r_{o(mir)}} \quad (4.175)$$

Substituting (4.175) into (4.135) gives

$$g_{m4}v_3 = g_{m4}i_3r_3 = \frac{g_{m(mir)}r_{\pi(mir)}r_{o(mir)}i_3}{r_{\pi(mir)} + 2r_{o(mir)} + g_{m(mir)}r_{\pi(mir)}r_{o(mir)}} \quad (4.176)$$

Substituting (4.133) into (4.176) gives

$$\epsilon_m = \frac{r_{\pi(mir)} + 2r_{o(mir)}}{r_{\pi(mir)} + 2r_{o(mir)} + g_{m(mir)}r_{\pi(mir)}r_{o(mir)}} \quad (4.177)$$

For bipolar transistors, r_{π} is usually much less than r_o ; therefore,

$$\epsilon_m[bip] = \frac{2 + \frac{r_{\pi(mir)}}{r_{o(mir)}}}{2 + \frac{r_{\pi(mir)}}{r_{o(mir)}} + g_{m(mir)}r_{\pi(mir)}} \simeq \frac{1}{1 + \frac{g_{m(mir)}r_{\pi(mir)}}{2}} = \frac{1}{1 + \frac{\beta_0}{2}} \quad (4.178)$$

Since $r_{\pi} \rightarrow \infty$ for MOS transistors,

$$\epsilon_m[MOS] = \frac{1}{1 + g_{m(mir)}r_{o(mir)}} \quad (4.179)$$

For the bipolar circuit in Fig. 4.29b, substituting (4.173) and (4.178) into (4.167) gives

$$\text{CMRR} \simeq \frac{1 + 2g_{m(dp)}r_{tail}}{\left(\frac{1}{1 + g_{m(mir)}r_{o(dp)}} + \frac{1}{1 + \frac{g_{m(mir)}r_{\pi(mir)}}{2}} \right)} \quad (4.180)$$

If $(g_{m(mir)}r_{o(dp)}) \gg 1$ and $(g_{m(mir)}r_{\pi(mir)}/2) \gg 1$, (4.180) can be simplified to give

$$\begin{aligned} \text{CMRR} &\simeq (1 + 2g_{m(dp)}r_{\text{tail}})g_{m(mir)} \left(r_{o(dp)} \parallel \frac{r_{\pi(mir)}}{2} \right) \\ &\simeq (2g_{m(dp)}r_{\text{tail}})g_{m(mir)} \left(r_{o(dp)} \parallel \frac{r_{\pi(mir)}}{2} \right) \end{aligned} \quad (4.181)$$

Comparing (4.181) and (4.156) shows that the active load increases the common-mode rejection ratio by a factor of about $2g_{m(mir)}(r_{o(dp)} \parallel (r_{\pi(mir)}/2))$ for the bipolar circuit in Fig. 4.29b compared to its passive-load counterpart in Fig. 4.29a.

On the other hand, for the MOS circuit in Fig. 4.29b, substituting (4.173) and (4.179) into (4.167) gives

$$\text{CMRR} \simeq \frac{1 + 2g_{m(dp)}r_{\text{tail}}}{\left(\frac{1}{1 + g_{m(mir)}r_{o(dp)}} + \frac{1}{1 + g_{m(mir)}r_{o(mir)}} \right)} \quad (4.182)$$

If $(g_{m(mir)}r_{o(dp)}) \gg 1$ and $(g_{m(mir)}r_{o(mir)}) \gg 1$, (4.182) can be simplified to give

$$\begin{aligned} \text{CMRR} &\simeq (1 + 2g_{m(dp)}r_{\text{tail}})g_{m(mir)}(r_{o(dp)} \parallel r_{o(mir)}) \\ &\simeq (2g_{m(dp)}r_{\text{tail}})g_{m(mir)}(r_{o(dp)} \parallel r_{o(mir)}) \end{aligned} \quad (4.183)$$

Comparing (4.183) and (4.156) shows that the active load increases the common-mode rejection ratio by a factor of about $2g_{m(mir)}(r_{o(dp)} \parallel r_{o(mir)})$ for the MOS circuit in Fig. 4.29b compared to its passive-load counterpart in Fig. 4.29a.

For these calculations, perfect matching was assumed so that $g_{m1} = g_{m2}$, $g_{m3} = g_{m4}$, $r_{o1} = r_{o2}$, and $r_{o3} = r_{o4}$. In practice, however, nonzero mismatch occurs. With mismatch in a MOS differential pair using a current-mirror load, the differential-mode transconductance is

$$G_m[dm] \simeq g_{m1-2} \left[\frac{1 - \left(\frac{\Delta g_{m1-2}}{2g_{m1-2}} \right)^2}{1 + \left(\frac{\Delta g_{m3-4}}{2g_{m3-4}} \right)} \right] \quad (4.184)$$

where $\Delta g_{m1-2} = g_{m1} - g_{m2}$, $g_{m1-2} = (g_{m1} + g_{m2})/2$, $\Delta g_{m3-4} = g_{m3} - g_{m4}$, and $g_{m3-4} = (g_{m3} + g_{m4})/2$. See Problem 4.18. The approximation in (4.184) is valid to the extent that $g_{m1}r_o \gg 1$ for each transistor and $(g_{m1} + g_{m2})r_{\text{tail}} \gg 1$ for the tail current source. Equation 4.184 shows that the mismatch between g_{m1} and g_{m2} has only a minor effect on $G_m[dm]$. This result stems from the fact that the small-signal voltage across the tail current source, v_{tail} , is zero with a purely differential input only when $g_{m1} = g_{m2}$, assuming $r_{o1} \rightarrow \infty$ and $r_{o2} \rightarrow \infty$. For example, increasing g_{m1} compared to g_{m2} tends to increase the small-signal drain current i_1 if v_{gs1} is constant. However, this change also increases v_{tail} , which reduces v_{gs1} for a fixed v_{id} . The combination of these two effects causes i_1 to be insensitive to $g_{m1} - g_{m2}$. On the other hand, mismatch between g_{m3} and g_{m4} directly modifies the contribution of i_1 through the current mirror to the output current. Therefore, (4.184) shows that $G_m[dm]$ is most sensitive to the mismatch between g_{m3} and g_{m4} .

With mismatch in a MOS differential pair using a current-mirror load, the common-mode transconductance is

$$G_m[cm] \simeq -\frac{1}{2r_{\text{tail}}}(\epsilon_d + \epsilon_m) \quad (4.185)$$

where ϵ_d is the gain error in the source-coupled pair with a pure common-mode input defined in (4.161) and ϵ_m is the gain error in the current mirror defined in (4.133). From Problem 4.19,

$$\epsilon_d \simeq \frac{1}{g_{m3}r_{o(dp)}} - \frac{\Delta g_{m1-2}}{g_{m1-2}} \left(1 + \frac{2r_{tail}}{r_{o(dp)}} \right) - \frac{2r_{tail}}{r_{o(dp)}} \frac{\Delta r_{o(dp)}}{r_{o(dp)}} \quad (4.186)$$

Each term in (4.186) corresponds to one source of gain error by itself, and interactions between terms are ignored. The first term in (4.186) is consistent with (4.173) when $g_{m3}r_{o(dp)} \gg 1$ and stems from the observation that the drain of T_1 is not connected to a small-signal ground during the calculation of $G_m[dm]$, unlike the drain of T_2 . The second term in (4.186) stems from mismatch between g_{m1} and g_{m2} alone. The third term in (4.186) stems from the mismatch between r_{o1} and r_{o2} alone. The contribution of this mismatch to $G_m[cm]$ is significant because the action of the current mirror nearly cancels the contributions of the input g_m generators to $G_m[cm]$ under ideal conditions, causing $G_m[cm] \simeq 0$ in (4.166). In contrast, $G_m[dm]$ is insensitive to the mismatch between r_{o1} and r_{o2} because the dominant contributions to $G_m[dm]$ arising from the input g_m generators do not cancel at the output. From Problem 4.19,

$$\epsilon_m = \frac{1}{1 + g_{m3}r_{o3}} + \frac{(g_{m3} - g_{m4})r_{o3}}{1 + g_{m3}r_{o3}} \simeq \frac{1}{g_{m3}r_{o3}} + \frac{\Delta g_{m3-4}}{g_{m3-4}} \quad (4.187)$$

Each term in (4.187) corresponds to one source of gain error by itself, and interactions between terms are ignored. The first term in (4.187), which is consistent with (4.179) when $g_{m3}r_{o3} \gg 1$, stems from the observation that the small-signal input resistance of the current mirror is not exactly $1/g_{m3}$ but $(1/g_{m3})||r_{o3}$. The second term in (4.187) stems from mismatch between g_{m3} and g_{m4} alone. The CMRR with mismatch is the ratio of $G_m[dm]$ in (4.184) to $G_m[cm]$ in (4.185), using (4.186) and (4.187) for ϵ_d and ϵ_m , respectively. Since the common-mode transconductance is very small without mismatch (as a result of the behavior of the current-mirror load), mismatch usually reduces the CMRR by increasing $|G_m[cm]|$.

4.4 Voltage and Current References

4.4.1 Low-Current Biasing

4.4.1.1 Bipolar Widlar Current Source

In ideal operational amplifiers, the current is zero in each of the two input leads. However, the input current is not zero in real op amps with bipolar input transistors because β_F is finite. Since the op-amp inputs are usually connected to a differential pair, the tail current must usually be very small in such op amps to keep the input current small. Typically, the tail current is on the order of 5 μA . Bias currents of this magnitude are also required in a variety of other applications, especially where minimizing power dissipation is important. The simple current mirrors shown in Fig. 4.30 are usually not optimum for such small currents. For example, using a simple bipolar current mirror as in Fig. 4.30a and assuming a maximum practical emitter area ratio between transistors of ten to one, the mirror would need an input current of 50 μA for an output current of 5 μA . If the power-supply voltage in Fig. 4.30a is 5 V, and if $V_{BE(\text{on})} = 0.7$ V, $R = 86$ k Ω would be required. Resistors of this magnitude are costly in terms of die area. Currents of such low magnitude can be obtained with moderate values of resistance, however, by modifying the simple current mirror so that the transistors operate with unequal base-emitter voltages. In the Widlar current source of Fig. 4.31a, resistor R_2 is inserted in series with the emitter of Q_2 , and transistors Q_1 and Q_2 operate with unequal base-emitter voltages if $R_2 \neq 0$.^{10,11} This circuit is referred to as a current source rather than a current mirror because the output current in Fig. 4.31a is much less dependent on the input

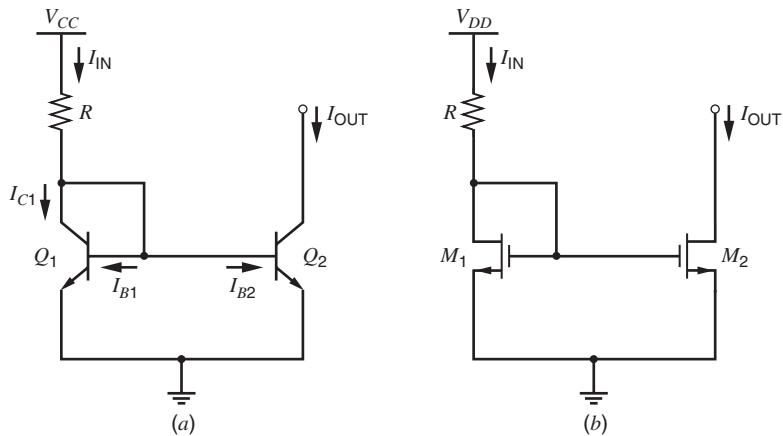


Figure 4.30 Simple two-transistor current mirrors where the input current is set by the supply voltage and a resistor using (a) bipolar and (b) MOS transistors.

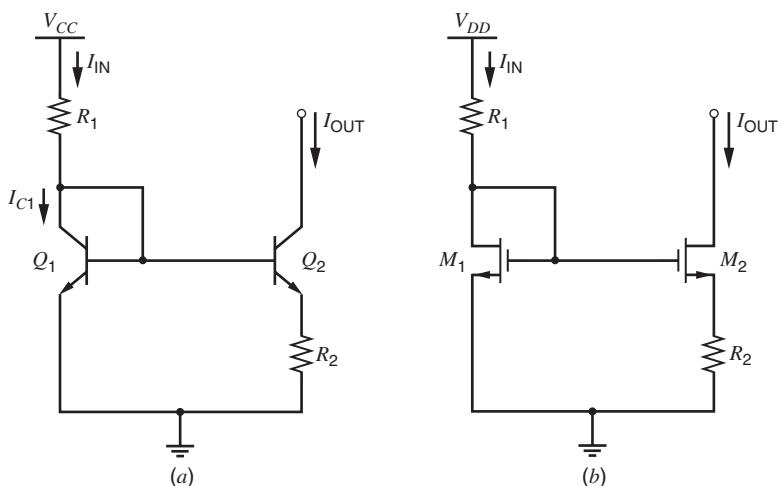


Figure 4.31 Widlar current sources: (a) bipolar and (b) MOS.

current and the power-supply voltage than in the simple current mirror of Fig. 4.30a, as shown in Section 4.4.2. We will now calculate the output current of the Widlar current source.

If $I_{IN} > 0$, Q_1 operates in the forward-active region because it is diode connected. Assume that Q_2 also operates in the forward active region. KVL around the base-emitter loop gives

$$V_{BE1} - V_{BE2} - \frac{\beta_F + 1}{\beta_F} I_{OUT} R_2 = 0 \quad (4.188)$$

If we assume that $V_{BE1} = V_{BE2} = V_{BE(on)} = 0.7$ V in (4.188), we would predict that $I_{OUT} = 0$. Although I_{OUT} is small in practice, it is greater than zero under the usual bias conditions, which means that the standard assumption about $V_{BE(on)}$ is invalid here. In contrast, the standard assumption is usually valid in calculating I_{IN} because small variations in V_{BE1} have little effect on I_{IN} if $V_{CC} \gg V_{BE1}$. When one base-emitter voltage is subtracted from another, however, small differences between them are important. If $V_A \rightarrow \infty$, (4.188) can be rewritten

using (1.35) as

$$V_T \ln \frac{I_{C1}}{I_{S1}} - V_T \ln \frac{I_{OUT}}{I_{S2}} - \frac{\beta_F + 1}{\beta_F} I_{OUT} R_2 = 0 \quad (4.189)$$

If $\beta_F \rightarrow \infty$, (4.189) simplifies to

$$V_T \ln \frac{I_{IN}}{I_{S1}} - V_T \ln \frac{I_{OUT}}{I_{S2}} - I_{OUT} R_2 = 0 \quad (4.190)$$

For identical transistors, I_{S1} and I_{S2} are equal, and (4.190) becomes

$$V_T \ln \frac{I_{IN}}{I_{OUT}} = I_{OUT} R_2 \quad (4.191)$$

This transcendental equation can be solved by trial and error to find I_{OUT} if R_2 and I_{IN} are known, as in typical analysis problems. Because the logarithm function compresses changes in its argument, attention can be focused on the linear term in (4.191), simplifying convergence of the trial-and-error process. In design problems, however, the desired I_{IN} and I_{OUT} are usually known, and (4.191) provides the required value of R_2 .

■ EXAMPLE

In the circuit of Fig. 4.31a, determine the proper value of R_2 to give $I_{OUT} = 5 \mu A$. Assume that $V_{CC} = 5 V$, $R_1 = 4.3 \text{ k}\Omega$, $V_{BE(on)} = 0.7 \text{ V}$, and $\beta_F \rightarrow \infty$.

$$I_{IN} = \frac{5 \text{ V} - 0.7 \text{ V}}{4.3 \text{ k}\Omega} = 1 \text{ mA}$$

$$V_T \ln \frac{I_{IN}}{I_{OUT}} = 26 \text{ mV} \ln \left(\frac{1 \text{ mA}}{5 \mu A} \right) = 137 \text{ mV}$$

Thus from (4.191)

$$I_{OUT} R_2 = 137 \text{ mV}$$

and

$$R_2 = \frac{137 \text{ mV}}{5 \mu A} = 27.4 \text{ k}\Omega$$

■ The total resistance in the circuit is $31.7 \text{ k}\Omega$.

■ EXAMPLE

In the circuit of Fig. 4.31a, assume that $I_{IN} = 1 \text{ mA}$, $R_2 = 5 \text{ k}\Omega$, and $\beta_F \rightarrow \infty$. Find I_{OUT} . From (4.191),

$$V_T \ln \frac{1 \text{ mA}}{I_{OUT}} - 5 \text{ k}\Omega(I_{OUT}) = 0$$

Try

$$I_{OUT} = 15 \mu A$$

$$108 \text{ mV} - 75 \text{ mV} \neq 0$$

The linear term $I_{OUT} R_2$ is too small; therefore, $I_{OUT} > 15 \mu A$ should be tried. Try

$$I_{OUT} = 20 \mu A$$

$$101.7 \text{ mV} - 100 \text{ mV} \simeq 0$$

Therefore, the output current is close to 20 μA . Notice that while the linear term increased by 25 mV from the first to the second trial, the logarithm term decreased by only about 6 mV because the logarithm function compresses changes in its argument.

4.4.1.2 MOS Widlar Current Source

The Widlar configuration can also be used in MOS technology, as shown in Fig. 4.31b.

If $I_{IN} > 0$, M_1 operates in the active region because it is diode connected. Assume that M_2 also operates in the forward active region. KVL around the gate-source loop gives

$$V_{GS1} - V_{GS2} - I_{OUT}R_2 = 0 \quad (4.192)$$

If we ignore the body effect, the threshold components of the gate-source voltages cancel and (4.192) simplifies to

$$I_{OUT}R_2 + V_{ov2} - V_{ov1} = 0 \quad (4.193)$$

If the transistors operate in strong inversion and $V_A \rightarrow \infty$,

$$I_{OUT}R_2 + \sqrt{\frac{2I_{OUT}}{k'(W/L)_2}} - V_{ov1} = 0 \quad (4.194)$$

This quadratic equation can be solved for $\sqrt{I_{OUT}}$.

$$\sqrt{I_{OUT}} = \frac{-\sqrt{\frac{2}{k'(W/L)_2}} \pm \sqrt{\frac{2}{k'(W/L)_2} + 4R_2V_{ov1}}}{2R_2} \quad (4.195)$$

where $V_{ov1} = \sqrt{2I_{IN}/[k'(W/L)_1]}$. From (1.157),

$$\sqrt{I_{OUT}} = \sqrt{\frac{k'(W/L)_2}{2}} (V_{GS2} - V_t) \quad (4.196)$$

Equation 4.196 applies only when M_2 operates in the active region, which means that $V_{GS2} > V_t$. As a result, $\sqrt{I_{OUT}} > 0$ and the potential solution where the second term in the numerator of (4.195) is subtracted from the first, cannot occur in practice. Therefore,

$$\sqrt{I_{OUT}} = \frac{-\sqrt{\frac{2}{k'(W/L)_2}} + \sqrt{\frac{2}{k'(W/L)_2} + 4R_2V_{ov1}}}{2R_2} \quad (4.197)$$

Equation 4.197 shows that a closed-form solution for the output current can be written for a Widlar current source that uses MOS transistors operating in strong inversion, unlike the bipolar case where trial and error is required to find I_{OUT} .

EXAMPLE

In Fig. 4.31b, find I_{OUT} if $I_{IN} = 100 \mu\text{A}$, $R_2 = 4 \text{ k}\Omega$, $k' = 200 \mu\text{A/V}^2$, and $(W/L)_1 = (W/L)_2 = 25$. Assume the temperature is 27°C and that $n = 1.5$ in (1.247).

Then $R_2 = 0.004 \text{ M}\Omega$, $V_{ov1} = \sqrt{200/(200 \times 25)} \text{ V} = 0.2 \text{ V}$,

$$\sqrt{I_{OUT}} = \frac{-\sqrt{\frac{2}{200(25)}} + \sqrt{\frac{2}{200(25)} + 4(0.004)(0.2)}}{2(0.004)} \sqrt{\mu\text{A}} = 5\sqrt{\mu\text{A}}$$

and $I_{\text{OUT}} = 25 \mu\text{A}$. Also,

$$V_{ov2} = V_{ov1} - I_{\text{OUT}}R_2 = 0.2 - 25 \times 0.004 = 0.1 \text{ V} > 2nV_T \approx 78 \text{ mV}$$

Therefore, both transistors operate in strong inversion, as assumed.

4.4.1.3 Bipolar Peaking Current Source

The Widlar source described in Section 4.4.1.1 allows currents in the microamp range to be realized with moderate values of resistance. Biasing integrated-circuit stages with currents on the order of nanoamps is often desirable. To reach such low currents with moderate values of resistance, the circuit shown in Fig. 4.32 can be used.^{12,13,14} Neglecting base currents, we have

$$V_{BE1} - I_{\text{IN}}R = V_{BE2} \quad (4.198)$$

If $V_A \rightarrow \infty$, (4.198) can be rewritten using (1.35) as

$$V_T \ln \frac{I_{\text{IN}}}{I_{S1}} - V_T \ln \frac{I_{\text{OUT}}}{I_{S2}} = I_{\text{IN}}R \quad (4.199)$$

If Q_1 and Q_2 are identical, (4.199) can be rewritten as

$$I_{\text{OUT}} = I_{\text{IN}} \exp \left(-\frac{I_{\text{IN}}R}{V_T} \right) \quad (4.200)$$

Equation 4.200 is useful for analysis of a given circuit. For design with identical Q_1 and Q_2 , (4.199) can be rewritten as

$$R = \frac{V_T}{I_{\text{IN}}} \ln \frac{I_{\text{IN}}}{I_{\text{OUT}}} \quad (4.201)$$

For example, for $I_{\text{IN}} = 10 \mu\text{A}$ and $I_{\text{OUT}} = 100 \text{ nA}$, (4.201) can be used to show that $R \approx 12 \text{ k}\Omega$.

A plot of I_{OUT} versus I_{IN} from (4.200) is shown in Fig. 4.33. When the input current is small, the voltage drop on the resistor is small, and $V_{BE2} \approx V_{BE1}$ so $I_{\text{OUT}} \approx I_{\text{IN}}$. As the input current increases, V_{BE1} increases in proportion to the logarithm of the input current while the drop on the resistor increases linearly with the input current. As a result, increases in the input current eventually cause the base-emitter voltage of Q_2 to decrease. The output current

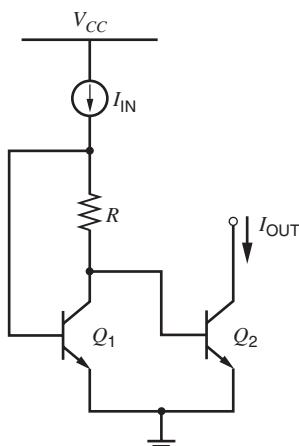


Figure 4.32 Bipolar peaking current source.

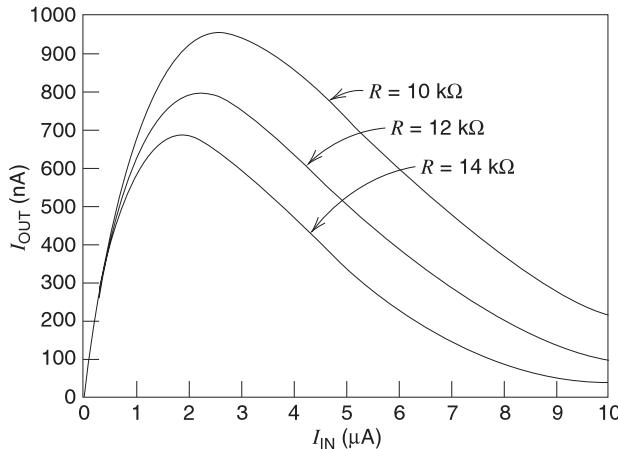


Figure 4.33 Transfer characteristics of the bipolar peaking current source with $T = 27^\circ\text{C}$.

reaches a maximum when V_{BE2} is maximum. The name *peaking current source* stems from this behavior, and the location and magnitude of the peak both depend on R .

4.4.1.4 MOS Peaking Current Source

The peaking-current configuration can also be used in MOS technology, as shown in Fig. 4.34. If I_{IN} is small and positive, the voltage drop on R is small and M_1 operates in the active region. Assume that M_2 also operates in the active region. KVL around the gate-source loop gives

$$V_{GS1} - I_{IN}R - V_{GS2} = 0 \quad (4.202)$$

Since the sources of M_1 and M_2 are connected together, the thresholds cancel and (4.202) simplifies to

$$V_{ov2} = V_{ov1} - I_{IN}R \quad (4.203)$$

From (1.157),

$$I_{OUT} = \frac{k'(W/L)_2}{2}(V_{ov2})^2 = \frac{k'(W/L)_2}{2}(V_{ov1} - I_{IN}R)^2 \quad (4.204)$$

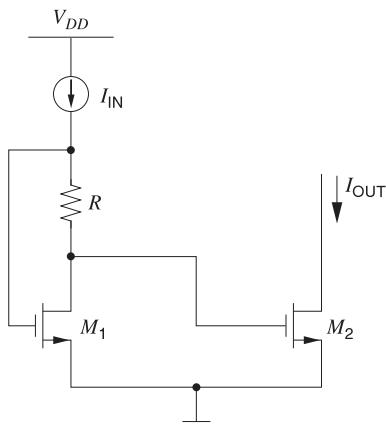


Figure 4.34 MOS peaking current source.

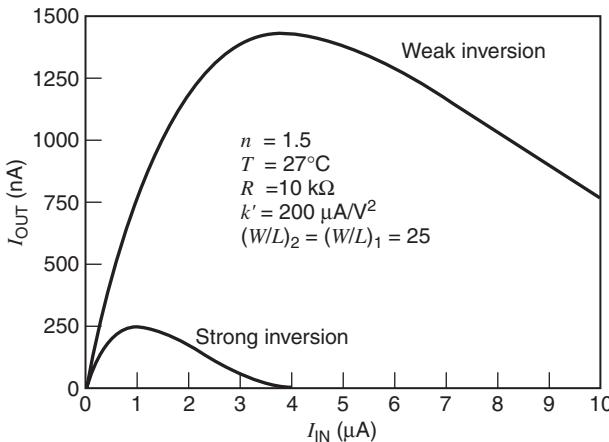


Figure 4.35 Transfer characteristics of the MOS peaking current source assuming both transistors operate in weak inversion or in strong inversion.

where $V_{ov1} = \sqrt{2I_{IN}/[k'(W/L)_1]}$. Equation 4.204 assumes that the transistors operate in strong inversion. In practice, the input current is usually small enough that the overdrive of M_1 is less than $2nV_T$, where n is defined in (1.247) and V_T is a thermal voltage. Equation 4.203 shows that the overdrive of M_2 is even smaller than that of M_1 . Therefore, both transistors usually operate in weak inversion, where the drain current is an exponential function of the gate-source voltage as shown in (1.252). If $V_{DS1} > 3V_T$, applying (1.252) to M_1 and substituting into (4.202) gives

$$V_{GS2} - V_t \simeq nV_T \ln \left(\frac{I_{IN}}{(W/L)_1 I_t} \right) - I_{IN} R \quad (4.205)$$

Then if the transistors are identical and $V_{DS2} > 3V_T$, substituting (4.205) into (1.252) gives

$$I_{OUT} \simeq \frac{W}{L} I_t \exp \left(\frac{V_{GS2} - V_t}{nV_T} \right) \simeq I_{IN} \exp \left(-\frac{I_{IN} R}{nV_T} \right) \quad (4.206)$$

where I_t is given by (1.251) and represents the drain current of M_2 with $V_{GS2} = V_t$, $W/L = 1$, and $V_{DS} \gg V_T$. Comparing (4.206) with (4.200) shows that the output current in an MOS peaking current source where both transistors operate in weak inversion is the same as in the bipolar case except that $1.3 \leq n \leq 1.5$ in the MOS case and $n = 1$ in the bipolar case.

Plots of (4.206) and (4.204) are shown in Fig. 4.35 for $n = 1.5$, $T = 27^\circ C$, $R = 10 \text{ k}\Omega$, $k' = 200 \mu A/V^2$, and $(W/L)_2 = (W/L)_1 = 25$. In both cases, when the input current is small, the voltage drop on the resistor is small, and $I_{OUT} \simeq I_{IN}$. As the input current increases, V_{GS1} increases more slowly than the drop on the resistor. As a result, increases in the input current eventually cause the gate-source voltage of M_2 to decrease. The output current reaches a maximum when V_{GS2} is maximum. As in the bipolar case, the name *peaking current source* stems from this behavior, and the location and magnitude of the peak both depend on R . Because the overdrives on both transistors are usually very small, the strong-inversion equation (4.204) usually underestimates the output current.

4.4.2 Supply-Insensitive Biasing

Consider the simple current mirror of Fig. 4.30a, where the input current source has been replaced by a resistor. Ignoring the effects of finite β_F and V_A , (4.5) shows that the output

current is

$$I_{\text{OUT}} \simeq I_{\text{IN}} = \frac{V_{CC} - V_{BE(\text{on})}}{R} \quad (4.207)$$

If $V_{CC} \gg V_{BE(\text{on})}$, this circuit has the drawback that the output current is proportional to the power-supply voltage. For example, if $V_{BE(\text{on})} = 0.7$ V, and if this current mirror is used in an operational amplifier that has to function with power-supply voltages ranging from 3 V to 10 V, the bias current would vary over a four-to-one range, and the power dissipation would vary over a thirteen-to-one range.

One measure of this aspect of bias-circuit performance is the fractional change in the bias current that results from a given fractional change in supply voltage. The most useful parameter for describing the variation of the output current with the power-supply voltage is the sensitivity S . The sensitivity of any circuit variable y to a parameter x is defined as follows:

$$S_x^y = \lim_{\Delta x \rightarrow 0} \frac{\Delta y/y}{\Delta x/x} = \frac{x}{y} \frac{\partial y}{\partial x} \quad (4.208)$$

Applying (4.208) to find the sensitivity of the output current to small variations in the power-supply voltage gives

$$S_{V_{\text{SUP}}}^{I_{\text{OUT}}} = \frac{V_{\text{SUP}}}{I_{\text{OUT}}} \frac{\partial I_{\text{OUT}}}{\partial V_{\text{SUP}}} \quad (4.209)$$

The supply voltage V_{SUP} is usually called V_{CC} in bipolar circuits and V_{DD} in MOS circuits. If $V_{CC} \gg V_{BE(\text{on})}$ in Fig. 4.30a, and if $V_{DD} \gg V_{GS1}$ in Fig. 4.30b,

$$S_{V_{\text{SUP}}}^{I_{\text{OUT}}} \simeq 1 \quad (4.210)$$

Equation 4.210 shows that the output currents in the simple current mirrors in Fig. 4.30 depend strongly on the power-supply voltages. Therefore, this configuration should not be used when supply insensitivity is important.

4.4.2.1 Widlar Current Sources

For the case of the bipolar Widlar source in Fig. 4.31a, the output current is given implicitly by (4.191). To determine the sensitivity of I_{OUT} to the power-supply voltage, this equation is differentiated with respect to V_{CC} :

$$V_T \frac{\partial}{\partial V_{CC}} \ln \frac{I_{\text{IN}}}{I_{\text{OUT}}} = R_2 \frac{\partial I_{\text{OUT}}}{\partial V_{CC}} \quad (4.211)$$

Differentiating yields

$$V_T \left(\frac{I_{\text{OUT}}}{I_{\text{IN}}} \right) \left(\frac{1}{I_{\text{OUT}}} \frac{\partial I_{\text{IN}}}{\partial V_{CC}} - \frac{I_{\text{IN}}}{I_{\text{OUT}}^2} \frac{\partial I_{\text{OUT}}}{\partial V_{CC}} \right) = R_2 \frac{\partial I_{\text{OUT}}}{\partial V_{CC}} \quad (4.212)$$

Solving this equation for $\partial I_{\text{OUT}}/\partial V_{CC}$, we obtain

$$\frac{\partial I_{\text{OUT}}}{\partial V_{CC}} = \left(\frac{1}{1 + \frac{I_{\text{OUT}} R_2}{V_T}} \right) \frac{I_{\text{OUT}}}{I_{\text{IN}}} \frac{\partial I_{\text{IN}}}{\partial V_{CC}} \quad (4.213)$$

Substituting (4.213) into (4.209) gives

$$S_{V_{CC}}^{I_{\text{OUT}}} = \left(\frac{1}{1 + \frac{I_{\text{OUT}} R_2}{V_T}} \right) \frac{V_{CC}}{I_{\text{IN}}} \frac{\partial I_{\text{IN}}}{\partial V_{CC}} = \left(\frac{1}{1 + \frac{I_{\text{OUT}} R_2}{V_T}} \right) S_{V_{CC}}^{I_{\text{IN}}} \quad (4.214)$$

If $V_{CC} \gg V_{BE(on)}$, $I_{IN} \simeq V_{CC}/R_1$ and the sensitivity of I_{IN} to V_{CC} is approximately unity, as in the simple current mirror of Fig. 4.30a. For the example in Section 4.4.1.1 where $I_{IN} = 1 \text{ mA}$, $I_{OUT} = 5 \mu\text{A}$, and $R_2 = 27.4 \text{ k}\Omega$, (4.214) gives

$$S_{V_{CC}}^{I_{OUT}} = \frac{V_{CC}}{I_{OUT}} \frac{\partial I_{OUT}}{\partial V_{CC}} \simeq \frac{1}{1 + \frac{137 \text{ mV}}{26 \text{ mV}}} \simeq 0.16 \quad (4.215)$$

Thus for this case, a 10 percent power-supply voltage change results in only 1.6 percent change in I_{OUT} .

For the case of the MOS Widlar source in Fig. 4.31b, the output current is given by (4.197). Differentiating with respect to V_{DD} gives

$$\frac{1}{2\sqrt{I_{OUT}}} \frac{\partial I_{OUT}}{\partial V_{DD}} = \frac{1}{4R_2} \frac{1}{\sqrt{\frac{2}{k'(W/L)_2} + 4R_2 V_{ov1}}} 4R_2 \frac{\partial V_{ov1}}{\partial V_{DD}} \quad (4.216)$$

where

$$\frac{\partial V_{ov1}}{\partial V_{DD}} = \sqrt{\frac{2}{k'(W/L)_1}} \frac{1}{2\sqrt{I_{IN}}} \frac{\partial I_{IN}}{\partial V_{DD}} = \frac{V_{ov1}}{2I_{IN}} \frac{\partial I_{IN}}{\partial V_{DD}} \quad (4.217)$$

Substituting (4.216) and (4.217) into (4.209) gives

$$S_{V_{DD}}^{I_{OUT}} = \frac{V_{ov1}}{\sqrt{V_{ov2}^2 + 4I_{OUT}R_2V_{ov1}}} S_{V_{DD}}^{I_{IN}} \quad (4.218)$$

Since I_{OUT} is usually much less than I_{IN} , V_{ov2} is usually small and $I_{OUT}R_2 \simeq V_{ov1}$ and (4.218) simplifies to

$$S_{V_{DD}}^{I_{OUT}} \simeq \frac{V_{ov1}}{\sqrt{4V_{ov1}^2}} S_{V_{DD}}^{I_{IN}} = 0.5 S_{V_{DD}}^{I_{IN}} \quad (4.219)$$

If $V_{DD} \gg V_{GS1}$, $I_{IN} \simeq V_{DD}/R_1$ and the sensitivity of I_{IN} to V_{DD} is approximately unity, as in the simple current mirror of Fig. 4.30b. Thus for this case, a 10 percent power-supply voltage change results in a 5 percent change in I_{OUT} .

4.4.2.2 Current Sources Using Other Voltage Standards

The level of power-supply independence provided by the bipolar and MOS Widlar current sources is not adequate for many types of analog circuits. Much lower sensitivity can be obtained by causing bias currents in the circuit to depend on a voltage standard other than the supply voltage. Bias reference circuits can be classified according to the voltage standard by which the bias currents are established. The most convenient standards are the base-emitter or threshold voltage of a transistor, the thermal voltage, or the breakdown voltage of a reverse-biased *pn* junction (a Zener diode). Each of these standards can be used to reduce supply sensitivity, but the drawback of the first three standards is that the reference voltage is quite temperature dependent. Both the base-emitter and threshold voltages have negative temperature coefficients of magnitude 1 to 2 mV/°C, and the thermal voltage has a positive temperature coefficient of $k/q \simeq 86 \mu\text{V/}^\circ\text{C}$. The Zener diode has the disadvantage that at least 7 to 10 V of supply voltage are required because standard integrated-circuit processes produce a minimum breakdown voltage of about 6 V across the most highly doped junctions (usually *n*p transistor emitter-base junctions). Furthermore, *pn* junctions produce large amounts of voltage

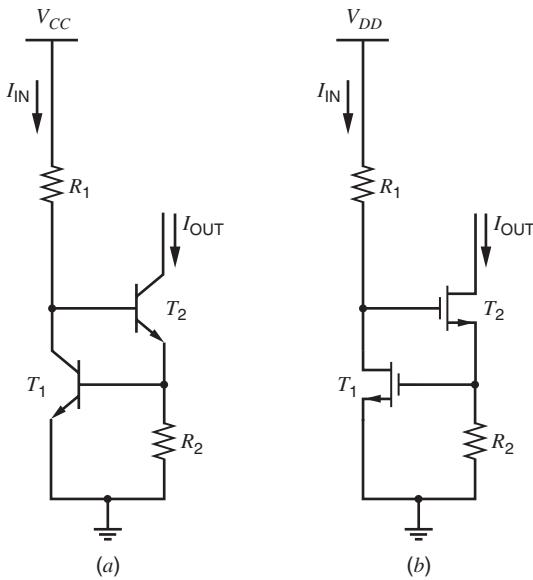


Figure 4.36 (a) Base-emitter referenced current source. (b) Threshold referenced current source.

noise under the reverse-breakdown conditions encountered in a bias reference circuit. Noise in avalanche breakdown is considered further in Chapter 11.

We now consider bias reference circuits based on the base-emitter or gate-source voltage. The circuit in simplest form in bipolar technology is shown in Fig. 4.36a. This circuit is similar to a Wilson current mirror where the diode-connected transistor is replaced by a resistor. For the input current to flow in T_1 , transistor T_2 must supply enough current into R_2 so that the base-emitter voltage of T_1 is

$$V_{BE1} = V_T \ln \frac{I_{IN}}{I_{S1}} \quad (4.220)$$

If we neglect base currents, I_{OUT} is equal to the current flowing through R_2 . Since the voltage drop on R_2 is V_{BE1} , the output current is proportional to this base-emitter voltage. Thus, neglecting base currents, we have

$$I_{OUT} = \frac{V_{BE1}}{R_2} = \frac{V_T}{R_2} \ln \frac{I_{IN}}{I_{S1}} \quad (4.221)$$

Differentiating (4.221) and substituting into (4.209) gives

$$S_{V_{CC}}^{I_{OUT}} = \frac{V_T}{I_{OUT} R_2} S_{V_{CC}}^{I_{IN}} = \frac{V_T}{V_{BE(on)}} S_{V_{CC}}^{I_{IN}} \quad (4.222)$$

If $V_{CC} \gg 2V_{BE(on)}$, $I_{IN} \approx V_{CC}/R_1$ and the sensitivity of I_{IN} to V_{CC} is approximately unity. With $V_{BE(on)} = 0.7$ V,

$$S_{V_{CC}}^{I_{OUT}} = \frac{0.026 \text{ V}}{0.7 \text{ V}} \approx 0.037 \quad (4.223)$$

Thus for this case, a 10 percent power-supply voltage change results in a 0.37 percent change in I_{OUT} . The result is significantly better than for a bipolar Widlar current source.

The MOS counterpart of the base-emitter reference is shown in Fig. 4.36b. Here

$$I_{\text{OUT}} = \frac{V_{GS1}}{R_2} = \frac{V_t + V_{ov1}}{R_2} = \frac{V_t + \sqrt{\frac{2I_{\text{IN}}}{k'(W/L)_1}}}{R_2} \quad (4.224)$$

The case of primary interest is when the overdrive of T_1 is small compared to the threshold voltage. This case can be achieved in practice by choosing sufficiently low input current and large $(W/L)_1$. In this case, the output current is determined mainly by the threshold voltage and R_2 . Therefore, this circuit is known as a *threshold-referenced* bias circuit. Differentiating (4.224) with respect to V_{DD} and substituting into (4.209) gives

$$S_{V_{DD}}^{I_{\text{OUT}}} = \frac{V_{ov1}}{2I_{\text{OUT}}R_2} S_{V_{DD}}^{I_{\text{IN}}} = \frac{V_{ov1}}{2V_{GS1}} S_{V_{DD}}^{I_{\text{IN}}} \quad (4.225)$$

For example, if $V_t = 1$ V, $V_{ov1} = 0.1$ V, and $S_{V_{DD}}^{I_{\text{IN}}} \simeq 1$

$$S_{V_{DD}}^{I_{\text{OUT}}} \simeq \frac{0.1}{2(1.1)} \simeq 0.045 \quad (4.226)$$

These circuits are not fully supply independent because the base-emitter or gate-source voltages of T_1 change slightly with power-supply voltage. This change occurs because the collector or drain current of T_1 is approximately proportional to the supply voltage. The resulting supply sensitivity is often a problem in bias circuits whose input current is derived from a resistor connected to the supply terminal, since this configuration causes the currents in some portion of the circuit to change with the supply voltage.

4.4.2.3 Self-Biasing

Power-supply sensitivity can be greatly reduced by the use of the so-called *bootstrap* bias technique, also referred to as *self-biasing*. Instead of developing the input current by connecting a resistor to the supply, the input current is made to depend directly on the output current of the current source itself. The concept is illustrated in block-diagram form in Fig. 4.37a. Assuming that the feedback loop formed by this connection has a stable operating point, the currents flowing in the circuit are much less sensitive to power-supply voltage than in the resistively biased case. The two key variables here are the input current, I_{IN} , and the output current, I_{OUT} . The relationship between these variables is governed by both the current source and the current

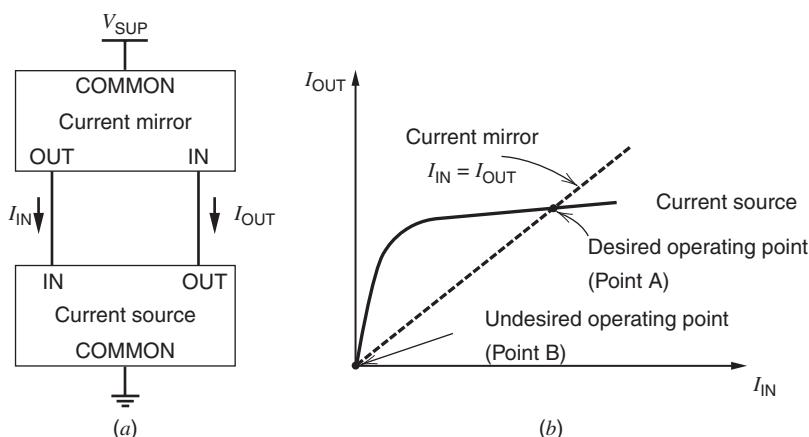


Figure 4.37 (a) Block diagram of a self-biased reference. (b) Determination of operating point.

mirror. From the standpoint of the current source, the output current is almost independent of the input current for a wide range of input currents as shown in Fig. 4.37b. From the standpoint of the current mirror, I_{IN} is set equal to I_{OUT} , assuming that the gain of the current mirror is unity. The operating point of the circuit must satisfy both constraints and hence is at the intersection of the two characteristics. In the plot of Fig. 4.37b, two intersections or potential operating points are shown. Point A is the desired operating point, and point B is an undesired operating point because $I_{OUT} = I_{IN} = 0$.

If the output current in Fig. 4.37a increases for any reason, the current mirror increases the input current by the same amount because the gain of the current mirror is assumed to be unity. As a result, the current source increases the output current by an amount that depends on the gain of the current source. Therefore, the loop responds to an initial change in the output current by further changing the output current in a direction that reinforces the initial change. In other words, the connection of a current source and a current mirror as shown in Fig. 4.37a forms a positive feedback loop, and the gain around the loop is the gain of the current source. In Chapter 9, we will show that circuits with positive feedback are stable if the gain around the loop is less than unity. At point A, the gain around the loop is quite small because the output current of the current source is insensitive to changes in the input current around point A. On the other hand, at point B, the gain around the feedback loop is deliberately made greater than unity so that the two characteristics shown in Fig. 4.37b intersect at a point away from the origin. As a result, this simplified analysis shows that point B is an unstable operating point in principle, and the circuit would ideally tend to drive itself out of this state.

In practice, however, point B is frequently a stable operating point because the currents in the transistors at this point are very small, often in the picoampere range. At such low current levels, leakage currents and other effects reduce the current gain of both bipolar and MOS transistors, usually causing the gain around the loop to be less than unity. As a result, actual circuits of this type are usually unable to drive themselves out of the zero-current state. Thus, unless precautions are taken, the circuit may operate in the zero-current condition. For these reasons, self-biased circuits often have a stable state in which zero current flows in the circuit even when the power-supply voltage is nonzero. This situation is analogous to a gasoline engine that is not running even though it has a full tank of fuel. An electrical or mechanical device is required to start the engine. Similarly, a start-up circuit is usually required to prevent the self-biased circuit from remaining in the zero-current state.

The application of this technique to the V_{BE} -referenced current source is illustrated in Fig. 4.38a, and the threshold-referenced MOS counterpart is shown in Fig. 4.38b. We assume for simplicity that $V_A \rightarrow \infty$. The circuit composed of T_1 , T_2 , and R dictates that the current I_{OUT} depends weakly on I_{IN} , as indicated by (4.221) and (4.224). Second, the current mirror composed of matched transistors T_4 and T_5 dictates that I_{IN} is equal to I_{OUT} . The operating point of the circuit must satisfy both constraints and hence is at the intersection of the two characteristics as in Fig. 4.37b. Except for the effects of finite output resistance of the transistors, the bias currents are independent of supply voltage. If required, the output resistance of the current source and mirror could be increased by the use of cascode or Wilson configurations in the circuits. The actual bias currents for other circuits are supplied by T_6 and/or T_3 , which are matched to T_5 and T_1 , respectively.

The zero-current state can be avoided by using a start-up circuit to ensure that some current always flows in the transistors in the reference so that the gain around the feedback loop at point B in Fig. 4.37b does not fall below unity. An additional requirement is that the start-up circuit must not interfere with the normal operation of the reference once the desired operating point is reached. The V_{BE} -referenced current source with a typical start-up circuit used in bipolar technologies is illustrated in Fig. 4.39a. We first assume that the circuit is in the undesired zero-current state. If this were true, the base-emitter voltage of T_1 would be

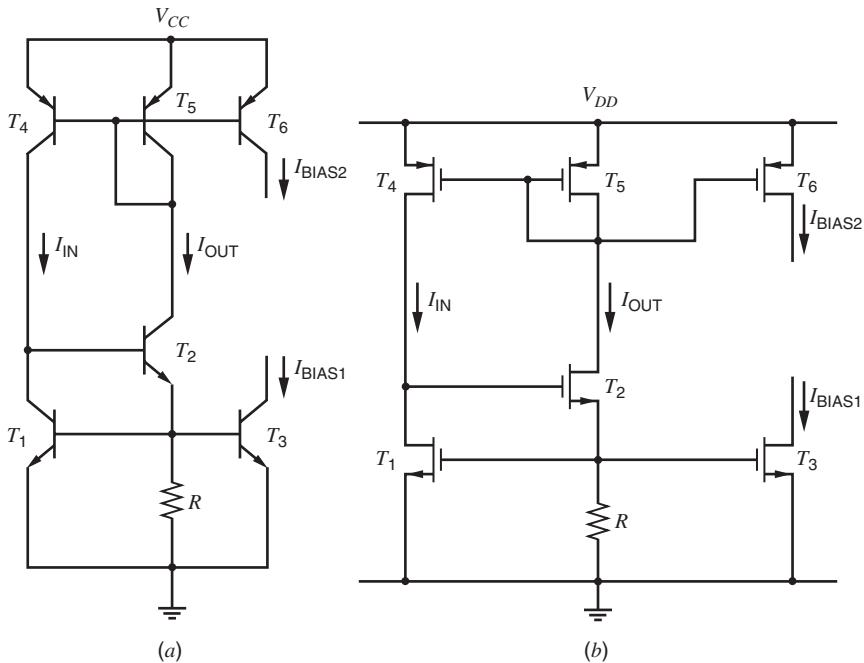


Figure 4.38 (a) Self-biasing V_{BE} reference. (b) Self-biasing V_t reference.

zero. The base-emitter voltage T_2 would be tens of millivolts above ground, determined by the leakage currents in the circuit. However, the voltage on the left-hand end of D_1 is four diode drops above ground, so that a voltage of at least three diode drops would appear across R_x , and a current would flow through R_x into the T_1 - T_2 combination. This action would cause current to flow in T_4 and T_5 , avoiding the zero-current state.

The bias reference circuit then drives itself toward the desired stable state, and we require that the start-up circuit not affect the steady-state current values. This can be accomplished by causing R_x to be large enough that when the steady-state current is established in T_1 , the voltage drop across R_x is large enough to reverse bias D_1 . In the steady state, the collector-emitter voltage of T_1 is two diode drops above ground, and the left-hand end of D_1 is four diode drops above ground. Thus if we make $I_{IN}R_x$ equal to two diode drops, D_1 will have zero voltage across it in the steady state. As a result, the start-up circuit composed of R_s , D_2 - D_5 , and D_1 is, in effect, disconnected from the circuit for steady-state operation.

Floating diodes are not usually available in MOS technologies. The threshold-referenced current source with a typical start-up circuit used in MOS technologies is illustrated in Fig. 4.39b. If the circuit is in the undesired zero-current state, the gate-source voltage of T_1 would be less than a threshold voltage. As a result, T_7 is off and T_8 operates in the triode region, pulling the gate-source voltage of T_9 up to V_{DD} . Therefore, T_9 is on and pulls down on the gates of T_4 and T_5 . This action causes current to flow in T_4 and T_5 , avoiding the zero-current state.

In steady state, the gate-source voltage of T_7 rises to $I_{OUT}R$, which turns on T_7 and reduces the gate-source voltage of T_9 . In other words, T_7 and T_8 form a CMOS inverter whose output falls when the reference circuit turns on. Since the start-up circuit should not interfere with normal operation of the reference in steady state, the inverter output should fall low enough to turn T_9 off in steady state. Therefore, the gate-source voltage of T_9 must fall below a threshold voltage when the inverter input rises from zero to $I_{OUT}R$. In practice,

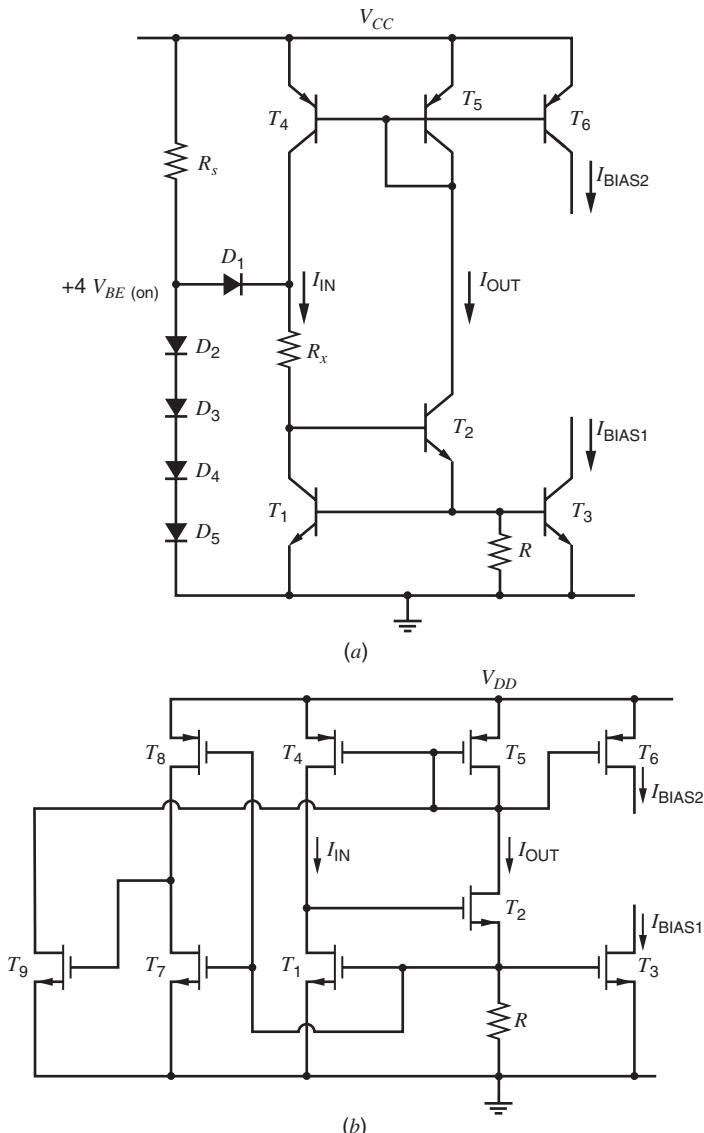


Figure 4.39 (a) Self-biasing V_{BE} reference with start-up circuit. (b) Self-biasing V_t reference with start-up circuit.

this requirement is satisfied by choosing the aspect ratio of T_7 to be much larger than that of T_8 .

Another important aspect of the performance of biasing circuits is their dependence on temperature. This variation is most conveniently expressed in terms of the fractional change in output current per degree centigrade of temperature variation, which we call the fractional temperature coefficient TC_F :

$$TC_F = \frac{1}{I_{OUT}} \frac{\partial I_{OUT}}{\partial T} \quad (4.227)$$

For the V_{BE} -referenced circuit of Fig. 4.38a,

$$I_{\text{OUT}} = \frac{V_{BE1}}{R} \quad (4.228)$$

$$\frac{\partial I_{\text{OUT}}}{\partial T} = \frac{1}{R} \frac{\partial V_{BE1}}{\partial T} - \frac{V_{BE1}}{R^2} \frac{\partial R}{\partial T} \quad (4.229)$$

$$= I_{\text{OUT}} \left(\frac{1}{V_{BE1}} \frac{\partial V_{BE1}}{\partial T} - \frac{1}{R} \frac{\partial R}{\partial T} \right) \quad (4.230)$$

Therefore,

$$TC_F = \frac{1}{I_{\text{OUT}}} \frac{\partial I_{\text{OUT}}}{\partial T} = \frac{1}{V_{BE1}} \frac{\partial V_{BE1}}{\partial T} - \frac{1}{R} \frac{\partial R}{\partial T} \quad (4.231)$$

Thus the temperature dependence of the output current is related to the difference between the resistor temperature coefficient and that of the base-emitter junction. Since the former has a positive and the latter a negative coefficient, the net TC_F is quite large.

■ EXAMPLE

Design a bias reference as shown in Fig. 4.38a to produce 100 μA output current. Find the TC_F . Assume that for T_1 , $I_S = 10^{-14}$ A. Assume that $\partial V_{BE}/\partial T = -2\text{mV}^\circ\text{C}$ and that $(1/R)(\partial R/\partial T) = +1500 \text{ ppm}^\circ\text{C}$.

The current in T_1 will be equal to I_{OUT} , so that

$$V_{BE1} = V_T \ln \frac{100 \mu\text{A}}{10^{-14} \text{ A}} = 598 \text{ mV}$$

Thus from (4.228),

$$R = \frac{598 \text{ mV}}{0.1 \text{ mA}} = 5.98 \text{ k}\Omega$$

From (4.231),

$$TC_F \simeq \frac{-2 \text{ mV}^\circ\text{C}}{598 \text{ mV}} - 1.5 \times 10^{-3} \simeq -3.3 \times 10^{-3} - 1.5 \times 10^{-3}$$

and thus

$$TC_F \simeq -4.8 \times 10^{-3} \text{ }^\circ\text{C} = -4800 \text{ ppm}^\circ\text{C}$$

■ The term ppm is an abbreviation for parts per million and implies a multiplier of 10^{-6} .

For the threshold-referenced circuit of Fig. 4.38b,

$$I_{\text{OUT}} = \frac{V_{GS1}}{R} \simeq \frac{V_t}{R} \quad (4.232)$$

Differentiating (4.232) and substituting into (4.227) gives

$$TC_F = \frac{1}{I_{\text{OUT}}} \frac{\partial I_{\text{OUT}}}{\partial T} \simeq \frac{1}{V_t} \frac{\partial V_t}{\partial T} - \frac{1}{R} \frac{\partial R}{\partial T} \quad (4.233)$$

Since the threshold voltage of an MOS transistor and the base-emitter voltage of a bipolar transistor both change at about $-2 \text{ mV}^\circ\text{C}$, (4.233) and (4.231) show that the temperature dependence of the threshold-referenced current source in Fig. 4.38b is about the same as the V_{BE} -referenced current source in Fig. 4.38a.

V_{BE} -referenced bias circuits are also used in CMOS technology. An example is shown in Fig. 4.40, where the *pnp* transistor is the parasitic device inherent in *p*-substrate CMOS

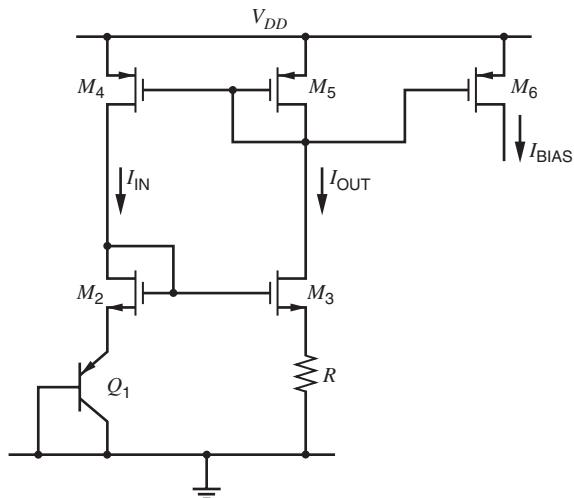


Figure 4.40 Example of a V_{BE} -referenced self-biased circuit in CMOS technology.

technologies. A corresponding circuit utilizing *npn* transistors can be used in *n*-substrate CMOS technologies. The feedback circuit formed by M_2 , M_3 , M_4 , and M_5 forces the current in transistor Q_1 to be the same as in resistor R . Assuming matched devices, $V_{GS2} = V_{GS3}$ and thus

$$I_{OUT} = \frac{V_{BE1}}{R} \quad (4.234)$$

An alternate source for the voltage reference is the thermal voltage V_T . The difference in junction potential between two junctions operated at different current densities can be shown to be proportional to V_T . This voltage difference must be converted to a current to provide the bias current. For the Widlar source shown in Fig. 4.31a, (4.190) shows that the voltage across the resistor R_2 is

$$I_{OUT}R_2 = V_T \ln \frac{I_{IN}}{I_{OUT}} \frac{I_{S2}}{I_{S1}} \quad (4.235)$$

Thus if the ratio of the input to the output current is held constant, the voltage across R_2 is indeed proportional to V_T . This fact is utilized in the self-biased circuit of Fig. 4.41. Here Q_3 and Q_4 are selected to have equal areas. Therefore, if we assume that $\beta_F \rightarrow \infty$ and $V_A \rightarrow \infty$, the current mirror formed by Q_3 and Q_4 forces the collector current of Q_1 to equal that of Q_2 . Figure 4.41 also shows that Q_2 has two emitters and Q_1 has one emitter, which indicates that the emitter area of Q_2 is twice that of Q_1 in this example. This selection is made to force the gain around the positive feedback loop at point B in Fig. 4.37b to be more than unity so that point B is an unstable operating point and a stable nonzero operating point exists at point A . As in other self-biased circuits, a start-up circuit is required to make sure that enough current flows to force operation at point A in Fig. 4.37b in practice. Under these conditions, $I_{S2} = 2I_{S1}$ and the voltage across R_2 is

$$I_{OUT}R_2 = V_T \ln \frac{I_{IN}}{I_{OUT}} \frac{I_{S2}}{I_{S1}} = V_T \ln 2 \quad (4.236)$$

Therefore, the output current is

$$I_{OUT} = \frac{V_T}{R_2} \ln 2 \quad (4.237)$$

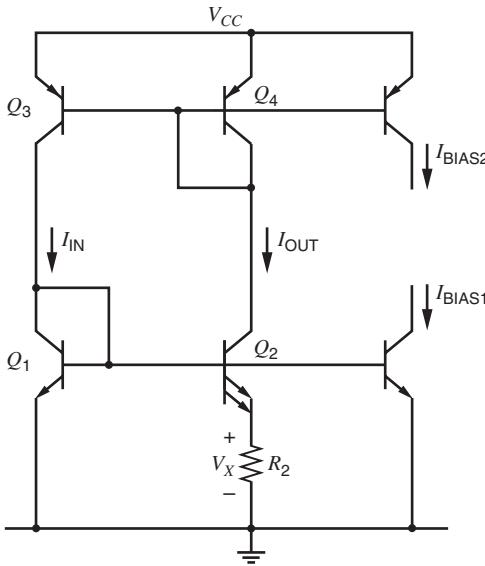


Figure 4.41 Bias current source using the thermal voltage.

The temperature variation of the output current can be calculated as follows. From (4.237)

$$\begin{aligned} \frac{\partial I_{\text{OUT}}}{\partial T} &= (\ln 2) \frac{R_2 \frac{\partial V_T}{\partial T} - V_T \frac{\partial R_2}{\partial T}}{R_2^2} \\ &= \frac{V_T}{R_2} (\ln 2) \left(\frac{1}{V_T} \frac{\partial V_T}{\partial T} - \frac{1}{R_2} \frac{\partial R_2}{\partial T} \right) \end{aligned} \quad (4.238)$$

Substituting (4.237) in (4.238) gives

$$TC_F = \frac{1}{I_{\text{OUT}}} \frac{\partial I_{\text{OUT}}}{\partial T} = \frac{1}{V_T} \frac{\partial V_T}{\partial T} - \frac{1}{R_2} \frac{\partial R_2}{\partial T} \quad (4.239)$$

This circuit produces much smaller temperature coefficient of the output current than the V_{BE} reference because the fractional sensitivities of both V_T and that of a diffused resistor R_2 are positive and tend to cancel in (4.239). We have chosen a transistor area ratio of two to one as an example. In practice, this ratio is often chosen to minimize the total area required for the transistors and for resistor R_2 .

■ EXAMPLE

Design a bias reference of the type shown in Fig. 4.41 to produce an output current of 100 μA . Find the TC_F of I_{OUT} . Assume the resistor temperature coefficient $(1/R)(\partial R/\partial T) = +1500 \text{ ppm}/^\circ\text{C}$.

From (4.237)

$$R_2 = \frac{V_T (\ln 2)}{I_{\text{OUT}}} = \frac{(26 \text{ mV})(\ln 2)}{100 \mu\text{A}} \simeq 180 \Omega$$

From (4.239)

$$\begin{aligned}\frac{1}{I_{\text{OUT}}} \frac{\partial I_{\text{OUT}}}{\partial T} &= \frac{1}{V_T} \frac{\partial V_T}{\partial T} - 1500 \times 10^{-6} = \frac{1}{V_T} \frac{V_T}{T} - 1500 \times 10^{-6} \\ &= \frac{1}{T} - 1500 \times 10^{-6}\end{aligned}$$

Assuming operation at room temperature, $T = 300^\circ\text{K}$ and

$$\frac{1}{I_{\text{OUT}}} \frac{\partial I_{\text{OUT}}}{\partial T} \simeq 3300 \times 10^{-6} - 1500 \times 10^{-6} = 1800 \text{ ppm}/^\circ\text{C}$$

V_T -referenced bias circuits are also commonly used in CMOS technology. A simple example is shown in Fig. 4.42, where bipolar transistors Q_1 and Q_2 are parasitic devices inherent in p -substrate CMOS technologies. Here the emitter areas of these transistors differ by a factor n , and the feedback loop forces them to operate at the same bias current. As a result, the difference between the two base-emitter voltages must appear across resistor R . The resulting current is

$$I_{\text{OUT}} = \frac{V_T \ln(n)}{R} \quad (4.240)$$

In the circuit of Fig. 4.42, small differences in the gate-source voltages of M_3 and M_4 result in large variations in the output current because the voltage drop across R is only on the order of 100 mV. Such gate-source voltage differences can result from device mismatches or from channel-length modulation in M_3 and M_4 because they have different drain-source voltages. Practical implementations of this circuit typically utilize large geometry devices for M_3 and M_4 to minimize offsets and cascode or Wilson current sources to minimize channel-length modulation effects. A typical example of a practical circuit is shown in Fig. 4.43. In general, cascoding is often used to improve the performance of reference circuits in all technologies. The main limitation of the application of cascoding is that it increases the minimum required power-supply voltage to operate all transistors in the active region.

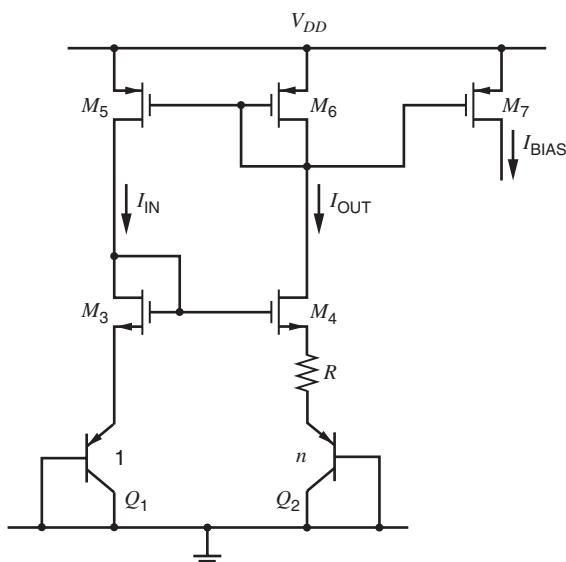


Figure 4.42 Example of a CMOS V_T -referenced self-biased circuit.

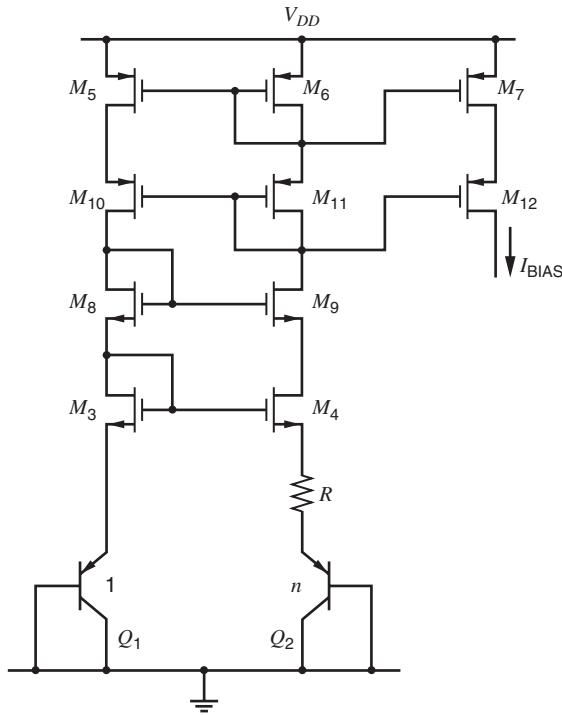


Figure 4.43 Example of a CMOS V_T -referenced self-biased reference circuit with cascoded devices to improve power-supply rejection and initial accuracy.

4.4.3 Temperature-Insensitive Biasing

As illustrated by the examples in Section 4.4.2, the base-emitter-voltage- and thermal-voltage-referenced circuits have rather high temperature coefficients of output current. Although the temperature sensitivity is reduced considerably in the thermal-voltage circuit, even its temperature coefficient is not low enough for many applications. Thus we are led to examine other possibilities for the realization of a biasing circuit with low temperature coefficient.

4.4.3.1 Band-Gap-Referenced Bias Circuits in Bipolar Technology

Since the bias sources referenced to $V_{BE(on)}$ and V_T have opposite TC_F , the possibility exists for referencing the output current to a composite voltage that is a weighted sum of $V_{BE(on)}$ and V_T . By proper weighting, zero temperature coefficient should be attainable.

In the biasing sources described so far, we have concentrated on the problem of obtaining a *current* with low temperature coefficient. In practice, requirements often arise for low-temperature-coefficient voltage bias or reference *voltages*. The voltage reference for a voltage regulator is a good example. The design of these two types of circuits is similar except that in the case of the current source, a temperature coefficient must be intentionally introduced into the voltage reference to compensate for the temperature coefficient of the resistor that will define the current. In the following description of the band-gap reference, we assume for simplicity that the objective is a *voltage* source of low temperature coefficient.

First consider the hypothetical circuit of Fig. 4.44. An output voltage is developed that is equal to $V_{BE(on)}$ plus a constant M times V_T . To determine the required value for M , we must determine the temperature coefficient of $V_{BE(on)}$. Neglecting base current,

$$V_{BE(on)} = V_T \ln \frac{I_1}{I_S} \quad (4.241)$$

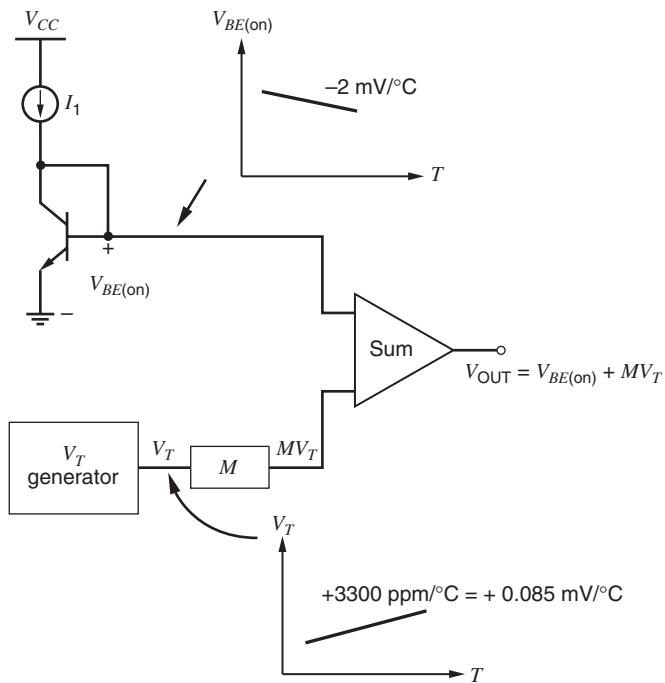


Figure 4.44 Hypothetical band-gap reference circuit.

As shown in Chapter 1, the saturation current I_S can be related to the device structure by

$$I_S = \frac{qA n_i^2 \bar{\mu}_n}{Q_B} = B n_i^2 \bar{\mu}_n = B' n_i^2 T \bar{\mu}_n \quad (4.242)$$

where n_i is the intrinsic minority-carrier concentration, Q_B is the total base doping per unit area, $\bar{\mu}_n$ is the average electron mobility in the base, A is the emitter-base junction area, and T is the temperature. Here, the constants B and B' involve only temperature-independent quantities. The Einstein relation $\mu_n = (q/kT)D_n$ was used to write I_S in terms of $\bar{\mu}_n$ and n_i^2 . The quantities in (4.242) that are temperature dependent are given by¹⁵

$$\bar{\mu}_n = CT^{-n} \quad (4.243)$$

$$n_i^2 = DT^3 \exp\left(-\frac{V_{G0}}{V_T}\right) \quad (4.244)$$

where V_{G0} is the band-gap voltage of silicon extrapolated to 0°K . Here again C and D are temperature-independent quantities whose exact values are unimportant in the analysis. The exponent n in the expression for base-region electron mobility $\bar{\mu}_n$ is dependent on the doping level in the base. Combining (4.241), (4.242), (4.243), and (4.244) yields

$$V_{BE(on)} = V_T \ln\left(I_1 T^{-\gamma} E \exp \frac{V_{G0}}{V_T}\right) \quad (4.245)$$

where E is another temperature-independent constant and

$$\gamma = 4 - n \quad (4.246)$$

In actual band-gap circuits, the current I_1 is not constant but varies with temperature. We assume for the time being that this temperature variation is known and that it can be written

in the form

$$I_1 = GT^\alpha \quad (4.247)$$

where G is another temperature-independent constant. Combining (4.245) and (4.247) gives

$$V_{BE(on)} = V_{G0} - V_T[(\gamma - \alpha) \ln T - \ln(EG)] \quad (4.248)$$

From Fig. 4.44, the output voltage is

$$V_{OUT} = V_{BE(on)} + MV_T \quad (4.249)$$

Substitution of (4.248) into (4.249) gives

$$V_{OUT} = V_{G0} - V_T(\gamma - \alpha) \ln T + V_T[M + \ln(EG)] \quad (4.250)$$

This expression gives the output voltage as a function of temperature in terms of the circuit parameters G , α , and M , and the device parameters E and γ . Our objective is to make V_{OUT} independent of temperature. To this end, we take the derivative of V_{OUT} with respect to temperature to find the required values of G , γ , and M to give zero TC_F . Differentiating (4.250) gives

$$0 = \frac{dV_{OUT}}{dT} \Big|_{T=T_0} = \frac{V_{T0}}{T_0}[M + \ln(EG)] - \frac{V_{T0}}{T_0}(\gamma - \alpha) \ln T_0 - \frac{V_{T0}}{T_0}(\gamma - \alpha) \quad (4.251)$$

where T_0 is the temperature at which the TC_F of the output is zero and V_{T0} is the thermal voltage V_T evaluated at T_0 . Equation 4.251 can be rearranged to give

$$[M + \ln(EG)] = (\gamma - \alpha) \ln T_0 + (\gamma - \alpha) \quad (4.252)$$

This equation gives the required values of circuit parameters M , α , and G in terms of the device parameters E and γ . In principle, these values could be calculated directly from (4.252). However, further insight is gained by back-substituting (4.252) into (4.250). The result is

$$V_{OUT} = V_{G0} + V_T(\gamma - \alpha) \left(1 + \ln \frac{T_0}{T} \right) \quad (4.253)$$

Thus the temperature dependence of the output voltage is entirely described by the single parameter T_0 , which in turn is determined by the constants M , E , and G .

Using (4.253), the output voltage at the zero TC_F temperature ($T = T_0$) is given by

$$V_{OUT}|_{T=T_0} = V_{G0} + V_{T0}(\gamma - \alpha) \quad (4.254)$$

For example, to achieve zero TC_F at 27°C , assuming that $\gamma = 3.2$ and $\alpha = 1$,

$$V_{OUT}|_{T=T_0=25^\circ\text{C}} = V_{G0} + 2.2V_{T0} \quad (4.255)$$

The band-gap voltage of silicon is $V_{G0} = 1.205$ V so that

$$V_{OUT}|_{T=T_0=25^\circ\text{C}} = 1.205 \text{ V} + (2.2)(0.026 \text{ V}) = 1.262 \text{ V} \quad (4.256)$$

Therefore, the output voltage for zero temperature coefficient is close to the band-gap voltage of silicon, which explains the name given to these bias circuits.

Differentiating (4.253) with respect to temperature yields

$$\begin{aligned} \frac{dV_{OUT}}{dT} &= \frac{1}{T} \left[V_T(\gamma - \alpha) \left(1 + \ln \frac{T_0}{T} \right) \right] - \frac{V_T}{T}(\gamma - \alpha) \\ &= (\gamma - \alpha) \frac{V_T}{T} \left(\ln \frac{T_0}{T} \right) \end{aligned} \quad (4.257)$$

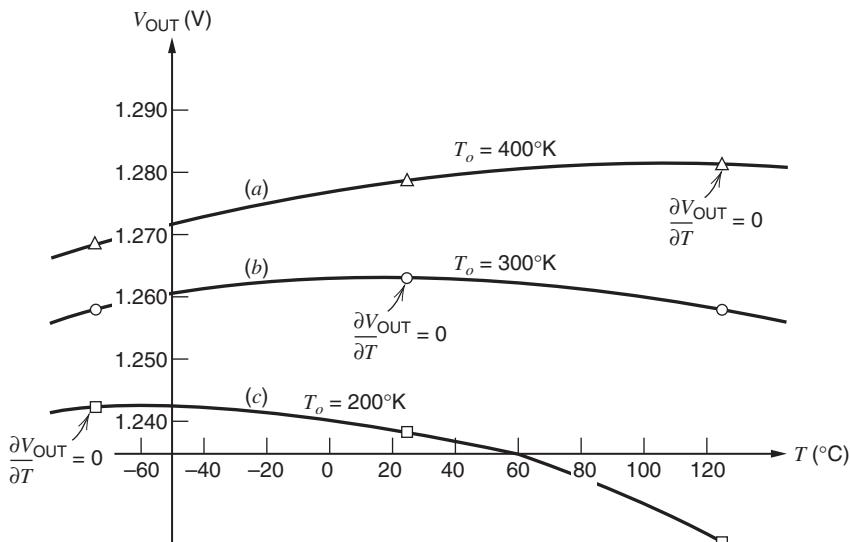


Figure 4.45 Variation of band-gap reference output voltage with temperature.

Equation 4.257 gives the slope of the output as a function of temperature. A typical family of output-voltage-variation characteristics is shown in Fig. 4.45 for different values of T_0 for the special case in which $\alpha = 0$ and I_1 is temperature independent. The slope of each curve is zero at $T = T_0$. When $T < T_0$, the slope is positive because the argument of the logarithm in (4.257) is more than unity. Similarly, the slope is negative when $T > T_0$. For values of T near T_0 ,

$$\ln \frac{T_0}{T} = \ln \left(1 + \frac{T_0 - T}{T} \right) \simeq \frac{T_0 - T}{T} \quad (4.258)$$

and we have

$$\frac{dV_{\text{OUT}}}{dT} \simeq (\gamma - \alpha) \frac{V_T}{T} \left(\frac{T_0 - T}{T} \right) \quad (4.259)$$

As shown by (4.257) and (4.259), the temperature coefficient of the output is zero only at one temperature $T = T_0$. This result stems from the addition of a weighted thermal voltage to a base-emitter voltage as in Fig. 4.44. Since the temperature coefficient of base-emitter voltage is not exactly constant, the gain M can be chosen to set the temperature coefficient of the output to zero only at one temperature. In other words, the thermal voltage generator is used to cancel the linear dependence of the base-emitter voltage with temperature. After this cancellation, the changing outputs in Fig. 4.45 stem from the nonlinear dependence of the base-emitter voltage with temperature. Band-gap references that compensate for this nonlinearity are said to be *curvature compensated*.^{16,17,18}

EXAMPLE

A band-gap reference is designed to give a nominal output voltage of 1.262 V, which gives zero TC_F at 27°C . Because of component variations, the actual room temperature output voltage is 1.280 V. Find the temperature of actual zero TC_F of V_{OUT} . Also, write an equation for V_{OUT} as a function of temperature, and calculate the TC_F at room temperature. Assume that $\gamma = 3.2$ and $\alpha = 1$.

From (4.253) at $T = 27^\circ\text{C} = 300^\circ\text{K}$,

$$1.280 \text{ V} = 1.205 + (0.026 \text{ V})(2.2) \left(1 + \ln \frac{T_0}{300^\circ\text{K}} \right)$$

and thus

$$T_0 = 300^\circ\text{K} \left(\exp \frac{18 \text{ mV}}{57 \text{ mV}} \right) = 411^\circ\text{K}$$

Therefore, the TC_F will be zero at $T_0 = 411^\circ\text{K} = 138^\circ\text{C}$, and we can express V_{OUT} as

$$V_{\text{OUT}} = 1.205 \text{ V} + 57 \text{ mV} \left(1 + \ln \frac{411^\circ\text{K}}{T} \right)$$

From (4.259) with $T = 300^\circ\text{K}$ and $T_0 = 411^\circ\text{K}$,

$$\frac{dV_{\text{OUT}}}{dT} \simeq (2.2) \frac{26 \text{ mV}}{300^\circ\text{K}} \left(\frac{411 - 300}{300} \right) \simeq 70 \mu\text{V}/^\circ\text{K} = 70 \mu\text{V}/^\circ\text{C}$$

Therefore, the TC_F at room temperature is

$$TC_F = \frac{1}{V_{\text{OUT}}} \frac{dV_{\text{OUT}}}{dT} \simeq \frac{70 \mu\text{V}/^\circ\text{C}}{1.280 \text{ V}} \simeq 55 \text{ ppm}/^\circ\text{C}$$

To reduce the TC_F , the constant M in (4.249)–(4.252) is often trimmed at one temperature so that the band-gap output is set to a desired target voltage.¹⁹ In principle, the target voltage is given by (4.253). In practice, however, significant inaccuracy in (4.253) stems from an approximation in (4.244).²⁰ As a result, the target voltage is usually determined experimentally by measuring the TC_F directly for several samples of each band-gap reference in a given process.^{21,22} This procedure reduces the TC_F at the reference temperature to a level of about 10 ppm/ $^\circ\text{C}$.

A key parameter of interest in reference sources is the variation of the output that is encountered over the entire temperature range. Since the TC_F expresses the temperature sensitivity only at one temperature, a different parameter must be used to characterize the behavior of the circuit over a broad temperature range. An effective temperature coefficient can be defined for a voltage reference as

$$TC_{F(\text{eff})} = \frac{1}{V_{\text{OUT}}} \left(\frac{V_{\text{MAX}} - V_{\text{MIN}}}{T_{\text{MAX}} - T_{\text{MIN}}} \right) \quad (4.260)$$

where V_{MAX} and V_{MIN} are the largest and smallest output voltages observed over the temperature range, and $T_{\text{MAX}} - T_{\text{MIN}}$ is the temperature excursion. V_{OUT} is the nominal output voltage. By this standard, $TC_{F(\text{eff})}$ over the -55 to 125°C range for case (b) of Fig. 4.45 is 44 ppm/ $^\circ\text{C}$. If the temperature range is restricted to 0 to 70°C , $TC_{F(\text{eff})}$ improves to 17 ppm/ $^\circ\text{C}$. Thus over a restricted temperature range, this reference is comparable with the standard cell in temperature stability once the zero TC_F temperature has been set at room temperature. Saturated standard cells (precision batteries) have a TC_F of about ± 30 ppm/ $^\circ\text{C}$.

Practical realizations of band-gap references in bipolar technologies take on several forms.^{15,19,23} One such circuit is illustrated in Fig. 4.46a.¹⁵ This circuit uses a feedback loop to establish an operating point in the circuit such that the output voltage is equal to a $V_{BE(\text{on})}$ plus a voltage proportional to the difference between two base-emitter voltages. The operation of the feedback loop is best understood by reference to Fig. 4.46b, in which a portion of the circuit is shown. We first consider the variation of the output voltage V_2 as the input voltage V_1 is varied from zero in the positive direction. Initially, with $V_1 = 0$, devices Q_1 and Q_2 do not

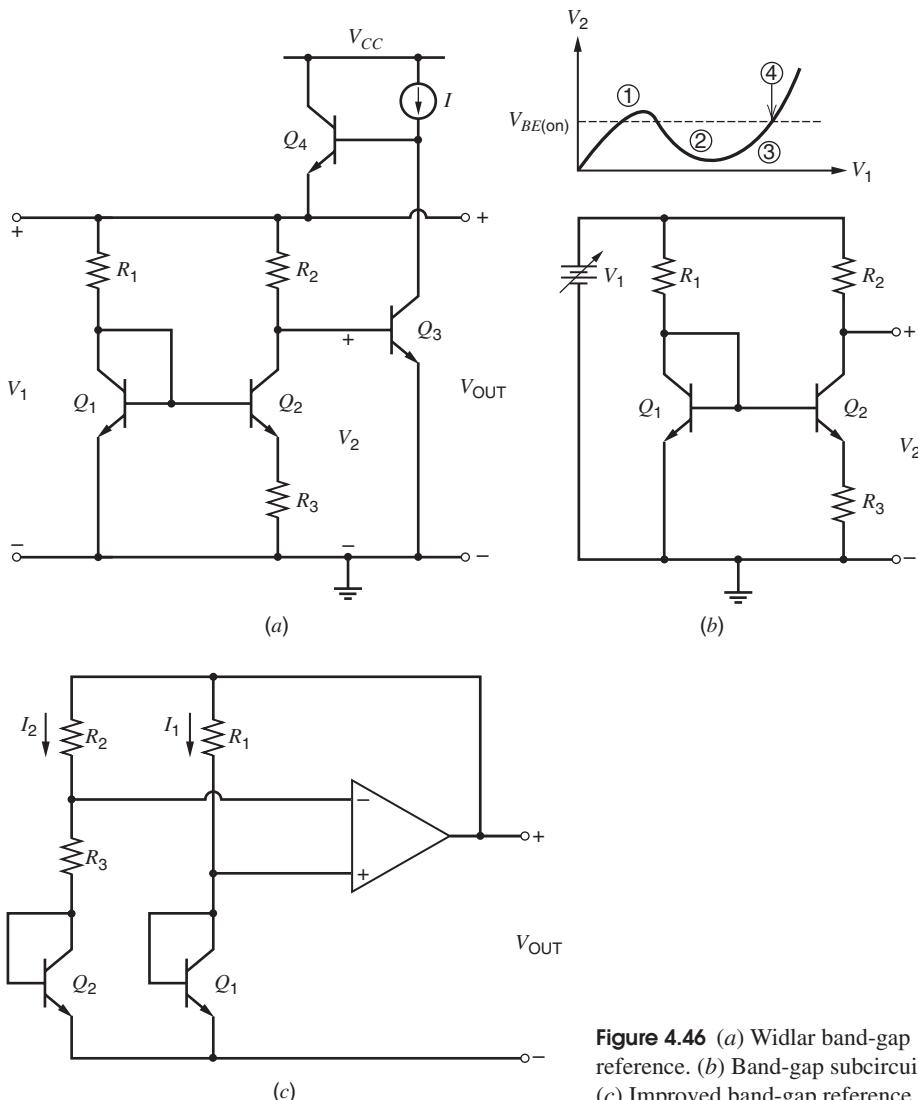


Figure 4.46 (a) Widlar band-gap reference. (b) Band-gap subcircuit. (c) Improved band-gap reference.

conduct and $V_2 = 0$. As V_1 is increased, Q_1 and Q_2 do not conduct significant current until the input voltage reaches about 0.6 V. When $V_1 < 0.6$ V, $V_2 = V_1$ since the voltage drop on R_2 is zero. When V_1 exceeds 0.6 V, however, Q_1 begins to conduct current, corresponding to point ① in Fig. 4.46b. The magnitude of the current in Q_1 is roughly equal to $(V_1 - 0.6 \text{ V})/R_1$. For small values of this current, Q_1 and Q_2 carry the same current because the drop across R_3 is negligible at low currents. Since R_2 is much larger than R_1 , the voltage drop across R_2 is much larger than $(V_1 - 0.6 \text{ V})$, and transistor Q_2 saturates, corresponding to point ② in Fig. 4.46b. Because of the presence of R_3 , the collector current that would flow in Q_2 if it were in the forward-active region has an approximately logarithmic dependence on V_1 , exactly as in the Widlar source. Thus as V_1 is further increased, a point is reached at which Q_2 comes out of saturation because V_1 increases faster than the voltage drop across R_2 . This point is labeled point ③ in Fig. 4.46b.

Now consider the complete circuit of Fig. 4.46a. If transistor Q_3 is initially turned off, transistor Q_4 will drive V_1 in the positive direction. This process will continue until enough voltage is developed at the base of Q_3 to produce a collector current in Q_3 approximately equal to I . Thus the circuit stabilizes with voltage V_2 equal to one diode drop, the base-emitter voltage of Q_3 , which can occur at point ① or point ④ in Fig. 4.46b. Appropriate start-up circuitry must be included to ensure operation at point ④.

Assuming that the circuit has reached a stable operating point at point ④, the output voltage V_{OUT} is the sum of the base-emitter voltage of Q_3 and the voltage drop across R_2 . The drop across R_2 is equal to the voltage drop across R_3 multiplied by R_2/R_3 because the collector current of Q_2 is approximately equal to its emitter current. The voltage drop across R_3 is equal to the difference in base-emitter voltages of Q_1 and Q_2 . The ratio of currents in Q_1 and Q_2 is set by the ratio of R_2 to R_1 .

A drawback of this reference is that the current I is set by the power supply and may vary with power-supply variations. A self-biased band-gap reference circuit is shown in Fig. 4.46c. Assume that a stable operating point exists for this circuit and that the op amp is ideal. Then the differential input voltage of the op amp must be zero and the voltage drops across resistors R_1 and R_2 are equal. Thus the ratio of R_2 to R_1 determines the ratio of I_1 to I_2 . These two currents are the collector currents of the two diode-connected transistors Q_2 and Q_1 , assuming base currents are negligible. The voltage across R_3 is

$$V_{R3} = \Delta V_{BE} = V_{BE1} - V_{BE2} = V_T \ln \frac{I_1 I_{S2}}{I_2 I_{S1}} = V_T \ln \frac{R_2}{R_1} \frac{I_{S2}}{I_{S1}} \quad (4.261)$$

Since the same current that flows in R_3 also flows in R_2 , the voltage across R_2 must be

$$V_{R2} = \frac{R_2}{R_3} V_{R3} = \frac{R_2}{R_3} \Delta V_{BE} = \frac{R_2}{R_3} V_T \ln \frac{R_2}{R_1} \frac{I_{S2}}{I_{S1}} \quad (4.262)$$

This equation shows that the voltage across R_2 is proportional to absolute temperature (PTAT) because of the temperature dependence of the thermal voltage. Since the op amp forces the voltages across R_1 and R_2 to be equal, the currents I_1 and I_2 are both proportional to temperature if the resistors have zero temperature coefficient. Thus for this reference, $\alpha = 1$ in (4.247). The output voltage is the sum of the voltage across Q_2 , R_3 , and R_2 :

$$\begin{aligned} V_{\text{OUT}} &= V_{BE2} + V_{R3} + V_{R2} = V_{BE2} + \left(1 + \frac{R_2}{R_3}\right) \Delta V_{BE} \\ &= V_{BE2} + \left(1 + \frac{R_2}{R_3}\right) V_T \ln \frac{R_2}{R_1} \frac{I_{S2}}{I_{S1}} = V_{BE2} + M V_T \end{aligned} \quad (4.263)$$

The circuit thus behaves as a band-gap reference, with the value of M set by the ratios of R_2/R_3 , R_2/R_1 , and I_{S2}/I_{S1} .

4.4.3.2 Band-Gap-Referenced Bias Circuits in CMOS Technology

Band-gap-referenced biasing also can be implemented using the parasitic bipolar devices inherent in CMOS technology. For example, in a n -well process, substrate pnp transistors can be used to replace the npn transistors in Fig. 4.46c, as shown in Fig. 4.47. Assume that the CMOS op amp has infinite gain but nonzero input-referred offset voltage V_{OS} . (The input-referred offset voltage of an op amp is defined as the differential input voltage required to drive the output to zero.) Because of the threshold mismatch and the low transconductance per current of CMOS transistors, the offset of op amps in CMOS technologies is usually larger than in bipolar technologies. With the offset voltage, the voltage across R_3 is

$$V_{R3} = V_{EB1} - V_{EB2} + V_{OS} = \Delta V_{EB} + V_{OS} \quad (4.264)$$

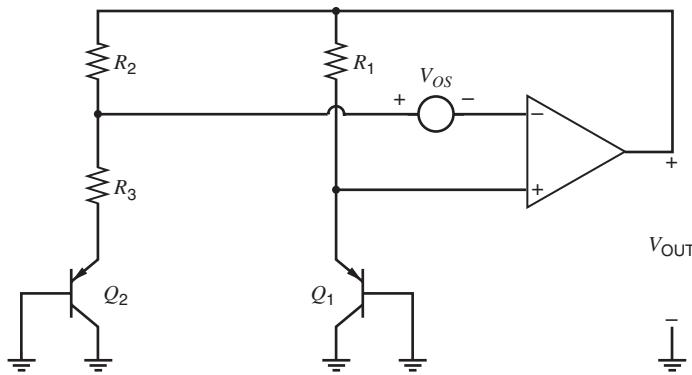


Figure 4.47 A band-gap reference in *n*-well CMOS.

The emitter-base voltages are used here because the base-emitter voltages of the *pnp* transistors operating in the forward-active region are negative. Then the voltage across R_2 is

$$V_{R2} = \frac{R_2}{R_3} V_{R3} = \frac{R_2}{R_3} (V_{EB1} - V_{EB2} + V_{OS}) = \frac{R_2}{R_3} (\Delta V_{EB} + V_{OS}) \quad (4.265)$$

and the output voltage is¹⁸

$$\begin{aligned} V_{OUT} &= V_{EB2} + V_{R3} + V_{R2} \\ &= V_{EB2} + \left(1 + \frac{R_2}{R_3}\right) (\Delta V_{EB} + V_{OS}) \end{aligned} \quad (4.266)$$

Since the difference in the base-emitter voltages is proportional to the thermal voltage, comparing (4.266) with $V_{OS} = 0$ to (4.249) shows that the gain M here is proportional to $(1 + R_2/R_3)$. Rearranging (4.266) gives

$$V_{OUT} = V_{EB2} + \left(1 + \frac{R_2}{R_3}\right) (\Delta V_{EB}) + V_{OS(\text{out})} \quad (4.267)$$

where the output-referred offset is

$$V_{OS(\text{out})} = \left(1 + \frac{R_2}{R_3}\right) V_{OS} \quad (4.268)$$

Equations 4.267 and 4.268 show that the output contains an offset voltage that is a factor of $(1 + R_2/R_3)$ times bigger than the input-referred offset voltage. Therefore, the same gain that is applied to the difference in the base-emitter voltages is also applied to the input-referred offset voltage.

Assume that the offset voltage is independent of temperature. To set TC_F of the output equal to zero, the gain must be changed so that temperature coefficients of the V_{EB} and ΔV_{EB} terms cancel. Since the offset is assumed to be temperature independent, this cancellation occurs when the output is equal to the target, where zero offset was assumed, plus the output-referred offset. If the gain is trimmed at $T = T_0$ to set the output to a target voltage assuming the offset is zero, (4.267) shows that the gain is too small if the offset voltage is positive and that the gain is too big if the offset voltage is negative. Since the gain is applied to the PTAT term, the resulting slope of the output versus temperature is negative when the offset is positive and the gain is too small. On the other hand, this slope is positive when the offset is negative and the gain is too big.

We will now calculate the magnitude of the slope of the output versus temperature at $T = T_0$. With zero offset and a target that assumes zero offset, trimming R_2 and/or R_3 to set the output in (4.267) to the target forces the slope of the ΔV_{EB} term to cancel the slope of the V_{EB} term. With nonzero offset but the same target, the factor $(1 + R_2/R_3)$ differs from its ideal value after trimming by $-V_{OS(\text{out})}/\Delta V_{EB}$. Since this error is multiplied by ΔV_{EB} in (4.267), the resulting slope of the output versus temperature is

$$\frac{dV_{\text{OUT}}}{dT} \Big|_{T=T_0} = - \left(\frac{V_{OS(\text{out})}}{\Delta V_{EB}} \right) \frac{d\Delta V_{EB}}{dT} \quad (4.269)$$

Since ΔV_{EB} is proportional to the thermal voltage V_T ,

$$\Delta V_{EB} = HV_T \quad (4.270)$$

where H is a temperature-independent constant. Substituting (4.270) into (4.269) gives

$$\frac{dV_{\text{OUT}}}{dT} \Big|_{T=T_0} = - \frac{V_{OS(\text{out})}}{HV_T} \frac{HV_T}{T} \Big|_{T=T_0} = - \frac{V_{OS(\text{out})}}{T_0} \quad (4.271)$$

Therefore, when the gain is trimmed at one temperature to set the band-gap output to a desired target voltage, variation in the op-amp offset causes variation in the output temperature coefficient. In practice, the op-amp offset is usually the largest source of nonzero temperature coefficient.¹⁸ Equation 4.271 shows that the temperature coefficient at $T = T_0$ is proportional to the output-referred offset under these circumstances. Furthermore, (4.268) shows that the output-referred offset is equal to the gain that is applied to the ΔV_{EB} term times the input-referred offset. Therefore, minimizing this gain minimizes the variation in the temperature coefficient at the output. Since the reference output at $T = T_0$ for zero TC_F is approximately equal to the band-gap voltage, the required gain can be minimized by maximizing the ΔV_{EB} term.

To maximize the ΔV_{EB} term, designers generally push a large current into a small transistor and a small current into a large transistor, as shown in Fig. 4.48. Ignoring base currents,

$$\Delta V_{EB} = V_{EB1} - V_{EB2} = V_T \ln \left(\frac{I_1 I_{S2}}{I_2 I_{S1}} \right) \quad (4.272)$$

Equation 4.272 shows that maximizing the product of the ratios I_1/I_2 and I_{S2}/I_{S1} maximizes ΔV_{EB} . In Fig. 4.48, $I_1 > I_2$ is emphasized by drawing the symbol for I_1 larger than the symbol for I_2 . Similarly, the emitter area of Q_2 is larger than that of Q_1 to make $I_{S2} > I_{S1}$,

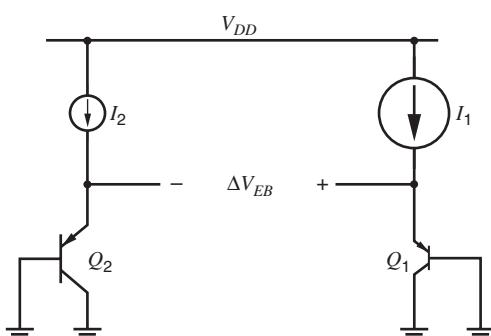


Figure 4.48 A circuit that increases ΔV_{EB} by increasing I_1/I_2 and I_{S2}/I_{S1} .

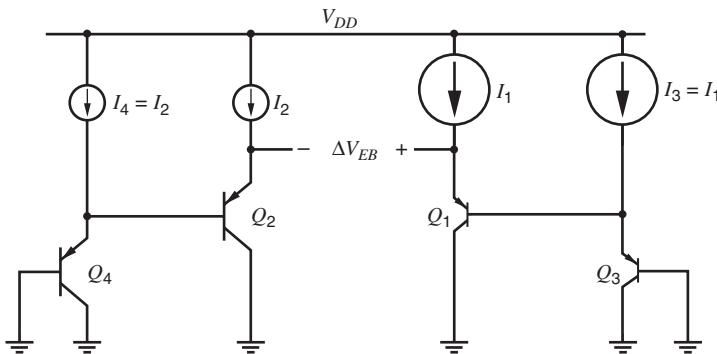


Figure 4.49 A circuit that cascades emitter followers to double ΔV_{EB} if $I_{S3} = I_{S1}$ and $I_{S4} = I_{S2}$.

and this relationship is shown by drawing the symbol of Q_2 larger than the symbol of Q_1 .²⁴ In practice, these ratios are often each set to be about equal to ten, and the resulting $\Delta V_{EB} \simeq 120$ mV at room temperature. Because the logarithm function compresses its argument, however, a limitation of this approach arises. For example, if the argument is increased by a factor of ten, ΔV_{EB} increases by only $V_T \ln(10) \simeq 60$ mV. Therefore, to double ΔV_{EB} to 240 mV, $(I_1/I_2)(I_{S2}/I_{S1})$ must be increased by a factor of 100 to 10,000. On the other hand, if Q_1 and the transistors that form I_2 are minimum-sized devices when $(I_1/I_2)(I_{S2}/I_{S1}) = 100$, the required die area would be dominated by the biggest devices (Q_2 and/or the transistors that form I_1). Therefore, increasing $(I_1/I_2)(I_{S2}/I_{S1})$ from 100 to 10,000 would increase the die area by about a factor of 100 but only double ΔV_{EB} .

To overcome this limitation, stages that each contribute to ΔV_{EB} can be cascaded.²⁵ For example, consider Fig. 4.49, where two emitter-follower stages are cascaded. Here

$$\Delta V_{EB} = V_{EB3} - V_{EB4} + V_{EB1} - V_{EB2} \quad (4.273)$$

Assume the new devices in Fig. 4.49 are identical to the corresponding original devices in Fig. 4.48 so that $I_3 = I_1$, $I_4 = I_2$, $I_{S3} = I_{S1}$, and $I_{S4} = I_{S2}$. Then ignoring base currents

$$\Delta V_{EB} = 2(V_{EB1} - V_{EB2}) = 2V_T \ln \left(\frac{I_1}{I_2} \frac{I_{S2}}{I_{S1}} \right) \quad (4.274)$$

Thus cascading two identical emitter followers doubles ΔV_{EB} while only doubling the required die area.

The effect of the offset in a band-gap reference can also be reduced by using offset cancellation. An example of offset cancellation in a CMOS band-gap reference with curvature correction in addition to an analysis of other high-order effects arising from finite β_F , β_F mismatch, β_F variation with temperature, nonzero base resistance, and nonzero temperature coefficient in the resistors is presented in Ref. 18.

A high-performance CMOS band-gap reference is shown in Fig. 4.50, where cascaded current mirrors are used to improve supply rejection. A V_T -dependent current from M_{11} develops a V_T -dependent voltage across resistor xR . A proper choice of the ratio x can give a band-gap voltage at V_{OUT} . If desired, a temperature-independent output current can be realized by choosing x to give an appropriate temperature coefficient to V_{OUT} to cancel the temperature coefficient of resistor R_2 .

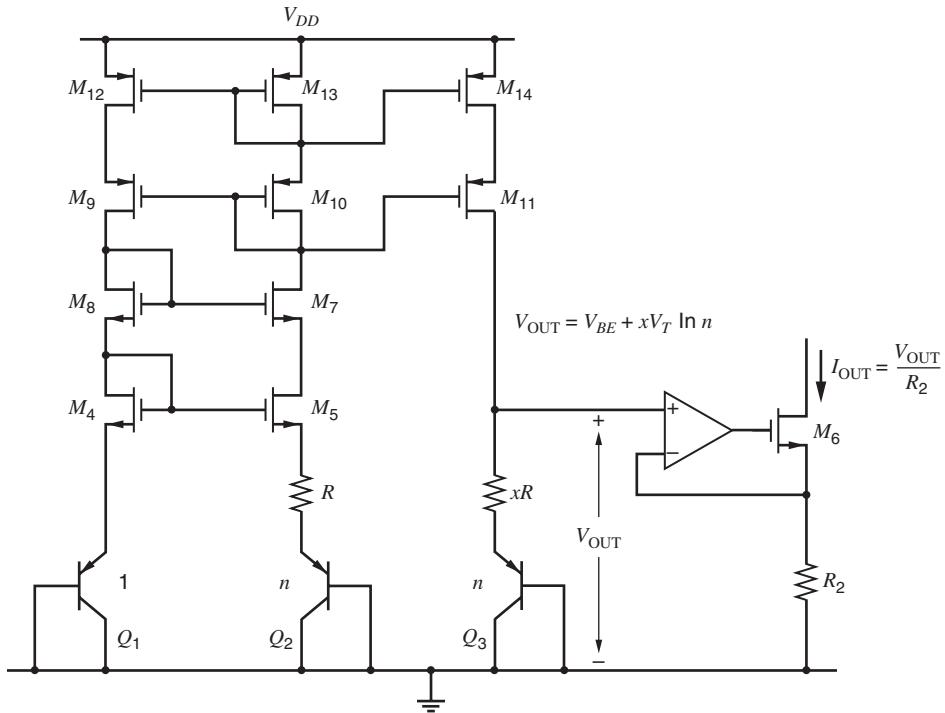


Figure 4.50 Example of a V_{BE} -referenced self-biased reference circuit in CMOS technology.

APPENDIX

A.4.1 MATCHING CONSIDERATIONS IN CURRENT MIRRORS

In many types of circuits, an objective of current-mirror design is generation of two or more current sources whose values are identical. This objective is particularly important in the design of digital-to-analog converters, operational amplifiers, and instrumentation amplifiers. We first examine the factors affecting matching in active current mirrors in bipolar technologies and then in MOS technologies.

A.4.1.1 BIPOLAR

Consider the bipolar current mirror with two outputs in Fig. 4.51. If the resistors and transistors are identical and the collector voltages are the same, the collector currents will match precisely. However, mismatch in the transistor parameters α_F and I_S and in the emitter resistors will cause the currents to be unequal. For Q_3 ,

$$V_T \ln \frac{I_{C3}}{I_{S3}} + \frac{I_{C3}}{\alpha_{F3}} R_3 = V_B \quad (4.275)$$

For Q_4 ,

$$V_T \ln \frac{I_{C4}}{I_{S4}} + \frac{I_{C4}}{\alpha_{F4}} R_4 = V_B \quad (4.276)$$

Subtraction of these two equations gives

$$V_T \ln \frac{I_{C3}}{I_{C4}} - V_T \ln \frac{I_{S3}}{I_{S4}} + \frac{I_{C3}}{\alpha_{F3}} R_3 - \frac{I_{C4}}{\alpha_{F4}} R_4 = 0 \quad (4.277)$$

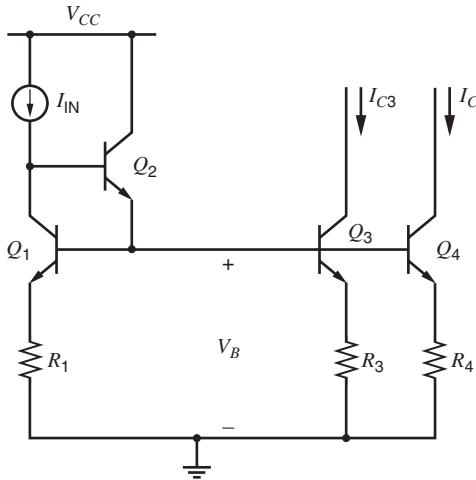


Figure 4.51 Matched bipolar current sources.

We now define *average* and *mismatch* parameters as follows:

$$I_C = \frac{I_{C3} + I_{C4}}{2} \quad (4.278)$$

$$\Delta I_C = I_{C3} - I_{C4} \quad (4.279)$$

$$I_S = \frac{I_{S3} + I_{S4}}{2} \quad (4.280)$$

$$\Delta I_S = I_{S3} - I_{S4} \quad (4.281)$$

$$R = \frac{R_3 + R_4}{2} \quad (4.282)$$

$$\Delta R = R_3 - R_4 \quad (4.283)$$

$$\alpha_F = \frac{\alpha_{F3} + \alpha_{F4}}{2} \quad (4.284)$$

$$\Delta \alpha_F = \alpha_{F3} - \alpha_{F4} \quad (4.285)$$

These relations can be inverted to give the original parameters in terms of the average and mismatch parameters. For example,

$$I_{C3} = I_C + \frac{\Delta I_C}{2} \quad (4.286)$$

$$I_{C4} = I_C - \frac{\Delta I_C}{2} \quad (4.287)$$

This set of equations for the various parameters is now substituted into (4.277). The result is

$$V_T \ln \left(\frac{I_C + \frac{\Delta I_C}{2}}{I_C - \frac{\Delta I_C}{2}} \right) - V_T \ln \left(\frac{I_S + \frac{\Delta I_S}{2}}{I_S - \frac{\Delta I_S}{2}} \right) + \frac{\left(I_C + \frac{\Delta I_C}{2} \right) \left(R + \frac{\Delta R}{2} \right)}{\alpha_F + \frac{\Delta \alpha_F}{2}} - \frac{\left(I_C - \frac{\Delta I_C}{2} \right) \left(R - \frac{\Delta R}{2} \right)}{\alpha_F - \frac{\Delta \alpha_F}{2}} = 0 \quad (4.288)$$

The first term in this equation can be rewritten as

$$V_T \ln \left(\frac{I_C + \frac{\Delta I_C}{2}}{I_C - \frac{\Delta I_C}{2}} \right) = V_T \ln \left(\frac{1 + \frac{\Delta I_C}{2I_C}}{1 - \frac{\Delta I_C}{2I_C}} \right) \quad (4.289)$$

If $\Delta I_C / 2I_C \ll 1$, this term can be rewritten as

$$V_T \ln \left(\frac{1 + \frac{\Delta I_C}{2I_C}}{1 - \frac{\Delta I_C}{2I_C}} \right) \simeq V_T \ln \left[\left(1 + \frac{\Delta I_C}{2I_C} \right) \left(1 + \frac{\Delta I_C}{2I_C} \right) \right] \quad (4.290)$$

$$\simeq V_T \ln \left[1 + \frac{\Delta I_C}{I_C} + \left(\frac{\Delta I_C}{2I_C} \right)^2 \right] \quad (4.291)$$

$$\simeq V_T \ln \left(1 + \frac{\Delta I_C}{I_C} \right) \quad (4.292)$$

where the squared term is neglected. The logarithm function has the infinite series

$$\ln(1 + x) = x - \frac{x^2}{2} + \dots \quad (4.293)$$

If $x \ll 1$,

$$\ln(1 + x) \simeq x \quad (4.294)$$

To simplify (4.292) when $\Delta I_C / I_C \ll 1$, let $x = \Delta I_C / I_C$. Then

$$V_T \ln \left(\frac{I_C + \frac{\Delta I_C}{2}}{I_C - \frac{\Delta I_C}{2}} \right) \simeq V_T \frac{\Delta I_C}{I_C} \quad (4.295)$$

Applying the same approximations to the other terms in (4.288), we obtain

$$\frac{\Delta I_C}{I_C} \simeq \left(\frac{1}{1 + \frac{g_m R}{\alpha_F}} \right) \frac{\Delta I_S}{I_S} + \frac{\frac{g_m R}{\alpha_F}}{1 + \frac{g_m R}{\alpha_F}} \left(-\frac{\Delta R}{R} + \frac{\Delta \alpha_F}{\alpha_F} \right) \quad (4.296)$$

We will consider two important limiting cases. First, since $g_m = I_C / V_T$, when $g_m R \ll 1$, the voltage drop on an emitter resistor is much smaller than the thermal voltage. In this case, the second term in (4.296) is small and the mismatch is mainly determined by the transistor I_S mismatch in the first term. Observed mismatches in I_S typically range from ± 10 to ± 1 percent depending on geometry. Second, when $g_m R \gg 1$, the voltage drop on an emitter resistor is much larger than the thermal voltage. In this case, the first term in (4.296) is small and the mismatch is mainly determined by the resistor mismatch and transistor α_F mismatch in the second term. Resistor mismatch typically ranges from ± 2 to ± 0.1 percent depending on geometry, and α_F matching is in the ± 0.1 percent range for *npn* transistors. Thus for *npn* current sources, the use of emitter resistors offers significantly improved current matching. On the other hand, for *pnp* current sources, the α_F mismatch is larger due to the lower β_F , typically around ± 1 percent. Therefore, the advantage of emitter degeneration is less significant with *pnp* than *npn* current sources.

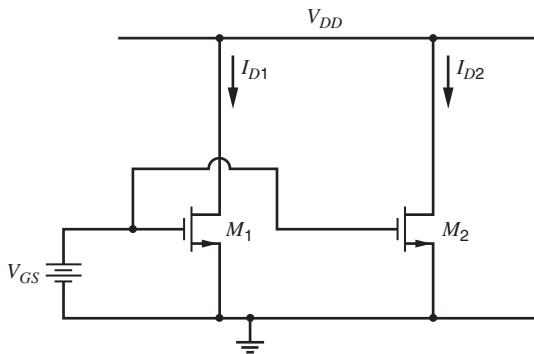


Figure 4.52 Matched MOS current sources.

A.4.1.2 MOS

Matched current sources are often required in MOS analog integrated circuits. The factors affecting this mismatch can be calculated using the circuit of Fig. 4.52. The two transistors M_1 and M_2 will have mismatches in their W/L ratios and threshold voltages. The drain currents are given by

$$I_{D1} = \frac{1}{2} \mu_n C_{ox} \left(\frac{W}{L} \right)_1 (V_{GS} - V_{t1})^2 \quad (4.297)$$

$$I_{D2} = \frac{1}{2} \mu_n C_{ox} \left(\frac{W}{L} \right)_2 (V_{GS} - V_{t2})^2 \quad (4.298)$$

Defining average and mismatch quantities, we have

$$I_D = \frac{I_{D1} + I_{D2}}{2} \quad (4.299)$$

$$\Delta I_D = I_{D1} - I_{D2} \quad (4.300)$$

$$\frac{W}{L} = \frac{1}{2} \left[\left(\frac{W}{L} \right)_1 + \left(\frac{W}{L} \right)_2 \right] \quad (4.301)$$

$$\Delta \frac{W}{L} = \left(\frac{W}{L} \right)_1 - \left(\frac{W}{L} \right)_2 \quad (4.302)$$

$$V_t = \frac{V_{t1} + V_{t2}}{2} \quad (4.303)$$

$$\Delta V_t = V_{t1} - V_{t2} \quad (4.304)$$

Substituting these expressions into (4.297) and (4.298) and neglecting high-order terms, we obtain

$$\frac{\Delta I_D}{I_D} = \frac{\Delta \frac{W}{L}}{\frac{W}{L}} - \frac{\Delta V_t}{(V_{GS} - V_t)/2} \quad (4.305)$$

The current mismatch consists of two components. The first is geometry dependent and contributes a fractional current mismatch that is independent of bias point. The second is dependent on threshold voltage mismatch and increases as the overdrive ($V_{GS} - V_t$) is reduced. This change occurs because as the overdrive is reduced, the fixed threshold mismatch progressively becomes a larger fraction of the total gate drive that is applied to the transistors and therefore contributes a progressively larger percentage error to the current mismatch. In practice, these

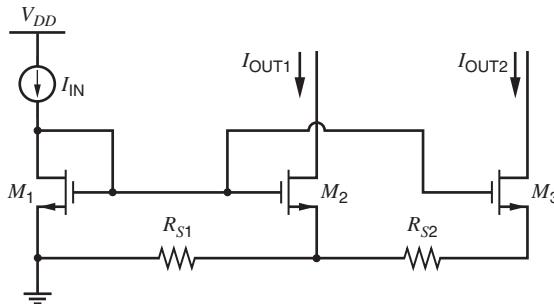


Figure 4.53 Current mirror with two outputs used to compare voltage- and current-routing techniques.

observations are important because they affect the techniques used to distribute bias signals on integrated circuits.

Consider the current mirror shown in Fig. 4.53, which has one input and two outputs. At first, assume that $R_{S1} = R_{S2} = 0$. Also, assume that the input current is generated by a circuit with desirable properties. For example, a self-biased band-gap reference might be used to make I_{IN} insensitive to changes in the power supply and temperature. Finally, assume that each output current is used to provide the required bias in one analog circuit on the integrated circuit (IC). For example, M_2 and M_3 could each act as the tail current source of a differential pair.

One way to build the circuit in Fig. 4.53 is to place M_1 on the IC near the input current source I_{IN} , while M_2 and M_3 are placed near the circuits that they bias, respectively. Since the gate-source voltage of M_1 must be routed to M_2 and M_3 here, this case is referred to as an example of the *voltage routing* of bias signals. An advantage of this approach is that by routing only two nodes (the gate and the source of M_1) around the IC, any number of output currents can be produced. Furthermore the gains from the input to each output of the current mirror are not affected by the number of outputs in MOS technologies because $\beta_F \rightarrow \infty$. (In bipolar technologies, β_F is finite, and the gain error increases as the number of outputs increase, but a beta-helper configuration can be used to reduce such errors as described in Section 4.2.3.)

Unfortunately, voltage routing has two important disadvantages. First, the input and output transistors in the current mirror may be separated by distances that are large compared to the size of the IC, increasing the potential mismatches in (4.305). In particular, the threshold voltage typically displays considerable gradient with distance across a wafer. Therefore, when the devices are physically separated by large distances, large current mismatch can result from biasing current sources sharing the same gate-source bias, especially when the overdrive is small. The second disadvantage of voltage routing is that the output currents are sensitive to variations in the supply resistances R_{S1} and R_{S2} . Although these resistances were assumed to be zero above, they are nonzero in practice because of imperfect conduction in the interconnect layers and their contacts. Since I_{OUT2} flows in R_{S2} and $(I_{OUT1} + I_{OUT2})$ flows in R_{S1} , nonzero resistances cause $V_{GS2} < V_{GS1}$ and $V_{GS3} < V_{GS1}$ when $I_{OUT1} > 0$ and $I_{OUT2} > 0$. Therefore, with perfectly matched transistors, the output currents are less than the input current, and the errors in the output currents can be predicted by an analysis similar to that presented in Section 4.4.1 for Widlar current sources. The key point here is that R_{S1} and R_{S2} increase as the distances between the input and output transistors increase, increasing the errors in the output currents. As a result of both of these disadvantages, the output currents may have considerable variation from one IC to another with voltage routing, increasing the difficulty of designing the circuits biased by M_2 and M_3 to meet the required specifications even if I_{IN} is precisely controlled.

To overcome these problems, the circuit in Fig. 4.53 can be built so that M_1-M_3 are close together physically, and the current outputs I_{OUT1} and I_{OUT2} are routed as required on the IC. This case is referred to as an example of the *current routing* of bias signals. Current routing reduces the problems with mismatch and supply resistance by reducing the distances

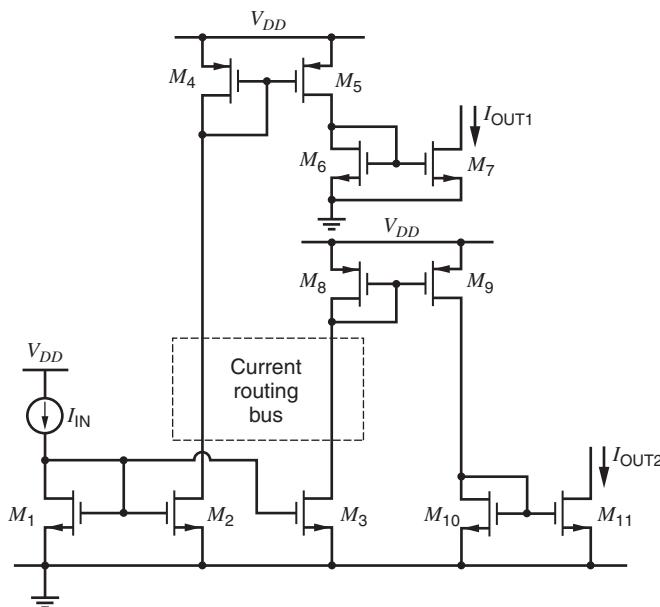


Figure 4.54 Bias-distribution circuit using both current routing and voltage routing.

between the input and output transistors in the current mirror in Fig. 4.53 compared to voltage routing. One disadvantage of current routing is that it requires one node to be routed for each bias signal. Therefore, when the number of bias outputs is large, the die area required for the interconnect to distribute the bias currents can be much larger than that required with voltage routing. Another disadvantage of current routing is that it can increase the parasitic capacitance on the drains of M_2 and M_3 . If these nodes are connected to circuits that process high-frequency signals, increased parasitic capacitance can reduce performance in some ways. For example, if M_2 and M_3 act as the tail current sources of differential pairs, increased parasitic capacitance will increase the common-mode gain and reduce the common-mode rejection ratio of each differential pair at high frequencies.

In practice, many ICs use a combination of current- and voltage-routing techniques. For example, Fig. 4.54 shows a circuit with five current mirrors, where the input and output currents are still referenced as in Fig. 4.53. If the current routing bus in Fig. 4.54 travels over a large distance, the parasitic capacitances on the drains of M_2 and M_3 may be large. However, the parasitic capacitances on the drains of M_7 and M_{11} are minimized by using voltage routing within each current mirror. Although simple current mirrors are shown in Fig. 4.54, cascoding is often used in practice to reduce gain errors stemming from a finite Early voltage. In ICs using both current and voltage routing, currents are routed globally and voltages locally, where the difference between global and local routing depends on distance. When the distance is large enough to significantly worsen mismatch or supply-resistance effects, the routing is *global*. Otherwise, it is *local*. An effective combination of these bias distribution techniques is to divide an IC into blocks, where bias currents are routed between blocks and bias voltages within the blocks.

A.4.2 INPUT OFFSET VOLTAGE OF DIFFERENTIAL PAIR WITH ACTIVE LOAD

A.4.2.1 BIPOLAR

For the resistively loaded emitter-coupled pair, we showed in Chapter 3 that the input offset voltage arises primarily from mismatches in I_S in the input transistors and from mismatches in the collector load resistors. In the active-load case, the input offset voltage results from nonzero

base current of the load devices and mismatches in the input transistors and load devices. Refer to Fig. 4.25a. Assume the inputs are grounded. If the matching is perfect and if $\beta_F \rightarrow \infty$ in T_3 and T_4 ,

$$V_{\text{OUT}} = V_{CC} - |V_{BE3}| \quad (4.306)$$

Equation 4.306 holds because only this output voltage forces $V_{CE3} = V_{CE4}$, where $I_{C1} = I_{C2}$ and $V_{BE1} = V_{BE2}$, which is required by KVL when $V_{I1} = V_{I2}$.

The differential input required to drive the output to the value given by (4.306) is the input-referred offset voltage. With finite β_F in the active-load transistors and/or device mismatch, the offset is usually nonzero. In the active-load, KVL shows that

$$V_{BE3} = V_{BE4} \quad (4.307)$$

Solving (1.58) for V_{BE3} and V_{BE4} and substituting in (4.307) gives

$$\frac{I_{C3}}{I_{S3}} \left(\frac{1}{1 + \frac{V_{CE3}}{V_{A3}}} \right) = \frac{I_{C4}}{I_{S4}} \left(\frac{1}{1 + \frac{V_{CE4}}{V_{A4}}} \right) \quad (4.308)$$

Assume that the Early voltages of T_3 and T_4 are identical. Since $V_{CE3} = V_{CE4}$ when (4.306) is satisfied, (4.308) can be simplified to

$$I_{C4} = I_{C3} \left(\frac{I_{S4}}{I_{S3}} \right) \quad (4.309)$$

Since $I_{C2} = -I_{C4}$, (4.309) can be written as

$$I_{C2} = -I_{C3} \left(\frac{I_{S4}}{I_{S3}} \right) \quad (4.310)$$

From KCL at the collector of T_3 ,

$$I_{C1} = -I_{C3} \left[1 + \left(\frac{2}{\beta_F} \right) \right] \quad (4.311)$$

where β_F is the ratio of the collector to base current in the active-load devices. From KVL in the input loop,

$$V_{ID} = V_{I1} - V_{I2} = V_{BE1} - V_{BE2} \quad (4.312)$$

Then the input offset voltage, V_{OS} , is the value of V_{ID} for which the output voltage is given by (4.306). If the Early voltages of T_1 and T_2 are identical, solving (1.58) for V_{BE1} and V_{BE2} and substituting into (4.312) gives

$$V_{OS} = V_{ID} = V_T \ln \left(\frac{I_{C1} I_{S2}}{I_{C2} I_{S1}} \right) \quad (4.313)$$

because $V_{CE1} = V_{CE2}$ when (4.306) is satisfied. Substituting (4.310) and (4.311) in (4.313) gives

$$V_{OS} = V_T \ln \left[\frac{I_{S3} I_{S2}}{I_{S4} I_{S1}} \left(1 + \frac{2}{\beta_F} \right) \right] \quad (4.314)$$

If the mismatches are small, this expression can be approximated as

$$V_{OS} \simeq V_T \left(\frac{\Delta I_{SP}}{I_{SP}} - \frac{\Delta I_{SN}}{I_{SN}} + \frac{2}{\beta_F} \right) \quad (4.315)$$

using the technique described in Section 3.5.6.3, where

$$\Delta I_{SP} = I_{S3} - I_{S4} \quad (4.316)$$

$$I_{SP} = \frac{I_{S3} + I_{S4}}{2} \quad (4.317)$$

$$\Delta I_{SN} = I_{S1} - I_{S2} \quad (4.318)$$

$$I_{SN} = \frac{I_{S1} + I_{S2}}{2} \quad (4.319)$$

In the derivation of (4.315), we assumed that the Early voltages of matched transistors are identical. In practice, mismatch in Early voltages also contributes to the offset, but the effect is usually negligible when the transistors are biased with collector-emitter voltages much less than their Early voltages.

Assuming a worst-case value for $\Delta I_S/I_S$ of ± 5 percent and a *pnp* beta of 20, the worst-case offset voltage is

$$V_{OS} \simeq V_T(0.05 + 0.05 + 0.1) = 0.2V_T \simeq 5 \text{ mV} \quad (4.320)$$

To find the worst-case offset, we have added the mismatch terms for the *pnp* and *npn* transistors in (4.320) instead of subtracting them as shown in (4.315) because the mismatch terms are random and independent of each other in practice. Therefore, the polarity of the mismatch terms is unknown in general. Comparing (4.320) to (3.219) shows that the actively loaded differential pair has significantly higher offset than the resistively loaded case under similar conditions. The offset arising here from mismatch in the load devices can be reduced by inserting resistors in series with the emitters of T_3 and T_4 as shown in Section A.4.1. To reduce the offset arising from finite β_F in the load devices, the current mirror in the load can use a beta helper transistor as described in Section 4.2.3.

A.4.2.2 MOS

The offset in the CMOS differential pair with active load shown in Fig. 4.25b is similar to the bipolar case. If the matching is perfect with the inputs grounded,

$$V_{OUT} = V_{DD} - |V_{GS3}| \quad (4.321)$$

Equation 4.321 holds because only this output voltage forces $V_{DS3} = V_{DS4}$, where $I_1 = I_2$ and $V_{GS1} = V_{GS2}$, which is required by KVL when $V_{I1} = V_{I2}$.

The differential input required to drive the output to the value given by (4.321) is the input-referred offset voltage. With device mismatch, the offset is usually nonzero.

$$V_{ID} = V_{GS1} - V_{GS2} = V_{I1} + V_{ov1} - V_{I2} - V_{ov2} \quad (4.322)$$

Assume that the Early voltages of T_1 and T_2 are identical. Since $V_{DS1} = V_{DS2} = V_{DSN}$ when $V_{ID} = V_{OS}$, applying (1.165) to V_{ov1} and V_{ov2} in (4.322) gives

$$V_{OS} = V_{I1} - V_{I2} + \sqrt{\frac{1}{1 + \lambda_N V_{DSN}}} \left(\sqrt{\frac{2I_1}{k'(W/L)_1}} - \sqrt{\frac{2I_2}{k'(W/L)_2}} \right) \quad (4.323)$$

If the mismatches are small, this expression can be approximated as

$$V_{OS} \simeq V_{I1} - V_{I2} + \frac{V_{ovN}}{2} \left(\frac{\Delta I_N}{I_N} - \frac{\Delta(W/L)_N}{(W/L)_N} \right) \quad (4.324)$$

using the technique described in Section 3.5.6.7, where

$$V_{ovN} = \sqrt{\frac{2I_N}{k'(W/L)_N(1 + \lambda_N V_{DSN})}} \quad (4.325)$$

$$\Delta I_N = I_1 - I_2 \quad (4.326)$$

$$I_N = \frac{I_1 + I_2}{2} \quad (4.327)$$

$$\Delta(W/L)_N = (W/L)_1 - (W/L)_2 \quad (4.328)$$

$$(W/L)_N = \frac{(W/L)_1 + (W/L)_2}{2} \quad (4.329)$$

Since $I_1 = -I_3$ and $I_2 = -I_4$

$$\frac{\Delta I_N}{I_N} = \frac{\Delta I_P}{I_P} \quad (4.330)$$

where

$$\Delta I_P = I_3 - I_4 \quad (4.331)$$

$$I_P = \frac{I_3 + I_4}{2} \quad (4.332)$$

To find $\Delta I_P/I_P$, we will use KVL in the gate-source loop in the load as follows

$$0 = V_{GS3} - V_{GS4} = V_{t3} + V_{ov3} - V_{t4} - V_{ov4} \quad (4.333)$$

Since T_3 and T_4 are p -channel transistors, their overdrives are negative. Assume that the Early voltages of T_3 and T_4 are identical. Since $V_{DS3} = V_{DS4} = V_{DSP}$ when $V_{ID} = V_{OS}$ (4.333) can be rewritten as

$$0 = V_{t3} - V_{t4} - \sqrt{\frac{1}{1 + |\lambda_P V_{DSP}|}} \left(\sqrt{\frac{2|I_3|}{k'(W/L)_3}} - \sqrt{\frac{2|I_4|}{k'(W/L)_4}} \right) \quad (4.334)$$

In (4.334), absolute value functions have been used so that the arguments of the square-root functions are positive. If the mismatches are small, this expression can be approximated as

$$\frac{\Delta I_P}{I_P} \simeq \frac{V_{t3} - V_{t4}}{|V_{ovP}|} + \frac{\Delta(W/L)_P}{(W/L)_P} \quad (4.335)$$

using the technique described in Section 3.5.6.7, where

$$|V_{ovP}| = \sqrt{\frac{2|I_P|}{k'(W/L)_P(1 + |\lambda_P V_{DSP}|)}} \quad (4.336)$$

$$\Delta(W/L)_P = (W/L)_3 - (W/L)_4 \quad (4.337)$$

$$(W/L)_P = \frac{(W/L)_3 + (W/L)_4}{2} \quad (4.338)$$

Substituting (4.335) and (4.330) into (4.324) gives

$$V_{OS} \simeq V_{t1} - V_{t2} + \frac{V_{ovN}}{2} \left(\frac{V_{t3} - V_{t4}}{|V_{ovP}|} + \frac{\Delta(W/L)_P}{(W/L)_P} - \frac{\Delta(W/L)_N}{(W/L)_N} \right) \quad (4.339)$$

Comparing (4.339) to (4.315) shows that the MOS differential pair with active load includes terms to account for threshold mismatch but excludes a term to account for finite beta in the active load because $\beta_F \rightarrow \infty$ in MOS transistors.

■ EXAMPLE

Find the input-referred offset voltage of the circuit in Fig. 4.25b using the transistor parameters in the table below.

Transistor	V_t (V)	W (μm)	L (μm)	k' ($\mu\text{A}/\text{V}^2$)
T_1	0.705	49	1	100
T_2	0.695	51	1	100
T_3	-0.698	103	1	50
T_4	-0.702	97	1	50

Assume that $I_{\text{TAIL}} = 200 \mu\text{A}$ and that $\lambda_N V_{DSN} \ll 1$ and $|\lambda_P V_{DSP}| \ll 1$. From (4.327) and KCL,

$$I_N = \frac{I_1 + I_2}{2} = \frac{I_{\text{TAIL}}}{2} = 100 \mu\text{A} \quad (4.340)$$

Substituting (4.340) and (4.329) into (4.325) gives

$$V_{ovN} \simeq \sqrt{\frac{200}{100(49 + 51)/2}} \text{ V} = 0.2 \text{ V} \quad (4.341)$$

Similarly, from (4.332) and KCL

$$I_P = \frac{I_3 + I_4}{2} = -\frac{I_{\text{TAIL}}}{2} = -100 \mu\text{A} \quad (4.342)$$

Substituting (4.342) and (4.338) into (4.336) gives

$$|V_{ovP}| \simeq \sqrt{\frac{200}{50(103 + 97)/2}} \text{ V} = 0.2 \text{ V} \quad (4.343)$$

Substituting (4.337) and (4.328) into (4.339) gives

$$\begin{aligned} V_{OS} &\simeq 0.705 \text{ V} - 0.695 \text{ V} \\ &+ 0.1 \left(\frac{-0.698 + 0.702}{0.1} + \frac{103 - 97}{(103 + 97)/2} - \frac{49 - 51}{(49 + 51)/2} \right) \text{ V} \\ &\simeq 0.01 \text{ V} + 0.1(0.04 + 0.06 + 0.04) \text{ V} = 0.024 \text{ V} \end{aligned} \quad (4.344)$$

In this example, the mismatches have been chosen so that the individual contributions to the offset add constructively to give the worst-case offset.

PROBLEMS

For the bipolar transistors in these problems, use the high-voltage device parameters given in Fig. 2.30 and Fig. 2.35, unless otherwise specified. Assume that $r_b = 0$ and $r_\mu \rightarrow \infty$ in all problems. Assume all bipolar transistors operate in the forward-active region, and neglect base currents in bias calculations unless otherwise specified.

4.1 Determine the output current and output resistance of the bipolar current mirror shown in Fig. 4.55. Find the output current if $V_{\text{OUT}} = 1 \text{ V}, 5 \text{ V}$, and 30 V . Ignore the effects of nonzero base currents. Compare your answer with a SPICE simulation.

4.2 Repeat Problem 4.1 including the effects of nonzero base currents.

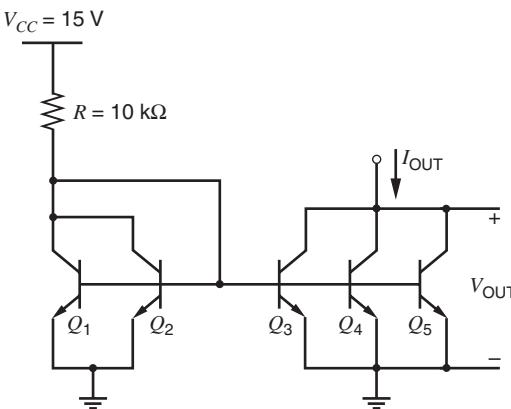


Figure 4.55 Circuit for Problem 4.1.

4.3 Design a simple MOS current mirror of the type shown in Fig. 4.4 to meet the following constraints:

- (a) Transistor M_2 must operate in the active region for values of V_{OUT} to within 0.2 V of ground.
- (b) The output current must be 50 μA .
- (c) The output current must change less than 1 percent for a change in output voltage of 1 V.

Make M_1 and M_2 identical. You are to minimize the total device area within the given constraints. Here the device area will be taken to be the total gate area ($W \times L$ product). Assume $X_d = 0$ and take other device data from Table 2.4.

4.4 Calculate an analytical expression for the small-signal output resistance R_o of the bipolar cascode current mirror of Fig. 4.8. Assume that the input current source is not ideal and that the nonideality is modeled by placing a resistor R_1 in parallel with I_{IN} . Show that for large R_1 , the output resistance approaches $\beta_0 r_o / 2$. Calculate the value of R_o if $V_{\text{CC}} = 5\text{ V}$, $I_{\text{IN}} = 0$, and $R_1 = 10\text{ k}\Omega$, and estimate the value of V_{OUT} below which R_o will begin to decrease substantially. Use SPICE to check your calculations and also to investigate the β_F sensitivity by varying β_F by -50 percent and examining I_{OUT} . Use SPICE to plot the large-signal $I_{\text{OUT}}-V_{\text{OUT}}$ characteristic.

4.5 Calculate the output resistance of the circuit of Fig. 4.9, assuming that $I_{\text{IN}} = 100\text{ }\mu\text{A}$ and the devices have drawn dimensions of $100\text{ }\mu\text{m}/1\text{ }\mu\text{m}$. Use the process parameters given in Table 2.4, and assume for all devices that $X_d = 0$. Also, ignore the body effect for simplicity. Compare your answer with a SPICE simulation and also use SPICE to plot the $I_{\text{OUT}}-V_{\text{OUT}}$ characteristic for V_{OUT} from 0 to 3 V.

4.6 Using the data given in the example of Section 1.9, include the effects of substrate leakage in the

calculation of the output resistance for the circuit of Problem 4.5. Let $V_{\text{OUT}} = 2\text{ V}$ and 3 V.

4.7 Design the circuit of Fig. 4.11b to satisfy the constraints in Problem 4.3 except the output resistance objective is that the output current change less than 0.02 percent for a 1 V change in the output voltage. Ignore the body effect for simplicity. Make all devices identical except for M_4 . Use SPICE to check your design and also to plot the $I_{\text{OUT}}-V_{\text{OUT}}$ characteristic for V_{OUT} from 0 to 3 V.

4.8 For the circuit of Fig. 4.56, assume that $(W/L)_8 = (W/L)$. Ignoring the body effect, find $(W/L)_6$ and $(W/L)_7$ so that $V_{DS6} = V_{DS7} = V_{ov8}$. Draw the schematic of a double-cascode current mirror that uses the circuit of Fig. 4.56 to bias both cascode devices in the output branch. For this current mirror, calculate the output resistance, the minimum output voltage for which all three transistors in the output branch operate in the active region, the total voltage across all the devices in the input branch, and the systematic gain error.

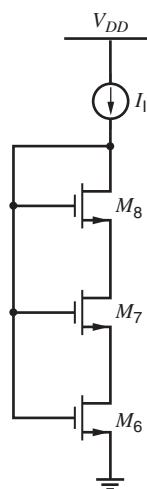


Figure 4.56 Circuit for Problem 4.8.

4.9 Calculate the output resistance of the Wilson current mirror shown in Fig. 4.57. What is the percentage change in I_{OUT} for a 5-V change in V_{OUT} ? Compare your answer with a SPICE simulation using a full device model. Use SPICE to check the β_F sensitivity by varying β_F by -50 percent and examining I_{OUT} . Also, use SPICE to plot the large-signal $I_{\text{OUT}}-V_{\text{OUT}}$ characteristic for V_{OUT} from 0 to 15 V.

4.10 Calculate the small-signal voltage gain of the common-source amplifier with active load in Fig. 4.16b. Assume that $V_{DD} = 3\text{ V}$ and that all the transistors operate in the active region. Do the calculations for values of I_{REF} of 1 mA, 100 μA , 10 μA , and 1 μA .

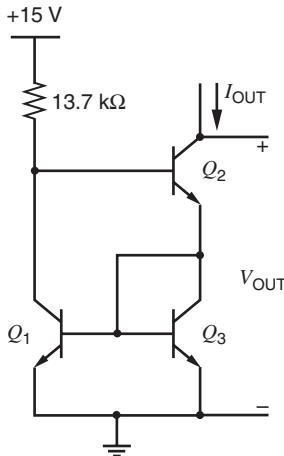


Figure 4.57
Circuit for
Problem 4.9.

Assume that the drawn dimensions of each transistor are $W = 100 \mu\text{m}$ and $L = 1 \mu\text{m}$. Assume $X_d = 0$ and use Table 2.4 for other parameters.

(a) At first, assume the transistors operate in strong inversion in all cases.

(b) Repeat part (a) including the effects of weak inversion by using (1.253) with $n = 1.5$ to calculate the transconductance of M_1 . Assume that a transistor operates in weak inversion when its overdrive is less than $2nV_T$, as given in (1.255).

(c) Use SPICE to check your calculations for both parts (a) and (b).

4.11 Calculate the small-signal voltage gain of a common-source amplifier with depletion load in Fig. 4.20, including both the body effect and channel-length modulation. Assume that $V_{DD} = 3 \text{ V}$ and that the dc input voltage is adjusted so that the dc output voltage is 1 V. Assume that M_1 has drawn dimensions of $W = 100 \mu\text{m}$ and $L = 1 \mu\text{m}$. Also, assume that M_2 has drawn dimensions of $W = 10 \mu\text{m}$ and $L = 1 \mu\text{m}$. For M_2 , assume $V_{t0} = -1 \text{ V}$. For both transistors, assume that $X_d = 0$. Use Table 2.4 for other parameters of both transistors.

4.12 Determine the unloaded voltage gain v_o/v_i and output resistance for the circuit of Fig. 4.58. Check with SPICE and also use SPICE to plot out the large-signal V_O-V_I transfer characteristic for $V_{SUP} = 2.5 \text{ V}$. Use SPICE to determine the CMRR if the current-source output resistance is $1 \text{ M}\Omega$.

4.13 Repeat Problem 4.12, but now assuming that 2-kΩ resistors are inserted in series with the emitters of Q_3 and Q_4 .

4.14 Repeat Problem 4.12 except replace Q_1 and Q_2 with *n*-channel MOS transistors M_1 and M_2 . Also, replace Q_3 and Q_4 with *p*-channel MOS transistors M_3 and M_4 . Assume $W_n = 50 \mu\text{m}$ and $W_p = 100 \mu\text{m}$.

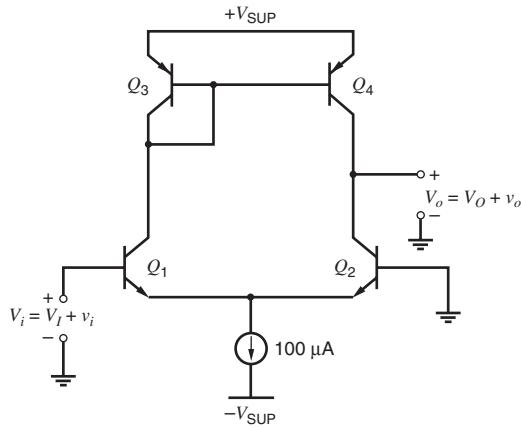


Figure 4.58 Circuit for Problem 4.12.

For all transistors, assume $L_{\text{drwn}} = 1 \mu\text{m}$ and $X_d = 0$. Use Table 2.3 for other parameters.

4.15 Repeat Problem 4.14, but now assuming that 2-kΩ resistors are inserted in series with the sources of M_3 and M_4 . Ignore the body effect.

4.16 Determine the unloaded voltage gain v_o/v_i and output resistance for the circuit of Fig. 4.59. Neglect r_μ . Verify with SPICE and also use SPICE to plot the large-signal V_O-V_I transfer characteristic for $V_{SUP} = 2.5 \text{ V}$.

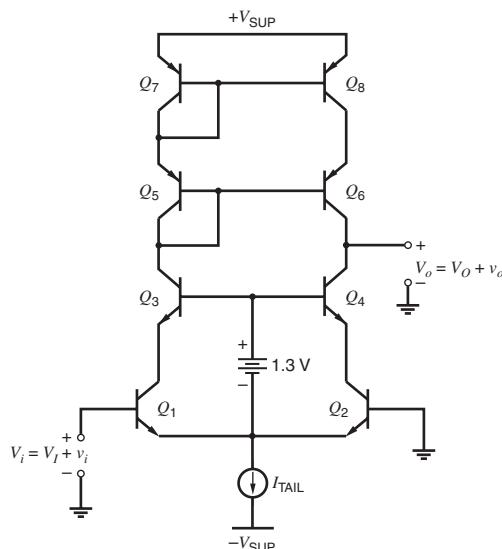


Figure 4.59 Cascode active-load circuit for Problem 4.16.

4.17 Repeat Problem 4.16 except replace the *npn* and *pnp* transistors with *n*-channel and *p*-channel MOS transistors, respectively. Assume $W_n = 50 \mu\text{m}$ and $W_p = 100 \mu\text{m}$. For all transistors, assume $L_{\text{drwn}} = 1 \mu\text{m}$ and $X_d = 0$. Let $I_{\text{TAIL}} = 100 \mu\text{A}$. Ignore

the body effect. Use Table 2.3 for other parameters.

4.18 Find $G_m[dm]$ of a source-coupled pair with a current-mirror load with nonzero mismatch (Fig. 4.29b) and show that it is approximately given by (4.184). Calculate the value of $G_m[dm]$ using the following data:

	T_1	T_2	T_3	T_4	T_5
g_m (mA/V)	1.05	0.95	1.1	0.9	2.0
r_o ($M\Omega$)	0.95	1.05	1.0	1.0	0.5

Compare your answer with a SPICE simulation. Also, compare your answer to the result that would apply without mismatch.

4.19 Although $G_m[cm]$ of a differential pair with a current-mirror load can be calculated exactly from a small-signal diagram where mismatch is allowed, the calculation is complicated because the mismatch terms interact, and the results are difficult to interpret. In practice, the mismatch terms are often a small fraction of the corresponding average values, and the interactions between mismatch terms are often negligible. Using the following steps as a guide, calculate an approximation to $G_m[cm]$ including the effects of mismatch.

(a) Derive the ratio i_2/v_{ic} included in (4.165) and show that this ratio is approximately $1/2r_{tail}$ as shown in (4.185) if $\epsilon_d \ll 2$, $g_{m2}r_{o2} \gg 1$, and $2g_{m2}r_{tail} \gg 1$.

(b) Use (4.173) to calculate ϵ_d with perfect matching, where ϵ_d represents the gain error of the differential pair with a pure common-mode input and is defined in (4.161).

(c) Calculate ϵ_d if $1/g_{m3} = 0$ and if the only mismatch is $g_{m1} \neq g_{m2}$.

(d) Calculate ϵ_d if $1/g_{m3} = 0$ and if the only mismatch is $r_{o1} \neq r_{o2}$.

(e) Now estimate the total ϵ_d including mismatch by adding the values calculated in parts (b), (c), and (d). Show that the result agrees with (4.186) if $g_{m3}r_{o(dp)} \gg 1$.

(f) Calculate ϵ_m , which represents the gain error of the current mirror and is defined in (4.133). Show that the result agrees with (4.187).

(g) Calculate the value of $G_m[cm]$ using (4.185) and the CMRR for the data given in Problem 4.18. Compare your answer with a SPICE simulation. Also, compare your answer to the result that would apply without mismatch.

4.20 Design a Widlar current source using *npn* transistors that produces a 5- μ A output current. Use

Fig. 4.31a with identical transistors, $V_{CC} = 30$ V, and $R_1 = 30$ k Ω . Find the output resistance.

4.21 In the design of a Widlar current source of Fig. 4.31a to produce a specified output current, two resistors must be selected. Resistor R_1 sets I_{IN} , and the emitter resistor R_2 sets I_{OUT} . Assuming a supply voltage of V_{CC} and a desired output current I_{OUT} , determine the values of the two resistors so that the total resistance in the circuit is minimized. Your answer should be given as expressions for R_1 and R_2 in terms of V_{CC} and I_{OUT} . What values would these expressions give for Problem 4.20? Are these values practical?

4.22 Determine the output current in the circuit of Fig. 4.40.

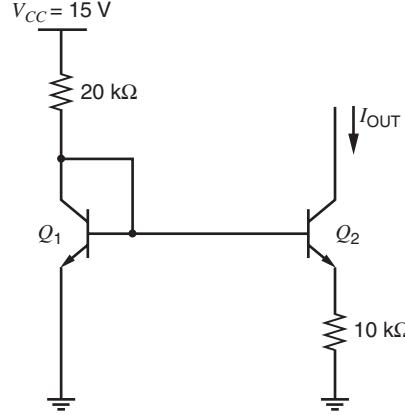


Figure 4.60 Circuit for Problem 4.22.

4.23 Design a MOS Widlar current source using the circuit shown in Fig. 4.31b to meet the following constraints with $V_{DD} = 3$ V:

(a) The input current should be 100 μ A, and the output current should be 10 μ A.

(b) $V_{ov1} = 0.2$ V.

(c) Transistor M_2 must operate in the active region if the voltage from the drain of M_2 to ground is at least 0.2 V.

(d) The output resistance should be 50 M Ω .

Ignore the body effect. Assume $L_{drwn} = 1$ μ m and $X_D = L_D = 0$. Use Table 2.4 for other parameters.

4.24 Design the MOS peaking current source in Fig. 4.34 so that $I_{OUT} = 0.1$ μ A.

(a) First, let $I_{IN} = 1$ μ A and find the required value of R .

(b) Second, let $R = 10$ k Ω and find the required I_{IN} .

In both cases, assume that both transistors are identical and operate in weak inversion with $I_t = 0.1$ μ A and $n = 1.5$. Also, find the minimum W/L

in both cases, assuming that $V_{GS} - V_t < 0$ is required to operate a transistor in weak inversion as shown in Fig. 1.45.

4.25 Determine the output current and output resistance of the circuit shown in Fig. 4.61.

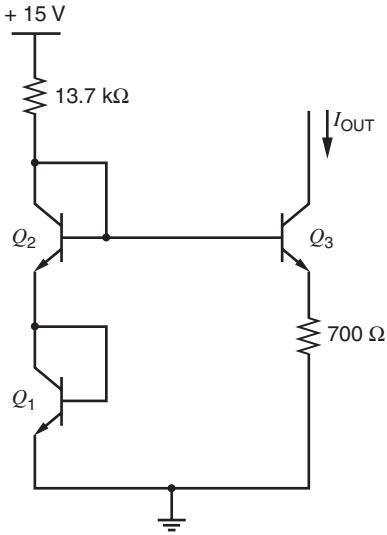


Figure 4.61 Circuit for Problem 4.25.

4.26 Determine the value of sensitivity S of output current to supply voltage for the circuit of Fig. 4.62, where $S = (V_{CC}/I_{OUT})(\partial I_{OUT}/\partial V_{CC})$.

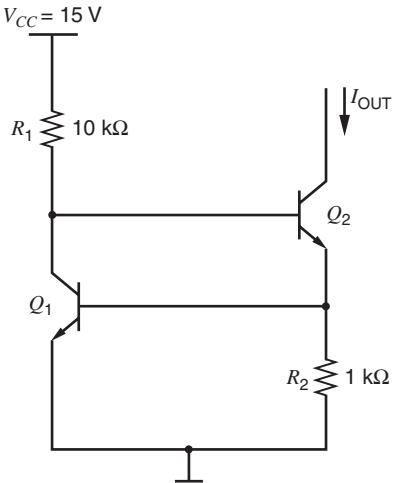


Figure 4.62 Circuit for Problem 4.26.

4.27 In the analysis of the hypothetical reference of Fig. 4.44, the current I_1 was assumed proportional to temperature. Assume instead that this current is derived from a diffused resistor, and thus has a TC_F of $-1500 \text{ ppm}/^\circ\text{C}$. Determine the new value of V_{OUT} required to achieve zero TC_F at 25°C . Neglect base current.

4.28 The circuit of Fig. 4.46c is to be used as a band-gap reference. If the op amp is ideal, its differential input voltage and current are both zero and

$$V_{OUT} = (V_{BE1} + I_1 R_1) = (V_{BE1} + I_2 R_2)$$

$$V_{OUT} = V_{BE1} + R_2 \left(\frac{V_{BE1} - V_{BE2}}{R_3} \right)$$

Assume that I_1 is to be made equal to $200 \mu\text{A}$, and that $(V_{BE1} - V_{BE2})$ is to be made equal to 100 mV . Determine R_1 , R_2 , and R_3 to realize zero TC_F of V_{OUT} at 25°C . Neglect base currents.

4.29 A band-gap reference like that of Fig. 4.47 is designed to have nominally zero TC_F at 25°C . Due to process variations, the saturation current I_S of the transistors is actually twice the nominal value. Assume $V_{OS} = 0$. What is dV_{OUT}/dT at 25°C ? Neglect base currents.

4.30 Simulate the band-gap reference from Problem 4.29 on SPICE. Assume that the amplifier is just a voltage-controlled voltage source with an open-loop gain of 10,000 and that the resistor values are independent of temperature. Also assume that $I_{S1} = 1.25 \times 10^{-17} \text{ A}$ and $I_{S2} = 1 \times 10^{-16} \text{ A}$. In SPICE, adjust the closed-loop gain of the amplifier (by choosing suitable resistor values) so that the output TC_F is zero at 25°C . What is the resulting target value of V_{OUT} ? Now double I_{S1} and I_{S2} . Use SPICE to adjust the gain so that V_{OUT} is equal to the target at 25°C . Find the new dV_{OUT}/dT at 25°C with SPICE. Compare this result with the calculations from Problem 4.29.

4.31 Repeat Problem 4.29 assuming that the values of I_S , R_2 , and R_1 are nominal but that R_3 is 1 percent low. Assume $V_{BE(on)} = 0.6 \text{ V}$.

4.32 A band-gap reference circuit is shown in Fig. 4.63. Assume that $\beta_F \rightarrow \infty$, $V_A \rightarrow \infty$, $I_{S1} = 1 \times 10^{-15} \text{ A}$, and $I_{S2} = 8 \times 10^{-15} \text{ A}$. Assume the op amp is ideal except for a possibly nonzero offset voltage V_{OS} , which is modeled by a voltage source in Fig. 4.63.

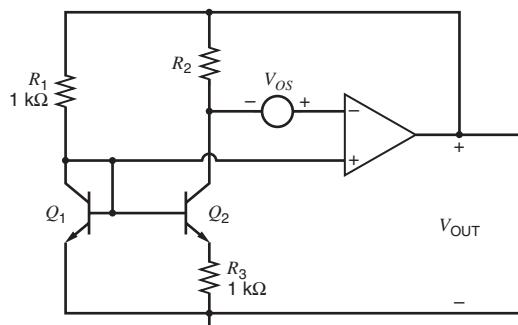


Figure 4.63 Band-gap reference circuit for Problem 4.32.

(a) Suppose that R_2 is trimmed to set V_{OUT} equal to the target voltage for which $dV_{\text{OUT}}/dT = 0$ at $T = 25^\circ\text{C}$ when $V_{\text{OS}} = 0$. Find dV_{OUT}/dT at $T = 25^\circ\text{C}$ when $V_{\text{OS}} = 30 \text{ mV}$.

(b) Under the conditions in part (a), is dV_{OUT}/dT positive or negative? Explain.

4.33 For the circuit of Fig. 4.64, find the value of W/L for which $dV_{GS}/dT = 0$ at 25°C . Assume that the threshold voltage falls 2 mV for each 1°C increase in temperature. Also, assume that the mobility temperature dependence is given by (4.243) with $n = 1.5$. Finally, use Table 2.4 for other parameters at 25°C , and let $I = 200 \mu\text{A}$.

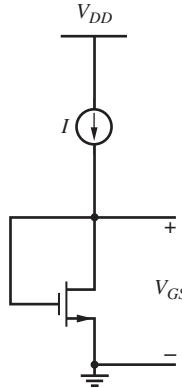


Figure 4.64 Circuit for Problem 4.33.

4.34 Calculate the bias current of the circuit shown in Fig. 4.65 as a function of R , $\mu_n C_{\text{ox}}$, $(W/L)_1$, and $(W/L)_2$. Comment on the temperature behavior of the bias current. For simplicity, assume that $X_d = L_d = 0$ and ignore the body effect. Assume M_4 is identical to M_3 .

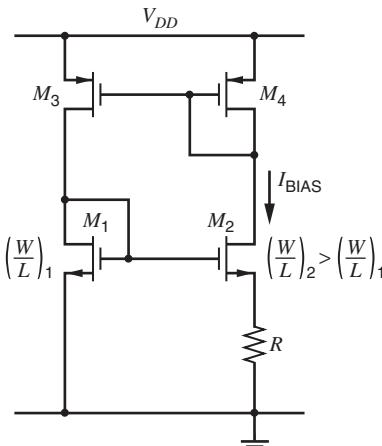


Figure 4.65 Circuit for Problem 4.34.

4.35 The circuit of Fig. 4.65 produces a supply-insensitive current. Calculate the ratio of small-signal

variations in I_{BIAS} to small-signal variations in V_{DD} at low frequencies. Ignore the body effect but include finite transistor r_o in this calculation.

4.36 For the bias circuit shown in Fig. 4.66, determine the bias current. Assume that $X_d = L_d = 0$. Neglect base currents and the body effect. Comment on the temperature dependence of the bias current. Assume a channel mobility and oxide thickness from Table 2.4. Compare your calculations to a SPICE simulation using a full circuit model from Table 2.4, and also use SPICE to determine the supply-voltage sensitivity of I_{BIAS} .

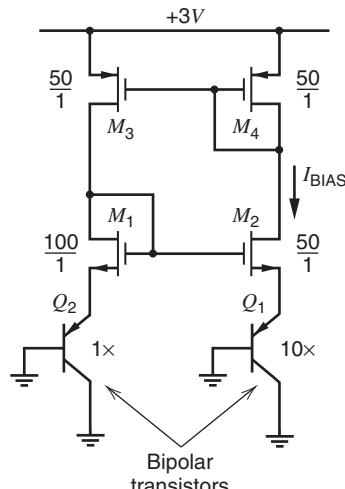


Figure 4.66 Circuit for Problem 4.36.

4.37 A pair of bipolar current sources is to be designed to produce output currents that match with ± 1 percent. If resistors display a worst-case mismatch of ± 0.5 percent, and transistors a worst-case V_{BE} mismatch of 2 mV, how much voltage must be dropped across the emitter resistors?

4.38 Determine the worst-case input offset voltage for the circuit of Fig. 4.58. Assume the worst-case I_S mismatches in the transistors are ± 5 percent and $\beta_F = 15$ for the pnp transistors. Assume the dc output voltage is $V_{\text{SUP}} - |V_{BE(\text{on})}|$.

4.39 Repeat Problem 4.38, but assume that $2-k\Omega$ resistors are placed in series with the emitters of Q_3 and Q_4 . Assume the worst-case resistor mismatch is ± 0.5 percent and the worst-case pnp β_F mismatch is ± 10 percent.

4.40 Repeat Problem 4.38 but replace the bipolar transistors with MOS transistors as in Problem 4.14. Assume the worst-case W/L mismatches in

the transistors are ± 5 percent and the worst-case V_t mismatches are ± 10 mV. Assume the dc output voltage to ground is $V_{\text{SUP}} - |V_{GS3}|$. Also, assume

that $(W/L)_1 + (W/L)_2 = 20$ and $(W/L)_3 + (W/L)_4 = 60$. Use Table 2.4 to calculate the transconductance parameters.

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