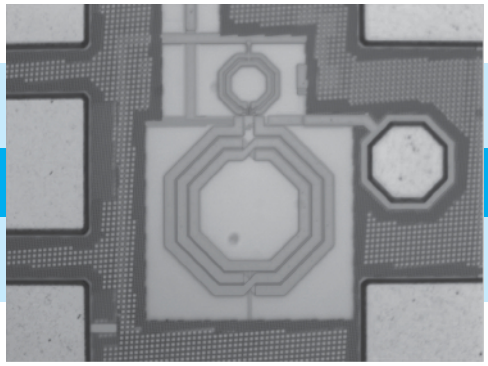


3

Diode Models and Circuits

Having studied the physics of diodes in Chapter 2, we now rise to the next level of abstraction and deal with diodes as circuit elements, ultimately arriving at interesting and real-life applications. This chapter also prepares us for understanding transistors as circuit elements in subsequent chapters. We proceed as follows:

Diodes as Circuit Elements
- Ideal Diode
- Circuit Characteristics
- Actual Diode

→

Applications
- Regulators
- Rectifiers
- Limiting and Clamping Circuits

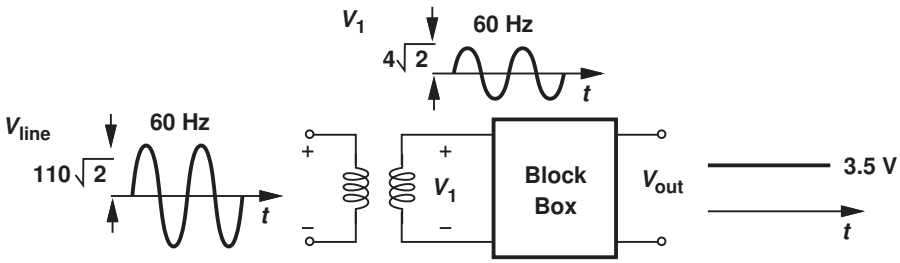
3.1 IDEAL DIODE

3.1.1 Initial Thoughts

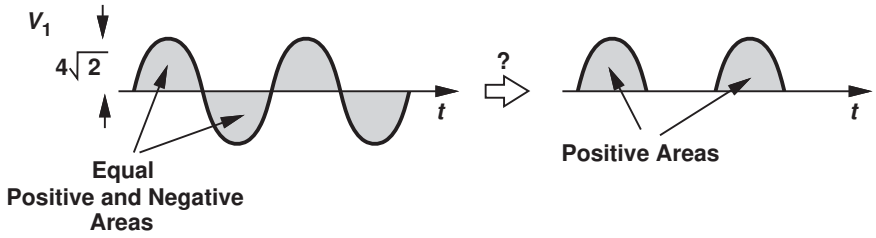
In order to appreciate the need for diodes, let us briefly study the design of a cellphone charger. The charger converts the line ac voltage at 110 V[1] and 60 Hz[2] to a dc voltage of 3.5 V. As shown in Fig. 3.1(a), this is accomplished by first stepping down the ac voltage by means of a transformer to about 4 V and subsequently converting the ac voltage to a dc quantity.[3] The same principle applies to adaptors that power other electronic devices.

How does the black box in Fig. 3.1(a) perform this conversion? As depicted in Fig. 3.1(b), the output of the transformer exhibits a zero dc content because the negative and positive half cycles enclose equal areas, leading to a zero average. Now suppose this waveform is applied to a mysterious device that passes the positive half cycles but blocks the negative ones. The result displays a positive average and some ac components, which can be removed by a low-pass filter (Section 3.5.1).

[1]This value refers to the root-mean-square (rms) voltage. The peak value is therefore equal to $110\sqrt{2}$.
[2]The line ac voltage in most countries is at 220 V and 50 Hz.
[3]The actual operation of adaptors is somewhat different.



(a)



(b)

Figure 3.1 (a) Charger circuit, (b) elimination of negative half cycles.

Did you know?

The rectification effect was discovered by Carl Braun around 1875. He observed that a metal wire pressed against a sulphide carried more current in one direction than the other. In subsequent decades, researchers tried other structures, arriving at "cat's whisker" rectifiers, which served as detectors for the reception of wireless signals in early radios and radars. These were eventually supplanted by *pn* junctions.

The waveform conversion in Fig. 3.1(b) points to the need for a device that *discriminates* between positive and negative voltages, passing only one and blocking the other. A simple resistor cannot serve in this role because it is *linear*. That is, Ohm's law, $V = IR$, implies that if the voltage across a resistor goes from positive to negative, so does the current through it. We must therefore seek a device that behaves as a short for positive voltages and as an open for negative voltages.

Figure 3.2 summarizes the result of our thought process thus far. The mysterious device generates an output equal to the input for positive half cycles and equal to zero for negative half cycles. Note that the device is nonlinear because it does not satisfy $y = \alpha x$; if $x \rightarrow -x$, $y \not\rightarrow -y$.

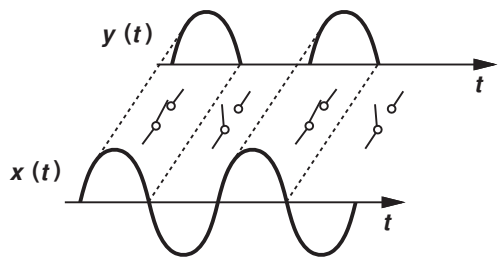


Figure 3.2 Conceptual operation of a diode.

3.1.2 Ideal Diode

The mysterious device mentioned above is called an "ideal diode." Shown in Fig. 3.3(a), the diode is a two-terminal device, with the triangular head denoting the allowable direction of current flow and the vertical bar representing the blocking behavior for currents in the opposite direction. The corresponding terminals are called the "anode" and the "cathode," respectively.

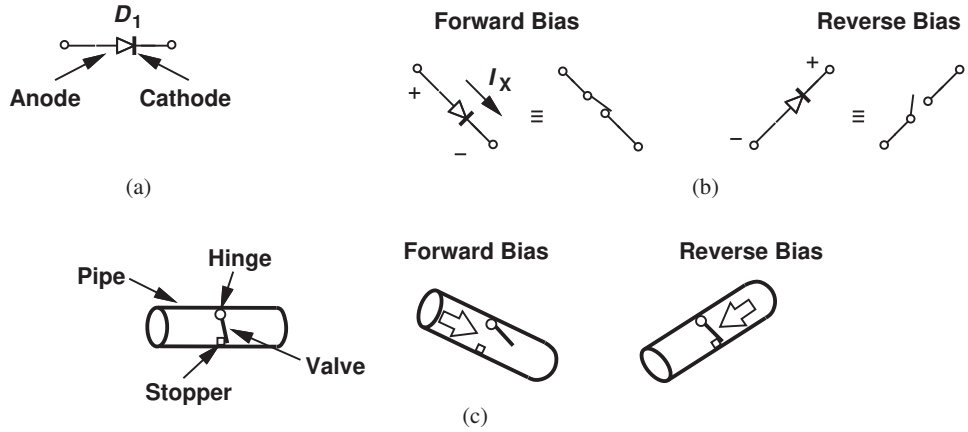


Figure 3.3 (a) Diode symbol, (b) equivalent circuit, (c) water pipe analogy.

Forward and Reverse Bias To serve as the mysterious device in the charger example of Fig. 3.3(a), the diode must turn "on" if $V_{\text{anode}} > V_{\text{cathode}}$ and "off" if $V_{\text{anode}} < V_{\text{cathode}}$ [Fig. 3.3(b)]. Defining $V_{\text{anode}} - V_{\text{cathode}} = V_D$, we say the diode is "forward-biased" if V_D tends to exceed zero and "reverse-biased" if $V_D < 0$.[4]

A water pipe analogy proves useful here. Consider the pipe shown in Fig. 3.3(c), where a valve (a plate) is hinged on the top and faces a stopper on the bottom. If water pressure is applied from the left, the valve rises, allowing a current. On the other hand, if water pressure is applied from the right, the stopper keeps the valve shut.

Example 3.1

As with other two-terminal devices, diodes can be placed in series (or in parallel). Determine which one of the configurations in Fig. 3.4 can conduct current.

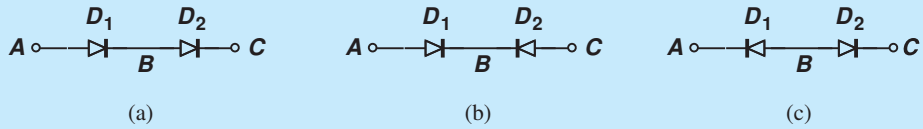


Figure 3.4 Series combinations of diodes.

[4]In our drawings, we sometimes place more positive nodes higher to provide a visual picture of the circuit's operation. The diodes in Fig. 3.3(b) are drawn according to this convention.

Solution In Fig. 3.4(a), the anodes of D_1 and D_2 point to the same direction, allowing the flow of current from A to B to C but not in the reverse direction. In Fig. 3.4(b), D_1 stops current flow from B to A, and D_2, from B to C. Thus, no current can flow in either direction. By the same token, the topology of Fig. 3.4(c) behaves as an open for any voltage. Of course, none of these circuits appears particularly useful at this point, but they help us become comfortable with diodes.

Exercise Determine all possible series combinations of three diodes and study their conduction properties.

I/V Characteristics In studying electronic devices, it is often helpful to accompany equations with graphical visualizations. A common type of plot is that of the current/voltage (I/V) characteristic, i.e., the current that flows through the device as a function of the voltage across it.

Since an ideal diode behaves as a short or an open, we first construct the I/V characteristics for two special cases of Ohm's law:

$$R = 0 \Rightarrow I = \frac{V}{R} = \infty \tag{3.1}$$

$$R = \infty \Rightarrow I = \frac{V}{R} = 0. \tag{3.2}$$

The results are illustrated in Fig. 3.5(a). For an ideal diode, we combine the positive-voltage region of the first with the negative-voltage region of the second, arriving at the I_D/V_D characteristic in Fig. 3.5(b). Here, $V_D = V_{\text{anode}} - V_{\text{cathode}}$, and I_D is defined as the current flowing into the anode and out of the cathode.

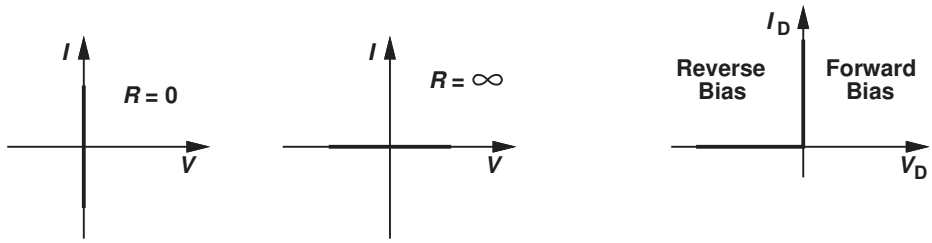


Figure 3.5 I/V characteristics of (a) zero and infinite resistors, (b) ideal diode.

Example 3.2 We said that an ideal diode turns on for positive anode-cathode voltages. But the characteristic in Fig. 3.5(b) does not appear to show any I_D values for $V_D > 0$. How do we interpret this plot?

Solution This characteristic indicates that as V_D exceeds zero by a very small amount, then the diode turns on and conducts infinite current *if* the circuit surrounding the diode can provide such a current. Thus, in circuits containing only finite currents, a forward-biased ideal diode sustains a zero voltage—similar to a short circuit.

Exercise How is the characteristic modified if we place a 1-Ω resistor in series with the diode?

Example 3.3

Plot the I/V characteristic for the "antiparallel" diodes shown in Fig. 3.6(a).

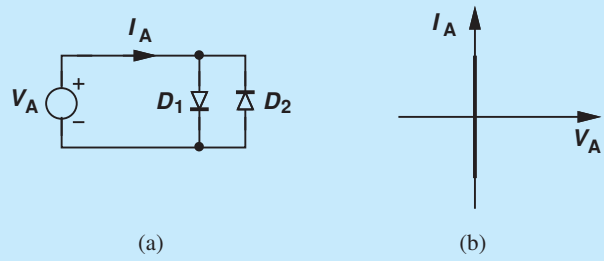


Figure 3.6 (a) Antiparallel diodes, (b) resulting I/V characteristic.

Solution

If $V_A > 0$, D_1 is on and D_2 is off, yielding $I_A = \infty$. If $V_A < 0$, D_1 is off, but D_2 is on, again leading to $I_A = \infty$. The result is illustrated in Fig. 3.6(b). The antiparallel combination therefore acts as a short for all voltages. Seemingly a useless circuit, this topology becomes much more interesting with actual diodes (Section 3.5.3).

Exercise

Repeat the above example if a 1-V battery is placed in series with the parallel combination of the diodes.

Example 3.4

Plot the I/V characteristic for the diode-resistor combination of Fig. 3.7(a).

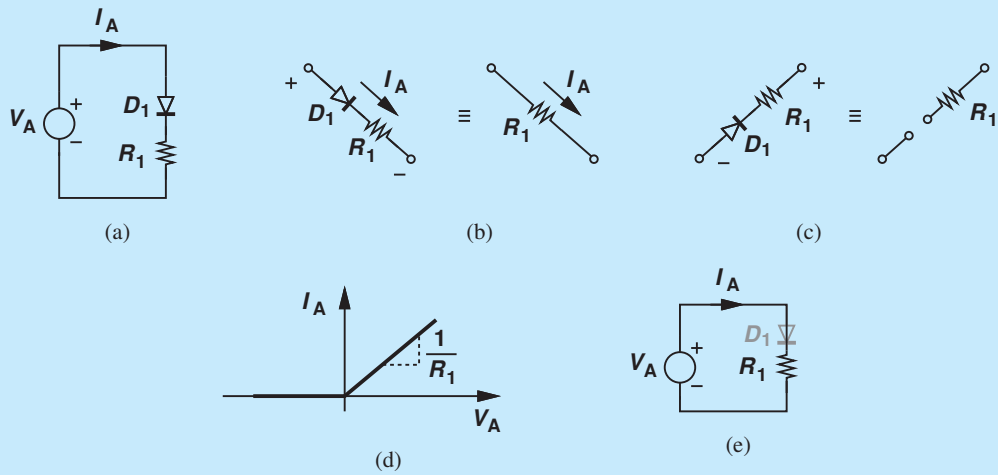


Figure 3.7 (a) Diode-resistor series combination, (b) equivalent circuit under forward bias, (c) equivalent circuit under reverse bias, (d) I/V characteristic, (e) equivalent circuit if D_1 is on.

Solution We surmise that, if $V_A > 0$, the diode is on [Fig. 3.7(b)] and $I_A = V_A/R_1$ because $V_{D1} = 0$ for an ideal diode. On the other hand, if $V_A < 0$, D_1 is probably off [Fig. 3.7(c)] and $I_D = 0$. Figure 3.7(d) plots the resulting I/V characteristic.

The above observations are based on guesswork. Let us study the circuit more rigorously. We begin with $V_A < 0$, postulating that the diode is off. To confirm the validity of this guess, let us assume D_1 is on and see if we reach a conflicting result. If D_1 is on, the circuit is reduced to that in Fig. 3.7(e), and if V_A is negative, so is I_A; i.e., the actual current flows from right to left. But this implies that D_1 carries a current from its cathode to its anode, violating the definition of the diode. Thus, for $V_A < 0$, D_1 remains off and $I_A = 0$.

As V_A rises above zero, it tends to forward bias the diode. Does D_1 turn on for any $V_A > 0$ or does R_1 shift the turn-on point? We again invoke proof by contradiction. Suppose for some $V_A > 0$, D_1 is still off, behaving as an open circuit and yielding $I_A = 0$. The voltage drop across R_1 is therefore equal to zero, suggesting that $V_{D1} = V_A$ and hence $I_{D1} = \infty$ and contradicting the original assumption. In other words, D_1 turns on for any $V_A > 0$.

Exercise Repeat the above analysis if the terminals of the diode are swapped.

The above example leads to two important points. First, the series combination of D_1 and R_1 acts as an open for negative voltages and as a resistor of value R_1 for positive voltages. Second, in the analysis of circuits, we can assume an arbitrary state (on or off) for each diode and proceed with the computation of voltages and currents; if the assumptions are incorrect, the final result contradicts the original assumptions. Of course, it is helpful to first examine the circuit carefully and make an intuitive guess.

Example 3.5 Why are we interested in I/V characteristics rather than V/I characteristics?

Solution In the analysis of circuits, we often prefer to consider the voltage to be the "cause" and the current, the "effect." This is because in typical circuits, voltage polarities can be predicted more readily and intuitively than current polarities. Also, devices such as transistors fundamentally produce current in response to voltage.

Exercise Plot the V/I characteristic of an ideal diode.

Example 3.6 In the circuit of Fig. 3.8, each input can assume a value of either zero or +3 V. Determine the response observed at the output.

Solution If $V_A = +3$ V, and $V_B = 0$, then we surmise that D_1 is forward-biased and D_2, reverse-biased. Thus, $V_{out} = V_A = +3$ V. If uncertain, we can assume both D_1 and D_2 are

forward-biased, immediately facing a conflict: D_1 enforces a voltage of +3 V at the output whereas D_2 shorts V_{out} to $V_B = 0$. This assumption is therefore incorrect.

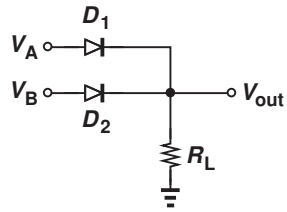


Figure 3.8 OR gate realized by diodes.

The symmetry of the circuit with respect to V_A and V_B suggests that $V_{out} = V_B = +3$ V if $V_A = 0$ and $V_B = +3$ V. The circuit operates as a logical OR gate and was in fact used in early digital computers.

Exercise Construct a three-input OR gate.

Example 3.7 Is an ideal diode on or off if $V_D = 0$?

Solution An ideal diode experiencing a zero voltage must carry a zero current (why?). However, this does not mean it acts as an open circuit. After all, a piece of wire experiencing a zero voltage behaves similarly. Thus, the state of an ideal diode with $V_D = 0$ is somewhat arbitrary and ambiguous. In practice, we consider slightly positive or negative voltages to determine the response of a diode circuit.

Exercise Repeat the above example if a 1-Ω resistor is placed in series with the diode.

Input/Output Characteristics Electronic circuits process an input and generate a corresponding output. It is therefore instructive to construct the input/output characteristics of a circuit by varying the input across an allowable range and plotting the resulting output.

As an example, consider the circuit depicted in Fig. 3.9(a), where the output is defined as the voltage across D_1. If $V_{in} < 0$, D_1 is reverse biased, reducing the circuit to that in Fig. 3.9(b). Since no current flows through R_1, we have $V_{out} = V_{in}$. If $V_{in} > 0$, then D_1 is forward biased, shorting the output and forcing $V_{out} = 0$ [Fig. 3.9(c)]. Figure 3.9(d) illustrates the overall input/output characteristic.

3.1.3 Application Examples

Recall from Fig. 3.2 that we arrived at the concept of the ideal diode as a means of converting $x(t)$ to $y(t)$. Let us now design a circuit that performs this function. We may naturally construct the circuit as shown in Fig. 3.10(a). Unfortunately, however, the cathode of the diode is "floating," the output current is always equal to zero, and the state of the diode is ambiguous. We therefore modify the circuit as depicted in Fig. 3.10(b) and analyze

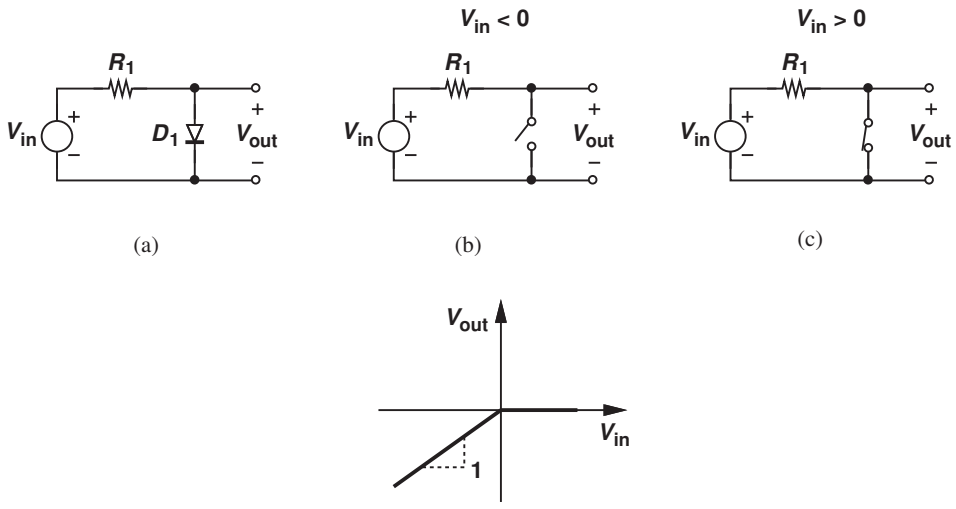


Figure 3.9 (a) Resistor-diode circuit, (b) equivalent circuit for negative input, (c) equivalent circuit for positive input, (d) input/output characteristic.

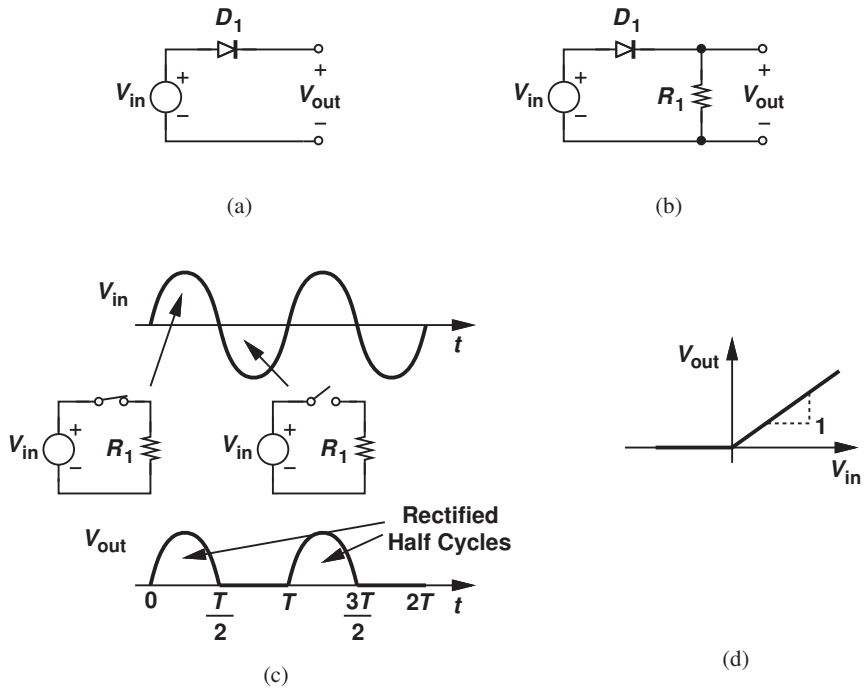


Figure 3.10 (a) A diode operating as a rectifier, (b) complete rectifier, (c) input and output waveforms, (d) input/output characteristic.

its response to a sinusoidal input [Fig. 3.10(c)]. Since R_1 has a tendency to maintain the cathode of D_1 near zero, as V_{in} rises, D_1 is forward biased, shorting the output to the input. This state holds for the positive half cycle. When V_{in} falls below zero, D_1 turns off and R_1 ensures that $V_{out} = 0$ because $I_D R_1 = 0$.[5] The circuit of Fig. 3.10(b) is called a "rectifier."

It is instructive to plot the input/output characteristic of the circuit as well. Noting that if $V_{in} < 0$, D_1 is off and $V_{out} = 0$, and if $V_{in} > 0$, D_1 is on and $V_{out} = V_{in}$, we obtain the behavior shown in Fig. 3.10(d). The rectifier is a nonlinear circuit because if $V_{in} \rightarrow -V_{in}$ then $V_{out} \not\rightarrow -V_{out}$.

Example 3.8 Is it a coincidence that the characteristics in Figs. 3.7(d) and 3.10(d) look similar?

Solution No, we recognize that the output voltage in Fig. 3.10(b) is simply equal to $I_A R_1$ in Fig. 3.7(a). Thus, the two plots differ by only a scaling factor equal to R_1.

Exercise Construct the characteristic if the terminals of D_1 are swapped.

We now determine the time average (dc value) of the output waveform in Fig. 3.10(c) to arrive at another interesting application. Suppose $V_{in} = V_p \sin \omega t$, where $\omega = 2\pi/T$ denotes the frequency in radians per second and T the period. Then, in the first cycle after $t = 0$, we have

$$V_{out} = V_p \sin \omega t \quad \text{for } 0 \le t \le \frac{T}{2} \tag{3.3}$$

$$= 0 \quad \text{for } \frac{T}{2} \le t \le T. \tag{3.4}$$

To compute the average, we obtain the area under V_{out} and normalize the result to the period:

$$V_{out,avg} = \frac{1}{T} \int_0^T V_{out}(t)\, dt \tag{3.5}$$

$$= \frac{1}{T} \int_0^{T/2} V_p \sin \omega t\, dt \tag{3.6}$$

$$= \frac{1}{T} \cdot \frac{V_p}{\omega} [-\cos \omega t]_0^{T/2} \tag{3.7}$$

$$= \frac{V_p}{\pi}. \tag{3.8}$$

Thus, the average is proportional to V_p, an expected result because a larger input amplitude yields a greater area under the rectified half cycles.

The above observation reveals that the average value of a rectified output can serve as a measure of the "strength" (amplitude) of the input. That is, a rectifier can operate as a "signal strength indicator." For example, since cellphones receive varying levels of signal depending on the user's location and environment, they require an indicator to determine how much the signal must be amplified.

[5] Note that without R_1, the output voltage is not defined because a floating node can assume any potential.

Example 3.9 A cellphone receives a 1.8-GHz signal with a peak amplitude ranging from 2 μV to 10 mV. If the signal is applied to a rectifier, what is the corresponding range of the output average?

Solution The rectified output exhibits an average value ranging from $2\ \mu\text{V}/(\pi) = 0.637\ \mu\text{V}$ to $10\ \text{mV}/(\pi) = 3.18\ \text{mV}$.

Exercise Do the above results change if a 1-Ω resistor is placed in series with the diode?

In our effort toward understanding the role of diodes, we examine another circuit that will eventually (in Section 3.5.3) lead to some important applications. First, consider the topology in Fig. 3.11(a), where a 1-V battery is placed in series with an ideal diode. How does this circuit behave? If $V_1 < 0$, the cathode voltage is higher than the anode voltage, placing D_1 in reverse bias. Even if V_1 is slightly greater than zero, e.g., equal to 0.9 V, the anode is not positive enough to forward bias D_1. Thus, V_1 must approach +1 V for D_1

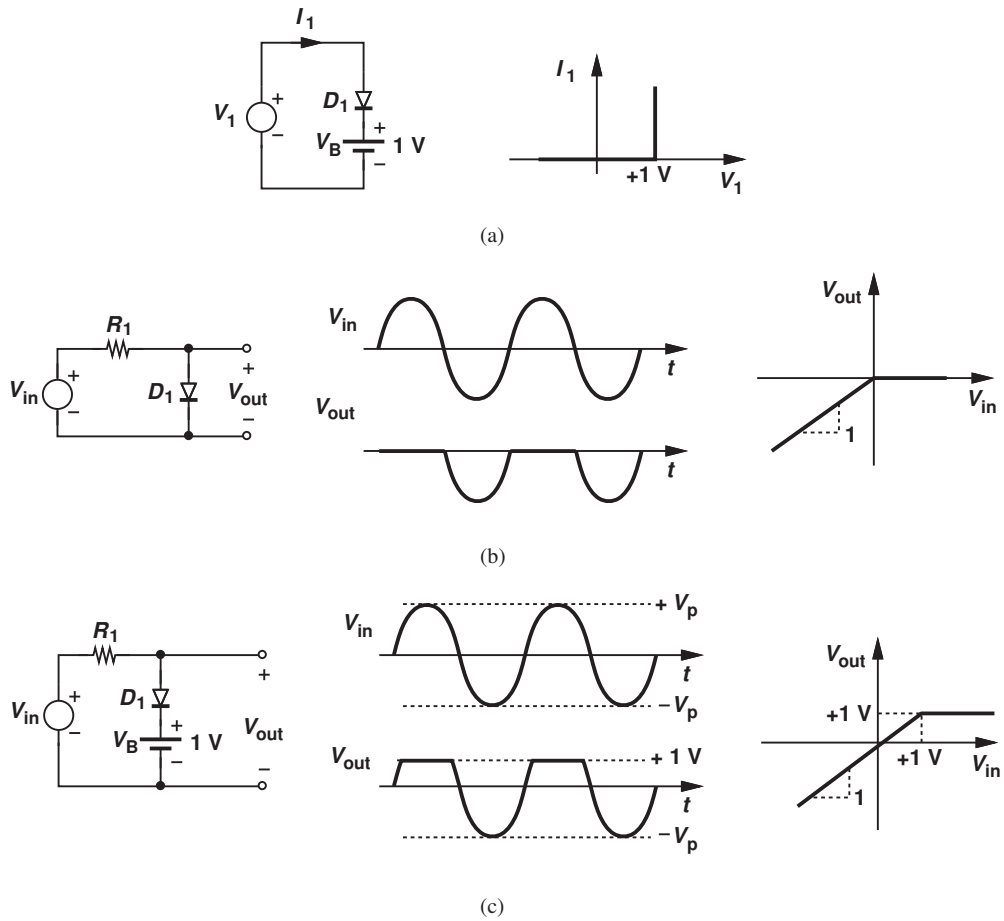


Figure 3.11 (a) Diode-battery circuit, (b) resistor-diode circuit, (c) addition of series battery to (b).

to turn on. Shown in Fig. 3.11(a), the I/V characteristic of the diode-battery combination resembles that of a diode, but shifted to the right by 1 V.

Now, let us examine the circuit in Fig. 3.11(b). Here, for $V_{in} < 0$, D_1 remains off, yielding $V_{out} = V_{in}$. For $V_{in} > 0$, D_1 acts a short, and $V_{out} = 0$. The circuit therefore does not allow the output to exceed zero, as illustrated in the output waveform and the input/output characteristic. But suppose we seek a circuit that must not allow the output to exceed +1 V (rather than zero). How should the circuit of Fig. 3.11(b) be modified? In this case, D_1 must turn on only when V_{out} approaches +1 V, implying that a 1-V battery must be inserted in series with the diode. Depicted in Fig. 3.11(c), the modification indeed guarantees $V_{out} \leq +1$ V for any input level. We say the circuit "clips" or "limits" at +1 V. "Limiters" prove useful in many applications and are described in Section 3.5.3.

Example 3.10

Sketch the time average of V_{out} in Fig. 3.11(c) for a sinusoidal input as the battery voltage, V_B, varies from $-\infty$ to $+\infty$.

Solution

If V_B is very negative, D_1 is always on because $V_{in} \geq -V_p$. In this case, the output average is equal to V_B [Fig. 3.12(a)]. For $-V_p < V_B < 0$, D_1 turns off at some point in the negative half cycle and remains off in the positive half cycle, yielding an average greater than $-V_p$ but less than V_B. For $V_B = 0$, the average reaches $-V_p/(\pi)$. Finally, for $V_B \geq V_p$, no limiting occurs and the average is equal to zero. Figure 3.12(b) sketches this behavior.

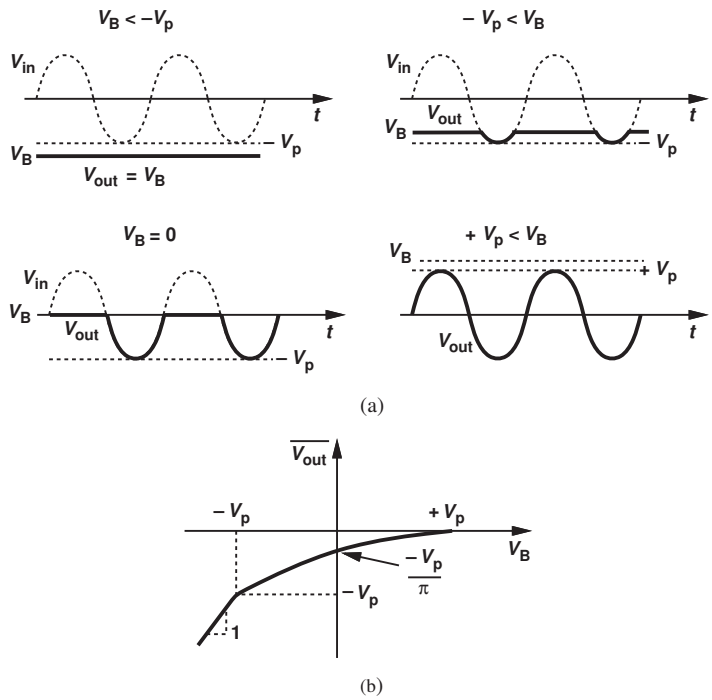


Figure 3.12

Exercise

Repeat the above example if the terminals of the diode are swapped.

Example 3.11 Is the circuit of Fig. 3.11(b) a rectifier?

Solution Yes, indeed. The circuit passes only negative cycles to the output, producing a negative average.

Exercise How should the circuit of Fig. 3.11(b) be modified to pass only positive cycles to the output?

3.2 *pn* JUNCTION AS A DIODE

The operation of the ideal diode is somewhat reminiscent of the current conduction in *pn* junctions. In fact, the forward and reverse bias conditions depicted in Fig. 3.3(b) are quite similar to those studied for *pn* junctions in Chapter 2. Figures 3.13(a) and (b) plot the I/V characteristics of the ideal diode and the *pn* junction, respectively. The latter can serve as an approximation of the former by providing "unilateral" current conduction. Shown in Fig. 3.13 is the constant-voltage model developed in Chapter 2, providing a simple approximation of the exponential function and also resembling the characteristic plotted in Fig. 3.11(a).

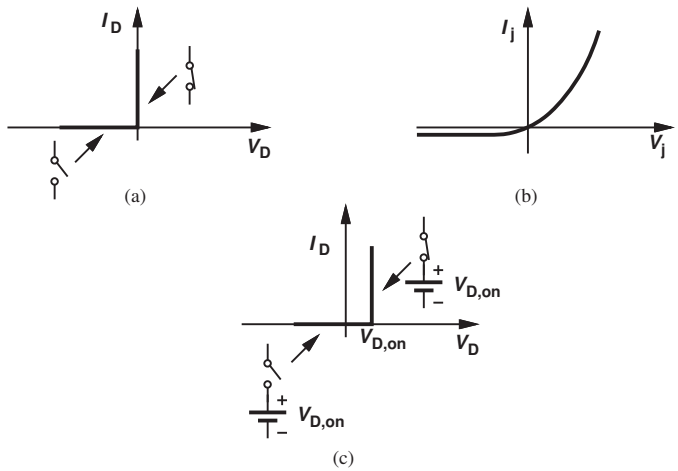


Figure 3.13 Diode characteristics: (a) ideal model, (b) exponential model, (c) constant-voltage model.

Did you know?

Diodes are among few human-made devices that have a very wide range of sizes. The diodes in integrated circuits may have a cross-section area of 0.5 μm × 0.5 μm and carry a current of a few hundred microamperes. On the other hand, diodes used in industrial applications such as electroplating have a cross section of 10 cm × 10 cm and carry a current of several thousand amperes! Can you think of any other device that comes in such a wide range of sizes?

Given a circuit topology, how do we choose one of the above models for the diodes? We may utilize the ideal model so as to develop a quick, rough understanding of the circuit's operation. Upon performing this exercise, we may discover that this idealization is inadequate and hence employ the constant-voltage model. This model suffices in most cases, but we may need to resort to the exponential model for some circuits. The following examples illustrate these points.

It is important to bear in mind two peinciples: (1) if a diode is at the edge of turning on or off, then $I_D \approx 0$ and $V_D \approx V_{D,on}$; (2) if a diode is on I_D *must* flow from anode to cathode.

Example 3.12

Plot the input/output characteristic of the circuit shown in Fig. 3.14(a) using (a) the ideal model and (b) the constant-voltage model.

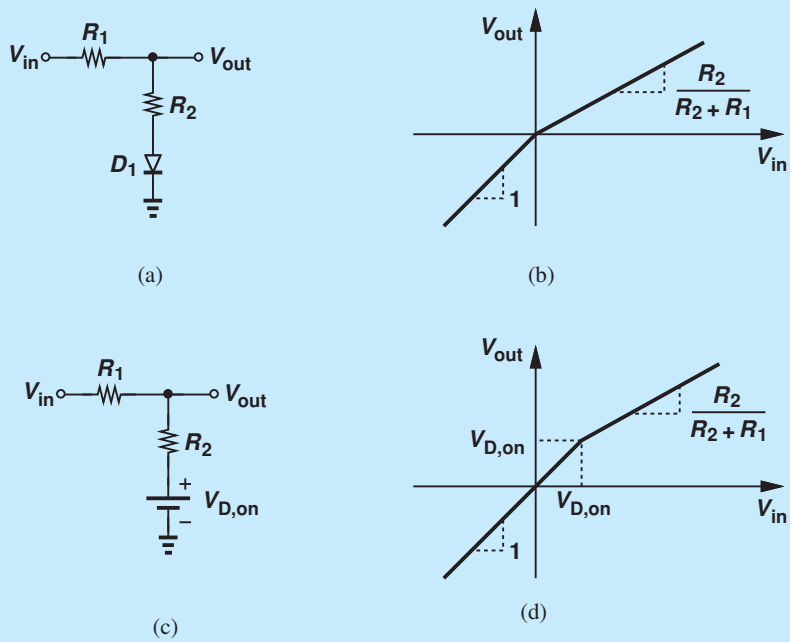


Figure 3.14 (a) Diode circuit, (b) input/output characteristic with ideal diode model, (c) input/output characteristic with constant-voltage diode model.

Solution

(a) We begin with $V_{in} = -\infty$, recognizing that D_1 is reverse biased. In fact, for $V_{in} < 0$, the diode remains off and no current flows through the circuit. Thus, the voltage drop across R_1 is zero and $V_{out} = V_{in}$.

As V_{in} exceeds zero, D_1 turns on, operating as a short and reducing the circuit to a voltage divider. That is,

$$V_{out} = \frac{R_2}{R_1 + R_2} V_{in} \text{ for } V_{in} > 0. \tag{3.9}$$

Figure 3.14(b) plots the overall characteristic, revealing a slope equal to unity for $V_{in} < 0$ and $R_2/(R_2 + R_1)$ for $V_{in} > 0$. In other words, the circuit operates as a voltage divider once the diode turns on and loads the output node with R_2.

(b) In this case, D_1 is reverse biased for $V_{in} < V_{D,on}$, yielding $V_{out} = V_{in}$. As V_{in} exceeds $V_{D,on}$, D_1 turns on, operating as a constant voltage source with a value $V_{D,on}$ [as illustrated in Fig. 3.13(c)]. Reducing the circuit to that in Fig. 3.14(c), we apply Kirchoff's current law to the output node:

$$\frac{V_{in} - V_{out}}{R_1} = \frac{V_{out} - V_{D,on}}{R_2}. \tag{3.10}$$

It follows that

$$V_{out} = \frac{\frac{R_2}{R_1}V_{in} + V_{D,on}}{1 + \frac{R_2}{R_1}}. \tag{3.11}$$

As expected, $V_{out} = V_{D,on}$ if $V_{in} = V_{D,on}$. Figure 3.14(d) plots the resulting characteristic, displaying the same shape as that in Fig. 3.14(b) but with a shift in the break point.

Exercise In the above example, plot the current through R_1 as a function of V_{in}.

It is important to remember that a diode about to turn on or off carries no current but sustains a voltage equal to $V_{D,on}$.

3.3 ADDITIONAL EXAMPLES*

Example 3.13 In the circuit of Fig. 3.15, D_1 and D_2 have different cross section areas but are otherwise identical. Determine the current flowing through each diode.

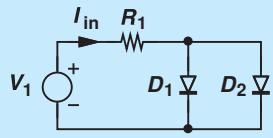


Figure 3.15 Diode circuit.

Solution In this case, we must resort to the exponential equation because the ideal and constant-voltage models do not include the device area. We have

$$I_{in} = I_{D1} + I_{D2}. \tag{3.12}$$

We also equate the voltages across D_1 and D_2:

$$V_T \ln \frac{I_{D1}}{I_{S1}} = V_T \ln \frac{I_{D2}}{I_{S2}}; \tag{3.13}$$

that is,

$$\frac{I_{D1}}{I_{S1}} = \frac{I_{D2}}{I_{S2}}. \tag{3.14}$$

Solving (3.13) and (3.15) together yields

$$I_{D1} = \frac{I_{in}}{1 + \frac{I_{S2}}{I_{S1}}} \tag{3.15}$$

$$I_{D2} = \frac{I_{in}}{1 + \frac{I_{S1}}{I_{S2}}}. \tag{3.16}$$

As expected, $I_{D1} = I_{D2} = I_{in}/2$ if $I_{S1} = I_{S2}$.

Exercise For the circuit of Fig. 3.15, calculate V_D is terms of I_{in}, I_{S1}, and I_{S2}.

*This section can be skipped in a first reading.

Example 3.14

Using the constant-voltage model, plot the input/output characteristics of the circuit depicted in Fig. 3.16(a). Note that a diode about to turn on carries *zero* current but sustains $V_{D,on}$.

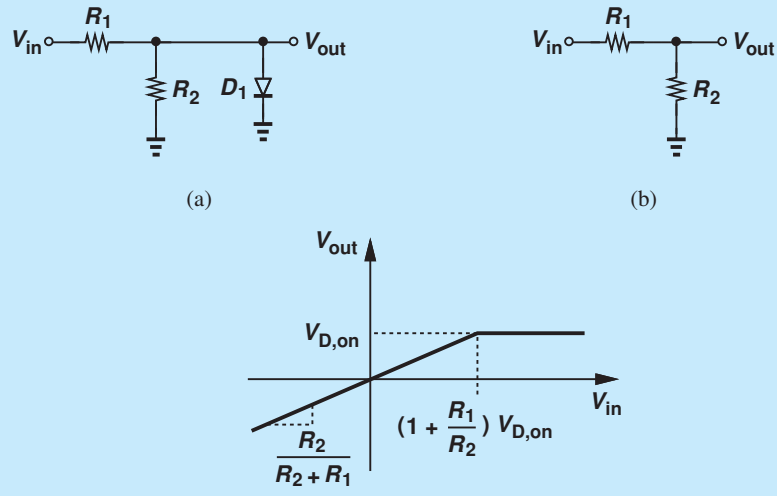


Figure 3.16 (a) Diode circuit, (b) equivalent circuit when D_1 is off, (c) input/output characteristic.

Solution

In this case, the voltage across the diode happens to be equal to the output voltage. We note that if $V_{in} = -\infty$, D_1 is reverse biased and the circuit reduces to that in Fig. 3.16(b). Consequently,

$$v_{out} = \frac{R_2}{R_1 + R_2} V_{in}. \tag{3.17}$$

At what point does D_1 turn on? The diode voltage must reach $V_{D,on}$, requiring an input voltage given by:

$$\frac{R_2}{R_1 + R_2} V_{in} = V_{D,on}, \tag{3.18}$$

and hence

$$V_{in} = \left(1 + \frac{R_1}{R_2}\right) V_{D,on}. \tag{3.19}$$

The reader may question the validity of this result: if the diode is indeed on, it draws current and the diode voltage is no longer equal to $[R_2/(R_1 + R_2)]V_{in}$. So why did we express the diode voltage as such in Eq. (3.18)? To determine the break point, we assume V_{in} gradually increases so that it places the diode at the *edge* of the turn-on, e.g., it creates

$V_{out} \approx 799$ mV. The diode therefore still draws no current, but the voltage across it and hence the input voltage are almost sufficient to turn it on.

For $V_{in} > (1 + R_1/R_2)V_{D,on}$, D_1 remains forward-biased, yielding $V_{out} = V_{D,on}$. Figure 3.16(c) plots the overall characteristic.

Exercise Repeat the above example but assume the terminals of D_1 are swapped, i.e., the anode is tied to ground and the cathode the output node.

Exercise For the above example, plot the current through R_1 as a function of V_{in}.

Example 3.15 Plot the input/output characteristic for the circuit shown in Fig. 3.17(a). Assume a constant-voltage model for the diode.

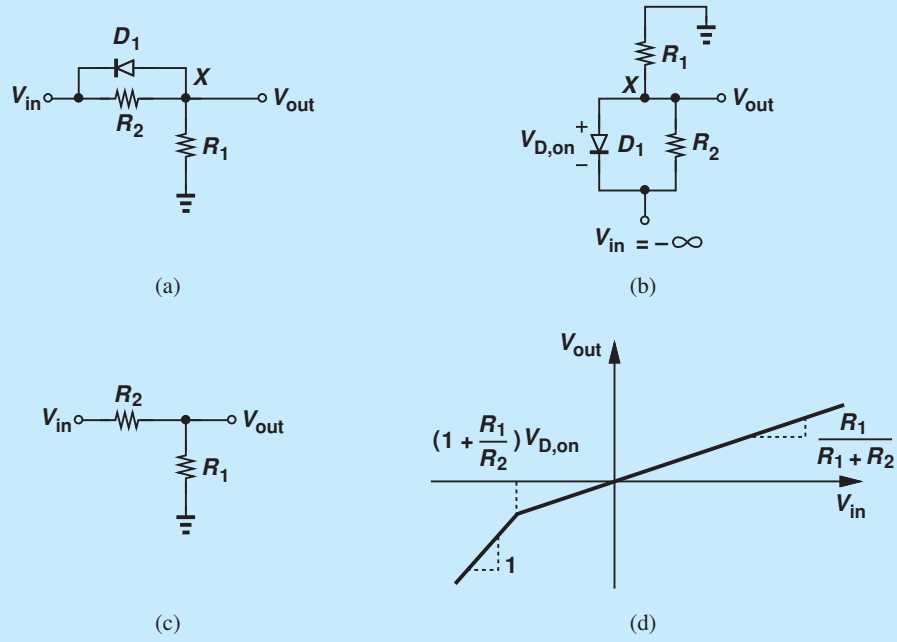


Figure 3.17 (a) Diode circuit, (b) illustration for very negative inputs, (c) equivalent circuit when D_1 is off, (d) input/output characteristic.

Solution We begin with $V_{in} = -\infty$, and redraw the circuit as depicted in Fig. 3.17(b), placing the more negative voltages on the bottom and the more positive voltages on the top. This diagram suggests that the diode operates in forward bias, establishing a voltage at node X equal to $V_{in} + V_{D,on}$. Note that in this regime, V_X is independent of R_2 because D_1 acts as a battery. Thus, so long as D_1 is on, we have

$$V_{out} = V_{in} + V_{D,on}. \tag{3.20}$$

We also compute the current flowing through R_2 and R_1:

$$I_{R2} = \frac{V_{D,on}}{R_2} \tag{3.21}$$

$$I_{R1} = \frac{0 - V_X}{R_1} \tag{3.22}$$

$$= \frac{-(V_{in} + V_{D,on})}{R_1}. \tag{3.23}$$

Thus, as V_{in} increases from $-\infty$, I_{R2} remains constant but $|I_{R1}|$ decreases; i.e., at some point $I_{R2} = I_{R1}$.

At what point does D_1 turn off? Interestingly, in this case it is simpler to seek the condition that results in a zero current through the diode rather than insufficient voltage across it. The observation that at some point, $I_{R2} = I_{R1}$ proves useful here as this condition also implies that D_1 carries no current (KCL at node X). In other words, D_1 turns off if V_{in} is chosen to yield $I_{R2} = I_{R1}$. From (3.21) and (3.23),

$$\frac{V_{D,on}}{R_2} = -\frac{V_{in} + V_{D,on}}{R_1} \tag{3.24}$$

and hence

$$V_{in} = -\left(1 + \frac{R_1}{R_2}\right) V_{D,on}. \tag{3.25}$$

As V_{in} exceeds this value, the circuit reduces to that shown in Fig. 3.17(c) and

$$V_{out} = \frac{R_1}{R_1 + R_2} V_{in}. \tag{3.26}$$

The overall characteristic is shown in Fig. 3.17(d).

The reader may find it interesting to recognize that the circuits of Figs. 3.16(a) and 3.17(a) are identical: in the former, the output is sensed across the diode whereas in the latter it is sensed across the series resistor.

Exercise Repeat the above example if the terminals of the diode are swapped.

As mentioned in Example 3.4, in more complex circuits, it may be difficult to correctly predict the region of operation of each diode by inspection. In such cases, we may simply make a guess, proceed with the analysis, and eventually determine if the final result agrees or conflicts with the original guess. Of course, we still apply intuition to minimize the guesswork. The following example illustrates this approach.

Example 3.16 Plot the input/output characteristic of the circuit shown in Fig. 3.18(a) using the constant-voltage diode model.

Solution We begin with $V_{in} = -\infty$, predicting intuitively that D_1 is on. We also (blindly) assume that D_2 is on, thus reducing the circuit to that in Fig. 3.18(b). The path through $V_{D,on}$ and

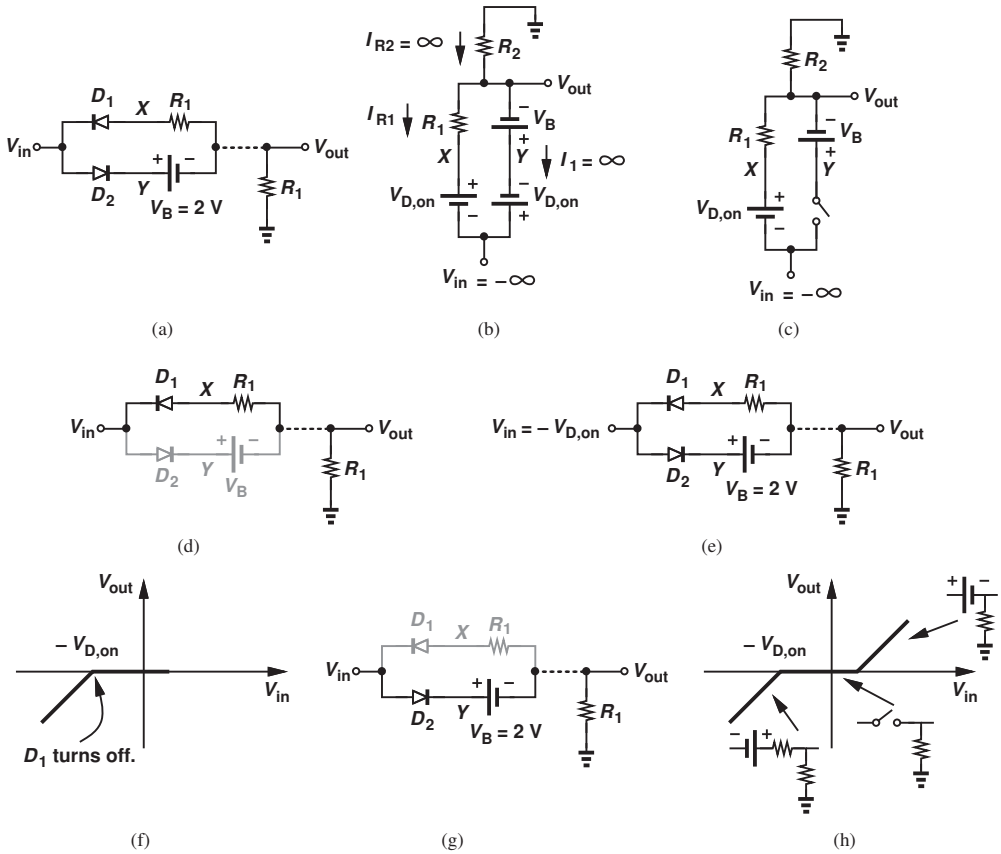


Figure 3.18 (a) Diode circuit, (b) possible equivalent circuit for very negative inputs, (c) simplified circuit, (d) equivalent circuit, (e) equivalent circuit for $V_{in} = -V_{D,on}$, (f) section of input/output characteristic, (g) equivalent circuit, (f) complete input/output characteristic.

V_B creates a difference of $V_{D,on} + V_B$ between V_{in} and V_{out}, i.e., $V_{out} = V_{in} - (V_{D,on} + V_B)$. This voltage difference also appears across the branch consisting of R_1 and $V_{D,on}$, yielding

$$R_1 I_{R1} + V_{D,on} = -(V_B + V_{D,on}), \tag{3.27}$$

and hence

$$I_{R1} = \frac{-V_B - 2V_{D,on}}{R_1}. \tag{3.28}$$

That is, I_{R1} is independent of V_{in}. We must now analyze these results to determine whether they agree with our assumptions regarding the state of D_1 and D_2.

Consider the current flowing through R_2:

$$I_{R2} = -\frac{V_{out}}{R_2} \tag{3.29}$$

$$= -\frac{V_{in} - (V_{D,on} - V_B)}{R_2}, \tag{3.30}$$

which approaches $+\infty$ for $V_{in} = -\infty$. The large value of I_{R2} and the constant value of I_{R1} indicate that the branch consisting of V_B and D_2 carries a large current with the direction shown. That is, D_2 must conduct current from its cathode to its anode, which is not possible.

In summary, we have observed that the forward bias assumption for D_2 translates to a current in a prohibited direction. Thus, D_2 operates in reverse bias for $V_{in} = -\infty$. Redrawing the circuit as in Fig. 3.18(c) and noting that $V_X = V_{in} + V_{D,on}$, we have

$$V_{out} = (V_{in} + V_{D,on})\frac{R_2}{R_1 + R_2}. \tag{3.31}$$

We now raise V_{in} and determine the first break point, i.e., the point at which D_1 turns off or D_2 turns on. Which one occurs first? Let us assume D_1 turns off first and obtain the corresponding value of V_{in}. Since D_2 is assumed off, we draw the circuit as shown in Fig. 3.18(d). Assuming that D_1 is still slightly on, we recognize that at $V_{in} \approx -V_{D,on}$, $V_X = V_{in} + V_{D,on}$ approaches zero, yielding a zero current through R_1, R_2, and hence D_1. The diode therefore turns off at $V_{in} = -V_{D,on}$.

We must now verify the assumption that D_2 remains off. Since at this break point, $V_X = V_{out} = 0$, the voltage at node Y is equal to $+V_B$ whereas the cathode of D_2 is at $-V_{D,on}$ [Fig. 3.18(e)]. In other words, D_2 is indeed off. Fig. 3.18(f) plots the input/output characteristic to the extent computed thus far, revealing that $V_{out} = 0$ after the first break point because the current flowing through R_1 and R_2 is equal to zero.

At what point does D_2 turn on? The input voltage must exceed V_Y by $V_{D,on}$. Before D_2 turns on, $V_{out} = 0$, and $V_Y = V_B$; i.e., V_{in} must reach $V_B + V_{D,on}$, after which the circuit is configured as shown in Fig. 3.18(g). Consequently,

$$V_{out} = V_{in} - V_{D,on} - V_B. \tag{3.32}$$

Figure 3.18(h) plots the overall result, summarizing the regions of operation.

Exercise In the above example, assume D_2 turns on before D_1 turns off and show that the results conflict with the assumption.

3.4 LARGE-SIGNAL AND SMALL-SIGNAL OPERATION

Our treatment of diodes thus far has allowed arbitrarily large voltage and current changes, thereby requiring a "general" model such as the exponential I/V characteristic. We call this regime "large-signal operation" and the exponential characteristic the "large-signal model" to emphasize that the model can accommodate arbitrary signal levels. However, as seen in previous examples, this model often complicates the analysis, making it difficult to develop an intuitive understanding of the circuit's operation. Furthermore, as the

number of nonlinear devices in the circuit increases, "manual" analysis eventually becomes impractical.

The ideal and constant-voltage diode models resolve the issues to some extent, but the sharp nonlinearity at the turn-on point still proves problematic. The following example illustrates the general difficulty.

Example 3.17

Having lost his 2.4-V cellphone charger, an electrical engineering student tries several stores but does not find adaptors with outputs less than 3 V. He then decides to put his knowledge of electronics to work and constructs the circuit shown in Fig. 3.19, where three identical diodes in forward bias produce a total voltage of $V_{out} = 3V_D \approx 2.4$ V and resistor R_1 sustains the remaining 600 mV. Neglect the current drawn by the cellphone.[6] (a) Determine the reverse saturation current, I_{S1} so that $V_{out} = 2.4$ V. (b) Compute V_{out} if the adaptor voltage is in fact 3.1 V.

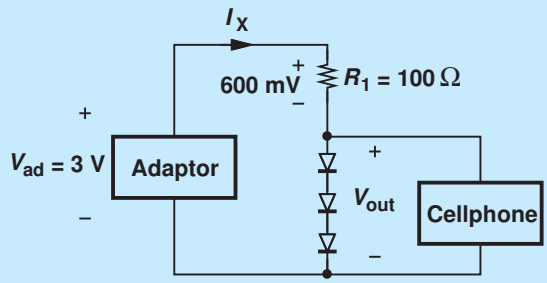


Figure 3.19 Adaptor feeding a cellphone.

Solution

(a) With $V_{out} = 2.4$ V, the current flowing through R_1 is equal to

$$I_X = \frac{V_{ad} - V_{out}}{R_1} \tag{3.33}$$

$$= 6\,\text{mA}. \tag{3.34}$$

We note that each diode carries I_X and hence

$$I_X = I_S \exp \frac{V_D}{V_T}. \tag{3.35}$$

It follows that

$$6\,\text{mA} = I_S \exp \frac{800\,\text{mV}}{26\,\text{mV}} \tag{3.36}$$

and

$$I_S = 2.602 \times 10^{-16}\,\text{A}. \tag{3.37}$$

(b) If V_{ad} increases to 3.1 V, we expect that V_{out} increases only slightly. To understand why, first suppose V_{out} remains constant and equal to 2.4 V. Then, the additional 0.1 V must drop across R_1, raising I_X to 7 mA. Since the voltage across each diode has a

[6] Made for the sake of simplicity here, this assumption may not be valid.

logarithmic dependence upon the current, the change from 6 mA to 7 mA indeed yields a small change in V_{out}.[7]

To examine the circuit quantitatively, we begin with $I_X = 7$ mA and iterate:

$$V_{out} = 3V_D \tag{3.38}$$

$$= 3V_T \ln \frac{I_X}{I_S} \tag{3.39}$$

$$= 2.412\,\text{V}. \tag{3.40}$$

This value of V_{out} gives a new value for I_X:

$$I_X = \frac{V_{ad} - V_{out}}{R_1} \tag{3.41}$$

$$= 6.88\,\text{mA}, \tag{3.42}$$

which translates to a new V_{out}:

$$V_{out} = 3V_D \tag{3.43}$$

$$= 2.411\,\text{V}. \tag{3.44}$$

Noting the very small difference between (3.40) and (3.44), we conclude that $V_{out} = 2.411$ V with good accuracy. The constant-voltage diode model would not be useful in this case.

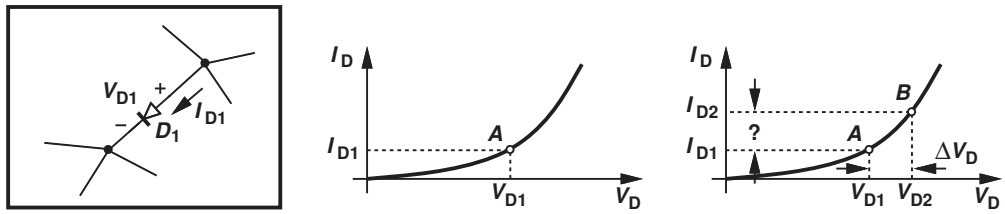
Exercise Repeat the above example if an output voltage of 2.35 is desired.

The situation[6] described above is an example of small "perturbations" in circuits. The change in V_{ad} from 3 V to 3.1 V results in a small change in the circuit's voltages and currents, motivating us to seek a simpler analysis method that can replace the nonlinear equations and the inevitable iterative procedure. Of course, since the above example does not present an overwhelmingly difficult problem, the reader may wonder if a simpler approach is really necessary. But, as seen in subsequent chapters, circuits containing complex devices such as transistors may indeed become impossible to analyze if the nonlinear equations are retained.

These thoughts lead us to the extremely important concept of "small-signal operation," whereby the circuit experiences only small changes in voltages and currents and can therefore be simplified through the use of "small-signal models" for nonlinear devices. The simplicity arises because such models are *linear*, allowing standard circuit analysis and obviating the need for iteration. The definition of "small" will become clear later.

To develop our understanding of small-signal operation, let us consider diode D_1 in Fig. 3.20(a), which sustains a voltage V_{D1} and carries a current I_{D1} [point A in Fig. 3.20(b)]. Now suppose a perturbation in the circuit changes the diode voltage by a small amount

[67] Recall from Eq. (2.109) that a tenfold change in a diode's current translates to a 60-mV change in its voltage.



(a) (b) (c)

Figure 3.20 (a) General circuit containing a diode, (b) operating point of D_1, (c) change in I_D as a result of change in V_D.

ΔV_D [point B in Fig. 3.20(c)]. How do we predict the change in the diode current, ΔI_D? We can begin with the nonlinear characteristic:

$$I_{D2} = I_S \exp \frac{V_{D1} + \Delta V}{V_T} \tag{3.45}$$

$$= I_S \exp \frac{V_{D1}}{V_T} \exp \frac{\Delta V}{V_T}. \tag{3.46}$$

If $\Delta V \ll V_T$, then $\exp(\Delta V/V_T) \approx 1 + \Delta V/V_T$ and

$$I_{D2} = I_S \exp \frac{V_{D1}}{V_T} + \frac{\Delta V}{V_T} I_S \exp \frac{V_{D1}}{V_T} \tag{3.47}$$

$$= I_{D1} + \frac{\Delta V}{V_T} I_{D1}. \tag{3.48}$$

That is,

$$\Delta I_D = \frac{\Delta V}{V_T} I_{D1}. \tag{3.49}$$

The key observation here is that ΔI_D is a *linear* function of ΔV, with a proportionality factor equal to I_{D1}/V_T. (Note that larger values of I_{D1} lead to a greater ΔI_D for a given ΔV_D. The significance of this trend becomes clear later.)

The above result should not come as a surprise: if the change in V_D is small, the section of the characteristic in Fig. 3.20(c) between points A and B can be approximated by a straight line (Fig. 3.21), with a slope equal to the local slope of the characteristic.

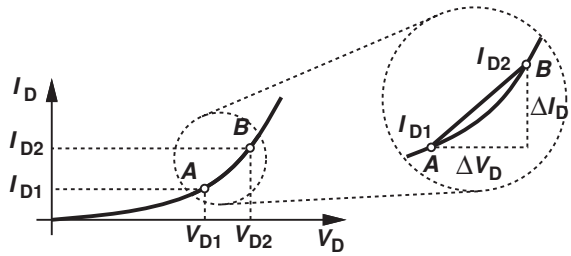


Figure 3.21 Approximation of characteristic by a straight line.

In other words,

$$\frac{\Delta I_D}{\Delta V_D} = \left.\frac{dI_D}{dV_D}\right|_{VD=VD1} \tag{3.50}$$

$$= \frac{I_S}{V_T} \exp \frac{V_{D1}}{V_T} \tag{3.51}$$

$$= \frac{I_{D1}}{V_T}, \tag{3.52}$$

which yields the same result as that in Eq. (3.49).[8]

Let us summarize our results thus far. If the voltage across a diode changes by a small amount (much less than V_T), then the change in the current is given by Eq. (3.49). Equivalently, for small-signal analysis, we can assume the operation is at a point such as A in Fig. 3.21 and, due to a small perturbation, it moves on a straight line to point B with a slope equal to the local slope of the characteristic (i.e., dI_D/dV_D calculated at $V_D = V_{D1}$ or $I_D = I_{D1}$). Point A is called the "bias" point, the "quiescent" point, or the "operating" point.

Example 3.18

A diode is biased at a current of 1 mA. (a) Determine the current change if V_D changes by 1 mV. (b) Determine the voltage change if I_D changes by 10%.

Solution

(a) We have

$$\Delta I_D = \frac{I_D}{V_T}\Delta V_D \tag{3.53}$$

$$= 38.4\,\mu\text{A}. \tag{3.54}$$

(b) Using the same equation yields

$$\Delta V_D = \frac{V_T}{I_D}\Delta I_D \tag{3.55}$$

$$= \left(\frac{26\,\text{mV}}{1\,\text{mA}}\right) \times (0.1\,\text{mA}) \tag{3.56}$$

$$= 2.6\,\text{mV}. \tag{3.57}$$

Exercise

In response to a current change of 1 mA, a diode exhibits a voltage change of 3 mV. Calculate the bias current of the diode.

Equation (3.58) in the above example reveals an interesting aspect of small-signal operation: as far as (small) changes in the diode current and voltage are concerned, the device behaves as a linear resistor. In analogy with Ohm's Law, we define the "small-signal

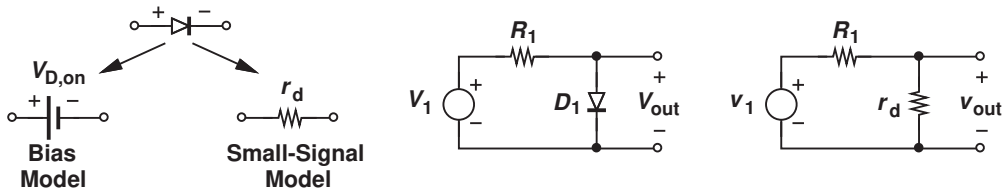
[8]This is also to be expected. Writing Eq. (3.45) to obtain the change in I_D for a small change in V_D is in fact equivalent to taking the derivative.

resistance" of the diode as:

$$r_d = \frac{V_T}{I_D}. \tag{3.58}$$

This quantity is also called the "incremental" resistance to emphasize its validity for small changes. In the above example, $r_d = 26\,\Omega$.

Figure 3.22(a) summarizes the results of our derivations for a forward-biased diode. For bias calculations, the diode is replaced with an ideal voltage source of value $V_{D,on}$, and for small changes, with a resistance equal to r_d. For example, the circuit of Fig. 3.22(b) is transformed to that in Fig. 3.22(c) if only small changes in V_1 and V_{out} are of interest. Note that v_1 and v_{out} in Fig. 3.22(c) represent *changes* in voltage and are called small-signal quantities. In general, we denote small-signal voltages and currents by lower-case letters.



(a) (b) (c)

Figure 3.22 Summary of diode models for bias and signal calculations, (b) circuit example, (c) small-signal model.

Example 3.19

A sinusoidal signal having a peak amplitude of V_p and a dc value of V_0 can be expressed as $V(t) = V_0 + V_p \cos \omega t$. If this signal is applied across a diode and $V_p \ll V_T$, determine the resulting diode current.

Solution

The signal waveform is illustrated in Fig. 3.23(a). As shown in Fig. 3.23(b), we rotate this diagram by 90° so that its vertical axis is aligned with the voltage axis of the diode characteristic. With a signal swing much less than V_T, we can view V_0 and the corresponding current, I_0, as the bias point of the diode and V_p as a small perturbation. It follows that

$$I_0 = I_S \exp \frac{V_0}{V_T}, \tag{3.59}$$

and

$$r_d = \frac{V_T}{I_0}. \tag{3.60}$$

Thus, the peak current is simply equal to

$$I_p = V_p / r_d \tag{3.61}$$

$$= \frac{I_0}{V_T} V_p, \tag{3.62}$$

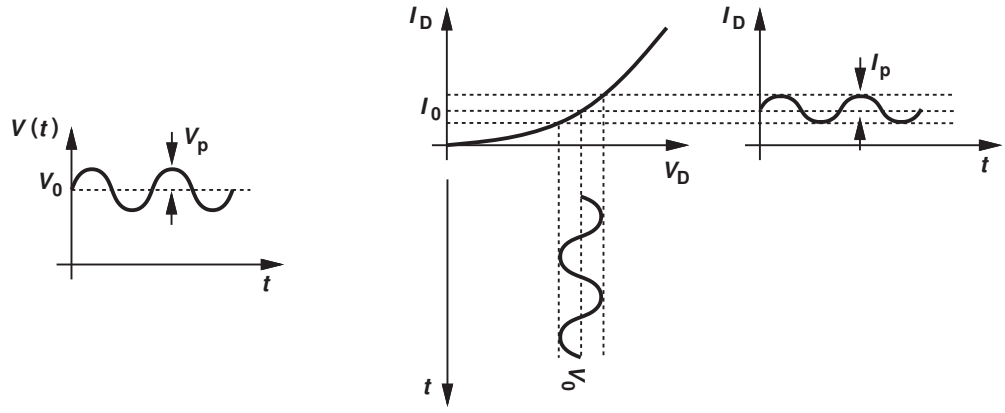


Figure 3.23 (a) Sinusoidal input along with a dc level, (b) response of a diode to the sinusoid.

yielding

$$I_D(t) = I_0 + I_p \cos \omega t \tag{3.63}$$

$$= I_S \exp \frac{V_0}{V_T} + \frac{I_0}{V_T} V_p \cos \omega t. \tag{3.64}$$

Exercise The diode in the above example produces a peak current of 0.1 mA in response to $V_0 = 800\,\text{mV}$ and $V_p = 1.5\,\text{mV}$. Calculate I_S.

The above example demonstrates the utility of small-signal analysis. If V_p were large, we would need to solve the following equation:

$$I_D(t) = I_S \exp \frac{V_0 + V_p \cos \omega t}{V_T}, \tag{3.65}$$

a task much more difficult than the above linear calculations.[9]

Example 3.20 In the derivation leading to Eq. (3.49), we assumed a small change in V_D and obtained the resulting change in I_D. Beginning with $V_D = V_T \ln(I_D/I_s)$, investigate the reverse case, i.e., I_D changes by a small amount and we wish to compute the change in V_D.

[9]The function $\exp(a \sin bt)$ can be approximated by a Taylor expansion or Bessel functions.

Solution Denoting the change in V_D by ΔV_D, we have

$$V_{D1} + \Delta V_D = V_T \ln \frac{I_{D1} + \Delta I_D}{I_S} \tag{3.66}$$

$$= V_T \ln \left[\frac{I_{D1}}{I_S} \left(1 + \frac{\Delta I_D}{I_{D1}} \right) \right] \tag{3.67}$$

$$= V_T \ln \frac{I_{D1}}{I_S} + V_T \ln \left(1 + \frac{\Delta I_D}{I_{D1}} \right). \tag{3.68}$$

For small-signal operation, we assume $\Delta I_D \ll I_{D1}$ and note that $\ln(1+\epsilon) \approx \epsilon$ if $\epsilon \ll 1$. Thus,

$$\Delta V_D = V_T \cdot \frac{\Delta I_D}{I_{D1}}, \tag{3.69}$$

which is the same as Eq. (3.49). Figure 3.24 illustrates the two cases, distinguishing between the cause and the effect.

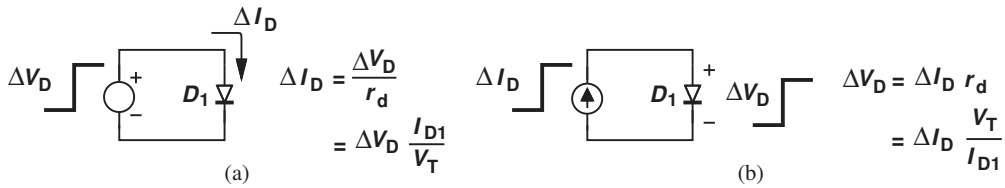


Figure 3.24 Change in diode current (voltage) due to a change in voltage (current).

Exercise Repeat the above example by taking the derivative of the diode voltage equation with respect to I_D.

With our understanding of small-signal operation, we now revisit Example 3.17.

Example 3.21 Repeat part (b) of Example 3.17 with the aid of a small-signal model for the diodes.

Solution Since each diode carries $I_{D1} = 6$ mA with an adaptor voltage of 3 V and $V_{D1} = 800$ mV, we can construct the small-signal model shown in Fig. 3.25, where $v_{ad} = 100$ mV and $r_d = (26\text{ mV})/(6\text{ mA}) = 4.33\ \Omega$. (As mentioned earlier, the voltages shown in this model denote small changes.) We can thus write:

$$v_{out} = \frac{3r_d}{R_1 + 3r_d} v_{ad} \tag{3.70}$$

$$= 11.5\text{ mV}. \tag{3.71}$$

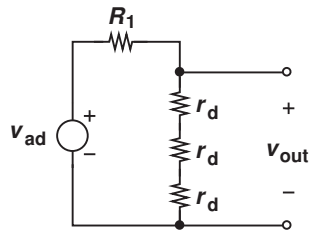


Figure 3.25 Small-signal model of adaptor.

That is, a 100-mV change in V_{ad} yields an 11.5-mV change in V_{out}. In Example 3.17, solution of nonlinear diode equations predicted an 11-mV change in V_{out}. The small-signal analysis therefore offers reasonable accuracy while requiring much less computational effort.

Exercise Repeat Examples (3.17) and (3.21) if the value of R_1 in Fig. 3.19 is changed to 200 Ω.

Considering the power of today's computer software tools, the reader may wonder if the small-signal model is really necessary. Indeed, we utilize sophisticated simulation tools in the design of integrated circuits today, but the intuition gained by hand analysis of a circuit proves invaluable in understanding fundamental limitations and various trade-offs that eventually lead to a compromise in the design. A good circuit designer analyzes and understands the circuit before giving it to the computer for a more accurate analysis. A bad circuit designer, on the other hand, allows the computer to think for him/her.

Example 3.22 In Examples 3.17 and 3.21, the current drawn by the cellphone is neglected. Now suppose, as shown in Fig. 3.26, the load pulls a current of 0.5 mA[10] and determine V_{out}.

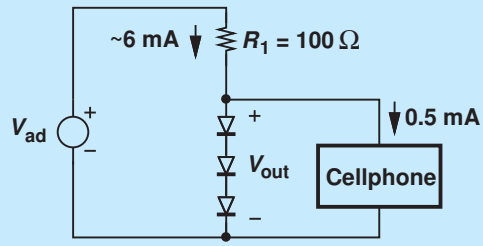


Figure 3.26 Adaptor feeding a cellphone.

[10] A cellphone in reality draws a much higher current.

Solution Since the current flowing through the diodes decreases by 0.5 mA and since this change is much less than the bias current (6 mA), we write the change in the output voltage as:

$$\Delta V_{out} = \Delta I_D \cdot (3r_d) \tag{3.72}$$

$$= 0.5\,\text{mA}(3 \times 4.33\,\Omega) \tag{3.73}$$

$$= 6.5\,\text{mV}. \tag{3.74}$$

Exercise Repeat the above example if R_1 is reduced to 80 Ω.

Did you know?

What would our life be like without diodes? Forget about cell phones, laptops, and digital cameras. We would not even have radios, TVs, GPS, radars, satellites, power plants, or long-distance telephone communication. And, of course, no Google or Facebook. In essence, we would return to the simple lifestyle of the early 1900s—which might not be that bad after all ...

In summary, the analysis of circuits containing diodes (and other nonlinear devices such as transistors) proceeds in three steps: (1) determine—perhaps with the aid of the constant-voltage model—the initial values of voltages and currents (before an input change is applied); (2) develop the small-signal model for each diode (i.e., calculate r_d); (3) replace each diode with its small-signal model and compute the effect of the input change.

3.5 APPLICATIONS OF DIODES

The remainder of this chapter deals with circuit applications of diodes. A brief outline is shown below.

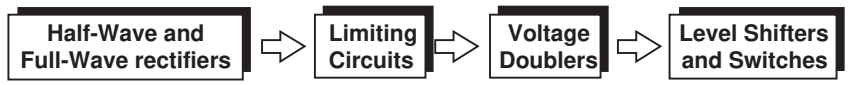


Figure 3.27 Applications of diodes.

3.5.1 Half-Wave and Full-Wave Rectifiers

Half-Wave Rectifier Let us return to the rectifier circuit of Fig. 3.10(b) and study it more closely. In particular, we no longer assume D_1 is ideal, but use a constant-voltage model. As illustrated in Fig. 3.28, V_{out} remains equal to zero until V_{in} exceeds $V_{D,on}$, at which point D_1 turns on and $V_{out} = V_{in} - V_{D,on}$. For $V_{in} < V_{D,on}$, D_1 is off[11] and $V_{out} = 0$. Thus, the circuit still operates as a rectifier but produces a slightly lower dc level.

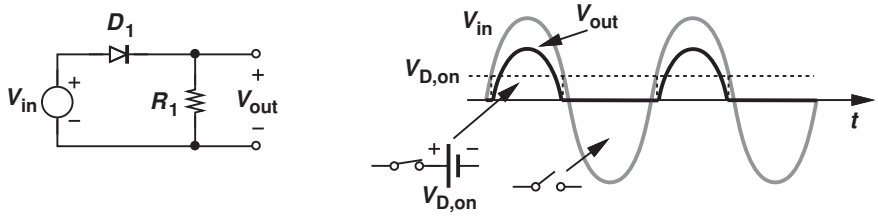


Figure 3.28 Simple rectifier.

[11] If $V_{in} < 0$, D_1 carries a small leakage current, but the effect is negligible.

Example 3.23

Prove that the circuit shown in Fig. 3.29(a) is also a rectifier.

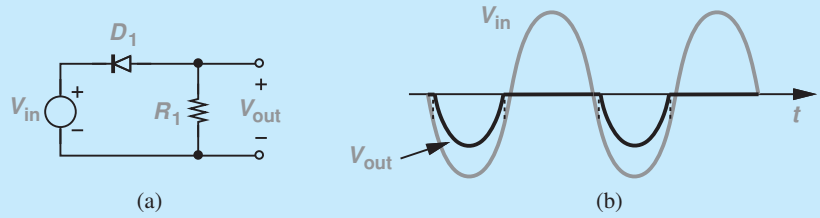


Figure 3.29 Rectification of positive cycles.

Solution

In this case, D_1 remains on for *negative* values of V_{in}, specifically, for $V_{in} \leq -V_{D,on}$. As V_{in} exceeds $-V_{D,on}$, D_1 turns off, allowing R_2 to maintain $V_{out} = 0$. Depicted in Fig. 3.29, the resulting output reveals that this circuit is also a rectifier, but it blocks the positive cycles.

Exercise

Plot the output if D_1 is an ideal diode.

Called a "half-wave rectifier," the circuit of Fig. 3.28 does not produce a useful output. Unlike a battery, the rectifier generates an output that *varies* considerably with time and cannot supply power to electronic devices. We must therefore attempt to create a *constant* output.

Fortunately, a simple modification solves the problem. As depicted in Fig. 3.30(a), the resistor is replaced with a capacitor. The operation of this circuit is quite different from that of the above rectifier. Assuming a constant-voltage model for D_1 in forward bias, we begin with a zero initial condition across C_1 and study the behavior of the circuit [Fig. 3.30(b)]. As V_{in} rises from zero, D_1 is off until $V_{in} > V_{D,on}$, at which point D_1 begins to act as a battery and $V_{out} = V_{in} - V_{D,on}$. Thus, V_{out} reaches a peak value of $V_p - V_{D,on}$. What happens as V_{in}

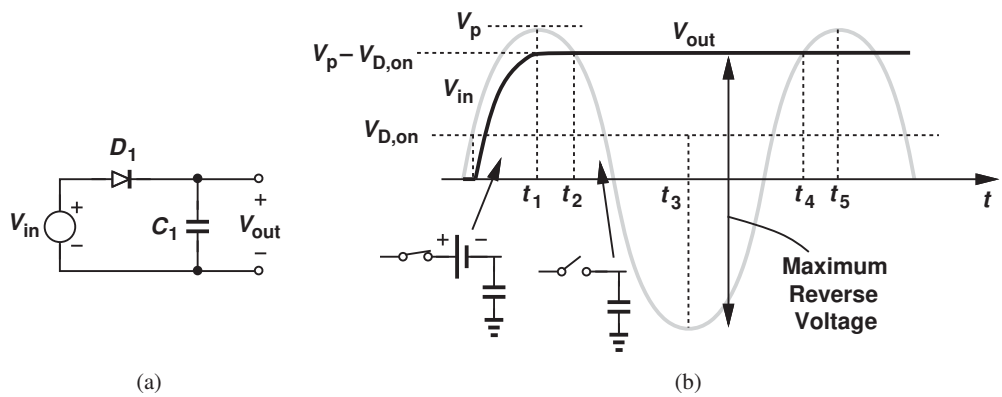


Figure 3.30 (a) Diode-capacitor circuit, (b) input and output waveforms.

passes its peak value? At $t = t_1$, we have $V_{in} = V_p$ and $V_{out} = V_p - V_{D,on}$. As V_{in} begins to fall, V_{out} must remain *constant*. This is because if V_{out} were to fall, then C_1 would need to be *discharged* by a current flowing from its top plate through the cathode of D_1, which is impossible.[12] The diode therefore turns off after t_1. At $t = t_2$, $V_{in} = V_p - V_{D,on} = V_{out}$, i.e., the diode sustains a zero voltage difference. At $t > t_2$, $V_{in} < V_{out}$ and the diode experiences a negative voltage.

Continuing our analysis, we note that at $t = t_3$, $V_{in} = -V_p$, applying a maximum reverse bias of $V_{out} - V_{in} = 2V_p - V_{D,on}$ across the diode. For this reason, diodes used in rectifiers must withstand a reverse voltage of approximately $2V_p$ with no breakdown.

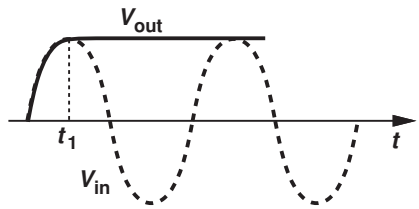
Does V_{out} change after $t = t_1$? Let us consider $t = t_4$ as a potentially interesting point. Here, V_{in} just exceeds V_{out} but still cannot turn D_1 on. At $t = t_5$, $V_{in} = V_p = V_{out} + V_{D,on}$, and D_1 is on, but V_{out} exhibits no tendency to change because the situation is identical to that at $t = t_1$. In other words, V_{out} remains equal to $V_p - V_{D,on}$ indefinitely.

Example 3.24

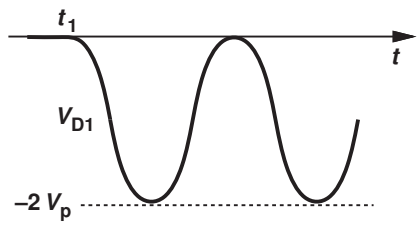
Assuming an ideal diode model, (a) Repeat the above analysis. (b) Plot the voltage across D_1, V_{D1}, as a function of time.

Solution

(a) With a zero initial condition across C_1, D_1 turns on as V_{in} exceeds zero and $V_{out} = V_{in}$. After $t = t_1$, V_{in} falls below V_{out}, turning D_1 off. Figure 3.31(a) shows the input and output waveforms.



(a)



(b)

Figure 3.31 (a) Input and output waveforms of the circuit in Fig. 3.30 with an ideal diode, (b) voltage across the diode.

[12] The water pipe analogy in Fig. 3.3(c) proves useful here.

(b) The voltage across the diode is $V_{D1} = V_{in} - V_{out}$. Using the plots in Fig. 3.31(a), we readily arrive at the waveform in Fig. 3.31(b). Interestingly, V_{D1} is similar to V_{in} but with the average value shifted from zero to $-V_p$. We will exploit this result in the design of voltage doublers (Section 3.5.4).

Exercise Repeat the above example if the terminals of the diode are swapped.

The circuit of Fig. 3.30(a) achieves the properties required of an "ac-dc converter," generating a constant output equal to the peak value of the input sinusoid.[13] But how is the value of C_1 chosen? To answer this question, we consider a more realistic application where this circuit must provide a *current* to a load.

Example 3.25 A laptop computer consumes an average power of 25 W with a supply voltage of 3.3 V. Determine the average current drawn from the batteries or the adaptor.

Solution Since $P = V \cdot I$, we have $I \approx 7.58$ A. If the laptop is modeled by a resistor, R_L, then $R_L = V/I = 0.436\,\Omega$.

Exercise What power dissipation does a 1-Ω load represent for such a supply voltage?

As suggested by the above example, the load can be represented by a simple resistor in some cases [Fig. 3.32(a)]. We must therefore repeat our analysis with R_L present. From the waveforms in Fig. 3.32(b), we recognize that V_{out} behaves as before until $t = t_1$, still exhibiting a value of $V_{in} - V_{D,on} = V_p - V_{D,on}$ if the diode voltage is assumed relatively constant. However, as V_{in} begins to fall after $t = t_1$, so does V_{out} because R_L provides a discharge path for C_1. Of course, since changes in V_{out} are undesirable, C_1 must be so large that the current drawn by R_L does not reduce V_{out} significantly. With such a choice of C_1, V_{out} falls slowly and D_1 remains reverse biased.

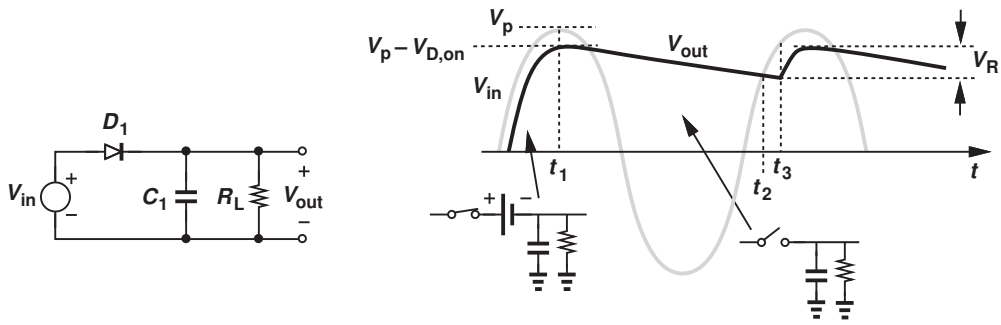


Figure 3.32 (a) Rectifier driving a resistive load, (b) input and output waveforms.

[13] This circuit is also called a "peak detector."

The output voltage continues to decrease while V_{in} goes through a negative excursion and returns to positive values. At some point, $t = t_2$, V_{in} and V_{out} become equal and slightly later, at $t = t_3$, V_{in} exceeds V_{out} by $V_{D,on}$, thereby turning D_1 on and forcing $V_{out} = V_{in} - V_{D,on}$. Hereafter, the circuit behaves as in the first cycle. The resulting variation in V_{out} is called the "ripple." Also, C_1 is called the "smoothing" or "filter" capacitor.

Example 3.26 Sketch the output waveform of Fig. 3.32 as C_1 varies from very large values to very small values.

Solution If C_1 is very large, the current drawn by R_L when D_1 is off creates only a small change in V_{out}. Conversely, if C_1 is very small, the circuit approaches that in Fig. 3.28, exhibiting large variations in V_{out}. Figure 3.33 illustrates several cases.

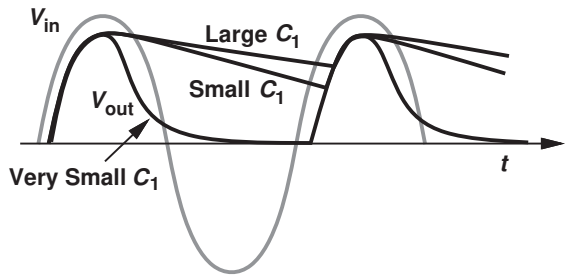


Figure 3.33 Output waveform of rectifier for different values of smoothing capacitor.

Exercise Repeat the above example for different values of R_L with C_1 constant.

Ripple Amplitude* In typical applications, the (peak-to-peak) amplitude of the ripple, V_R, in Fig. 3.32(b) must remain below 5 to 10% of the input peak voltage. If the maximum current drawn by the load is known, the value of C_1 is chosen large enough to yield an acceptable ripple. To this end, we must compute V_R analytically (Fig. 3.34). Since $V_{out} = V_p - V_{D,on}$ at $t = t_1$, the discharge of C_1 through R_L can be expressed as:

$$V_{out}(t) = (V_p - V_{D,on}) \exp \frac{-t}{R_L C_1} \quad 0 \le t \le t_3, \tag{3.75}$$

where we have chosen $t_1 = 0$ for simplicity. To ensure a small ripple, $R_L C_1$ must be much greater than $t_3 - t_1$; thus, noting that $\exp(-\epsilon) \approx 1 - \epsilon$ for $\epsilon \ll 1$,

$$V_{out}(t) \approx (V_p - V_{D,on}) \left(1 - \frac{t}{R_L C_1}\right) \tag{3.76}$$

$$\approx (V_p - V_{D,on}) - \frac{V_p - V_{D,on}}{R_L} \cdot \frac{t}{C_1}. \tag{3.77}$$

*This section can be skipped in a first reading.

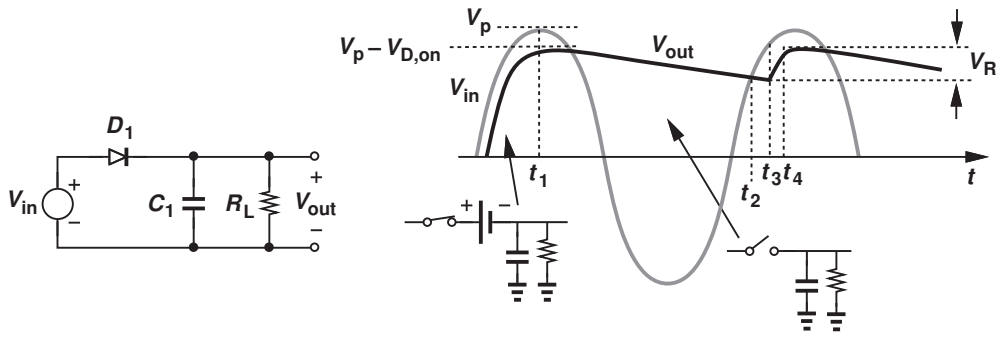


Figure 3.34 Ripple at output of a rectifier.

The first term on the right-hand side represents the initial condition across C_1 and the second term, a falling ramp—as if a constant current equal to $(V_p - V_{D,on})/R_L$ discharges C_1.[14] This result should not come as a surprise because the nearly constant voltage across R_L results in a relatively constant current equal to $(V_p - V_{D,on})/R_L$.

The peak-to-peak amplitude of the ripple is equal to the amount of discharge at $t = t_3$. Since $t_4 - t_3$ is equal to the input period, T_{in}, we write $t_3 - t_1 = T_{in} - \Delta T$, where $\Delta T (= t_4 - t_3)$ denotes the time during which D_1 is on. Thus,

$$V_R = \frac{V_p - V_{D,on}}{R_L} \frac{T_{in} - \Delta T}{C_1}. \tag{3.78}$$

Recognizing that if C_1 discharges by a small amount, then the diode turns on for only a brief period, we can assume $\Delta T \ll T_{in}$ and hence

$$V_R \approx \frac{V_p - V_{D,on}}{R_L} \cdot \frac{T_{in}}{C_1} \tag{3.79}$$

$$\approx \frac{V_p - V_{D,on}}{R_L C_1 f_{in}}, \tag{3.80}$$

where $f_{in} = T_{in}^{-1}$.

Example 3.27

A transformer converts the 110-V, 60-Hz line voltage to a peak-to-peak swing of 9 V. A half-wave rectifier follows the transformer to supply the power to the laptop computer of Example 3.25. Determine the minimum value of the filter capacitor that maintains the ripple below 0.1 V. Assume $V_{D,on} = 0.8$ V.

Solution

We have $V_p = 4.5$ V, $R_L = 0.436\ \Omega$, and $T_{in} = 16.7$ ms. Thus,

$$C_1 = \frac{V_p - V_{D,on}}{V_R} \cdot \frac{T_{in}}{R_L} \tag{3.81}$$

$$= 1.417 \text{ F}. \tag{3.82}$$

[14] Recall that $I = CdV/dt$ and hence $dV = (I/C)dt$.

This is a very large value. The designer must trade the ripple amplitude with the size, weight, and cost of the capacitor. In fact, limitations on size, weight, and cost of the adaptor may dictate a much greater ripple, e.g., 0.5 V, thereby demanding that the circuit following the rectifier tolerate such a large, periodic variation.

Exercise Repeat the above example for 220-V, 50-Hz line voltage, assuming the transformer still produces a peak-to-peak swing of 9 V. Which mains frequency gives a more desirable choice of C_1?

In many cases, the current drawn by the load is known. Repeating the above analysis with the load represented by a constant current source or simply viewing $(V_p - V_{D,on})/R_L$ in Eq. (3.80) as the load current, I_L, we can write

$$V_R = \frac{I_L}{C_1 f_{in}}. \tag{3.83}$$

Diode Peak Current* We noted in Fig. 3.30(b) that the diode must exhibit a reverse breakdown voltage of at least $2V_p$. Another important parameter of the diode is the maximum forward bias current that it must tolerate. For a given junction doping profile and geometry, if the current exceeds a certain limit, the power dissipated in the diode ($= V_D I_D$) may raise the junction temperature so much as to damage the device.

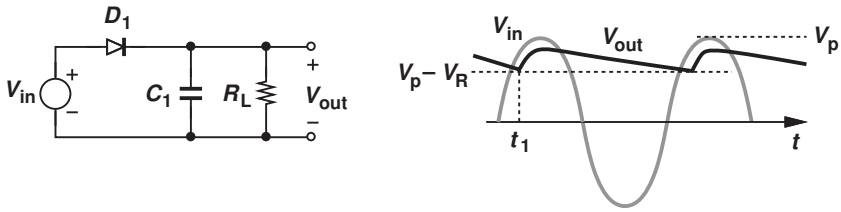


Figure 3.35 Rectifier circuit for calculation of I_D.

We recognize from Fig. 3.35, that the diode current in forward bias consists of two components: (1) the transient current drawn by C_1, $C_1 dV_{out}/dt$, and (2) the current supplied to R_L, approximately equal to $(V_p - V_{D,on})/R_L$. The peak diode current therefore occurs when the first component reaches a maximum, i.e., at the point D_1 turns on because the slope of the output waveform is maximum. Assuming $V_{D,on} \ll V_p$ for simplicity, we note that the point at which D_1 turns on is given by $V_{in}(t_1) = V_p - V_R$. Thus, for $V_{in}(t) = V_p \sin \omega_{in} t$,

$$V_p \sin \omega_{in} t_1 = V_p - V_R, \tag{3.84}$$

and hence

$$\sin \omega_{in} t_1 = 1 - \frac{V_R}{V_p}. \tag{3.85}$$

*This section can be skipped in a first reading.

With $V_{D,on}$ neglected, we also have $V_{out}(t) \approx V_{in}(t)$, obtaining the diode current as

$$I_{D1}(t) = C_1 \frac{dV_{out}}{dt} + \frac{V_p}{R_L} \tag{3.86}$$

$$= C_1 \omega_{in} V_p \cos \omega_{in} t + \frac{V_p}{R_L}. \tag{3.87}$$

This current reaches a peak at $t = t_1$:

$$I_p = C_1 \omega_{in} V_p \cos \omega_{in} t_1 + \frac{V_p}{R_L}, \tag{3.88}$$

which, from (3.85), reduces to

$$I_p = C_1 \omega_{in} V_p \sqrt{1 - \left(1 - \frac{V_R}{V_p}\right)^2} + \frac{V_p}{R_L} \tag{3.89}$$

$$= C_1 \omega_{in} V_p \sqrt{\frac{2V_R}{V_p} - \frac{V_R^2}{V_p^2}} + \frac{V_p}{R_L}. \tag{3.90}$$

Since $V_R \ll V_p$, we neglect the second term under the square root:

$$I_p \approx C_1 \omega_{in} V_p \sqrt{\frac{2V_R}{V_p}} + \frac{V_p}{R_L} \tag{3.91}$$

$$\approx \frac{V_p}{R_L} \left(R_L C_1 \omega_{in} \sqrt{\frac{2V_R}{V_p}} + 1 \right). \tag{3.92}$$

Example 3.28 Determine the peak diode current in Example 3.27 assuming $V_{D,on} \approx 0$ and $C_1 = 1.417$ F.

Solution We have $V_p = 4.5$ V, $R_L = 0.436\ \Omega$, $\omega_{in} = 2\pi(60\text{ Hz})$, and $V_R = 0.1$ V. Thus,

$$I_p = 517 \text{ A}. \tag{3.93}$$

This value is extremely large. Note that the current drawn by C_1 is much greater than that flowing through R_L.

Exercise Repeat the above example if $C_1 = 1000\ \mu$F.

Full-Wave Rectifier The half-wave rectifier studied above blocks the negative half cycles of the input, allowing the filter capacitor to be discharged by the load for almost the entire period. The circuit therefore suffers from a large ripple in the presence of a heavy load (a high current).

It is possible to reduce the ripple voltage by a factor of two through a simple modification. Illustrated in Fig. 3.36(a), the idea is to pass both positive and negative half cycles to the output, but with the negative half cycles *inverted* (i.e., multiplied by -1). We first implement a circuit that performs this function [called a "full-wave

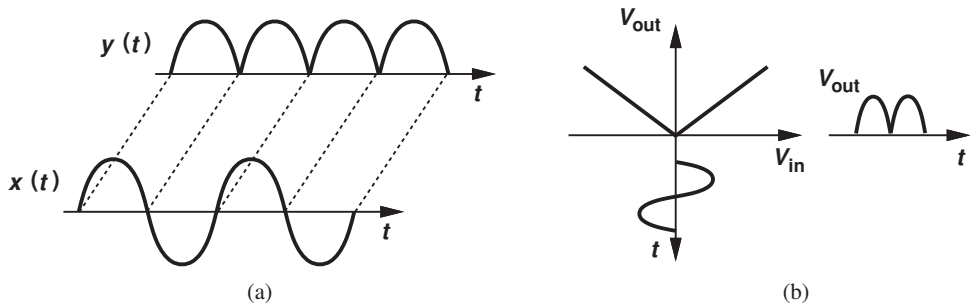


Figure 3.36 (a) Input and output waveforms and (b) input/output characteristic of a full-wave rectifier.

rectifier" (FWR)] and next prove that it indeed exhibits a smaller ripple. We begin with the assumption that the diodes are ideal to simplify the task of circuit synthesis. Figure 3.36(b) depicts the desired input/output characteristic of the full-wave rectifier.

Consider the two half-wave rectifiers shown in Fig. 3.37(a), where one blocks negative half cycles and the other, positive half cycles. Can we combine these circuits to realize a full-wave rectifier? We may attempt the circuit in Fig. 3.37(b), but, unfortunately, the output contains both positive and negative half cycles, i.e., no rectification is performed because the negative half cycles are not inverted. Thus, the problem is reduced to that illustrated in Fig. 3.37(c): we must first design a half-wave rectifier that *inverts*. Shown in Fig. 3.37(d) is such a topology, which can also be redrawn as in Fig. 3.37(e) for simplicity. Note the polarity of V_{out} in the two diagrams. Here, if $V_{in} < 0$, both D_2 and D_1 are on and $V_{out} = -V_{in}$. Conversely, if $V_{in} > 0$, both diodes are off, yielding a zero current through R_L and hence $V_{out} = 0$. In analogy with this circuit, we also compose that in Fig. 3.37(f), which simply blocks the negative input half cycles; i.e., $V_{out} = 0$ for $V_{in} < 0$ and $V_{out} = V_{in}$ for $V_{in} > 0$.

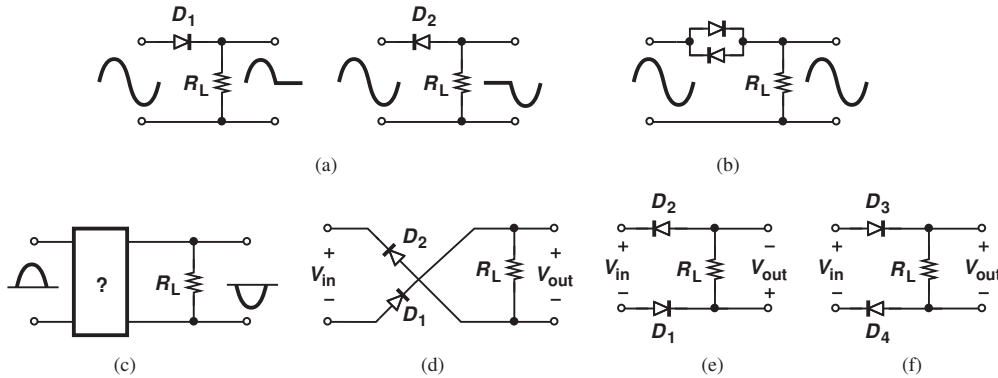


Figure 3.37 (a) Rectification of each half cycle, (b) no rectification, (c) rectification and inversion, (d) realization of (c), (e) path for negative half cycles, (f) path for positive half cycles.

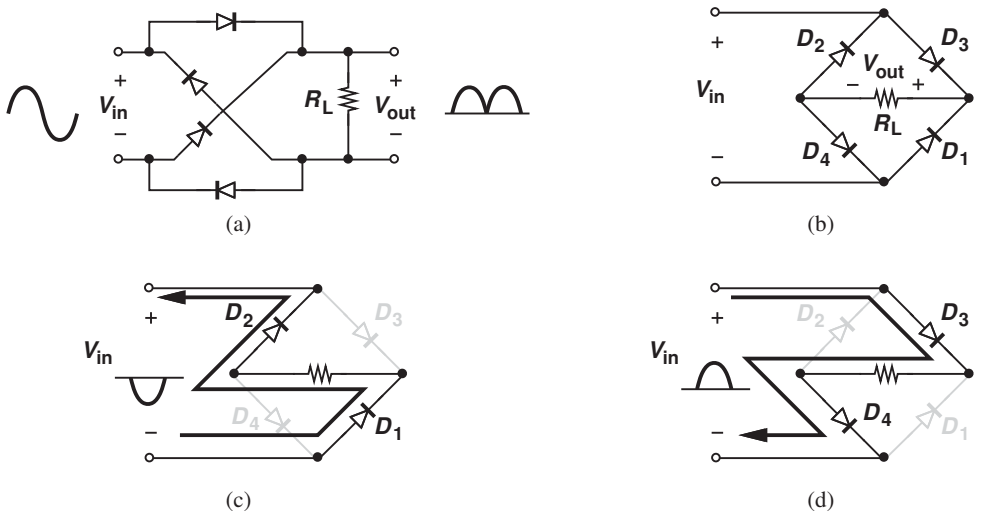


Figure 3.38 (a) Full-wave rectifier, (b) simplified diagram, (c) current path for negative input, (d) current path for positive input.

With the foregoing developments, we can now combine the topologies of Figs. 3.37(d)and (f) to form a full-wave rectifier. Depicted in Fig. 3.38(a), the resulting circuit passes the negative half cycles through D_1 and D_2 with a sign reversal [as in Fig. 3.37(d)] and the positive half cycles through D_3 and D_4 with no sign reversal [as in Fig. 3.37(f)]. This configuration is usually drawn as in Fig. 3.38(b)and called a "bridge rectifier."

Let us summarize our thoughts with the aid of the circuit shown in Fig. 3.38(b). If $V_{in} < 0$, D_2 and D_1 are on and D_3 and D_4 are off, reducing the circuit to that shown in Fig. 3.38(c) and yielding $V_{out} = -V_{in}$. On the other hand, if $V_{in} > 0$, the bridge is simplified as shown in Fig. 3.38(d), and $V_{out} = V_{in}$.

How do these results change if the diodes are not ideal? Figures 3.38(c) and (d) reveal that the circuit introduces *two* forward-biased diodes in series with R_L, yielding $V_{out} = -V_{in} - 2V_{D,on}$ for $V_{in} < 0$. By contrast, the half-wave rectifier in Fig. 3.28produces $V_{out} = V_{in} - V_{D,on}$. The drop of $2V_{D,on}$ may pose difficulty if V_p is relatively small and the output voltage must be close to V_p.

Example 3.29 Assuming a constant-voltage model for the diodes, plot the input/output characteristic of a full-wave rectifier.

Solution The output remains equal to zero for $|V_{in}| < 2V_{D,on}$ and "tracks" the input for $|V_{in}| > V_{D,on}$ with a slope of unity. Figure 3.39 plots the result.

Exercise What is the slope of the characteristic for $|V_{in}| > 2V_{D,on}$?

We now redraw the bridge once more and add the smoothing capacitor to arrive at the complete design [Fig. 3.40(a)]. Since the capacitor discharge occurs for about half of

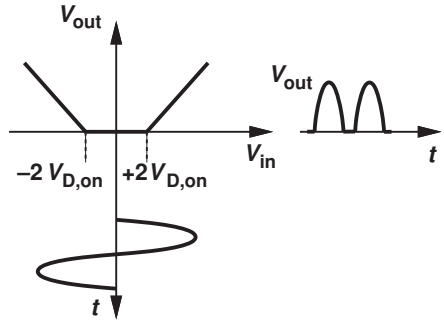


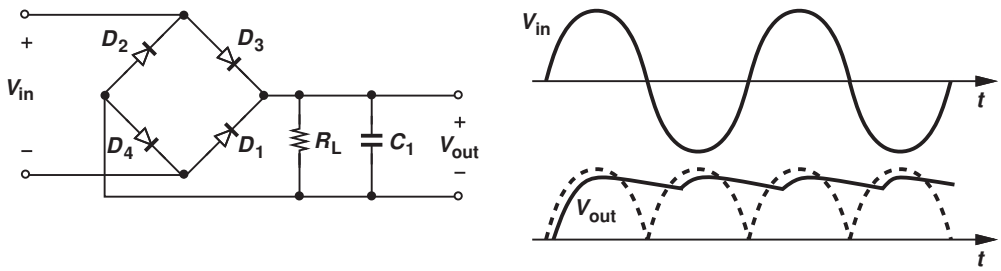
Figure 3.39 Input/output characteristic of full-wave rectifier with nonideal diodes.

the input cycle, the ripple is approximately equal to half of that in Eq. (3.80):

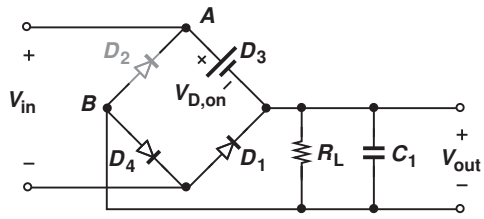
$$V_R \approx \frac{1}{2} \cdot \frac{V_p - 2V_{D,on}}{R_L C_1 f_{in}}, \tag{3.94}$$

where the numerator reflects the drop of $2V_{D,on}$ due to the bridge.

In addition to a lower ripple, the full-wave rectifier offers another important advantage: the maximum reverse bias voltage across each diode is approximately equal to V_p rather than $2V_p$. As illustrated in Fig. 3.40(b), when V_{in} is near V_p and D_3 is on, the voltage across D_2, V_{AB}, is simply equal to $V_{D,on} + V_{out} = V_p - V_{D,on}$. A similar argument applies to the other diodes.



(a)



(b)

Figure 3.40 (a) Ripple in full-wave rectifier, (b) equivalent circuit.

Another point of contrast between half-wave and full-wave rectifiers is that the former has a common terminal between the input and output ports (node G in Fig. 3.28),whereas the latter does not. In Problem 3.40, we study the effect of shorting the input and output grounds of a full-wave rectifier and conclude that it disrupts the operation of the circuit.

Example 3.30 Plot the currents carried by each diode in a bridge rectifier as a function of time for a sinusoidal input. Assume no smoothing capacitor is connected to the output.

Solution From Figs. 3.38(c) and (d), we have $V_{out} = -V_{in} + 2V_{D,on}$ for $V_{in} < -2V_{D,on}$ and $V_{out} = V_{in} - 2V_{D,on}$ for $V_{in} > +2V_{D,on}$. In each half cycle, two of the diodes carry a current equal to V_{out}/R_L and the other two remain off. Thus, the diode currents appear as shown in Fig. 3.41.

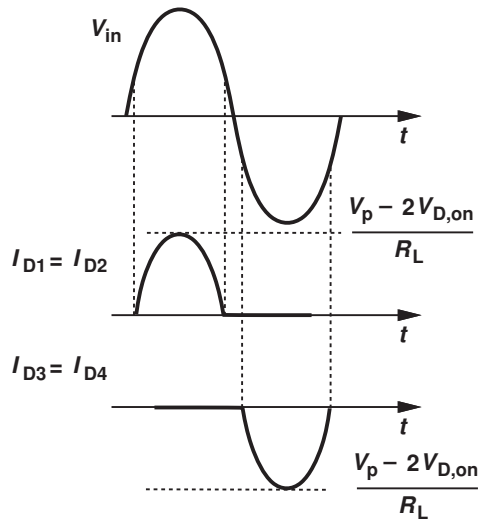


Figure 3.41 Currents carried by diodes in a full-wave rectifier.

Exercise Sketch the power consumed in each diode as a function of time.

The results of our study are summarized in Fig. 3.42. While using two more diodes, full-wave rectifiers exhibit a lower ripple and require only half the diode breakdown voltage, well justifying their use in adaptors and chargers.[15]

[15]The four diodes are typically manufactured in a single package having four terminals.

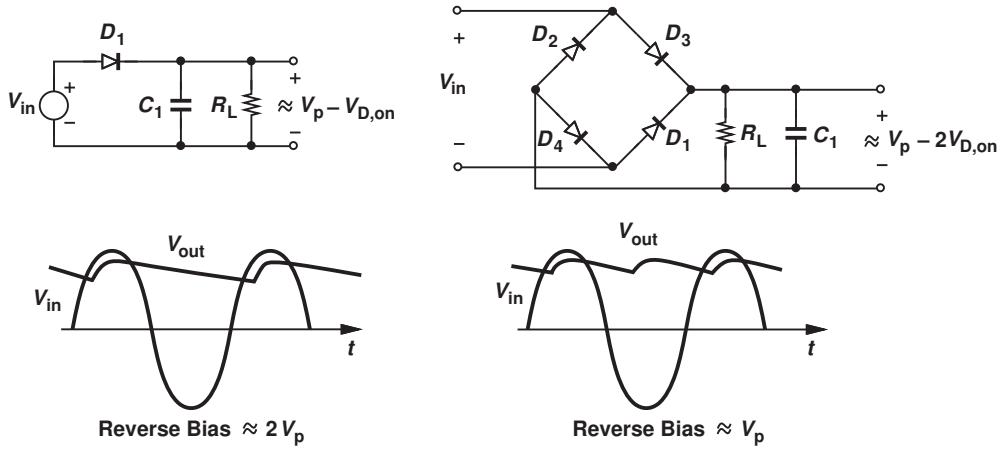


Figure 3.42 Summary of rectifier circuits.

Example 3.31 Design a full-wave rectifier to deliver an average power of 2 W to a cellphone with a voltage of 3.6 V and a ripple of 0.2 V.

Solution We begin with the required input swing. Since the output voltage is approximately equal to $V_p - 2V_{D,on}$, we have

$$V_{in,p} = 3.6\,\text{V} + 2V_{D,on} \tag{3.95}$$

$$\approx 5.2\,\text{V}. \tag{3.96}$$

Thus, the transformer preceding the rectifier must step the line voltage ($110\,\text{V}_{rms}$ or $220\,\text{V}_{rms}$) down to a peak value of 5.2 V.

Next, we determine the minimum value of the smoothing capacitor that ensures $V_R \leq 0.2\,\text{V}$. Rewriting Eq. (3.83) for a full-wave rectifier gives

$$V_R = \frac{I_L}{2C_1 f_{in}} \tag{3.97}$$

$$= \frac{2\,\text{W}}{3.6\,\text{V}} \cdot \frac{1}{2C_1 f_{in}}. \tag{3.98}$$

For $V_R = 0.2\,\text{V}$ and $f_{in} = 60\,\text{Hz}$,

$$C_1 = 23{,}000\,\mu\text{F}. \tag{3.99}$$

The diodes must withstand a reverse bias voltage of 5.2 V.

Exercise If cost and size limitations impose a maximum value of 1000 μF on the smoothing capacitor, what is the maximum allowable power drain in the above example?

Example 3.32 A radio frequency signal received and amplified by a cellphone exhibits a peak swing of 10 mV. We wish to generate a dc voltage representing the signal amplitude [Eq. (3.8)]. Is it possible to use the half-wave or full-wave rectifiers studied above?

Solution No, it is not. Owing to its small amplitude, the signal cannot turn actual diodes on and off, resulting in a zero output. For such signal levels, "precision rectification" is necessary, a subject studied in Chapter 8.

Exercise What if a constant voltage of 0.8 V is added to the desired signal?

3.5.2 Voltage Regulation*

The adaptor circuit studied above generally proves inadequate. Due to the significant variation of the line voltage, the peak amplitude produced by the transformer and hence the dc output vary considerably, possibly exceeding the maximum level that can be tolerated by the load (e.g., a cellphone). Furthermore, the ripple may become seriously objectionable in many applications. For example, if the adaptor supplies power to a stereo, the 120-Hz ripple can be heard from the speakers. Moreover, the finite output impedance of the transformer leads to changes in V_{out} if the current drawn by the load varies. For these reasons, the circuit of Fig. 3.40(a) is often followed by a "voltage regulator" so as to provide a constant output.

We have already encountered a voltage regulator without calling it such: the circuit studied in Example 3.17 provides a voltage of 2.4 V, incurring only an 11-mV change in the output for a 100-mV variation in the input. We may therefore arrive at the circuit shown in Fig. 3.43 as a more versatile adaptor having a nominal output of $3V_{D,on} \approx 2.4$ V. Unfortunately, as studied in Example 3.22, the output voltage varies with the load current.

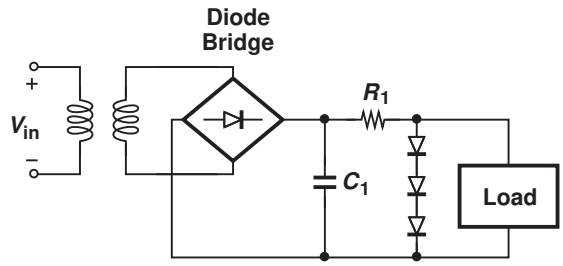


Figure 3.43 Voltage regulator block diagram.

*This section can be skipped in a first reading.

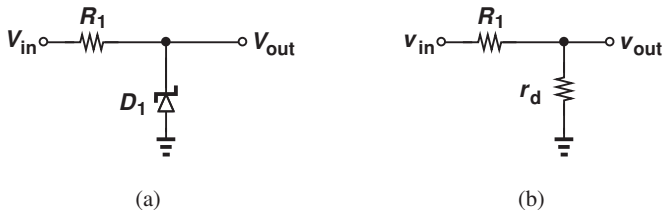


Figure 3.44 (a) Regulator using a Zener diode, (b) small-signal equivalent of (a).

Did you know?

The diodes used in power supplies may not seem to have a large carbon footprint, but if we add up the power consumption of all of the diodes in the world, we see a frightening picture.

As an example, consider Google's server farms. It is estimated that Google has about half a million servers. If one server draws 200 W from a 12-V supply, then each rectifier diode carries an average current of 200 W/12 V/2 ≈ 8.5 A. (We assume two diodes alternately turn on, each carrying half of the server's average current.) With a forward bias of about 0.7 V, two diodes consume 12 W, suggesting that the rectifier diodes in Google's servers dissipate a total power of roughly 6 MW. This is equivalent to the power generated by about 10 nuclear power plants! Indeed, a great deal of effort is presently expended on "green electronics," trying to reduce the power consumption of every circuit, including the power supply itself. (Our example is actually quite pessimistic as computers use "switching" power supplies to improve the efficiency.)

Figure 3.44(a) shows another regulator circuit employing a Zener diode. Operating in the reverse breakdown region, D_1 exhibits a small-signal resistance, r_D, in the range of 1 to 10 Ω, thus providing a relatively constant output despite input variations if $r_D \ll R_1$. This can be seen from the small-signal model of Fig. 3.44(b):

$$v_{out} = \frac{r_D}{r_D + R_1} v_{in} \tag{3.100}$$

For example, if $r_D = 5\,\Omega$ and $R_1 = 1\,\text{k}\Omega$, then changes in V_{in} are attenuated by approximately a factor of 200 as they appear in V_{out}. The Zener regulator nonetheless has the same drawback as the circuit of Fig. 3.43, namely, poor stability if the load current varies significantly.

Our brief study of regulators thus far reveals two important aspects of their design: the stability of the output with respect to input variations, and the stability of the output with respect to load current variations. The former is quantified by "line regulation," defined as $\Delta V_{out}/\Delta V_{in}$, and the latter by "load regulation," defined as $\Delta V_{out}/\Delta I_L$.

Example 3.33

In the circuit of Fig. 3.45(a), V_{in} has a nominal value of 5 V, $R_1 = 100\,\Omega$, and D_2 has a reverse breakdown of 2.7 V and a small-signal resistance of 5 Ω. Assuming $V_{D,on} \approx 0.8$ V for D_1, determine the line and load regulation of the circuit.

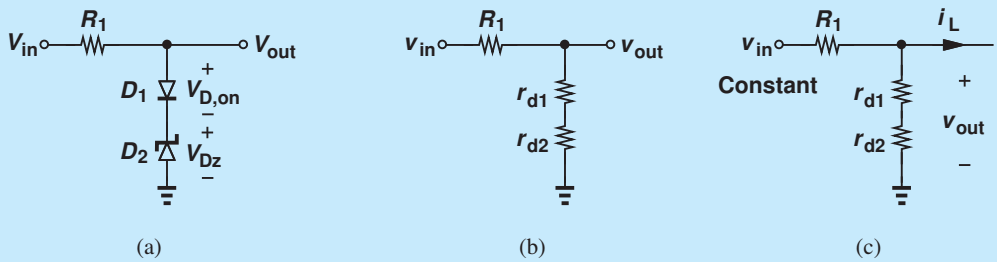


Figure 3.45 Circuit using two diodes, (b) small-signal equivalent, (c) load regulation.

Solution We first determine the bias current of D_1 and hence its small-signal resistance:

$$I_{D1} = \frac{V_{in} - V_{D,on} - V_{D2}}{R_1} \tag{3.101}$$

$$= 15\,\text{mA}. \tag{3.102}$$

Thus,

$$r_{D1} = \frac{V_T}{I_{D1}} \tag{3.103}$$

$$= 1.73\,\Omega. \tag{3.104}$$

From the small-signal model of Fig. 3.44(b), we compute the line regulation as

$$\frac{v_{out}}{v_{in}} = \frac{r_{D1} + r_{D2}}{r_{D1} + r_{D2} + R_1} \tag{3.105}$$

$$= 0.063. \tag{3.106}$$

For load regulation, we assume the input is constant and study the effect of load current variations. Using the small-signal circuit shown in Fig. 3.45(c) (where $v_{in} = 0$ to represent a constant input), we have

$$\frac{v_{out}}{(r_{D1} + r_{D2})||R_1} = -i_L. \tag{3.107}$$

That is,

$$\left|\frac{v_{out}}{i_L}\right| = (r_{D1} + r_{D2})||R_1 \tag{3.108}$$

$$= 6.31\,\Omega. \tag{3.109}$$

This value indicates that a 1-mA change in the load current results in a 6.31-mV change in the output voltage.

Exercise Repeat the above example for $R_1 = 50\,\Omega$ and compare the results.

Figure 3.46 summarizes the results of our study in this section.

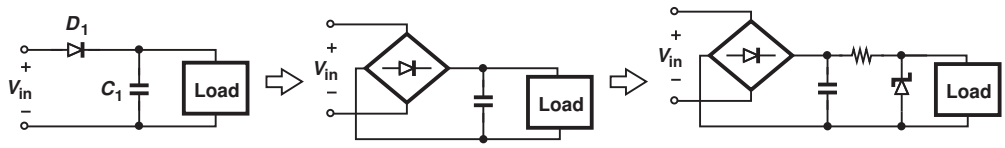


Figure 3.46 Summary of regulators.

3.5.3 Limiting Circuits

Consider the signal received by a cellphone as the user comes closer to a base station (Fig. 3.47). As the distance decreases from kilometers to hundreds of meters, the signal level may become large enough to "saturate" the circuits as it travels through the receiver chain. It is therefore desirable to "limit" the signal amplitude at a suitable point in the receiver.

Figure 3.47 Signals received (a) far from or (b) near a base station.

How should a limiting circuit behave? For small input levels, the circuit must simply pass the input to the output, e.g., $V_{out} = V_{in}$, and as the input level exceeds a "threshold" or "limit," the output must remain constant. This behavior must hold for both positive and negative inputs, translating to the input/output characteristic shown in Fig. 3.48(a). As illustrated in Fig. 3.48(b), a signal applied to the input emerges at the output with its peak values "clipped" at $\pm V_L$.

We now implement a circuit that exhibits the above behavior. The nonlinear input/output characteristic suggests that one or more diodes must turn on or off as V_{in} approaches $\pm V_L$. In fact, we have already seen simple examples in Figs. 3.11(b)and (c), where the positive half cycles of the input are clipped at 0 V and +1 V, respectively. We reexamine the former assuming a more realistic diode, e.g., the constant-voltage model. As illustrated in Fig. 3.49(a), V_{out} is equal to V_{in} for $V_{in} < V_{D,on}$ and equal to $V_{D,on}$ thereafter.

To serve as a more general limiting circuit, the above topology must satisfy two other conditions. First, the limiting level, V_L, must be an arbitrary voltage and not necessarily equal to $V_{D,on}$. Inspired by the circuit of Fig. 3.11 (c), we postulate that a constant voltage source in series with D_1 shifts the limiting point, accomplishing this objective. Depicted in Fig. 3.49(b), the resulting circuit limits at $V_L = V_{B1} + V_{D,on}$. Note that V_{B1} can be positive or negative to shift V_L to higher or lower values, respectively.

Second, the negative values of V_{in} must also experience limiting. Beginning with the circuit of Fig. 3.49(a), we recognize that if the anode and cathode of D_1 are swapped, then the circuit limits at $V_{in} = -V_{D,on}$ [Fig. 3.50(a)]. Thus, as shown in Fig. 3.50(b), two "antiparallel" diodes can create a characteristic that limits at $\pm V_{D,on}$. Finally, inserting constant voltage sources in series with the diodes shifts the limiting points to arbitrary levels (Fig. 3.51).

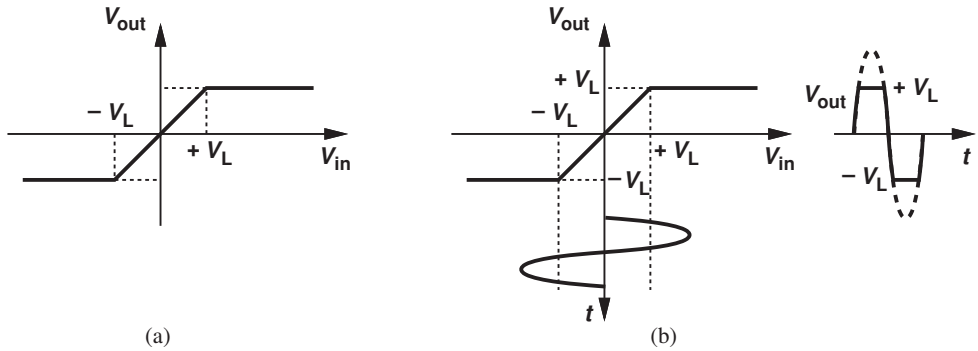


Figure 3.48 (a) Input/output characteristic of a limiting circuit, (b) response to a sinusoid.

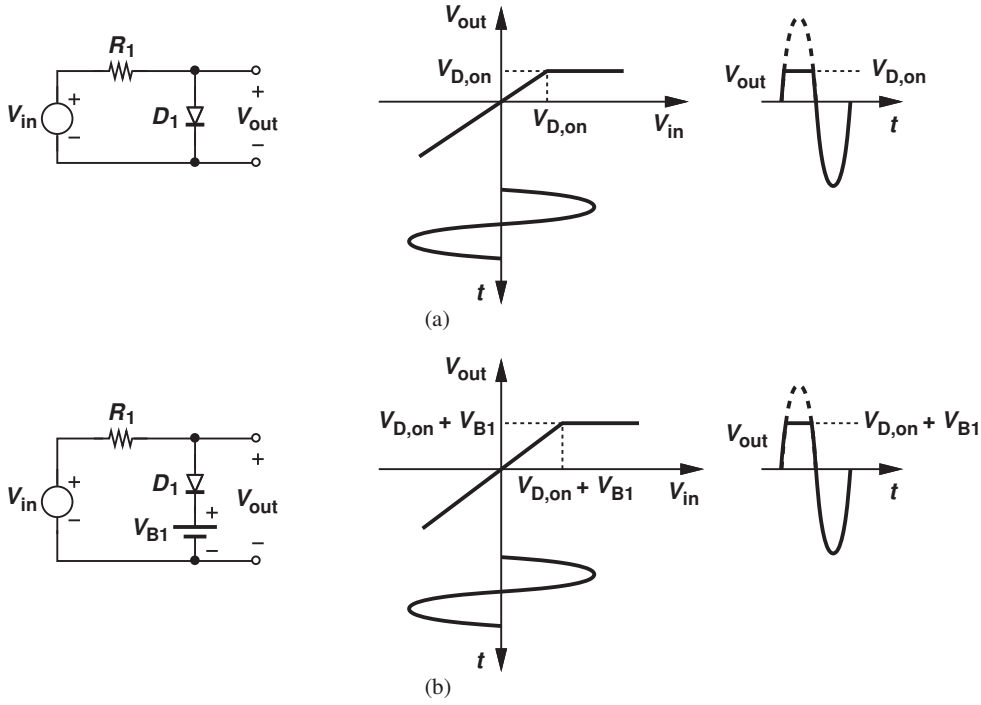


Figure 3.49 (a) Simple limiter, (b) limiter with level shift.

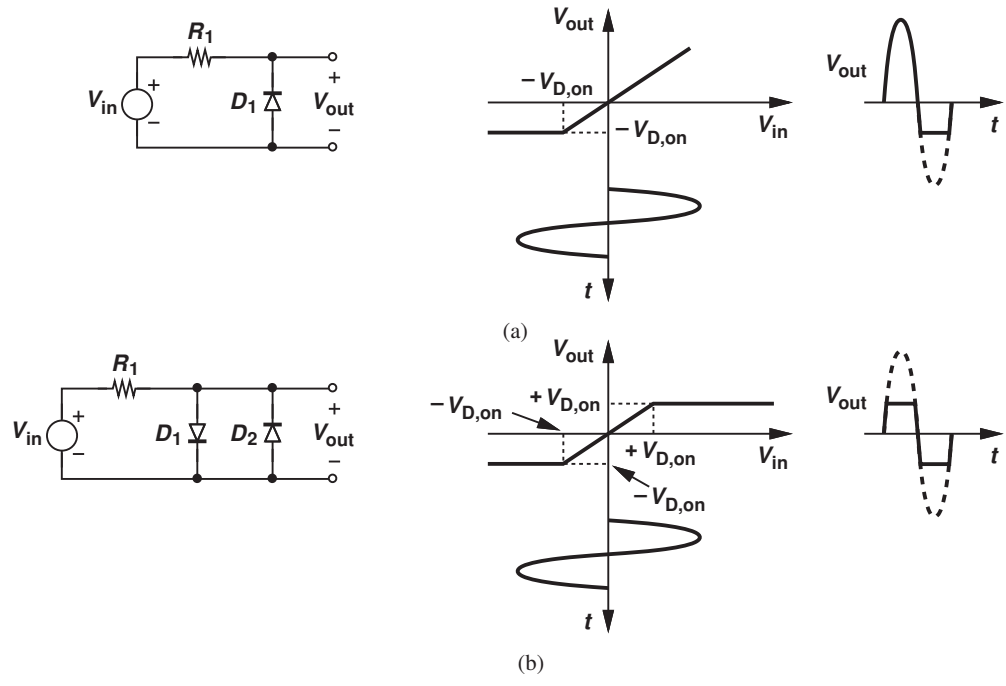


Figure 3.50 (a) Negative-cycle limiter, (b) limiter for both half cycles.

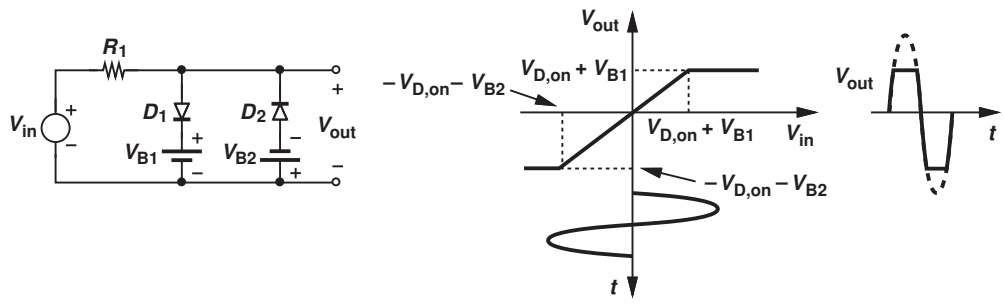


Figure 3.51 General limiter and its characteristic.

Example 3.34

A signal must be limited at ±100 mV. Assuming $V_{D,on} = 800$ mV, design the required limiting circuit.

Solution

Figure 3.52(a) illustrates how the voltage sources must shift the break points. Since the positive limiting point must shift to the left, the voltage source in series with D_1 must be *negative* and equal to 700 mV. Similarly, the source in series with D_2 must be positive and equal to 700 mV. Figure 3.52(b) shows the result.

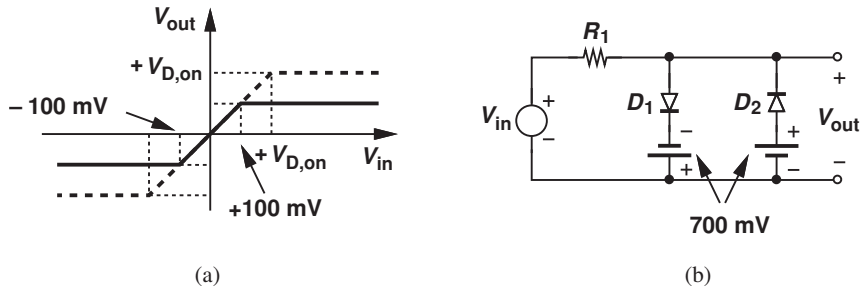


Figure 3.52 (a) Example of a limiting circuit, (b) input/output characteristic.

Exercise

Repeat the above example if the positive values of the signal must be limited at +200 mV and the negative values at −1.1 V.

Before concluding this section, we make two observations. First, the circuits studied above actually display a nonzero slope in the limiting region (Fig. 3.53). This is because, as V_{in} increases, so does the current through the diode that is forward biased and hence the diode voltage.[16] Nonetheless, the 60-mV/decade rule expressed by Eq. (2.109) implies that this effect is typically negligible. Second, we have thus far assumed $V_{out} = V_{in}$ for $-V_L < V_{in} < +V_L$, but it is possible to realize a non-unity slope in the region: $V_{out} = \alpha V_{in}$.

[16]Recall that $V_D = V_T \ln(I_D/I_S)$.

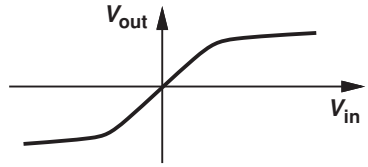


Figure 3.53 Effect of nonideal diodes on limiting characteristic.

3.5.4 Voltage Doublers*

Electronic systems typically employ a "global" supply voltage, e.g., 3 V, requiring that the discrete and integrated circuits operate with such a value. However, the design of some circuits in the system is greatly simplified if they run from a *higher* supply voltage, e.g., 6 V. "Voltage doublers" may serve this purpose.[17]

Before studying doublers, it is helpful to review some basic properties of capacitors. First, to charge one plate of a capacitor to $+Q$, the other plate *must* be charged to $-Q$. Thus, in the circuit of Fig. 3.54(a), the voltage across C_1 *cannot* change even if V_{in} changes because the right plate of C_1 cannot receive or release charge ($Q = CV$). Since V_{C1} remains constant, an input change ΔV_{in} appears directly at the output. This is an important observation.

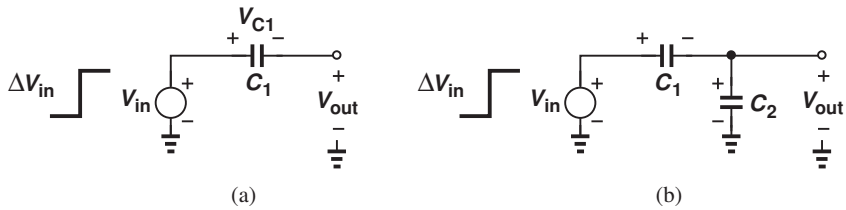


Figure 3.54 (a) Voltage change at one plate of a capacitor, (b) voltage division.

Second, a capacitive voltage divider such as that in Fig. 3.54(b) operates as follows. If V_{in} becomes more positive, the left plate of C_1 receives positive charge from V_{in}, thus requiring that the right plate absorb negative charge of the same magnitude from the top plate of C_2. Having lost negative charge, the top plate of C_2 equivalently holds more positive charge, and hence the bottom plate absorbs negative charge from ground. Note that all four plates receive or release equal amounts of charge because C_1 and C_2 are in series. To determine the change in V_{out}, ΔV_{out}, resulting from ΔV_{in}, we write the change in the charge on C_2 as $\Delta Q_2 = C_2 \cdot \Delta V_{out}$, which also holds for C_1: $\Delta Q_2 = \Delta Q_1$. Thus, the voltage change across C_1 is equal to $C_2 \cdot \Delta V_{out}/C_1$. Adding these two voltage changes and equating the result to ΔV_{in}, we have

$$\Delta V_{in} = \frac{C_2}{C_1}\Delta V_{out} + \Delta V_{out}. \tag{3.110}$$

*This section can be skipped in a first reading.

[17]Voltage doublers are an example of "dc-dc converters."

That is,

$$\Delta V_{out} = \frac{C_1}{C_1 + C_2} \Delta V_{in}. \tag{3.111}$$

This result is similar to the voltage division expression for resistive dividers, except that C_1 (rather than C_2) appears in the numerator. Interestingly, the circuit of Fig. 3.54(a) is a special case of the capacitive divider with $C_2 = 0$ and hence $\Delta V_{out} = \Delta V_{in}$.

As our first step toward realizing a voltage doubler, recall the result illustrated in Fig. 3.31: the voltage across the diode in the peak detector exhibits an average value of $-V_p$ and, more importantly, a peak value of $-2V_p$ (with respect to zero). For further investigation, we redraw the circuit as shown in Fig. 3.55, where the diode and the capacitors are exchanged and the voltage across D_1 is labeled V_{out}. While V_{out} in this circuit behaves exactly the same as V_{D1} in Fig. 3.30(a), we derive the output waveform from a different perspective so as to gain more insight.

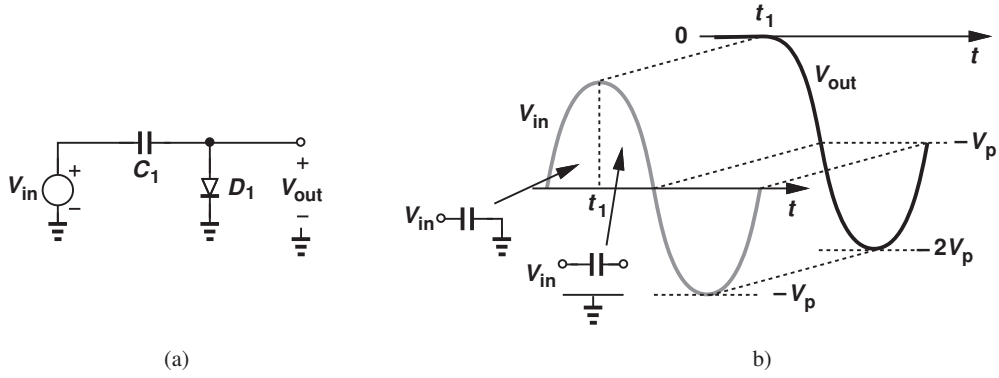


Figure 3.55 (a) Capacitor-diode circuit and (b) its waveforms.

Assuming an ideal diode and a zero initial condition across C_1, we note that as V_{in} exceeds zero, the input tends to place positive charge on the left plate of C_1 and hence draw negative charge from D_1. Consequently, D_1 turns on, forcing $V_{out} = 0$.[18] As the input rises toward V_p, the voltage across C_1 remains equal to V_{in} because its right plate is "pinned" at zero by D_1. After $t = t_1$, V_{in} begins to fall and tends to discharge C_1, i.e., draw positive charge from the left plate and hence from D_1. The diode therefore turns off, reducing the circuit to that in Fig. 3.54(a). From this time, the output simply tracks the changes in the input while C_1 sustains a constant voltage equal to V_p. In particular, as V_{in} varies from $+V_p$ to $-V_p$, the output goes from zero to $-2V_p$, and the cycle repeats indefinitely. The output waveform is thus identical to that obtained in Fig. 3.31(b).

[18] If we assume D_1 does *not* turn on, then the circuit resembles that in Fig. 3.54(a), requiring that V_{out} rise and D_1 turn on.

Example 3.35

Plot the output waveform of the circuit shown in Fig. 3.56 if the initial condition across C_1 is zero.

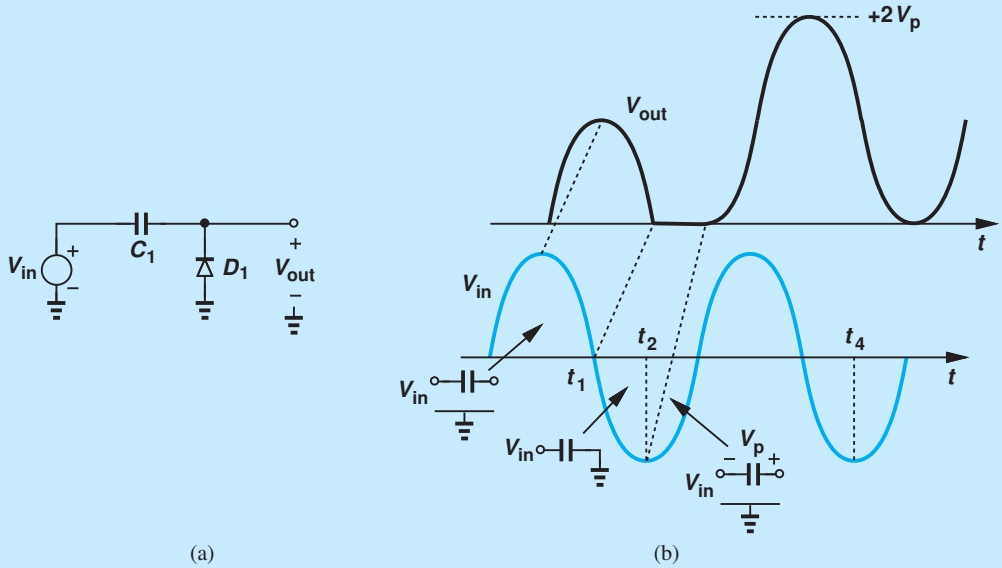


Figure 3.56 Capacitor-diode circuit and (b) its waveforms.

Solution

As V_{in} rises from zero, attempting to place positive charge on the left plate of C_1 and hence draw negative charge from D_1, the diode turns off. As a result, C_1 directly transfers the input change to the output for the entire positive half cycle. After $t = t_1$, the input tends to push negative charge into C_1, turning D_1 on and forcing $V_{out} = 0$. Thus, the voltage across C_1 remains equal to V_{in} until $t = t_2$, at which point the direction of the current through C_1 and D_1 must change, turning D_1 off. Now, C_1 carries a voltage equal to V_p and transfers the input change to the output; i.e., the output tracks the input but with a level shift of $+V_p$, reaching a peak value of $+2V_p$.

Exercise

Repeat the above example if the right plate of C_1 is 1 V more positive than its left plate at $t = 0$.

We have thus far developed circuits that generate a periodic output with a peak value of $-2V_p$ or $+2V_p$ for an input sinusoid varying between $-V_p$ and $+V_p$. We surmise that if these circuits are followed by a *peak detector* [e.g., Fig. 3.30(a)], then a constant output equal to $-2V_p$ or $+2V_p$ may be produced. Figure 3.57 exemplifies this concept, combining the circuit of Fig. 3.56 with the peak detector of Fig. 3.30(a). Of course, since the peak detector "loads" the first stage when D_2 turns on, we must still analyze this circuit carefully and determine whether it indeed operates as a voltage doubler.

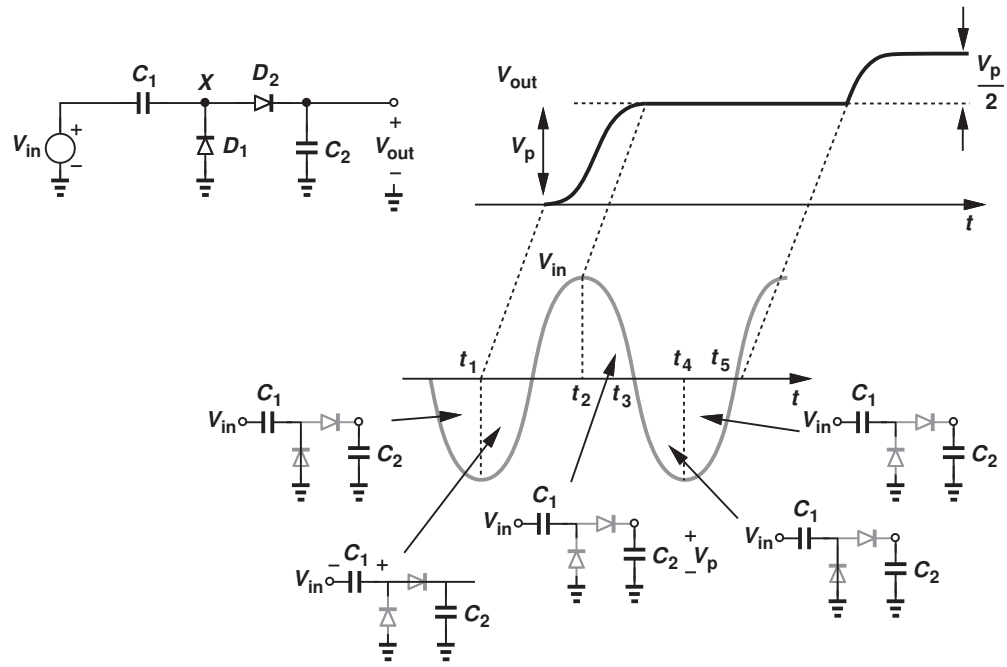


Figure 3.57 Voltage doubler circuit and its waveforms.

We assume ideal diodes, zero initial conditions across C_1 and C_2, and $C_1 = C_2$. In this case, the analysis is simplified if we begin with a negative cycle. As V_{in} falls below zero, D_1 turns on, pinning node X to zero.[19] Thus, for $t < t_1$, D_2 remains off and $V_{out} = 0$. At $t = t_1$, the voltage across C_1 reaches $-V_p$. For $t > t_1$, the input begins to rise and tends to deposit positive charge on the left plate of C_1, turning D_1 off and yielding the circuit shown in Fig. 3.57.

How does D_2 behave in this regime? Since V_{in} is now rising, we postulate that V_X also tends to increase (from zero), turning D_2 on. (If D_2 remains off, then C_1 simply transfers the change in V_{in} to node X, raising V_X and hence turning D_2 on.) As a result, the circuit reduces to a simple capacitive divider that follows Eq. (3.111):

$$\Delta V_{out} = \frac{1}{2}\Delta V_{in}, \tag{3.112}$$

because $C_1 = C_2$. In other words, V_X and V_{out} begin from zero, remain equal, and vary sinusoidally but with an amplitude equal to $V_p/2$. Thus, from t_1 to t_2, a change of $2V_p$ in V_{in} appears as a change equal to V_p in V_X and V_{out}. Note at $t = t_2$, the voltage across C_1 is zero because both V_{in} and V_{out} are equal to $+V_p$.

What happens after $t = t_2$? Since V_{in} begins to fall and tends to draw charge from C_1, D_2 turns off, maintaining V_{out} at $+V_p$. The reader may wonder if something is wrong here;

[19] As always, the reader is encouraged to assume otherwise (i.e., D_1 remains off) and arrive at a conflicting result.

our objective was to generate an output equal to $2V_p$ rather than V_p. But again, patience is a virtue and we must continue the transient analysis. For $t > t_2$, both D_1 and D_2 are off, and each capacitor holds a constant voltage. Since the voltage across C_1 is zero, $V_X = V_{in}$, falling to zero at $t = t_3$. At this point, D_1 turns on again, allowing C_1 to charge to $-V_p$ at $t = t_4$. As V_{in} begins to rise again, D_1 turns off and D_2 remains off because $V_X = 0$ and $V_{out} = +V_p$. Now, with the right plate of C_1 floating, V_X tracks the change at the input, reaching $+V_p$ as V_{in} goes from $-V_p$ to 0. Thus, D_2 turns on at $t = t_5$, forming a capacitive divider again. After this time, the output change is equal to half of the input change, i.e., V_{out} increases from $+V_p$ to $+V_p + V_p/2$ as V_{in} goes from 0 to $+V_p$. The output has now reached $3V_p/2$.

Did you know?

Doublers are often used to generate larger dc voltages than the system's power supply can provide. For example, a "photomultiplier" requires a supply voltage of 1000 to 2000 V to accelerate electrons and, through a process called "secondary emission," amplify the number of photons. In this case, we begin with a line voltage of 110 V or 220 V and employ a cascade of voltage doublers to reach the necessary value. Photomultipliers find application in many fields, including astronomy, high-energy physics, and medicine. For example, blood cells are counted under low light level conditions with the aid of photomultipliers.

As is evident from the foregoing analysis, the output continues to rise by V_p, $V_p/2$, $V_p/4$, etc., in each input cycle, approaching a final value of

$$V_{out} = V_p\left(1 + \frac{1}{2} + \frac{1}{4} + \cdots\right) \tag{3.113}$$

$$= \frac{V_p}{1 - \frac{1}{2}} \tag{3.114}$$

$$= 2V_p. \tag{3.115}$$

The reader is encouraged to continue the analysis for a few more cycles and verify this trend.

Example 3.36 Sketch the current through D_1 in the doubler circuit as function of time.

Solution Using the diagram in Fig. 3.58(a), noting that D_1 and C_1 carry equal currents when D_1 is forward biased, and writing the current as $I_{D1} = -C_1 dV_{in}/dt$, we construct the plot shown in Fig. 3.58(b).[20] For $0 < t < t_1$, D_1 conducts and the peak current corresponds to the maximum slope of V_{in}, i.e., immediately after $t = 0$. From $t = t_1$ to $t = t_3$, the diode remains off, repeating the same behavior in subsequent cycles.

Exercise Plot the current through D_2 in the above example as a function of time.

[20] As usual, I_{D1} denotes the current flowing from the anode to the cathode.

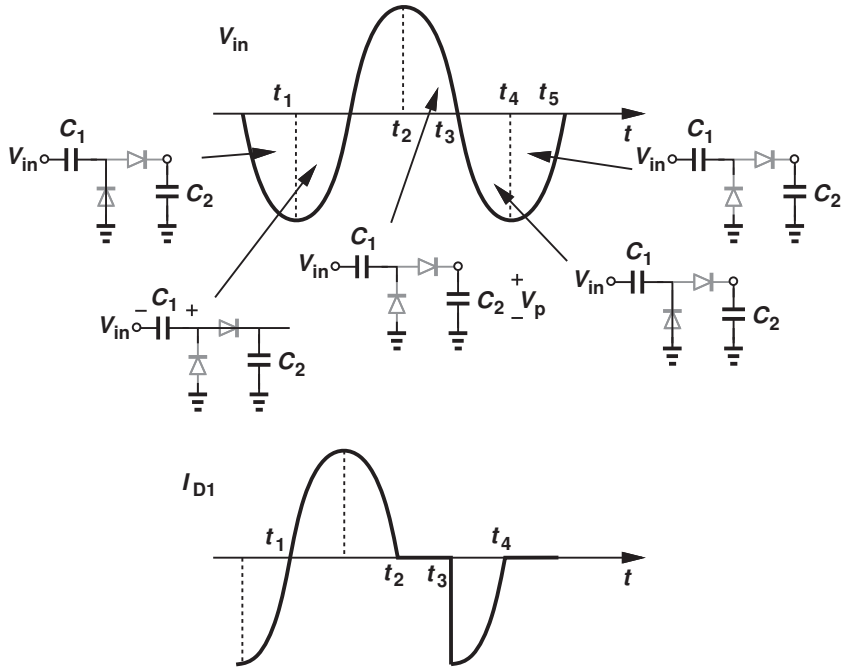


Figure 3.58 Diode current in a voltage doubler.

3.5.5 Diodes as Level Shifters and Switches*

In the design of electronic circuits, we may need to shift the average level of a signal up or down because the subsequent stage (e.g., an amplifier) may not operate properly with the present dc level.

Sustaining a relatively constant voltage in forward bias, a diode can be viewed as a battery and hence a device capable of shifting the signal level. In our first attempt, we consider the circuit shown in Fig. 3.59(a) as a candidate for shifting the level *down* by $V_{D,on}$. However, the diode current remains unknown and dependent on the next stage. To alleviate this issue we modify the circuit as depicted in Fig. 3.59(b), where I_1 draws a constant current, establishing $V_{D,on}$ across D_1.[21] If the current pulled by the next stage is negligible (or at least constant), V_{out} is simply lower than V_{in} by a constant amount, $V_{D,on}$.

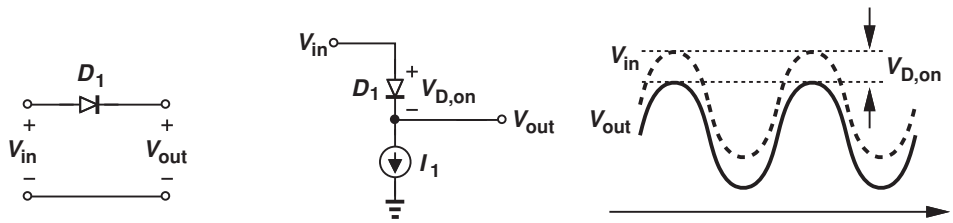


Figure 3.59 (a) Use of a diode for level shift, (b) practical implementation.

*This section can be skipped in a first reading.

[21]The diode is drawn vertically to emphasize that V_{out} is lower than V_{in}.

Example 3.37 Design a circuit that shifts up the dc level of a signal by $2V_{D,on}$.

Solution To shift the level *up*, we apply the input to the *cathode*. Also, to obtain a shift of $2V_{D,on}$, we place two diodes in series. Figure 3.60 shows the result.

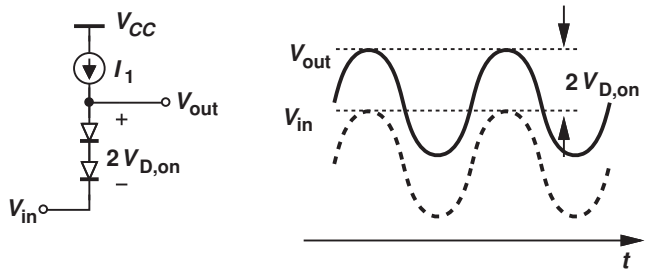


Figure 3.60 Positive voltage shift by two diodes.

Exercise What happens if I_1 is extremely small?

The level shift circuit of Fig. 3.59(b) can be transformed to an electronic switch. For example, many applications employ the topology shown in Fig. 3.61(a) to "sample" V_{in} across C_1 and "freeze" the value when S_1 turns off. Let us replace S_1 with the level shift circuit and allow I_1 to be turned on and off [Fig. 3.61(b)]. If I_1 is on, V_{out} tracks V_{in} except for a level shift equal to $V_{D,on}$. When I_1 turns off, so does D_1, evidently disconnecting C_1 from the input and freezing the voltage across C_1.

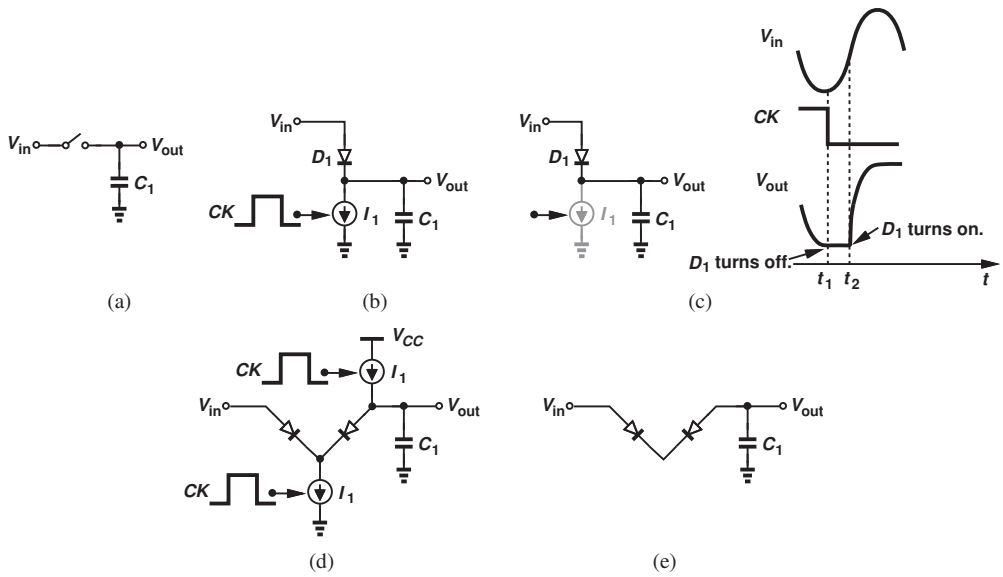


Figure 3.61 (a) Switched-capacitor circuit, (b) realization of (a) using a diode as a switch, (c) problem of diode conduction, (d) more complete circuit, (e) equivalent circuit when I_1 and I_2 are off.

We used the term "evidently" in the last sentence because the circuit's true behavior somewhat differs from the above description. The assumption that D_1 turns off holds only if C_1 draws no current from D_1, i.e., only if $V_{in} - V_{out}$ remains less than $V_{D,on}$. Now consider the case illustrated in Fig. 3.61(c), where I_1 turns off at $t = t_1$, allowing C_1 to store a value equal to $V_{in1} - V_{D,on}$. As the input waveform completes a negative excursion and exceeds V_{in1} at $t = t_2$, the diode is forward-biased again, charging C_1 with the input (in a manner similar to a peak detector). That is, even though I_1 is off, D_1 turns on for part of the cycle.

To resolve this issue, the circuit is modified as shown in Fig. 3.61(d), where D_2 is inserted between D_1 and C_1, and I_2 provides a bias current for D_2. With both I_1 and I_2 on, the diodes operate in forward bias, $V_X = V_{in} - V_{D1}$, and $V_{out} = V_X + V_{D2} = V_{in}$ if $V_{D1} = V_{D2}$. Thus, V_{out} tracks V_{in} with no level shift. When I_1 and I_2 turn off, the circuit reduces to that in Fig. 3.61(e), where the back-to-back diodes fail to conduct for any value of $V_{in} - V_{out}$, thereby isolating C_1 from the input. In other words, the two diodes and the two current sources form an electronic switch.

Example 3.38

Recall from Chapter 2 that diodes exhibit a junction capacitance in reverse bias. Study the effect of this capacitance on the operation of the above circuit.

Solution

Figure 3.62 shows the equivalent circuit for the case where the diodes are off, suggesting that the conduction of the input through the junction capacitances disturbs the output. Specifically, invoking the capacitive divider of Fig. 3.54(b) and assuming

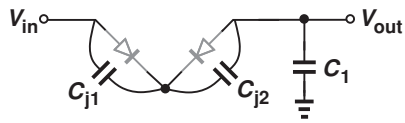


Figure 3.62 Feedthrough in the diode switch.

$C_{j1} = C_{j2} = C_j$, we have

$$\Delta V_{out} = \frac{C_j/2}{C_j/2 + C_1} \Delta V_{in}. \tag{3.116}$$

To ensure this "feedthrough" is small, C_1 must be sufficiently large.

Exercise

Calculate the change in the voltage at the left plate of C_{j1} (with respect to ground) in terms of ΔV_{in}.

3.6 CHAPTER SUMMARY

- In addition to the exponential and constant-voltage models, an "ideal" model is sometimes used to analyze diode circuits. The ideal model assumes the diode turns on with a very small forward bias voltage.
- For many electronic circuits, the "input/output characteristics" are studied to understand the response to various input levels, e.g., as the input level goes from $-\infty$ to $+\infty$.

- "Large-signal operation" occurs when a circuit or device experiences arbitrarily large voltage or current excursions. The exponential, constant-voltage, or ideal diode models are used in this case.
- If the *changes* in voltages and currents are sufficiently small, then nonlinear devices and circuits can be approximated by linear couterparts, greatly simplifying the analysis. This is called "small-signal operation."
- The small-signal model of a diode consists of an "incremental resistance" given by V_T/I_D.
- Diodes find application in many circuits, including rectifiers, limiting circuits, voltage doublers, and level shifters.
- Half-wave rectifiers pass the positive (negative) half cycles of the input waveform and block the negative (positive) half cycles. If followed by a capacitor, a rectifier can produce a dc level nearly equal to the peak of the input swing.
- A half-wave rectifier with a smoothing capacitor of value C_1 and load resistor R_L exhibits an output ripple equal to $(V_P - V_{D,on})/(R_L C_1 f_{in})$.
- Full-wave rectifiers convert both positive and negative input cycles to the same polarity at the output. If followed by a smoothing capacitor and a load resistor, these rectifiers exhibit an output ripple given by $0.5(V_P - 2V_{D,on})/(R_L C_1 f_{in})$.
- Diodes can operate as limiting devices, i.e., limit the output swing even if the input swing continues to increase.

PROBLEMS

In the following problems, assume $V_{D,on} = 800$ mV for the constant-voltage diode model.

Section 3.2 *pn* Junction as a Diode

3.1. Plot the I/V characteristic of the circuit shown in Fig. 3.63.

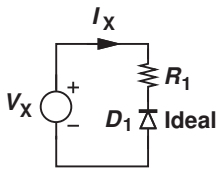


Figure 3.63

3.2. If the input in Fig. 3.63 is expressed as $V_X = V_0 \cos \omega t$, plot the current flowing through the circuit as a function of time.

3.3. Plot I_X as a function of V_X for the circuit shown in Fig. 3.65 for two cases: $V_B = -1$ V and $V_B = +1$ V.

3.4. For the circuit depicted in Fig. 3.64, plot I_X as a function of V_X for two cases: $V_B = -1$ V and $V_B = +1$ V.

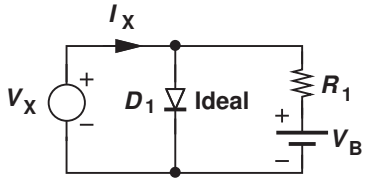


Figure 3.64

3.5. If in Fig. 3.65, $V_X = V_0 \cos \omega t$, plot I_X as a function of time for two cases: $V_B = -1$ V and $V_B = +1$ V.

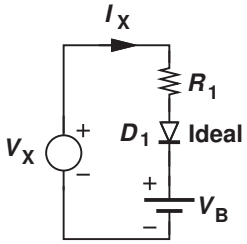


Figure 3.65

3.6. Plot I_X and I_{D1} as a function of V_X for the circuit shown in Fig. 3.66. Assume $V_B > 0$.

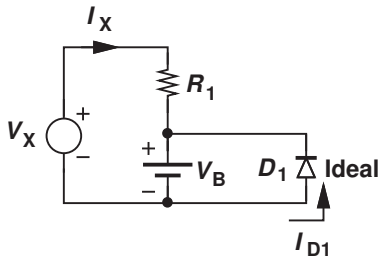


Figure 3.66

3.7. In the circuit of Fig. 3.67, plot I_X and I_{R1} as a function of V_X for two cases: $V_B = -1$ V and $V_B = +1$ V.

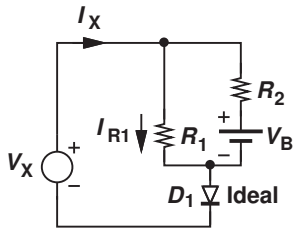


Figure 3.67

3.8. For the circuit depicted in Fig. 3.68, plot I_X and I_{R1} as a function of V_X for two cases: $V_B = -1$ V and $V_B = +1$ V.

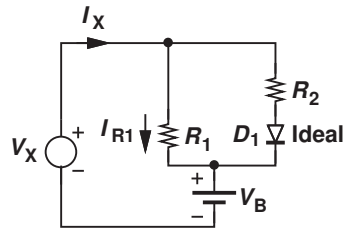


Figure 3.68

*__3.9.__ Plot the input/output characteristics of the circuits depicted in Fig. 3.69 using an ideal model for the diodes. Assume $V_B = 2$ V.

*__3.10.__ Repeat Problem 3.9 with a constant-voltage diode model.

*__3.11.__ If the input is given by $V_{in} = V_0 \cos \omega t$, plot the output of each circuit in Fig. 3.69 as a function of time. Assume an ideal diode model.

**__3.12.__ Plot the input/output characteristics of the circuits shown in Fig. 3.70 using an ideal model for the diodes.

**__3.13.__ Repeat Problem 3.12 with a constant-voltage diode model.

**__3.14.__ Assuming the input is expressed as $V_{in} = V_0 \cos \omega t$, plot the output of each circuit in Fig. 3.70 as a function of time. Use an ideal diode model.

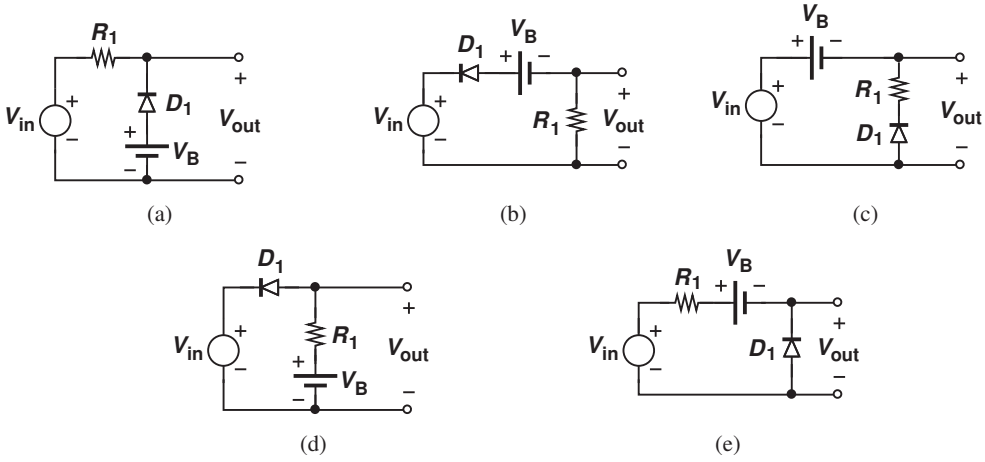


Figure 3.69

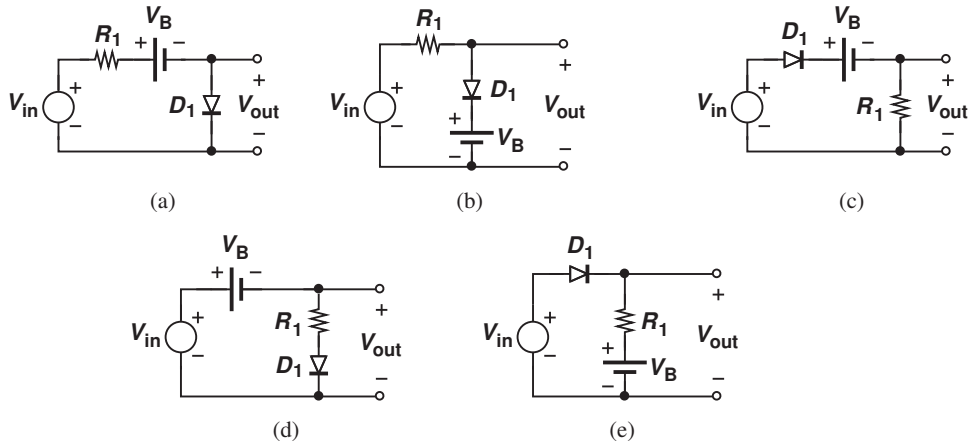


Figure 3.70

**3.15. Assuming a constant-voltage diode model, plot V_{out} as a function of I_{in} for the circuits shown in Fig. 3.71.

**3.16. In the circuits of Fig. 3.71, plot the current flowing through R_1 as a function of V_{in}. Assume a constant-voltage diode model.

**3.17. For the circuits illustrated in Fig. 3.71, plot V_{out} as a function of time if $I_{in} = I_0 \cos \omega t$. Assume a constant-voltage model and a relatively large I_0.

**3.18. Plot V_{out} as a function of I_{in} for the circuits shown in Fig. 3.72. Assume a constant-voltage diode model.

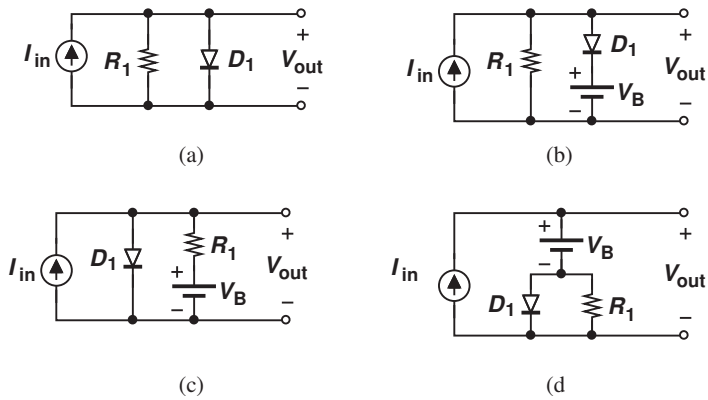


Figure 3.71

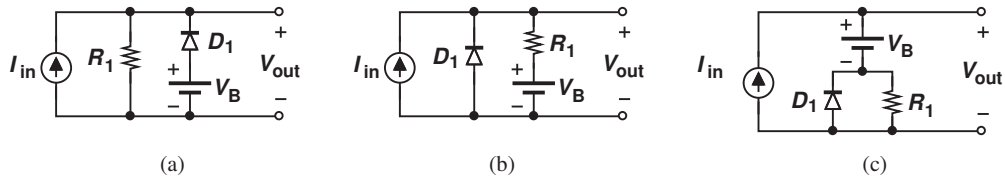


Figure 3.72

*3.19. Plot the current flowing through R_1 in the circuits of Fig. 3.72 as a function of I_{in}. Assume a constant-voltage diode model.

*3.20. In the circuits depicted in Fig. 3.72, assume $I_{in} = I_0 \cos \omega t$, where I_0 is relatively large. Plot V_{out} as a function of time using a constant-voltage diode model.

**3.21. For the circuits shown in Fig. 3.73, plot V_{out} as a function of I_{in} assuming a constant-voltage model for the diodes.

**3.22. Plot the current flowing through R_1 as a function of I_{in} for the circuits of Fig. 3.73. Assume a constant-voltage diode model.

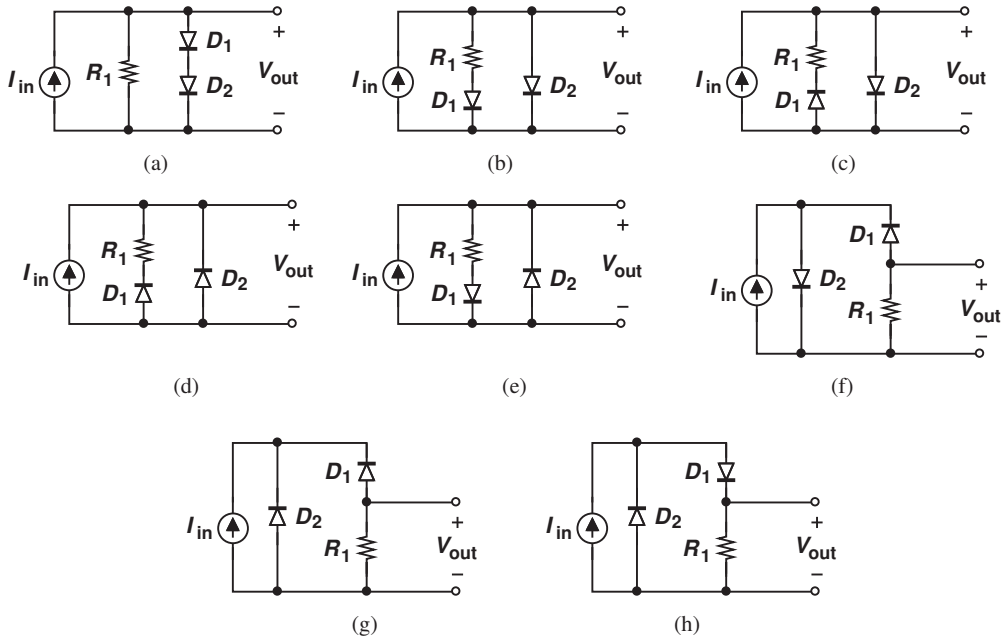


Figure 3.73

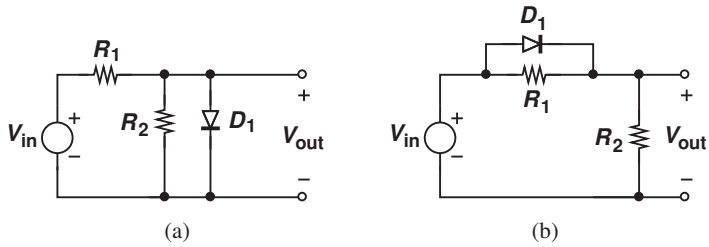


Figure 3.74

*3.23. Plot the input/output characteristic of the circuits illustrated in Fig. 3.74 assuming a constant-voltage model.

*3.24. Plot the currents flowing through R_1 and D_1 as a function of V_{in} for the circuits of Fig. 3.74. Assume a constant-voltage diode model.

**3.25. Plot the input/output characteristic of the circuits illustrated in Fig. 3.75 assuming a constant-voltage model.

**3.26. Plot the currents flowing through R_1 and D_1 as a function of V_{in} for the circuits of Fig. 3.75. Assume a constant-voltage diode model.

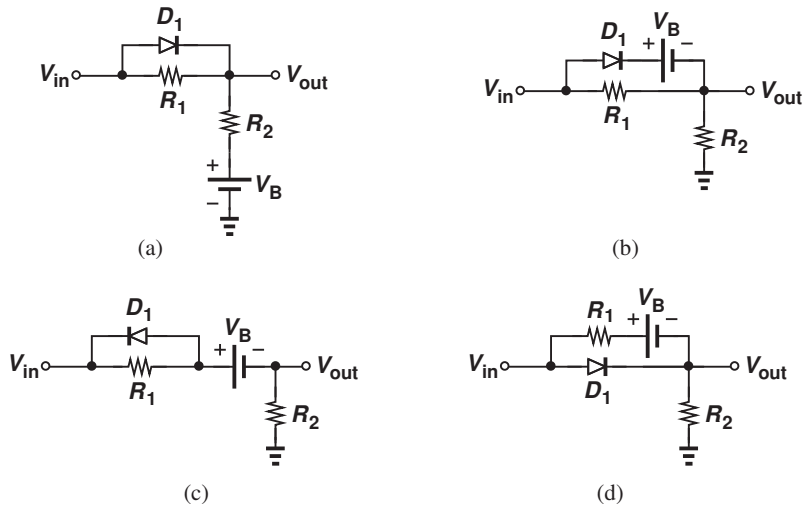


Figure 3.75

**3.27. Plot the input/output characteristic of the circuits illustrated in Fig. 3.76 assuming a constant-voltage model and $V_B = 2\,\text{V}$.

**3.28. Plot the currents flowing through R_1 and D_1 as a function of V_{in} for the circuits of Fig. 3.76. Assume a constant-voltage diode model and $V_B = 2\,\text{V}$.

**3.29. Plot the input/output characteristic of the circuits illustrated in Fig. 3.77 assuming a constant-voltage model.

**3.30. Plot the currents flowing through R_1 and D_1 as a function of V_{in} for the circuits of Fig. 3.77. Assume constant-voltage diode model.

*3.31. Beginning with $V_{D,on} \approx 800\,\text{mV}$ for each diode, determine the change in V_{out} if V_{in} changes from $+2.4\,\text{V}$ to $+2.5\,\text{V}$ for the circuits shown in Fig. 3.78.

*3.32. Beginning with $V_{D,on} \approx 800\,\text{mV}$ for each diode, calculate the change in V_{out} if I_{in} changes from 3 mA to 3.1 mA in the circuits of Fig. 3.79.

3.33. In Problem 3.32, determine the change in the current flowing through the 1-kΩ resistor in each circuit.

3.34. Assuming $V_{in} = V_p \sin \omega t$, plot the output waveform of the circuit depicted in Fig. 3.80 for an initial condition of $+0.5\,\text{V}$ across C_1. Assume $V_p = 5\,\text{V}$.

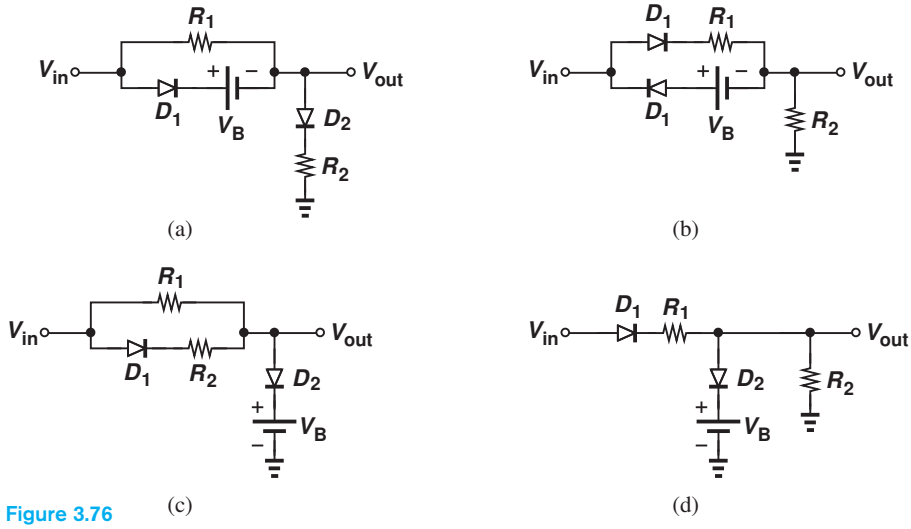


Figure 3.76

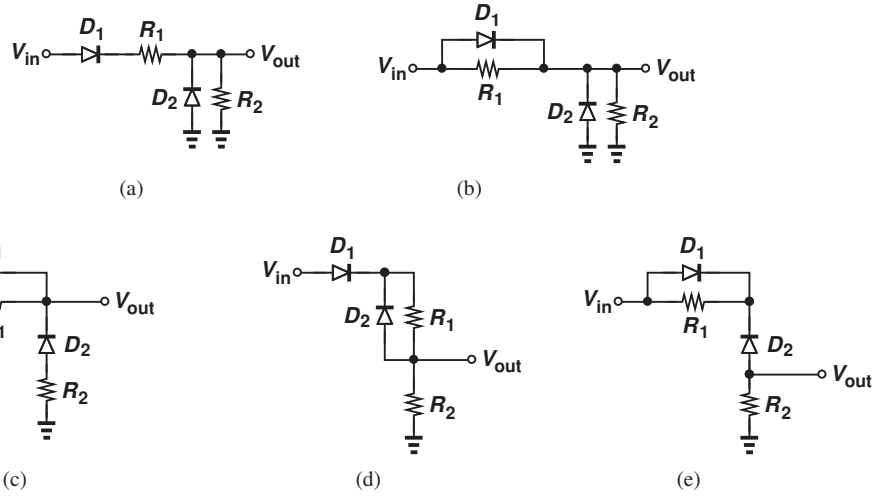


Figure 3.77

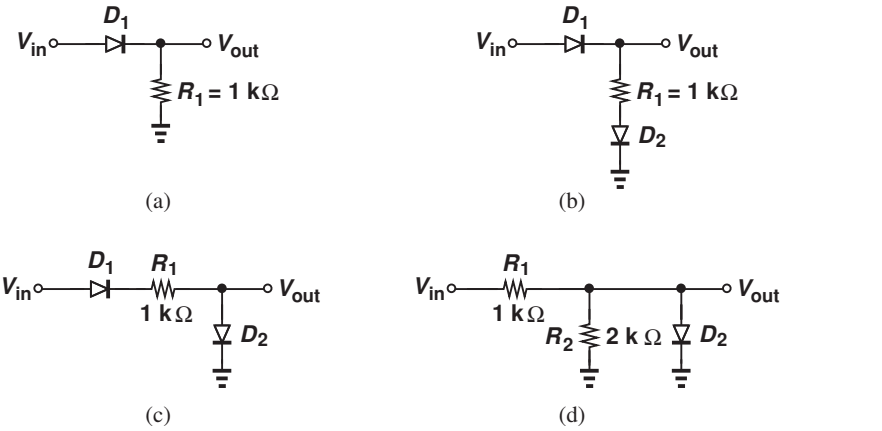


Figure 3.78

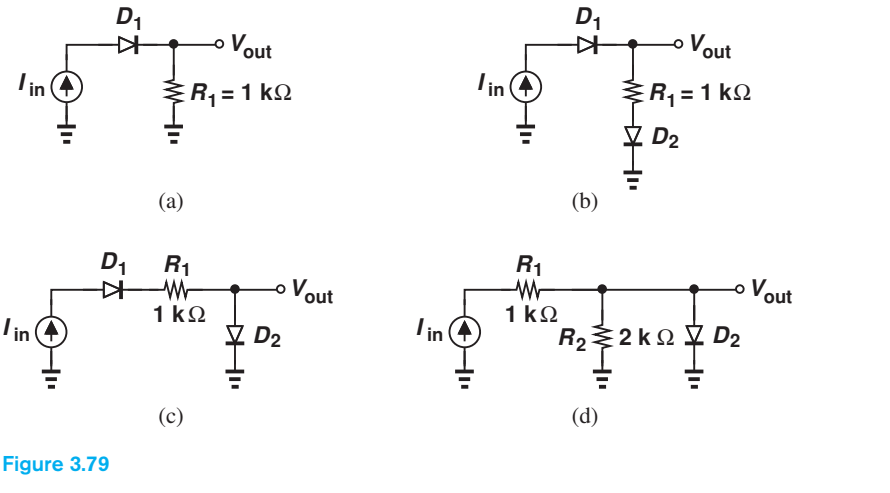


Figure 3.79

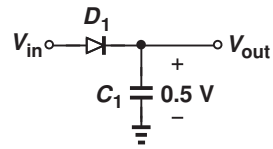


Figure 3.80

3.35. Repeat Problem 3.34 for the circuit shown in Fig. 3.81.

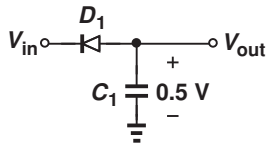


Figure 3.81

Section 3.5 Applications of Diodes

3.36. Suppose the rectifier of Fig. 3.32 drives a 100-Ω load with a peak voltage of 3.5 V. For a 1000-μF smoothing capacitor, calculate the ripple amplitude if the frequency is 60 Hz.

3.37. A 3-V adaptor using a half-wave rectifier must supply a current of 0.5 A with a maximum ripple of 300 mV. For a frequency of 60 Hz, compute the minimum required smoothing capacitor.

*__3.38.__ While constructing a full-wave rectifier, a student mistakenly has swapped the terminals of D_3 as depicted in Fig. 3.82. Explain what happens.

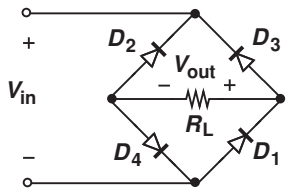


Figure 3.82

3.39. Plot the voltage across each diode in Fig. 3.38(b) as a function of time if $V_{in} = V_0 \cos \omega t$. Assume a constant-voltage diode model and $V_D > V_{D,on}$.

3.40. Assume the input and output grounds in a full-wave rectifier are shorted together. Draw the output waveform with and without the load capacitor and explain why the circuit does not operate as a rectifier.

3.41. A full-wave rectifier is driven by a sinusoidal input $V_{in} = V_0 \cos \omega t$, where $V_0 = 3$ V and $\omega = 2\pi(60\text{ Hz})$. Assuming $V_{D,on} = 800$ mV, determine the ripple amplitude with a 1000-μF smoothing capacitor and a load resistance of 30 Ω.

3.42. Suppose the negative terminals of V_{in} and V_{out} in Fig. 3.38(b) are shorted together. Plot the input-output characteristic assuming an ideal diode model and explaining why the circuit does not operate as a full-wave rectifier.

3.43. Suppose in Fig. 3.43, the diodes carry a current of 5 mA and the load, a current of 20 mA. If the load current increases to 21 mA, what is the change in the total voltage across the three diodes? Assume R_1 is much greater than $3r_d$.

3.44. In this problem, we estimate the ripple seen by the load in Fig. 3.43 so as to appreciate the regulation provided by the diodes. For simplicity, neglect the load. Also, $f_{in} = 60$ Hz, $C_1 = 100\ \mu$F, $R_1 = 1000\ \Omega$, and the peak voltage produced by the transformer is equal to 5 V.

(a) Assuming R_1 carries a relatively constant current and $V_{D,on} \approx 800$ mV, estimate the ripple amplitude across C_1.

(b) Using the small-signal model of the diodes, determine the ripple amplitude across the load.

3.45. Design the limiting circuit of Fig. 3.51 for a negative threshold of -1.9 V and a positive threshold of $+2.2$ V. Assume the input peak voltage is equal to 5 V, the maximum allowable current through each diode is 2 mA, and $V_{D,on} \approx 800$ mV.

*__3.46.__ In the limiting circuit of Fig. 3.51, plot the currents flowing through D_1 and D_2 as a function of time if the input is given by $V_0 \cos \omega t$ and $V_0 > V_{D,on} + V_{B1}$ and $-V_0 > -V_{D,on} - V_{B2}$.

3.47. We wish to design a circuit that exhibits the input/output characteristic shown in Fig. 3.83. Using 1-kΩ resistors, ideal diodes, and other components, construct the circuit.

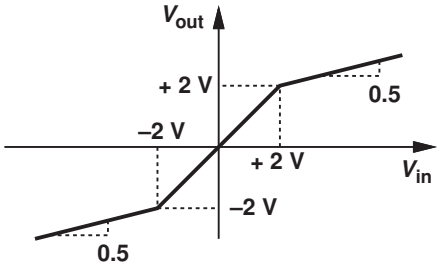


Figure 3.83

*__3.48.__ "Wave-shaping" applications require the input/output characteristic illustrated in Fig. 3.84. Using ideal diodes and other components, construct a circuit that provides such a characteristic. (The value of resistors is not unique.)

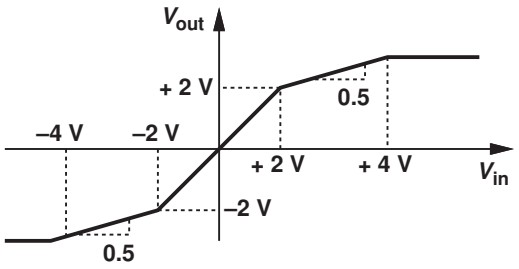


Figure 3.84

**__3.49.__ Suppose a triangular waveform is applied to the characteristic of Fig. 3.84 as shown in Fig. 3.85. Plot the output waveform and note that it is a rough approximation of a sinusoid. How should the input-output characteristic be modified so that the output becomes a better approximation of a sinusoid?

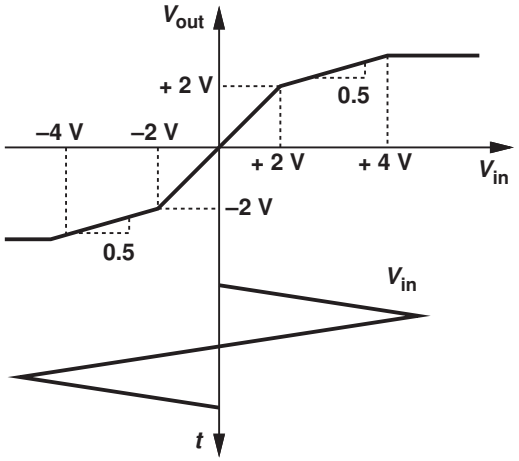


Figure 3.85

SPICE PROBLEMS

In the following problems, assume $I_S = 5 \times 10^{-16}$ A.

3.50. The half-wave rectifier of Fig. 3.86 must deliver a current of 5 mA to R_1 for a peak input level of 2 V.

(a) Using hand calculations, determine the required value of R_1.

(b) Verify the result by SPICE.

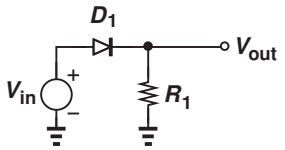


Figure 3.86

3.51. In the circuit of Fig. 3.87, $R_1 = 500\,\Omega$ and $R_2 = 1\,\text{k}\Omega$. Use SPICE to construct the input/output characteristic for $-2\,\text{V} < V_{in} < +2\,\text{V}$. Also, plot the current flowing through R_1 as a function of V_{in}.

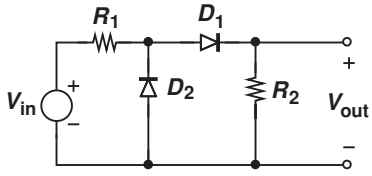


Figure 3.87

3.52. The rectifier shown in Fig. 3.88 is driven by a 60-Hz sinusoid input with a peak amplitude of 5 V. Using the transient analysis in SPICE,

(a) Determine the peak-to-peak ripple at the output.

(b) Determine the peak current flowing through D_1.

(c) Compute the heaviest load (smallest R_L) that the circuit can drive while maintaining a ripple less than 200 mV_{pp}.

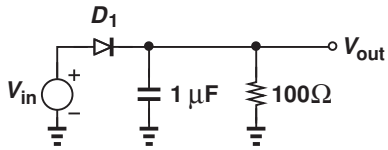


Figure 3.88

3.53. The circuit of Fig. 3.89 is used in some analog circuits. Plot the input/output characteristic for $-2\,\text{V} < V_{in} < +2\,\text{V}$ and determine the maximum input range across which $|V_{in} - V_{out}| < 5\,\text{mV}$.

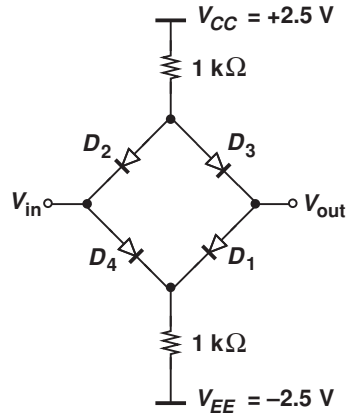
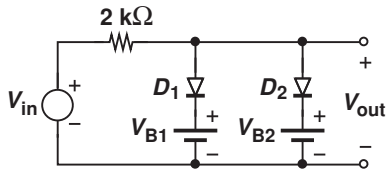
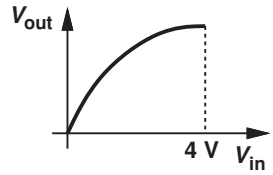


Figure 3.89

3.54. The circuit shown in Fig. 3.90 can provide an approximation of a sinusoid at the output in response to a triangular input waveform. Using the dc analysis in SPICE to plot the input/output characteristic for $0 < V_{in} < 4\,\text{V}$, determine the values of V_{B1} and V_{B2} such that the characteristic closely resembles a sinusoid.



(a)



(b)

Figure 3.90