Contents

CHAPTER 1
Models for Integrated-Circuit Active Devices 1

1.1 Introduction 1

1.2 Depletion Region of a *pn* Junction 1

1.2.1 Depletion-Region Capacitance 5

1.2.2 Junction Breakdown 6

1.3 Large-Signal Behavior of Bipolar Transistors 8

1.3.1 Large-Signal Models in the Forward-Active Region 8

1.3.2 Effects of Collector Voltage on Large-Signal Characteristics in the Forward-Active Region 14

1.3.3 Saturation and Inverse-Active Regions 16

1.3.4 Transistor Breakdown Voltages 20

1.3.5 Dependence of Transistor Current Gain β_F on Operating Conditions 23

1.4 Small-Signal Models of Bipolar Transistors 25

1.4.1 Transconductance 26

1.4.2 Base-Charging Capacitance 27

1.4.3 Input Resistance 28

1.4.4 Output Resistance 29

1.4.5 Basic Small-Signal Model of the Bipolar Transistor 30

1.4.6 Collector-Base Resistance 30

1.4.7 Parasitic Elements in the Small-Signal Model 31

1.4.8 Specification of Transistor Frequency Response 34

1.5 Large-Signal Behavior of Metal-Oxide-Semiconductor Field-Effect Transistors 38

1.5.1 Transfer Characteristics of MOS Devices 38

1.5.2 Comparison of Operating Regions of Bipolar and MOS Transistors 45

1.5.3 Decomposition of Gate-Source Voltage 47

1.5.4 Threshold Temperature Dependence 47

1.5.5 MOS Device Voltage Limitations 48

1.6 Small-Signal Models of MOS Transistors 49

1.6.1 Transconductance 50

1.6.2 Intrinsic Gate-Source and Gate-Drain Capacitance 51

1.6.3 Input Resistance 52

1.6.4 Output Resistance 52

1.6.5 Basic Small-Signal Model of the MOS Transistor 52

1.6.6 Body Transconductance 53

1.6.7 Parasitic Elements in the Small-Signal Model 54

1.6.8 MOS Transistor Frequency Response 55

1.7 Short-Channel Effects in MOS Transistors 59

1.7.1 Velocity Saturation from the Horizontal Field 59

1.7.2 Transconductance and Transition Frequency 63

1.7.3 Mobility Degradation from the Vertical Field 65

1.8 Weak Inversion in MOS Transistors 65

1.8.1 Drain Current in Weak Inversion 66

1.8.2 Transconductance and Transition Frequency in Weak Inversion 69

1.9 Substrate Current Flow in MOS Transistors 71

A.1.1 Summary of Active-Device Parameters 73

CHAPTER 2
Bipolar, MOS, and BiCMOS Integrated-Circuit Technology 78

2.1 Introduction 78
2.2 Basic Processes in Integrated-Circuit Fabrication 79
2.2.1 Electrical Resistivity of Silicon 79
2.2.2 Solid-State Diffusion 80
2.2.3 Electrical Properties of Diffused Layers 82
2.2.4 Photolithography 84
2.2.5 Epitaxial Growth 86
2.2.6 Ion Implantation 87
2.2.7 Local Oxidation 87
2.2.8 Polysilicon Deposition 87
2.3 High-Voltage Bipolar Integrated-Circuit Fabrication 88
2.4 Advanced Bipolar Integrated-Circuit Fabrication 92
2.5 Active Devices in Bipolar Analog Integrated Circuits 95
2.5.1 Integrated-Circuit *npn* Transistors 96
2.5.2 Integrated-Circuit *pnp* Transistors 107
2.6 Passive Components in Bipolar Integrated Circuits 115
2.6.1 Diffused Resistors 115
2.6.2 Epitaxial and Epitaxial Pinch Resistors 119
2.6.3 Integrated-Circuit Capacitors 120
2.6.4 Zener Diodes 121
2.6.5 Junction Diodes 122
2.7 Modifications to the Basic Bipolar Process 123
2.7.1 Dielectric Isolation 123
2.7.2 Compatible Processing for High-Performance Active Devices 124
2.7.3 High-Performance Passive Components 127
2.8 MOS Integrated-Circuit Fabrication 127
2.9 Active Devices in MOS Integrated Circuits 131
2.9.1 *n*-Channel Transistors 131
2.9.2 *p*-Channel Transistors 144
2.9.3 Depletion Devices 144
2.9.4 Bipolar Transistors 145
2.10 Passive Components in MOS Technology 146
2.10.1 Resistors 146
2.10.2 Capacitors in MOS Technology 148
2.10.3 Latchup in CMOS Technology 151
2.11 BiCMOS Technology 152
2.12 Heterojunction Bipolar Transistors 153
2.13 Interconnect Delay 156
2.14 Economics of Integrated-Circuit Fabrication 156
2.14.1 Yield Considerations in Integrated-Circuit Fabrication 157
2.14.2 Cost Considerations in Integrated-Circuit Fabrication 159
A.2.1 SPICE Model-Parameter Files 162

CHAPTER 3
Single-Transistor and Multiple-Transistor Amplifiers 169

3.1 Device Model Selection for Approximate Analysis of Analog Circuits 170
3.2 Two-Port Modeling of Amplifiers 171
3.3 Basic Single-Transistor Amplifier Stages 173
3.3.1 Common-Emitter Configuration 174
3.3.2 Common-Source Configuration 178
3.3.3 Common-Base Configuration 182
3.3.4 Common-Gate Configuration 185
3.3.5 Common-Base and Common-Gate Configurations with Finite r_o 187
3.3.5.1 Common-Base and Common-Gate Input Resistance 187
3.3.5.2 Common-Base and Common-Gate Output Resistance 189

Si el tipo hizo una sección para esos x q' es bicante

3.3.6 Common-Collector Configuration (Emitter Follower) 191
3.3.7 Common-Drain Configuration (Source Follower) 194
3.3.8 Common-Emitter Amplifier with Emitter Degeneration 196
3.3.9 Common-Source Amplifier with Source Degeneration 199
3.4 Multiple-Transistor Amplifier Stages 201
3.4.1 The CC-CE, CC-CC, and Darlington Configurations 201
3.4.2 The Cascode Configuration 205
3.4.2.1 The Bipolar Cascode 205
3.4.2.2 The MOS Cascode 207
3.4.3 The Active Cascode 210
3.4.4 The Super Source Follower 212
3.5 Differential Pairs 214
3.5.1 The dc Transfer Characteristic of an Emitter-Coupled Pair 214
3.5.2 The dc Transfer Characteristic with Emitter Degeneration 216
3.5.3 The dc Transfer Characteristic of a Source-Coupled Pair 217
3.5.4 Introduction to the Small-Signal Analysis of Differential Amplifiers 220
3.5.5 Small-Signal Characteristics of Balanced Differential Amplifiers 223
3.5.6 Device Mismatch Effects in Differential Amplifiers 229
3.5.6.1 Input Offset Voltage and Current 230
3.5.6.2 Input Offset Voltage of the Emitter-Coupled Pair 230
3.5.6.3 Offset Voltage of the Emitter-Coupled Pair: Approximate Analysis 231
3.5.6.4 Offset Voltage Drift in the Emitter-Coupled Pair 233
3.5.6.5 Input Offset Current of the Emitter-Coupled Pair 233
3.5.6.6 Input Offset Voltage of the Source-Coupled Pair 234
3.5.6.7 Offset Voltage of the Source-Coupled Pair: Approximate Analysis 235
3.5.6.8 Offset Voltage Drift in the Source-Coupled Pair 236
3.5.6.9 Small-Signal Characteristics of Unbalanced Differential Amplifiers 237
A.3.1 Elementary Statistics and the Gaussian Distribution 244

CHAPTER 4
Current Mirrors, Active Loads, and References 251
4.1 Introduction 251
4.2 Current Mirrors 251
4.2.1 General Properties 251
4.2.2 Simple Current Mirror 253
4.2.2.1 Bipolar 253
4.2.2.2 MOS 255
4.2.3 Simple Current Mirror with Beta Helper 258
4.2.3.1 Bipolar 258
4.2.3.2 MOS 260
4.2.4 Simple Current Mirror with Degeneration 260
4.2.4.1 Bipolar 260
4.2.4.2 MOS 261
4.2.5 Cascode Current Mirror 261
4.2.5.1 Bipolar 261
4.2.5.2 MOS 264
4.2.6 Wilson Current Mirror 272
4.2.6.1 Bipolar 272
4.2.6.2 MOS 275
4.3 Active Loads 276
4.3.1 Motivation 276
4.3.2 Common-Emitter–Common-Source Amplifier with Complementary Load 277
4.3.3 Common-Emitter–Common-Source Amplifier with Depletion Load 280
4.3.4 Common-Emitter–Common-Source Amplifier with Diode-Connected Load 282
4.3.5 Differential Pair with Current-Mirror Load 285
4.3.5.1 Large-Signal Analysis 285
4.3.5.2 Small-Signal Analysis 286
4.3.5.3 Common-Mode Rejection Ratio 291

4.4 Voltage and Current References 297
4.4.1 Low-Current Biasing 297
4.4.1.1 Bipolar Widlar Current Source 297
4.4.1.2 MOS Widlar Current Source 300
4.4.1.3 Bipolar Peaking Current Source 301
4.4.1.4 MOS Peaking Current Source 302
4.4.2 Supply-Insensitive Biasing 303
4.4.2.1 Widlar Current Sources 304
4.4.2.2 Current Sources Using Other Voltage Standards 305
4.4.2.3 Self-Biasing 307
4.4.3 Temperature-Insensitive Biasing 315
4.4.3.1 Band-Gap-Referenced Bias Circuits in Bipolar Technology 315
4.4.3.2 Band-Gap-Referenced Bias Circuits in CMOS Technology 321
A.4.1 Matching Considerations in Current Mirrors 325
A.4.1.1 Bipolar 325
A.4.1.2 MOS 328
A.4.2 Input Offset Voltage of Differential Pair with Active Load 330
A.4.2.1 Bipolar 330
A.4.2.2 MOS 332

CHAPTER 5
Output Stages 341

5.1 Introduction 341
5.2 The Emitter Follower as an Output Stage 341
5.2.1 Transfer Characteristics of the Emitter-Follower 341
5.2.2 Power Output and Efficiency 344
5.2.3 Emitter-Follower Drive Requirements 351
5.2.4 Small-Signal Properties of the Emitter Follower 352
5.3 The Source Follower as an Output Stage 353
5.3.1 Transfer Characteristics of the Source Follower 353
5.3.2 Distortion in the Source Follower 355
5.4 Class B Push–Pull Output Stage 359
5.4.1 Transfer Characteristic of the Class B Stage 360
5.4.2 Power Output and Efficiency of the Class B Stage 362
5.4.3 Practical Realizations of Class B Complementary Output Stages 366
5.4.4 All-*npn* Class B Output Stage 373
5.4.5 Quasi-Complementary Output Stages 376
5.4.6 Overload Protection 377
5.5 CMOS Class AB Output Stages 379
5.5.1 Common-Drain Configuration 380
5.5.2 Common-Source Configuration with Error Amplifiers 381
5.5.3 Alternative Configurations 388
5.5.3.1 Combined Common-Drain Common-Source Configuration 388
5.5.3.2 Combined Common-Drain Common-Source Configuration with High Swing 390
5.5.3.3 Parallel Common-Source Configuration 390

CHAPTER 6
Operational Amplifiers with Single-Ended Outputs 400

6.1 Applications of Operational Amplifiers 401
6.1.1 Basic Feedback Concepts 401
6.1.2 Inverting Amplifier 402
6.1.3 Noninverting Amplifier 404
6.1.4 Differential Amplifier 404
6.1.5 Nonlinear Analog Operations 405
6.1.6 Integrator, Differentiator 406
6.1.7 Internal Amplifiers 407
6.1.7.1 Switched-Capacitor Amplifier 407
6.1.7.2 Switched-Capacitor Integrator 412

6.2 Deviations from Ideality in Real Operational Amplifiers 415
6.2.1 Input Bias Current 415
6.2.2 Input Offset Current 416
6.2.3 Input Offset Voltage 416
6.2.4 Common-Mode Input Range 416
6.2.5 Common-Mode Rejection Ratio (CMRR) 417
6.2.6 Power-Supply Rejection Ratio (PSRR) 418
6.2.7 Input Resistance 420
6.2.8 Output Resistance 420
6.2.9 Frequency Response 420
6.2.10 Operational-Amplifier Equivalent Circuit 420
6.3 Basic Two-Stage MOS Operational Amplifiers 421
6.3.1 Input Resistance, Output Resistance, and Open-Circuit Voltage Gain 422
6.3.2 Output Swing 423
6.3.3 Input Offset Voltage 424
6.3.4 Common-Mode Rejection Ratio 427
6.3.5 Common-Mode Input Range 427
6.3.6 Power-Supply Rejection Ratio (PSRR) 430
6.3.7 Effect of Overdrive Voltages 434
6.3.8 Layout Considerations 435
6.4 Two-Stage MOS Operational Amplifiers with Cascodes 438
6.5 MOS Telescopic-Cascode Operational Amplifiers 439
6.6 MOS Folded-Cascode Operational Amplifiers 442
6.7 MOS Active-Cascode Operational Amplifiers 446
6.8 Bipolar Operational Amplifiers 448
6.8.1 The dc Analysis of the NE5234 Operational Amplifier 452
6.8.2 Transistors that Are Normally Off 467
6.8.3 Small-Signal Analysis of the NE5234 Operational Amplifier 469
6.8.4 Calculation of the Input Offset Voltage and Current of the NE5234 477

CHAPTER 7
Frequency Response of Integrated Circuits 490

7.1 Introduction 490
7.2 Single-Stage Amplifiers 490
7.2.1 Single-Stage Voltage Amplifiers and the Miller Effect 490
7.2.1.1 The Bipolar Differential Amplifier: Differential-Mode Gain 495
7.2.1.2 The MOS Differential Amplifier: Differential-Mode Gain 499
7.2.2 Frequency Response of the Common-Mode Gain for a Differential Amplifier 501
7.2.3 Frequency Response of Voltage Buffers 503
7.2.3.1 Frequency Response of the Emitter Follower 505
7.2.3.2 Frequency Response of the Source Follower 511
7.2.4 Frequency Response of Current Buffers 514
7.2.4.1 Common-Base Amplifier Frequency Response 516
7.2.4.2 Common-Gate Amplifier Frequency Response 517
7.3 Multistage Amplifier Frequency Response 518
7.3.1 Dominant-Pole Approximation 518
7.3.2 Zero-Value Time Constant Analysis 519
7.3.3 Cascode Voltage-Amplifier Frequency Response 524
7.3.4 Cascode Frequency Response 527
7.3.5 Frequency Response of a Current Mirror Loading a Differential Pair 534
7.3.6 Short-Circuit Time Constants 536
7.4 Analysis of the Frequency Response of the NE5234 Op Amp 539
7.4.1 High-Frequency Equivalent Circuit of the NE5234 539
7.4.2 Calculation of the −3-dB Frequency of the NE5234 540
7.4.3 Nondominant Poles of the NE5234 542

7.5 Relation Between Frequency Response and Time Response 542

CHAPTER 8
Feedback 553

8.1 Ideal Feedback Equation 553
8.2 Gain Sensitivity 555
8.3 Effect of Negative Feedback on Distortion 555
8.4 Feedback Configurations 557
8.4.1 Series-Shunt Feedback 557
8.4.2 Shunt-Shunt Feedback 560
8.4.3 Shunt-Series Feedback 561
8.4.4 Series-Series Feedback 562
8.5 Practical Configurations and the Effect of Loading 563
8.5.1 Shunt-Shunt Feedback 563
8.5.2 Series-Series Feedback 569
8.5.3 Series-Shunt Feedback 579
8.5.4 Shunt-Series Feedback 583
8.5.5 Summary 587
8.6 Single-Stage Feedback 587
8.6.1 Local Series-Series Feedback 587
8.6.2 Local Series-Shunt Feedback 591
8.7 The Voltage Regulator as a Feedback Circuit 593
8.8 Feedback Circuit Analysis Using Return Ratio 599
8.8.1 Closed-Loop Gain Using Return Ratio 601
8.8.2 Closed-Loop Impedance Formula Using Return Ratio 607
8.8.3 Summary—Return-Ratio Analysis 612
8.9 Modeling Input and Output Ports in Feedback Circuits 613

CHAPTER 9
Frequency Response and Stability of Feedback Amplifiers 624

9.1 Introduction 624
9.2 Relation Between Gain and Bandwidth in Feedback Amplifiers 624
9.3 Instability and the Nyquist Criterion 626
9.4 Compensation 633
9.4.1 Theory of Compensation 633
9.4.2 Methods of Compensation 637
9.4.3 Two-Stage MOS Amplifier Compensation 643
9.4.4 Compensation of Single-Stage CMOS Op Amps 650
9.4.5 Nested Miller Compensation 654
9.5 Root-Locus Techniques 664
9.5.1 Root Locus for a Three-Pole Transfer Function 665
9.5.2 Rules for Root-Locus Construction 667
9.5.3 Root Locus for Dominant-Pole Compensation 676
9.5.4 Root Locus for Feedback-Zero Compensation 677
9.6 Slew Rate 681
9.6.1 Origin of Slew-Rate Limitations 681
9.6.2 Methods of Improving Slew-Rate in Two-Stage Op Amps 685
9.6.3 Improving Slew-Rate in Bipolar Op Amps 687
9.6.4 Improving Slew-Rate in MOS Op Amps 688
9.6.5 Effect of Slew-Rate Limitations on Large-Signal Sinusoidal Performance 692

A.9.1 Analysis in Terms of Return-Ratio Parameters 693
A.9.2 Roots of a Quadratic Equation 694

CHAPTER 10
Nonlinear Analog Circuits 704

10.1 Introduction 704
10.2 Analog Multipliers Employing the Bipolar Transistor 704
10.2.1 The Emitter-Coupled Pair as a Simple Multiplier 704
10.2.2 The dc Analysis of the Gilbert Multiplier Cell 706

10.2.3 The Gilbert Cell as an Analog Multiplier 708
10.2.4 A Complete Analog Multiplier 711
10.2.5 The Gilbert Multiplier Cell as a Balanced Modulator and Phase Detector 712
10.3 Phase-Locked Loops (PLL) 716
10.3.1 Phase-Locked Loop Concepts 716
10.3.2 The Phase-Locked Loop in the Locked Condition 718
10.3.3 Integrated-Circuit Phase-Locked Loops 727
10.4 Nonlinear Function Synthesis 731

CHAPTER 11
Noise in Integrated Circuits 736

11.1 Introduction 736
11.2 Sources of Noise 736
11.2.1 Shot Noise 736
11.2.2 Thermal Noise 740
11.2.3 Flicker Noise (1/f Noise) 741
11.2.4 Burst Noise (*Popcorn Noise*) 742
11.2.5 Avalanche Noise 743
11.3 Noise Models of Integrated-Circuit Components 744
11.3.1 Junction Diode 744
11.3.2 Bipolar Transistor 745
11.3.3 MOS Transistor 746
11.3.4 Resistors 747
11.3.5 Capacitors and Inductors 747
11.4 Circuit Noise Calculations 748
11.4.1 Bipolar Transistor Noise Performance 750
11.4.2 Equivalent Input Noise and the Minimum Detectable Signal 754
11.5 Equivalent Input Noise Generators 756
11.5.1 Bipolar Transistor Noise Generators 757
11.5.2 MOS Transistor Noise Generators 762
11.6 Effect of Feedback on Noise Performance 764
11.6.1 Effect of Ideal Feedback on Noise Performance 764
11.6.2 Effect of Practical Feedback on Noise Performance 765
11.7 Noise Performance of Other Transistor Configurations 771
11.7.1 Common-Base Stage Noise Performance 771
11.7.2 Emitter-Follower Noise Performance 773
11.7.3 Differential-Pair Noise Performance 773
11.8 Noise in Operational Amplifiers 776
11.9 Noise Bandwidth 782
11.10 Noise Figure and Noise Temperature 786
11.10.1 Noise Figure 786
11.10.2 Noise Temperature 790

CHAPTER 12
Fully Differential Operational Amplifiers 796

12.1 Introduction 796
12.2 Properties of Fully Differential Amplifiers 796
12.3 Small-Signal Models for Balanced Differential Amplifiers 799
12.4 Common-Mode Feedback 804
12.4.1 Common-Mode Feedback at Low Frequencies 805
12.4.2 Stability and Compensation Considerations in a CMFB Loop 810
12.5 CMFB Circuits 811
12.5.1 CMFB Using Resistive Divider and Amplifier 812
12.5.2 CMFB Using Two Differential Pairs 816
12.5.3 CMFB Using Transistors in the Triode Region 819
12.5.4 Switched-Capacitor CMFB 821
12.6 Fully Differential Op Amps 823
12.6.1 A Fully Differential Two-Stage Op Amp 823
12.6.2 Fully Differential Telescopic Cascode Op Amp 833

12.6.3 Fully Differential Folded-Cascode Op Amp 834
12.6.4 A Differential Op Amp with Two Differential Input Stages 835
12.6.5 Neutralization 835
12.7 Unbalanced Fully Differential Circuits 838
12.8 Bandwidth of the CMFB Loop 844
12.9 Analysis of a CMOS Fully Differential Folded-Cascode Op Amp 845
12.9.1 DC Biasing 848
12.9.2 Low-Frequency Analysis 850
12.9.3 Frequency and Time Responses in a Feedback Application 856
Index 871

Symbol Convention

Unless otherwise stated, the following symbol convention is used in this book. *Bias* or *dc* quantities, such as transistor collector current I_C and collector-emitter voltage V_{CE}, are represented by uppercase symbols with uppercase subscripts. Small-signal quantities, such as the incremental change in transistor collector current i_c, are represented by lowercase symbols with lowercase subscripts. Elements such as transconductance g_m in small-signal equivalent circuits are represented in the same way. Finally, quantities such as *total* collector current I_c, which represent the sum of the bias quantity *and* the signal quantity, are represented by an uppercase symbol with a lowercase subscript.