

Single-Transistor and Multiple-Transistor Amplifiers

The technology used to fabricate integrated circuits presents a unique set of component-cost constraints to the circuit designer. The most cost-effective circuit approach to accomplish a given function may be quite different when the realization of the circuit is to be in monolithic form as opposed to discrete transistors and passive elements.¹ As an illustration, consider the two realizations of a three-stage audio amplifier shown in Figs. 3.1 and 3.2. The first reflects a cost-effective solution in the context of discrete-component circuits, since passive components such as resistors and capacitors are less expensive than the active components, the transistors. Hence, the circuit contains a minimum number of transistors, and the interstage coupling is accomplished with capacitors. However, for the case of monolithic construction, a key determining factor in cost is the die area used. Capacitors of the values used in most discrete-component circuits are not feasible and would have to be external to the chip, increasing the pin count of the package, which increases cost. Therefore, a high premium is placed on eliminating large capacitors, and a dc-coupled circuit realization is very desirable. A second constraint is that the *cheapest* component that can be fabricated in the integrated circuit is the one that occupies the least area, usually a transistor. Thus a circuit realization that contains the minimum possible total resistance while using more active components may be optimum.^{2,3} Furthermore, an important application of analog circuits is to provide interfaces between the real world and digital circuits. In building digital integrated circuits, CMOS technologies have become dominant because of their high densities and low power dissipations. To reduce the cost and increase the portability of mixed-analog-and-digital systems, both increased levels of integration and reduced power dissipations are required. As a result, we are interested in building analog interface circuits in CMOS technologies. The circuit of Fig. 3.2 reflects these constraints. It uses a CMOS technology and many more transistors than in Fig. 3.1, has less total resistance, and has no coupling capacitors. A differential pair is used to allow direct coupling between stages, while transistor current sources provide biasing without large amounts of resistance. In practice, feedback would be required around the amplifier shown in Fig. 3.2 but is not shown for simplicity. Feedback is described in Chapter 8.

The next three chapters analyze various circuit configurations encountered in linear integrated circuits. In discrete-component circuits, the number of transistors is usually minimized. The best way to analyze such circuits is usually to regard each individual transistor as a *stage* and to analyze the circuit as a collection of single-transistor stages. A typical monolithic circuit, however, contains a large number of transistors that perform many functions, both passive and active. Thus monolithic circuits are often regarded as a collection of *subcircuits* that perform specific functions, where the subcircuits may contain many transistors. In this chapter, we first consider the dc and low-frequency properties of the simplest subcircuits: common-emitter, common-base, and common-collector single-transistor amplifiers and their counterparts using

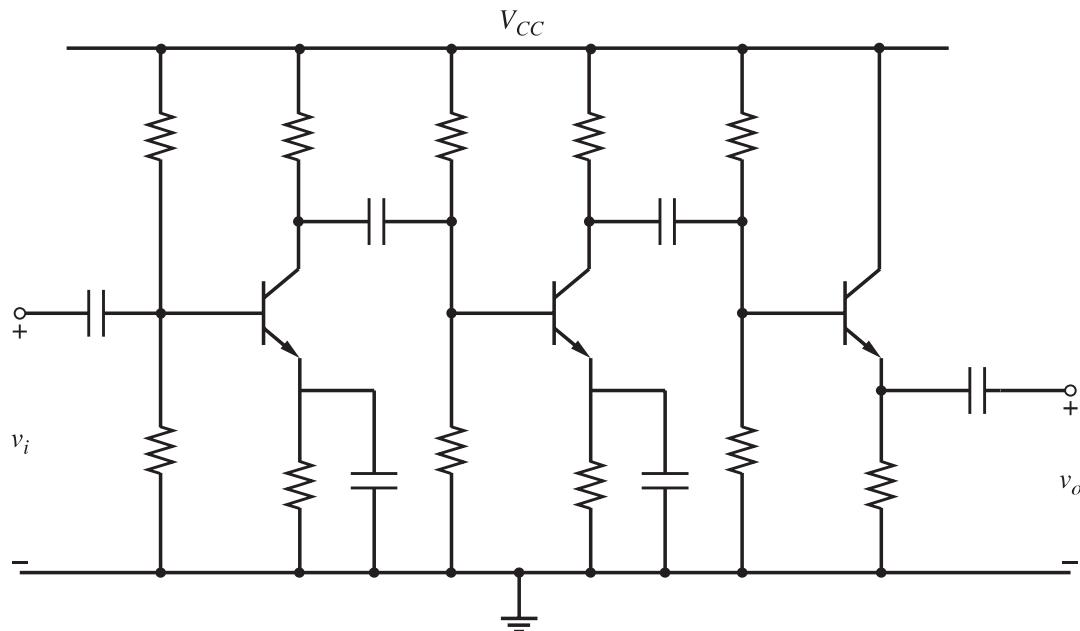


Figure 3.1 Typical discrete-component realization of an audio amplifier.

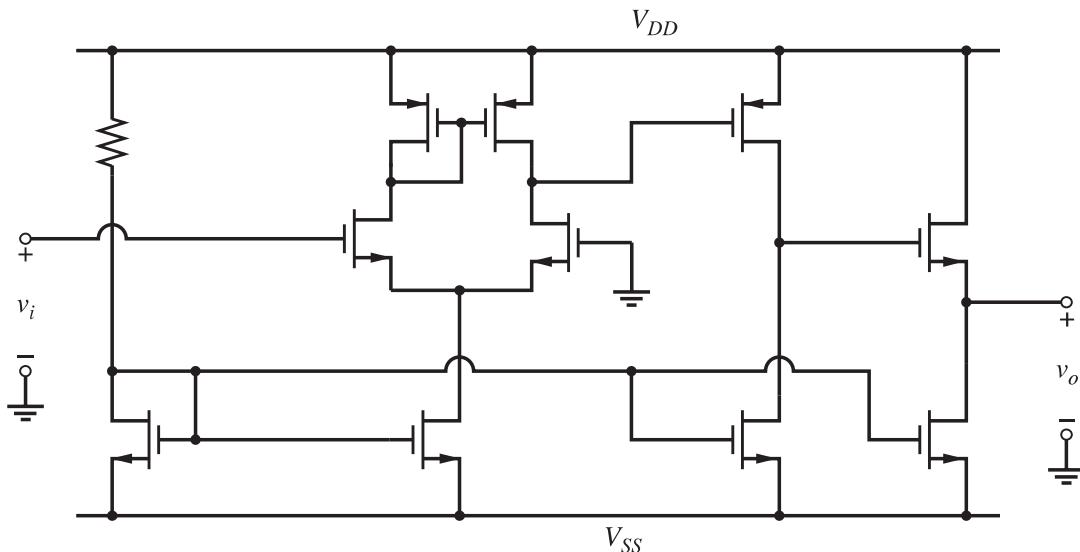


Figure 3.2 Typical CMOS integrated-circuit realization of an audio amplifier.

MOS transistors. We then consider some multi-transistor subcircuits that are useful as amplifying stages. The most widely used of these multi-transistor circuits are the differential pairs, which are analyzed extensively in this chapter.

3.1 Device Model Selection for Approximate Analysis of Analog Circuits

Much of this book is concerned with the salient performance characteristics of a variety of subcircuits commonly used in analog circuits and of complete functional blocks made up of these subcircuits. The aspects of the performance that are of interest include the dc currents and voltages within the circuit, the effect of mismatches in device characteristics on these voltages and currents, the small-signal, low-frequency input and output resistance, and the voltage gain of the circuit. In later chapters, the high-frequency, small-signal behavior of

circuits is considered. The subcircuit or circuit under investigation is often one of considerable complexity, and the most important single principle that must be followed to achieve success in the hand analysis of such circuits is *selecting the simplest possible model* for the devices within the circuit that will result in the required accuracy. For example, in the case of dc analysis, hand analysis of a complex circuit is greatly simplified by neglecting certain aspects of transistor behavior, such as the output resistance, which may result in a 10 to 20 percent error in the dc currents calculated. The principal objective of hand analysis, however, is to obtain an intuitive understanding of factors affecting circuit behavior so that an iterative design procedure resulting in improved performance can be carried out. The performance of the circuit can at any point in this cycle be determined precisely by computer simulation, but this approach does not yield the intuitive understanding necessary for design.

Unfortunately, no specific rules can be formulated regarding the selection of the simplest device model for analysis. For example, in the dc analysis of bipolar biasing circuits, assuming constant base-emitter voltages and neglecting transistor output resistances often provides adequate accuracy. However, certain bias circuits depend on the nonlinear relation between the collector current and base-emitter voltage to control the bias current, and the assumption of a constant V_{BE} will result in gross errors in the analyses of these circuits. When analyzing the active-load stages in Chapter 4, the output resistance must be considered to obtain meaningful results. Therefore, a key step in every analysis is to inspect the circuit to determine what aspects of the behavior of the transistors strongly affect the performance of the circuit, and then simplify the model(s) to include only those aspects. This step in the procedure is emphasized in this and the following chapters.

3.2 Two-Port Modeling of Amplifiers

The most basic parameter of an amplifier is its gain. Since amplifiers may be connected to a wide variety of sources and loads, predicting the dependence of the gain on the source and load resistance is also important. One way to observe this dependence is to include these resistances in the amplifier analysis. However, this approach requires a completely new amplifier analysis each time the source or load resistance is changed. To simplify this procedure, amplifiers are often modeled as two-port equivalent networks. As shown in Fig. 3.3, two-port networks have four terminals and four port variables (a voltage and a current at each port). A pair of terminals is a port if the current that flows into one terminal is equal to the current that flows out of the other terminal. To model an amplifier, one port represents the amplifier input characteristics and the other represents the output. One variable at each port can be set independently. The other variable at each port is dependent on the two-port network and the independent variables. This dependence is expressed by two equations. We will focus here on the admittance-parameter equations, where the terminal currents are viewed as dependent variables controlled by the independent terminal voltages because we usually model transistors with voltage-controlled current sources. If the network is linear and

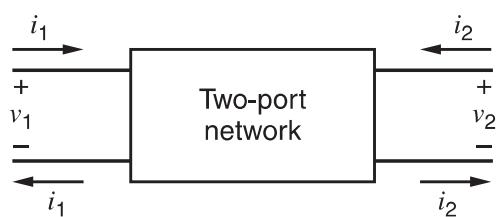


Figure 3.3 Two-port-network block diagram.

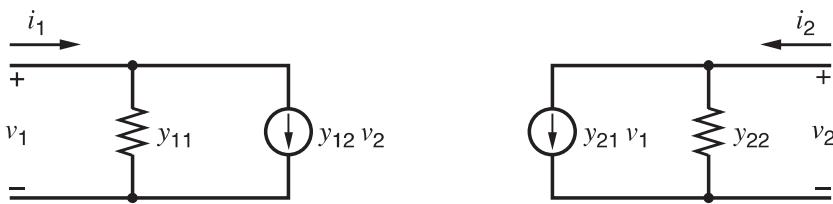


Figure 3.4 Admittance-parameter, two-port equivalent circuit.

contains no independent sources, the admittance-parameter equations are:

$$i_1 = y_{11}v_1 + y_{12}v_2 \quad (3.1)$$

$$i_2 = y_{21}v_1 + y_{22}v_2 \quad (3.2)$$

The voltages and currents in these equations are deliberately written as small-signal quantities because transistors behave in an approximately linear way only for small signals around a fixed operating point. An equivalent circuit for these equations is shown in Fig. 3.4. The parameters can be found and interpreted as follows:

$$y_{11} = \left. \frac{i_1}{v_1} \right|_{v_2=0} = \text{Input admittance with the output short-circuited} \quad (3.3)$$

$$y_{12} = \left. \frac{i_1}{v_2} \right|_{v_1=0} = \text{Reverse transconductance with the input short-circuited} \quad (3.4)$$

$$y_{21} = \left. \frac{i_2}{v_1} \right|_{v_2=0} = \text{Forward transconductance with the output short-circuited} \quad (3.5)$$

$$y_{22} = \left. \frac{i_2}{v_2} \right|_{v_1=0} = \text{Output admittance with the input short-circuited} \quad (3.6)$$

The y_{12} parameter represents feedback in the amplifier. When the signal propagates back from the output to the input as well as forward from the input to the output, the amplifier is said to be *bilateral*. In many practical cases, especially at low frequencies, this feedback is negligible and y_{12} is assumed to be zero. Then the amplifier is *unilateral* and characterized by the other three parameters. Since the model includes only one transconductance when $y_{12} = 0$, y_{21} is usually referred to simply as the *short-circuit transconductance*, which will be represented by G_m in this book. When an amplifier is unilateral, the calculation of y_{11} is simplified from that given in (3.3) because the connections at the output port do not affect the input admittance when $y_{12} = 0$.

Instead of calculating y_{11} and y_{22} , we will often calculate the reciprocals of these parameters, or the input and output impedances $Z_i = 1/y_{11}$ and $Z_o = 1/y_{22}$, as shown in the unilateral two-port model of Fig. 3.5a. Also, instead of calculating the short-circuit transconductance $G_m = y_{21}$, we will sometimes calculate the open-circuit voltage gain a_v . This substitution is justified by conversion of the Norton-equivalent output model shown in Fig. 3.5a to the Thévenin-equivalent output model shown in Fig. 3.5b. In general, finding any two of the three parameters including G_m , Z_o , and a_v specifies the third parameter because

$$a_v = \left. \frac{v_2}{v_1} \right|_{i_2=0} = -G_m Z_o \quad (3.7)$$

Once two of these parameters and the input impedance are known, calculation of the effects of loading at the input and output ports is possible. At low frequencies, the input and output impedances are usually dominated by resistances. Therefore, we will characterize the low-frequency behavior of many amplifiers in this book by finding the input and output resistances, R_i and R_o , as well as G_m or a_v .

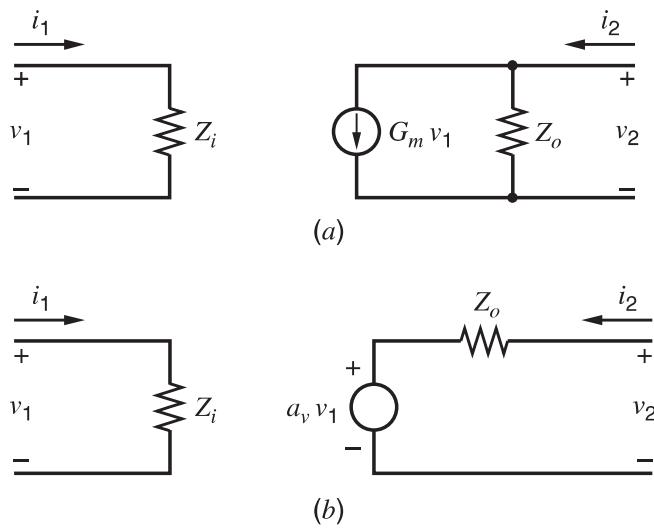


Figure 3.5 Unilateral two-port equivalent circuits with (a) Norton output model (b) Thévenin output model.

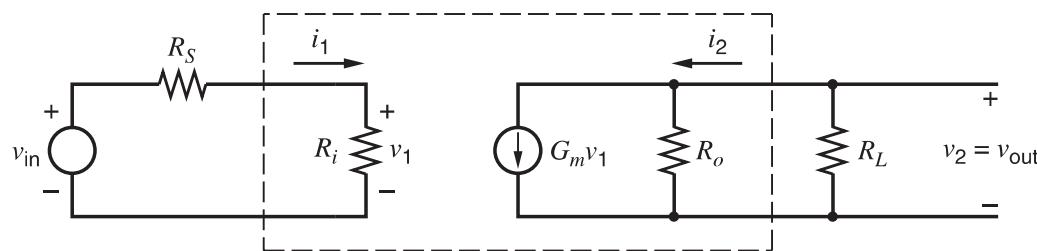


Figure 3.6 Example of loading at the input and output of an amplifier modeled by a two-port equivalent circuit.

■ EXAMPLE

A two-port model of a unilateral amplifier is shown in Fig. 3.6. Assume $R_i = 1 \text{ k}\Omega$, $R_o = 1 \text{ M}\Omega$, and $G_m = 1 \text{ mA/V}$. Let R_S and R_L represent the source resistance of the input generator and load resistance, respectively. Find the low-frequency gain $v_{\text{out}}/v_{\text{in}}$, assuming that the input is an ideal voltage source and the output is unloaded. Repeat, assuming that $R_S = 1 \text{ k}\Omega$ and $R_L = 1 \text{ M}\Omega$.

The open-circuit voltage gain of the two-port amplifier model by itself from v_1 to v_{out} is

$$\left. \frac{v_{\text{out}}}{v_1} \right|_{R_L \rightarrow \infty} = \left. \frac{v_2}{v_1} \right|_{i_2=0} = -G_m R_o = -(1 \text{ mA/V})(1000 \text{ k}\Omega) = -1000$$

Since the source and input resistances form a voltage divider, and since the output resistance appears in parallel with the load resistance, the overall gain from v_{in} to v_{out} is

$$\frac{v_{\text{out}}}{v_{\text{in}}} = \frac{v_1}{v_{\text{in}}} \frac{v_{\text{out}}}{v_1} = -\frac{R_i}{R_i + R_S} G_m (R_o \parallel R_L)$$

With an ideal voltage source at the input and no load at the output, $R_S = 0$, $R_L \rightarrow \infty$, and $v_{\text{out}}/v_{\text{in}} = -1000$. With $R_S = 1 \text{ k}\Omega$ and $R_L = 1 \text{ M}\Omega$, the gain is reduced by a factor of four to $v_{\text{out}}/v_{\text{in}} = -0.5(1 \text{ mA/V})(500 \text{ k}\Omega) = -250$.

3.3 Basic Single-Transistor Amplifier Stages

Bipolar and MOS transistors are capable of providing useful amplification in three different configurations. In the common-emitter or common-source configuration, the signal is applied to the base or gate of the transistor and the amplified output is taken from the collector or drain.

In the common-collector or common-drain configuration, the signal is applied to the base or gate and the output signal is taken from the emitter or source. This configuration is often referred to as the *emitter follower* for bipolar circuits and the *source follower* for MOS circuits. In the common-base or common-gate configuration, the signal is applied to the emitter or the source, and the output signal is taken from the collector or the drain. Each of these configurations provides a unique combination of input resistance, output resistance, voltage gain, and current gain. In many instances, the analysis of complex multistage amplifiers can be reduced to the analysis of a number of single-transistor stages of these types.

We showed in Chapter 1 that the small-signal equivalent circuits for the bipolar and MOS transistors are very similar, with the two devices differing mainly in the values of some of their small-signal parameters. In particular, MOS transistors have essentially infinite input resistance from the gate to the source, in contrast with the finite r_π of bipolar transistors. On the other hand, bipolar transistors have a g_m that is usually an order of magnitude larger than that of MOS transistors biased with the same current. These differences often make one or the other device desirable for use in different situations. For example, amplifiers with very high input impedance are more easily realized with MOS transistors than with bipolar transistors. However, the higher g_m of bipolar transistors makes the realization of high-gain amplifiers with bipolar transistors easier than with MOS transistors. In other applications, the exponential large-signal characteristics of bipolar transistors and the square-law characteristics of MOS transistors may each be used to advantage.

As described in Chapter 2, integrated-circuit processes of many varieties now exist. Examples include processes with bipolar or MOS transistors as the only active devices and combined bipolar and CMOS devices in BiCMOS processes. Because the more complex processes involve more masking steps and are thus somewhat more costly to produce, integrated-circuit designers generally use the simplest process available that allows the desired circuit specifications to be achieved. Therefore, designers must appreciate the similarities and differences between bipolar and MOS transistors so that appropriate choices of technology can be made.

3.3.1 Common-Emitter Configuration

The resistively loaded common-emitter (CE) amplifier configuration is shown in Fig. 3.7. The resistor R_C represents the collector load resistance. The short horizontal line labeled V_{CC} at the top of R_C implies that a voltage source of value V_{CC} is connected between that point and ground. This symbol will be used throughout the book. We first calculate the dc transfer characteristic of the amplifier as the input voltage is increased in the positive direction from

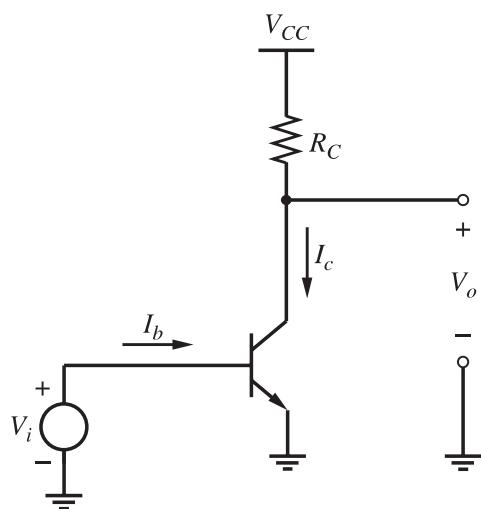


Figure 3.7 Resistively loaded common-emitter amplifier.

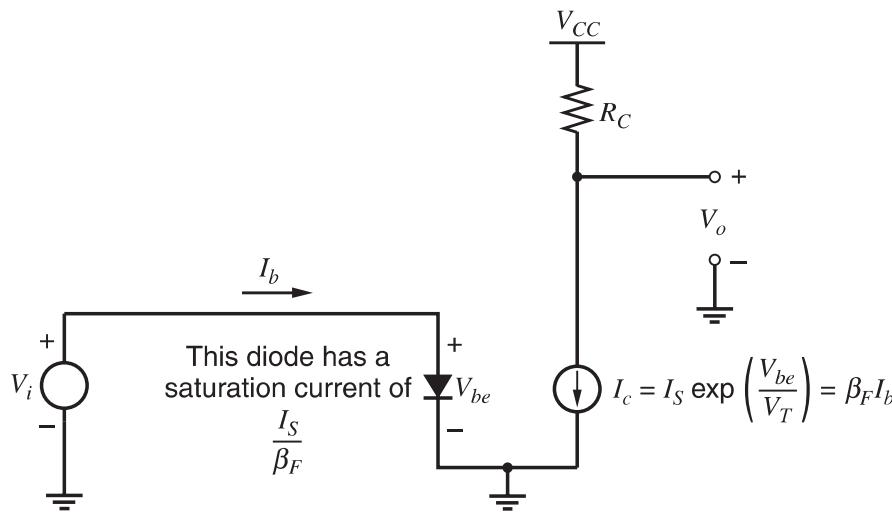


Figure 3.8 Large-signal equivalent circuit valid when the transistor is in the forward-active region. The saturation current of the equivalent base-emitter diode is I_S/β_F .

zero. We assume that the base of the transistor is driven by a voltage source of value V_i . When V_i is zero, the transistor operates in the cutoff state and no collector current flows other than the leakage current I_{CO} . As the input voltage is increased, the transistor enters the forward-active region, and the collector current is given by

$$I_c = I_S \exp \frac{V_i}{V_T} \quad (3.8)$$

The equivalent circuit for the amplifier when the transistor operates in the forward-active region was derived in Chapter 1 and is repeated in Fig. 3.8. Because of the exponential relationship between I_c and V_{be} , the value of the collector current is very small until the input voltage reaches approximately 0.5 V. As long as the transistor operates in the forward-active region, the base current is equal to the collector current divided by β_F , or

$$I_b = \frac{I_c}{\beta_F} = \frac{I_S}{\beta_F} \exp \frac{V_i}{V_T} \quad (3.9)$$

The output voltage is equal to the supply voltage, V_{CC} , minus the voltage drop across the collector resistor:

$$V_o = V_{CC} - I_c R_C = V_{CC} - R_C I_S \exp \frac{V_i}{V_T} \quad (3.10)$$

When the output voltage approaches zero, the collector-base junction of the transistor becomes forward biased and the device enters saturation. Once the transistor becomes saturated, the output voltage and collector current take on nearly constant values:

$$V_o = V_{CE(\text{sat})} \quad (3.11)$$

$$I_c = \frac{V_{CC} - V_{CE(\text{sat})}}{R_C} \quad (3.12)$$

The base current, however, continues to increase with further increases in V_i . Therefore, the forward current gain I_c/I_b decreases from β_F as the transistor leaves the forward-active region of operation and moves into saturation. In practice, the current available from the signal source is limited. When the signal source can no longer increase the base current, V_i is maximum. The output voltage and the base current are plotted as a function of the input voltage in Fig. 3.9. Note that when the device operates in the forward-active region, small changes in the input voltage can give rise to large changes in the output voltage. The circuit thus provides *voltage gain*. We now proceed to calculate the voltage gain in the forward-active region.

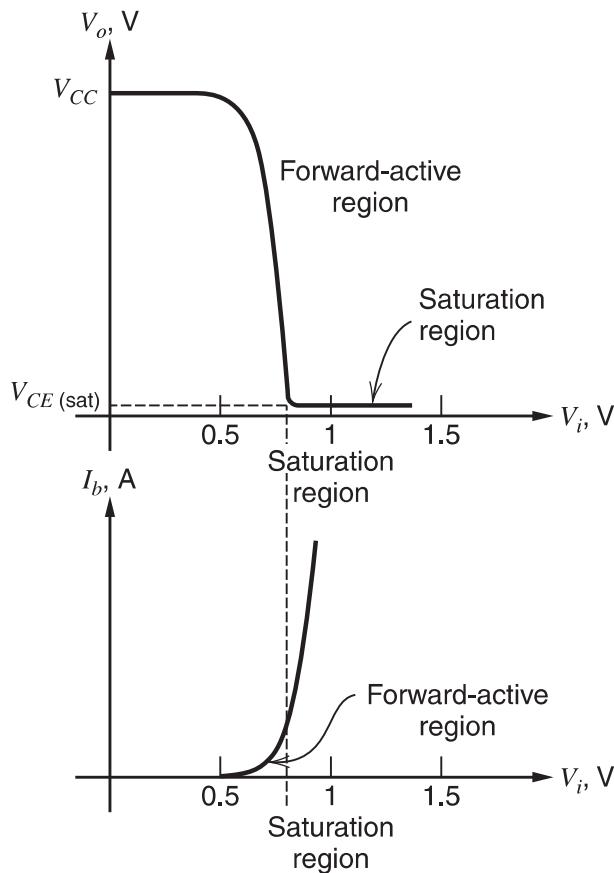


Figure 3.9 Output voltage and base current as function of V_i for the common-emitter circuit.

While incremental performance parameters such as the voltage gain can be calculated from derivatives of the large-signal analysis, the calculations are simplified by using the small-signal hybrid- π model for the transistor developed in Chapter 1. The small-signal equivalent circuit for the common-emitter amplifier is shown in Fig. 3.10. Here we have neglected r_b , assuming that it is much smaller than r_π . We have also neglected r_μ . This equivalent circuit does not include the resistance of the load connected to the amplifier output. The collector resistor R_C is included because it is usually present in some form as a biasing element. Our objective is to characterize the amplifier alone so that the voltage gain can then be calculated under arbitrary conditions of loading at the input and output. Since the common-emitter amplifier is unilateral when r_μ is neglected, we will calculate the small-signal input resistance, transconductance, and output resistance of the circuit as explained in Section 3.2.

The input resistance is the Thévenin-equivalent resistance seen looking into the input. For the CE amplifier,

$$R_i = \frac{v_i}{i_i} = r_\pi = \frac{\beta_0}{g_m} \quad (3.13)$$

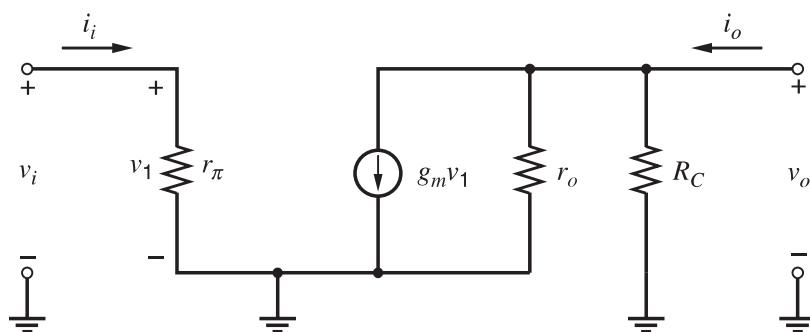


Figure 3.10 Small-signal equivalent circuit for the CE amplifier.

The transconductance G_m is the change in the short-circuit output current per unit change of input voltage and is given by

$$G_m = \frac{i_o}{v_i} \Big|_{v_o=0} = g_m \quad (3.14)$$

Equation 3.14 shows that the transconductance of the CE amplifier is equal to the transconductance of the transistor. The output resistance is the Thévenin-equivalent resistance seen looking into the output with the input shorted, or

$$R_o = \frac{v_o}{i_o} \Big|_{v_i=0} = R_C \parallel r_o \quad (3.15)$$

The *open-circuit, or unloaded, voltage gain* is

$$a_v = \frac{v_o}{v_i} \Big|_{i_o=0} = -g_m(r_o \parallel R_C) \quad (3.16)$$

If the collector load resistor R_C is made very large, then a_v becomes

$$\lim_{R_C \rightarrow \infty} a_v = -g_m r_o = -\frac{I_C}{V_T} \frac{V_A}{I_C} = -\frac{V_A}{V_T} = -\frac{1}{\eta} \quad (3.17)$$

where I_C is the dc collector current at the operating point, V_T is the thermal voltage, V_A is the Early voltage, and η is given in (1.114). This gain represents the maximum low-frequency voltage gain obtainable from the transistor. It is independent of the collector bias current for bipolar transistors, and the magnitude is approximately 5000 for typical *npn* devices.

Another parameter of interest is the *short-circuit current gain* a_i . This parameter is the ratio of i_o to i_i when the output is shorted. For the CE amplifier,

$$a_i = \frac{i_o}{i_i} \Big|_{v_o=0} = \frac{G_m v_i}{\frac{v_i}{R_i}} = g_m r_\pi = \beta_0 \quad (3.18)$$

■ EXAMPLE

(a) Find the input resistance, output resistance, voltage gain, and current gain of the common-emitter amplifier in Fig. 3.11a. Assume that $I_C = 100 \mu\text{A}$, $\beta_0 = 100$, $r_b = 0$, and $r_o \rightarrow \infty$.

$$R_i = r_\pi = \frac{\beta_0}{g_m} \simeq \frac{100 \text{ (26 mV)}}{100 \mu\text{A}} = 26 \text{ k}\Omega$$

$$R_o = R_C = 5 \text{ k}\Omega$$

$$a_v = -g_m R_C \simeq -\left(\frac{100 \mu\text{A}}{26 \text{ mV}}\right) (5 \text{ k}\Omega) \simeq -19.2$$

$$a_i = \beta_0 = 100$$

(b) Calculate the voltage gain of the circuit of Fig. 3.11b. Assume that V_{BIAS} is adjusted so that the dc collector current is maintained at $100 \mu\text{A}$.

$$v_1 = v_s \left(\frac{R_i}{R_S + R_i} \right)$$

$$v_o = -G_m v_1 (R_o \parallel R_L) = -G_m \left(\frac{R_i}{R_S + R_i} \right) (R_o \parallel R_L) v_s$$

$$\frac{v_o}{v_s} = -\left(\frac{1}{260 \Omega}\right) \left(\frac{26 \text{ k}\Omega}{26 \text{ k}\Omega + 20 \text{ k}\Omega}\right) \left[\frac{(10 \text{ k}\Omega)(5 \text{ k}\Omega)}{10 \text{ k}\Omega + 5 \text{ k}\Omega}\right] \simeq -7.25$$

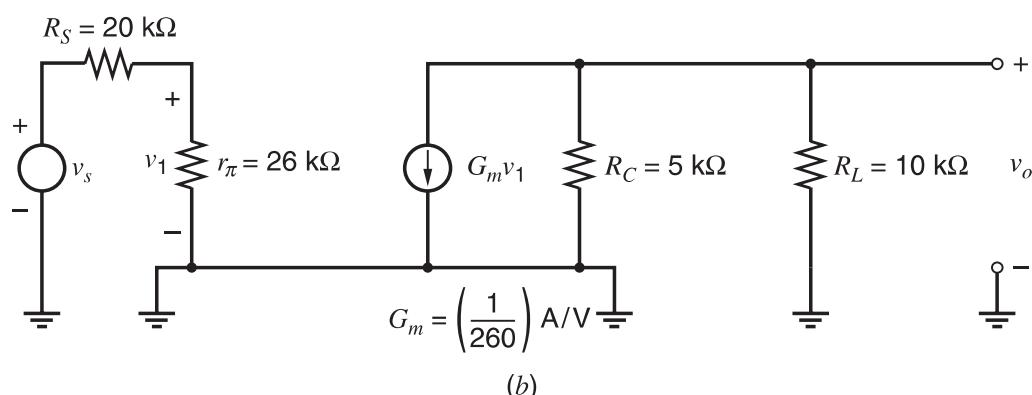
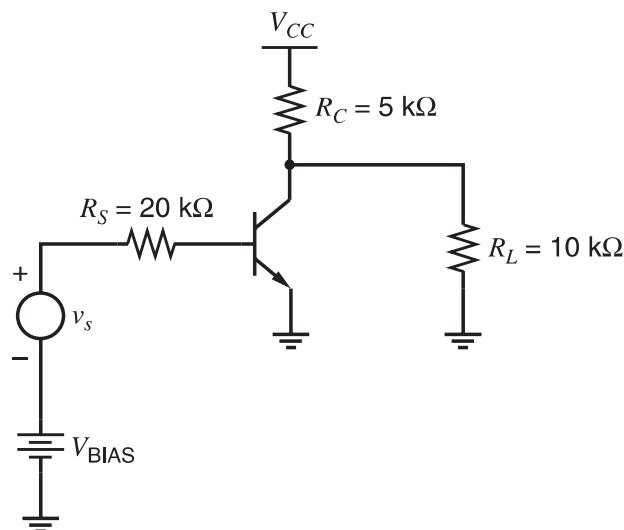
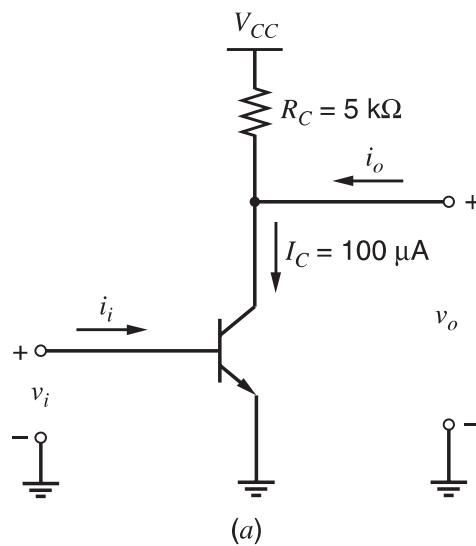


Figure 3.11 (a) Example amplifier circuit. (b) Circuit for calculation of voltage gain with typical source and load resistance values.

3.3.2 Common-Source Configuration

The resistively loaded common-source (CS) amplifier configuration is shown in Fig. 3.12a using an *n*-channel MOS transistor. The corresponding small-signal equivalent circuit is shown in Fig. 3.12b. As in the case of the bipolar transistor, the MOS transistor is cutoff for $V_i = 0$ and thus $I_d = 0$ and $V_o = V_{DD}$. As V_i is increased beyond the threshold voltage V_t , nonzero drain current flows and the transistor operates in the active region (which is often called saturation for MOS transistors) when $V_o > V_{GS} - V_t$. The large-signal model of Fig. 1.30 can then be

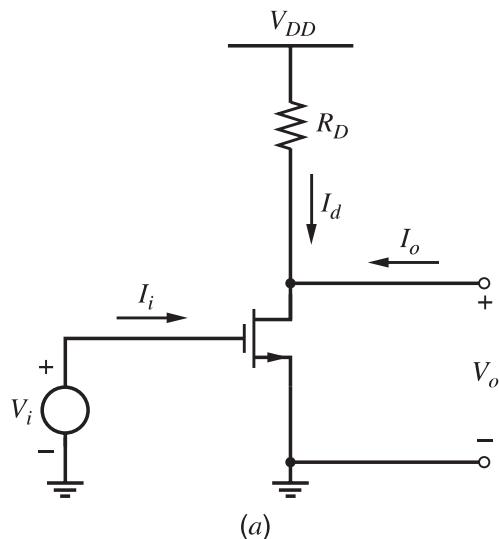
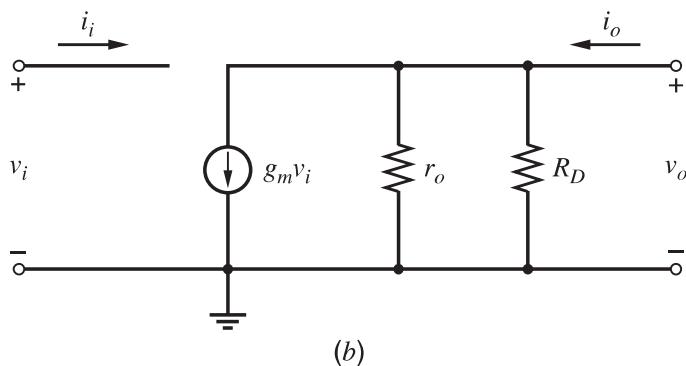


Figure 3.12 (a) Resistively loaded, common-source amplifier. (b) Small-signal equivalent circuit for the common-source amplifier.



used together with (1.157) to derive

$$V_o = V_{DD} - I_d R_D \quad (3.19)$$

$$= V_{DD} - \frac{\mu_n C_{ox}}{2} \frac{W}{L} R_D (V_i - V_t)^2 \quad (3.20)$$

The output voltage is equal to the drain-source voltage and decreases as the input increases. When $V_o < V_{GS} - V_t$, the transistor enters the triode region, where its output resistance becomes low and the small-signal voltage gain drops dramatically. In the triode region, the output voltage can be calculated by using (1.152) in (3.19). These results are illustrated in the plot of Fig. 3.13. The slope of this transfer characteristic at any operating point is the small-signal

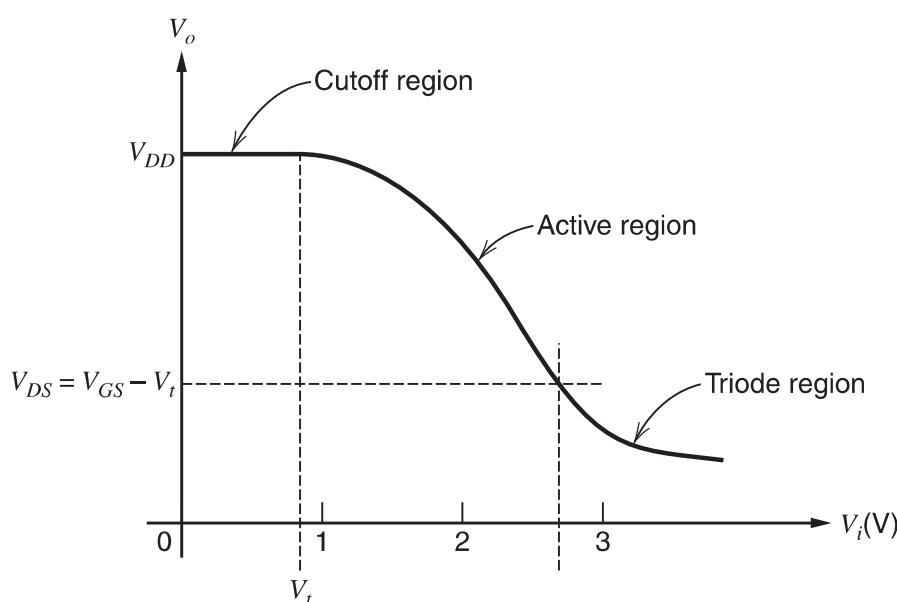


Figure 3.13 Output voltage versus input voltage for the common-source circuit.

voltage gain at that point. The MOS transistor has much lower voltage gain in the active region than does the bipolar transistor; therefore, the active region for the MOS CS amplifier extends over a much larger range of V_i than in the bipolar common-emitter amplifier.

Since the source and body of the MOS transistor both operate at ac ground, $v_{bs} = 0$ in Fig. 1.36; therefore, the g_{mb} generator is omitted in Fig. 3.12b. As a result, this circuit is topologically identical to the small-signal equivalent circuit for the common-emitter amplifier shown in Fig. 3.10. The CS amplifier is unilateral because it contains no feedback. Therefore, the low-frequency behavior of this circuit can be characterized using the transconductance, input resistance, and output resistance as described in Section 3.2.

The transconductance G_m is

$$G_m = \frac{i_o}{v_i} \Big|_{v_o=0} = g_m \quad (3.21)$$

Equation 3.21 shows that the transconductance of the CS amplifier is equal to the transconductance of the transistor, as in a common-emitter amplifier. Since the input of the CS amplifier is connected to the gate of an MOS transistor, the dc input current and its low-frequency, small-signal variation i_i are both assumed to equal zero. Under this assumption, the input resistance R_i is

$$R_i = \frac{v_i}{i_i} \rightarrow \infty \quad (3.22)$$

Another way to see this result is to let $\beta_0 \rightarrow \infty$ in (3.13) because MOS transistors behave like bipolar transistors with infinite β_0 . The output resistance is the Thévenin-equivalent resistance seen looking into the output with the input shorted, or

$$R_o = \frac{v_o}{i_o} \Big|_{v_i=0} = R_D \parallel r_o \quad (3.23)$$

The *open-circuit*, or *unloaded*, voltage gain is

$$a_v = \frac{v_o}{v_i} \Big|_{i_o=0} = -g_m(r_o \parallel R_D) \quad (3.24)$$

If the drain load resistor R_D is replaced by a current source, $R_D \rightarrow \infty$ and a_v becomes

$$\lim_{R_D \rightarrow \infty} a_v = -g_m r_o \quad (3.25)$$

Equation 3.25 gives the maximum possible voltage gain of a one-stage CS amplifier. This result is identical to the first part of (3.17) for a common-emitter amplifier. In the case of the CS amplifier, however, g_m is proportional to $\sqrt{I_D}$ from (1.180) whereas r_o is inversely proportional to I_D from (1.194). Thus, we find in (3.25) that the maximum voltage gain per stage is proportional to $1/\sqrt{I_D}$. In contrast, the maximum voltage gain in the common-emitter amplifier is independent of current. A plot of the maximum voltage gain versus I_D for a typical MOS transistor is shown in Fig. 3.14. At very low currents, the gain approaches a constant value comparable to that of a bipolar transistor. This region is sometimes called *subthreshold*, where the transistor operates in weak inversion and the square-law characteristic in (1.157) is no longer valid. As explained in Section 1.8, the drain current becomes an exponential function of the gate-source voltage in this region, resembling the collector-current dependence on the base-emitter voltage in a bipolar transistor.

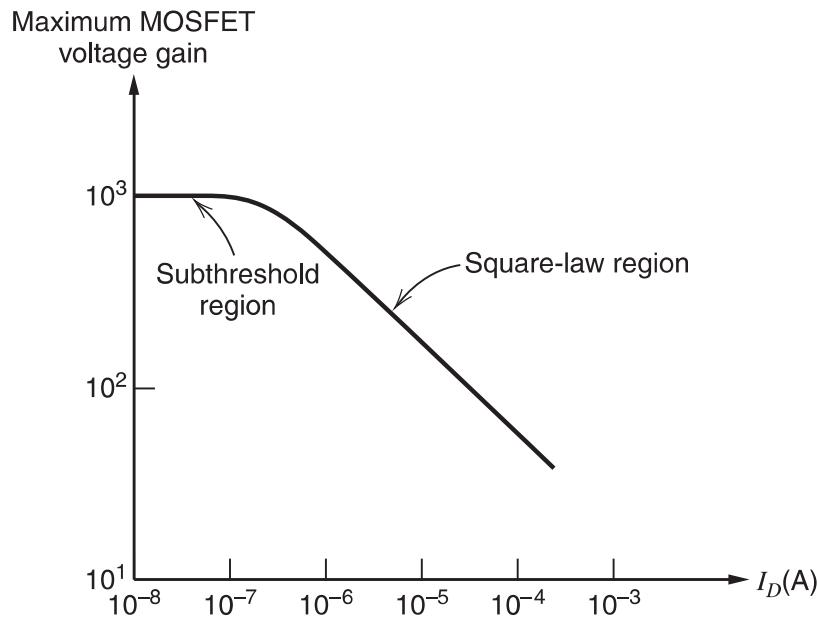


Figure 3.14 Typical variation of maximum MOSFET voltage gain with bias current.

Using (1.194), the limiting gain given by (3.25) can also be expressed as

$$\lim_{R_D \rightarrow \infty} a_v = -g_m r_o = -\frac{g_m}{I_D} I_D r_o = -\frac{g_m}{I_D} V_A \quad (3.26)$$

In the square-law region in Fig. 3.14, substituting (1.181) into (3.26) gives

$$\lim_{R_D \rightarrow \infty} a_v = -\frac{V_A}{(V_{GS} - V_t)/2} = -\frac{2V_A}{V_{ov}} \quad (3.27)$$

where $V_{ov} = V_{GS} - V_t$ is the gate *overdrive*. Since the gate overdrive is typically an order of magnitude larger than the thermal voltage V_T , the magnitude of the maximum gain predicted by (3.27) is usually much smaller than that predicted by (3.17) for the bipolar case. Substituting (1.163) into (3.27) gives

$$\lim_{R_D \rightarrow \infty} a_v = -\frac{2L_{\text{eff}}}{V_{GS} - V_t} \left(\frac{dX_d}{dV_{DS}} \right)^{-1} \quad (3.28)$$

■ EXAMPLE

Find the voltage gain of the common-source amplifier of Fig. 3.12a with $V_{DD} = 5$ V, $R_D = 5$ kΩ, $k' = \mu_n C_{ox} = 100 \mu\text{A/V}^2$, $W = 50 \mu\text{m}$, $L = 1 \mu\text{m}$, $V_t = 0.8$ V, $L_d = 0$, $X_d = 0$, and $\lambda = 0$. Assume that the bias value of V_i is 1 V.

To determine whether the transistor operates in the active region, we first find the dc output voltage $V_O = V_{DS}$. If the transistor operates in the active region, (1.157) gives

$$I_D = \frac{k' W}{2 L} (V_{GS} - V_t)^2 = \frac{100}{2} \times 10^{-6} \times \frac{50}{1} (1 - 0.8)^2 = 100 \mu\text{A}$$

Then

$$V_O = V_{DS} = V_{DD} - I_D R_D = 5 \text{ V} - (0.1 \text{ mA})(5 \text{ k}\Omega) = 4.5 \text{ V}$$

Since $V_{DS} = 4.5$ V > $V_{GS} - V_t = 0.2$ V, the transistor does operate in the active region, as assumed. Then from (1.180),

$$g_m = k' \frac{W}{L} (V_{GS} - V_t) = 100 \times 10^{-6} \times \frac{50}{1} (1 - 0.8) = 1000 \frac{\mu\text{A}}{\text{V}}$$

Then since $\lambda = 0$, $V_A \rightarrow \infty$ and (3.24) gives

$$a_v = -g_m R_D = -(1.0 \text{ mA/V}) (5 \text{ k}\Omega) = -5$$

Note that the open-circuit voltage gain here is much less than in the bipolar example in Section 3.3.1 even though the dc bias currents are equal.

3.3.3 Common-Base Configuration

In the common-base (CB) configuration,⁴ the input signal is applied to the emitter of the transistor, and the output is taken from the collector. The base is tied to ac ground. The common-base connection is shown in Fig. 3.15. While the connection is not as widely used as the common-emitter amplifier, it has properties that make it useful in certain circumstances. In this section, we calculate the small-signal properties of the common-base stage.

The hybrid- π model provides an accurate representation of the small-signal behavior of the transistor independent of the circuit configuration. For the common-base stage, however, the hybrid- π model is somewhat cumbersome because the dependent current source is connected between the input and output terminals.⁴ The analysis of common-base stages can be simplified if the model is modified as shown in Fig. 3.16. The small-signal hybrid- π model is shown in Fig. 3.16a. First note that the dependent current source flows from the collector terminal to the emitter terminal. The circuit behavior is unchanged if we replace this single current source with two current sources of the same value, one going from the collector to the base and the other going from the base to the emitter, as shown in Fig. 3.16b. Since the currents fed into and removed from the base are equal, the equations that describe the operation of these circuits are identical. We next note that the controlled current source connecting the base and emitter is controlled by the voltage across its own terminals. Therefore, by the application of Ohm's law to this branch, this dependent current source can be replaced by a resistor of value $1/g_m$. This resistance appears in parallel with r_π , and the parallel combination of the two is called the emitter resistance r_e .

$$r_e = \frac{1}{g_m + \frac{1}{r_\pi}} = \frac{1}{g_m \left(1 + \frac{1}{\beta_0}\right)} = \frac{\alpha_0}{g_m} \quad (3.29)$$

The new equivalent circuit is called the *T model* and is shown in Fig. 3.16c. It has terminal properties exactly equivalent to those of the hybrid- π model but is often more convenient to use for common-base calculations. For dc and low input frequencies, the capacitors C_π and C_μ appear as high-impedance elements and can be neglected. Assume at first that $r_b = 0$ and $r_o \rightarrow \infty$ so that the circuit is unilateral. When r_μ is also neglected, the model reduces to the simple form shown in Fig. 3.16d. Using the T model under these conditions, the small-signal

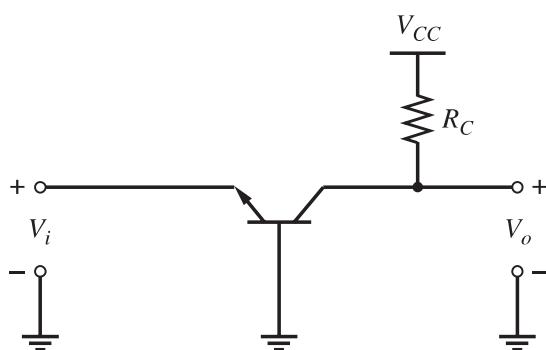


Figure 3.15 Typical common-base amplifier.

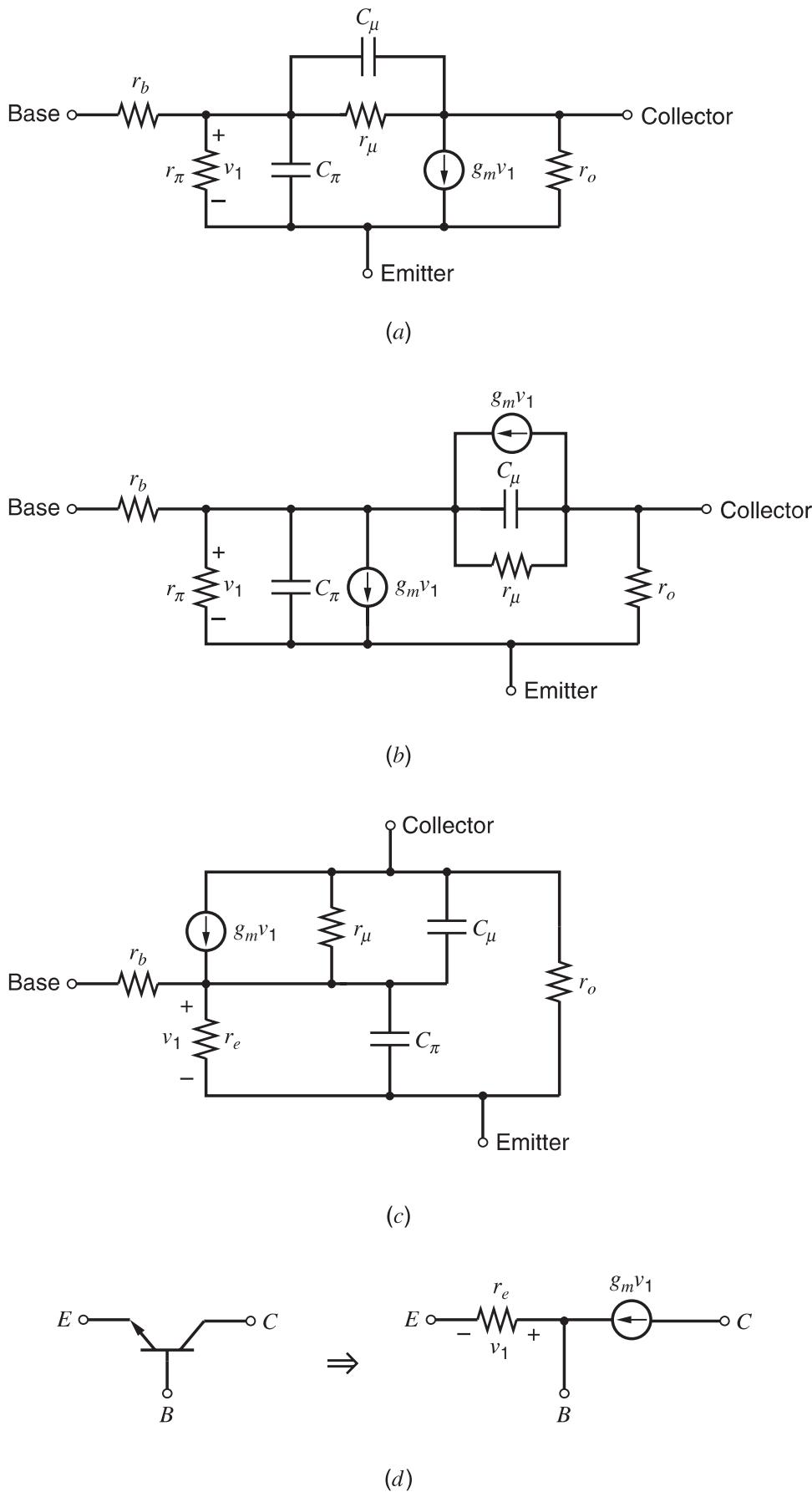


Figure 3.16 Generation of emitter-current-controlled T model from the hybrid- π . (a) Hybrid- π model. (b) The collector current source $g_m v_1$ is changed to two current sources in series, and the point between them attached to the base. This change does not affect the current flowing in the base. (c) The current source between base and emitter is converted to a resistor of value $1/g_m$. (d) T model for low frequencies, neglecting r_o , r_μ , and the charge-storage elements.

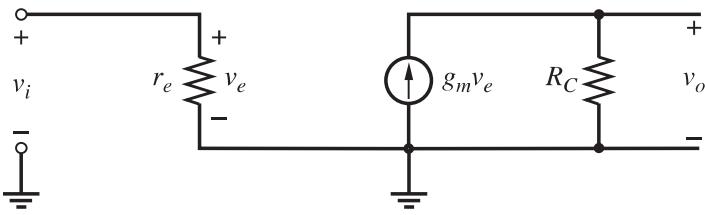


Figure 3.17 Small-signal equivalent circuit of the common-base stage; r_o , r_b , and r_μ are assumed negligible.

equivalent circuit of the common-base stage is shown in Fig. 3.17. By inspection of Fig. 3.17, the short-circuit transconductance is

$$G_m = g_m \quad (3.30)$$

The input resistance is just the resistance r_e :

$$R_i = r_e \quad (3.31)$$

The output resistance is given by

$$R_o = R_C \quad (3.32)$$

Using these parameters, the open-circuit voltage gain and the short-circuit current gain are

$$a_v = G_m R_o = g_m R_C \quad (3.33)$$

$$a_i = G_m R_i = g_m r_e = \alpha_0 \quad (3.34)$$

Comparing (3.31) and (3.13) shows that the input resistance of the common-base configuration is a factor of $(\beta_0 + 1)$ less than in the common-emitter configuration. Also, comparing (3.34) and (3.18) shows that the current gain of the common-base configuration is reduced by a factor of $(\beta_0 + 1)$ compared to that of the common-emitter configuration.

Until now, we have assumed that r_b is negligible. In practice, however, the base resistance has a significant effect on the transconductance and the input resistance when the common-base stage is operated at sufficiently high current levels. To recalculate these parameters with $r_b > 0$, assume the transistor operates in the forward-active region and consider the small-signal model shown in Fig. 3.18. Here, the transconductance is

$$G_m = \frac{i_o}{v_i} \Big|_{v_o=0} = g_m \left(\frac{v_e}{v_i} \right) \quad (3.35)$$

To find the relationship between v_e and v_i , Kirchoff's current law (KCL) and Kirchoff's voltage law (KVL) can be applied at the internal base node (node ①) and around the input loop, respectively. From KCL at node ①,

$$g_m v_e + \frac{v_b}{r_b} - \frac{v_e}{r_e} = 0 \quad (3.36)$$

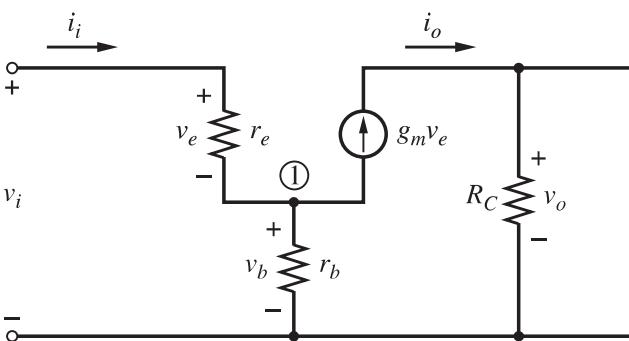


Figure 3.18 Small-signal model of the common-base stage with $r_b > 0$.

From KVL around the input loop,

$$v_i = v_e + v_b \quad (3.37)$$

Solving (3.37) for v_b , substituting into (3.36), and rearranging gives

$$\frac{v_i}{v_e} = 1 + \frac{g_m}{\beta_0} r_b = 1 + \frac{r_b}{r_\pi} \quad (3.38)$$

Substituting (3.38) into (3.35) gives

$$G_m = \frac{g_m}{1 + \frac{r_b}{r_\pi}} \quad (3.39)$$

Similarly, the input resistance in Fig. 3.18 is

$$R_i = \frac{v_i}{i_i} = \frac{v_i}{v_e/r_e} = r_e \left(\frac{v_i}{v_e} \right) \quad (3.40)$$

Substituting (3.38) into (3.40) gives

$$R_i = r_e \left(1 + \frac{r_b}{r_\pi} \right) = \frac{\alpha_0}{g_m} \left(1 + \frac{r_b}{r_\pi} \right) \quad (3.41)$$

Thus if the dc collector current is large enough that r_π is comparable with r_b , then the effects of base resistance must be included. For example, if $r_b = 100 \Omega$ and $\beta_0 = 100$, then a collector current of 26 mA makes r_b and r_π equal.

The main motivation for using common-base stages is twofold. First, the collector-base capacitance does not cause high-frequency feedback from output to input as in the common-emitter amplifier. As described in Chapter 7, this change can be important in the design of high-frequency amplifiers. Second, as described in Chapter 4, the common-base amplifier can achieve much larger output resistance than the common-emitter stage in the limiting case where $R_C \rightarrow \infty$. As a result, the common-base configuration can be used as a current source whose current is nearly independent of the voltage across it.

3.3.4 Common-Gate Configuration

In the common-gate configuration, the input signal is applied to the source of the transistor, and the output is taken from the drain while the gate is connected to ac ground. This configuration is shown in Fig. 3.19, and its behavior is similar to that of a common-base stage.

As in the analysis of common-base amplifiers in Section 3.3.3, the analysis of common-gate amplifiers can be simplified if the model is changed from a hybrid- π configuration to a T model, as shown in Fig. 3.20. In Fig. 3.20a, the low-frequency hybrid- π model is shown. Note that both transconductance generators are now active. If the substrate or body connection is assumed to operate at ac ground, then $v_{bs} = v_{gs}$ because the gate also operates at ac ground.

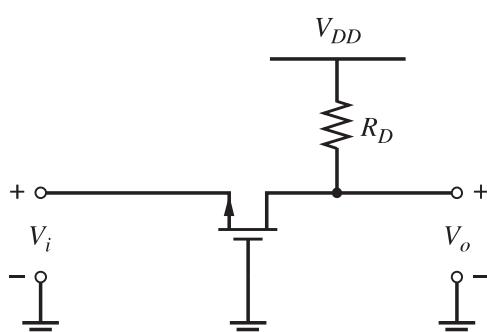


Figure 3.19 Common-gate configuration.

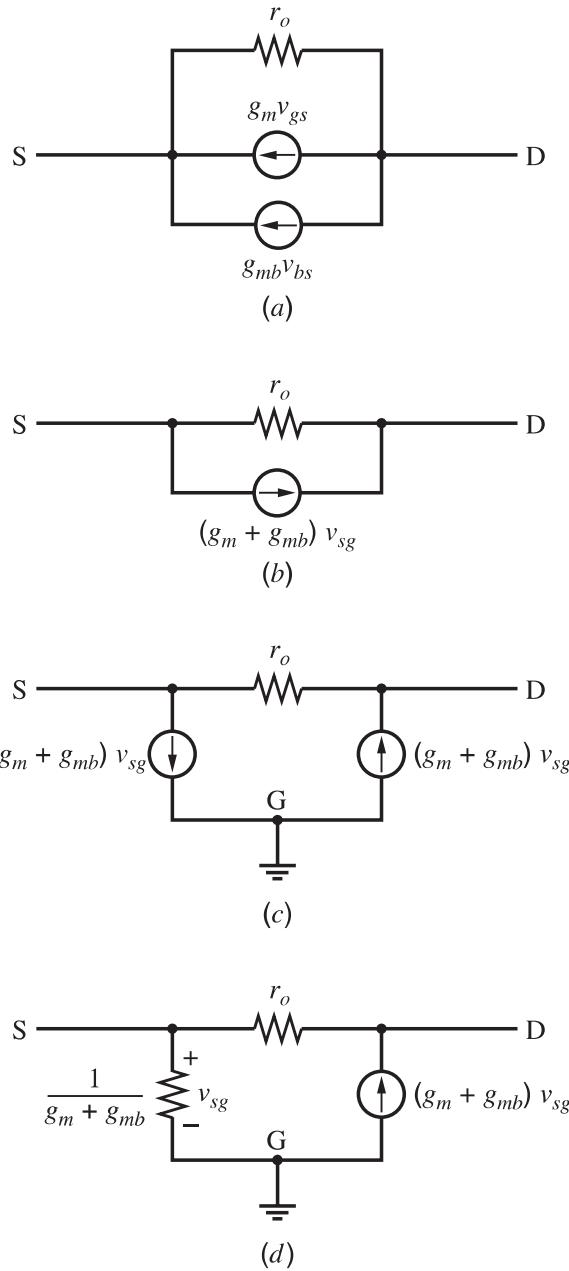


Figure 3.20 Conversion from hybrid- π to T model.
 (a) Low-frequency hybrid- π model. (b) The two dependent sources are combined. (c) The combined source is converted into two sources. (d) The current source between the source and gate is converted into a resistor.

Therefore, in Fig. 3.20b, the two dependent current sources are combined. In Fig. 3.20c, the combined current source from the source to the drain is replaced by two current sources: one from the source to the gate and the other from the gate to the drain. Since equal currents are pushed into and pulled out of the gate, the equations that describe the operation of the circuits in Figs. 3.20b and 3.20c are identical. Finally, because the current source from the source to the gate is controlled by the voltage across itself, it can be replaced by a resistor of value $1/(g_m + g_{mb})$, as in Fig. 3.20d.

If r_o is finite, the circuit of Fig. 3.20d is bilateral because of feedback provided through r_o . At first, we will assume that $r_o \rightarrow \infty$ so that the circuit is unilateral. Using the T model under these conditions, the small-signal equivalent circuit of the common-gate stage is shown in Fig. 3.21. By inspection of Fig. 3.21,

$$G_m = g_m + g_{mb} \quad (3.42)$$

$$R_i = \frac{1}{g_m + g_{mb}} \quad (3.43)$$

$$R_o = R_D \quad (3.44)$$

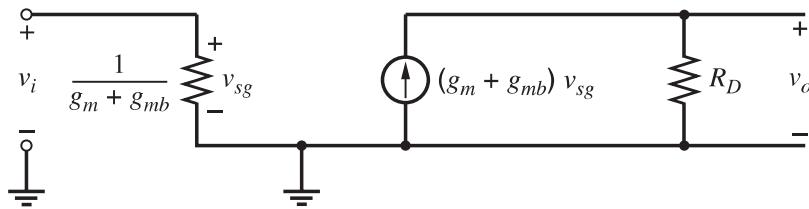


Figure 3.21 Small-signal equivalent circuit of the common-gate stage; r_o is assumed negligible.

Using these parameters, the open-circuit voltage gain and the short-circuit current gain are

$$a_v = G_m R_o = (g_m + g_{mb}) R_D \quad (3.45)$$

$$a_i = G_m R_i = 1 \quad (3.46)$$

3.3.5 Common-Base and Common-Gate Configurations with Finite r_o

In calculating the expressions for G_m , R_i , and R_o of the common-base and common-gate amplifiers, we have neglected the effects of r_o . Since r_o is connected from each amplifier output back to its input, finite r_o causes each circuit to be bilateral, making the input resistance depend on the connection at the amplifier output. Let $R = R_C$ in Fig. 3.17 or $R = R_D$ in Fig. 3.21, depending on which circuit is under consideration. When R becomes large enough that it is comparable with r_o , r_o must be included in the small-signal model to accurately predict not only the input resistance, but also the output resistance. On the other hand, since the transconductance is calculated with the output shorted, the relationship between r_o and R has no effect on this calculation, and the effect of finite r_o on transconductance can be ignored if $r_o \gg 1/G_m$.

3.3.5.1 Common-Base and Common-Gate Input Resistance

Figure 3.22a shows a small-signal T model of a common-base or common-gate stage including finite r_o , where $R_{i(\text{ideal})}$ is given by (3.31) for a common-base amplifier or by (3.43) for a common-gate amplifier. Also, R represents R_C in Fig. 3.17 or R_D in Fig. 3.21. Connections to the load and the input source are shown in Fig. 3.22a to include their contributions to the input and output resistance, respectively. In Fig. 3.22a, the input resistance is $R_i = v_1/i_1$. To find the input resistance, a simplified equivalent circuit such as in Fig. 3.22b is often used. Here, a test voltage source v_t is used to drive the amplifier input, and the resulting test current i_t is calculated. KCL at the output node in Fig. 3.22b gives

$$\frac{v_o}{R \parallel R_L} + \frac{v_o - v_t}{r_o} = G_m v_t \quad (3.47)$$

KCL at the input in Fig. 3.22b gives

$$i_t = \frac{v_t}{R_{i(\text{ideal})}} + \frac{v_t - v_o}{r_o} \quad (3.48)$$

Solving (3.47) for v_o and substituting into (3.48) gives

$$\frac{i_t}{v_t} = \frac{1}{R_{i(\text{ideal})}} + \frac{1}{r_o} \left(1 - \frac{\frac{G_m + \frac{1}{r_o}}{1}}{\frac{1}{R \parallel R_L} + \frac{1}{r_o}} \right) \quad (3.49)$$

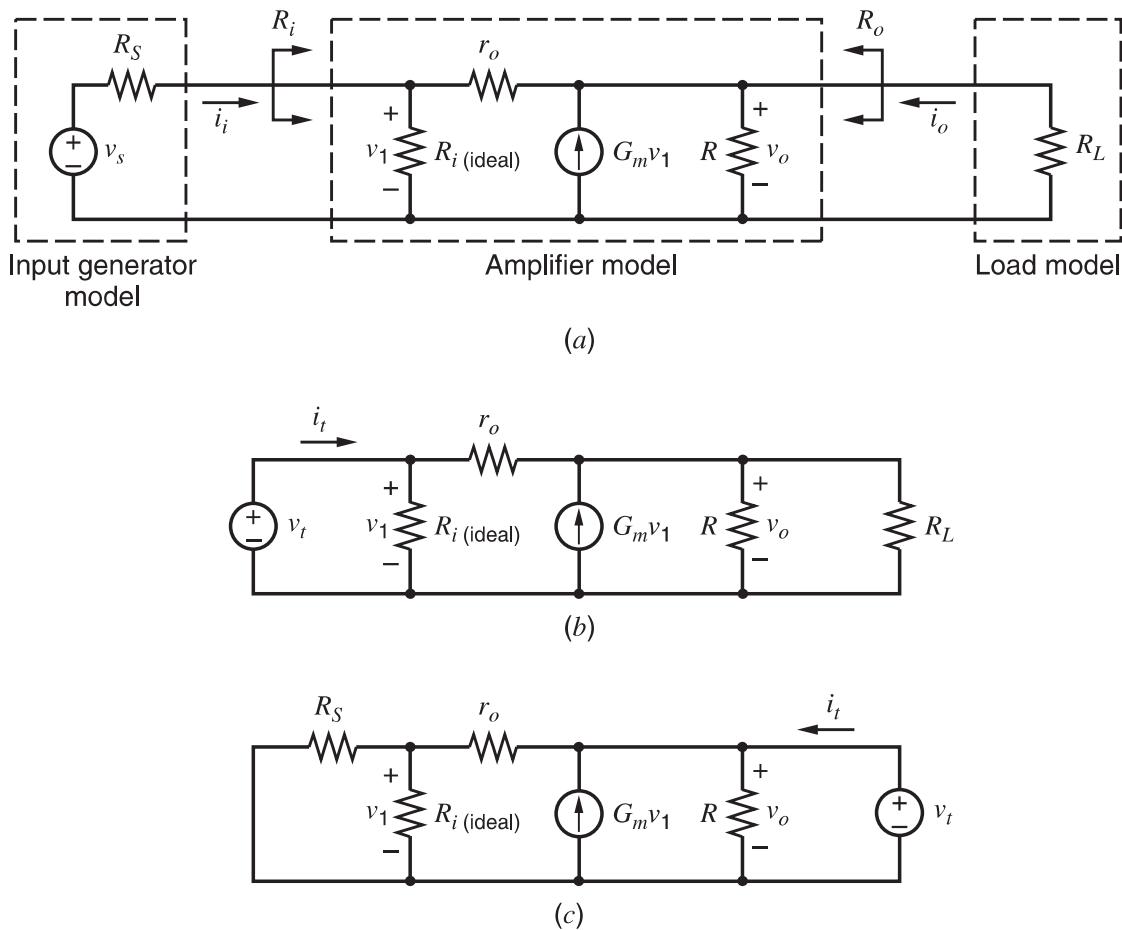


Figure 3.22 (a) Model of common-base and common-gate amplifiers with finite r_o , showing connections to the input source and load. (b) Equivalent circuit for calculation of R_i . (c) Equivalent circuit for calculation of R_o .

Rearranging (3.49) gives

$$R_i = \frac{v_t}{i_t} = \frac{r_o + R \parallel R_L}{1 - G_m(R \parallel R_L) + \frac{r_o + R \parallel R_L}{R_{i(\text{ideal})}}} \quad (3.50)$$

Common-Base Input Resistance. For the common-base amplifier, $G_m = g_m$ from (3.30), and $R_{i(\text{ideal})} = r_e = \alpha_0/g_m$ from (3.31). Substituting (3.30) and (3.31) into (3.50) with $R = R_C$ and rearranging gives

$$R_i = \frac{v_t}{i_t} = \frac{r_o + R_C \parallel R_L}{1 + \frac{g_m(R_C \parallel R_L)}{\beta_0} + \frac{g_m r_o}{\alpha_0}} = \frac{r_o + R_C \parallel R_L}{1 + \frac{g_m}{\beta_0} (R_C \parallel R_L + (\beta_0 + 1) r_o)} \quad (3.51)$$

From (3.51), when $(\beta_0 + 1)r_o \gg R_C \parallel R_L$,

$$\alpha_0? \alpha_0 = 1 \quad R_i \simeq \frac{r_o + R_C \parallel R_L}{1 + \frac{g_m r_o}{\alpha_0}} \quad \text{cosas de la tala idea} \quad (3.52)$$

From (3.52), when $g_m r_o \gg \alpha_0$,

$$R_i \simeq \frac{\alpha_0}{g_m} + \frac{\alpha_0 (R_C \parallel R_L)}{g_m r_o} = \frac{||}{r_e} + \frac{\alpha_0 (R_C \parallel R_L)}{g_m r_o} \quad (3.53)$$

The first term on the right side of (3.53) is the same as in (3.31), where the common-base amplifier was unilateral because infinite r_o was assumed. The second term shows that the input resistance now depends on the connection to the output (because finite r_o provides feedback and makes the amplifier bilateral). The second term is about equal to the resistance at the amplifier output divided by the $G_m r_o$ product. When $r_o \gg (R_C \parallel R_L)$, the effect of the second term can be neglected.

r_0 muestrea tensión. ¿Suma corriente o suma tensión? Creo que suma tensión

Common-Gate Input Resistance. For the common-gate amplifier, $G_m = (g_m + g_{mb})$ from (3.42) and $R_{i(\text{ideal})} = 1/(g_m + g_{mb})$ from (3.43). Substituting (3.42) and (3.43) into (3.50) with $R = R_D$ and rearranging gives

$$\left\{ \begin{array}{l} g_{mb} ? \rightarrow \frac{\partial I_D}{\partial v_{BS}} = 0 \\ \text{para mas otros} \end{array} \right. \quad R_i = \frac{v_t}{i_t} = \frac{r_o + R_D \parallel R_L}{1 + (g_m + g_{mb}) r_o} \quad (3.54)$$

When $(g_m + g_{mb}) r_o \gg 1$,

$$R_i \approx \frac{1}{g_m + g_{mb}} + \frac{R_D \parallel R_L}{(g_m + g_{mb}) r_o} \quad (3.55)$$

The first term on the right side of (3.55) is the same as in (3.43), where the common-gate amplifier was unilateral because infinite r_o was assumed. The second term is about equal to the resistance at the amplifier output divided by the $G_m r_o$ product and shows the effect of finite r_o , which makes the circuit bilateral. When $r_o \gg (R_D \parallel R_L)$, the effect of the second term can be neglected. Neglecting the second term usually causes only a small error when R_D here or R_C in the common-base case is built as a physical resistor even if the amplifier is unloaded ($R_L \rightarrow \infty$). However, when R_D or R_C is replaced by a transistor current source, the effect of the second term can be significant. Chapter 4 describes techniques used to construct transistor current sources that can have very high equivalent resistance.

3.3.5.2 Common-Base and Common-Gate Output Resistance

The output resistance in Fig. 3.22a is $R_o = v_o/i_o$ with $v_s = 0$. For this calculation, consider the equivalent circuit shown in Fig. 3.22c, where $v_s = 0$. A test voltage v_t is used to drive the amplifier output, and the resulting test current i_t can be calculated. Since R appears in parallel with the amplifier output, the calculation will be done in two steps. First, the output resistance with $R \rightarrow \infty$ is calculated. Second, this result is placed in parallel with R to give the overall output resistance. From KCL at the input node in Fig. 3.22c,

$$\frac{v_1}{R_S} + \frac{v_1}{R_{i(\text{ideal})}} + \frac{v_1 - v_t}{r_o} = 0 \quad (3.56)$$

With $R \rightarrow \infty$, KCL at the output node gives

$$i_t = -G_m v_1 + \frac{v_t - v_1}{r_o} \quad (3.57)$$

Solving (3.56) for v_1 and substituting into (3.57) gives

$$\frac{i_t}{v_t} = \frac{1}{r_o} - \frac{1}{r_o} \left(\frac{\frac{G_m + \frac{1}{r_o}}{\frac{1}{R_S} + \frac{1}{R_{i(\text{ideal})}} + \frac{1}{r_o}}}{\frac{1}{R_S} + \frac{1}{R_{i(\text{ideal})}} + \frac{1}{r_o}} \right) \quad (3.58)$$

Rearranging (3.58) gives

$$\frac{v_t}{i_t} = \frac{r_o \left(\frac{1}{R_S} + \frac{1}{R_{i(\text{ideal})}} + \frac{1}{r_o} \right)}{\frac{1}{R_S} + \frac{1}{R_{i(\text{ideal})}} - G_m} \quad (3.59)$$

With finite R , the output resistance is

$$R_o = R \parallel \left(\frac{v_t}{i_t} \right) = R \parallel \left[\frac{r_o \left(\frac{1}{R_S} + \frac{1}{R_{i(\text{ideal})}} + \frac{1}{r_o} \right)}{\frac{1}{R_S} + \frac{1}{R_{i(\text{ideal})}} - G_m} \right] \quad (3.60)$$

Common-Base Output Resistance. For the common-base amplifier, $G_m = g_m$ from (3.30) and $R_{i(\text{ideal})} = r_e = \alpha_0/g_m$ from (3.31). Substituting (3.30) and (3.31) into (3.60) and rearranging gives

$$R_o = R \parallel \left[\frac{r_o + R_S \left(1 + \frac{g_m r_o}{\alpha_0} \right)}{1 + \frac{R_S}{r_\pi}} \right] \quad (3.61)$$

The term in brackets on the right side of (3.61) shows that the output resistance of the common-base amplifier depends on the resistance of the input source R_S when r_o is finite. For example, if the input comes from an ideal voltage source, $R_S = 0$ and

$$R_o = R \parallel r_o \quad (3.62)$$

On the other hand, if the input comes from an ideal current source, $R_S \rightarrow \infty$ and

$$R_o = R \parallel \left[\left(\frac{1 + g_m r_o}{\alpha_0} \right) r_\pi \right] \quad (3.63)$$

From (3.61), when $R_S \ll r_\pi$,

$$R_o \simeq R \parallel \left[r_o + R_S \left(\frac{1 + g_m r_o}{\alpha_0} \right) \right] \quad (3.64)$$

From (3.64), when $g_m r_o \gg \alpha_0$ and $g_m R_S \gg \alpha_0$,

$$R_o \simeq R \parallel \left(\frac{g_m r_o}{\alpha_0} R_S \right) \quad (3.65)$$

The term in parentheses in (3.65) is about equal to the input source resistance multiplied by the $G_m r_o$ product. Therefore, (3.65) and (3.53) together show that the common-base amplifier can be thought of as a resistance scaler, where the resistance is scaled up from the emitter to the collector and down from the collector to the emitter by a factor approximately equal to the $G_m r_o$ product in each case.

Common-Gate Output Resistance. For the common-gate amplifier, $G_m = (g_m + g_{mb})$ from (3.42) and $R_{i(\text{ideal})} = 1/(g_m + g_{mb})$ from (3.43). Substituting (3.42) and (3.43) into (3.60) and rearranging gives

$$R_o = R \parallel [r_o + R_S (1 + (g_m + g_{mb}) r_o)] \quad (3.66)$$

From (3.66), when $(g_m + g_{mb}) r_o \gg 1$ and $(g_m + g_{mb}) R_S \gg 1$,

$$R_o \simeq R \parallel ((g_m + g_{mb}) r_o R_S) \quad (3.67)$$

The term in parentheses in (3.67) is equal to the input source resistance multiplied by the $G_m r_o$ product. Therefore, (3.67) and (3.55) together show that the common-gate amplifier is also a resistance scaler, where the resistance is scaled up from the source to the drain and down from the drain to the source by a factor approximately equal to the $G_m r_o$ product in each case.

~~Básicamente hay 4 planteamientos de jode~~

3.3.6 Common-Collector Configuration (Emitter Follower)

The common-collector connection is shown in Fig. 3.23a. The distinguishing feature of this configuration is that the signal is applied to the base and the output is taken from the emitter.⁴ From a large-signal standpoint, the output voltage is equal to the input voltage minus the base-emitter voltage. Since the base-emitter voltage is a logarithmic function of the collector current, the base-emitter voltage is almost constant even when the collector current varies. If the base-emitter voltage were exactly constant, the output voltage of the common-collector amplifier would be equal to the input voltage minus a constant offset, and the small-signal gain of the circuit would be unity. For this reason, the circuit is also known as an *emitter follower* because the emitter voltage follows the base voltage. In practice, the base-emitter voltage is not exactly constant if the collector current varies. For example, (1.82) shows that the base-emitter voltage must increase by about 18 mV to double the collector current and by about 60 mV to increase the collector current by a factor of 10 at room temperature. Furthermore, even if the collector current were exactly constant, the base-emitter voltage depends to some extent on the collector-emitter voltage if the Early voltage is finite. These effects are most easily studied using small-signal analysis.

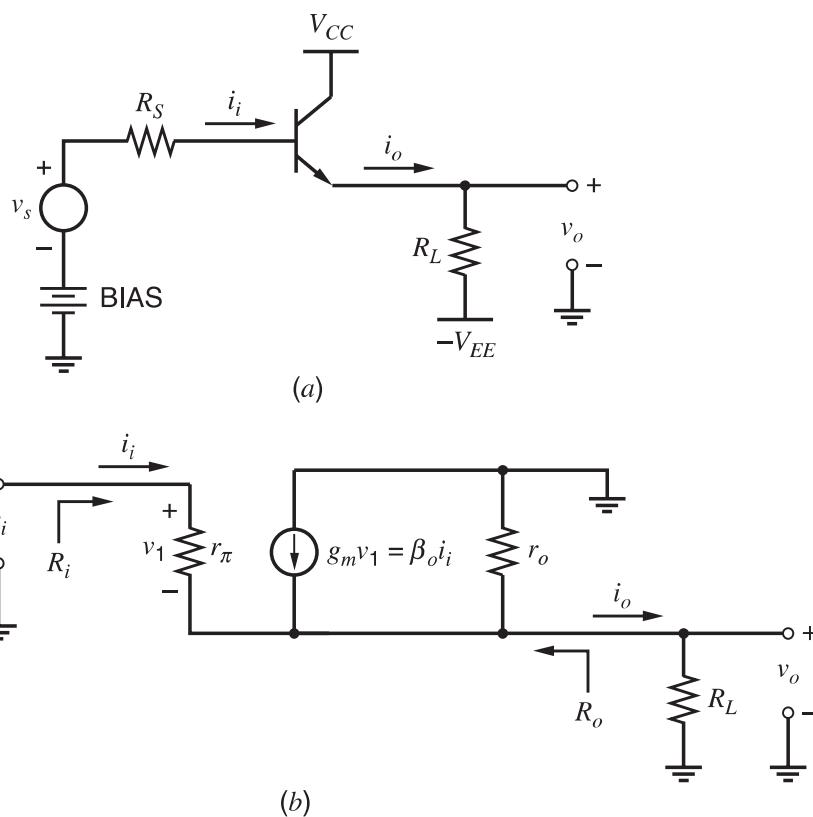


Figure 3.23 (a) Common-collector configuration. (b) Small-signal equivalent circuit of the emitter-follower circuit including R_L and R_S .

The appropriate small-signal transistor model is the hybrid- π , and the small-signal equivalent circuit is shown in Fig. 3.23b. When the input voltage v_s increases, the base-emitter voltage of the transistor increases, which increases the output current i_o . However, increasing i_o increases the output voltage v_o , which decreases the base-emitter voltage by negative feedback. Negative feedback is covered thoroughly in Chapter 8. The key point here is that the common-collector configuration is not unilateral. As a result, the input resistance depends on the load resistor R_L and the output resistance depends on the source resistance R_S . Therefore, the characterization of the emitter follower by the corresponding equivalent two-port network is not particularly useful for intuitive understanding. Instead, we will analyze the entire emitter-follower circuit of Fig. 3.23b, including both the source resistance R_S and the load resistor R_L . From KCL at the output node, we find

$$\frac{v_s - v_o}{R_S + r_\pi} + \beta_0 \left(\frac{v_s - v_o}{R_S + r_\pi} \right) - \frac{v_o}{R_L} - \frac{v_o}{r_o} = 0 \quad (3.68)$$

from which we find

$$\frac{v_o}{v_s} = \frac{1}{1 + \frac{R_S + r_\pi}{(\beta_0 + 1)(R_L \parallel r_o)}} \quad (3.69)$$

If the base resistance r_b is significant, it can simply be added to R_S in these expressions. The voltage gain is always less than unity and will be close to unity if $\beta_0 (R_L \parallel r_o) \gg (R_S + r_\pi)$. In most practical circuits, this condition holds. Note that because we have included the source resistance in this calculation, the value of v_o/v_s is not analogous to a_v calculated for the CE and CB stages. When $r_\pi \gg R_S$, $\beta_0 \gg 1$, and $r_o \gg R_L$, (3.69) can be approximated as

$$\frac{v_o}{v_s} \approx \frac{g_m R_L}{1 + g_m R_L} \quad (3.70)$$

We calculate the input resistance R_i by removing the input source, driving the input with a test current source i_t , and calculating the resulting voltage v_t across the input terminals. The circuit used to do this calculation is shown in Fig. 3.24a. From KCL at the output node,

$$\frac{v_o}{R_L} + \frac{v_o}{r_o} = i_t + \beta_0 i_t \quad (3.71)$$

Then the voltage v_t is

$$v_t = i_t r_\pi + v_o = i_t r_\pi + \frac{i_t + \beta_0 i_t}{\frac{1}{R_L} + \frac{1}{r_o}} \quad (3.72)$$

and thus

$$R_i = \frac{v_t}{i_t} = r_\pi + (\beta_0 + 1)(R_L \parallel r_o) \quad (3.73)$$

A general property of emitter followers is that the resistance looking into the base is equal to r_π plus $(\beta_0 + 1)$ times the incremental resistance connected from the emitter to small-signal ground. The factor of $\beta_0 + 1$ in (3.73) stems from the current gain of the common-collector configuration from the base to the emitter, which increases the voltage drop on the resistance connected from the emitter to small-signal ground and its contribution to the test voltage v_t in (3.72).

We now calculate the output resistance R_o by removing the load resistance R_L and finding the Thévenin-equivalent resistance looking into the output terminals. We can do this by either inserting a test current and calculating the resulting voltage or applying a test voltage and

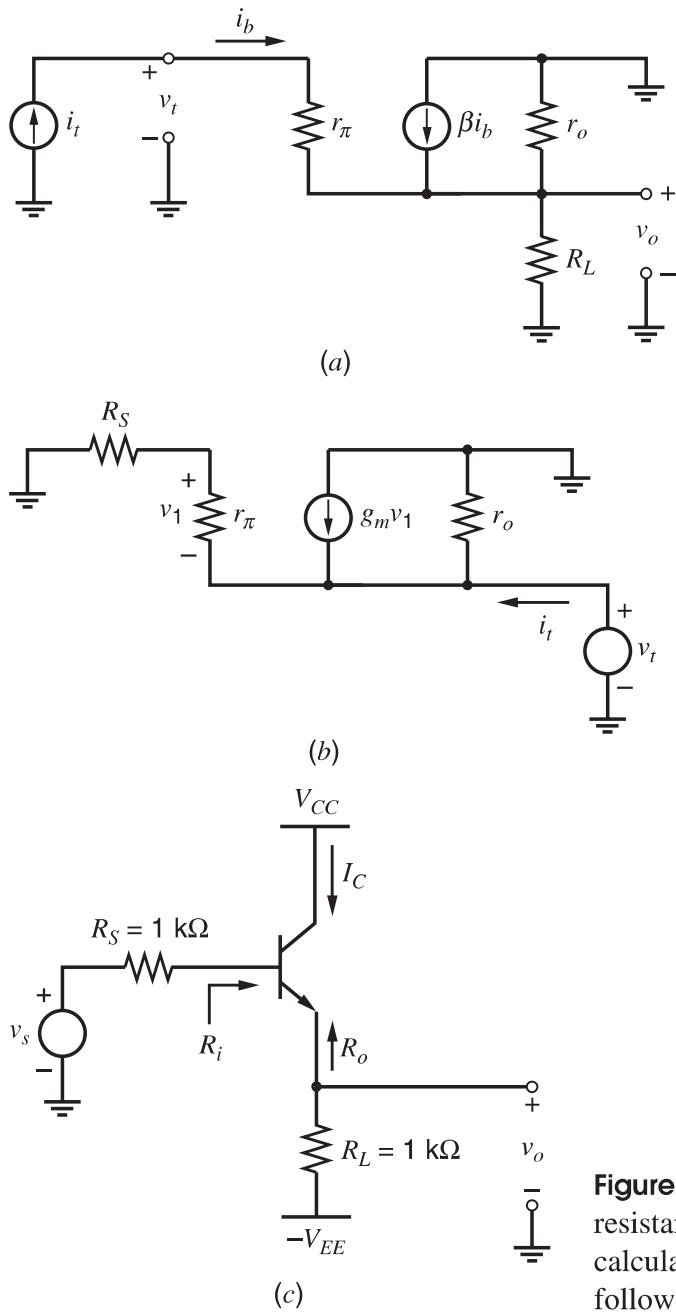


Figure 3.24 (a) Circuit for calculation of the input resistance of the emitter follower. (b) Circuit for calculation of the output resistance of the emitter follower. (c) Example emitter follower.

calculating the current. In this case, the calculation is simpler if a test voltage v_t is applied as shown in Fig. 3.24b. The voltage v_1 is given by

$$v_1 = -v_t \left(\frac{r_\pi}{r_\pi + R_S} \right) \quad (3.74)$$

The total output current i_t is thus

$$i_t = \frac{v_t}{r_\pi + R_S} + \frac{v_t}{r_o} + g_m v_t \left(\frac{r_\pi}{r_\pi + R_S} \right) \quad (3.75)$$

Therefore,

$$R_o = \frac{v_t}{i_t} = \left(\frac{r_\pi + R_S}{\beta_0 + 1} \right) \parallel r_o \quad (3.76)$$

If $\beta_0 \gg 1$ and $r_o \gg (1/g_m) + R_S/(\beta_0 + 1)$,

$$R_o \simeq \frac{1}{g_m} + \frac{R_S}{\beta_0 + 1} \quad (3.77)$$

Equation 3.77 shows that the resistance at the output is about equal to the resistance in the base lead, divided by $(\beta_0 + 1)$, plus $1/g_m$. In (3.77), R_S is divided by $\beta_0 + 1$ because the base current flows in R_S , and the base current is $\beta_0 + 1$ times smaller than the emitter current.

Therefore, the emitter follower has high input resistance, low output resistance, and near-unity voltage gain. It is most widely used as an impedance transformer to reduce loading of a preceding signal source by the input impedance of a following stage. It also finds application as a unity-voltage-gain level shift because the dc output voltage is shifted from the dc input voltage by $V_{BE(on)}$.

■ EXAMPLE

Calculate the input resistance, output resistance, and voltage gain of the emitter follower of Fig. 3.24c. Assume that $\beta_0 = 100$, $r_b = 0$, $r_o \rightarrow \infty$, and $I_C = 100 \mu\text{A}$.

$$R_i = r_\pi + R_L (1 + \beta_0) = 26 \text{ k}\Omega + (1 \text{ k}\Omega)(101) = 127 \text{ k}\Omega$$

$$\frac{v_o}{v_s} = \frac{1}{1 + \frac{r_\pi + R_S}{(\beta_0 + 1)R_L}} = \frac{1}{1 + \frac{26 \text{ k}\Omega + 1 \text{ k}\Omega}{(101)(1 \text{ k}\Omega)}} \simeq 0.79$$

$$R_o = \frac{R_S + r_\pi}{1 + \beta_0} = \frac{1 \text{ k}\Omega + 26 \text{ k}\Omega}{101} \simeq 270 \Omega$$

3.3.7 Common-Drain Configuration (Source Follower)

The common-drain configuration is shown in Fig. 3.25a. The input signal is applied to the gate and the output is taken from the source. From a large-signal standpoint, the output voltage is equal to the input voltage minus the gate-source voltage. The gate-source voltage consists of two parts: the threshold and the overdrive. If both parts are constant, the resulting output

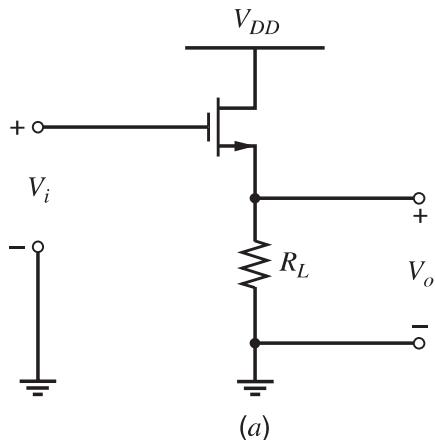
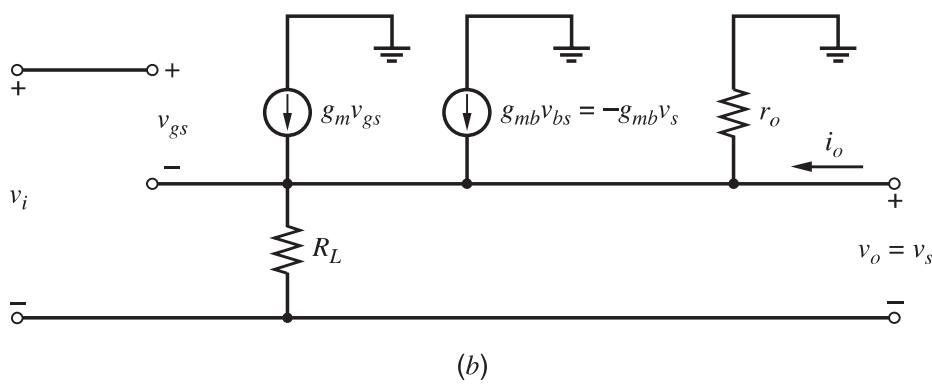


Figure 3.25 (a) Common-drain configuration. (b) Small-signal equivalent circuit of the common-drain configuration.



voltage is simply offset from the input, and the small-signal gain would be unity. Therefore, the source follows the gate, and the circuit is also known as a *source follower*. In practice, the body effect changes the threshold voltage, and the overdrive depends on the drain current, which changes as the output voltage changes unless $R_L \rightarrow \infty$. Furthermore, even if the current were exactly constant, the overdrive depends to some extent on the drain-source voltage unless the Early voltage is infinite. We will use small-signal analysis to study these effects.

The small-signal equivalent circuit is shown in Fig. 3.25b. Since the body terminal is not shown in Fig. 3.25a, we assume that the body is connected to the lowest supply voltage (ground here) to keep the source-body *pn* junction reverse biased. As a result, v_{bs} changes when the output changes because the source is connected to the output, and the g_{mb} generator is active in general.

From KVL around the input loop,

$$v_i = v_{gs} + v_o \quad (3.78)$$

With the output open circuited, $i_o = 0$, and KCL at the output node gives

$$g_m v_{gs} - g_{mb} v_o - \frac{v_o}{R_L} - \frac{v_o}{r_o} = 0 \quad (3.79)$$

Solving (3.78) for v_{gs} , substituting into (3.79), and rearranging gives

$$\left. \frac{v_o}{v_i} \right|_{i_o=0} = \frac{g_m}{g_m + g_{mb} + \frac{1}{R_L} + \frac{1}{r_o}} = \frac{g_m r_o}{1 + (g_m + g_{mb}) r_o + \frac{r_o}{R_L}} \quad (3.80)$$

If $R_L \rightarrow \infty$, (3.80) simplifies to

$$\lim_{R_L \rightarrow \infty} \left. \frac{v_o}{v_i} \right|_{i_o=0} = \frac{g_m r_o}{1 + (g_m + g_{mb}) r_o} \quad (3.81)$$

Equation 3.81 gives the open-circuit voltage gain of the source follower with the load resistor replaced by an ideal current source. If r_o is finite, this gain is less than unity even if the body effect is eliminated by connecting the source to the body to deactivate the g_{mb} generator. In this case, variation in the output voltage changes the drain-source voltage and the current through r_o . From a large-signal standpoint, solving (1.165) for $V_{GS} - V_t$ shows that the overdrive also depends on the drain-source voltage unless the channel-length modulation parameter λ is zero. This dependence causes the small-signal gain to be less than unity.

A significant difference between bipolar and MOS followers is apparent from (3.80). If $R_L \rightarrow \infty$ and $r_o \rightarrow \infty$,

$$\lim_{\substack{R_L \rightarrow \infty \\ r_o \rightarrow \infty}} \frac{v_o}{v_i} = \frac{g_m}{g_m + g_{mb}} = \frac{1}{1 + \chi} \quad (3.82)$$

Equation 3.82 shows that the source-follower gain is less than unity under these conditions and that the gain depends on $\chi = g_{mb}/g_m$, which is typically in the range of 0.1 to 0.3. In contrast, the gain of an emitter follower would be unity under these conditions. As a result, the source-follower gain is not as well specified as that of an emitter follower when body effect is a factor. Furthermore, (1.200) shows that χ depends on the source-body voltage which is equal to V_o when the body is connected to ground. Therefore, the gain calculated in (3.82) depends on the output voltage, causing distortion to arise for large-signal changes in the output as shown in Section 5.3.2. To overcome these limitations in practice, the type of source follower (*n*-channel or *p*-channel) can be chosen so that it can be fabricated in an isolated well. Then the well can be connected to the source of the transistor, setting $V_{SB} = 0$ and $v_{sb} = 0$. Unfortunately, the parasitic capacitance from the well to the substrate increases the capacitance attached to the

source with this connection, reducing the bandwidth of the source follower. The frequency response of source followers is covered in Chapter 7.

The output resistance of the source follower can be calculated from Fig. 3.25b by setting $v_i = 0$ and driving the output with a voltage source v_o . Then $v_{gs} = -v_o$ and i_o is

$$i_o = \frac{v_o}{r_o} + \frac{v_o}{R_L} + g_m v_o + g_{mb} v_o \quad (3.83)$$

Rearranging (3.83) gives

$$R_o = \frac{v_o}{i_o} = \frac{1}{g_m + g_{mb} + \frac{1}{r_o} + \frac{1}{R_L}} \quad (3.84)$$

Equation 3.84 shows that the body effect reduces the output resistance, which is desirable because the source follower produces a voltage output. This beneficial effect stems from the nonzero small-signal current conducted by the g_{mb} generator in Fig. 3.25b, which increases the output current for a given change in the output voltage. As $r_o \rightarrow \infty$ and $R_L \rightarrow \infty$, this output resistance approaches $1/(g_m + g_{mb})$. The common-gate input resistance given in (3.54) approaches the same limiting value.

As with emitter followers, source followers are used as voltage buffers and level shifters. When used as a level shifter, they are more flexible than emitter followers because the dc value of V_{GS} can be altered by changing the W/L ratio.

3.3.8 Common-Emitter Amplifier with Emitter Degeneration

In the common-emitter amplifier considered earlier, the signal is applied to the base, the output is taken from the collector, and the emitter is attached to ac ground. In practice, however, the common-emitter circuit is often used with a nonzero resistance in series with the emitter as shown in Fig. 3.26a. The resistance has several effects, including reducing the transconductance, increasing the output resistance, and increasing the input resistance. These changes stem from negative feedback introduced by the emitter resistor R_E . When V_i increases, the base-emitter voltage increases, which increases the collector current. As a result, the voltage dropped across the emitter resistor increases, reducing the base-emitter voltage compared to the case where $R_E = 0$. Therefore, the presence of nonzero R_E reduces the base-emitter voltage through a negative-feedback process termed *emitter degeneration*. This circuit is examined from a feedback standpoint in Chapter 8.

In this section, we calculate the input resistance, output resistance, and transconductance of the emitter-degenerated, common-emitter amplifier. To find the input resistance and transconductance, consider the small-signal equivalent circuit shown in Fig. 3.26b, and focus on v_i , i_b , and i_o . From KCL at the emitter,

$$\frac{v_e}{R_E} + \frac{v_e + i_o R_C}{r_o} = (\beta_0 + 1) i_b \quad (3.85)$$

From KCL at the collector,

$$i_o + \frac{v_e + i_o R_C}{r_o} = \beta_0 i_b \quad (3.86)$$

From KVL around the input loop,

$$i_b = \frac{v_i - v_e}{r_\pi} \quad (3.87)$$

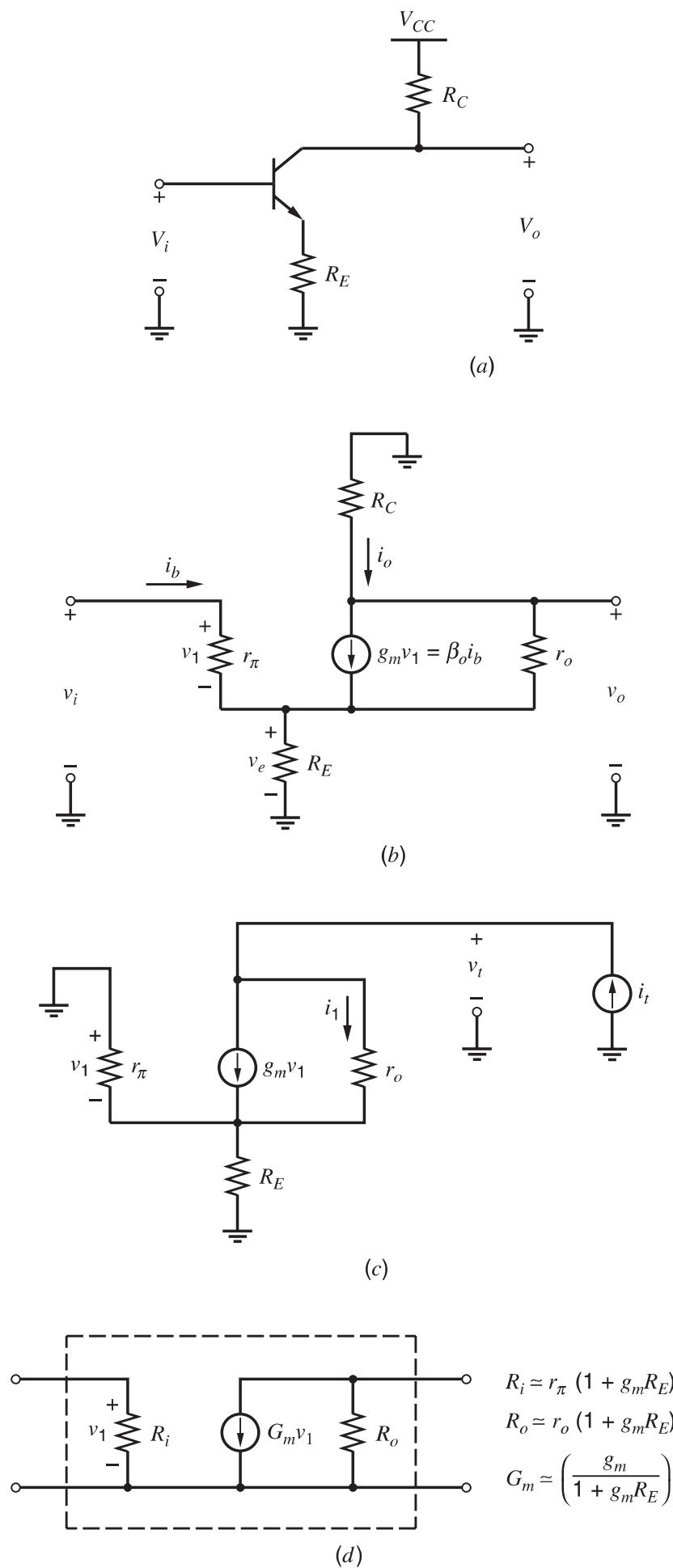


Figure 3.26 (a) Common-emitter amplifier with emitter degeneration. (b) Small-signal equivalent circuit for emitter-degenerated, common-emitter amplifier. (c) Circuit for calculation of output resistance. (d) Small-signal, two-port equivalent of emitter-degenerated CE amplifier.

Solving (3.85) for i_o , substituting into (3.86) and rearranging gives

$$v_e = i_b \left(\frac{1 + (\beta_0 + 1) \frac{r_o}{R_C}}{\frac{1}{R_C} + \frac{1}{R_E} + \frac{r_o}{R_C R_E}} \right) \quad (3.88)$$

Substituting (3.88) into (3.87) and rearranging gives

$$R_i = \frac{v_i}{i_b} = r_\pi + (\beta_0 + 1) R_E \left(\frac{r_o + \frac{R_C}{\beta_0 + 1}}{r_o + R_C + R_E} \right) \quad (3.89)$$

If $r_o \gg R_C$ and $r_o \gg R_E$, the last term in parentheses in (3.89) is approximately equal to unity and

$$R_i \simeq r_\pi + (\beta_0 + 1) R_E \quad (3.90)$$

Because the last term in parentheses in (3.89) is less than one, comparing (3.89) and (3.90) shows that finite r_o reduces the input resistance of the common-emitter amplifier with emitter degeneration. This reduction stems from nonzero current that flows in r_o when r_o is finite. If v_i increases, v_e follows v_i because the base-emitter voltage is approximately constant, but the collector voltage ($-i_o R_C$) decreases by an amount determined by the small-signal gain from the base to the collector. Therefore, the current that flows in r_o from the emitter to the collector increases, increasing the base current and reducing the input resistance. In practice, (3.90) is usually used to calculate the input resistance. The error in the approximation is usually small unless the resistances represented by R_C or R_E are large, such as when implemented with transistors in active-load configurations. Active loads are considered in Chapter 4.

Now we will calculate the transconductance of the stage. First, set $R_C = 0$ in Fig. 3.26b because $G_m = i_o/v_i$ with the output shorted. Substituting (3.87) into (3.85) with $R_C = 0$ and rearranging gives

$$v_e = v_i \left(\frac{\frac{(\beta_0 + 1)}{r_\pi}}{\frac{1}{R_E} + \frac{1}{r_o} + \frac{\beta_0 + 1}{r_\pi}} \right) \quad (3.91)$$

Substituting (3.87) and (3.91) into (3.86) with $R_C = 0$ and rearranging gives

$$G_m = \frac{i_o}{v_i} = g_m \left[\frac{1 - \frac{R_E}{\beta_0 r_o}}{1 + g_m R_E \left(1 + \frac{1}{\beta_0} + \frac{1}{g_m r_o} \right)} \right] \quad (3.92)$$

In most practical cases, $\beta_0 \gg 1$, $r_o \gg R_E$, and $g_m r_o \gg 1$. Then

$$G_m \simeq \frac{g_m}{1 + g_m R_E} \quad (3.93)$$

Equation 3.93 is usually used to calculate the transconductance of a common-emitter amplifier with emitter degeneration.

The output resistance is calculated using the equivalent circuit of Fig. 3.26c. For the time being, assume that R_C is very large and can be neglected. The test current i_t flows in the parallel combination of r_π and R_E , so that

$$v_1 = -i_t(r_\pi \parallel R_E) \quad (3.94)$$

The current through r_o is

$$i_1 = i_t - g_m v_1 = i_t + i_t g_m (r_\pi \parallel R_E) \quad (3.95)$$

As a result, the voltage v_t is

$$v_t = -v_1 + i_1 r_o = i_t (r_\pi \parallel R_E) + i_t r_o [1 + g_m (r_\pi \parallel R_E)] \quad (3.96)$$

Thus

$$R_o = \frac{v_t}{i_t} = (r_\pi \parallel R_E) + r_o [1 + g_m (r_\pi \parallel R_E)] \quad (3.97)$$

In this equation, the first term is much smaller than the second. If the first term is neglected, we obtain,

$$R_o \simeq r_o \left(1 + g_m \frac{r_\pi R_E}{r_\pi + R_E} \right) = r_o \left(1 + \frac{g_m R_E}{1 + \frac{R_E}{r_\pi}} \right) = r_o \left(1 + \frac{g_m R_E}{1 + \frac{g_m R_E}{\beta_0}} \right) \quad (3.98)$$

If $g_m R_E \ll \beta_0$, then

$$R_o \simeq r_o (1 + g_m R_E) \quad (3.99)$$

Thus the output resistance is increased by a factor $(1 + g_m R_E)$. This fact makes the use of emitter degeneration desirable in transistor current sources. If the collector load resistor R_C is not large enough to neglect, it must be included in parallel with the expressions in (3.97)–(3.99). A small-signal equivalent circuit, neglecting R_C , is shown in Fig. 3.26d. On the other hand, if $g_m R_E \gg \beta_0$, (3.98) shows that

$$R_o \simeq r_o (1 + \beta_0) \quad (3.100)$$

The output resistance is finite even when $R_E \rightarrow \infty$ because nonzero test current flows in r_π when β_0 is finite.

3.3.9 Common-Source Amplifier with Source Degeneration

Source degeneration in MOS transistor amplifiers is not as widely used as emitter degeneration in bipolar circuits for at least two reasons. First, the transconductance of MOS transistors is normally much lower than that of bipolar transistors so that further reduction in transconductance is usually undesirable. Second, although degeneration increases the input resistance in the bipolar case, $R_i \rightarrow \infty$ even without degeneration in the MOS case. However, examining the effects of source degeneration is important in part because it is widely used to increase the output resistance of MOS current sources. Also, because small-geometry MOS transistors can be modeled as ideal square-law devices with added source resistors as shown in Section 1.7.1, we will consider the effects of source degeneration below.

A common-source amplifier with source degeneration is shown in Fig. 3.27. Its small-signal equivalent circuit is shown in Fig. 3.28. Because the input is connected to the gate of the MOS transistor, $R_i \rightarrow \infty$. To calculate the transconductance, set $R_D = 0$ because $G_m = i_o/v_i$ with the output shorted. Also, since a connection to the body is not shown in Fig. 3.27, we assume that the body is connected to the lowest power-supply voltage, which is ground. Therefore, the dc body voltage is constant and $v_b = 0$. From KCL at the source with $R_D = 0$,

$$\frac{v_s}{R_S} + \frac{v_s}{r_o} = g_m (v_i - v_s) + g_{mb} (0 - v_s) \quad (3.101)$$

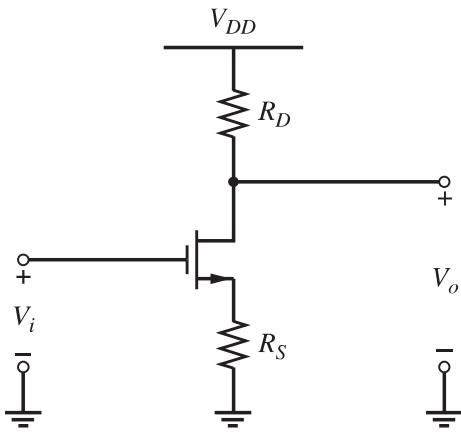


Figure 3.27 Common-source amplifier with source degeneration.

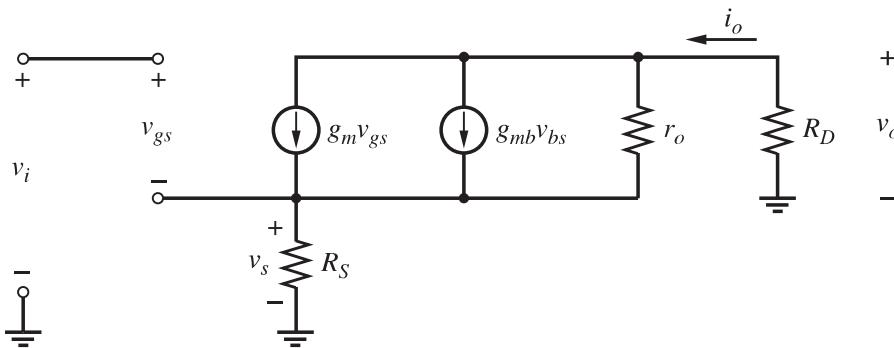


Figure 3.28 Small-signal equivalent of the source-degenerated, common-source amplifier.

From KCL at the drain with $R_D = 0$,

$$i_o + \frac{v_s}{r_o} = g_m (v_i - v_s) + g_{mb} (0 - v_s) \quad (3.102)$$

Solving (3.101) for v_s , substituting into (3.102), and rearranging gives

$$G_m = \frac{i_o}{v_i} = \frac{g_m}{1 + (g_m + g_{mb}) R_S + \frac{R_S}{r_o}} \quad (3.103)$$

If $r_o \gg R_S$,

$$G_m \simeq \frac{g_m}{1 + (g_m + g_{mb}) R_S} \quad (3.104)$$

For large R_S , (3.104) shows that the value of G_m approaches $1/[(1 + \chi) R_S]$. Even in this limiting case, the transconductance of the common-source amplifier with degeneration is dependent on an active-device parameter χ . Since χ is typically in the range of 0.1 to 0.3, the body effect causes the transconductance in this case to deviate from $1/R_S$ by about 10 to 20 percent. In contrast, (3.92) indicates that the value of G_m for a common-emitter amplifier with degeneration approaches $\beta_0/[(\beta_0 + 1) R_E]$ for large R_E , assuming that $r_o \gg R_E$ and $g_m r_o \gg 1$. If $\beta_0 > 100$, the transconductance of this bipolar amplifier is within 1 percent of $1/R_E$. Therefore, the transconductance of a common-source amplifier with degeneration is usually much more dependent on active-device parameters than in its bipolar counterpart.

The output resistance of the circuit can be calculated from the equivalent circuit of Fig. 3.29, where R_D is neglected. Since the entire test current flows in R_S ,

$$v_s = i_t R_S \quad (3.105)$$

Then

$$v_t = v_s + i_1 r_o = v_s + r_o [i_t - g_m (0 - v_s) - g_{mb} (0 - v_s)] \quad (3.106)$$

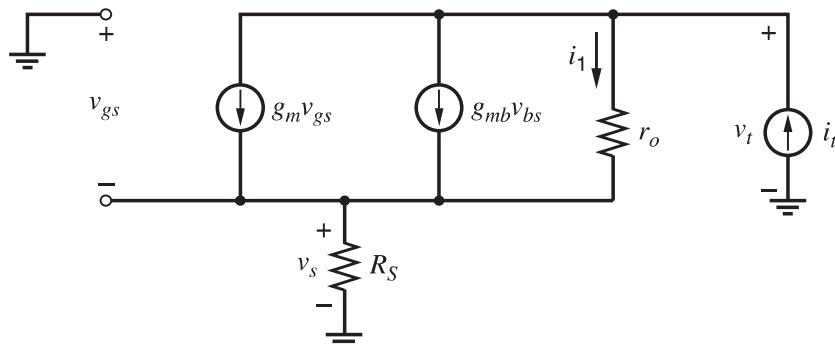


Figure 3.29 Circuit for calculation of output resistance.

Substituting (3.105) into (3.106) and rearranging gives

$$R_o = \frac{v_t}{i_t} = R_S + r_o [1 + (g_m + g_{mb}) R_S] \quad (3.107)$$

This equation shows that as R_S is made arbitrarily large, the value of R_o continues to increase. In contrast, (3.100) shows that R_o in the common-emitter amplifier with degeneration approaches a maximum value of about $(\beta_0 + 1) r_o$ as $R_E \rightarrow \infty$.

3.4 Multiple-Transistor Amplifier Stages

Most integrated-circuit amplifiers consist of a number of stages, each of which provides voltage gain, current gain, and/or impedance-level transformation from input to output. Such circuits can be analyzed by considering each transistor to be a *stage* and analyzing the circuit as a collection of individual transistors. However, certain combinations of transistors occur so frequently that these combinations are usually characterized as *subcircuits* and regarded as a single stage. The usefulness of these topologies varies considerably with the technology being used. For example, the Darlington two-transistor connection is widely used in bipolar integrated circuits to improve the effective current gain and input resistance of a single bipolar transistor. Since the current gain and input resistance are infinite with MOS transistors however, this connection finds little use in pure MOS integrated circuits. On the other hand, the cascode connection achieves a very high output resistance and is useful in both bipolar and MOS technologies.

Darlington CMOS no tiene sentido

3.4.1 The CC-CE, CC-CC and Darlington Configurations

The common-collector-common-emitter (CC-CE), common-collector-common-collector (CC-CC), and Darlington⁵ configurations are all closely related. They incorporate an additional transistor to boost the current gain and input resistance of the basic bipolar transistor. The common-collector-common-emitter configuration is shown in Fig. 3.30a. The biasing current source I_{BIAS} is present to establish the quiescent dc operating current in the emitter-follower transistor Q_1 ; this current source may be absent in some cases or may be replaced by a resistor. The common-collector-common-collector configuration is illustrated in Fig. 3.30b. In both of these configurations, the effect of transistor Q_1 is to increase the current gain through the stage and to increase the input resistance. For the purpose of the low-frequency, small-signal analysis of circuits, the two transistors Q_1 and Q_2 can be thought of as a single composite transistor, as illustrated in Fig. 3.31. The small-signal equivalent circuit for this composite device is shown in Fig. 3.32, assuming that the effects of the r_o of Q_1 are negligible. We will now calculate effective values for the r_π , g_m , β_0 , and r_o of the composite device, and we will designate these composite parameters with a superscript c . We will also denote the



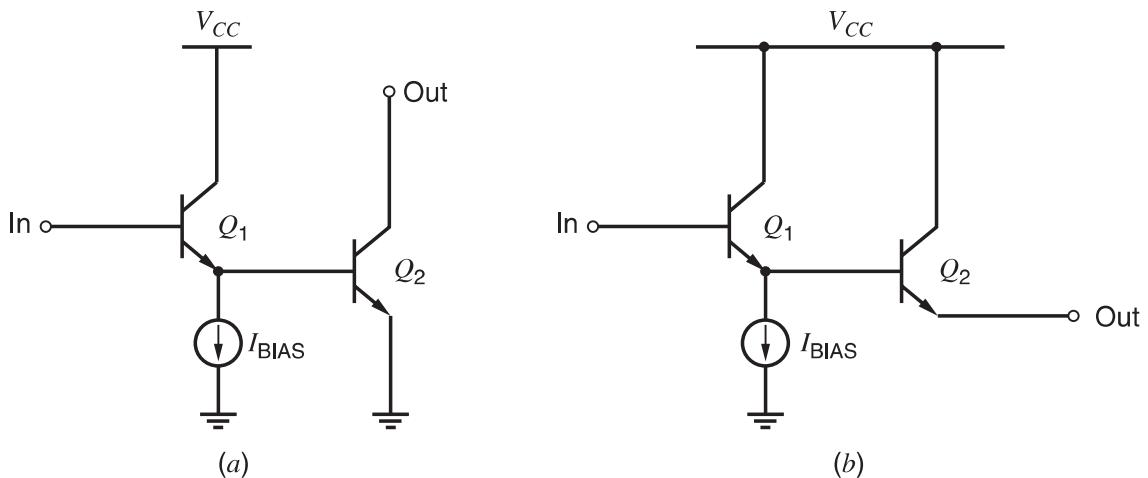


Figure 3.30 (a) Common-collector–common-emitter cascade. (b) Common-collector– common-collector cascade.

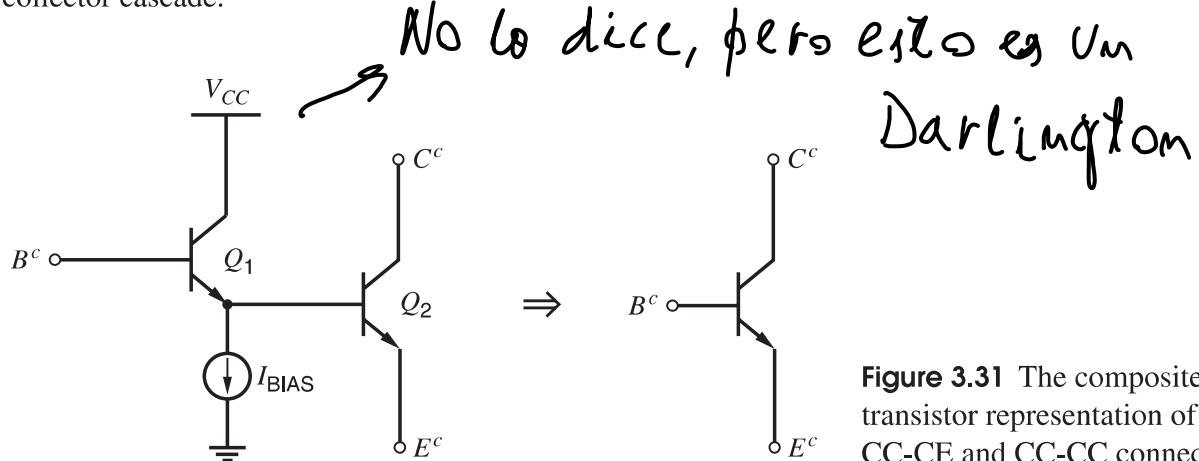
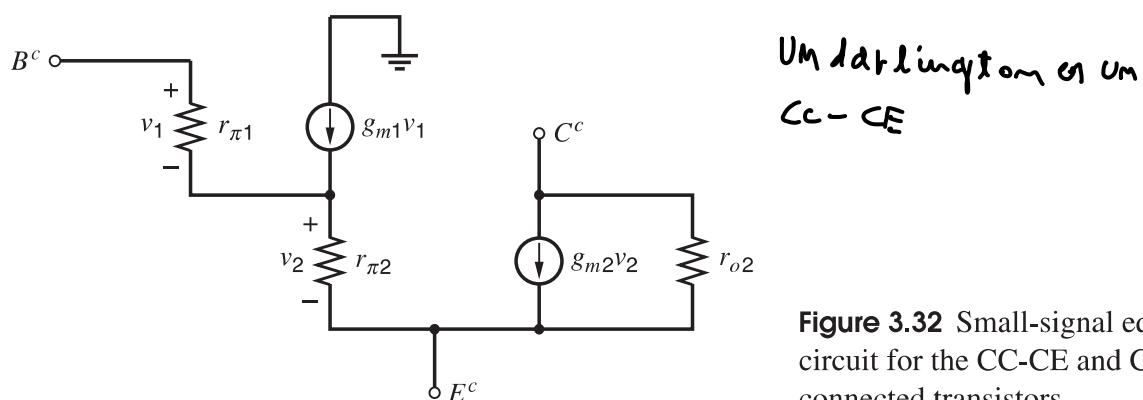


Figure 3.31 The composite transistor representation of the CC-CE and CC-CC connections.



Um darlington en um
CC-CE

Figure 3.32 Small-signal equivalent circuit for the CC-CE and CC-CC connected transistors.

terminal voltages and currents of the composite device with a superscript c . We assume that β_0 is constant.

The effective value of r_π , r_π^c , is the resistance seen looking into the composite base B^c with the composite emitter E^c grounded. Referring to Fig. 3.32, we see that the resistance looking into the base of Q_2 with E^c grounded is simply $r_{\pi 2}$. Thus (3.73) for the input resistance of the emitter follower can be used. Substituting $r_{\pi 2}$ for R_L and allowing $r_o \rightarrow \infty$ gives

$$r_\pi^c = r_{\pi 1} + (\beta_0 + 1) r_{\pi 2} \quad (3.108)$$

The effective transconductance of the configuration g_m^c is the change in the collector current of Q_2 , i_c^c , for a unit change in v_{be}^c with C^c and E^c grounded. To calculate this transconductance, we first find the change in v_2 that occurs for a unit change in v_{be}^c . Equation 3.69 can be used

directly, giving

$$\frac{v_2}{v_{be}^c} = \frac{1}{1 + \left(\frac{r_{\pi 1}}{(\beta_0 + 1) r_{\pi 2}} \right)} \quad (3.109)$$

Also

No VSA LAS MISMAS

$$i_c^c = g_m^c v_{be}^c = g_m 2 v_2 = \frac{g_m 2 v_{be}^c}{1 + \left(\frac{r_{\pi 1}}{(\beta_0 + 1) r_{\pi 2}} \right)} \quad (3.110)$$

→ MALA D.O.

Thus

Simplificaciones q'

$$g_m^c = \frac{i_c^c}{v_{be}^c} = \frac{g_m 2}{1 + \left(\frac{r_{\pi 1}}{(\beta_0 + 1) r_{\pi 2}} \right)} \rightarrow \frac{g_m 2}{2} \quad (3.111)$$

Si $r_{\pi 1} = \beta_0 r_{\pi 2}$

For the special case in which the biasing current source I_{BIAS} is zero, the emitter current of Q_1 is equal to the base current of Q_2 . Thus the ratio of $r_{\pi 1}$ to $r_{\pi 2}$ is $(\beta_0 + 1)$, and (3.111) reduces to

g_m^c = g_{m2} / 2 → *No Digenada*

$$g_m^c = \frac{g_m 2}{2} \quad (3.112)$$

The effective current gain β^c is the ratio

$$\beta^c = \frac{i_c^c}{i_b^c} = \frac{i_{c2}}{i_{b1}} \quad (3.113)$$

The emitter current of Q_1 is given by

$$i_{e1} = (\beta_0 + 1) i_{b1} \quad (3.114)$$

Since $i_{e1} = i_{b2}$,

$$i_{c2} = i_c^c = \beta_0 i_{b2} = \beta_0 (\beta_0 + 1) i_{b1} = \beta_0 (\beta_0 + 1) i_{b1}^c \quad (3.115)$$

Therefore,

$\beta^c = \beta_0 (\beta_0 + 1)$

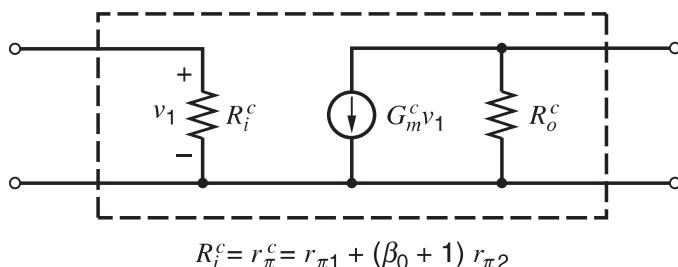
$$\beta^c = \beta_0 (\beta_0 + 1) \quad (3.116)$$

Equation 3.116 shows that the current gain of the composite transistor is approximately equal to β_0^2 . Also, by inspection of Fig. 3.32, assuming r_μ is negligible, we have

$$r_o^c = r_{o2} \quad (3.117)$$

The small-signal, two-port network equivalent for the CC-CE connection is shown in Fig. 3.33, where the collector resistor R_C has not been included. This small-signal equivalent can be used to represent the small-signal operation of the composite device, simplifying the analysis of circuits containing this structure.

The Darlington configuration, illustrated in Fig. 3.34, is a composite two-transistor device in which the collectors are tied together and the emitter of the first device drives the base of the second. A biasing element of some sort is used to control the emitter current of Q_1 . The result is a three-terminal composite transistor that can be used in place of a single transistor in common-emitter, common-base, and common-collector configurations. When used as an emitter follower, the device is identical to the CC-CC connection already described. When used as a common-emitter amplifier, the device is very similar to the CC-CE connection, except that the collector of Q_1 is connected to the output instead of to the power supply. One effect of this change is to reduce the effective output resistance of the device



$$G_m^c = g_m^c = \frac{g_{m2}}{1 + \left[\frac{r_{\pi 1}}{(\beta_0 + 1) r_{\pi 2}} \right]}$$

$$R_o^c = r_o^c = r_{o2}$$

Figure 3.33 Two-port representation, CC-CE connection.

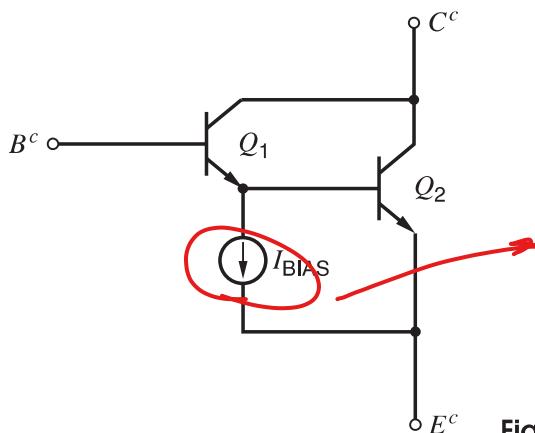


Figure 3.34 The Darlington configuration.

because of feedback through the r_o of Q_1 . Also, this change increases the input capacitance because of the connection of the collector-base capacitance of Q_1 from the input to the output. Because of these drawbacks, the CC-CE connection is normally preferable in integrated small-signal amplifiers. The term **Darlington** is often used to refer to both the CC-CE and CC-CC connections.

As mentioned previously, Darlington-type connections are used to boost the effective current gain of bipolar transistors and have no significant application in pure-MOS circuits. In BiCMOS technologies, however, a potentially useful connection is shown in Fig. 3.35, where an MOS transistor is used for Q_1 . This configuration not only realizes the infinite input resistance and current gain of the MOS transistor, but also the large transconductance of the bipolar transistor. Lomejor de los 2

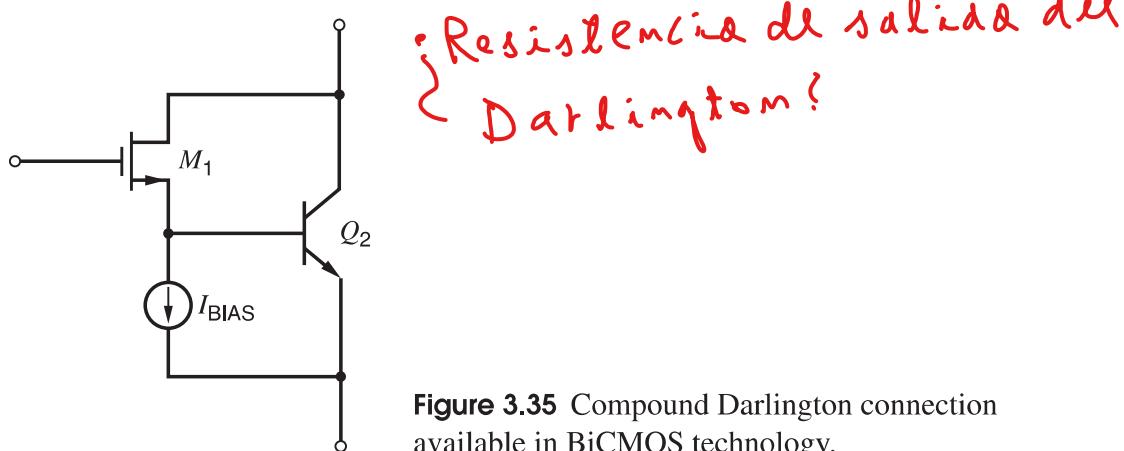


Figure 3.35 Compound Darlington connection available in BiCMOS technology.

■ EXAMPLE

Find the effective r_π^c , β^c , and g_m^c for the composite transistor shown in Fig. 3.31. For both devices, assume that $\beta_0 = 100$, $r_b = 0$, and $r_o \rightarrow \infty$. For Q_2 , assume that $I_C = 100 \mu\text{A}$ and that $I_{\text{BIAS}} = 10 \mu\text{A}$.

The base current of Q_2 is $100 \mu\text{A}/100 = 1 \mu\text{A}$. Thus the emitter current of Q_1 is $11 \mu\text{A}$. Then

$$\begin{aligned} r_{\pi 1} &= \frac{\beta_0}{g_m} = \frac{100}{11 \mu\text{A}/26 \text{ mV}} = 236 \text{ k}\Omega \\ g_{m1} &= (2.36 \text{ k}\Omega)^{-1} \\ r_{\pi 2} &= 26 \text{ k}\Omega \\ g_{m2} &= (260 \Omega)^{-1} \\ r_\pi^c &= 236 \text{ k}\Omega + (101)(26 \text{ k}\Omega) = 2.8 \text{ M}\Omega \\ \beta^c &= (101)(100) = 10,100 \\ g_m^c &= g_{m2} (0.916) = (283 \Omega)^{-1} \end{aligned}$$

Thus the composite transistor has much higher input resistance and current gain than a single transistor.

3.4.2 The Cascode Configuration

*otigen
de
CASCODE*

The cascode configuration was first invented for vacuum-tube circuits.^{6,7} With vacuum tubes, the terminal that emits electrons is the *cathode*, the terminal that controls current flow is the *grid*, and the terminal that collects electrons is the *anode*. The *cascode* is a **cascade** of common-cathode and common-grid stages joined at the *anode* of the first stage and the *cathode* of the second stage. The cascode configuration is important mostly because it increases output resistance and reduces unwanted capacitive feedback in amplifiers, allowing operation at higher frequencies than would otherwise be possible. The high output resistance attainable is particularly useful in desensitizing bias references from variations in power-supply voltage and in achieving large amounts of voltage gain. These applications are described further in Chapter 4. The topic of frequency response is covered in Chapter 7. Here, we will focus on the **low-frequency**, small-signal properties of the cascode configuration.



3.4.2.1 The Bipolar Cascode

In bipolar form, the cascode is a common-emitter–common-base (CE-CB) amplifier, as shown in Fig. 3.36. We will assume here that r_b in both devices is zero. Although the base resistances have a negligible effect on the low-frequency performance, the effects of nonzero r_b are important in the high-frequency performance of this combination. These effects are considered in Chapter 7. $r_b = \text{muestra } t_x(\text{C129})$

The small-signal equivalent for the bipolar cascode circuit is shown in Fig. 3.37. Since we are considering the low-frequency performance, we neglect the capacitances in the model of each transistor. We will determine the input resistance, output resistance, and transconductance of the cascode circuit. By inspection of Fig. 3.37, the input resistance is simply

$$R_i = r_{\pi 1} \quad (3.118)$$

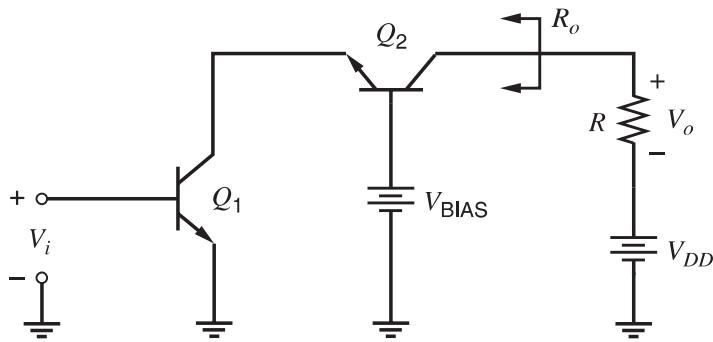


Figure 3.36 The cascode amplifier using bipolar transistors.

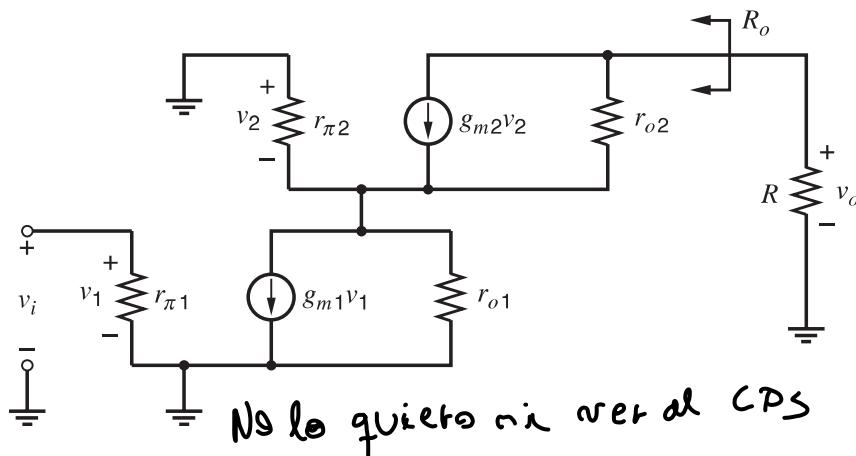


Figure 3.37 Small-signal equivalent circuit for the bipolar-transistor cascode connection.

Since the current gain from the emitter to the collector of Q_2 is nearly unity, the transconductance of the circuit from input to output is → *la etapa planteada como amplificador-dot de transconductancia*

$$G_m \simeq g_{m1} \quad (3.119)$$

The output resistance can be calculated by shorting the input v_i to ground and applying a test signal at the output. Then $v_1 = 0$ in Fig. 3.37 and the $g_{m1}v_1$ generator is inactive. The circuit is then identical to that of Fig. 3.26c for a bipolar transistor with emitter degeneration. Therefore, using (3.98) with $R_E = r_{o1}$ shows that the output resistance is

como la R_o del BC o del EC con
Emitor degenerado, es tan
de hacer mdo. ↪

$$R_o \simeq r_{o2} \left(1 + \frac{g_{m2}r_{o1}}{1 + \frac{g_{m2}r_{o1}}{\beta_0}} \right) \quad (3.120)$$

If $g_{m2}r_{o1} \gg \beta_0$ and $\beta_0 \gg 1$, *Si pones un RC, mi te importa*

$$R_o \simeq \beta_0 r_{o2} \quad (3.121)$$

Therefore, the CE-CB connection displays an output resistance that is larger by a factor of about β_0 than the CE stage alone. If this circuit is operated with a hypothetical *collector load that has infinite incremental resistance*, the voltage gain is

???

$$A_v = \frac{v_o}{v_i} = -G_m R_o \simeq -g_{m1} r_{o2} \beta_0 = -\frac{\beta_0}{\eta} \quad (3.122)$$

Thus the magnitude of the maximum available voltage gain is higher by a factor β_0 than for the case of a single transistor. For a typical *npn* transistor, the ratio of β_0/η is approximately 2×10^5 . In this analysis, we have neglected r_μ . As described in Chapter 1, the value of r_μ for integrated-circuit *npn* transistors is usually much larger than $\beta_0 r_o$, and then r_μ has little effect on R_o . For lateral *pnp* transistors, however, r_μ is comparable with $\beta_0 r_o$ and decreases R_o somewhat.

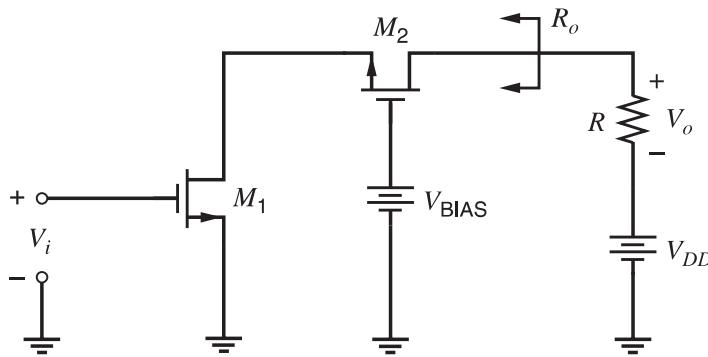


Figure 3.38 Cascode amplifier using MOSFETs.

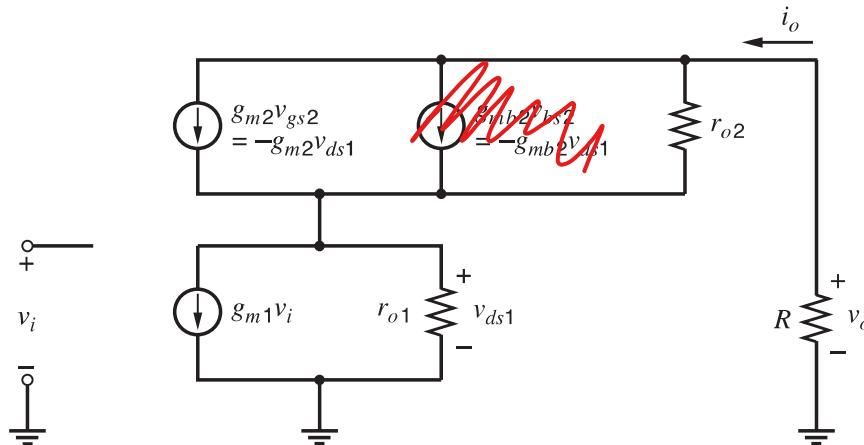


Figure 3.39 Small-signal equivalent circuit for the MOS-transistor cascode connection.

3.4.2.2 The MOS Cascode

In MOS form, the cascode is a common-source–common-gate (CS-CG) amplifier, as shown in Fig. 3.38. The small-signal equivalent circuit is shown in Fig. 3.39. Since the input is connected to the gate of M_1 , the input resistance is

$$R_i \rightarrow \infty \quad (3.123)$$

To find the transconductance, set $R = 0$ to short the output and calculate the current i_o . From KCL at the output,

$$i_o + g_{m2}v_{ds1} + \cancel{g_{mb2}v_{ds1}} + \frac{v_{ds1}}{r_{o2}} = 0 \quad (3.124)$$

From KCL at the source of M_2 ,

$$g_{m1}v_i + g_{m2}v_{ds1} + \cancel{g_{mb2}v_{ds1}} + \frac{v_{ds1}}{r_{o1}} + \frac{v_{ds1}}{r_{o2}} = 0 \quad (3.125)$$

Solving (3.125) for v_{ds1} , substituting into (3.124), and rearranging gives

$$G_m = \left. \frac{i_o}{v_i} \right|_{v_o=0} = g_{m1} \left(1 - \frac{1}{1 + (g_{m2} + \cancel{g_{mb2}}) r_{o1} + \frac{r_{o1}}{r_{o2}}} \right) \simeq g_{m1} \quad (3.126)$$

Equation 3.126 shows that the transconductance of the simple cascode is less than g_{m1} . If $(g_{m2} + g_{mb2}) r_{o1} \gg 1$, however, the difference is small, and the main point here is that the cascode configuration has little effect on the transconductance. This result stems from the observation that R_{i2} , the resistance looking in the source of M_2 , is much less than r_{o1} . From (3.54) and (3.55) with $R = R_D \parallel R_L$,

$$R_{i2} = \frac{r_{o2} + R}{1 + (g_{m2} + \cancel{g_{mb2}}) r_{o2}} \simeq \frac{1}{g_{m2} + \cancel{g_{mb2}}} + \frac{R}{(g_{m2} + \cancel{g_{mb2}}) r_{o2}} \quad (3.127)$$

In finding the transconductance, we set $R = 0$ so that $v_o = 0$. Then $R_{i2} \simeq 1/(g_m + g_{mb})$, and most of the $g_{m1}v_i$ current flows in the source of M_2 because $R_{i2} \ll r_{o1}$. Finally, the current gain from the source to the drain of M_2 is unity. Therefore, most of the $g_{m1}v_i$ current flows in the output, and $G_m \simeq g_{m1}$, as shown in (3.126).

To find the output resistance, set $v_i = 0$, which deactivates the g_{m1} generator in Fig. 3.39 and reduces the model for common-source transistor M_1 to simply r_{o1} . Therefore, the output resistance of the cascode can be found by substituting $R_S = r_{o1}$ in (3.66), which was derived for a common-gate amplifier. To focus on the output resistance of the cascode itself, let $R \rightarrow \infty$. The result is

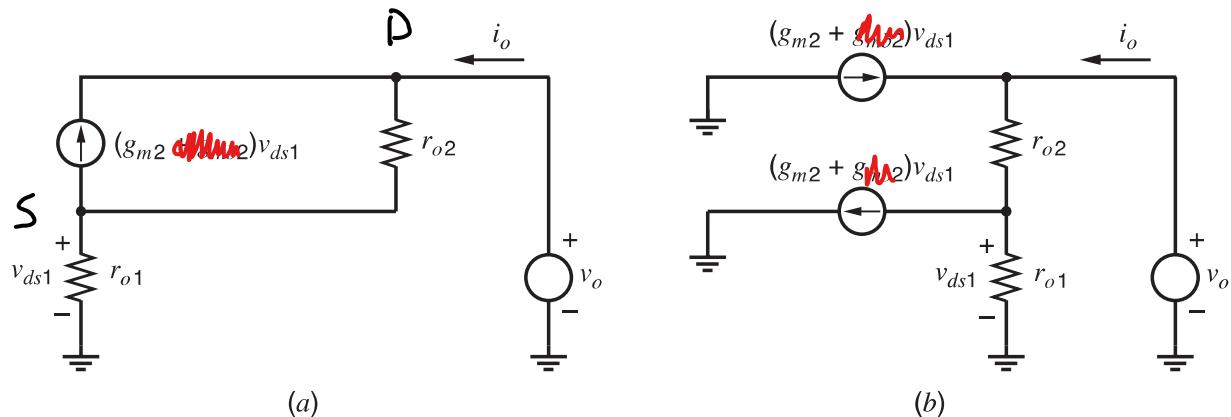
$$R_o = r_{o1} + r_{o2} + (g_{m2} + g_{mb2}) r_{o1} r_{o2} \simeq (g_{m2} + g_{mb2}) r_{o1} r_{o2} \quad (3.128)$$

Equation 3.128 shows that the MOS cascode increases the output resistance by a factor of about $(g_m + g_{mb}) r_o$ compared to a common-source amplifier.

The increase in the output resistance can be predicted in another way that provides insight into the operation of the cascode. Let i_o represent the current that flows in the output node in Fig. 3.39 when the output is driven by voltage v_o . Since $v_{ds1} = i_o r_{o1}$ when $v_i = 0$, the output resistance is

$$R_o = \frac{v_o}{i_o} \Big|_{v_i=0} = \frac{v_o}{(v_{ds1}/r_{o1})} \Big|_{v_i=0} = r_{o1} \left(\frac{v_{ds1}}{v_o} \right)^{-1} \Big|_{v_i=0} \quad (3.129)$$

To find the ratio v_{ds1}/v_o , consider the modified small-signal circuits shown in Fig. 3.40. In Fig. 3.40a, $R \rightarrow \infty$ so we can concentrate on the output resistance of the cascode circuit itself. Also, the $g_{m1}v_i$ generator is eliminated because $v_i = 0$, and the two generators $g_{m2}v_{ds1}$ and $g_{mb2}v_{ds1}$ have been combined into one equivalent generator $(g_{m2} + g_{mb2})v_{ds1}$. In Fig. 3.40b,



Intercambiante entre

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R_o=1 k  s en paralelo con
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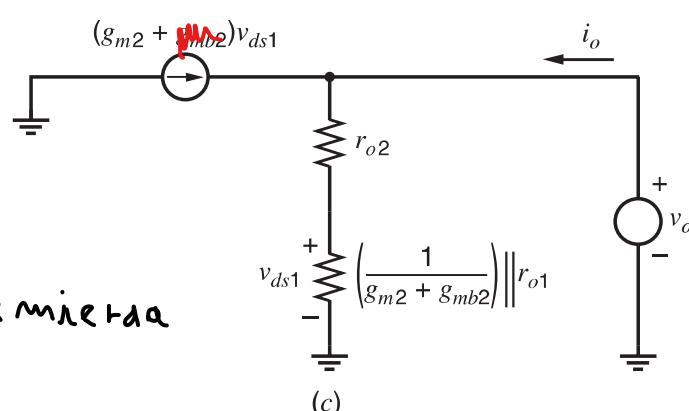


Figure 3.40 Construction of a cascode model to find v_{ds1}/v_o . (a) The dependent sources are combined. (b) The combined source is converted into two sources. (c) The current source between the source of M_2 and ground is converted into a resistor.

the $(g_{m2} + g_{mb2}) v_{ds1}$ generator from the source to the drain of M_2 has been replaced by two equal-valued generators: one from ground to the drain of M_2 and the other from the source of M_2 to ground. This replacement is similar to the substitution made in Fig. 3.20 to convert the hybrid- π model to a T model for a common-gate amplifier. Because the equations that describe the operation of the circuits in Fig. 3.40a and Fig. 3.40b are identical, the circuit in Fig. 3.40b is equivalent to that in Fig. 3.40a. Finally, in Fig. 3.40c, the current source from the source of M_2 to ground, which is controlled by the voltage across itself, is replaced by an equivalent resistor of value $1/(g_{m2} + g_{mb2})$. The current $(g_{m2} + g_{mb2}) v_{ds1}$ in Fig. 3.40c flows into the test source v_o . The two resistors in Fig. 3.40c form a voltage divider, giving

$$\frac{v_{ds1}}{v_o} = \frac{\left(\frac{1}{g_{m2} + g_{mb2}}\right) \| r_{o1}}{\left[\left(\frac{1}{g_{m2} + g_{mb2}}\right) \| r_{o1}\right] + r_{o2}} \simeq \frac{1}{(g_{m2} + g_{mb2}) r_{o2}} \quad (3.130)$$

Substituting (3.130) into (3.129) and rearranging gives the same result as in (3.128). In (3.130), the term $1/(g_{m2} + g_{mb2})$ represents the resistance looking into the source of the common-gate transistor M_2 when the output in Fig. 3.39 is voltage driven. The key point here is that the output resistance of the cascode can be increased by reducing the input resistance of the common-gate transistor under these conditions because this change reduces both v_{ds1} and i_o .

NO ME IMPOR TA Unlike in the bipolar case, the maximum value of the output resistance in the MOS cascode does not saturate at a level determined by β_0 ; therefore, further increases in the output resistance can be obtained by using more than one level of cascoding. This approach is used in practice. Ultimately, the maximum output resistance is limited by impact ionization as described in Section 1.9 or by leakage current in the reverse-biased junction diode at the output. Also, the number of levels of cascoding is limited by the power-supply voltage and signal-swing requirements. Each additional level of cascoding places one more transistor in series with the input transistor between the power supply and ground. To operate all the transistors in the active region, the drain-source voltage of each transistor must be greater than its overdrive $V_{GS} - V_t$. Since the cascode transistors operate in series with the input transistor, additional levels of cascoding use some of the available power-supply voltage, reducing the amount by which the output can vary before pushing one or more transistors into the triode region. This topic is considered further in Chapter 4.

In BiCMOS technologies, cascodes are sometimes used with the MOS transistor M_2 in Fig. 3.38 replaced by a bipolar transistor, such as Q_2 in Fig. 3.36. This configuration has the infinite input resistance given by M_1 . Also, the resistance looking into the emitter of the common-base stage Q_2 when the output is grounded is $R_{i2} \simeq 1/g_{m2}$ in this configuration. Since the transconductance for a given bias current of bipolar transistors is usually much greater than for MOS transistors, the BiCMOS configuration is often used to reduce the load resistance presented to M_1 and to improve the high-frequency properties of the cascode amplifier. The frequency response of a cascode amplifier is described in Chapter 7.

EXAMPLE

Calculate the transconductance and output resistance of the cascode circuit of Fig. 3.38. Assume that both transistors operate in the active region with $g_m = 1 \text{ mA/V}$, $\chi = 0.1$, and $r_o = 20 \text{ k}\Omega$.

From (3.126),

$$G_m = \left(1 \frac{\text{mA}}{\text{V}}\right) \left(1 - \frac{1}{1 + (1.1)(20) + 1}\right) = 960 \frac{\mu\text{A}}{\text{V}}$$

From (3.128),

$$R_o = 20 \text{ k}\Omega + 20 \text{ k}\Omega + (1.1)(20) 20 \text{ k}\Omega = 480 \text{ k}\Omega$$

The approximations in (3.126) and (3.128) give $G_m \simeq 1 \text{ mA/V}$ and $R_o \simeq 440 \text{ k}\Omega$. These approximations deviate from the exact results by about 4 percent and 8 percent, respectively, and are usually close enough for hand calculations.

3.4.3 The Active Cascode \rightarrow muy poco de cascode con MOS.

As mentioned in the previous section, increasing the number of levels of cascoding increases the output resistance of MOS amplifiers. In practice, however, the power-supply voltage and signal-swing requirements limit the number of levels of cascoding that can be applied. One way to increase the output resistance of the MOS cascode circuit without increasing the number of levels of cascoding is to use the active-cascode circuit, as shown in Fig. 3.41.^{8,9}

This circuit uses an amplifier in a negative feedback loop to control the voltage from the gate of M_2 to ground. If the amplifier gain a is infinite, the negative feedback loop adjusts the gate of M_2 until the voltage difference between the two amplifier inputs is zero. In other words, the drain-source voltage of M_1 is driven to equal V_{BIAS} . If the drain-source voltage of M_1 is constant, the change in the drain current in response to changes in the output voltage V_o is zero, and the output resistance is infinite. In practice, the amplifier gain a is finite, which means that the drain-source voltage of M_1 is not exactly constant and the output resistance is finite. The effect of negative feedback on output resistance is considered quantitatively in Chapter 8. In this section, we will derive the small-signal properties of the active-cascode circuit by comparing its small-signal model to that of the simple cascode described in the previous section.

Qualitatively, when the output voltage increases, the drain current of M_2 increases, which increases the drain current and drain-source voltage of M_1 . This voltage increase is amplified by $-a$, causing the voltage from the gate of M_2 to ground to fall. The falling gate voltage of M_2 acts to reduce the change in its drain current, increasing the output resistance compared to a simple cascode, where the voltage from the gate of M_2 to ground is held constant.

Figure 3.42 shows the low-frequency, small-signal equivalent circuit. The body-effect transconductance generator for M_1 is inactive because $v_{bs1} = 0$. The gate-source voltage of M_2 is

$$v_{gs2} = v_{g2} - v_{s2} = v_{g2} - v_{ds1} = -(a) v_{ds1} - v_{ds1} = -(a + 1) v_{ds1} \quad (3.131)$$

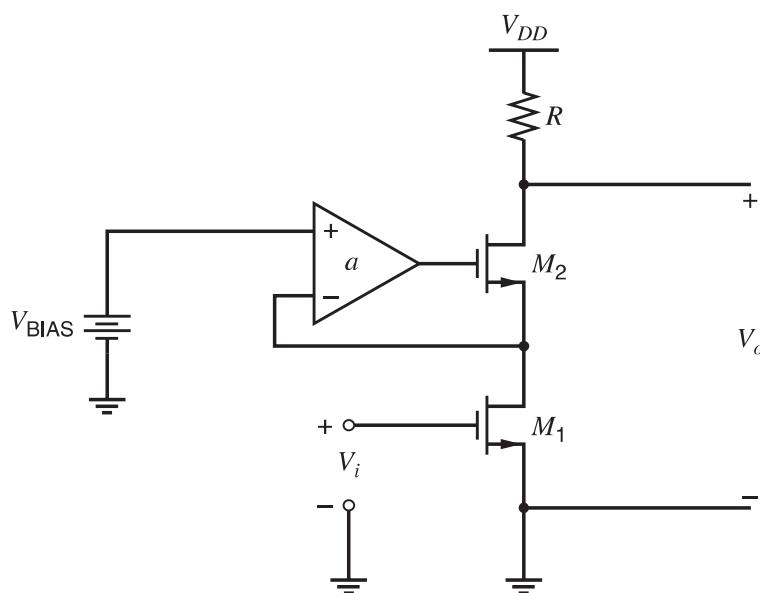


Figure 3.41 Active cascode amplifier using MOSFETs.

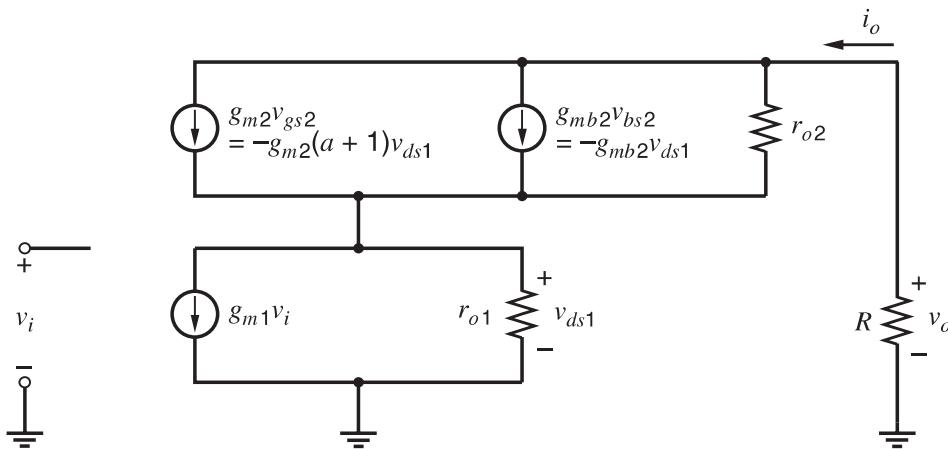


Figure 3.42 Small-signal equivalent circuit for the active-cascode connection with MOS transistors.

In contrast, $v_{gs2} = -v_{ds1}$ in a simple cascode because the voltage from the gate of M_2 to ground is constant in Fig. 3.38. Therefore, if $a > 0$, the factor $(a + 1)$ in (3.131) amplifies the gate-source voltage of M_2 compared to the case of a simple cascode. This amplification is central to the characteristics of the active-cascode circuit. Since the small-signal diagrams of the simple and active-cascode circuits are identical except for the value of v_{gs2} , and since v_{gs2} is only used to control the current flowing in the g_{m2} generator, the active-cascode circuit can be analyzed using the equations for the simple cascode with g_{m2} replaced by $(a + 1) g_{m2}$. In other words, the active cascode behaves as if it were a simple cascode with an enhanced value of g_{m2} .

To find the transconductance of the active cascode, $g_{m2}(a + 1)$ replaces g_{m2} in (3.126), giving

$$G_m = g_{m1} \left(1 - \frac{1}{1 + [g_{m2}(a + 1) + g_{mb2}] r_{o1} + \frac{r_{o1}}{r_{o2}}} \right) \quad (3.132)$$

Again, $G_m \approx g_{m1}$ under most conditions; therefore, the active-cascode structure is generally not used to modify the transconductance.

The active cascode reduces R_{i2} , the resistance looking into the source of M_2 , compared to the simple cascode, which reduces the v_{ds1}/v_o ratio given in (3.130) and increases the output resistance. Substituting (3.130) into (3.129) with $g_{m2}(a + 1)$ replacing g_{m2} gives

$$R_o = r_{o1} + r_{o2} + [g_{m2}(a + 1) + g_{mb2}] r_{o1} r_{o2} \approx [g_{m2}(a + 1) + g_{mb2}] r_{o1} r_{o2} \quad (3.133)$$

This result can also be derived by substituting $g_{m2}(a + 1)$ for g_{m2} in (3.128). Equation 3.133 shows that the active-cascode configuration increases the output resistance by a factor of about $[g_m(a + 1) + g_{mb}] r_o$ compared to a common-source amplifier.

A key limitation of the active-cascode circuit is that the output impedance is increased only at frequencies where the amplifier that drives the gate of M_2 provides some gain. In practice, the gain of this amplifier falls with increasing frequency, reducing the potential benefits of the active-cascode circuits in high-frequency applications. A potential problem with the active-cascode configuration is that the negative feedback loop through M_2 may not be stable in all cases.

3.4.4 The Super Source Follower → IDEM 3.4.3

Equation 3.84 shows that the output resistance of a source follower is approximately $1/(g_m + g_{mb})$. Because MOS transistors usually have much lower transconductance than their bipolar counterparts, this output resistance may be too high for some applications, especially when a resistive load must be driven. One way to reduce the output resistance is to increase the transconductance by increasing the W/L ratio of the source follower and its dc bias current. However, this approach requires a proportionate increase in the area and power dissipation to reduce R_o . To minimize the area and power dissipation required to reach a given output resistance, the super source follower configuration shown in Fig. 3.43 is sometimes used. This circuit uses negative feedback through M_2 to reduce the output resistance. Negative feedback is studied quantitatively in Chapter 8. From a qualitative standpoint, when the input voltage is constant and the output voltage increases, the magnitude of the drain current of M_1 also increases, in turn increasing the gate-source voltage of M_2 . As a result, the drain current of M_2 increases, reducing the output resistance by increasing the total current that flows into the output node under these conditions.

From a dc standpoint, the bias current in M_2 is the difference between I_1 and I_2 ; therefore, $I_1 > I_2$ is required for proper operation. This information can be used to find the small-signal parameters of both transistors. The small-signal equivalent circuit is shown in Fig. 3.44. The body-effect transconductance generator for M_2 is inactive because $v_{bs2} = 0$. Also, the polarities of the voltage-controlled current sources for *n*- and *p*-channel devices are identical. Finally, the output resistances of current sources I_1 and I_2 are represented by r_1 and r_2 , respectively.

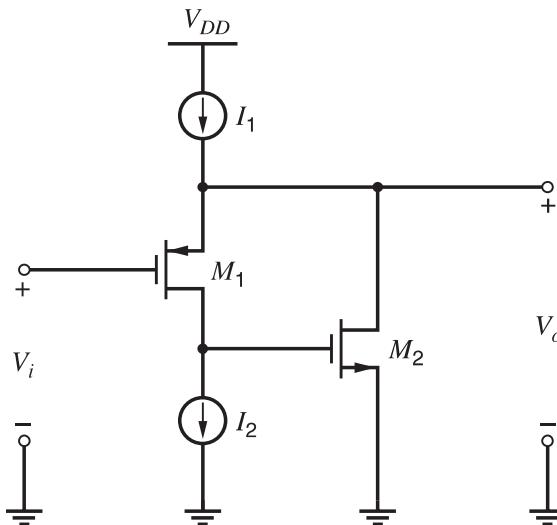


Figure 3.43 Super-source-follower configuration.

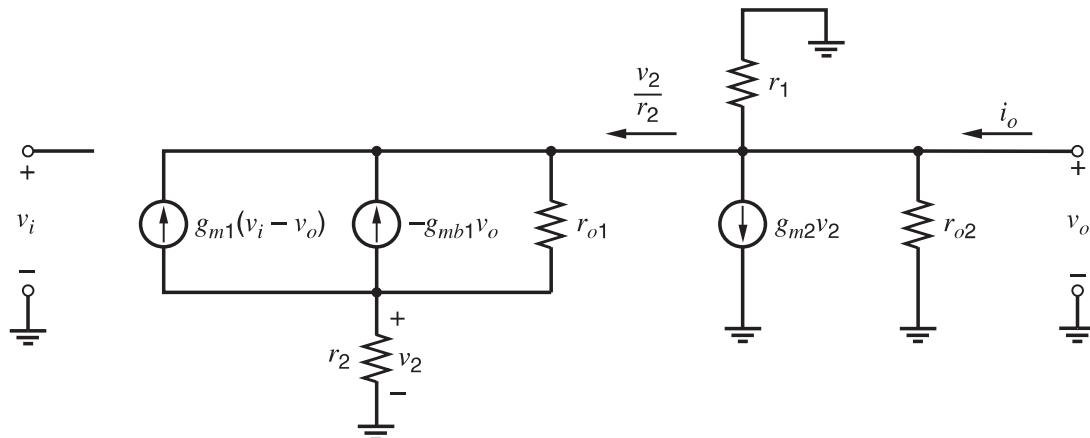


Figure 3.44 Small-signal equivalent circuit of the super-source follower.

If the current sources are ideal, $r_1 \rightarrow \infty$ and $r_2 \rightarrow \infty$. In practice, these resistances are large but finite. Techniques to build high-resistance current sources are considered in Chapter 4.

To find the output resistance, set $v_i = 0$ and calculate the current i_o that flows in the output node when the output is driven by a voltage v_o . From KCL at the output under these conditions,

$$i_o = \frac{v_o}{r_1} + \frac{v_o}{r_{o2}} + g_{m2}v_2 + \frac{v_2}{r_2} \quad (3.134)$$

From KCL at the drain of M_1 with $v_i = 0$,

$$\frac{v_2}{r_2} - g_{m1}v_o - g_{mb1}v_o + \frac{v_2 - v_o}{r_{o1}} = 0 \quad (3.135)$$

Solving (3.135) for v_2 , substituting into (3.134), and rearranging gives

$$R_o = \left. \frac{v_o}{i_o} \right|_{v_i=0} = r_1 \parallel r_{o2} \parallel \left(\frac{r_{o1} + r_2}{[1 + (g_{m1} + g_{mb1}) r_{o1}] (1 + g_{m2} r_2)} \right) \quad (3.136)$$

Assume I_1 and I_2 are ideal current sources so that $r_1 \rightarrow \infty$ and $r_2 \rightarrow \infty$. If $r_{o2} \rightarrow \infty$, and if $(g_{m1} + g_{mb1}) r_{o1} \gg 1$,

$$R_o \simeq \frac{1}{g_{m1} + g_{mb1}} \left(\frac{1}{g_{m2} r_{o1}} \right) \quad (3.137)$$

Comparing (3.84) and (3.137) shows that the negative feedback through M_2 reduces the output resistance by a factor of about $g_{m2} r_{o1}$.

Now we will calculate the open-circuit voltage gain of the super-source follower. With the output open circuited, KCL at the output node gives

$$\frac{v_o}{r_1} + \frac{v_o}{r_{o2}} + g_{m2}v_2 + \frac{v_2}{r_2} = 0 \quad (3.138)$$

From KCL at the drain of M_1 ,

$$\frac{v_2}{r_2} + g_{m1}(v_i - v_o) - g_{mb1}v_o + \frac{v_2 - v_o}{r_{o1}} = 0 \quad (3.139)$$

Solving (3.138) for v_2 , substituting into (3.139), and rearranging gives

$$\left. \frac{v_o}{v_i} \right|_{i_o=0} = \frac{g_{m1} r_{o1}}{1 + (g_{m1} + g_{mb1}) r_{o1} + \frac{(r_2 + r_{o1})}{(r_1 \parallel r_{o2})(1 + g_{m2} r_2)}} \quad (3.140)$$

With ideal current sources,

$$\lim_{\substack{r_1 \rightarrow \infty \\ r_2 \rightarrow \infty}} \left. \frac{v_o}{v_i} \right|_{i_o=0} = \frac{g_{m1} r_{o1}}{1 + (g_{m1} + g_{mb1}) r_{o1} + \frac{1}{g_{m2} r_{o2}}} \quad (3.141)$$

Comparing (3.141) and (3.81) shows that the deviation of this gain from unity is greater than with a simple source follower. If $g_{m2} r_{o2} \gg 1$, however, the difference is small and the main conclusion is that the super-source-follower configuration has little effect on the open-circuit voltage gain.

As mentioned earlier, the super-source follower is sometimes used in MOS technologies to reduce the source-follower output resistance. It is also used in bipolar technologies in output stages to reduce the current conducted in a weak lateral *pnp* transistor. This application is

described in Chapter 5. The main potential problem with the super-source-follower configuration is that the negative feedback loop through M_2 may not be stable in all cases, especially when driving a capacitive load. The stability of feedback amplifiers is considered in Chapter 9.

De acá en adelante se va a la mierda. La verdad que ni siquiera me fue tan útil esta parte, pero bueno, tampoco perdí tanto tiempo.

3.5 Differential Pairs

The differential pair is another example of a circuit that was first invented for use with vacuum tubes.¹⁰ The original circuit uses two vacuum tubes whose cathodes are connected together. Modern differential pairs use bipolar or MOS transistors coupled at their emitters or sources, respectively, and are perhaps the most widely used two-transistor subcircuits in monolithic analog circuits. The usefulness of the differential pair stems from two key properties. First, cascades of differential pairs can be directly connected to one another without interstage coupling capacitors. Second, the differential pair is primarily sensitive to the difference between two input voltages, allowing a high degree of rejection of signals common to both inputs.^{11,12} In this section, we consider the properties of emitter-coupled pairs of bipolar transistors and source-coupled pairs of MOS transistors in detail.

3.5.1 The dc Transfer Characteristic of an Emitter-Coupled Pair

The simplest form of an emitter-coupled pair is shown in Fig. 3.45. The biasing circuit in the lead connected to the emitters of Q_1 and Q_2 can be a transistor current source, which is called a *tail* current source, or a simple resistor. If a simple resistor R_{TAIL} is used alone, $I_{TAIL} = 0$ in Fig. 3.45. Otherwise, I_{TAIL} and R_{TAIL} together form a Norton-equivalent model of the tail current source.

The large-signal behavior of the emitter-coupled pair is important in part because it illustrates the limited range of input voltages over which the circuit behaves almost linearly. Also, the large-signal behavior shows that the amplitude of analog signals in bipolar circuits can be limited without pushing the transistors into saturation, where the response time would be increased because of excess charge storage in the base region. For simplicity in the analysis, we assume that the output resistance of the tail current source $R_{TAIL} \rightarrow \infty$, that the output resistance of each transistor $r_o \rightarrow \infty$, and that the base resistance of each transistor $r_b = 0$. These

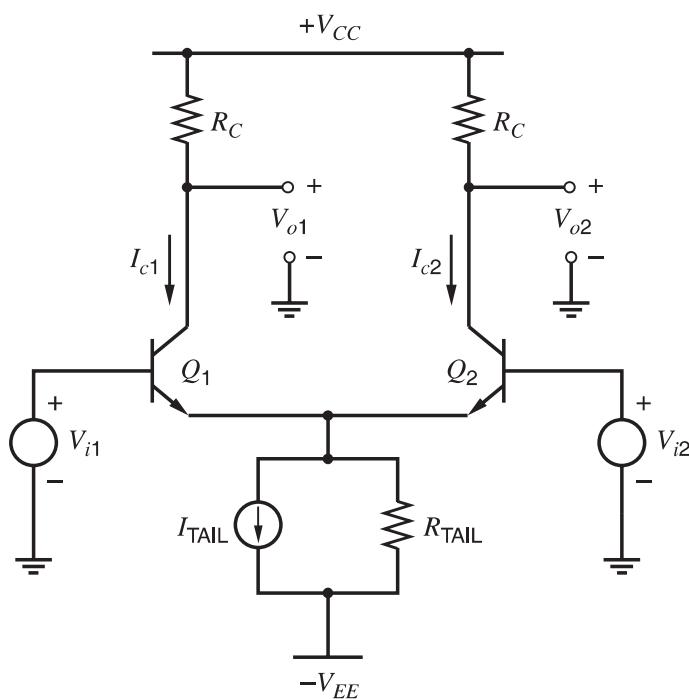


Figure 3.45 Emitter-coupled pair circuit diagram.

assumptions do not strongly affect the low-frequency, large-signal behavior of the circuit. From KVL around the input loop,

$$V_{i1} - V_{be1} + V_{be2} - V_{i2} = 0 \quad (3.142)$$

Assume the collector resistors are small enough that the transistors do not operate in saturation if $V_{i1} \leq V_{CC}$ and $V_{i2} \leq V_{CC}$. If $V_{be1} \gg V_T$ and $V_{be2} \gg V_T$, the Ebers-Moll equations show that

$$V_{be1} = V_T \ln \frac{I_{c1}}{I_{S1}} \quad (3.143)$$

$$V_{be2} = V_T \ln \frac{I_{c2}}{I_{S2}} \quad (3.144)$$

Assume the transistors are identical so that $I_{S1} = I_{S2}$. Then combining (3.142), (3.143), and (3.144), we find

$$\frac{I_{c1}}{I_{c2}} = \exp \left(\frac{V_{i1} - V_{i2}}{V_T} \right) = \exp \left(\frac{V_{id}}{V_T} \right) \quad (3.145)$$

where $V_{id} = V_{i1} - V_{i2}$. Since we have assumed that the transistors are identical, $\alpha_{F1} = \alpha_{F2} = \alpha_F$. Then KCL at the emitters of the transistors shows

$$-(I_{e1} + I_{e2}) = I_{TAIL} = \frac{I_{c1} + I_{c2}}{\alpha_F} \quad (3.146)$$

Combining (3.145) and (3.146), we find that

$$I_{c1} = \frac{\alpha_F I_{TAIL}}{1 + \exp \left(-\frac{V_{id}}{V_T} \right)} \quad (3.147)$$

$$I_{c2} = \frac{\alpha_F I_{TAIL}}{1 + \exp \left(\frac{V_{id}}{V_T} \right)} \quad (3.148)$$

These two currents are shown as a function of V_{id} in Fig. 3.46. When the magnitude of V_{id} is greater than about 3 V_T , which is approximately 78 mV at room temperature, the collector currents are almost independent of V_{id} because one of the transistors turns off and the other conducts all the current that flows. Furthermore, the circuit behaves in an approximately

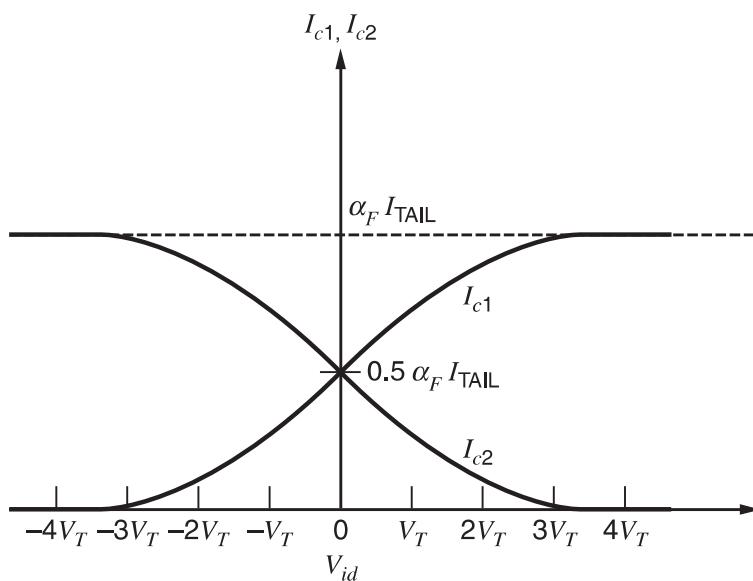


Figure 3.46 Emitter-coupled pair collector currents as a function of differential input voltage.

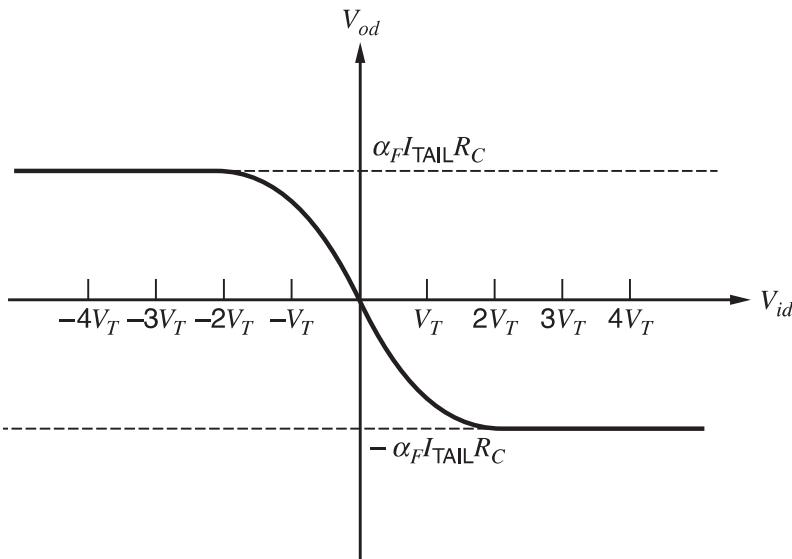


Figure 3.47 Emitter-coupled pair, differential output voltage as a function of differential input voltage.

linear fashion only when the magnitude of V_{id} is less than about V_T . We can now compute the output voltages as

$$V_{o1} = V_{CC} - I_{c1} R_C \quad (3.149)$$

$$V_{o2} = V_{CC} - I_{c2} R_C \quad (3.150)$$

The output signal of interest is often the difference between V_{o1} and V_{o2} , which we define as V_{od} . Then

$$V_{od} = V_{o1} - V_{o2} = \alpha_F I_{TAIL} R_C \tanh\left(\frac{-V_{id}}{2V_T}\right) \quad (3.151)$$

This function is plotted in Fig. 3.47. Here a significant advantage of differential amplifiers is apparent: When V_{id} is zero, V_{od} is zero if Q_1 and Q_2 are identical and if identical resistors are connected to the collectors of Q_1 and Q_2 . This property allows direct coupling of cascaded stages without offsets.

3.5.2 The dc Transfer Characteristic with Emitter Degeneration

To increase the range of V_{id} over which the emitter-coupled pair behaves approximately as a linear amplifier, emitter-degeneration resistors are frequently included in series with the emitters of the transistors, as shown in Fig. 3.48. The analysis of this circuit proceeds in the same manner as without degeneration, except that the voltage drop across these resistors must be included in the KVL equation corresponding to (3.142). A transcendental equation results from this analysis and a closed-form solution like that of (3.151) does not exist, but the effect of the resistors may be understood intuitively from the examples plotted in Fig. 3.49. For large values of emitter-degeneration resistors, the linear range of operation is extended by an amount approximately equal to $I_{TAIL} R_E$. This result stems from the observation that all of I_{TAIL} flows in one of the degeneration resistors when one transistor turns off. Therefore, the voltage drop is $I_{TAIL} R_E$ on one resistor and zero on the other, and the value of V_{id} required to turn one transistor off is changed by the difference of the voltage drops on these resistors. Furthermore, since the voltage gain is the slope of the transfer characteristic, the voltage gain is reduced by approximately the same factor that the input range is increased. In operation, the emitter resistors introduce local negative feedback in the differential pair. This topic is considered in Chapter 8.

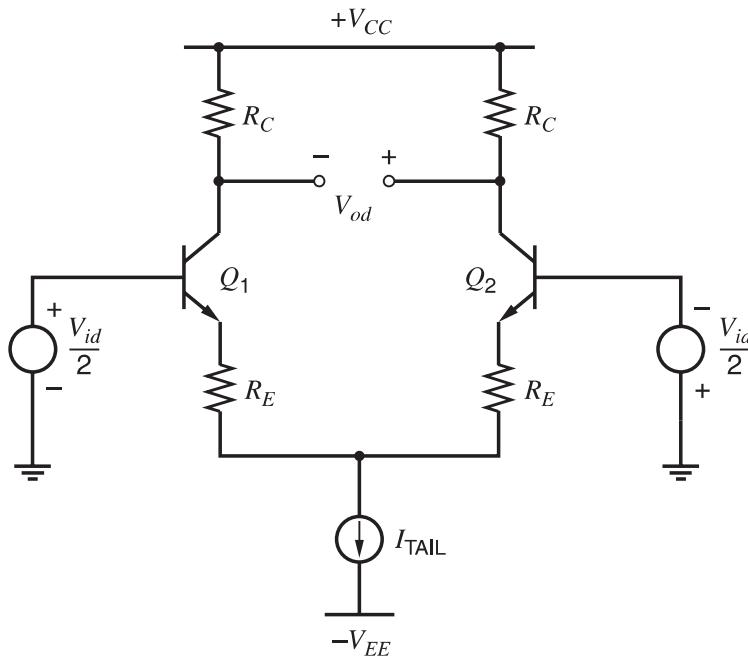


Figure 3.48 Circuit diagram of emitter-coupled pair with emitter degeneration.

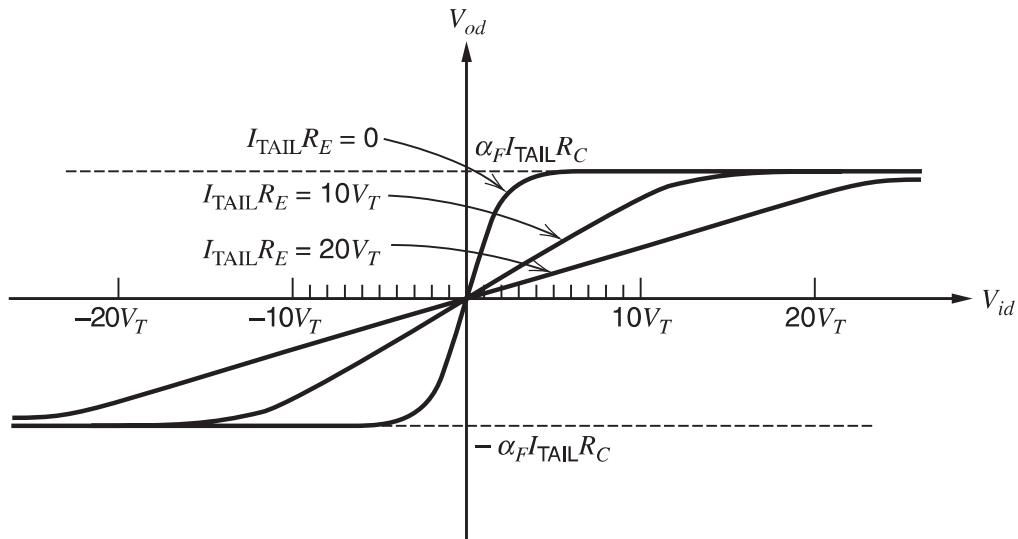


Figure 3.49 Output voltage as a function of input voltage, emitter-coupled pair with emitter degeneration.

3.5.3 The dc Transfer Characteristic of a Source-Coupled Pair

Consider the *n*-channel MOS-transistor source-coupled pair shown in Fig. 3.50. The following analysis applies equally well to a corresponding *p*-channel source-coupled pair with appropriate sign changes. In monolithic form, a transistor current source, called a *tail* current source, is usually connected to the sources of M_1 and M_2 . In that case, I_{TAIL} and R_{TAIL} together form a Norton-equivalent model of the tail current source.

For this large-signal analysis, we assume that the output resistance of the tail current source is $R_{TAIL} \rightarrow \infty$. Also, we assume that the output resistance of each transistor $r_o \rightarrow \infty$. Although these assumptions do not strongly affect the low-frequency, large-signal behavior of the circuit, they could have a significant impact on the small-signal behavior. Therefore, we will reconsider these assumptions when we analyze the circuit from a small-signal standpoint. From KVL around the input loop,

$$V_{i1} - V_{gs1} + V_{gs2} - V_{i2} = 0 \quad (3.152)$$

We assume that the drain resistors are small enough that neither transistor operates in the triode region if $V_{i1} \leq V_{DD}$ and $V_{i2} \leq V_{DD}$. Furthermore, we assume that the drain current of each

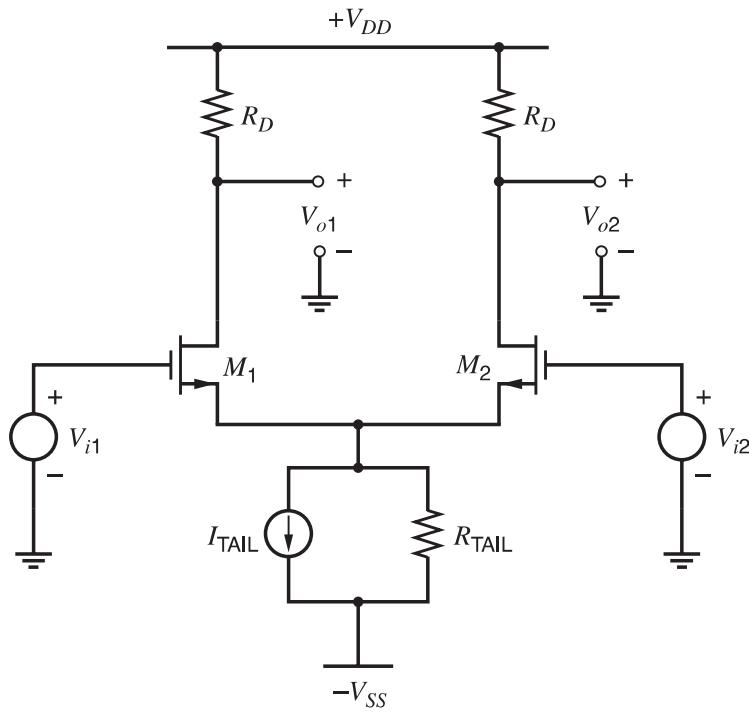


Figure 3.50 *n*-channel MOSFET source-coupled pair.

transistor is related to its gate-source voltage by the approximate square-law relationship given in (1.157). If the transistors are identical, applying (1.157) to each transistor and rearranging gives

$$V_{gs1} = V_t + \sqrt{\frac{2I_{d1}}{k' (W/L)}} \quad (3.153)$$

and

$$V_{gs2} = V_t + \sqrt{\frac{2I_{d2}}{k' (W/L)}} \quad (3.154)$$

Substituting (3.153) and (3.154) into (3.152) and rearranging gives

$$V_{id} = V_{i1} - V_{i2} = \frac{\sqrt{I_{d1}} - \sqrt{I_{d2}}}{\sqrt{\frac{k' W}{2 L}}} \quad (3.155)$$

From KCL at the source of M_1 and M_2 ,

$$I_{d1} + I_{d2} = I_{TAIL} \quad (3.156)$$

Solving (3.156) for I_{d2} , substituting into (3.155), rearranging, and using the quadratic formula gives

$$I_{d1} = \frac{I_{TAIL}}{2} \pm \frac{k' W}{4 L} V_{id} \sqrt{\frac{4I_{TAIL}}{k' (W/L)} - V_{id}^2} \quad (3.157)$$

Since $I_{d1} > I_{TAIL}/2$ when $V_{id} > 0$, the potential solution where the second term is subtracted from the first in (3.157) cannot occur in practice. Therefore,

$$I_{d1} = \frac{I_{TAIL}}{2} + \frac{k' W}{4 L} V_{id} \sqrt{\frac{4I_{TAIL}}{k' (W/L)} - V_{id}^2} \quad (3.158)$$

Substituting (3.158) into (3.156) gives

$$I_{d2} = \frac{I_{\text{TAIL}}}{2} - \frac{k' W}{4 L} V_{id} \sqrt{\frac{4I_{\text{TAIL}}}{k' (W/L)} - V_{id}^2} \quad (3.159)$$

Equations 3.158 and 3.159 are valid when both transistors operate in the active or saturation region. Since we have assumed that neither transistor operates in the triode region, the limitation here stems from turning off one of the transistors. When M_1 turns off, $I_{d1} = 0$ and $I_{d2} = I_{\text{TAIL}}$. On the other hand, $I_{d1} = I_{\text{TAIL}}$ and $I_{d2} = 0$ when M_2 turns off. Substituting these values in (3.155) shows that both transistors operate in the active region if

$$|V_{id}| \leq \sqrt{\frac{2I_{\text{TAIL}}}{k' (W/L)}} \quad (3.160)$$

Since $I_{d1} = I_{d2} = I_{\text{TAIL}}/2$ when $V_{id} = 0$, the range in (3.160) can be rewritten as

$$|V_{id}| \leq \sqrt{2} \left(\sqrt{\frac{2I_{d1}}{k' (W/L)}} \right) \Big|_{V_{id}=0} = \sqrt{2} (V_{ov})|_{V_{id}=0} \quad (3.161)$$

Equation 3.161 shows that the range of V_{id} for which both transistors operate in the active region is proportional to the overdrive calculated when $V_{id} = 0$. This result is illustrated in Fig. 3.51. The overdrive is an important quantity in MOS circuit design, affecting not only the input range of differential pairs, but also other characteristics including the speed, offset, and output swing of MOS amplifiers. Since the overdrive of an MOS transistor depends on its current and W/L ratio, the range of a source-coupled pair can be adjusted to suit a given application by adjusting the value of the tail current and/or the aspect ratio of the input devices. In contrast, the input range of the bipolar emitter-coupled pair is about $\pm 3V_T$, independent of bias current or device size. In fact, the source-coupled pair behaves somewhat like an emitter-coupled pair with emitter-degeneration resistors that can be selected to give a desired input voltage range.

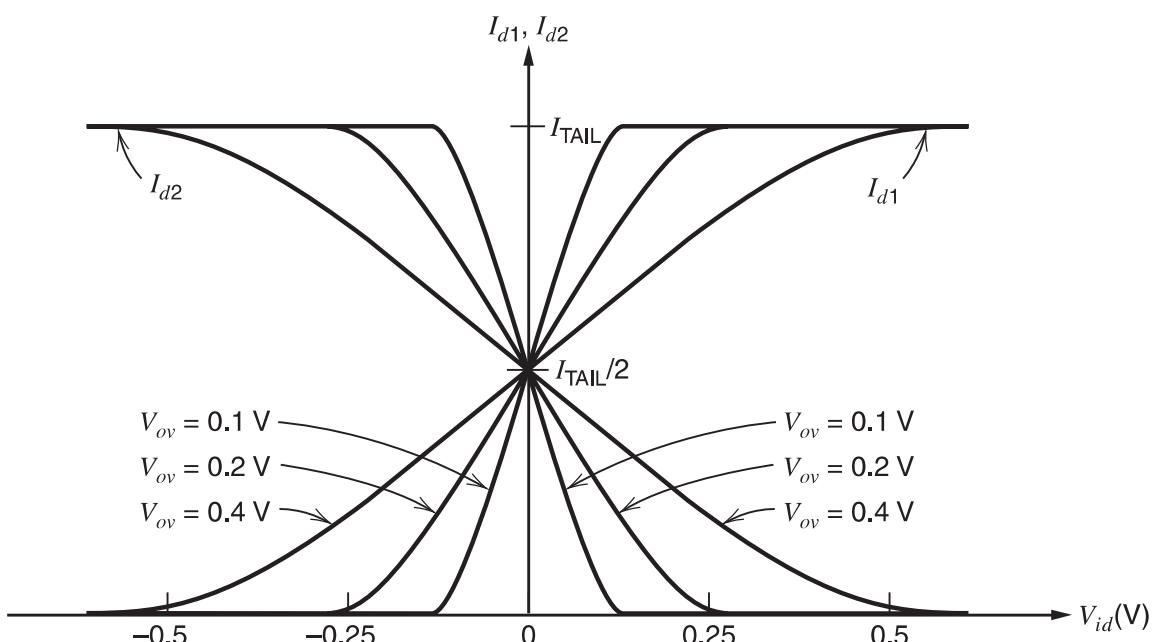


Figure 3.51 dc transfer characteristic of the MOS source-coupled pair. The parameter is the overdrive $V_{ov} = V_{GS} - V_t$ determined when $V_{id} = 0$.

In many practical cases, the key output of the differential pair is not I_{d1} or I_{d2} alone but the difference between these quantities. Subtracting (3.159) from (3.158) gives

$$\Delta I_d = I_{d1} - I_{d2} = \frac{k'}{2} \frac{W}{L} V_{id} \sqrt{\frac{4I_{TAIL}}{k' (W/L)} - V_{id}^2} \quad (3.162)$$

We can now compute the differential output voltage as

$$V_{od} = V_{o1} - V_{o2} = V_{DD} - I_{d1}R_D - V_{DD} + I_{d2}R_D = -(\Delta I_d) R_D \quad (3.163)$$

Since $\Delta I_d = 0$ when $V_{id} = 0$, (3.163) shows that $V_{od} = 0$ when $V_{id} = 0$ if M_1 and M_2 are identical and if identical resistors are connected to the drains of M_1 and M_2 . This property allows direct coupling of cascaded MOS differential pairs, as in the bipolar case.

3.5.4 Introduction to the Small-Signal Analysis of Differential Amplifiers

The features of interest in the performance of differential pairs are often the small-signal properties for dc differential input voltages near zero volts. In the next two sections, we assume that the dc differential input voltage is zero and calculate the small-signal parameters. If the parameters are constant, the small-signal model predicts that the circuit operation is linear. The results of the small-signal analysis are valid for signals that are small enough to cause insignificant nonlinearity.

In previous sections, we have considered amplifiers with two input terminals (V_i and ground) and two output terminals (V_o and ground). Small-signal analysis of such circuits leads to one equation for each circuit, such as

$$v_o = Av_i \quad (3.164)$$

Here, A is the small-signal voltage gain under given loading conditions. In contrast, differential pairs have three input terminals (V_{i1} , V_{i2} , and ground) and three output terminals (V_{o1} , V_{o2} , and ground). Therefore, direct small-signal analysis of differential pairs leads to two equations for each circuit (one for each output), where each output depends on each input:

$$v_{o1} = A_{11}v_{i1} + A_{12}v_{i2} \quad (3.165)$$

$$v_{o2} = A_{21}v_{i1} + A_{22}v_{i2} \quad (3.166)$$

Here, four voltage gains, A_{11} , A_{12} , A_{21} , and A_{22} , specify the small-signal operation of the circuit under given loading conditions. These gains can be interpreted as

$$A_{11} = \left. \frac{v_{o1}}{v_{i1}} \right|_{v_{i2}=0} \quad (3.167)$$

$$A_{12} = \left. \frac{v_{o1}}{v_{i2}} \right|_{v_{i1}=0} \quad (3.168)$$

$$A_{21} = \left. \frac{v_{o2}}{v_{i1}} \right|_{v_{i2}=0} \quad (3.169)$$

$$A_{22} = \left. \frac{v_{o2}}{v_{i2}} \right|_{v_{i1}=0} \quad (3.170)$$

Although direct small-signal analysis of differential pairs can be used to calculate these four gain values in a straightforward way, the results are difficult to interpret because differential

pairs usually are not used to react to v_{i1} or v_{i2} alone. Instead, differential pairs are used most often to sense the difference between the two inputs while trying to ignore the part of the two inputs that is common to each. Desired signals will be forced to appear as differences in differential circuits. In practice, undesired signals will also appear. For example, *mixed-signal* integrated circuits use both analog and digital signal processing, and the analog signals are vulnerable to corruption from noise generated by the digital circuits and transmitted through the common substrate. The hope in using differential circuits is that undesired signals will appear equally on both inputs and be rejected.

To highlight this behavior, we will define new differential and common-mode variables at the input and output as follows. The differential input, to which differential pairs are sensitive, is

$$v_{id} = v_{i1} - v_{i2} \quad (3.171)$$

The common-mode or average input, to which differential pairs are insensitive, is

$$v_{ic} = \frac{v_{i1} + v_{i2}}{2} \quad (3.172)$$

These equations can be inverted to give v_{i1} and v_{i2} in terms of v_{id} and v_{ic} :

$$v_{i1} = v_{ic} + \frac{v_{id}}{2} \quad (3.173)$$

$$v_{i2} = v_{ic} - \frac{v_{id}}{2} \quad (3.174)$$

The physical significance of these new variables can be understood by using (3.173) and (3.174) to redraw the input connections to a differential amplifier as shown in Fig. 3.52. The common-mode input is the input component that appears equally in v_{i1} and v_{i2} . The differential input is the input component that appears between v_{i1} and v_{i2} .

New output variables are defined in the same way. The differential output is

$$v_{od} = v_{o1} - v_{o2} \quad (3.175)$$

The common-mode or average output is

$$v_{oc} = \frac{v_{o1} + v_{o2}}{2} \quad (3.176)$$

Solving these equations for v_{o1} and v_{o2} , we obtain

$$v_{o1} = v_{oc} + \frac{v_{od}}{2} \quad (3.177)$$

$$v_{o2} = v_{oc} - \frac{v_{od}}{2} \quad (3.178)$$

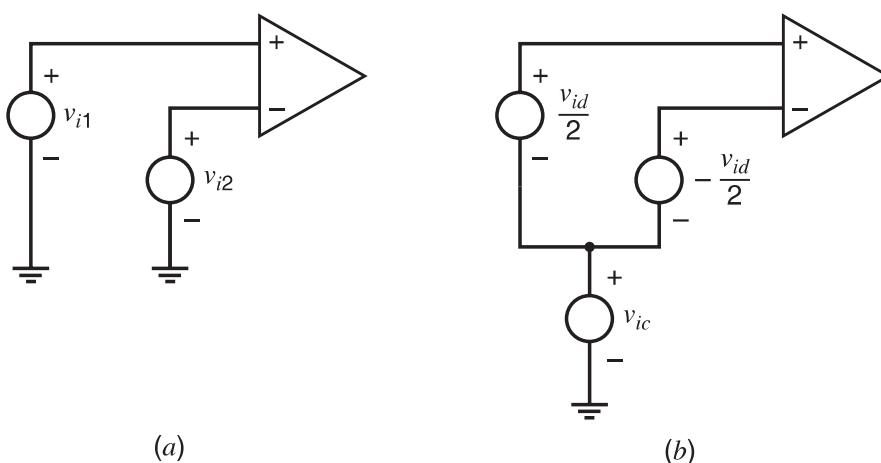


Figure 3.52 A differential amplifier with its inputs (a) shown as independent of each other and (b) redrawn in terms of the differential and common-mode components.

We have now defined two new input variables and two new output variables. By substituting the expressions for v_{i1} , v_{i2} , v_{o1} , and v_{o2} in terms of the new variables back into (3.165) and (3.166), we find

$$v_{od} = \left(\frac{A_{11} - A_{12} - A_{21} + A_{22}}{2} \right) v_{id} + (A_{11} + A_{12} - A_{21} - A_{22}) v_{ic} \quad (3.179)$$

$$v_{oc} = \left(\frac{A_{11} - A_{12} + A_{21} - A_{22}}{4} \right) v_{id} + \left(\frac{A_{11} + A_{12} + A_{21} + A_{22}}{2} \right) v_{ic} \quad (3.180)$$

Defining four new gain factors that are equal to the coefficients in these equations, (3.179) and (3.180) can be rewritten as

$$v_{od} = A_{dm} v_{id} + A_{cm-dm} v_{ic} \quad (3.181)$$

$$v_{oc} = A_{dm-cm} v_{id} + A_{cm} v_{ic} \quad (3.182)$$

The *differential-mode* gain A_{dm} is the change in the differential output per unit change in differential input:

$$A_{dm} = \left. \frac{v_{od}}{v_{id}} \right|_{v_{ic}=0} = \frac{A_{11} - A_{12} - A_{21} + A_{22}}{2} \quad (3.183)$$

The *common-mode* gain A_{cm} is the change in the common-mode output voltage per unit change in the common-mode input:

$$A_{cm} = \left. \frac{v_{oc}}{v_{ic}} \right|_{v_{id}=0} = \frac{A_{11} + A_{12} + A_{21} + A_{22}}{2} \quad (3.184)$$

The *differential-mode-to-common-mode* gain A_{dm-cm} is the change in the common-mode output voltage per unit change in the differential-mode input:

*Usam la comprensión de
que es q'nos otros*

$$A_{dm-cm} = \left. \frac{v_{oc}}{v_{id}} \right|_{v_{ic}=0} = \frac{A_{11} - A_{12} + A_{21} - A_{22}}{4} \quad (3.185)$$

The *common-mode-to-differential-mode* gain A_{cm-dm} is the change in the differential-mode output voltage per unit change in the common-mode input:

$$A_{cm-dm} = \left. \frac{v_{od}}{v_{ic}} \right|_{v_{id}=0} = A_{11} + A_{12} - A_{21} - A_{22} \quad (3.186)$$

The purpose of a differential amplifier is to sense changes in its differential input while rejecting changes in its common-mode input. The desired output is differential, and its variation should be proportional to the variation in the differential input. Variation in the common-mode output is undesired because it must be rejected by another differential stage to sense the desired differential signal. Therefore, an important design goal in differential amplifiers is to make A_{dm} large compared to the other three gain coefficients in (3.181) and (3.182).

In differential amplifiers with perfect symmetry, each component on the side of one output corresponds to an identical component on the side of the other output. With such *perfectly balanced* amplifiers, when $v_{i1} = -v_{i2}$, $v_{o1} = -v_{o2}$. In other words, when the input is purely differential ($v_{ic} = 0$), the output of a perfectly balanced differential amplifier is purely differential ($v_{oc} = 0$), and thus $A_{dm-cm} = 0$. Similarly, pure common-mode inputs (for which $v_{id} = 0$) produce pure common-mode outputs and $A_{cm-dm} = 0$ in perfectly balanced differential amplifiers. Even with perfect symmetry, however, $A_{cm} \neq 0$ is possible. Therefore, the ratio A_{dm}/A_{cm} is one figure of merit for a differential amplifier, giving the ratio of the desired

differential-mode gain to the undesired common-mode gain. In this book, we will define the magnitude of this ratio as the **common-mode-rejection ratio**, CMRR:

$$\text{CMRR} \equiv \left| \frac{A_{dm}}{A_{cm}} \right| \quad (3.187)$$

Furthermore, since differential amplifiers are not perfectly balanced in practice, $A_{dm-cm} \neq 0$ and $A_{cm-dm} \neq 0$. The ratios A_{dm}/A_{cm-dm} and A_{dm}/A_{dm-cm} are two other figures of merit that characterize the performance of differential amplifiers. Of these, the first is particularly important because ratio A_{dm}/A_{cm-dm} determines the extent to which the differential output is produced by the desired differential input instead of by the undesired common-mode input. This ratio is important because once a common-mode input is converted to a differential output, the result is treated as the *desired* signal by subsequent differential amplifiers. In fact, in multistage differential amplifiers, the common-mode-to-differential-mode gain of the first stage is usually an important factor in the overall CMRR. In Section 3.5.5, we consider perfectly balanced differential amplifiers from a small-signal standpoint; in Section 3.5.6.9, imperfectly balanced differential amplifiers from the same standpoint.

3.5.5 Small-Signal Characteristics of Balanced Differential Amplifiers

In this section, we will study perfectly balanced differential amplifiers. Therefore, $A_{cm-dm} = 0$ and $A_{dm-cm} = 0$ here, and our goal is to calculate A_{dm} and A_{cm} . Although calculating A_{dm} and A_{cm} from the entire small-signal equivalent circuit of a differential amplifier is possible, these calculations are greatly simplified by taking advantage of the symmetry that exists in perfectly balanced amplifiers. In general, we first find the response of a given circuit to pure differential and pure common-mode inputs separately. Then the results can be superposed to find the total solution. Since superposition is valid only for linear circuits, the following analysis is strictly valid only from a small-signal standpoint and approximately valid only for signals that cause negligible nonlinearity. In previous sections, we carried out large-signal analyses of differential pairs and assumed that the Norton-equivalent resistance of the tail current source was infinite. Since this resistance has a considerable effect on the small-signal behavior of differential pairs, however, we now assume that this resistance is finite.

Because the analysis here is virtually the same for both bipolar and MOS differential pairs, the two cases will be considered together. Consider the bipolar emitter-coupled pair of Fig. 3.45 and the MOS source-coupled pair of Fig. 3.50 from a small-signal standpoint. Then $V_{i1} = v_{i1}$ and $V_{i2} = v_{i2}$. These circuits are redrawn in Fig. 3.53a and Fig. 3.53b with the common-mode input voltages set to zero so we can consider the effect of the differential-mode input by itself. The small-signal equivalent circuit for both cases is shown in Fig. 3.54 with R used to replace R_C in Fig. 3.53a and R_D in 3.53b. Note that the small-signal equivalent circuit neglects finite r_o in both cases. Also, in the MOS case, nonzero g_{mb} is ignored and $r_\pi \rightarrow \infty$ because $\beta_0 \rightarrow \infty$.

Because the circuit in Fig. 3.54 is perfectly balanced, and because the inputs are driven by equal and opposite voltages, the voltage across R_{TAIL} does not vary at all. Another way to see this result is to view the two lower parts of the circuit as voltage followers. When one side pulls up, the other side pulls down, resulting in a constant voltage across the tail current source by superposition. Since the voltage across R_{TAIL} experiences no variation, the behavior of the small-signal circuit is unaffected by the placement of a short circuit across R_{TAIL} , as shown in Fig. 3.55. After placing this short circuit, we see that the two sides of the circuit are not only identical, but also independent because they are joined at a node that operates as a small-signal ground. Therefore, the response to small-signal differential inputs can be determined by analyzing one side of the original circuit with R_{TAIL} replaced by a short circuit.

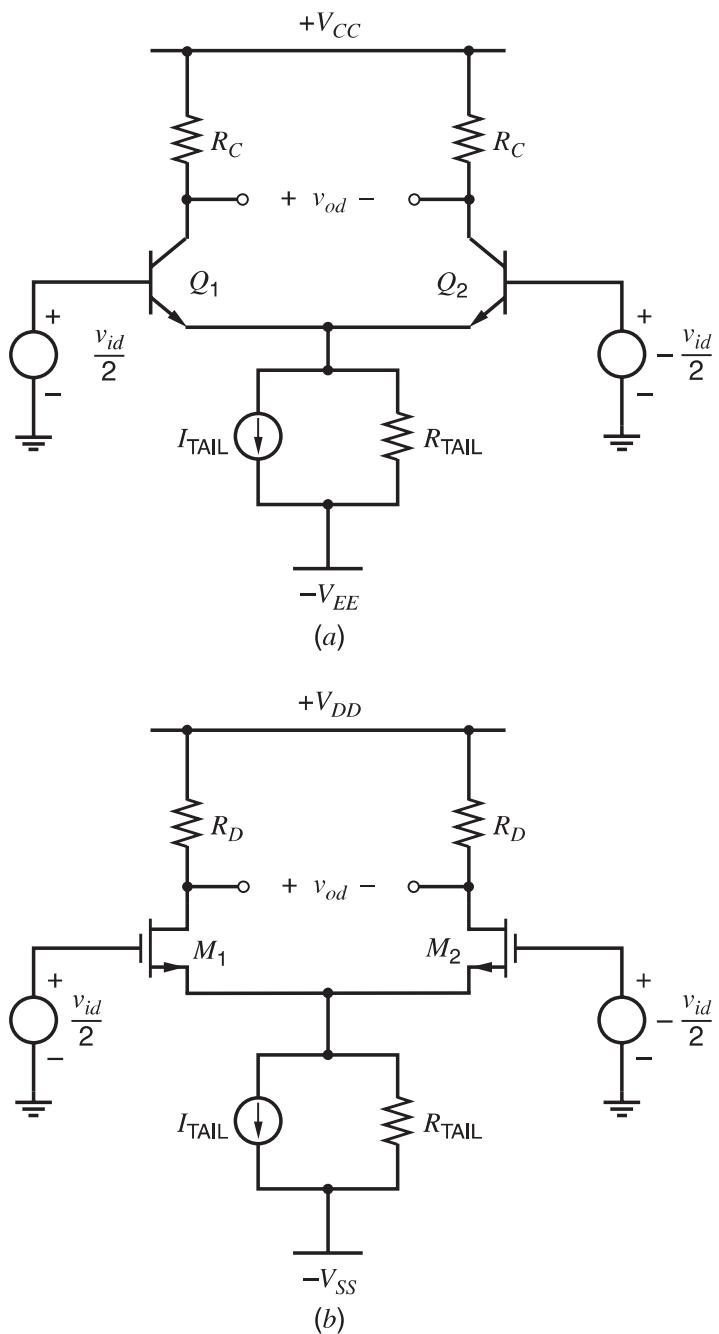


Figure 3.53 (a) Emitter-coupled pair with pure differential input. (b) Source-coupled pair with pure differential input.

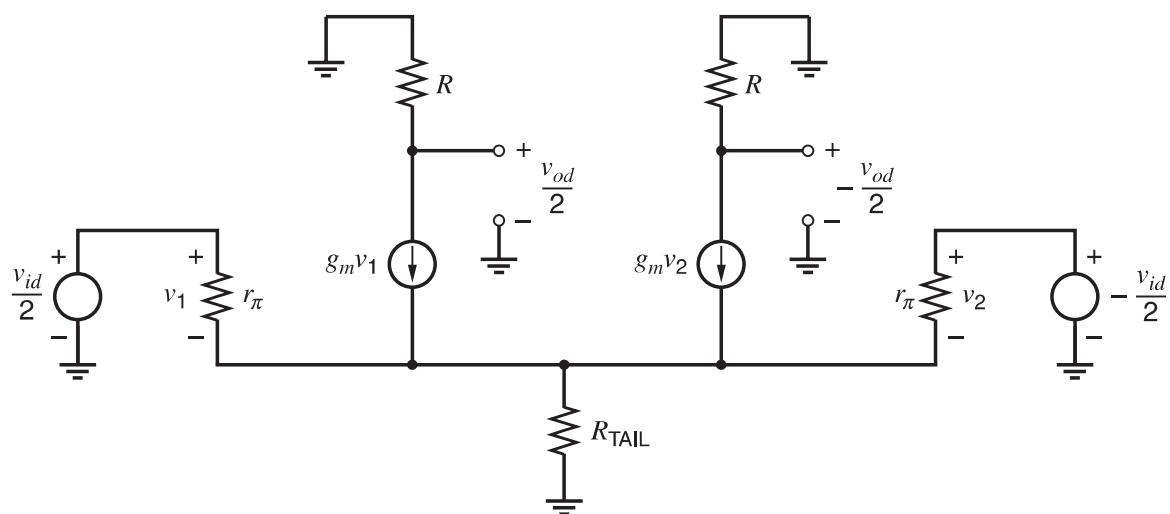


Figure 3.54 Small-signal equivalent circuit for differential pair with pure differential-mode input.

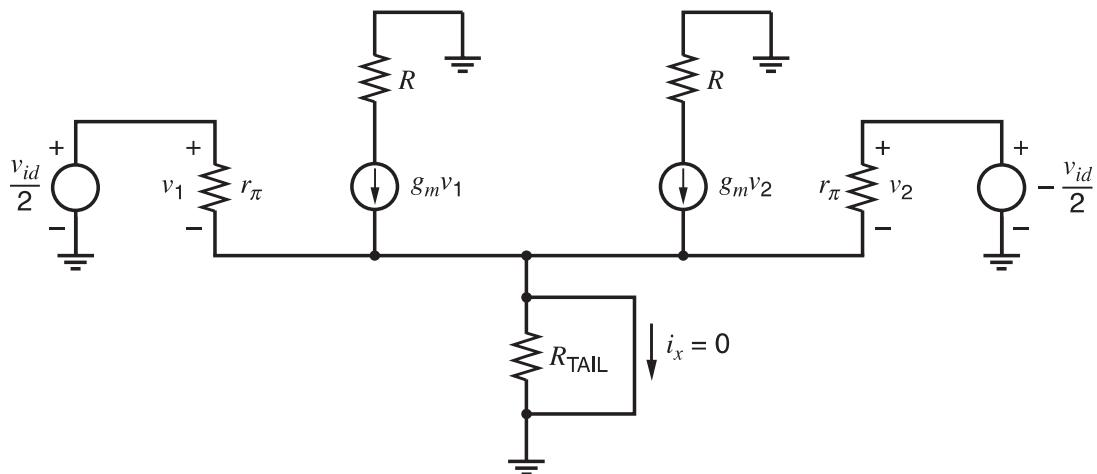


Figure 3.55 Differential-mode circuit with the tail current source grounded. Because of the symmetry of the circuit, $i_x = 0$.

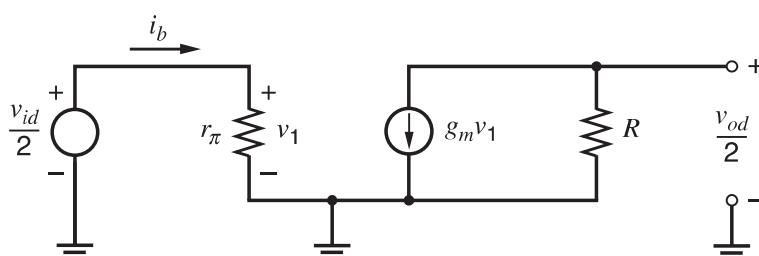


Figure 3.56 Differential-mode half circuit.

This simplified circuit, shown in Fig. 3.56, is called the *differential-mode* half circuit and is useful for analysis of both the low- and high-frequency performance of all types of differential amplifiers. By inspection of Fig. 3.56, we recognize this circuit as the small-signal equivalent of a common-emitter or common-source amplifier. Therefore,

$$\frac{v_{od}}{2} = -g_m R \frac{v_{id}}{2} \quad (3.188)$$

and

$$A_{dm} = \left. \frac{v_{od}}{v_{id}} \right|_{v_{ic}=0} = -g_m R \quad (3.189)$$

To include the output resistance of the transistor in the above analysis, R in (3.189) should be replaced by $R \parallel r_o$. Finally, note that neglecting g_{mb} from this analysis for MOS source-coupled pairs has no effect on the result because the voltage from the source to the body of the input transistors is the same as the voltage across the tail current source, which is constant with a pure differential input.

The circuits in Fig. 3.45 and Fig. 3.50 are now reconsidered from a small-signal, common-mode standpoint. Setting $V_{i1} = V_{i2} = v_{ic}$, the circuits are redrawn in Fig. 3.57a and Fig. 3.57b. The small-signal equivalent circuit is shown in Fig. 3.58, but with the modification that the resistor R_{TAIL} has been split into two parallel resistors, each of value twice the original. Also R has been used to replace R_C in Fig. 3.57a and R_D in 3.57b. Again r_o is neglected in both cases, and g_{mb} is neglected in the MOS case, where $r_\pi \rightarrow \infty$ because $\beta_0 \rightarrow \infty$.

Because the circuit in Fig. 3.58 is divided into two identical halves, and because each half is driven by the same voltage v_{ic} , no current i_x flows in the lead connecting the half circuits. The circuit behavior is thus unchanged when this lead is removed as shown in Fig. 3.59. As a result, we see that the two halves of the circuit in Fig. 3.58 are not only identical, but also independent because they are joined by a branch that conducts no small-signal current. Therefore, the response to small-signal, common-mode inputs can be determined by analyzing

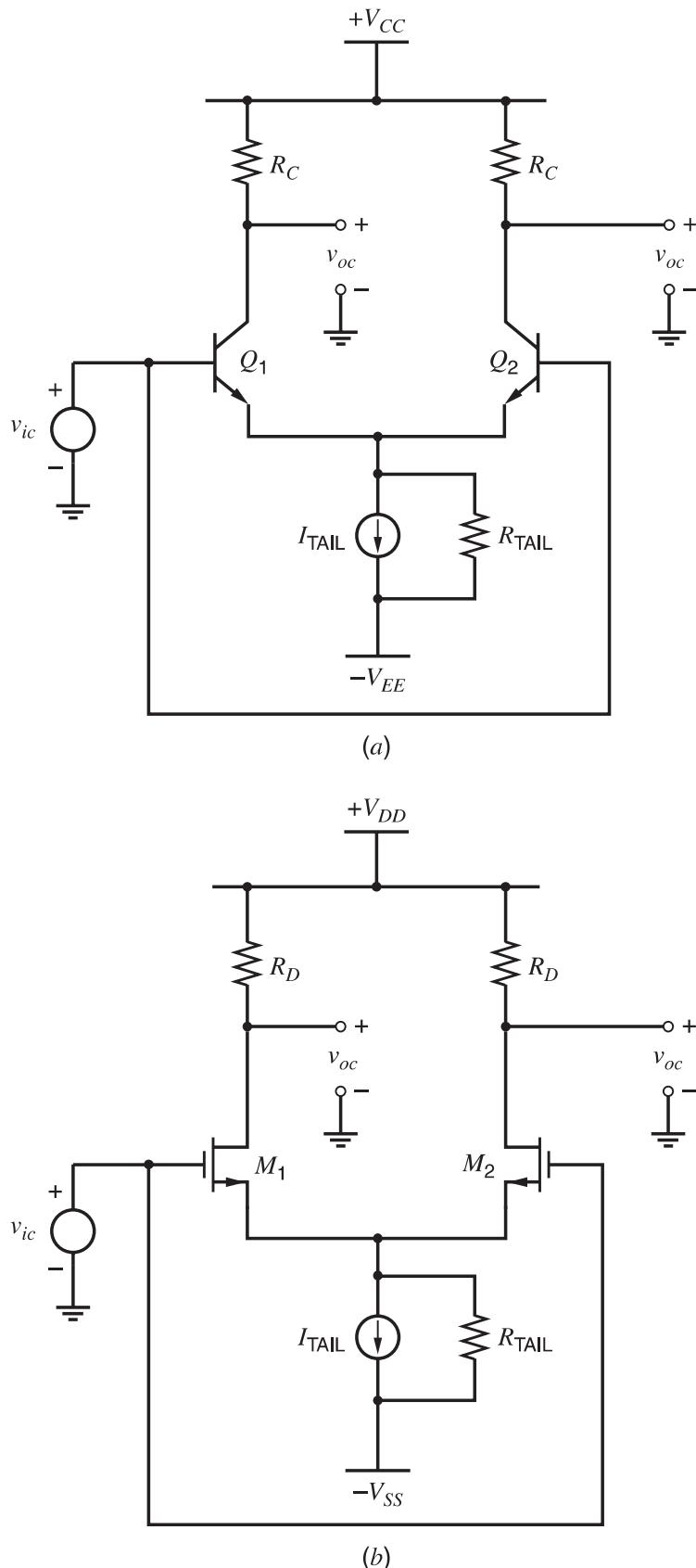


Figure 3.57 (a) Emitter-coupled pair with pure common-mode input. (b) Source-coupled pair with pure common-mode input.

one half of the original circuit with an open circuit replacing the branch that joins the two halves of the original circuit. This simplified circuit, shown in Fig. 3.60, is called the *common-mode* half circuit. By inspection of Fig. 3.60, we recognize this circuit as a common-emitter or common-source amplifier with degeneration. Then

$$v_{oc} = -G_m R v_{ic} \quad (3.190)$$

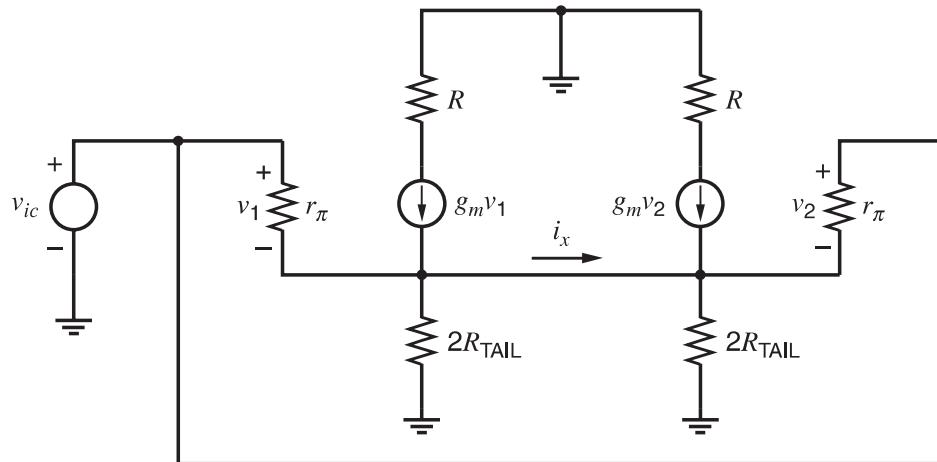


Figure 3.58 Small-signal equivalent circuit, pure common-mode input.

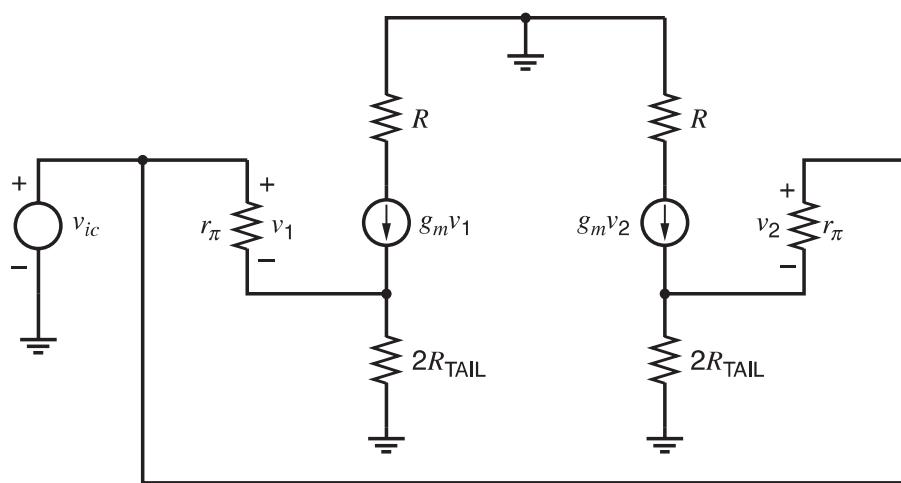


Figure 3.59 Modified common-mode equivalent circuit.

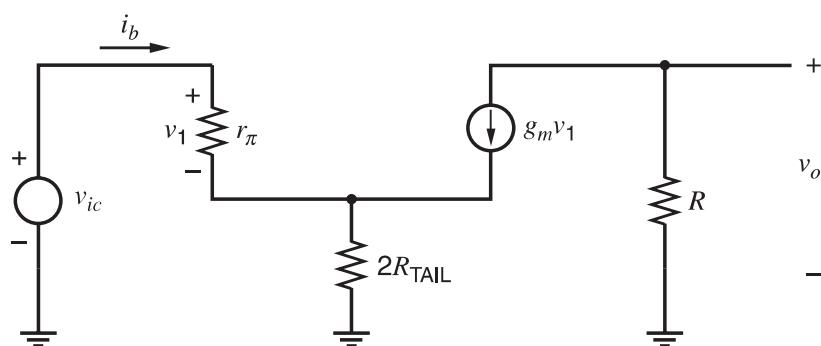


Figure 3.60 Common-mode half circuit.

and

$$A_{cm} = \left. \frac{v_{oc}}{v_{ic}} \right|_{v_{id}=0} = -G_m R \quad (3.191)$$

where G_m is the transconductance of a common-emitter or common-source amplifier with degeneration and will be considered quantitatively below. Since degeneration reduces the transconductance, and since degeneration occurs only in the common-mode case, (3.189) and (3.191) show that $|A_{dm}| > |A_{cm}|$; therefore, the differential pair is more sensitive to differential inputs than to common-mode inputs. In other words, the tail current source provides local negative feedback to common-mode inputs (or local common-mode feedback). Negative feedback is studied in Chapter 8.

Bipolar Emitter-Coupled Pair. For the bipolar case, substituting (3.93) for G_m with $R_E = 2R_{TAIL}$ into (3.191) and rearranging gives

$$A_{cm} \simeq -\frac{g_m R}{1 + g_m (2R_{TAIL})} = -\frac{g_m R}{1 + 2g_m R_{TAIL}} \quad (3.192)$$

To include the effect of finite r_o in the above analysis, R in (3.192) should be replaced by $R \parallel R_o$, where R_o is the output resistance of a common-emitter amplifier with emitter degeneration of $R_E = 2R_{TAIL}$, given in (3.97) or (3.98). This substitution ignores the effect of finite r_o on G_m , which is shown in (3.92) and is usually negligible.

The CMRR is found by substituting (3.189) and (3.192) into (3.187), which gives

$$\text{CMRR} = 1 + 2g_m R_{TAIL} \quad (3.193)$$

This expression applies to the particular case of a single-stage, emitter-coupled pair. It shows that increasing the output resistance of the tail current source R_{TAIL} improves the common-mode-rejection ratio. This topic is considered in Chapter 4.

Since bipolar transistors have finite β_0 , and since differential amplifiers are often used as the input stage of instrumentation circuits, the input resistance of emitter-coupled pairs is also an important design consideration. The differential input resistance R_{id} is defined as the ratio of the small-signal differential input voltage v_{id} to the small-signal input current i_b when a pure differential input voltage is applied. By inspecting Fig. 3.56, we find that

$$\frac{v_{id}}{2} = i_b r_\pi \quad (3.194)$$

Therefore, the differential input resistance of the emitter-coupled pair is

$$R_{id} = \left. \frac{v_{id}}{i_b} \right|_{v_{ic}=0} = 2r_\pi \quad (3.195)$$

Thus the differential input resistance depends on the r_π of the transistor, which increases with increasing β_0 and decreasing collector current. High input resistance is therefore obtained when an emitter-coupled pair is operated at low bias current levels. Techniques to achieve small bias currents are considered in Chapter 4.

The common-mode input resistance R_{ic} is defined as the ratio of the small-signal, common-mode input voltage v_{ic} to the small-signal input current i_b in one terminal when a pure common-mode input is applied. Since the common-mode half circuit in Fig. 3.60 is the same as that for a common-emitter amplifier with emitter degeneration, substituting $R_E = 2R_{TAIL}$ into (3.90) gives R_{ic} as

$$R_{ic} = \left. \frac{v_{ic}}{i_b} \right|_{v_{id}=0} = r_\pi + (\beta_0 + 1)(2R_{TAIL}) \quad (3.196)$$

The small-signal input current that flows when both common-mode and differential-mode input voltages are applied can be found by superposition and is given by

$$i_{b1} = \frac{v_{id}}{R_{id}} + \frac{v_{ic}}{R_{ic}} \quad (3.197)$$

$$i_{b2} = -\frac{v_{id}}{R_{id}} + \frac{v_{ic}}{R_{ic}} \quad (3.198)$$

where i_{b1} and i_{b2} represent the base currents of Q_1 and Q_2 , respectively.

The input resistance can be represented by the π equivalent circuit of Fig. 3.61a or by the T-equivalent circuit of Fig. 3.61b. For the π model, the common-mode input resistance is exactly R_{ic} independent of R_x . To make the differential-mode input resistance exactly R_{id} , the

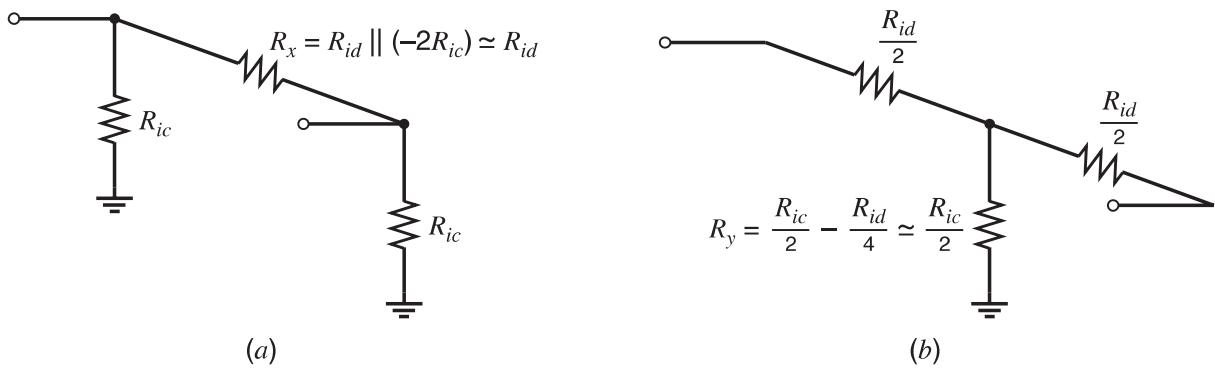


Figure 3.61 (a) General low-frequency, small-signal, π -equivalent input circuit for the differential amplifier. (b) T-equivalent input circuit.

value of R_x should be more than R_{id} to account for nonzero current in R_{ic} . On the other hand, for the T model, the differential-mode input resistance is exactly R_{id} independent of R_y , and the common-mode input resistance is R_{ic} if R_y is chosen to be less than $R_{ic}/2$ as shown. The approximations in Fig. 3.61 are valid if R_{ic} is much larger than R_{id} .

MOS Source-Coupled Pair. For the MOS case, substituting (3.104) for G_m with $g_{mb} = 0$ and $R_S = 2R_{TAIL}$ into (3.191) and rearranging gives

$$A_{cm} \approx -\frac{g_m R}{1 + g_m (2R_{TAIL})} = -\frac{g_m R}{1 + 2g_m R_{TAIL}} \quad (3.199)$$

Although (3.199) and the common-mode half circuit in Fig. 3.60 ignore the body-effect transconductance g_{mb} , the common-mode gain depends on g_{mb} in practice because the body effect changes the source-body voltage of the transistors in the differential pair. Since nonzero g_{mb} was included in the derivation of the transconductance of the common-source amplifier with degeneration, a simple way to include the body effect here is to allow nonzero g_{mb} when substituting (3.104) into (3.191). The result is

$$A_{cm} \approx -\frac{g_m R}{1 + (g_m + g_{mb})(2R_{TAIL})} = -\frac{g_m R}{1 + 2(g_m + g_{mb}) R_{TAIL}} \quad (3.200)$$

To include the effect of finite r_o in the above analysis, R in (3.199) and (3.200) should be replaced by $R \parallel R_o$, where R_o is the output resistance of a common-source amplifier with source degeneration of $R_S = 2R_{TAIL}$, given in (3.107). This substitution ignores the effect of finite r_o on G_m , which is shown in (3.103) and is usually negligible.

The CMRR is found by substituting (3.189) and (3.200) into (3.187), which gives

$$\text{CMRR} \approx 1 + 2(g_m + g_{mb}) R_{TAIL} \quad (3.201)$$

Equation 3.201 is valid for a single-stage, source-coupled pair and shows that increasing R_{TAIL} increases the CMRR. This topic is studied in Chapter 4.

3.5.6 Device Mismatch Effects in Differential Amplifiers

An important aspect of the performance of differential amplifiers is the minimum dc and ac differential voltages that can be detected. The presence of component mismatches within the amplifier itself and drifts of component values with temperature produce dc differential voltages at the output that are indistinguishable from the dc component of the signal being amplified. Also, such mismatches and drifts cause nonzero common-mode-to-differential-mode gain as well as nonzero differential-to-common-mode gain to arise. Nonzero A_{cm-dm} is especially important because it converts common-mode inputs to differential outputs, which

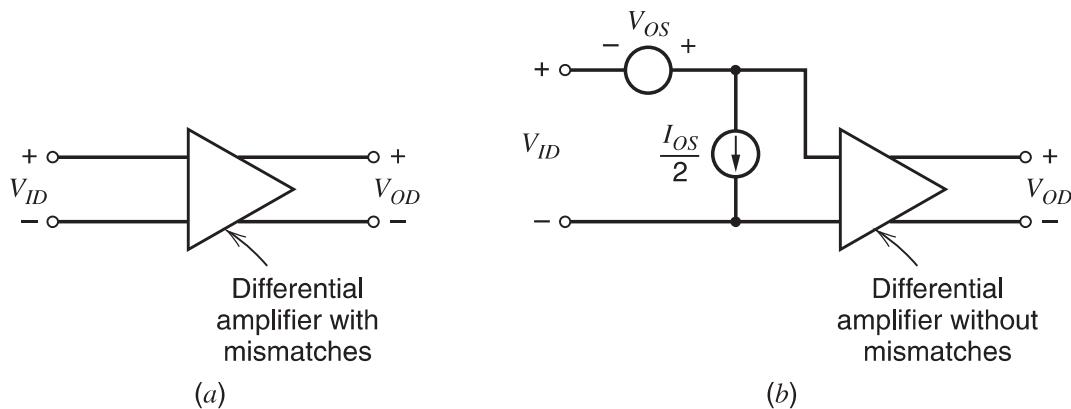


Figure 3.62 Equivalent input offset voltage (V_{OS}) and current (I_{OS}) for a differential amplifier. (a) Actual circuit containing mismatches. (b) Equivalent dc circuit with identically matched devices and the offset voltage and current referred to the input.

are treated as the desired signal by subsequent stages. In many analog systems, these types of errors pose the basic limitation on the resolution of the system, and hence consideration of mismatch-induced effects is often central to the design of analog circuits.

3.5.6.1 Input Offset Voltage and Current

For differential amplifiers, the effect of mismatches on dc performance is most conveniently represented by two quantities, the input offset voltage and the input offset current. These quantities represent the input-referred effect of all the component mismatches within the amplifier on its dc performance.^{11,12} As illustrated in Fig. 3.62, the dc behavior of the amplifier containing the mismatches is identical to an ideal amplifier with no mismatches but with the input offset voltage source added in series with the input and the input offset current source in shunt across the input terminals. Both quantities are required to represent the effect of mismatch in general so that the model is valid for any source resistance. For example, if the input terminals are driven by an ideal voltage source with zero resistance, the input offset current does not contribute to the amplifier output, and the offset voltage generator is needed to model the effect of mismatch. On the other hand, if the input terminals are driven by an ideal current source with infinite resistance, the input offset voltage does not contribute to the amplifier output, and the offset current generator is needed to model the effect of mismatch. These quantities are usually a function of both temperature and common-mode input voltage. In the next several sections, we calculate the input offset voltage and current of the emitter-coupled pair and the source-coupled pair.

3.5.6.2 Input Offset Voltage of the Emitter-Coupled Pair

The predominant sources of offset error in the emitter-coupled pair are the mismatches in the base width, base doping level, and collector doping level of the transistors, mismatches in the effective emitter area of the transistors, and mismatches in the collector load resistors. To provide analytical results simple enough for intuitive interpretation, the analysis will be carried out assuming a uniform-base transistor. The results are similar for the nonuniform case, although the analytical procedure is more tedious. In most instances the dc base current is low enough that the dc voltage drop in r_b is negligible, so we neglect r_b .

Consider Fig. 3.45 with dc signals so that $V_{i1} = V_{I1}$, $V_{i2} = V_{I2}$, $V_{o1} = V_{O1}$, and $V_{o2} = V_{O2}$. Let $V_{ID} = V_{I1} - V_{I2}$. Also, assume that the collector resistors may not be identical. Let R_{C1} and R_{C2} represent the values of the resistors attached to Q_1 and Q_2 , respectively. From KVL around the input loop,

$$V_{ID} - V_{BE1} + V_{BE2} = 0 \quad (3.202)$$

Therefore,

$$V_{ID} = V_T \ln \frac{I_{C1}}{I_{S1}} - V_T \ln \frac{I_{C2}}{I_{S2}} = V_T \ln \frac{I_{C1}}{I_{C2}} \frac{I_{S2}}{I_{S1}} \quad (3.203)$$

The factors determining the saturation current I_S of a bipolar transistor are described in Chapter 1. There it was shown that if the impurity concentration in the base region is uniform, these saturation currents can be written

$$I_{S1} = \frac{qn_i^2 \bar{D}_n}{N_A W_{B1}(V_{CB})} A_1 = \frac{qn_i^2 \bar{D}_n}{Q_{B1}(V_{CB})} A_1 \quad (3.204)$$

$$I_{S2} = \frac{qn_i^2 \bar{D}_n}{N_A W_{B2}(V_{CB})} A_2 = \frac{qn_i^2 \bar{D}_n}{Q_{B2}(V_{CB})} A_2 \quad (3.205)$$

where $W_B(V_{CB})$ is the base width as a function of V_{CB} , N_A is the acceptor density in the base, and A is the emitter area. We denote the product $N_A W_B(V_{CB})$ as $Q_B(V_{CB})$, the total base impurity doping per unit area.

The input offset voltage V_{OS} is equal to the value of $V_{ID} = V_{I1} - V_{I2}$ that must be applied to the input to drive the differential output voltage $V_{OD} = V_{O1} - V_{O2}$ to zero. For V_{OD} to be zero, $I_{C1} R_{C1} = I_{C2} R_{C2}$; therefore,

$$\frac{I_{C1}}{I_{C2}} = \frac{R_{C2}}{R_{C1}} \quad (3.206)$$

Substituting (3.204), (3.205), and (3.206) into (3.203) gives

$$V_{OS} = V_T \ln \left[\left(\frac{R_{C2}}{R_{C1}} \right) \left(\frac{A_2}{A_1} \right) \left(\frac{Q_{B1}(V_{CB})}{Q_{B2}(V_{CB})} \right) \right] \quad (3.207)$$

This expression relates the input offset voltage to the device parameters and R_C mismatch. Usually, however, the argument of the log function is very close to unity and the equation can be interpreted in a more intuitively satisfying way. In the following section we perform an approximate analysis, valid if the mismatches are small.

3.5.6.3 Offset Voltage of the Emitter-Coupled Pair: Approximate Analysis

In cases of practical interest involving offset voltages and currents, the mismatch between any two nominally matched circuit parameters is usually small compared with the absolute value of that parameter. This observation leads to a procedure by which the individual contributions to offset voltage can be considered separately and summed.

First, define new parameters to describe the mismatch in the components, using the relations

$$\Delta X = X_1 - X_2 \quad (3.208)$$

$$X = \frac{X_1 + X_2}{2} \quad (3.209)$$

Thus ΔX is the difference between two parameters, and X is the average of the two nominally matched parameters. Note that ΔX can be positive or negative. Next invert (3.208) and (3.209) to give

$$X_1 = X + \frac{\Delta X}{2} \quad (3.210)$$

$$X_2 = X - \frac{\Delta X}{2} \quad (3.211)$$

These relations can be applied to the collector resistances, the emitter areas, and the base doping parameters in (3.207) to give

$$V_{OS} = V_T \ln \left[\left(\frac{R_C - \frac{\Delta R_C}{2}}{R_C + \frac{\Delta R_C}{2}} \right) \left(\frac{A - \frac{\Delta A}{2}}{A + \frac{\Delta A}{2}} \right) \left(\frac{Q_B + \frac{\Delta Q_B}{2}}{Q_B - \frac{\Delta Q_B}{2}} \right) \right] \quad (3.212)$$

With the assumptions that $\Delta R_C \ll R_C$, $\Delta A \ll A$, and $\Delta Q_B \ll Q_B$, (3.212) can be simplified to

$$\begin{aligned} V_{OS} &\simeq V_T \ln \left[\left(1 - \frac{\Delta R_C}{R_C} \right) \left(1 - \frac{\Delta A}{A} \right) \left(1 + \frac{\Delta Q_B}{Q_B} \right) \right] \\ &\simeq V_T \left[\ln \left(1 - \frac{\Delta R_C}{R_C} \right) + \ln \left(1 - \frac{\Delta A}{A} \right) + \ln \left(1 + \frac{\Delta Q_B}{Q_B} \right) \right] \end{aligned} \quad (3.213)$$

If $x \ll 1$, a Taylor series can be used to show that

$$\ln(1+x) = x - \frac{x^2}{2} + \frac{x^3}{3} - \dots \quad (3.214)$$

Applying (3.214) to each logarithm in (3.213) and ignoring terms higher than first order in the expansions gives

$$V_{OS} \simeq V_T \left(-\frac{\Delta R_C}{R_C} - \frac{\Delta A}{A} + \frac{\Delta Q_B}{Q_B} \right) \quad (3.215)$$

Thus, under the assumptions made, we have obtained an approximate expression for the input offset voltage, which is the linear superposition of the effects of the different components. It can be shown that this can always be done for small component mismatches. Note that the signs of the individual terms of (3.215) are not particularly significant, since the mismatch factors can be positive or negative depending on the direction of the random parameter variation. The worst-case offset occurs when the terms have signs such that the individual contributions add.

Equation 3.215 relates the offset voltage to mismatches in the resistors and in the structural parameters A and Q_B of the transistors. For the purpose of predicting the offset voltage from device parameters that are directly measurable electrically, we rewrite (3.215) to express the offset in terms of the resistor mismatch and the mismatch in the saturation currents of the transistors:

$$V_{OS} \simeq V_T \left(-\frac{\Delta R_C}{R_C} - \frac{\Delta I_S}{I_S} \right) \quad (3.216)$$

where

$$\frac{\Delta I_S}{I_S} = \frac{\Delta A}{A} - \frac{\Delta Q_B}{Q_B} \quad (3.217)$$

is the offset voltage contribution from the transistors themselves, as reflected in the mismatch in saturation current. Mismatch factors $\Delta R_C/R_C$ and $\Delta I_S/I_S$ are actually random parameters that take on a different value for each circuit fabricated, and the distribution of the observed values is described by a probability distribution. For large samples the distribution tends toward a normal, or Gaussian, distribution with zero mean. Typically observed standard deviations for the preceding mismatch parameters for small-area diffused devices are

$$\sigma_{\Delta R/R} = 0.01 \quad \sigma_{\Delta I_S/I_S} = 0.05 \quad (3.218)$$

In the Gaussian distribution, 68 percent of the samples have a value within $\pm \sigma$ of the mean value. If we assume that the mean value of the distribution is zero, then 68 percent of the resistor pairs in a large sample will match within 1 percent, and 68 percent of the transistor pairs will have saturation currents that match within 5 percent for the distributions described by (3.218). These values can be heavily influenced by device geometry and processing. If we pick one sample from each distribution so that the parameter mismatch is equal to the corresponding standard deviation, and if the mismatch factors are chosen in the direction so that they add, the resulting offset from (3.216) would be

$$V_{OS} \simeq (26\text{mV})(0.01 + 0.05) \simeq 1.5\text{mV} \quad (3.219)$$

Large ion-implanted devices with careful layout can achieve $V_{OS} \simeq 0.1$ mV. A parameter of more interest to the circuit designer than the offset of one sample is the standard deviation of the total offset voltage. Since the offset is the sum of two uncorrelated random parameters, the standard deviation of the sum is equal to the square root of the sum of the squares of the standard deviation of the two mismatch contributions, or

$$\sigma_{V_{OS}} = V_T \sqrt{(\sigma_{\Delta R/R})^2 + (\sigma_{\Delta I_S/I_S})^2} \quad (3.220)$$

The properties of the Gaussian distribution are summarized in Appendix A.3.1.

3.5.6.4 Offset Voltage Drift in the Emitter-Coupled Pair

When emitter-coupled pairs are used as low-level dc amplifiers where the offset voltage is critical, provision is sometimes made to manually adjust the input offset voltage to zero with an external potentiometer. When this adjustment is done, the important parameter becomes not the offset voltage itself, but the variation of this offset voltage with temperature, often referred to as *drift*. For most practical circuits, the sensitivity of the input offset voltage to temperature is not zero, and the wider the excursion of temperature experienced by the circuit, the more error the offset voltage drift will contribute. This parameter is easily calculated for the emitter-coupled pair by differentiating (3.207) as follows

$$\frac{dV_{OS}}{dT} = \frac{V_{OS}}{T} \quad (3.221)$$

using $V_T = kT/q$ and assuming the ratios in (3.207) are independent of temperature. Thus the drift and offset are proportional for the emitter-coupled pair. This relationship is observed experimentally. For example, an emitter-coupled pair with a measured offset voltage of 2 mV would display a drift of 2mV/300°K or 6.6μV/°C under the assumptions we have made.

Equation 3.221 appears to show that the drift also would be nulled by externally adjusting the offset to zero. This observation is only approximately true because of the way in which the nulling is accomplished.¹³ Usually an external potentiometer is placed in parallel with a portion of one of the collector load resistors in the pair. The temperature coefficient of the nulling potentiometer generally does not match that of the diffused resistors, so a resistor-mismatch temperature coefficient is introduced that can make the drift worse than it was without nulling. Voltage drifts in the 1μV/°C range can be obtained with careful design.

3.5.6.5 Input Offset Current of the Emitter-Coupled Pair

The input offset current I_{OS} is measured with the inputs connected only to current sources and is the difference in the base currents that must be applied to drive the differential output voltage $V_{OD} = V_{O1} - V_{O2}$ to zero. Since the base current of each transistor is equal to the corresponding collector current divided by beta, the offset current is

$$I_{OS} = \frac{I_{C1}}{\beta_{F1}} - \frac{I_{C2}}{\beta_{F2}} \quad (3.222)$$

when $V_{OD} = 0$. As before, we can write

$$I_{C1} = I_C + \frac{\Delta I_C}{2} \quad I_{C2} = I_C - \frac{\Delta I_C}{2} \quad (3.223)$$

$$\beta_{F1} = \beta_F + \frac{\Delta \beta_F}{2} \quad \beta_{F2} = \beta_F - \frac{\Delta \beta_F}{2} \quad (3.224)$$

Inserting (3.223) and (3.224) into (3.222), the offset current becomes

$$I_{OS} = \left(\frac{I_C + \frac{\Delta I_C}{2}}{\beta_F + \frac{\Delta \beta_F}{2}} - \frac{I_C - \frac{\Delta I_C}{2}}{\beta_F - \frac{\Delta \beta_F}{2}} \right) \quad (3.225)$$

Neglecting higher-order terms, this becomes

$$I_{OS} \simeq \frac{I_C}{\beta_F} \left(\frac{\Delta I_C}{I_C} - \frac{\Delta \beta_F}{\beta_F} \right) \quad (3.226)$$

For V_{OD} to be zero, $I_{C1}R_{C1} = I_{C2}R_{C2}$; therefore, from (3.206), the mismatch in collector currents is

$$\frac{\Delta I_C}{I_C} = -\frac{\Delta R_C}{R_C} \quad (3.227)$$

Equation 3.227 shows that the fractional mismatch in the collector currents must be equal in magnitude and opposite in polarity from the fractional mismatch in the collector resistors to force $V_{OD} = 0$. Substituting (3.227) into (3.226) gives

$$I_{OS} \simeq -\frac{I_C}{\beta_F} \left(\frac{\Delta R_C}{R_C} + \frac{\Delta \beta_F}{\beta_F} \right) \quad (3.228)$$

A typically observed beta mismatch distribution displays a deviation of about 10 percent. Assuming a beta mismatch of 10 percent and a mismatch in collector resistors of 1 percent, we obtain

$$I_{OS} \simeq -\frac{I_C}{\beta_F} \left(\frac{\Delta R_C}{R_C} + \frac{\Delta \beta_F}{\beta_F} \right) = -\frac{I_C}{\beta_F}(0.11) = -0.11 (I_B) \quad (3.229)$$

In many applications, the input offset current as well as the input current itself must be minimized. A good example is the input stage of operational amplifiers. Various circuit and technological approaches to reduce these currents are considered in Chapter 6.

3.5.6.6 Input Offset Voltage of the Source-Coupled Pair

As mentioned earlier in the chapter, MOS transistors inherently provide higher input resistance and lower input bias current than bipolar transistors when the MOS gate is used as the input. This observation also applies to differential-pair amplifiers. The input offset current of an MOS differential pair is the difference between the two gate currents and is essentially zero because the gates of the input transistors are connected to silicon dioxide, which is an insulator. However, MOS transistors exhibit lower transconductance than bipolar transistors at the same current, resulting in poorer input offset voltage and common-mode rejection ratio in MOS differential pairs than in the case of bipolar transistors. In this section we calculate the input offset voltage of the source-coupled MOSFET pair.

Consider Fig. 3.50 with dc signals so that $V_{i1} = V_{I1}$, $V_{i2} = V_{I2}$, $V_{o1} = V_{O1}$, and $V_{o2} = V_{O2}$. Let $V_{ID} = V_{I1} - V_{I2}$. Also, assume that the drain resistors may not be identical. Let R_{D1} and R_{D2} represent the values of the resistors attached to M_1 and M_2 , respectively. KVL around the input loop gives

$$V_{ID} - V_{GS1} + V_{GS2} = 0 \quad (3.230)$$

Solving (1.157) for the gate-source voltage and substituting into (3.230) gives

$$\begin{aligned} V_{ID} &= V_{GS1} - V_{GS2} \\ &= V_{t1} + \sqrt{\frac{2I_{D1}}{k'(W/L)_1}} - V_{t2} - \sqrt{\frac{2I_{D2}}{k'(W/L)_2}} \end{aligned} \quad (3.231)$$

As in the bipolar case, the input offset voltage V_{OS} is equal to the value of $V_{ID} = V_{I1} - V_{I2}$ that must be applied to the input to drive the differential output voltage $V_{OD} = V_{O1} - V_{O2}$ to zero. For V_{OD} to be zero, $I_{D1}R_{D1} = I_{D2}R_{D2}$; therefore,

$$V_{OS} = V_{t1} - V_{t2} + \sqrt{\frac{2I_{D1}}{k'(W/L)_1}} - \sqrt{\frac{2I_{D2}}{k'(W/L)_2}} \quad (3.232)$$

subject to the constraint that $I_{D1}R_{D1} = I_{D2}R_{D2}$.

3.5.6.7 Offset Voltage of the Source-Coupled Pair: Approximate Analysis

The mismatch between any two nominally matched circuit parameters is usually small compared with the absolute value of that parameter in practice. As a result, (3.232) can be rewritten in a way that allows us to understand the contributions of each mismatch to the overall offset.

Defining difference and average quantities in the usual way, we have

$$\Delta I_D = I_{D1} - I_{D2} \quad (3.233)$$

$$I_D = \frac{I_{D1} + I_{D2}}{2} \quad (3.234)$$

$$\Delta(W/L) = (W/L)_1 - (W/L)_2 \quad (3.235)$$

$$(W/L) = \frac{(W/L)_1 + (W/L)_2}{2} \quad (3.236)$$

$$\Delta V_t = V_{t1} - V_{t2} \quad (3.237)$$

$$V_t = \frac{V_{t1} + V_{t2}}{2} \quad (3.238)$$

$$\Delta R_L = R_{L1} - R_{L2} \quad (3.239)$$

$$R_L = \frac{R_{L1} + R_{L2}}{2} \quad (3.240)$$

Rearranging (3.233) and (3.234) as well as (3.235) and (3.236) gives

$$I_{D1} = I_D + \frac{\Delta I_D}{2} \quad I_{D2} = I_D - \frac{\Delta I_D}{2} \quad (3.241)$$

$$(W/L)_1 = (W/L) + \frac{\Delta(W/L)}{2} \quad (W/L)_2 = (W/L) - \frac{\Delta(W/L)}{2} \quad (3.242)$$

Substituting (3.237), (3.241), and (3.242) into (3.232) gives

$$V_{OS} = \Delta V_t + \sqrt{\frac{2(I_D + \Delta I_D/2)}{k'[(W/L) + \Delta(W/L)/2]}} - \sqrt{\frac{2(I_D - \Delta I_D/2)}{k'[(W/L) - \Delta(W/L)/2]}} \quad (3.243)$$

Rearranging (3.243) gives

$$V_{OS} = \Delta V_t + (V_{GS} - V_t) \left(\sqrt{\frac{1 + \Delta I_D/2I_D}{1 + \frac{\Delta(W/L)}{2(W/L)}}} - \sqrt{\frac{1 - \Delta I_D/2I_D}{1 - \frac{\Delta(W/L)}{2(W/L)}}} \right) \quad (3.244)$$

If the mismatch terms are small, the argument of each square root in (3.244) is approximately unity. Using $\sqrt{x} \simeq (1 + x)/2$ when $x \simeq 1$ for the argument of each square root in (3.244), we have

$$V_{OS} \simeq \Delta V_t + \frac{(V_{GS} - V_t)}{2} \left(\frac{1 + \Delta I_D/2I_D}{1 + \frac{\Delta(W/L)}{2(W/L)}} - \frac{1 - \Delta I_D/2I_D}{1 - \frac{\Delta(W/L)}{2(W/L)}} \right) \quad (3.245)$$

Carrying out the long divisions in (3.245) and ignoring terms higher than first order gives

$$V_{OS} \simeq \Delta V_t + \frac{(V_{GS} - V_t)}{2} \left(\frac{\Delta I_D}{I_D} - \frac{\Delta(W/L)}{(W/L)} \right) \quad (3.246)$$

When the differential input voltage is V_{OS} , the differential output voltage is zero; therefore, $I_{D1}R_{L1} = I_{D2}R_{L2}$, and

$$\frac{\Delta I_D}{I_D} = -\frac{\Delta R_L}{R_L} \quad (3.247)$$

In other words, the mismatch in the drain currents must be opposite of the mismatch of the load resistors to set $V_{OD} = 0$. Substituting (3.247) into (3.246) gives

$$V_{OS} = \Delta V_t + \frac{(V_{GS} - V_t)}{2} \left(-\frac{\Delta R_L}{R_L} - \frac{\Delta(W/L)}{(W/L)} \right) \quad (3.248)$$

The first term on the right side of (3.248) stems from threshold mismatch. This mismatch component is present in MOS devices but not in bipolar transistors. This component results in a constant offset component that is bias-current independent. Threshold mismatch is a strong function of process cleanliness and uniformity and can be substantially improved by the use of careful layout. Measurements indicate that large-geometry structures are capable of achieving threshold-mismatch distributions with standard deviations on the order of 2 mV in a modern silicon-gate MOS process. This offset component alone limits the minimum offset in the MOS case and is an order of magnitude larger than the total differential-pair offset in modern ion-implanted bipolar technologies.

The second term on the right side of (3.248) shows that another component of the offset scales with the overdrive $V_{ov} = (V_{GS} - V_t)$ and is related to a mismatch in the load elements or in the device W/L ratio. In the bipolar emitter-coupled pair offset, the corresponding mismatch terms were multiplied by V_T , typically a smaller number than $V_{ov}/2$. Thus source-coupled pairs of MOS transistors display higher input offset voltage than bipolar pairs for the same level of geometric mismatch or process gradient even when threshold mismatch is ignored. The key reason for this limitation is that the ratio of the transconductance to the bias current is much lower with MOS transistors than in the bipolar case. The quantities V_T in (3.216) and $(V_{GS} - V_t)/2 = V_{ov}/2$ in (3.248) are both equal to I_{BIAS}/g_m for the devices in question. This quantity is typically in the range 50 mV to 500 mV for MOS transistors instead of 26 mV for bipolar transistors.

3.5.6.8 Offset Voltage Drift in the Source-Coupled Pair

Offset voltage drift in MOSFET source-coupled pairs does not show the high correlation with offset voltage observed in bipolar pairs. The offset consists of several terms that have different temperature coefficients. Both V_t and V_{ov} have a strong temperature dependence, affecting V_{GS} in opposite directions. The temperature dependence of V_{ov} stems primarily from the mobility variation, which gives a negative temperature coefficient to the drain current, while the threshold voltage depends on the Fermi potential. As shown in Section 1.5.4, the

latter decreases with temperature and contributes a positive temperature coefficient to the drain current. The drift due to the ΔV_t term in V_{OS} may be quite large if this term itself is large. These two effects can be made to cancel at one value of I_D , which is a useful phenomenon for temperature-stable biasing of single-ended amplifiers. In differential amplifiers, however, this phenomenon is not greatly useful because differential configurations already give first-order cancellation of V_{GS} temperature variations.

3.5.6.9 Small-Signal Characteristics of Unbalanced Differential Amplifiers¹¹

As mentioned in Section 3.5.4, the common-mode-to-differential-mode gain and differential-mode-to-common-mode gain of unbalanced differential amplifiers are nonzero. The direct approach to calculation of these cross-gain terms requires analysis of the entire small-signal diagram. In perfectly balanced differential amplifiers, the cross-gain terms are zero, and the differential-mode and common-mode gains can be found by using two *independent* half circuits, as shown in Section 3.5.5. With imperfect matching, exact half-circuit analysis is still possible if the half circuits are *coupled* instead of independent. Furthermore, if the mismatches are small, a modified version of half-circuit analysis gives results that are approximately valid. This modified half-circuit analysis not only greatly simplifies the required calculations, but also gives insight about how to reduce A_{cm-dm} and A_{dm-cm} in practice.

First consider a pair of mismatched resistors R_1 and R_2 shown in Fig. 3.63. Assume that the branch currents are i_1 and i_2 , respectively. From Ohm's law, the differential and common-mode voltages across the resistors can be written as

$$v_d = v_1 - v_2 = i_1 R_1 - i_2 R_2 \quad (3.249)$$

and

$$v_c = \frac{v_1 + v_2}{2} = \frac{i_1 R_1 + i_2 R_2}{2} \quad (3.250)$$

Define $i_d = i_1 - i_2$, $i_c = (i_1 + i_2)/2$, $\Delta R = R_1 - R_2$, and $R = (R_1 + R_2)/2$. Then (3.249) and (3.250) can be rewritten as

$$v_d = \left(i_c + \frac{i_d}{2} \right) \left(R + \frac{\Delta R}{2} \right) - \left(i_c - \frac{i_d}{2} \right) \left(R - \frac{\Delta R}{2} \right) = i_d R + i_c (\Delta R) \quad (3.251)$$

and

$$v_c = \frac{\left(i_c + \frac{i_d}{2} \right) \left(R + \frac{\Delta R}{2} \right) + \left(i_c - \frac{i_d}{2} \right) \left(R - \frac{\Delta R}{2} \right)}{2} = i_c R + \frac{i_d (\Delta R)}{4} \quad (3.252)$$

These equations can be used to draw differential and common-mode half circuits for the pair of mismatched resistors. Since the differential half circuit should give half the differential voltage dropped across the resistors, the two terms on the right-hand side of (3.251) are each divided by two and used to represent one component of a branch voltage of $v_d/2$. The differential half circuit is shown in Fig. 3.64a. The first component of the branch voltage is the voltage

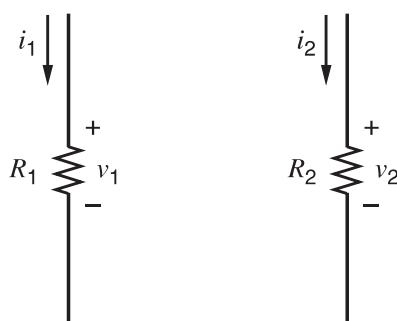


Figure 3.63 A pair of mismatched resistors.

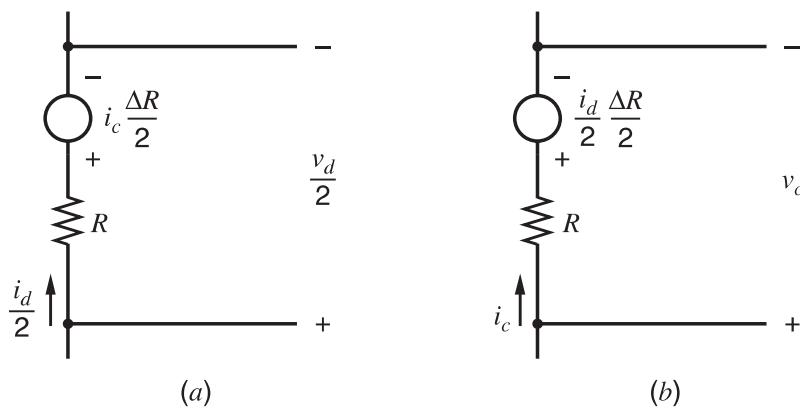


Figure 3.64 (a) Differential and (b) common-mode half circuits for a pair of mismatched resistors.

dropped across R and is half the differential current times the average resistor value. The second component is the voltage across the dependent voltage source controlled by the current flowing in the common-mode half circuit and is proportional to half the mismatch in the resistor values. The common-mode half circuit is constructed from (3.252) and is shown in Fig. 3.64b. Here the total branch voltage v_c is the sum of the voltages across a resistor and a dependent voltage source controlled by the current flowing in the differential half circuit. In the limiting case where $\Delta R = 0$, the voltage across each dependent source in Fig. 3.64 is zero, and each half circuit collapses to simply a resistor of value R . Therefore, the half circuits are independent in this case, as expected. In practice, however, $\Delta R \neq 0$, and Fig. 3.64 shows that the differential voltage depends not only on the differential current, but also on the common-mode current. Similarly, the common-mode voltage depends in part on the differential current. Thus the behavior of a pair of mismatched resistors can be represented exactly by using coupled half circuits.

Next consider a pair of mismatched voltage-controlled current sources as shown in Fig. 3.65. Assume that the control voltages are v_1 and v_2 , respectively. Then the differential and common-mode currents can be written as

$$\begin{aligned} i_d &= i_1 - i_2 = g_{m1}v_1 - g_{m2}v_2 \\ &= \left(g_m + \frac{\Delta g_m}{2} \right) \left(v_c + \frac{v_d}{2} \right) - \left(g_m - \frac{\Delta g_m}{2} \right) \left(v_c - \frac{v_d}{2} \right) \\ &= g_m v_d + \Delta g_m v_c \end{aligned} \quad (3.253)$$

and

$$\begin{aligned} i_c &= \frac{i_1 + i_2}{2} = \frac{g_{m1}v_1 + g_{m2}v_2}{2} \\ &= \frac{\left(g_m + \frac{\Delta g_m}{2} \right) \left(v_c + \frac{v_d}{2} \right) + \left(g_m - \frac{\Delta g_m}{2} \right) \left(v_c - \frac{v_d}{2} \right)}{2} \\ &= g_m v_c + \frac{\Delta g_m v_d}{4} \end{aligned} \quad (3.254)$$

where $v_d = v_1 - v_2$, $v_c = (v_1 + v_2)/2$, $\Delta g_m = g_{m1} - g_{m2}$, and $g_m = (g_{m1} + g_{m2})/2$.

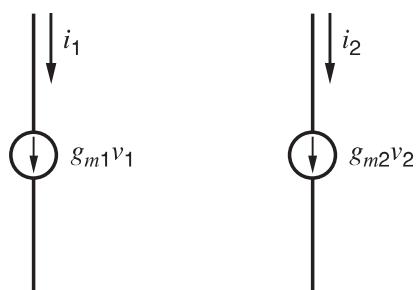


Figure 3.65 A pair of mismatched voltage-controlled current sources.

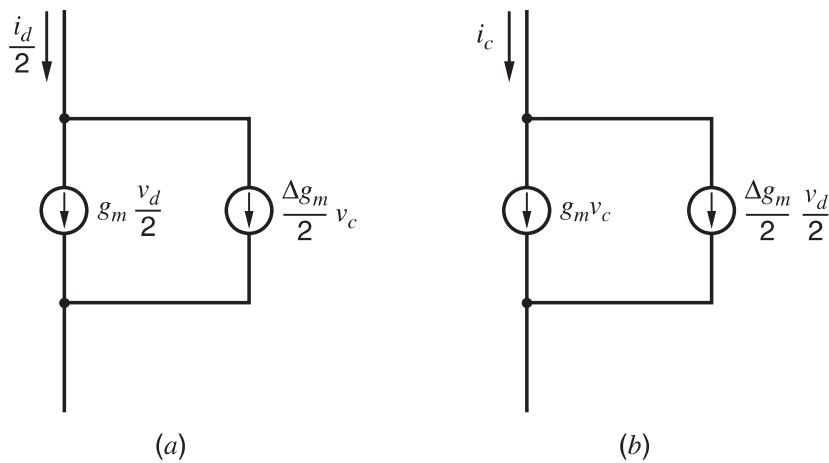


Figure 3.66 (a) Differential and (b) common-mode half circuits for a pair of mismatched voltage-controlled current sources.

The corresponding differential and common-mode half circuits each use two voltage-controlled current sources, as shown in Fig. 3.66. In each case, one dependent source is proportional to the average transconductance and the other to half the mismatch in the transconductances. With perfect matching, the mismatch terms are zero, and the two half circuits are independent. With imperfect matching, however, the mismatch terms are nonzero. In the differential half circuit, the mismatch current source is controlled by the common-mode control voltage. In the common-mode half circuit, the mismatch current source is controlled by half the differential control voltage. Thus, as for mismatched resistors, the behavior of a pair of mismatched voltage-controlled current sources can be represented exactly by using coupled half circuits.

With these concepts in mind, construction of the differential and common-mode half circuits of unbalanced differential amplifiers is straightforward. In the differential half circuit, mismatched resistors are replaced by the circuit shown in Fig. 3.64a, and mismatched voltage-controlled current sources are replaced by the circuit in Fig. 3.66a. Similarly, the circuits shown in Fig. 3.64b and Fig. 3.66b replace mismatched resistors and voltage-controlled current sources in the common-mode half circuit. Although mismatches change the differential and common-mode components of signals that appear at various points in the complete unbalanced amplifier, the differential components are still equal and opposite while the common-mode components are identical by definition. Therefore, small-signal short and open circuits induced by the differential and common-mode signals are unaffected by these replacements.

For example, the differential and common-mode half circuits of the unbalanced differential amplifier shown in Fig. 3.67 are shown in Fig. 3.68. KCL at the output of the differential half

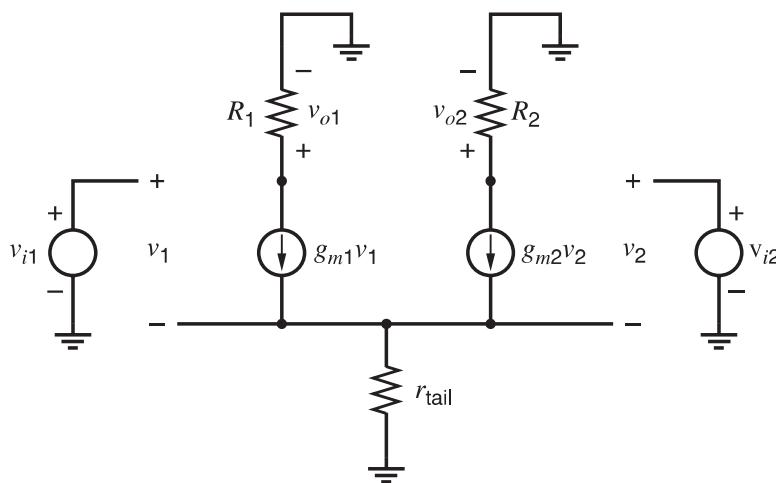


Figure 3.67 The small-signal diagram of an unbalanced differential amplifier.

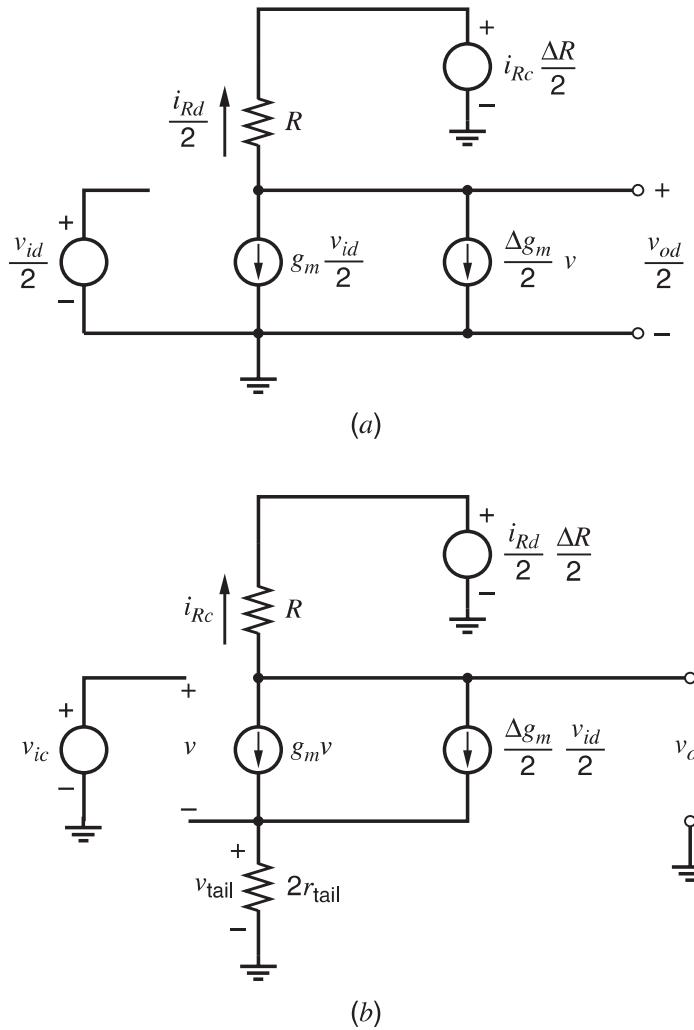


Figure 3.68 (a) Differential and (b) common-mode half circuits of the differential amplifier shown in Fig. 3.67.

circuit in Fig. 3.68a gives

$$\frac{i_{Rd}}{2} + g_m \frac{v_{id}}{2} + \frac{\Delta g_m}{2} v = 0 \quad (3.255)$$

KCL at the output of the common-mode half circuit in Fig. 3.68b gives

$$g_m v + \frac{\Delta g_m}{2} \frac{v_{id}}{2} + i_{Rc} = 0 \quad (3.256)$$

Also, KVL around the input loop in the common-mode half circuit gives

$$v = v_{ic} - v_{tail} = v_{ic} + 2i_{Rc}r_{tail} \quad (3.257)$$

Substituting (3.257) into (3.256) and rearranging gives

$$i_{Rc} = -\frac{g_m v_{ic} + \frac{\Delta g_m}{2} \frac{v_{id}}{2}}{1 + 2g_m r_{tail}} \quad (3.258)$$

Substituting (3.257) and (3.258) into (3.255) and rearranging gives

$$\frac{i_{Rd}}{2} = \frac{v_{id}}{2} \left(-g_m + \frac{\Delta g_m r_{tail}}{1 + 2g_m r_{tail}} \frac{\Delta g_m}{2} \right) + v_{ic} \left(-\frac{\Delta g_m}{2} + \frac{\Delta g_m r_{tail} g_m}{1 + 2g_m r_{tail}} \right) \quad (3.259)$$

From KVL in the R branch in the differential half circuit in Fig. 3.68a,

$$\frac{v_{od}}{2} = i_{Rc} \frac{\Delta R}{2} + \frac{i_{Rd}}{2} R \quad (3.260)$$

Substituting (3.258) and (3.259) into (3.260) and rearranging gives

$$v_{od} = A_{dm} v_{id} + A_{cm-dm} v_{ic} \quad (3.261)$$

where A_{dm} and A_{cm-dm} are

$$A_{dm} = \left. \frac{v_{od}}{v_{id}} \right|_{v_{ic}=0} = -g_m R + \frac{\Delta g_m r_{tail} \frac{\Delta g_m}{2} R - \frac{\Delta g_m}{2} \frac{\Delta R}{2}}{1 + 2g_m r_{tail}} \quad (3.262)$$

$$A_{cm-dm} = \left. \frac{v_{od}}{v_{ic}} \right|_{v_{id}=0} = - \left(\frac{g_m \Delta R + \Delta g_m R}{1 + 2g_m r_{tail}} \right) \quad (3.263)$$

From KVL in the R branch in the common-mode half circuit in Fig. 3.68b,

$$v_{oc} = \frac{i_{Rd}}{2} \frac{\Delta R}{2} + i_{Rc} R \quad (3.264)$$

Substituting (3.258) and (3.259) into (3.264) and rearranging gives

$$v_{oc} = A_{dm-cm} v_{id} + A_{cm} v_{ic} \quad (3.265)$$

where A_{dm-cm} and A_{cm} are

$$A_{dm-cm} = \left. \frac{v_{oc}}{v_{id}} \right|_{v_{ic}=0} = -\frac{1}{4} \left[g_m \Delta R + \frac{\Delta g_m R - g_m \Delta R \left(2g_m r_{tail} \left(\frac{\Delta g_m}{2g_m} \right)^2 \right)}{1 + 2g_m r_{tail}} \right] \quad (3.266)$$

$$A_{cm} = \left. \frac{v_{oc}}{v_{ic}} \right|_{v_{id}=0} = - \left(\frac{g_m R + \frac{\Delta g_m}{2} \frac{\Delta R}{2}}{1 + 2g_m r_{tail}} \right) \quad (3.267)$$

The calculations in (3.255) through (3.267) are based on the half circuits in Fig. 3.68 and give *exactly* the same results as an analysis of the entire differential amplifier shown in Fig. 3.67. Because the half circuits are coupled, however, exact half-circuit analysis requires the simultaneous consideration of both half circuits, which is about as complicated as the direct analysis of the entire original circuit.

In practice, the mismatch terms are usually a small fraction of the corresponding average values. As a result, the dominant contributions to the differential signals that control the mismatch generators in the common-mode half circuit stem from differential inputs. Similarly, the dominant part of the common-mode signals that control the mismatch generators in the differential half circuit arise from common-mode inputs. Therefore, we will assume that the signals controlling the mismatch generators can be found approximately by analyzing each half circuit independently without mismatch. The signals that control the mismatch generators in Fig. 3.68 are i_{Rc} , $i_{Rd}/2$, v , and $v_{id}/2$. We will find approximations to these quantities, \hat{i}_{Rc} , $\hat{i}_{Rd}/2$, \hat{v} , and $\hat{v}_{id}/2$ using the half circuits shown in Fig. 3.69, where the inputs are the same as in Fig. 3.68 but where the mismatch terms are set equal to zero. By ignoring the second-order

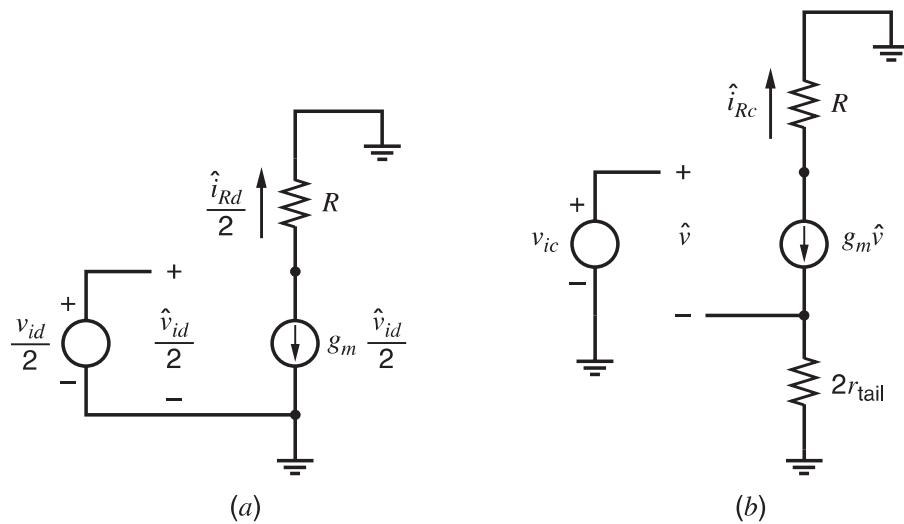


Figure 3.69 (a) Differential and (b) common-mode half circuits of the differential amplifier shown in Fig. 3.67 with mismatch terms set equal to zero.

interactions in which the mismatch generators influence the values of the control signals, this process greatly simplifies the required calculations, as shown next.

From inspection of the differential half circuit in Fig. 3.69a,

$$\frac{\hat{v}_{id}}{2} = \frac{v_{id}}{2} \quad (3.268)$$

and

$$\frac{\hat{i}_{Rd}}{2} = -g_m \frac{v_{id}}{2} \quad (3.269)$$

From the common-mode half circuit in Fig. 3.69b,

$$\hat{v} = v_{ic} - g_m \hat{v} (2r_{tail}) = \frac{v_{ic}}{1 + 2g_m r_{tail}} \quad (3.270)$$

Therefore,

$$\hat{i}_{Rc} = -\frac{g_m v_{ic}}{1 + 2g_m r_{tail}} \quad (3.271)$$

Now reconsider the differential half circuit with mismatch shown in Fig. 3.68a. Assume that $i_{Rc} \simeq \hat{i}_{Rc}$ and $v \simeq \hat{v}$. Then

$$\frac{v_{od}}{2} \simeq -\frac{\Delta R}{2} \left(\frac{g_m v_{ic}}{1 + 2g_m r_{tail}} \right) - g_m \frac{v_{id}}{2} R - \frac{\Delta g_m}{2} \frac{v_{ic}}{1 + 2g_m r_{tail}} R \quad (3.272)$$

From (3.272),

$$A_{dm} = \left. \frac{v_{od}}{v_{id}} \right|_{v_{ic}=0} \simeq -g_m R \quad (3.273)$$

and

$$A_{cm-dm} = \left. \frac{v_{od}}{v_{ic}} \right|_{v_{id}=0} \simeq - \left(\frac{g_m \Delta R + \Delta g_m R}{1 + 2g_m r_{tail}} \right) \quad (3.274)$$

Equation 3.274 shows that the ratio A_{dm}/A_{cm-dm} is approximately proportional to $1 + 2g_m r_{tail}$. Also, (3.274) agrees exactly with (3.263) in this case because the g_m generator in Fig. 3.68a is controlled by a purely differential signal. In other examples, the common-mode-to-differential-mode gain calculated in this way will be only approximately correct.

Now reconsider the common-mode half circuit with mismatch shown in Fig. 3.68b and assume that $i_{Rd} \simeq \hat{i}_{Rd}$. From KCL at the tail node,

$$v_{\text{tail}} \simeq \left(g_m v + \frac{\Delta g_m}{2} \frac{v_{id}}{2} \right) 2r_{\text{tail}} \quad (3.275)$$

Then

$$v = v_{ic} - v_{\text{tail}} \simeq \frac{v_{ic} - \frac{\Delta g_m}{2} \frac{v_{id}}{2} (2r_{\text{tail}})}{1 + 2g_m r_{\text{tail}}} \quad (3.276)$$

From KCL at the output node in Fig. 3.68b,

$$\frac{v_{oc} - \frac{i_{Rd}}{2} \frac{\Delta R}{2}}{R} + g_m v + \frac{\Delta g_m}{2} \frac{v_{id}}{2} = 0 \quad (3.277)$$

Assume that $i_{Rd} \simeq \hat{i}_{Rd}$. Substituting (3.269) and (3.276) into (3.277) and rearranging gives

$$v_{oc} \simeq -\frac{1}{4} \left(g_m \Delta R + \frac{\Delta g_m R}{1 + 2g_m r_{\text{tail}}} \right) v_{id} - \frac{g_m R}{1 + 2g_m r_{\text{tail}}} v_{ic} \quad (3.278)$$

From (3.278),

$$A_{dm-cm} = \frac{v_{oc}}{v_{id}} \Big|_{v_{ic}=0} \simeq -\frac{1}{4} \left(g_m \Delta R + \frac{\Delta g_m R}{1 + 2g_m r_{\text{tail}}} \right) \quad (3.279)$$

and

$$A_{cm} = \frac{v_{oc}}{v_{ic}} \Big|_{v_{id}=0} \simeq -\frac{g_m R}{1 + 2g_m r_{\text{tail}}} \quad (3.280)$$

These equations show that increasing the degeneration to common-mode inputs represented by the quantity $1 + 2g_m r_{\text{tail}}$ reduces the magnitude of A_{cm-dm} , A_{dm-cm} , and A_{cm} . As $r_{\text{tail}} \rightarrow \infty$ in this case, $A_{cm-dm} \rightarrow 0$ and $A_{cm} \rightarrow 0$. On the other hand, A_{dm-cm} does not approach zero when r_{tail} becomes infinite. Instead,

$$\lim_{r_{\text{tail}} \rightarrow \infty} A_{dm-cm} \simeq -\frac{g_m \Delta R}{4} \quad (3.281)$$

With finite and mismatched transistor output resistances, A_{cm-dm} also approaches a nonzero value as r_{tail} becomes infinite. Therefore, r_{tail} should be viewed as an important parameter because it reduces the sensitivity of differential pairs to common-mode inputs and helps reduce the effects of mismatch. However, even an ideal tail current source does not overcome all the problems introduced by mismatch. In Chapter 4, we will consider transistor current sources for which r_{tail} can be quite large.

■ EXAMPLE

Consider the unbalanced differential amplifier in Fig. 3.67. Assume that

$$g_{m1} = 1.001 \text{ mA/V} \quad g_{m2} = 0.999 \text{ mA/V}$$

$$R_1 = 101 \text{ k}\Omega \quad R_2 = 99 \text{ k}\Omega \quad r_{\text{tail}} = 1 \text{ M}\Omega$$

Find A_{dm} , A_{cm} , A_{cm-dm} , and A_{dm-cm} .

Calculating average and mismatch quantities gives

$$g_m = \frac{g_{m1} + g_{m2}}{2} = 1 \frac{\text{mA}}{\text{V}} \quad \Delta g_m = g_{m1} - g_{m2} = 0.002 \frac{\text{mA}}{\text{V}}$$

$$R = \frac{R_1 + R_2}{2} = 100\text{k}\Omega \quad \Delta R = R_1 - R_2 = 2\text{k}\Omega$$

From (3.269)

$$\frac{\hat{i}_{Rd}}{2} = -1 \frac{\text{mA}}{\text{V}} \frac{v_{id}}{2} = -\frac{v_{id}}{2\text{k}\Omega}$$

From (3.271)

$$\hat{i}_{Rc} = -\frac{1 \frac{\text{mA}}{\text{V}} v_{ic}}{1 + 2(1)(1000)} = -\frac{v_{ic}}{2001\text{k}\Omega}$$

From (3.273), (3.274), (3.279), and (3.280),

$$A_{dm} \simeq -1(100) = -100$$

$$A_{cm-dm} \simeq -\frac{1(2) + 0.002(100)}{1 + 2(1)(1000)} \simeq -0.0011$$

$$A_{dm-cm} \simeq -\frac{1}{4} \left(1(2) + \frac{0.002(100)}{1 + 2(1)(1000)} \right) \simeq -0.5$$

$$A_{cm} \simeq -\frac{1(100)}{1 + 2(1)(1000)} \simeq -0.05$$

■

APPENDIX

A.3.1 ELEMENTARY STATISTICS AND THE GAUSSIAN DISTRIBUTION

From the standpoint of a circuit designer, many circuit parameters are best regarded as random variables whose behavior is described by a probability distribution. This view is particularly important in the case of a parameter such as offset voltage. Even though the offset may be zero with perfectly matched components, random variations in resistors and transistors cause a spread of offset voltage around the mean value, and the size of this spread determines the fraction of circuits that meet a given offset specification.

Several factors cause the parameters of an integrated circuit to show random variations. One of these factors is the randomness of the edge definition when regions are defined to form resistors and active devices. In addition, random variations across the wafer in the diffusion of impurities can be a significant factor. These processes usually give rise to a *Gaussian* distribution (sometimes called a *normal* distribution) of the parameters. A Gaussian distribution of a parameter x is specified by a probability density function $p(x)$ given by

$$p(x) = \frac{1}{\sqrt{2\pi}\sigma} \exp \left[-\frac{(x-m)^2}{2\sigma^2} \right] \quad (3.282)$$

where σ is the standard deviation of the distribution and m is the mean or average value of x . The significance of this function is that, for one particular circuit chosen at random from a large collection of circuits, the probability of the parameter having values between x and $(x + dx)$ is given by $p(x)dx$, which is the *area under the curve* $p(x)$ in the range x to $(x + dx)$. For

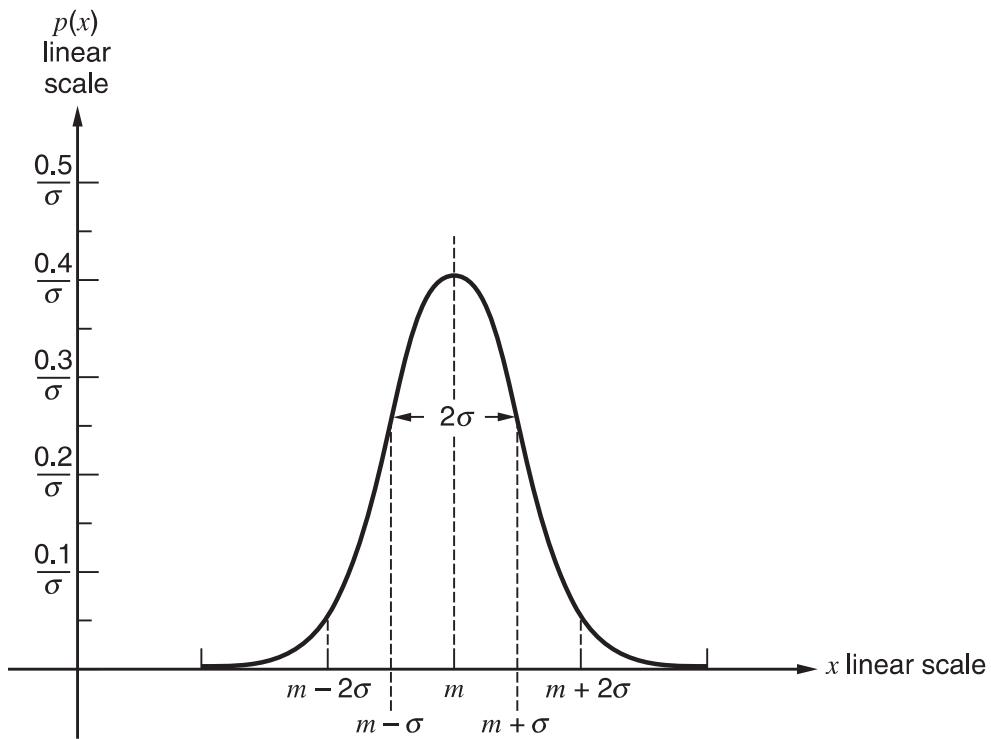


Figure 3.70 Probability density function $p(x)$ for a Gaussian distribution with mean value m and standard deviation σ . $p(x) = \exp[-(x - m)^2/(2\sigma^2)]/(\sqrt{2\pi}\sigma)$.

example, the probability that x has a value less than X is obtained by integrating (3.282) to give

$$P(x < X) = \int_{-\infty}^X p(x) dx \quad (3.283)$$

$$= \int_{-\infty}^X \frac{1}{\sqrt{2\pi}\sigma} \exp\left[-\frac{(x - m)^2}{2\sigma^2}\right] dx \quad (3.284)$$

In a large sample, the *fraction of circuits* where x is less than X will be given by the probability $P(x < X)$, and thus this quantity has real practical significance. The probability density function $p(x)$ in (3.282) is sketched in Fig. 3.70 and shows a characteristic bell shape. The peak value of the distribution occurs when $x = m$, where m is the mean value of x . The standard deviation σ is a measure of the *spread* of the distribution, and large values of σ give rise to a broad distribution. The distribution extends over $-\infty < x < \infty$, as shown by (3.282), but most of the area under the curve is found in the range $x = m \pm 3\sigma$, as will be seen in the following analysis.

The development thus far has shown that the probability of the parameter x having values in a certain range is just equal to the area under the curve of Fig. 3.70 in that range. Since x must lie somewhere in the range $\pm \infty$, the total area under the curve must be unity, and integration of (3.282) will show that this is so. The most common specification of interest to circuit designers is the fraction of a large sample of circuits that lies inside a band around the mean. For example, if a circuit has a gain x that has a Gaussian distribution with mean value 100, what fraction of circuits have gain values in the range 90 to 110? This fraction can be found by evaluating the probability that x takes on values in the range $x = m \pm 10$ where $m = 100$. This probability could be found from (3.282) if σ is known by integrating as follows:

$$P(m - 10 < x < m + 10) = \int_{m-10}^{m+10} \frac{1}{\sqrt{2\pi}\sigma} \exp\left[-\frac{(x - m)^2}{2\sigma^2}\right] dx \quad (3.285)$$

This equation gives the area under the Gaussian curve in the range $x = m \pm 10$.

<i>k</i>	Area under the Gaussian curve in the range $m \pm k\sigma$
0.2	0.159
0.4	0.311
0.6	0.451
0.8	0.576
1.0	0.683
1.2	0.766
1.4	0.838
1.6	0.890
1.8	0.928
2.0	0.954
2.2	0.972
2.4	0.984
2.6	0.991
2.8	0.995
3.0	0.997

Figure 3.71 Values of the integral in (3.286) for various values of k . This integral gives the area under the Gaussian curve of Fig. 3.70 in the range $x = \pm k\sigma$.

To simplify calculations of the kind described above, values of the integral in (3.285) have been calculated and tabulated. To make the tables general, the range of integration is normalized to σ to give

$$P(m - k\sigma < x < m + k\sigma) = \int_{m-k\sigma}^{m+k\sigma} \frac{1}{\sqrt{2\pi}\sigma} \exp\left[-\frac{(x-m)^2}{2\sigma^2}\right] dx \quad (3.286)$$

Values of this integral for various values of k are tabulated in Fig. 3.71. This table shows that $P = 0.683$ for $k = 1$ and thus 68.3 percent of a large sample of a Gaussian distribution lies within a range $x = m \pm \sigma$. For $k = 3$, the value of $P = 0.997$ and thus 99.7 percent of a large sample lies within a range $x = m \pm 3\sigma$.

Circuit parameters such as offset or gain often can be expressed as a linear combination of other parameters as shown in (3.216) and (3.248) for offset voltage. If all the parameters are independent random variables with Gaussian distributions, the standard deviations and means can be related as follows. Assume that the random variable x can be expressed in terms of random variables a , b , and c using

$$x = a + b - c \quad (3.287)$$

Then it can be shown that

$$m_x = m_a + m_b - m_c \quad (3.288)$$

$$\sigma_x^2 = \sigma_a^2 + \sigma_b^2 + \sigma_c^2 \quad (3.289)$$

where m_x is the mean value of x and σ_x is the standard deviation of x . Equation 3.289 shows that the square of the standard deviation of x is the sum of the square of the standard deviations of a , b , and c . This result extends to any number of variables.

These results were treated in the context of the random variations found in circuit parameters. The Gaussian distribution is also useful in the treatment of random noise, as described in Chapter 11.

■ EXAMPLE

The offset voltage of a circuit has a mean value of $m = 0$ and a standard deviation of $\sigma = 2$ mV. What fraction of circuits will have offsets with magnitudes less than 4 mV?

- A range of offset of ± 4 mV corresponds to $\pm 2\sigma$. From Fig. 3.71, we find that the area under the Gaussian curve in this range is 0.954, and thus 95.4 percent of circuits will have offsets with magnitudes less than 4 mV.

PROBLEMS

For the *npn* bipolar transistors in these problems, use the high-voltage bipolar device parameters given in Fig. 2.30, unless otherwise specified.

3.1 Determine the input resistance, transconductance, and output resistance of the CE amplifier of Fig. 3.7 if $R_C = 20\text{ k}\Omega$ and $I_C = 250\text{ }\mu\text{A}$. Assume that $r_b = 0$.

3.2 A CE transistor is to be used in the amplifier of Fig. 3.72 with a source resistance R_S and collector resistor R_C . First, find the overall small-signal gain v_o/v_i as a function of R_S , R_C , β_0 , V_A , and the collector current I_C . Next, determine the value of dc collector bias current I_C that maximizes the small-signal voltage gain. Explain qualitatively why the gain falls at very high and very low collector currents. Do not neglect r_o in this problem. What is the voltage gain at the optimum I_C ? Assume that $r_b = 0$.

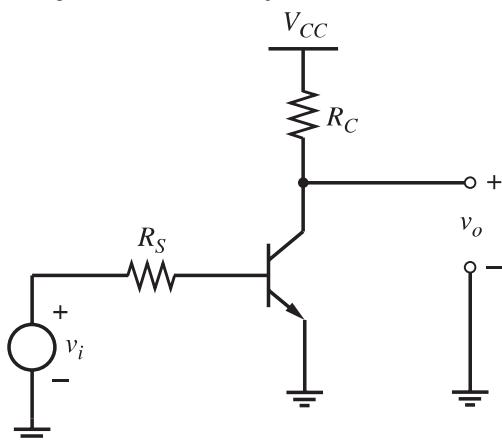


Figure 3.72 Circuit for Problem 3.2.

3.3 Assume that $R_S = R_C = 50\text{k}\Omega$ in Problem 3.2, and calculate the optimum I_C . What is the dc voltage drop across R_C ? What is the voltage gain?

3.4 For the common-source amplifier of Fig. 3.12, calculate the small-signal voltage gain and the bias values of V_i and V_o at the edge of the triode region. Also calculate the bias values of V_i and V_o where the small-signal voltage gain is unity with the transistor operating in the active region. What is the maximum voltage gain of this stage? Assume $V_{DD} = 3\text{V}$, $R_D = 5\text{k}\Omega$, $\mu_n C_{ox} = 200\text{ }\mu\text{A/V}^2$, $W = 10\text{ }\mu\text{m}$, $L = 1\text{ }\mu\text{m}$, $V_t = 0.6\text{ V}$, and $\lambda = 0$. Check your answer with SPICE.

3.5 Determine the input resistance, transconductance, and output resistance of the CB amplifier of Fig. 3.15 if $I_C = 250\text{ }\mu\text{A}$ and $R_C = 10\text{ k}\Omega$. Neglect r_b and r_o .

3.6 Assume that R_C is made large compared with r_o in the CB amplifier of Fig. 3.15. Use the equivalent circuit of Fig. 3.17 and add r_o between the input (emitter terminal) and the output (collector terminal) to calculate the output resistance when

(a) The amplifier is driven by an ideal current source.

(b) The amplifier is driven by an ideal voltage source. Neglect r_b .

3.7 Determine the input resistance of the CG amplifier of Fig. 3.19 if the transistor operates in the active region with $I_D = 100\text{ }\mu\text{A}$. Let $R_D = 10\text{ k}\Omega$, $\mu_n C_{ox} = 200\text{ }\mu\text{A/V}^2$, $\lambda = 0.01\text{ V}^{-1}$, $W = 100\text{ }\mu\text{m}$, and $L = 1\text{ }\mu\text{m}$. Ignore the body effect. Repeat with $R_D = 1\text{ M}\Omega$. If the $100\text{ }\mu\text{A}$ current flows through R_D in this case, a power-supply voltage of at least 100 V would be required. To overcome this problem, assume that an ideal $100\text{-}\mu\text{A}$ current source is placed in parallel with R_D here.

3.8 Determine the input resistance, voltage gain v_o/v_s , and output resistance of the CC amplifier of Fig. 3.23a if $R_S = 5\text{k}\Omega$, $R_L = 500\Omega$, and $I_C = 1\text{mA}$. Neglect r_b and r_o . Do not include R_S in calculating the input resistance. In calculating the output resistance, however, include R_L . Include both R_S and R_L in the gain calculation.

3.9 For the common-drain amplifier of Fig. 3.73, assume $W/L = 10$ and $\lambda = 0$. Use Table 2.2 for other parameters. Find the dc output voltage V_O and the small-signal gain v_o/v_i under the following conditions:

(a) Ignoring the body effect and with $R \rightarrow \infty$.

(b) Including the body effect and with $R \rightarrow \infty$.

(c) Including the body effect and with $R = 100\text{k}\Omega$.

(d) Including the body effect and with $R = 10\text{k}\Omega$.

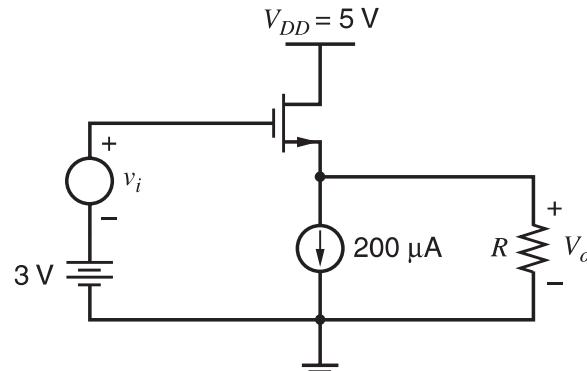


Figure 3.73 Circuit for Problem 3.9.

3.10 Determine the dc collector currents in Q_1 and Q_2 , and then the input resistance and voltage gain for the Darlington emitter follower of Fig. 3.74. Neglect r_μ , r_b , and r_o . Assume that $V_{BE(on)} = 0.7$ V. Check your answer with SPICE and also use SPICE to determine the output resistance of the stage.

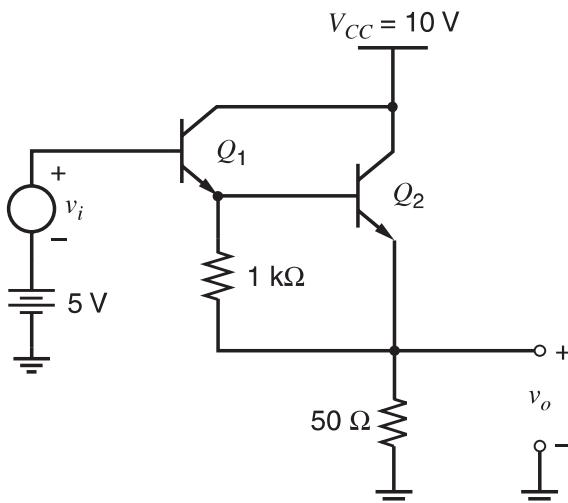


Figure 3.74 Circuit for Problem 3.10.

3.11 Calculate the output resistance r_o^c of the common-emitter Darlington transistor of Fig. 3.75 as a function of I_{BIAS} . Do not neglect either r_{o1} or r_{o2} in this calculation, but you may neglect r_b and r_μ . If $I_{C2} = 1\text{mA}$, what is r_o^c for $I_{BIAS} = 1\text{mA}$? For $I_{BIAS} = 0$?

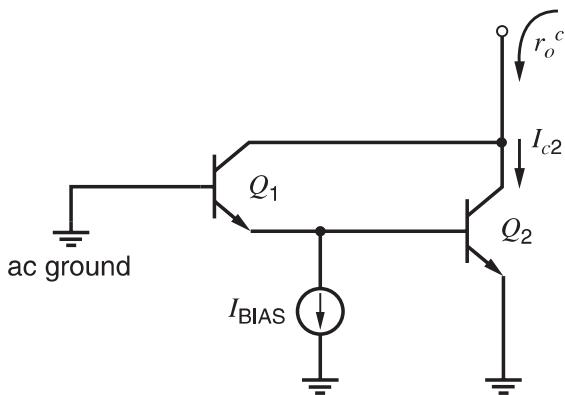


Figure 3.75 Circuit for Problem 3.11.

3.12 A BiCMOS Darlington is shown in Fig. 3.76. The bias voltage V_B is adjusted for a dc output voltage of 2 V. Calculate the bias currents in both devices and then calculate the small-signal voltage gain v_o/v_i of the circuit. For the MOS transistor, assume $W = 10\text{ }\mu\text{m}$, $L = 1\text{ }\mu\text{m}$, $\mu_n C_{ox} = 200\text{ }\mu\text{A/V}^2$, $V_t = 0.6\text{ V}$, $\gamma = 0.25\text{ V}^{1/2}$, $\phi_f = 0.3\text{ V}$, and $\lambda = 0$. For the bipolar transistor, assume $I_S = 10^{-16}\text{ A}$, $\beta_F = 100$, $r_b = 0$, and $V_A \rightarrow \infty$. Use SPICE to check your result. Then add $\lambda = 0.05\text{ V}^{-1}$, $r_b = 100\Omega$, and $V_A = 20\text{ V}$ and compare the original result to the result with this new transistor data. Finally, use SPICE to compute the dc transfer characteristic of the circuit.

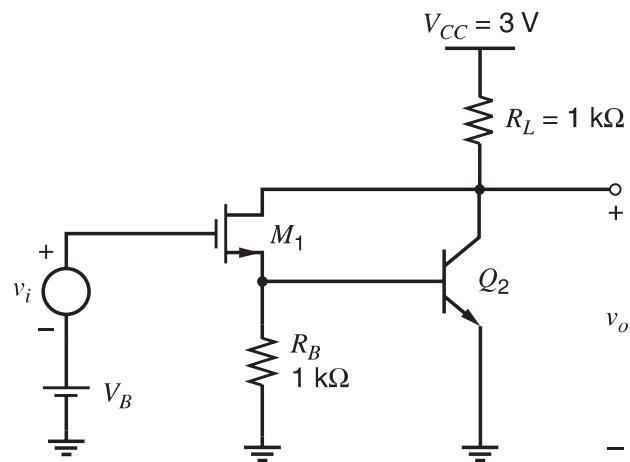


Figure 3.76 BiCMOS Darlington circuit for Problem 3.12.

3.13 Determine the input resistance, transconductance, output resistance, and maximum open-circuit voltage gain for the CE-CB circuit of Fig. 3.36 if $I_{C1} = I_{C2} = 250\text{ }\mu\text{A}$.

3.14 Determine the input resistance, transconductance, output resistance, and maximum open-circuit voltage gain for the CS-CG circuit of Fig. 3.38 if $I_{D1} = I_{D2} = 250\text{ }\mu\text{A}$. Assume $W/L = 100$, $\lambda = 0.1\text{ V}^{-1}$, and $\chi = 0.1$. Use Table 2.2 for other parameters.

3.15 Find the output resistance for the active-cascode circuit of Fig. 3.77 excluding resistor R . Assume that all the transistors operate in the active region with dc drain currents of $100\text{ }\mu\text{A}$. Use the transistor parameters in Table 2.4. Ignore the body effect. Assume $W = 10\text{ }\mu\text{m}$, $L_{drwn} = 0.4\text{ }\mu\text{m}$, and $X_d = 0.1\text{ }\mu\text{m}$ for all transistors. Check your answer with SPICE.

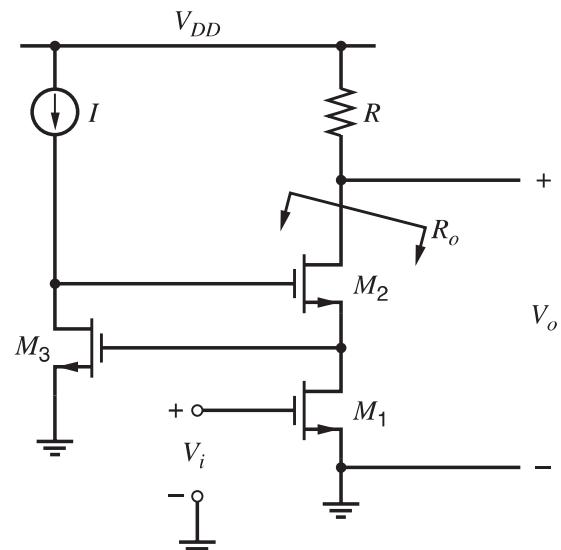


Figure 3.77 Active-cascode circuit for Problem 3.15.

3.16 Find the short-circuit transconductance of the super-source follower shown in Fig. 3.43. Assume $I_1 = 200\text{ }\mu\text{A}$, $I_2 = 100\text{ }\mu\text{A}$, $W_1 = 30\text{ }\mu\text{m}$, and $W_2 = 10\text{ }\mu\text{m}$. Also, assume that both transistors

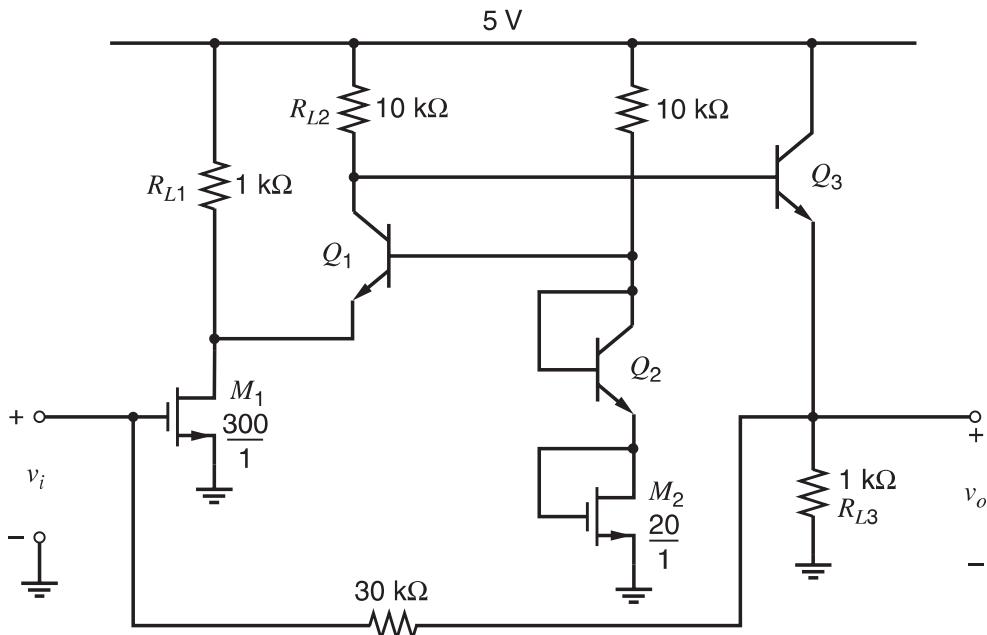


Figure 3.78 BiCMOS amplifier for Problem 3.17.

operate in the active region, and ignore the body effect. Use the transistor parameters in Table 2.4. Assume $L_{\text{drwn}} = 0.4 \mu\text{m}$ and $X_d = 0.1 \mu\text{m}$ for all transistors.

3.17 A BiCMOS amplifier is shown in Fig. 3.78. Calculate the small-signal voltage gain v_o/v_i . Assume $I_S = 10^{-16}\text{A}$, $\beta_F = 100$, $r_b = 0$, $V_A \rightarrow \infty$, $\mu_n C_{ox} = 200 \mu\text{A/V}^2$, $V_t = 0.6 \text{ V}$, and $\lambda = 0$. Check your answer with SPICE and then use SPICE to investigate the effects of velocity saturation by including source degeneration in the MOS transistors as shown in Fig. 1.41 using $\mathcal{E}_c = 1.5 \times 10^6 \text{ V/m}$.

3.18 Determine the differential-mode gain, common-mode gain, differential-mode input resistance, and common-mode input resistance for the circuit of Fig. 3.45 with $I_{\text{TAIL}} = 20 \mu\text{A}$, $R_{\text{TAIL}} = 10 \text{ M}\Omega$, $R_C = 100 \text{ k}\Omega$, and $V_{EE} = V_{CC} = 5 \text{ V}$. Neglect r_b , r_o , and r_μ . Calculate the CMRR. Check with SPICE and use SPICE to investigate the effects of adding nonzero r_b and finite V_A as given in Fig. 2.30.

3.19 Repeat Problem 3.18, but with the addition of emitter-degeneration resistors of value $4 \text{ k}\Omega$ each.

3.20 Determine the overall input resistance, voltage gain, and output resistance of the CC-CB connection of Fig. 3.79. Neglect r_o , r_μ , and r_b . Note that the addition of a $10\text{-k}\Omega$ resistor in the collector of Q_1 would not change the results, so that the results of the emitter-coupled pair analysis can be used.

3.21 Use half-circuit concepts to determine the differential-mode and common-mode gain of the circuit shown in Fig. 3.80. Neglect r_o , r_μ , and r_b . Calculate the differential-mode and common-mode input resistance.

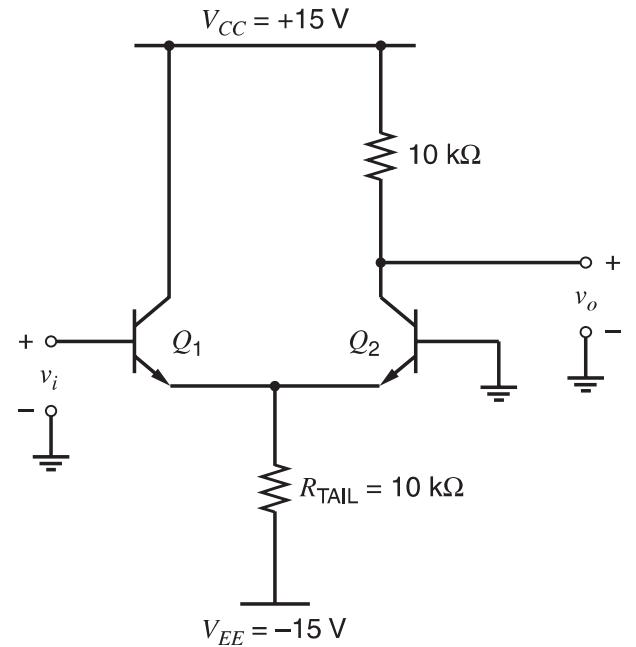


Figure 3.79 Circuit for Problem 3.20.

3.22 Consider the circuit of Fig. 3.80 except replace both *npn* transistors with *n*-channel MOS transistors. Neglect the body effect, and assume $\lambda = 0$. Use half-circuit concepts to determine the differential-mode and common-mode gain of this modified circuit.

3.23 Design an emitter-coupled pair of the type shown in Fig. 3.53a. Assume $I_{\text{TAIL}} = 0$ and select values of R_C and R_{TAIL} to give a differential input resistance of $2\text{M}\Omega$, a differential voltage gain of 500, and a CMRR of 500. What are the minimum values of V_{CC} and V_{EE} that will yield this performance while keeping the transistors biased in the forward-active region under zero-signal conditions? Assume that the dc common-mode input voltage is zero. Neglect r_b , r_μ , and r_o .

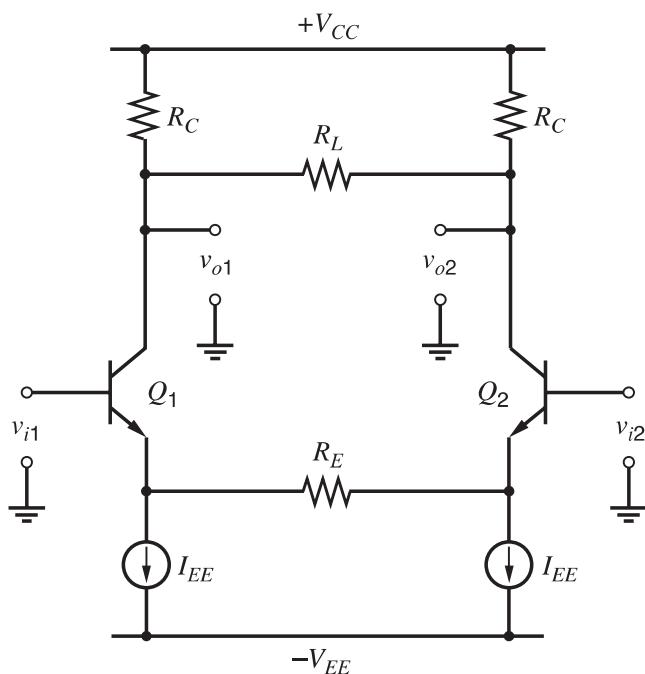


Figure 3.80 Circuit for Problem 3.21.

3.24 Determine the required bias current and device sizes to design a source-coupled pair to have the following two characteristics. First, the small-signal transconductance with zero differential input voltage should be 1.0 mA/V . Second, a differential input voltage of 0.2 V should result in a differential output current of 85 percent of the maximum value. Assume that the devices are n -channel transistors that are made

with the technology summarized in Table 2.4. Use a drawn device channel length of $1 \mu\text{m}$. Neglect channel-length modulation, and assume $X_d = 0$.

3.25 For the circuit of Fig. 3.45, determine the input offset voltage if the transistor base widths mismatch by 10 percent but otherwise the circuit is balanced. Let $R_{\text{TAIL}} \rightarrow \infty$.

3.26 Determine the input offset voltage of the source-coupled pair in Fig. 3.50 for which $I_{\text{TAIL}} = 50 \mu\text{A}$. The drawn device dimensions are $W = 10 \mu\text{m}$ and $L = 1 \mu\text{m}$. Use the process parameters given in Table 2.4. Assume that the worst-case W/L mismatch is 2 percent and the device thresholds are identical. Also assume that $X_d = 0$, $R_{\text{TAIL}} \rightarrow \infty$ and the load resistors are identical.

3.27 Use half-circuit analysis to determine A_{dm} , A_{cm} , A_{cm-dm} , and A_{dm-cm} for a resistively loaded differential pair with mismatched resistive loads, R_1 and R_2 . Assume that $R_1 = 10.1 \text{ k}\Omega$ and $R_2 = 9.9 \text{ k}\Omega$. Also assume that $g_{m1} = g_{m2} = 1 \text{ mA/V}$, $r_{o1} \rightarrow \infty$, and $r_{o2} \rightarrow \infty$. Finally, assume that the equivalent resistance of the tail current source $r_{\text{tail}} = 1 \text{ M}\Omega$.

3.28 Repeat Problem 3.27 but with matched loads and mismatched transistor output resistances. Assume $R_1 = R_2 = 10 \text{ k}\Omega$, $r_{o1} = 505 \text{ k}\Omega$, and $r_{o2} = 495 \text{ k}\Omega$. What happens when $r_{\text{tail}} \rightarrow \infty$?

BIBLIOGRAPHY

1. R. J. Widlar. "Some Circuit Design Techniques for Linear Integrated Circuits," *IEEE Transactions on Circuit Theory*, Vol. CT-12, pp. 586–590, December 1965.
2. H. R. Camenzind and A. B. Grebene. "An Outline of Design Techniques for Linear Integrated Circuits," *IEEE Journal of Solid-State Circuits*, Vol. SC-4, pp. 110–122, June 1969.
3. J. Giles. *Fairchild Semiconductor Linear Integrated Circuits Applications Handbook*. Fairchild Semiconductor, 1967.
4. C. L. Searle, A. R. Boothroyd, E. J. Angelo, P. E. Gray, and D. O. Pederson. *Elementary Circuit Properties of Transistors*. Chapter 7, Wiley, New York, 1964.
5. S. Darlington. "Semiconductor Signal Translating Device," U.S. Patent 2,663,806, May 1952.
6. F. V. Hunt and R. W. Hickman. "On Electronic Voltage Stabilizers," *Review of Scientific Instruments*, Vol. 10, pp. 6–21, January 1939.
7. H. Wallman, A. B. Macnee, and C. P. Gadsden. "A Low-Noise Amplifier," *Proceedings of the I.R.E.*, Vol. 36, pp. 700–708, June 1948.
8. B. J. Hosticka. "Improvement of the Gain of MOS Amplifiers," *IEEE Journal of Solid-State Circuits*, Vol. SC-14, pp. 1111–1114, December 1979.
9. E. Säckinger and W. Guggenbühl. "A High-Swing, High-Impedance MOS Cascode Circuit," *IEEE Journal of Solid-State Circuits*, Vol. 25, pp. 289–298, February 1990.
10. A. D. Blumlein. "Improvements in or Relating to Thermionic Valve Amplifying Circuit Arrangements," British Patent 482,740, July, 1936.
11. R. D. Middlebrook. *Differential Amplifiers*. Wiley, New York, 1963.
12. L. J. Giacoletto. *Differential Amplifiers*. Wiley, New York, 1970.
13. G. Erdi. "A Low-Drift, Low-Noise Monolithic Operational Amplifier for Low Level Signal Processing," *Fairchild Semiconductor Applications Brief*. No. 136, July 1969.