MANJUSRI SRIDHARA

602-921-5239 • msridh15@asu.edu • https://www.linkedin.com/in/manjusri-s-9a368b207

OBJECTIVE

Analog IC design graduate student with strong transistor-level expertise in **high-gain amplifiers, bias networks, and low-power analog blocks**, complemented by hands-on experience in **RF/mmWave front-end circuits (20–24 GHz)**. Proven ability to design, bias, and verify complete circuit blocks with emphasis on **noise, stability, linearity, and power efficiency** using Cadence Virtuoso and SpectreRF.

EDUCATION

Master Of Science in Electrical Engineering May 2026
Arizona State University, Tempe, AZ 3.92 GPA
Coursework: Analog Integrated Circuits, Advanced Analog IC Design, Digital system circuits, Semiconductor Modeling & Packaging, CMOS Processing, RF Transmitters and Amplifiers, Comm transceiver circuit design, Power management IC design

B. Tech Electronics and Communication Engineering May 2023
REVA University, Bengaluru, India 3.67 GPA

TECHNICAL SKILLS

Analog IC design: Differential amplifiers, OTAs, op-amps, biasing circuits, current mirrors, telescopic and folded cascodes, Noise analysis, Stability (GBW, phase margin, poles/zeros), PSRR, CMRR, slew rate, linearity
RF/mmWave circuit design: LNAs, mixers, LC oscillators, impedance matching, S-parameters, NF, IIP3, P1dB, stability (K, μ), Smith chart analysis
Test & Measurement: Digital Multimeter (DMM), Oscilloscope, Function Generator, Spectrum Analyzer
EDA Tools: Cadence Virtuoso, Spectre, HSPICE, MATLAB, ADS, Ansys HFSS
Programming: Verilog, Python, Embedded C, Git, MATLAB scripting
Soft Skills: Team Collaboration, Clear Communication, Documentation, Problem Solving, Time Management, Ability to Work Under Pressure

RESEARCH EXPERIENCE

Graduate Research Assistant (Circuits & Systems Lab), Arizona State University **Summer 2025**

- Developed STM32 + MATLAB control for an 8-channel **DAC** board, enabling RF phase shifter biasing.
- Automated **PNA**(Keysight N5225B) measurements with **MATLAB** for voltage sweeps, data logging, and **S-parameter extraction**.
- Collaborated on module bring-up, debugging DAC outputs, and ensuring compatibility with future RF phase shifter array testing.
- Gained hands-on experience with **wire bonding**, high-frequency measurement setup, and lab instrumentation.

ACADEMIC PROJECTS

Multi-stage Operational Amplifier Design (Cadence) **Fall 2024**

- Designed and optimized a multi-stage operational amplifier achieving **~96.9 dB gain** and **~1.8 MHz bandwidth**.
- Tuned transistor W/L ratios and compensation capacitors to improve **phase margin (>45°)** and stability.
- Performed DC, AC, and transient simulations in Cadence Spectre.

Telescopic Cascode Differential Amplifier **Spring 2025**

- Designed and simulated a fully differential telescopic cascode op-amp with a Beta-multiplier bias reference circuit
- Achieved 70 dB open-loop gain, 120 MHz unity gain bandwidth, and 1.9 MV/s slew rate while consuming <1 mA total current.
- Verified performance metrics (CMRR > 60 dB, PSRR > 70 dB) using Cadence Virtuoso & Spectre simulations, demonstrating high efficiency and reliability for analog front-end applications.

Source-Degenerated Cascode LNA Design (Cadence & ADS) **Fall 2025**

- Designed a 22 GHz source-degenerated cascode LNA achieving >15 dB gain, NF < 3.5 dB, and S11/S22 < –10 dB across 21–24 GHz.
- Optimized transistor biasing and sizing to minimize NF while maintaining stability ($\mu > 1$, $K-\Delta > 0$) and DC power = 11.8 mW at 1.8 V.
- Performed input/output matching using Smith chart analysis and verified unconditional stability across the band.
- Analyzed IIP3 ≈ –10 dBm and P1dB, highlighting linearity–noise trade-offs through overdrive voltage tuning.

Differential LC Oscillator Design (Cadence Virtuoso, SpectreRF (PSS, PNOISE)) **Fall 2025**

- Designed a differential cross-coupled LC oscillator covering **20.5–24.5 GHz** with discrete capacitor tuning.
- Optimized device sizing and biasing for startup, phase noise, and power efficiency.
- Achieved **< –115 dBc/Hz phase noise** @1 MHz offset **and** >0 dBm output power.

Active Analog Mixer Using Gilbert-Cell Topology **Fall 2025**

- Designed a zero-IF double-balanced Gilbert-cell mixer for **21–24 GHz** operation.
- Achieved **~13.3 dB conversion gain**, **NF <14 dB**, and **IIP3 > +6 dBm**.
- Implemented broadband 50 Ω RF input matching using L-networks.
- Analyzed LO drive, bias current trade-offs, and flicker noise behavior.

INDUSTRIAL EXPERIENCE

Associate Engineer: Bosch Global Software Technologies **July 2023 - July 2024**

- Worked on ADAS ECU HSW layer for Ford, integrating TI Jacinto board (j784s4) with tailored software kit.
- Developed and packaged builds using Conan, Make/CMake in a collaborative development environment.
- Independently merged SDK and QNX/PSDK components (EthFW, PDK), reducing integration issues by 30% and accelerating build/package generation efficiency by 25%.

COURSES AND CERTIFICATIONS

- Circuit Design for High-Speed Serial Links Udemy