

8-Bit Serial Input/Serial or Parallel Output Shift Register with Tri-State Output Latch

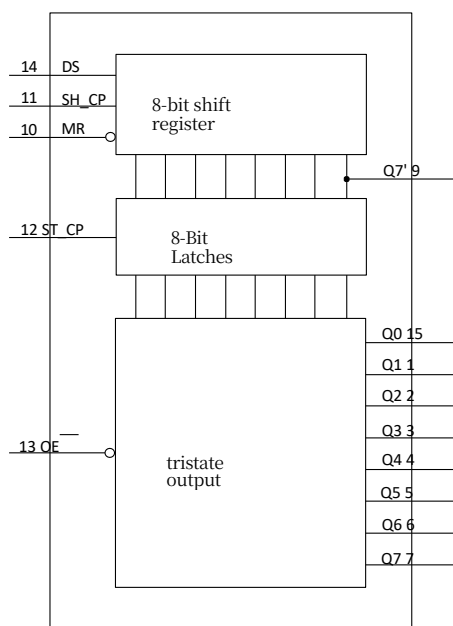
summarize

The 74HC595D is a high speed silicon gate COMS device and is pin compatible with low power Schottky TTL. The 74HC595D consists of an 8-bit shift register and an 8-bit D-type latch with a tri-state parallel output. The shift register receives serial data and provides serial or parallel outputs. The shift register also provides parallel data to the 8-bit latch. The shift register and latch have separate CLK inputs. The device also has an asynchronous reset to the shift register.

specificities

- 8-bit shift register (serial input, serial or parallel output)
- Latch with tri-state output
- 60MHz (typical) shifted output frequency
- ESD protection
- Package: DIP16, SOP16

Function Diagrams



IEC Logic Diagram

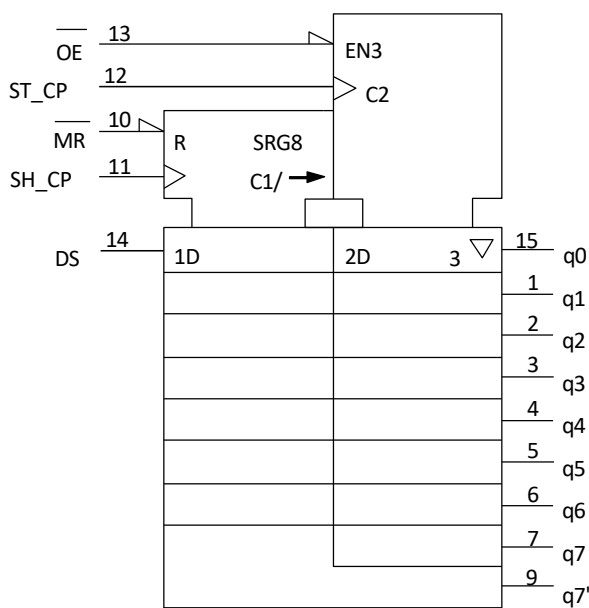
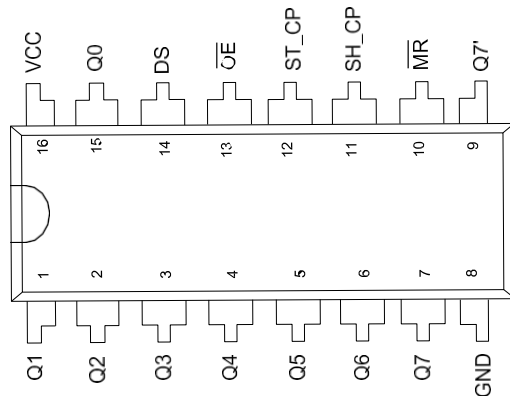


Figure 1 74HC595D functional diagram



Pinout

Ordering Information



Chip Model	Package form	Procurement code
74HC595D	DIP-16	595DIP16
74HC595D	SOP-16	595SOP16

Pin Function Description

Pin Number	Pin Name	Pin Function
1~7	Q1, Q2, Q3, Q4, Q5, Q6, Q7	parallel data output
8	GND	grounding
9	Q7'	Serial data output
10	MR	Master reset (active low)
11	SH_CP	Shift Register Clock Input
12	ST_CP	Latch Clock Input
13	OE	Output potential (active low)
14	DS	Serial Data Input
15	Q0	parallel data output
16	VCC	Positive supply voltage



Limit parameters

GND = 0V unless specifically requested.

Parameter name	notation	prerequisite	minimal	greatest	unit (of measure)
Supply Voltage	V _{CC}		-0.5	+6.5	V
Input diode current	I _{IK}	$V_I < -0.5V \sim V_I > V_{CC} + 0.5V$	-	±20	mA
Output Diode Current	I _{OK}	$V_I < -0.5V \sim V_I > V_{CC} + 0.5V$	-	±20	mA
Output supply current or irrigation current	I _O	$V_I < -0.5V \sim V_I > V_{CC} + 0.5V$ Q7' standard output	-	+25	mA
		Q _n bus drive output	-	+35	mA
Supply current or ground current	V _{CC} , I _{GND}		-	±70	mA
power wastage	P _D	T _{amb} = -40~+125°C		500	mW

Recommended Scope of Work

parameters	Symbol/Condition	minimum value	typical value	maximum values	unit (of measure)
storage temperature	T _{stg}		-65	+150	°C
Supply Voltage	V _{CC}	2.0	5.0	6.0	V
Input Voltage	V _I	0	-	V _{CC}	V
output voltage	V _O	0	-	V _{CC}	V
environmental temperature	T _{amb}	-40	-	+125	°C
Input rise time Tr and fall time Tf	V _{CC} = 2.0V	-	-	1000	ns
	V _{CC} = 4.5V	-	6.0	500	ns
	V _{CC} = 6.0V	-	-	400	ns



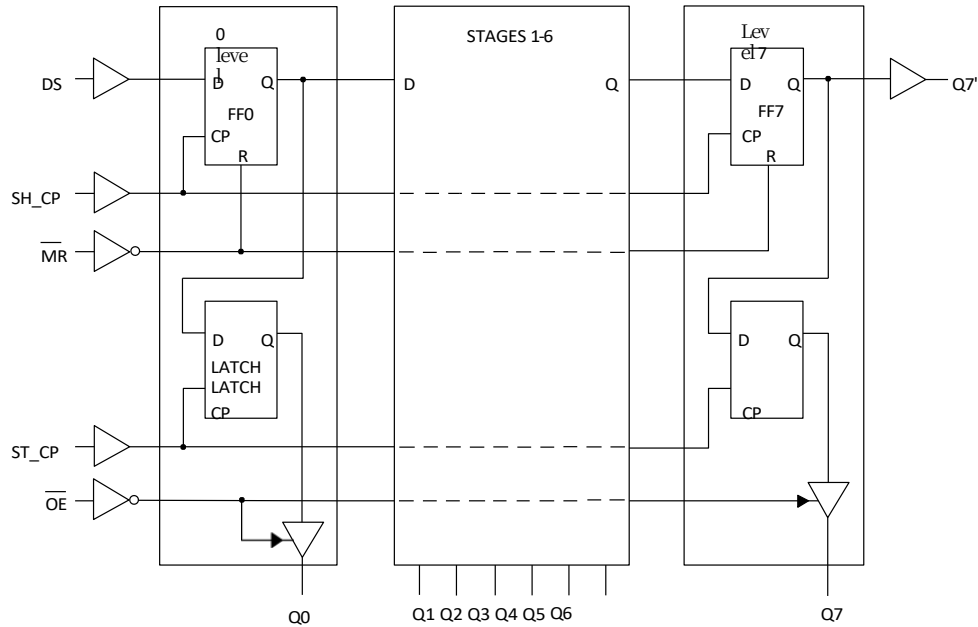
Electrical parameters:

$T_A = -40^\circ$ to $+85^\circ\text{C}$, GND = 0V unless otherwise specified.

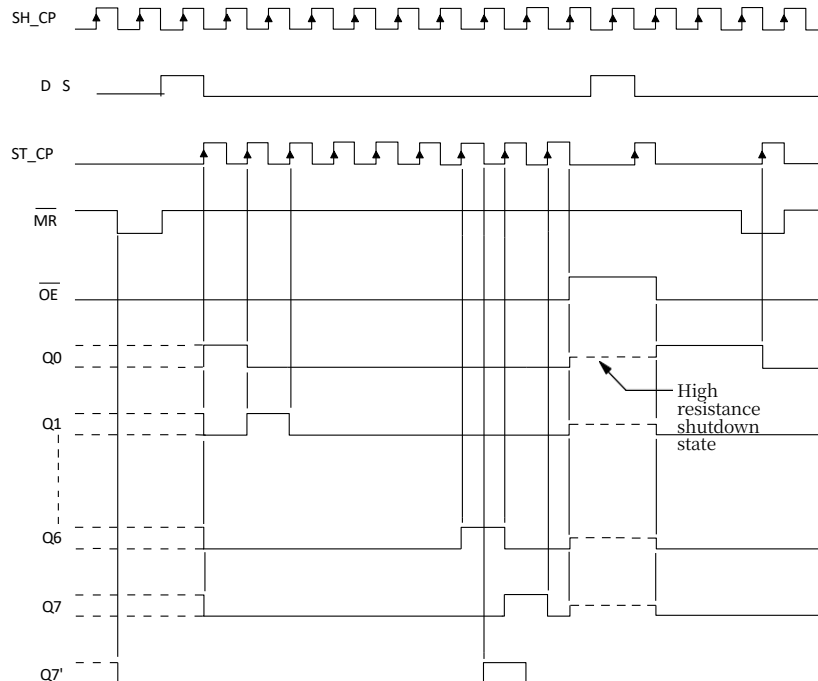
characterization	notation	prerequisite		minimum value	typical value	maximum values	unit (of measure)
		(sth. or sb) else	V_{CC} (V)				
Input High Level Voltage	V_{IH}		2.0	1.4	-	-	V
			4.5	3.15	-	-	
			6.0	4.2	-	-	
Input Low Level Voltage	V_{IL}		2.0	-	-	0.6	V
			4.5	-	-	1.35	
			6.0	-	-	1.8	
Output High Level Voltage	V_{OH}	$V_I = V_{IH}$ OR V_{IL}					V
		All Outputs $I_O = -20\mu\text{A}$	2.0	1.9	2.0	-	
			4.5	4.4	4.5	-	
			6.0	5.9	6.0	-	
		Q7' standard output $I_O = -4.0\text{mA}$ $I_O = -5.2\text{mA}$	4.5	3.84	4.32	-	
			6.0	5.34	5.81	-	
		Qn bus drive output $I_O = -6.0\text{mA}$ $I_O = -7.8\text{mA}$	4.5	3.84	4.32	-	
			6.0	5.34	5.81	-	
Output Low Level Voltage	V_{OL}	$V_I = V_{IH}$ OR V_{IL}					
		All Outputs $I_O = -20\text{A}$	2.0	-	0	0.1	
			4.5	-	0	0.1	
			6.0	-	0	0.1	
		Q7' standard output $I_O = -4.0\text{mA}$ $I_O = -5.2\text{mA}$	4.5	-	0.15	0.33	
			6.0	-	0.16	0.33	
		Qn bus drive output $I_O = -6.0\text{mA}$ $I_O = -7.8\text{mA}$	4.5	-	0.16	0.33	
			6.0	-	0.16	0.33	
Input Leakage Current	I_I	$V_I = V_{CC}$ or GND	6.0	-	-	± 1.0	μA
Tri-state output shutdown current	I_{OZ}	$V_I = V_{IH}$ or V_{IL} $V_O = V_{CC}$ or GND	6.0	-	-	± 5.0	μA
quiescent current	I_{CC}	$V_I = V_{CC}$ or GND $I_O = 0$		6.0	-	80	



logic diagram



chronology





Reference Measurement Information

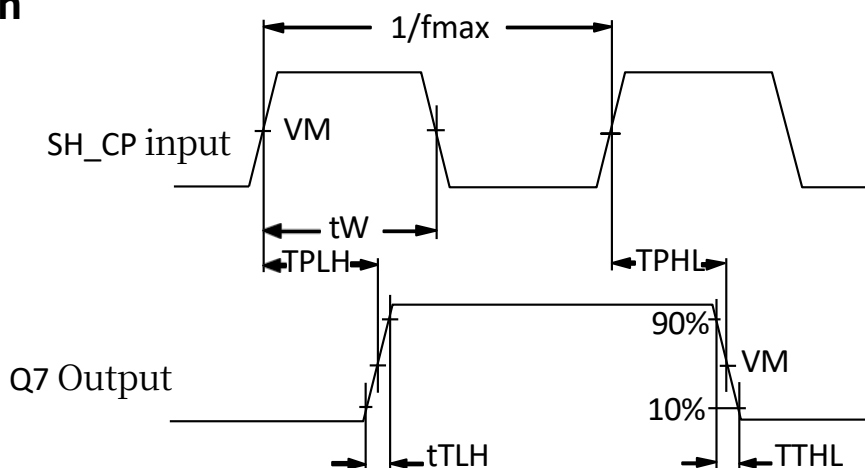


Fig. 1 Waveforms of propagation delay, shift register clock width and maximum shift clock frequency from SH_CP to Q7'

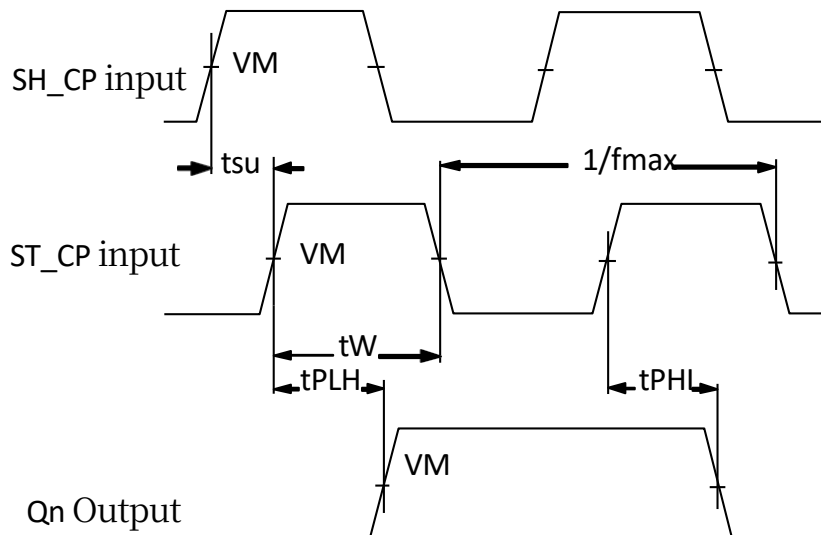


Figure 2 ST_CP to Qn Propagation Delay, Latch Pulse Width and Shift Register CLK to Latch CLK Establishment Time



Reference Measurement Information

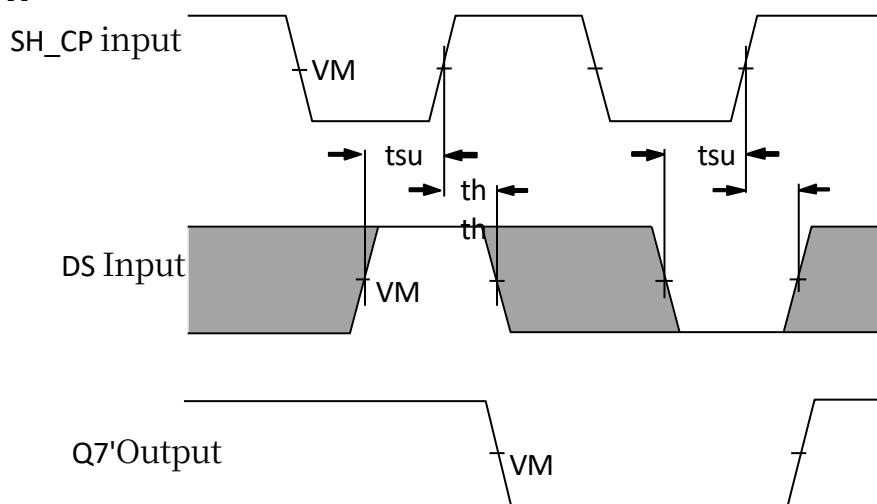


Figure 3 DS Input Data Establishment, Duration

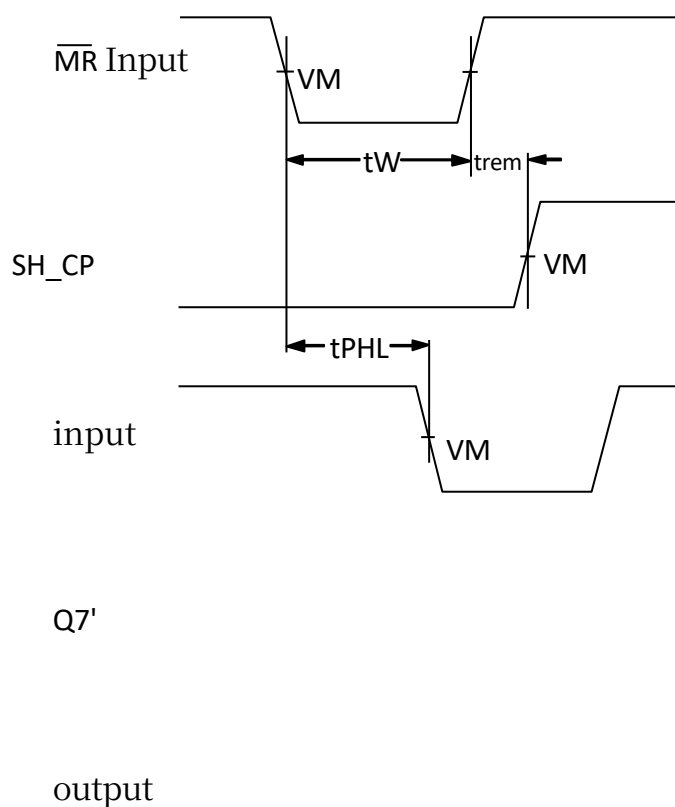


Fig. 4 MR pulse width, propagation delay from MR to Q7' and time from MR to SH_CP



Reference Measurement Information

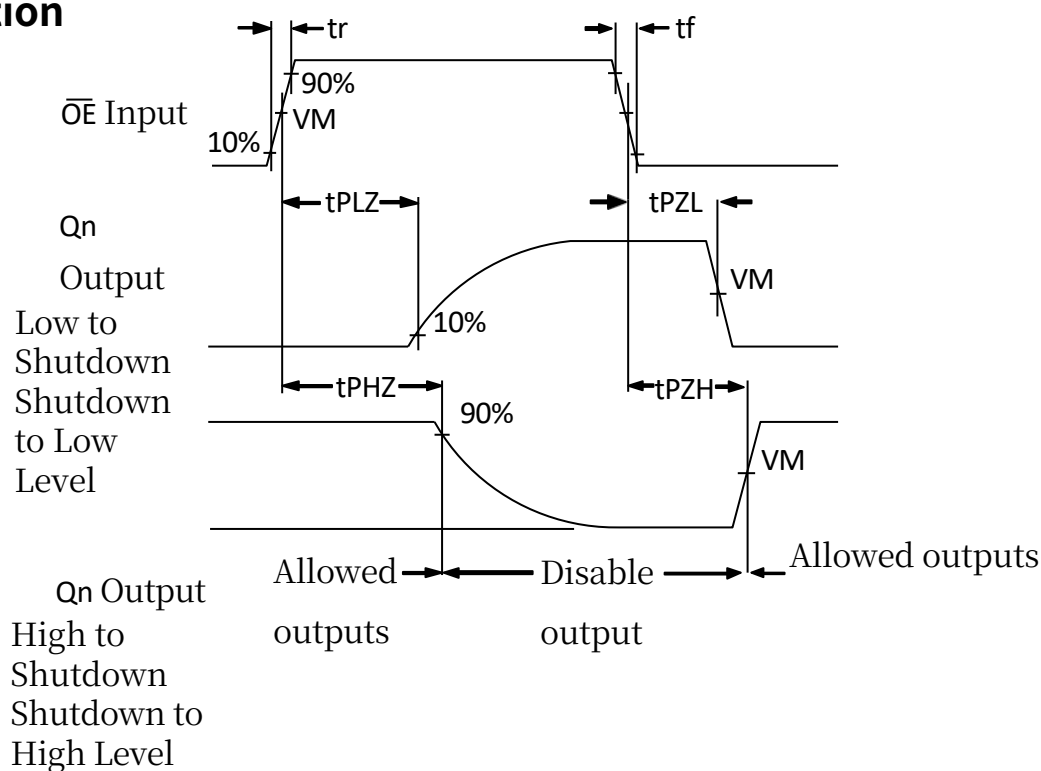


Figure 5 Time waveforms of tri-state allowable and prohibited outputs of OE inputs

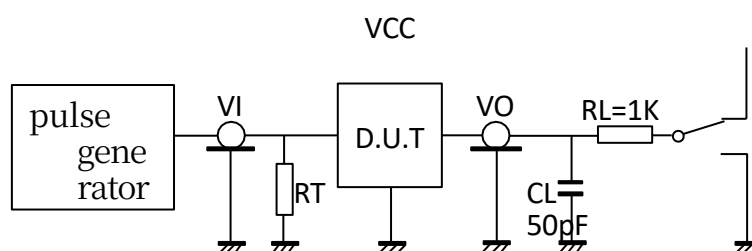
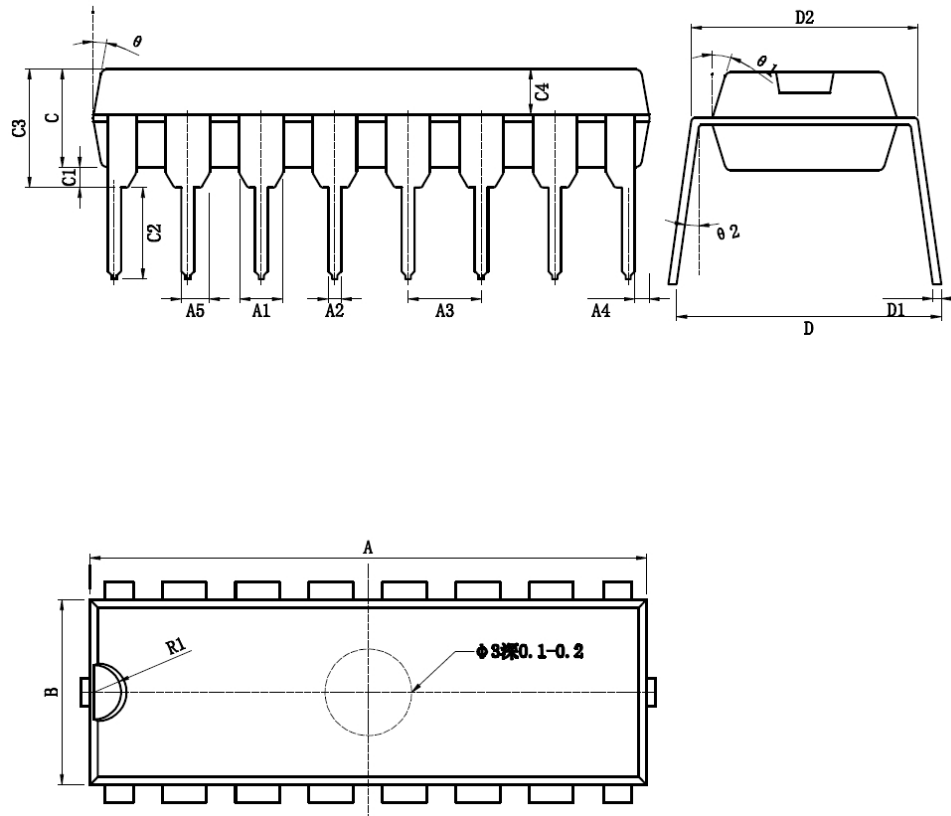


Fig. 63 Test circuit diagram of state output



Outline Package Diagram

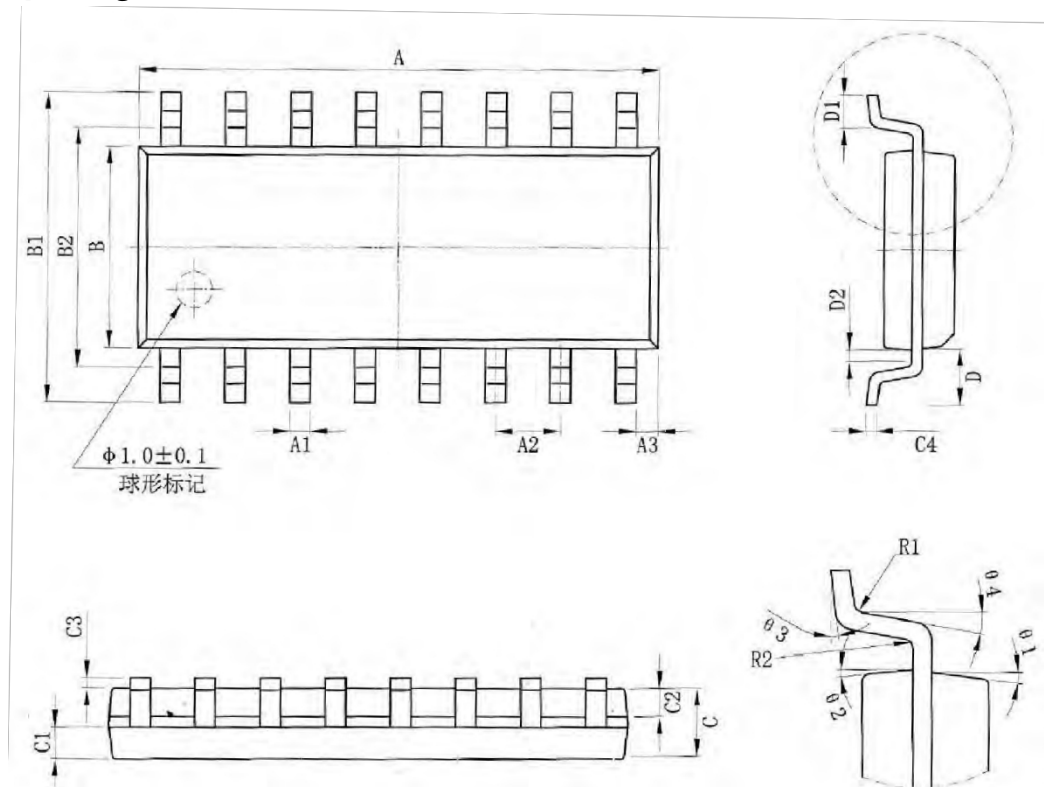
DIP-16 package



notation	Dimensions (mm)		notation	Dimensions (mm)	
	minimal	greatest		minimal	greatest
A	19.00	19.20	C3	3.85	4.45
A1	1.524TYP		C4	1.40	1.50
A2	0.41	0.51	D	8.20	8.80
A3	2.54TYP		D1	0.20	0.35
A4	0.38TYP		D2	7.74	8.00
A5	0.99 TYP		theta	10°TYP	
B	6.30	6.50	theta 1	17°TYP	
C	3.00	3.20	theta 2	6°TYP	
C1	0.51 TYP		R1	1.27TYP	
C2	3.00	3.60			



SOP-16 package



notation	Dimensions (mm)		notation	Dimensions (mm)	
	minimal	greatest		minimal	greatest
A	9.80	10.00	C3	0.05	0.25
A1	0.356	0.456	C4	0.203	0.233
A2	1.27TYP		D	0.15TYP	
A3	0.302TYP		D1	0.40	0.70
B	3.85	3.95	D2	0.15	0.25
B1	5.84	6.24	R1	0.20TYP	
B2	5.00TYP		R2	0.20TYP	
C	1.40	1.60	$\theta 1$	8°~12°TYP	
C1	0.61	0.71	$\theta 2$	8°~12°TYP	
C2	0.54	0.64	$\theta 3$	0°~12°	
			$\theta 4$	4°~12°	



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**8-Bit Serial Input/Serial or Parallel Output Shift Register
with Tri-State Output Latch**

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