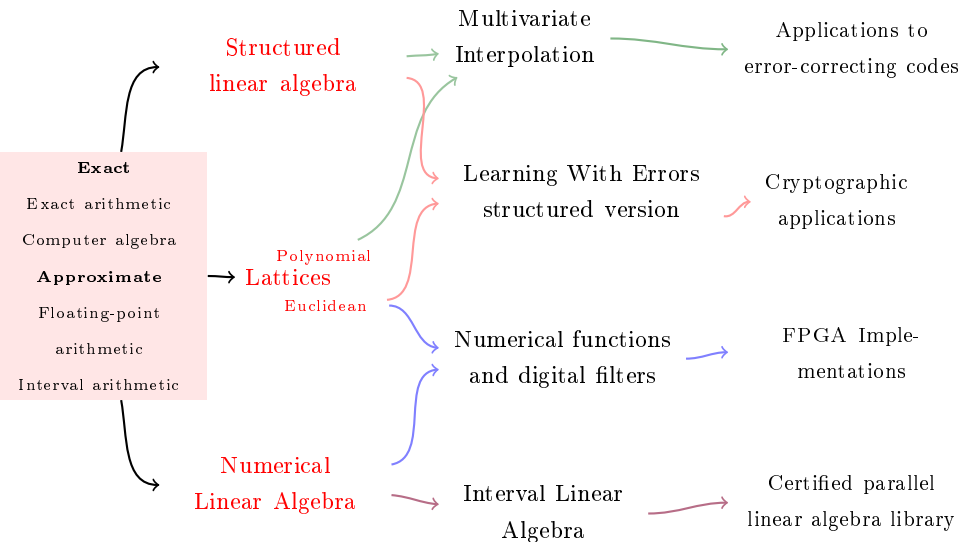


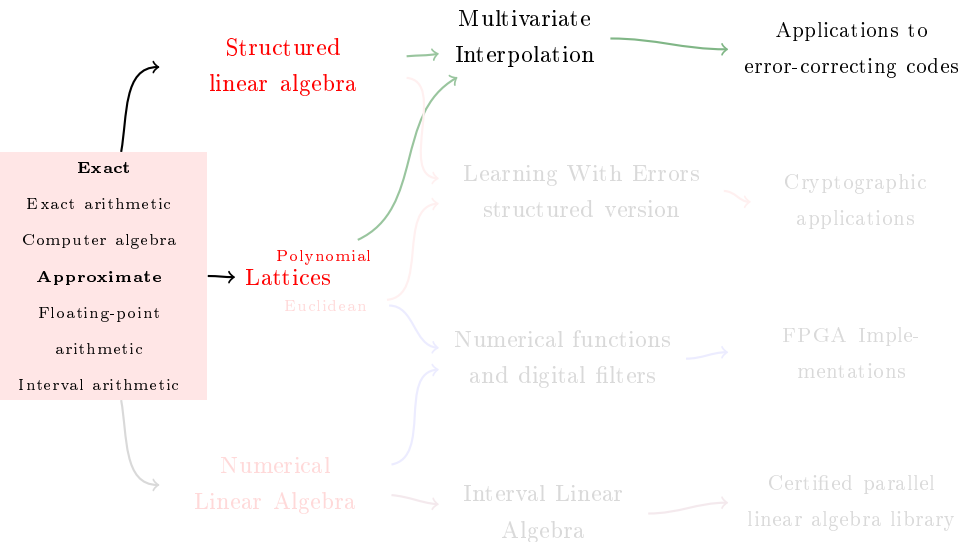
# Journée des doctorants

Silviu Filip   Sébastien Maulat   Stephen Melczer  
Vincent Neiger   Marie Paindavoine  
Antoine Plet   Valentina Popescu

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June 2015





# AriC — Error-correcting codes

Goal:

Enable **reliable** delivery of data over **unreliable** communication channels

Strategy:

add **redundancy** to the message

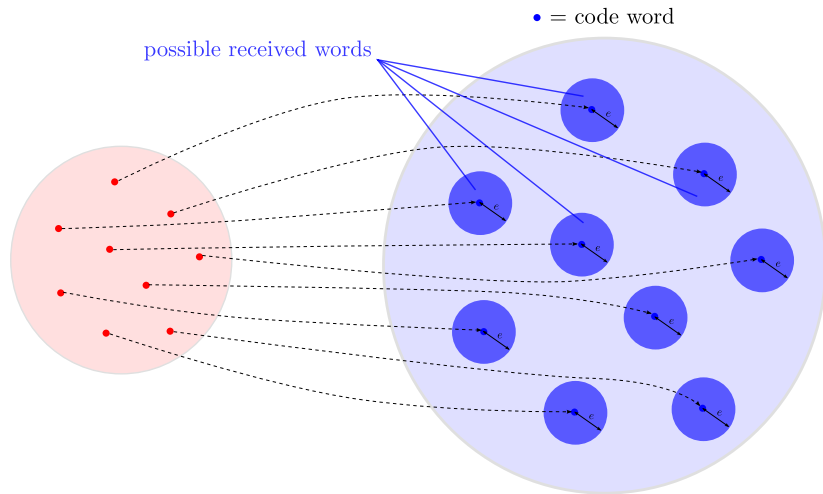
add **redundancy** to the message

add **redundancy** to the message



(courtesy of J.S.R. Nielsen)

# AriC — Error-correcting codes



polynomials of degree  $\leq k$   $\longrightarrow$  their evaluation at  $x_1, \dots, x_n$   
 $w = w_0 + w_1X + \dots + w_kX^k$   $(w(x_1), \dots, w(x_n))$

# AriC — (list-)Decoding

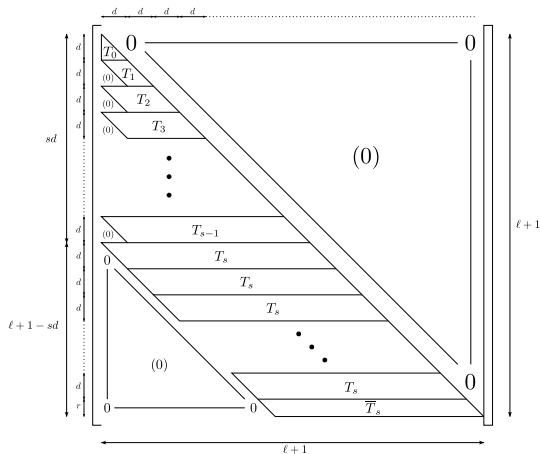
Find a **solution** of a **structured linear system**,

$$\begin{array}{c}
 \xrightarrow{mt} \quad \xrightarrow{mt-k} \quad \quad \quad \xrightarrow{N_j} \quad \quad \quad \xrightarrow{mt-\ell k} \\
 \begin{array}{c}
 \updownarrow nm \\
 \updownarrow n(m-1) \\
 \updownarrow M_i \\
 \updownarrow n
 \end{array}
 \left[ \begin{array}{c|c|c|c|c}
 A_{0,0} & & & A_{0,j} & A_{0,\ell} \\
 \hline
 & & & & \\
 \hline
 & & & & \\
 \hline
 A_{i,0} & & & A_{i,j} & A_{i,\ell} \\
 \hline
 & & & & \\
 \hline
 A_{m-1,0} & & & A_{m-1,j} & A_{m-1,\ell}
 \end{array} \right]
 \end{array}$$

where  $A_{i,j}$  is a **Toeplitz** / **Hankel** / **Vandermonde** / ... matrix

# AriC — (list-)Decoding

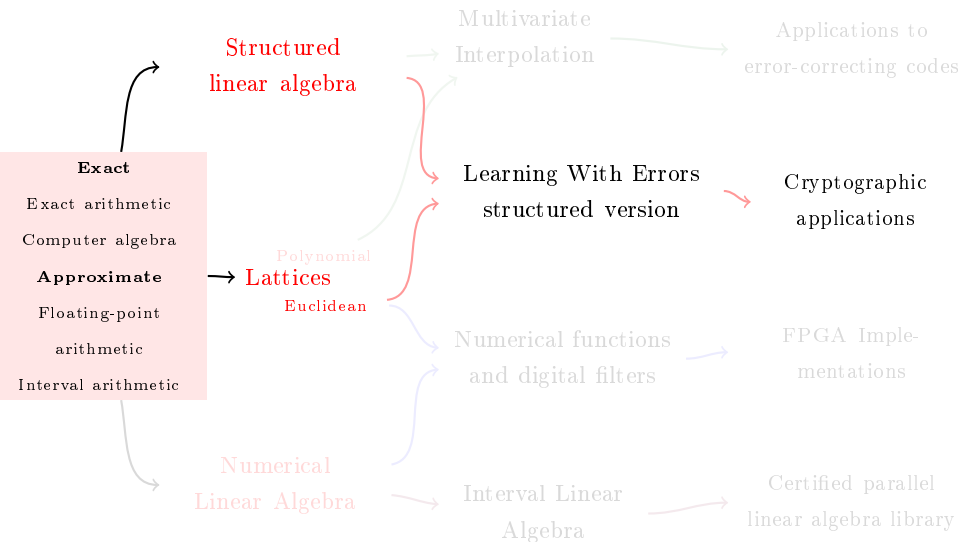
Find a **short vector** in a (structured) **polynomial lattice**,



where  $T_i$  has a **Toeplitz** structure:

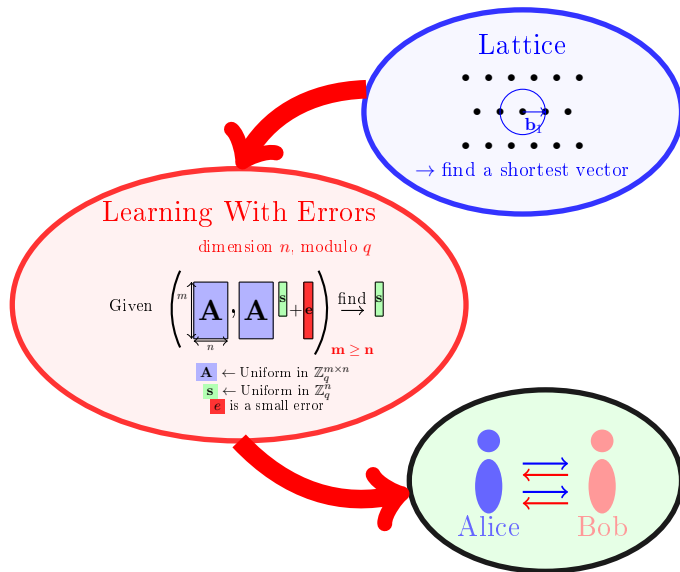
$$T_i = \begin{array}{|c|} \hline \begin{array}{c} \begin{array}{cccc} T_{i,0} & T_{i,1} & \dots & T_{i,sd} \end{array} \\ \begin{array}{c} (0) \end{array} \end{array} \\ \hline \end{array}$$

$(i+1)d$



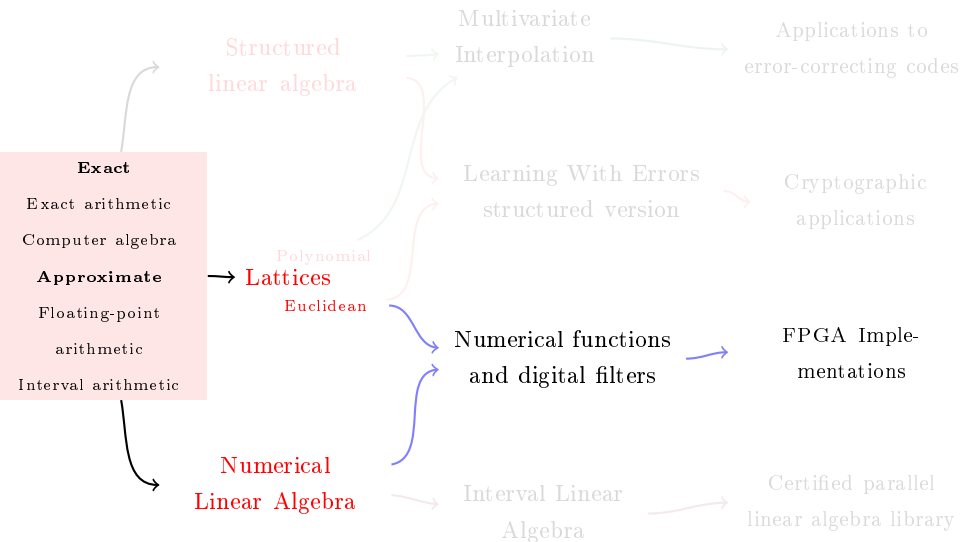


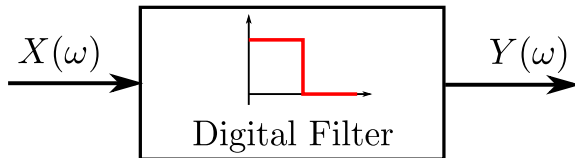
# AriC – Lattice-Based Cryptography



# AriC – Lattice-Based Cryptography

- ▶ Public Key Encryption
- ▶ Identity Based Encryption
- ▶ Fully Homomorphic Encryption
  
- ▶ Signature
- ▶ Group Signature
- ▶ Hash Function
  
- ▶ Cryptographic Multilinear Maps



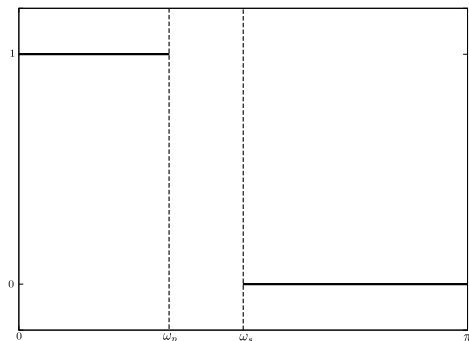


$$Y(\omega) = H_d(\omega)X(\omega), \omega \in [0, \pi]$$

Two types of filters:

- ▶ finite impulse response (**FIR**)  $\Rightarrow H_d(\omega)$  **polynomial**
- ▶ infinite impulse response (**IIR**)  $\Rightarrow H_d(\omega)$  **rational function**

FIR case:  $H_d(\omega) = \sum_{k=0}^L a_k \cos(\omega k)$



Steps:

1. Optimal filter computation:

$$H_d(\omega) = \sum_{k=0}^L a_k \cos(\omega k)$$

Naive rounding:

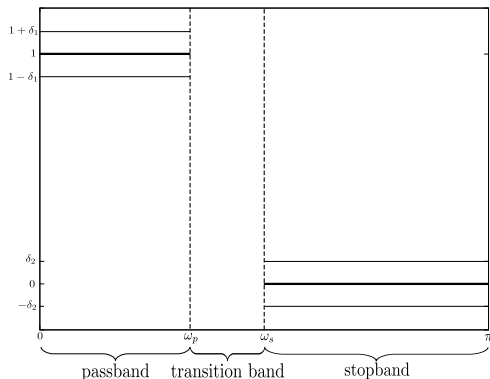
$$\bar{H}_d(\omega) = \sum_{k=0}^L \bar{a}_k \cos(\omega k)$$

2. Coefficient quantization:

$$H_d^*(\omega) = \sum_{k=0}^L a_k^* \cos(\omega k)$$

Goal: filter synthesis toolchain for embedded and FPGA targets

FIR case:  $H_d(\omega) = \sum_{k=0}^L a_k \cos(\omega k)$



Steps:

1. Optimal filter computation:

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1. Optimal filter computation:

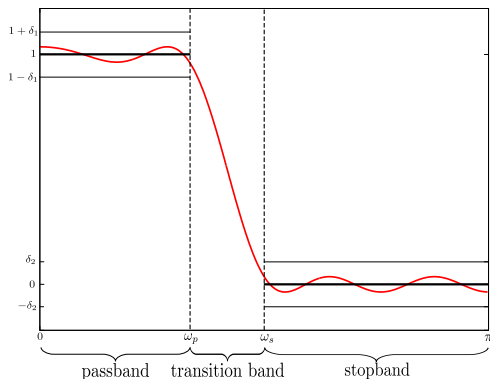
$$H_d(\omega) = \sum_{k=0}^L a_k \cos(\omega k)$$

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1. Optimal filter computation:

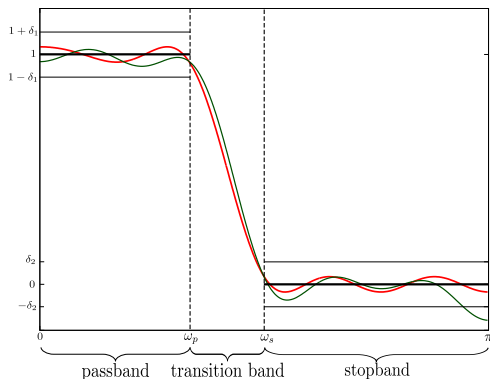
$$H_d(\omega) = \sum_{k=0}^L a_k \cos(\omega k)$$

Naive rounding:

$$\bar{H}_d(\omega) = \sum_{k=0}^L \bar{a}_k \cos(\omega k)$$

2. Coefficient quantization:

$$H_d^*(\omega) = \sum_{k=0}^L a_k^* \cos(\omega k)$$



Goal: filter synthesis toolchain for embedded and FPGA targets



# AriC – Digital Filter Design

$$\text{FIR case: } H_d(\omega) = \sum_{k=0}^L a_k \cos(\omega k)$$

Steps:

1. Optimal filter computation:

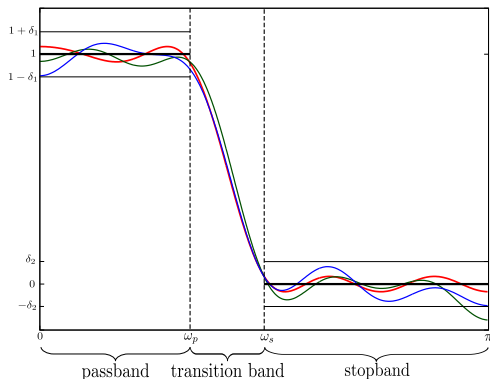
$$H_d(\omega) = \sum_{k=0}^L a_k \cos(\omega k)$$

Naive rounding:

$$\bar{H}_d(\omega) = \sum_{k=0}^L \bar{a}_k \cos(\omega k)$$

2. Coefficient quantization:

$$H_d^*(\omega) = \sum_{k=0}^L a_k^* \cos(\omega k)$$



Goal: filter synthesis toolchain for embedded and FPGA targets

FIR case:  $H_d(\omega) = \sum_{k=0}^L a_k \cos(\omega k)$

Steps:

1. Optimal filter computation:

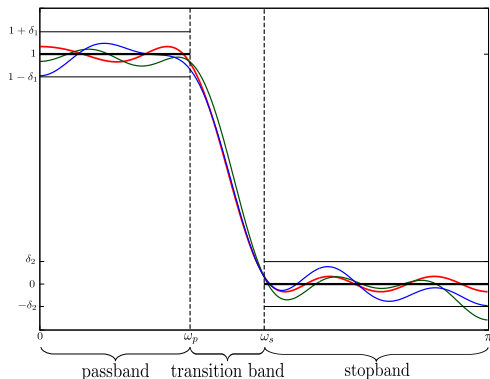
$$H_d(\omega) = \sum_{k=0}^L a_k \cos(\omega k)$$

Naive rounding:

$$\overline{H}_d(\omega) = \sum_{k=0}^L \overline{a}_k \cos(\omega k)$$

2. Coefficient quantization:

$$H_d^*(\omega) = \sum_{k=0}^L a_k^* \cos(\omega k)$$



Goal: filter synthesis toolchain for embedded and FPGA targets

