12.4 Interrupt Vectors in ATmega328 and ATmega328P

Table 12-6. Reset and Interrupt Vectors in ATmega328 and ATmega328P

VectorNo.	Program Address(2)	Source	Interrupt Definition
1	0x0000(1)	RESET	External Pin, Power-on Reset, Brown-out Reset and Watchdog System Reset
2	0x0002	INT0	External Interrupt Request 0
3	0x0004	INT1	External Interrupt Request 1
4	0x0006	PCINT0	Pin Change Interrupt Request 0
5	0x0008	PCINT1	Pin Change Interrupt Request 1
6	0x000A	PCINT2	Pin Change Interrupt Request 2
7	0x000C	WDT	Watchdog Time-out Interrupt
8	0x000E	TIMER2_COMPA	Timer/Counter2 Compare Match A
9	0x0010	TIMER2_COMPB	Timer/Counter2 Compare Match B
10	0x0012	TIMER2_OVF	Timer/Counter2 Overflow
11	0x0014	TIMER1_CAPT	Timer/Counter1 Capture Event
12	0x0016	TIMER1_COMPA	Timer/Counter1 Compare Match A
13	0x0018	TIMER1_COMPB	Timer/Counter1 Compare Match B
14	0x001A	TIMER1_OVF	Timer/Counter1 Overflow
15	0x001C	TIMER0_COMPA	Timer/Counter0 Compare Match A
16	0x001E	TIMER0_COMPB	Timer/Counter0 Compare Match B
17	0x0020	TIMER0_OVF	Timer/Counter0 Overflow
18	0x0022	SPI_STC	SPI Serial Transfer Complete
19	0x0024	USART_RX	USART Rx Complete
20	0x0026	USART_UDRE	USART, Data Register Empty
21	0x0028	USART_TX	USART, Tx Complete
22	0x002A	ADC	ADC Conversion Complete
23	0x002C	EE_READY	EEPROM Ready
24	0x002E	ANALOG_COMP	Analog Comparator
25	0x0030	TWI	2-wire Serial Interface
26	0x0032	SPM_Ready	Store Program Memory Ready

Notes:
1. When the BOOTRST Fuse is programmed, the device will jump to the Boot Loader address at reset, see "Boot Loader Support – Read-While-Write Self-Programming" on page 272.
2. When the IVSEL bit in MCUCR is set, Interrupt Vectors will be moved to the start of the Boot Flash Section. The address of each Interrupt Vector will then be the address in this table added to the start address of the Boot Flash Section.

Table 12-7 on page 75 shows reset and Interrupt Vectors placement for the various combinations of BOOTRST and IVSEL settings. If the program never enables an interrupt source, the Interrupt Vectors are not used, and

regular program code can be placed at these locations. This is also the case if the Reset Vector is in the Application section while the Interrupt Vectors are in the Boot section or vice versa.

Table 12-7. Reset and Interrupt Vectors Placement in ATmega328 and ATmega328P(1)

BOOTRST	IVSEL	Reset Address	Interrupt Vectors Start Address
1	0	0x000	0x002
1	1	0x000	Boot Reset Address + 0x0002
0	0	Boot Reset Address	0x002
0	1	Boot Reset Address	Boot Reset Address + 0x0002

Note: 1. The Boot Reset Address is shown in Table 27-7 on page 284. For the BOOTRST Fuse “1” means unprogrammed while “0” means programmed.

The most typical and general program setup for the Reset and Interrupt Vector Addresses in ATmega328/328P is:

```
Address  Labels  Code              Comments
0x0000           jmp    RESET       ; Reset Handler
0x0002           jmp    EXT_INT0    ; IRQ0 Handler
0x0004           jmp    EXT_INT1    ; IRQ1 Handler
0x0006           jmp    PCINT0      ; PCINT0 Handler
0x0008           jmp    PCINT1      ; PCINT1 Handler
0x000A           jmp    PCINT2      ; PCINT2 Handler
0x000C           jmp    WDT         ; Watchdog Timer Handler
0x000E           jmp    TIM2_COMPA  ; Timer2 Compare A Handler
0x0010           jmp    TIM2_COMPB  ; Timer2 Compare B Handler
0x0012           jmp    TIM2_OVF    ; Timer2 Overflow Handler
0x0014           jmp    TIM1_CAPT   ; Timer1 Capture Handler
0x0016           jmp    TIM1_COMPA  ; Timer1 Compare A Handler
0x0018           jmp    TIM1_COMPB  ; Timer1 Compare B Handler
0x001A           jmp    TIM1_OVF    ; Timer1 Overflow Handler
0x001C           jmp    TIM0_COMPA  ; Timer0 Compare A Handler
0x001E           jmp    TIM0_COMPB  ; Timer0 Compare B Handler
0x0020           jmp    TIM0_OVF    ; Timer0 Overflow Handler
0x0022           jmp    SPI_STC     ; SPI Transfer Complete Handler
0x0024           jmp    USART_RXC   ; USART, RX Complete Handler
0x0026           jmp    USART_UDRE  ; USART, UDR Empty Handler
0x0028           jmp    USART_TXC   ; USART, TX Complete Handler
0x002A           jmp    ADC         ; ADC Conversion Complete Handler
0x002C           jmp    EE_RDY      ; EEPROM Ready Handler
0x002E           jmp    ANA_COMP    ; Analog Comparator Handler
0x0030           jmp    TWI         ; 2-wire Serial Interface Handler
0x0032           jmp    SPM_RDY     ; Store Program Memory Ready Handler
;
0x0034   RESET:  ldi    r16, high(RAMEND); Main program start
0x0035           out    SPH,r16     ; Set Stack Pointer to top of RAM
0x0036           ldi    r16, low(RAMEND)
0x0037           out    SPL,r16
0x0038           sei                ; Enable interrupts
0x0039           <instr>  xxx
  ...     ...    ...     ...
```

When the BOOTRST Fuse is unprogrammed, the Boot section size set to 2Kbytes and the IVSEL bit in the MCUCR Register is set before any interrupts are enabled, the most typical and general program setup for the Reset and Interrupt Vector Addresses in ATmega328/328P is:

```
Address  Labels  Code              Comments
0x0000   RESET:  ldi    r16,high(RAMEND); Main program start
0x0001           out    SPH,r16     ; Set Stack Pointer to top of RAM
0x0002           ldi    r16,low(RAMEND)
0x0003           out    SPL,r16
0x0004           sei                ; Enable interrupts
0x0005           <instr>  xxx
;
.org 0x3C02
0x3C02           jmp    EXT_INT0    ; IRQ0 Handler
0x3C04           jmp    EXT_INT1    ; IRQ1 Handler
...              ...    ...         ;
0x3C32           jmp    SPM_RDY     ; Store Program Memory Ready Handler
```

When the BOOTRST Fuse is programmed and the Boot section size set to 2Kbytes, the most typical and general program setup for the Reset and Interrupt Vector Addresses in ATmega328/328P is:

```
Address  Labels  Code              Comments
.org 0x0002
0x0002           jmp    EXT_INT0    ; IRQ0 Handler
0x0004           jmp    EXT_INT1    ; IRQ1 Handler
...              ...    ...         ;
0x0032           jmp    SPM_RDY     ; Store Program Memory Ready Handler
;
.org 0x3C00
0x3C00   RESET:  ldi    r16,high(RAMEND); Main program start
0x3C01           out    SPH,r16     ; Set Stack Pointer to top of RAM
0x3C02           ldi    r16,low(RAMEND)
0x3C03           out    SPL,r16
0x3C04           sei                ; Enable interrupts
0x3C05           <instr>  xxx
```

When the BOOTRST Fuse is programmed, the Boot section size set to 2Kbytes and the IVSEL bit in the MCUCR Register is set before any interrupts are enabled, the most typical and general program setup for the Reset and Interrupt Vector Addresses in ATmega328/328P is:

```
Address  Labels  Code              Comments
;
.org 0x3C00
0x3C00           jmp    RESET       ; Reset handler
0x3C02           jmp    EXT_INT0    ; IRQ0 Handler
0x3C04           jmp    EXT_INT1    ; IRQ1 Handler
...              ...    ...         ;
0x3C32           jmp    SPM_RDY     ; Store Program Memory Ready Handler
;
0x3C34   RESET:  ldi    r16,high(RAMEND); Main program start
0x3C35           out    SPH,r16     ; Set Stack Pointer to top of RAM
0x3C36           ldi    r16,low(RAMEND)
0x3C37           out    SPL,r16
0x3C38           sei                ; Enable interrupts
0x3C39           <instr>  xxx
```