



Table 12. STM32F745xx and STM32F746xx alternate function mapping

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		SYS	TIM1/2	TIM3/4/5	TIM8/9/10/ 11/LPTIM 1/CEC	I2C1/2/3/ 4/CEC	SPI1/2/3/ 4/5/6	SPI3/ SAI1	SPI2/3/U SART1/2/ 3/UART5/ SPDIFRX	SAI2/US ART6/UA RT4/5/7/8 /SPDIFR X	CAN1/2/T IM12/13/ 14/QUAD SPI/LCD	SAI2/QU ADSPI/O TG2_HS/ OTG1_FS	ETH/ OTG1_FS	FMC/SD MMC1/O TG2_FS	DCMI	LCD	SYS
Port A	PA0	-	TIM2_C H1/TIM2 _ETR	TIM5_C H1	TIM8_ET R	-	-	-	USART2 _CTS	UART4_ TX	-	SAI2_SD_ B	ETH_MII_ CRS	-	-	-	EVEN TOUT
	PA1	-	TIM2_C H2	TIM5_C H2	-	-	-	-	USART2 _RTS	UART4_ RX	QUADSP I_BK1_IO 3	SAI2_MC K_B	ETH_MII_ RX_CLK/ ETH_RMI I_REF_C LK	-	-	LCD_R2	EVEN TOUT
	PA2	-	TIM2_C H3	TIM5_C H3	TIM9_CH 1	-	-	-	USART2 _TX	SAI2_SC K_B	-	-	ETH_MDI O	-	-	LCD_R1	EVEN TOUT
	PA3	-	TIM2_C H4	TIM5_C H4	TIM9_CH 2	-	-	-	USART2 _RX	-	-	OTG_HS_ ULPI_D0	ETH_MII_ COL	-	-	LCD_B5	EVEN TOUT
	PA4	-	-	-	-	-	SPI1_NS S/I2S1_ WS	SPI3_NS S/I2S3_ WS	USART2 _CK	-	-	-	-	OTG_HS_ _SOF	DCMI_H SYNC	LCD_VS YNC	EVEN TOUT
	PA5	-	TIM2_C H1/TIM2 _ETR	-	TIM8_CH 1N	-	SPI1_SC K/I2S1_ CK	-	-	-	-	OTG_HS_ ULPI_CK	-	-	-	LCD_R4	EVEN TOUT
	PA6	-	TIM1_B KIN	TIM3_C H1	TIM8_BKI N	-	SPI1_MI SO	-	-	-	TIM13_C H1	-	-	-	DCMI_PI XCLK	LCD_G2	EVEN TOUT
	PA7	-	TIM1_C H1N	TIM3_C H2	TIM8_CH 1N	-	SPI1_M OSI/I2S1 _SD	-	-	-	TIM14_C H1	-	ETH_MII_ RX_DV/E TH_RMII_ CRS_DV	FMC_SD NWE	-	-	EVEN TOUT
	PA8	MCO1	TIM1_C H1	-	TIM8_BKI N2	I2C3_SC L	-	-	USART1 _CK	-	-	OTG_FS_ SOF	-	-	-	LCD_R6	EVEN TOUT
	PA9	-	TIM1_C H2	-	-	I2C3_SM BA	SPI2_SC K/I2S2_ CK	-	USART1 _TX	-	-	-	-	-	DCMI_D 0	-	EVEN TOUT
	PA10	-	TIM1_C H3	-	-	-	-	-	USART1 _RX	-	-	OTG_FS_ ID	-	-	DCMI_D 1	-	EVEN TOUT
	PA11	-	TIM1_C H4	-	-	-	-	-	USART1 _CTS	-	CAN1_R X	OTG_FS_ DM	-	-	-	LCD_R4	EVEN TOUT

Table 12. STM32F745xx and STM32F746xx alternate function mapping (continued)

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		SYS	TIM1/2	TIM3/4/5	TIM8/9/10/11/LPTIM1/CEC	I2C1/2/3/4/CEC	SPI1/2/3/4/5/6	SPI3/SPI1	SPI2/3/USART1/2/3/UART5/SPDIFRX	SAI2/USART6/UART4/5/7/8/SPDIFRX	CAN1/2/TIM12/13/14/QUADSPI/LCD	SAI2/QUADSPI/OTG_HS/OTG1_FS	ETH/OTG1_FS	FMC/SDMMC1/OTG2_FS	DCMI	LCD	SYS
Port A	PA12	-	TIM1_ETR	-	-	-	-	-	USART1_RTS	SAI2_FS_B	CAN1_TX	OTG_FS_DP	-	-	-	LCD_R5	EVEN TOUT
	PA13	JTMS-SWDIO	-	-	-	-	-	-	-	-	-	-	-	-	-	-	EVEN TOUT
	PA14	JTCK-SWCLK	-	-	-	-	-	-	-	-	-	-	-	-	-	-	EVEN TOUT
	PA15	JTDI	TIM2_CH1/TIM2_ETR	-	-	HDMI-CEC	SPI1_NSS/I2S1_WS	SPI3_NSS/I2S3_WS	-	UART4_RTS	-	-	-	-	-	-	EVEN TOUT
Port B	PB0	-	TIM1_CH2N	TIM3_CH3	TIM8_CH2N	-	-	-	-	UART4_CTS	LCD_R3	OTG_HS_ULPI_D1	ETH_MII_RXD2	-	-	-	EVEN TOUT
	PB1	-	TIM1_CH3N	TIM3_CH4	TIM8_CH3N	-	-	-	-	-	LCD_R6	OTG_HS_ULPI_D2	ETH_MII_RXD3	-	-	-	EVEN TOUT
	PB2	-	-	-	-	-	-	SAI1_SDA	SPI3_MOSI/I2S3_SD	-	QUADSPI_CLK	-	-	-	-	-	EVEN TOUT
	PB3	JTDO/TRACES_WO	TIM2_CH2	-	-	-	SPI1_SCK/I2S1_CK	SPI3_SCK/I2S3_CK	-	-	-	-	-	-	-	-	EVEN TOUT
	PB4	NJTRST	-	TIM3_CH1	-	-	SPI1_MISO	SPI3_MISO	SPI2_NSS/I2S2_WS	-	-	-	-	-	-	-	EVEN TOUT
	PB5	-	-	TIM3_CH2	-	I2C1_SMBA	SPI1_MOSI/I2S1_SD	SPI3_MOSI/I2S3_SD	-	-	CAN2_RX	OTG_HS_ULPI_D7	ETH_PPS_OUT	FMC_SD_CKE1	DCMI_D10	-	EVEN TOUT
	PB6	-	-	TIM4_CH1	HDMI-CEC	I2C1_SCL	-	-	USART1_TX	-	CAN2_TX	QUADSPI_BK1_NCS	-	FMC_SD_NE1	DCMI_D5	-	EVEN TOUT
	PB7	-	-	TIM4_CH2	-	I2C1_SDA	-	-	USART1_RX	-	-	-	-	FMC_NL	DCMI_VSYNC	-	EVEN TOUT
	PB8	-	-	TIM4_CH3	TIM10_CH1	I2C1_SCL	-	-	-	-	CAN1_RX	-	ETH_MII_TXD3	SDMMC1_D4	DCMI_D6	LCD_B6	EVEN TOUT



Table 12. STM32F745xx and STM32F746xx alternate function mapping (continued)

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		SYS	TIM1/2	TIM3/4/5	TIM8/9/10/ 11/LPTIM 1/CEC	I2C1/2/3/ 4/CEC	SPI1/2/3/ 4/5/6	SPI3/ SAI1	SPI2/3/U SART1/2/ 3/UART5/ SPDIFRX	SAI2/US ART6/UA RT4/5/7/8 /SPDIFR X	CAN1/2/T IM12/13/ 14/QUAD SPI/LCD	SAI2/QU ADSPI/O TG2_HS/ OTG1_FS	ETH/ OTG1_FS	FMC/SD MMC1/O TG2_FS	DCMI	LCD	SYS
Port B	PB9	-	-	TIM4_C H4	TIM11_CH 1	I2C1_SD A	SPI2_NS S/I2S2_ WS	-	-	-	CAN1_T X	-	-	SDMMC 1_D5	DCMI_D 7	LCD_B7	EVEN TOUT
	PB10	-	TIM2_C H3	-	-	I2C2_SC L	SPI2_SC K/I2S2_ CK	-	USART3 _TX	-	-	OTG_HS_ ULPI_D3	ETH_MII_ RX_ER	-	-	LCD_G4	EVEN TOUT
	PB11	-	TIM2_C H4	-	-	I2C2_SD A	-	-	USART3 _RX	-	-	OTG_HS_ ULPI_D4	ETH_MII_ TX_EN/ ETH_RMII_ TX_EN	-	-	LCD_G5	EVEN TOUT
	PB12	-	TIM1_B KIN	-	-	I2C2_SM BA	SPI2_NS S/I2S2_ WS	-	USART3 _CK	-	CAN2_R X	OTG_HS_ ULPI_D5	ETH_MII_ TXD0/ET H_RMII_T XD0	OTG_HS _ID	-	-	EVEN TOUT
	PB13	-	TIM1_C H1N	-	-	-	SPI2_SC K/I2S2_ CK	-	USART3 _CTS	-	CAN2_T X	OTG_HS_ ULPI_D6	ETH_MII_ TXD1/ET H_RMII_T XD1	-	-	-	EVEN TOUT
	PB14	-	TIM1_C H2N	-	TIM8_CH 2N	-	SPI2_MI SO	-	USART3 _RTS	-	TIM12_C H1	-	-	OTG_HS _DM	-	-	EVEN TOUT
	PB15	RTC_R EFIN	TIM1_C H3N	-	TIM8_CH 3N	-	SPI2_M OSI/I2S2 _SD	-	-	-	TIM12_C H2	-	-	OTG_HS _DP	-	-	EVEN TOUT
Port C	PC0	-	-	-	-	-	-	-	-	SAI2_FS _B	-	OTG_HS_ ULPI_ST P	-	FMC_SD NWE	-	LCD_R5	EVEN TOUT
	PC1	TRACE D0	-	-	-	-	SPI2_M OSI/I2S2 _SD	SAI1_SD _A	-	-	-	-	ETH_MD C	-	-	-	EVEN TOUT
	PC2	-	-	-	-	-	SPI2_MI SO	-	-	-	-	OTG_HS_ ULPI_DIR	ETH_MII_ TXD2	FMC_SD NE0	-	-	EVEN TOUT
	PC3	-	-	-	-	-	SPI2_M OSI/I2S2 _SD	-	-	-	-	OTG_HS_ ULPI_NX T	ETH_MII_ TX_CLK	FMC_SD CKE0	-	-	EVEN TOUT

Table 12. STM32F745xx and STM32F746xx alternate function mapping (continued)

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		SYS	TIM1/2	TIM3/4/5	TIM8/9/10/ 11/LPTIM 1/CEC	I2C1/2/3/ 4/CEC	SPI1/2/3/ 4/5/6	SPI3/ SAI1	SPI2/3/U SART1/2/ 3/UART5/ SPDIFRX	SAI2/US ART6/UA RT4/5/7/8 /SPDIFR X	CAN1/2/T IM12/13/ 14/QUAD SPI/LCD	SAI2/QU ADSPI/O TG2_HS/ OTG1_FS	ETH/ OTG1_FS	FMC/SD MMC1/O TG2_FS	DCMI	LCD	SYS
Port C	PC4	-	-	-	-	-	I2S1_M CK	-	-	SPDIFRX _IN2	-	-	ETH_MII_ RXD0/ET H_RMII_ RXD0	FMC_SD NE0	-	-	EVEN TOUT
	PC5	-	-	-	-	-	-	-	-	SPDIFRX _IN3	-	-	ETH_MII_ RXD1/ET H_RMII_ RXD1	FMC_SD CKE0	-	-	EVEN TOUT
	PC6	-	-	TIM3_C H1	TIM8_CH 1	-	I2S2_M CK	-	-	USART6 _TX	-	-	-	SDMMC 1_D6	DCMI_D 0	LCD_HS YNC	EVEN TOUT
	PC7	-	-	TIM3_C H2	TIM8_CH2	-	-	I2S3_M CK	-	USART6 _RX	-	-	-	SDMMC 1_D7	DCMI_D 1	LCD_G6	EVEN TOUT
	PC8	TRACE D1	-	TIM3_C H3	TIM8_CH3	-	-	-	UART5_ RTS	USART6 _CK	-	-	-	SDMMC 1_D0	DCMI_D 2	-	EVEN TOUT
	PC9	MCO2	-	TIM3_C H4	TIM8_CH4	I2C3_SD A	I2S_CK1 N	-	UART5_ CTS	-	QUADSP I_BK1_IO 0	-	-	SDMMC 1_D1	DCMI_D 3	-	EVEN TOUT
	PC10	-	-	-	-	-	-	SPI3_SC K/I2S3_ CK	USART3 _TX	UART4_ TX	QUADSP I_BK1_IO 1	-	-	SDMMC 1_D2	DCMI_D 8	LCD_R2	EVEN TOUT
	PC11	-	-	-	-	-	-	SPI3_MI SO	USART3 _RX	UART4_ RX	QUADSP I_BK2_N CS	-	-	SDMMC 1_D3	DCMI_D 4	-	EVEN TOUT
	PC12	TRACE D3	-	-	-	-	-	SPI3_M OS/I2S3_ _SD	USART3 _CK	UART5_ TX	-	-	-	SDMMC 1_CK	DCMI_D 9	-	EVEN TOUT
	PC13	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	EVEN TOUT
	PC14	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	EVEN TOUT
	PC15	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	EVEN TOUT



Table 12. STM32F745xx and STM32F746xx alternate function mapping (continued)

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		SYS	TIM1/2	TIM3/4/5	TIM8/9/10/ 11/LPTIM 1/CEC	I2C1/2/3/ 4/CEC	SPI1/2/3/ 4/5/6	SPI3/ SAI1	SPI2/3/U SART1/2/ 3/UART5/ SPDIFRX	SAI2/US ART6/UA RT4/5/7/8 /SPDIFR X	CAN1/2/T IM12/13/ 14/QUAD SPI/LCD	SAI2/QU ADSPI/O TG2_HS/ OTG1_FS	ETH/ OTG1_FS	FMC/SD MMC1/O TG2_FS	DCMI	LCD	SYS
Port D	PD0	-	-	-	-	-	-	-	-	-	CAN1_R X	-	-	FMC_D2	-	-	EVEN TOUT
	PD1	-	-	-	-	-	-	-	-	-	CAN1_T X	-	-	FMC_D3	-	-	EVEN TOUT
	PD2	TRACE D2	-	TIM3_ET R	-	-	-	-	-	UART5_ RX	-	-	-	SDMMC 1_CMD	DCMI_D 11	-	EVEN TOUT
	PD3	-	-	-	-	-	SPI2_SC K/I2S2_ CK	-	USART2 _CTS	-	-	-	-	FMC_CL K	DCMI_D 5	LCD_G7	EVEN TOUT
	PD4	-	-	-	-	-	-	-	USART2 _RTS	-	-	-	-	FMC_N OE	-	-	EVEN TOUT
	PD5	-	-	-	-	-	-	-	USART2 _TX	-	-	-	-	FMC_N WE	-	-	EVEN TOUT
	PD6	-	-	-	-	-	SPI3_M OSI/I2S3 _SD	SAI1_SD _A	USART2 _RX	-	-	-	-	FMC_N WAIT	DCMI_D 10	LCD_B2	EVEN TOUT
	PD7	-	-	-	-	-	-	-	USART2 _CK	SPDIFRX _IN0	-	-	-	FMC_NE 1	-	-	EVEN TOUT
	PD8	-	-	-	-	-	-	-	USART3 _TX	SPDIFRX _IN1	-	-	-	FMC_D1 3	-	-	EVEN TOUT
	PD9	-	-	-	-	-	-	-	USART3 _RX	-	-	-	-	FMC_D1 4	-	-	EVEN TOUT
	PD10	-	-	-	-	-	-	-	USART3 _CK	-	-	-	-	FMC_D1 5	-	LCD_B3	EVEN TOUT
	PD11	-	-	-	-	I2C4_SM BA	-	-	USART3 _CTS	-	QUADSP I_BK1_IO 0	SAI2_SD_ A	-	FMC_A1 6/FMC_ CLE	-	-	EVEN TOUT
	PD12	-	-	TIM4_C H1	LPTIM1_ N1	I2C4_SC L	-	-	USART3 _RTS	-	QUADSP I_BK1_IO 1	SAI2_FS_ A	-	FMC_A1 7/FMC_ ALE	-	-	EVEN TOUT
	PD13	-	-	TIM4_C H2	LPTIM1_ OUT	I2C4_SD A	-	-	-	-	QUADSP I_BK1_IO 3	SAI2_SC K_A	-	FMC_A1 8	-	-	EVEN TOUT

**Table 12. STM32F745xx and STM32F746xx alternate function mapping (continued)**

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		SYS	TIM1/2	TIM3/4/5	TIM8/9/10/11/LPTIM1/CEC	I2C1/2/3/4/CEC	SPI1/2/3/4/5/6	SPI3/SAI1	SPI2/3/UART1/2/3/UART5/SPDIFRX	SAI2/USART6/UART4/5/7/8/SPDIFRX	CAN1/2/TIM12/13/14/QUADSPI/LCD	SAI2/QUADSPI/TG2_HS/OTG1_FS	ETH/OTG1_FS	FMC/SDMMC1/OTG2_FS	DCMI	LCD	SYS
Port D	PD14	-	-	TIM4_C H3	-	-	-	-	-	UART8_ CTS	-	-	-	FMC_D0	-	-	EVEN TOUT
	PD15	-	-	TIM4_C H4	-	-	-	-	-	UART8_ RTS	-	-	-	FMC_D1	-	-	EVEN TOUT
Port E	PE0	-	-	TIM4_ET R	LPTIM1_E TR	-	-	-	-	UART8_ Rx	-	SAI2_MC K_A	-	FMC_NB L0	DCMI_D 2	-	EVEN TOUT
	PE1	-	-	-	LPTIM1_I N2	-	-	-	-	UART8_T x	-	-	-	FMC_NB L1	DCMI_D 3	-	EVEN TOUT
	PE2	TRACE CLK	-	-	-	-	SPI4_SC K	SAI1_M CLK_A	-	-	QUADSP I_BK1_IO 2	-	ETH_MII_ TXD3	FMC_A2 3	-	-	EVEN TOUT
	PE3	TRACE D0	-	-	-	-	-	SAI1_SD _B	-	-	-	-	-	FMC_A1 9	-	-	EVEN TOUT
	PE4	TRACE D1	-	-	-	-	SPI4_NS S	SAI1_FS _A	-	-	-	-	-	FMC_A2 0	DCMI_D 4	LCD_B0	EVEN TOUT
	PE5	TRACE D2	-	-	TIM9_CH 1	-	SPI4_MI SO	SAI1_SC K_A	-	-	-	-	-	FMC_A2 1	DCMI_D 6	LCD_G0	EVEN TOUT
	PE6	TRACE D3	TIM1_B KIN2	-	TIM9_CH 2	-	SPI4_M OSI	SAI1_SD _A	-	-	-	SAI2_MC K_B	-	FMC_A2 2	DCMI_D 7	LCD_G1	EVEN TOUT
	PE7	-	TIM1_ET R	-	-	-	-	-	-	UART7_ Rx	-	QUADSPI_ BK2_IO0	-	FMC_D4	-	-	EVEN TOUT
	PE8	-	TIM1_C H1N	-	-	-	-	-	-	UART7_T x	-	QUADSPI_ BK2_IO1	-	FMC_D5	-	-	EVEN TOUT
	PE9	-	TIM1_C H1	-	-	-	-	-	-	UART7_ RTS	-	QUADSPI_ BK2_IO2	-	FMC_D6	-	-	EVEN TOUT
	PE10	-	TIM1_C H2N	-	-	-	-	-	-	UART7_ CTS	-	QUADSPI_ BK2_IO3	-	FMC_D7	-	-	EVEN TOUT
	PE11	-	TIM1_C H2	-	-	-	SPI4_NS S	-	-	-	-	SAI2_SD_ B	-	FMC_D8	-	LCD_G3	EVEN TOUT
	PE12	-	TIM1_C H3N	-	-	-	SPI4_SC K	-	-	-	-	SAI2_SC K_B	-	FMC_D9	-	LCD_B4	EVEN TOUT
	PE13	-	TIM1_C H3	-	-	-	SPI4_MI SO	-	-	-	-	SAI2_FS_ B	-	FMC_D1 0	-	LCD_DE	EVEN TOUT



Table 12. STM32F745xx and STM32F746xx alternate function mapping (continued)

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		SYS	TIM1/2	TIM3/4/5	TIM8/9/10/ 11/LPTIM 1/CEC	I2C1/2/3/ 4/CEC	SPI1/2/3/ 4/5/6	SPI3/ SAI1	SPI2/3/U SART1/2/ 3/UART5/ SPDIFRX	SAI2/US ART6/UA RT4/5/7/8 /SPDIFR X	CAN1/2/T IM12/13/ 14/QUAD SPI/LCD	SAI2/QU ADSPI/O TG2_HS/ OTG1_FS	ETH/ OTG1_FS	FMC/SD MMC1/O TG2_FS	DCMI	LCD	SYS
Port E	PE14	-	TIM1_C H4	-	-	-	SPI4_M OSI	-	-	-	-	SAI2_MC K_B	-	FMC_D1 1	-	LCD_CL K	EVEN TOUT
	PE15	-	TIM1_B KIN	-	-	-	-	-	-	-	-	-	-	FMC_D1 2	-	LCD_R7	EVEN TOUT
Port F	PF0	-	-	-	-	I2C2_SD A	-	-	-	-	-	-	-	FMC_A0	-	-	EVEN TOUT
	PF1	-	-	-	-	I2C2_SC L	-	-	-	-	-	-	-	FMC_A1	-	-	EVEN TOUT
	PF2	-	-	-	-	I2C2_SM BA	-	-	-	-	-	-	-	FMC_A2	-	-	EVEN TOUT
	PF3	-	-	-	-	-	-	-	-	-	-	-	-	FMC_A3	-	-	EVEN TOUT
	PF4	-	-	-	-	-	-	-	-	-	-	-	-	FMC_A4	-	-	EVEN TOUT
	PF5	-	-	-	-	-	-	-	-	-	-	-	-	FMC_A5	-	-	EVEN TOUT
	PF6	-	-	-	TIM10_C H1	-	SPI5_NS S	SAI1_SD _B	-	UART7_ Rx	QUADSP I_BK1_IO 3	-	-	-	-	-	EVEN TOUT
	PF7	-	-	-	TIM11_CH 1	-	SPI5_SC K	SAI1_M CLK_B	-	UART7_T x	QUADSP I_BK1_IO 2	-	-	-	-	-	EVEN TOUT
	PF8	-	-	-	-	-	SPI5_MI SO	SAI1_SC K_B	-	UART7_ RTS	TIM13_C H1	QUADSPI _BK1_IO0	-	-	-	-	EVEN TOUT
	PF9	-	-	-	-	-	SPI5_M OSI	SAI1_FS _B	-	UART7_ CTS	TIM14_C H1	QUADSPI _BK1_IO1	-	-	-	-	EVEN TOUT
	PF10	-	-	-	-	-	-	-	-	-	-	-	-	-	DCMI_D 11	LCD_DE	EVEN TOUT
	PF11	-	-	-	-	-	SPI5_M OSI	-	-	-	-	SAI2_SD_ B	-	FMC_SD NRAS	DCMI_D 12	-	EVEN TOUT
	PF12	-	-	-	-	-	-	-	-	-	-	-	-	FMC_A6	-	-	EVEN TOUT

Table 12. STM32F745xx and STM32F746xx alternate function mapping (continued)

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		SYS	TIM1/2	TIM3/4/5	TIM8/9/10/ 11/LPTIM 1/CEC	I2C1/2/3/ 4/CEC	SPI1/2/3/ 4/5/6	SPI3/ SAI1	SPI2/3/U SART1/2/ 3/UART5/ SPDIFRX	SAI2/US ART6/UA RT4/5/7/8 /SPDIFR X	CAN1/2/T IM12/13/ 14/QUAD SPI/LCD	SAI2/QU ADSPI/O TG2_HS/ OTG1_FS	ETH/ OTG1_FS	FMC/SD MMC1/O TG2_FS	DCMI	LCD	SYS
Port F	PF13	-	-	-	-	I2C4_SM BA	-	-	-	-	-	-	-	FMC_A7	-	-	EVEN TOUT
	PF14	-	-	-	-	I2C4_SC L	-	-	-	-	-	-	-	FMC_A8	-	-	EVEN TOUT
	PF15	-	-	-	-	I2C4_SD A	-	-	-	-	-	-	-	FMC_A9	-	-	EVEN TOUT
Port G	PG0	-	-	-	-	-	-	-	-	-	-	-	-	FMC_A1 0	-	-	EVEN TOUT
	PG1	-	-	-	-	-	-	-	-	-	-	-	-	FMC_A1 1	-	-	EVEN TOUT
	PG2	-	-	-	-	-	-	-	-	-	-	-	-	FMC_A1 2	-	-	EVEN TOUT
	PG3	-	-	-	-	-	-	-	-	-	-	-	-	FMC_A1 3	-	-	EVEN TOUT
	PG4	-	-	-	-	-	-	-	-	-	-	-	-	FMC_A1 4/FMC_ BA0	-	-	EVEN TOUT
	PG5	-	-	-	-	-	-	-	-	-	-	-	-	FMC_A1 5/FMC_ BA1	-	-	EVEN TOUT
	PG6	-	-	-	-	-	-	-	-	-	-	-	-	-	DCMI_D 12	LCD_R7	EVEN TOUT
	PG7	-	-	-	-	-	-	-	-	USART6 _CK	-	-	-	FMC_IN T	DCMI_D 13	LCD_CL K	EVEN TOUT
	PG8	-	-	-	-	-	SPI6_NS S	-	SPDIFRX _IN2	USART6 _RTS	-	-	ETH_PPS _OUT	FMC_SD CLK	-	-	EVEN TOUT
	PG9	-	-	-	-	-	-	-	SPDIFRX _IN3	USART6 _RX	QUADSP I_BK2_IO 2	SAI2_FS_ B	-	FMC_NE 2/FMC_ NCE	DCMI_V SYNC	-	EVEN TOUT
	PG10	-	-	-	-	-	-	-	-	-	LCD_G3	SAI2_SD_ B	-	FMC_NE 3	DCMI_D 2	LCD_B2	EVEN TOUT





Table 12. STM32F745xx and STM32F746xx alternate function mapping (continued)

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		SYS	TIM1/2	TIM3/4/5	TIM8/9/10/ 11/LPTIM 1/CEC	I2C1/2/3/ 4/CEC	SPI1/2/3/ 4/5/6	SPI3/ SAI1	SPI2/3/U SART1/2/ 3/UART5/ SPDIFRX	SAI2/US ART6/UA RT4/5/7/8 /SPDIFR X	CAN1/2/T IM12/13/ 14/QUAD SPI/LCD	SAI2/QU ADSPI/O TG2_HS/ OTG1_FS	ETH/ OTG1_FS	FMC/SD MMC1/O TG2_FS	DCMI	LCD	SYS
Port G	PG11	-	-	-	-	-	-	-	SPDIFRX _IN0	-	-	-	ETH_MII_ TX_EN/E TH_RMII_ TX_EN	-	DCMI_D 3	LCD_B3	EVEN TOUT
	PG12	-	-	-	LPTIM1_I N1	-	SPI6_MI SO	-	SPDIFRX _IN1	USART6 _RTS	LCD_B4	-	-	FMC_NE 4	-	LCD_B1	EVEN TOUT
	PG13	TRACE D0	-	-	LPTIM1_ OUT	-	SPI6_SC K	-	-	USART6 _CTS	-	-	ETH_MII_ TXD0/ET H_RMII_T XD0	FMC_A2 4	-	LCD_R0	EVEN TOUT
	PG14	TRACE D1	-	-	LPTIM1_E TR	-	SPI6_M OSI	-	-	USART6 _TX	QUADSP I_BK2_IO 3	-	ETH_MII_ TXD1/ET H_RMII_T XD1	FMC_A2 5	-	LCD_B0	EVEN TOUT
	PG15	-	-	-	-	-	-	-	-	USART6 _CTS	-	-	-	FMC_SD NCAS	DCMI_D 13	-	EVEN TOUT
Port H	PH0	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	EVEN TOUT
	PH1	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	EVEN TOUT
	PH2	-	-	-	LPTIM1_I N2	-	-	-	-	-	QUADSP I_BK2_IO 0	SAI2_SC K_B	ETH_MII_ CRS	FMC_SD CKE0	-	LCD_R0	EVEN TOUT
	PH3	-	-	-	-	-	-	-	-	-	QUADSP I_BK2_IO 1	SAI2_MC K_B	ETH_MII_ COL	FMC_SD NE0	-	LCD_R1	EVEN TOUT
	PH4	-	-	-	-	I2C2_SC L	-	-	-	-	-	OTG_HS_ ULPI_NX T	-	-	-	-	EVEN TOUT
	PH5	-	-	-	-	I2C2_SD A	SPI5_NS S	-	-	-	-	-	-	FMC_SD NWE	-	-	EVEN TOUT
	PH6	-	-	-	-	I2C2_SM BA	SPI5_SC K	-	-	-	TIM12_C H1	-	ETH_MII_ RXD2	FMC_SD NE1	DCMI_D 8	-	EVEN TOUT
	PH7	-	-	-	-	I2C3_SC L	SPI5_MI SO	-	-	-	-	-	ETH_MII_ RXD3	FMC_SD CKE1	DCMI_D 9	-	EVEN TOUT

Table 12. STM32F745xx and STM32F746xx alternate function mapping (continued)

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		SYS	TIM1/2	TIM3/4/5	TIM8/9/10/ 11/LPTIM 1/CEC	I2C1/2/3/ 4/CEC	SPI1/2/3/ 4/5/6	SPI3/ SAI1	SPI2/3/U SART1/2/ 3/UART5/ SPDIFRX	SAI2/US ART6/UA RT4/5/7/8 /SPDIFR X	CAN1/2/T IM12/13/ 14/QUAD SPI/LCD	SAI2/QU ADSPI/O TG2_HS/ OTG1_FS	ETH/ OTG1_FS	FMC/SD MMC1/O TG2_FS	DCMI	LCD	SYS
Port H	PH8	-	-	-	-	I2C3_SD A	-	-	-	-	-	-	-	FMC_D1 6	DCMI_H SYNC	LCD_R2	EVEN TOUT
	PH9	-	-	-	-	I2C3_SM BA	-	-	-	-	TIM12_C H2	-	-	FMC_D1 7	DCMI_D 0	LCD_R3	EVEN TOUT
	PH10	-	-	TIM5_C H1	-	I2C4_SM BA	-	-	-	-	-	-	-	FMC_D1 8	DCMI_D 1	LCD_R4	EVEN TOUT
	PH11	-	-	TIM5_C H2	-	I2C4_SC L	-	-	-	-	-	-	-	FMC_D1 9	DCMI_D 2	LCD_R5	EVEN TOUT
	PH12	-	-	TIM5_C H3	-	I2C4_SD A	-	-	-	-	-	-	-	FMC_D2 0	DCMI_D 3	LCD_R6	EVEN TOUT
	PH13	-	-	-	TIM8_CH 1N	-	-	-	-	-	CAN1_T X	-	-	FMC_D2 1	-	LCD_G2	EVEN TOUT
	PH14	-	-	-	TIM8_CH 2N	-	-	-	-	-	-	-	-	FMC_D2 2	DCMI_D 4	LCD_G3	EVEN TOUT
	PH15	-	-	-	TIM8_CH 3N	-	-	-	-	-	-	-	-	FMC_D2 3	DCMI_D 11	LCD_G4	EVEN TOUT
Port I	PI0	-	-	TIM5_C H4	-	-	SPI2_NS S/I2S2_ WS	-	-	-	-	-	-	FMC_D2 4	DCMI_D 13	LCD_G5	EVEN TOUT
	PI1	-	-	-	TIM8_BKI N2	-	SPI2_SC K/I2S2_ CK	-	-	-	-	-	-	FMC_D2 5	DCMI_D 8	LCD_G6	EVEN TOUT
	PI2	-	-	-	TIM8_CH 4	-	SPI2_MI SO	-	-	-	-	-	-	FMC_D2 6	DCMI_D 9	LCD_G7	EVEN TOUT
	PI3	-	-	-	TIM8_ET R	-	SPI2_M OSI/I2S2_ _SD	-	-	-	-	-	-	FMC_D2 7	DCMI_D 10	-	EVEN TOUT
	PI4	-	-	-	TIM8_BKI N	-	-	-	-	-	-	SAI2_MC K_A	-	FMC_NB L2	DCMI_D 5	LCD_B4	EVEN TOUT
	PI5	-	-	-	TIM8_CH 1	-	-	-	-	-	-	SAI2_SC K_A	-	FMC_NB L3	DCMI_V SYNC	LCD_B5	EVEN TOUT
	PI6	-	-	-	TIM8_CH 2	-	-	-	-	-	-	SAI2_SD_ A	-	FMC_D2 8	DCMI_D 6	LCD_B6	EVEN TOUT



Table 12. STM32F745xx and STM32F746xx alternate function mapping (continued)

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		SYS	TIM1/2	TIM3/4/5	TIM8/9/10/ 11/LPTIM 1/CEC	I2C1/2/3/ 4/CEC	SPI1/2/3/ 4/5/6	SPI3/ SAI1	SPI2/3/U SART1/2/ 3/UART5/ SPDIFRX	SAI2/US ART6/UA RT4/5/7/8 /SPDIFR X	CAN1/2/T IM12/13/ 14/QUAD SPI/LCD	SAI2/QU ADSPI/O TG2_HS/ OTG1_FS	ETH/ OTG1_FS	FMC/SD MMC1/O TG2_FS	DCMI	LCD	SYS
Port I	PI7	-	-	-	TIM8_CH 3	-	-	-	-	-	-	SAI2_FS_ A	-	FMC_D2 9	DCMI_D 7	LCD_B7	EVEN TOUT
	PI8	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	EVEN TOUT
	PI9	-	-	-	-	-	-	-	-	-	CAN1_R X	-	-	FMC_D3 0	-	LCD_VS YNC	EVEN TOUT
	PI10	-	-	-	-	-	-	-	-	-	-	-	ETH_MII_ RX_ER	FMC_D3 1	-	LCD_HS YNC	EVEN TOUT
	PI11	-	-	-	-	-	-	-	-	-	-	OTG_HS_ ULPI_DIR	-	-	-	-	EVEN TOUT
	PI12	-	-	-	-	-	-	-	-	-	-	-	-	-	-	LCD_HS YNC	EVEN TOUT
	PI13	-	-	-	-	-	-	-	-	-	-	-	-	-	-	LCD_VS YNC	EVEN TOUT
	PI14	-	-	-	-	-	-	-	-	-	-	-	-	-	-	LCD_CL K	EVEN TOUT
	PI15	-	-	-	-	-	-	-	-	-	-	-	-	-	-	LCD_R0	EVEN TOUT
Port J	PJ0	-	-	-	-	-	-	-	-	-	-	-	-	-	-	LCD_R1	EVEN TOUT
	PJ1	-	-	-	-	-	-	-	-	-	-	-	-	-	-	LCD_R2	EVEN TOUT
	PJ2	-	-	-	-	-	-	-	-	-	-	-	-	-	-	LCD_R3	EVEN TOUT
	PJ3	-	-	-	-	-	-	-	-	-	-	-	-	-	-	LCD_R4	EVEN TOUT
	PJ4	-	-	-	-	-	-	-	-	-	-	-	-	-	-	LCD_R5	EVEN TOUT
	PJ5	-	-	-	-	-	-	-	-	-	-	-	-	-	-	LCD_R6	EVEN TOUT
	PJ6	-	-	-	-	-	-	-	-	-	-	-	-	-	-	LCD_R7	EVEN TOUT

**Table 12. STM32F745xx and STM32F746xx alternate function mapping (continued)**

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		SYS	TIM1/2	TIM3/4/5	TIM8/9/10/ 11/LPTIM 1/CEC	I2C1/2/3/ 4/CEC	SPI1/2/3/ 4/5/6	SPI3/ SAI1	SPI2/3/U SART1/2/ 3/UART5/ SPDIFRX	SAI2/US ART6/UA RT4/5/7/8 /SPDIFR X	CAN1/2/T IM12/13/ 14/QUAD SPI/LCD	SAI2/QU ADSPI/O TG2_HS/ OTG1_FS	ETH/ OTG1_FS	FMC/SD MMC1/O TG2_FS	DCMI	LCD	SYS
Port J	PJ7	-	-	-	-	-	-	-	-	-	-	-	-	-	-	LCD_G0	EVEN TOUT
	PJ8	-	-	-	-	-	-	-	-	-	-	-	-	-	-	LCD_G1	EVEN TOUT
	PJ9	-	-	-	-	-	-	-	-	-	-	-	-	-	-	LCD_G2	EVEN TOUT
	PJ10	-	-	-	-	-	-	-	-	-	-	-	-	-	-	LCD_G3	EVEN TOUT
	PJ11	-	-	-	-	-	-	-	-	-	-	-	-	-	-	LCD_G4	EVEN TOUT
	PJ12	-	-	-	-	-	-	-	-	-	-	-	-	-	-	LCD_B0	EVEN TOUT
	PJ13	-	-	-	-	-	-	-	-	-	-	-	-	-	-	LCD_B1	EVEN TOUT
	PJ14	-	-	-	-	-	-	-	-	-	-	-	-	-	-	LCD_B2	EVEN TOUT
	PJ15	-	-	-	-	-	-	-	-	-	-	-	-	-	-	LCD_B3	EVEN TOUT



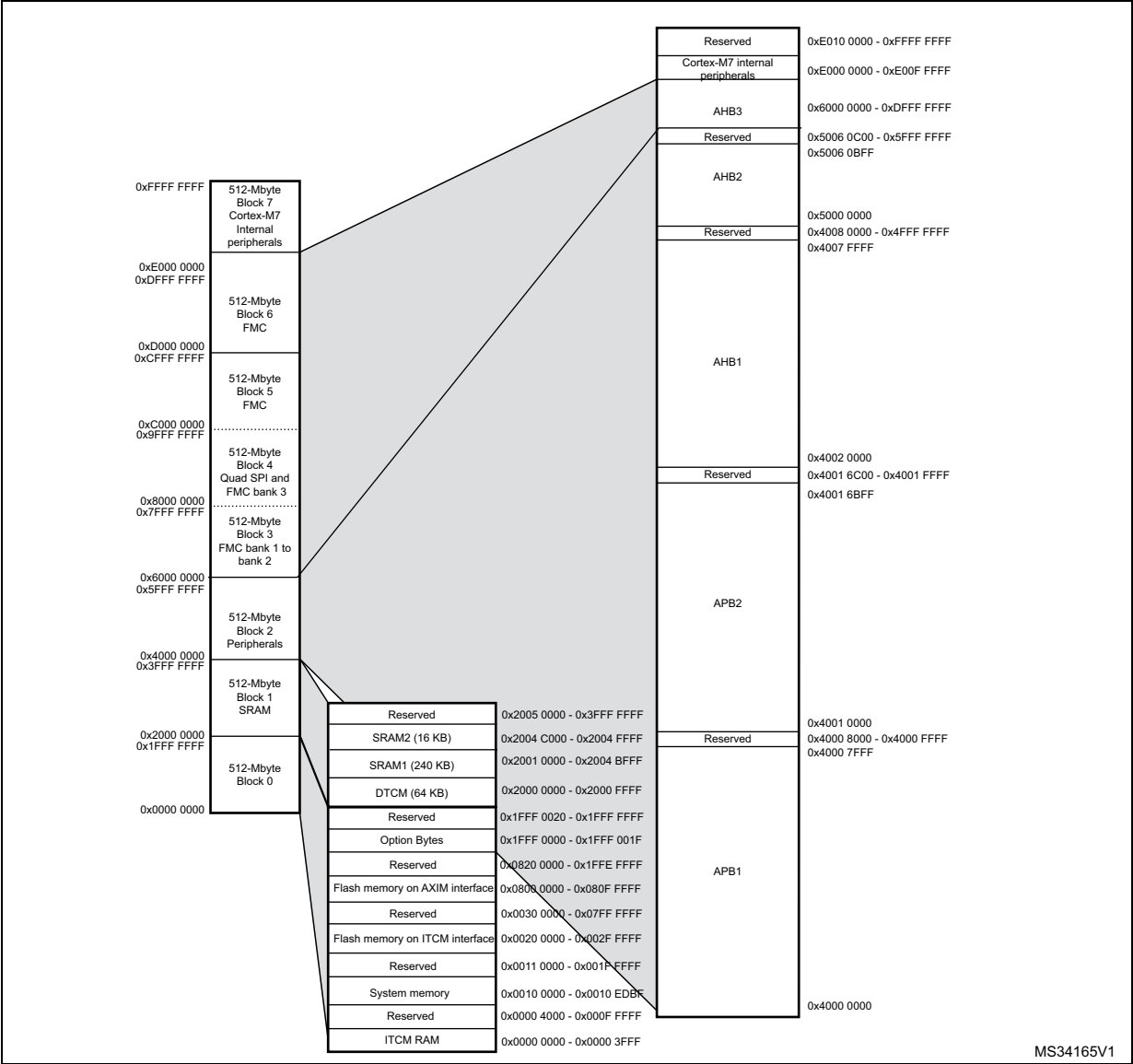
Table 12. STM32F745xx and STM32F746xx alternate function mapping (continued)

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		SYS	TIM1/2	TIM3/4/5	TIM8/9/10/ 11/LPTIM 1/CEC	I2C1/2/3/ 4/CEC	SPI1/2/3/ 4/5/6	SPI3/ SAI1	SPI2/3/U SART1/2/ 3/UART5/ SPDIFRX	SAI2/US ART6/UA RT4/5/7/8 /SPDIFR X	CAN1/2/T IM12/13/ 14/QUAD SPI/LCD	SAI2/QU ADSPI/O TG2_HS/ OTG1_FS	ETH/ OTG1_FS	FMC/SD MMC1/O TG2_FS	DCMI	LCD	SYS
Port K	PK0	-	-	-	-	-	-	-	-	-	-	-	-	-	-	LCD_G5	EVEN TOUT
	PK1	-	-	-	-	-	-	-	-	-	-	-	-	-	-	LCD_G6	EVEN TOUT
	PK2	-	-	-	-	-	-	-	-	-	-	-	-	-	-	LCD_G7	EVEN TOUT
	PK3	-	-	-	-	-	-	-	-	-	-	-	-	-	-	LCD_B4	EVEN TOUT
	PK4	-	-	-	-	-	-	-	-	-	-	-	-	-	-	LCD_B5	EVEN TOUT
	PK5	-	-	-	-	-	-	-	-	-	-	-	-	-	-	LCD_B6	EVEN TOUT
	PK6	-	-	-	-	-	-	-	-	-	-	-	-	-	-	LCD_B7	EVEN TOUT
	PK7	-	-	-	-	-	-	-	-	-	-	-	-	-	-	LCD_DE	EVEN TOUT

4 Memory mapping

The memory map is shown in [Figure 19](#).

Figure 19. Memory map



MS34165V1

Table 13. STM32F745xx and STM32F746xx register boundary addresses

Bus	Boundary address	Peripheral
	0xE00F FFFF - 0xFFFF FFFF	Reserved
Cortex-M7	0xE000 0000 - 0xE00F FFFF	Cortex-M7 internal peripherals
AHB3	0xD000 0000 - 0xDFFF FFFF	FMC bank 6
	0xC000 0000 - 0xCFFF FFFF	FMC bank 5
	0xA000 2000 - 0xBFFF FFFF	Reserved
	0xA000 1000 - 0xA000 1FFF	Quad-SPI control register
	0xA000 0000 - 0xA000 0FFF	FMC control register
	0x9000 0000 - 0x9FFF FFFF	Quad-SPI
	0x8000 0000 - 0x8FFF FFFF	FMC bank 3
	0x7000 0000 - 0x7FFF FFFF	FMC bank 2
	0x6000 0000 - 0x6FFF FFFF	FMC bank 1
	0x5006 0C00 - 0x5FFF FFFF	Reserved
AHB2	0x5006 0800 - 0x5006 0BFF	RNG
	0x5005 0400 - 0x5006 07FF	Reserved
	0x5005 0000 - 0x5005 03FF	DCMI
	0x5004 0000 - 0x5004 FFFF	Reserved
	0x5000 0000 - 0x5003 FFFF	USB OTG FS

Table 13. STM32F745xx and STM32F746xx register boundary addresses (continued)

Bus	Boundary address	Peripheral
	0x4008 0000 - 0x4FFF FFFF	Reserved
AHB1	0x4004 0000 - 0x4007 FFFF	USB OTG HS
	0x4002 BC00 - 0x4003 FFFF	Reserved
	0x4002 B000 - 0x4002 BBFF	Chrom-ART (DMA2D)
	0x4002 9400 - 0x4002 AFFF	Reserved
	0x4002 9000 - 0x4002 93FF	ETHERNET MAC
	0x4002 8C00 - 0x4002 8FFF	
	0x4002 8800 - 0x4002 8BFF	
	0x4002 8400 - 0x4002 87FF	
	0x4002 8000 - 0x4002 83FF	
	0x4002 6800 - 0x4002 7FFF	Reserved
	0x4002 6400 - 0x4002 67FF	DMA2
	0x4002 6000 - 0x4002 63FF	DMA1
	0x4002 5000 - 0x4002 5FFF	Reserved
	0x4002 4000 - 0x4002 4FFF	BKPSRAM
	0x4002 3C00 - 0x4002 3FFF	Flash interface register
	0x4002 3800 - 0x4002 3BFF	RCC
	0x4002 3400 - 0x4002 37FF	Reserved
	0x4002 3000 - 0x4002 33FF	CRC
	0x4002 2C00 - 0x4002 2FFF	Reserved
	0x4002 2800 - 0x4002 2BFF	GPIOK
	0x4002 2400 - 0x4002 27FF	GPIOJ
	0x4002 2000 - 0x4002 23FF	GPIOI
	0x4002 1C00 - 0x4002 1FFF	GPIOH
	0x4002 1800 - 0x4002 1BFF	GPIOG
	0x4002 1400 - 0x4002 17FF	GPIOF
	0x4002 1000 - 0x4002 13FF	GPIOE
	0x4002 0C00 - 0x4002 0FFF	GPIOD
	0x4002 0800 - 0x4002 0BFF	GPIOC
	0x4002 0400 - 0x4002 07FF	GPIOB
	0x4002 0000 - 0x4002 03FF	GPIOA



Table 13. STM32F745xx and STM32F746xx register boundary addresses (continued)

Bus	Boundary address	Peripheral
	0x4001 6C00 - 0x4001 FFFF	Reserved
APB2	0x4001 6800 - 0x4001 6BFF	LCD-TFT
	0x4001 6000 - 0x4001 67FF	Reserved
	0x4001 5C00 - 0x4001 5FFF	SAI2
	0x4001 5800 - 0x4001 5BFF	SAI1
	0x4001 5400 - 0x4001 57FF	SPI6
	0x4001 5000 - 0x4001 53FF	SPI5
	0x4001 4C00 - 0x4001 4FFF	Reserved
	0x4001 4800 - 0x4001 4BFF	TIM11
	0x4001 4400 - 0x4001 47FF	TIM10
	0x4001 4000 - 0x4001 43FF	TIM9
	0x4001 3C00 - 0x4001 3FFF	EXTI
	0x4001 3800 - 0x4001 3BFF	SYSCFG
	0x4001 3400 - 0x4001 37FF	SPI4
	0x4001 3000 - 0x4001 33FF	SPI1/I2S1
	0x4001 2C00 - 0x4001 2FFF	SDMMC
	0x4001 2400 - 0x4001 2BFF	Reserved
	0x4001 2000 - 0x4001 23FF	ADC1 - ADC2 - ADC3
	0x4001 1800 - 0x4001 1FFF	Reserved
	0x4001 1400 - 0x4001 17FF	USART6
	0x4001 1000 - 0x4001 13FF	USART1
	0x4001 0800 - 0x4001 0FFF	Reserved
	0x4001 0400 - 0x4001 07FF	TIM8
	0x4001 0000 - 0x4001 03FF	TIM1

Table 13. STM32F745xx and STM32F746xx register boundary addresses (continued)

Bus	Boundary address	Peripheral
	0x4000 8000 - 0x4000 FFFF	Reserved
APB1	0x4000 7C00 - 0x4000 7FFF	UART8
	0x4000 7800 - 0x4000 7BFF	UART7
	0x4000 7400 - 0x4000 77FF	DAC
	0x4000 7000 - 0x4000 73FF	PWR
	0x4000 6C00 - 0x4000 6FFF	HDMI-CEC
	0x4000 6800 - 0x4000 6BFF	CAN2
	0x4000 6400 - 0x4000 67FF	CAN1
	0x4000 6000 - 0x4000 63FF	I2C4
	0x4000 5C00 - 0x4000 5FFF	I2C3
	0x4000 5800 - 0x4000 5BFF	I2C2
	0x4000 5400 - 0x4000 57FF	I2C1
	0x4000 5000 - 0x4000 53FF	UART5
	0x4000 4C00 - 0x4000 4FFF	UART4
	0x4000 4800 - 0x4000 4BFF	USART3
	0x4000 4400 - 0x4000 47FF	USART2
	0x4000 4000 - 0x4000 43FF	SPDIFRX
	0x4000 3C00 - 0x4000 3FFF	SPI3 / I2S3
	0x4000 3800 - 0x4000 3BFF	SPI2 / I2S2
	0x4000 3400 - 0x4000 37FF	Reserved
	0x4000 3000 - 0x4000 33FF	IWDG
	0x4000 2C00 - 0x4000 2FFF	WWDG
	0x4000 2800 - 0x4000 2BFF	RTC & BKP Registers
	0x4000 2400 - 0x4000 27FF	LPTIM1
	0x4000 2000 - 0x4000 23FF	TIM14
	0x4000 1C00 - 0x4000 1FFF	TIM13
	0x4000 1800 - 0x4000 1BFF	TIM12
	0x4000 1400 - 0x4000 17FF	TIM7
	0x4000 1000 - 0x4000 13FF	TIM6
	0x4000 0C00 - 0x4000 0FFF	TIM5
	0x4000 0800 - 0x4000 0BFF	TIM4
	0x4000 0400 - 0x4000 07FF	TIM3
	0x4000 0000 - 0x4000 03FF	TIM2