

Table 10. STM32F745xx and STM32F746xx pin and ball definition (continued)

Pin Number								Pin name (function after reset) ⁽¹⁾	Pin type	I/O structure	Notes	Alternate functions	Additional functions
LQFP100	TFBGA100	WLCSP143	LQFP144	UFBGA176	LQFP176	LQFP208	TFBGA216						
-	-	-	-	G4	44	47	J4	PH3	I/O	FT	-	QUADSPI_BK2_IO1, SAI2_MCK_B, ETH_MII_COL, FMC_SDNE0, LCD_R1, EVENTOUT	-
-	-	-	-	H4	45	48	H4	PH4	I/O	FT	-	I2C2_SCL, OTG_HS_ULPI_NXT, EVENTOUT	-
-	-	-	-	J4	46	49	J3	PH5	I/O	FT	-	I2C2_SDA, SPI5_NSS, FMC_SDNWE, EVENTOUT	-
25	K2	M11	37	R2	47	50	R2	PA3	I/O	FT	(4)	TIM2_CH4, TIM5_CH4, TIM9_CH2, USART2_RX, OTG_HS_ULPI_D0, ETH_MII_COL, LCD_B5, EVENTOUT	ADC123_IN3
26	J1	-	38	-	-	51	K6	VSS	S	-	-	-	-
-	E6	N11	-	L4	48	-	L5	BYPASS_REG	I	FT	-	-	-
27	K1	J8	39	K4	49	52	K5	VDD	S	-	-	-	-
28	G3	M10	40	N4	50	53	N4	PA4	I/O	TTa	(4)	SPI1_NSS/I2S1_WS, SPI3_NSS/I2S3_WS, USART2_CK, OTG_HS_SOF, DCMI_HSYNC, LCD_VSYNC, EVENTOUT	ADC12_IN4, DAC_OUT1
29	H3	M9	41	P4	51	54	P4	PA5	I/O	TTa	(4)	TIM2_CH1/TIM2_ETR, TIM8_CH1N, SPI1_SCK/I2S1_CK, OTG_HS_ULPI_CK, LCD_R4, EVENTOUT	ADC12_IN5, DAC_OUT2
30	J3	N10	42	P3	52	55	P3	PA6	I/O	FT	(4)	TIM1_BKIN, TIM3_CH1, TIM8_BKIN, SPI1_MISO, TIM13_CH1, DCMI_PIXCLK, LCD_G2, EVENTOUT	ADC12_IN6