Peripheral clock enabl LSI LPTimer clock Peripheral clock enab LSE HSI USART clocks SYSCLK Peripheral **PCLKx** clock enable ► I2C clocks LSLRC Watchdog 32 kHz enable RTCSEL[1:0] To Independent watchdog RTC OSC32_IN LSE OSC RTCCLK enable ►To RTC 32.768 kHz Peripheral OSC32 OUT clock enable PLL48CLK SYSCLK ► SDMMC clock PLLI2S ___/1 to 5 ◀ HSE_RTC LSE. /2 to 31 ► HDMI-CEC clock Peripheral ► Ethernet PTP clock /488 Clock enable **HCLK** ▶ to AHB bus, core, 216 MHz max 16 MHz HSI RC HSI memory and DMA /8 SW to Cortex System timer HSI FCLK Cortex HSE AHB free-running clock PRESC PLLCLK /1,2,..512 Peripheral SYSCLK clock enable OSC_OUT [HSE 216 MHz 4-26 MHz APBx PRESC /1,2,4,8,16 ► APBx peripheral clocks HSE OSC Periphera OSC IN clock enable if (APBx presc ► APBx timer clocks 1x1 else x2 Peripheral clock enable PLLQ /Q χN PLL48CLI USB & RNG Clock Peripheral SPDIF-Rx Clock lvco Periphera /Q xΝ clock enable PLLI2SR I2S Clock PLLI2S Periphera I2S_CKIN clock enable PLLI2SQ DIV SAI1 clock Peripheral clock enable PLLSAIP SAI2 clock PLLSAIC DIV Periphera /Q χN clock enable LCD-TFT clock /R DIV PLLSAI Peripheral ETH_MII_TX_CLK_MII clock enable MACTXCLK PHY Etherne 25 to 50 MHz MII_RMII_SEL in SYSCFG_PMC to Ethernet MAC **▶** /2.20 Peripheral clock enable ► MACRXCLK ETH MII RX CLK MI Peripheral ► MACRMIICLK clock enable Periphera USBHS clock enable USB2 0 PHY OTG_HS_ULPI_CK ULPI clock 24 to 60 MHz MSv35914V2

Figure 13. Clock tree

- For full details about the internal and external clock source characteristics, refer to the Electrical characteristics section in the device datasheet.
- When TIMPRE bit of the RCC_DCKCFGR1 register is reset, if APBx prescaler is 1, then TIMxCLK = PCLKx, otherwise TIMxCLK = 2x PCLKx.
- 3. When TIMPRE bit in the RCC_DCKCFGR1 register is set, if APBx prescaler is 1,2 or 4, then TIMxCLK = HCLK, otherwise TIMxCLK = 4x PCLKx.

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