Register Description	Address	Notes
Read Control Register	Base + 0x0000	Bit 0 → Read enable
		Bit 1 → Output register clock enable
		Bit 2 → Output register reset
		Bit 3 → Sleep Mode
Read Data Register	Base + 0x0004	Bits 31 downto Bit 0 (Data output of FIFO)
Write Control Register	Base + 0x0008	Bit 0 → Write enable
Write Data Register	Base + 0x000C	Bits 31 downto Bit 0 (Data input of FIFO)
FIFO Status Register	Base + 0x0010	Bit 0 → FIFO Empty
		Bit 1 → FIFO Full
		Bit 2 → Programmable empty
		Bit 3 → Programmable full
		Bit 4 → Read error
		Bit 5 → Read Reset busy
		Bit 6 → Write error
		Bit 7 → Write Reset busy