

Register Description	Address	Notes
Read Data Register	Base + 0x0000	Bits 31 downto Bit 0 (Data output of FIFO)
Write Data Register	Base + 0x0004	Bits 31 downto Bit 0 (Data input of FIFO)
FIFO Status Register	Base + 0x0008	Bit 0 → FIFO Empty
		Bit 1 → FIFO Full
		Bit 2 → Programmable empty
		Bit 3 → Programmable full
		Bit 4 → Read error
		Bit 5 → Read Reset busy
		Bit 6 → Write error
		Bit 7 → Write Reset busy