ECE506 - Project 2 - Stevan Dupor - smdupor@ncsu.edu - id: 000211897
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ABSTRACT: This project explored the implementation and performance of MSI, MESI, and Dragon cache-coherence protocols for symmetric multiprocessor systems of fixed quantity of processors. Experiments across varying private cache sizes, associativity, and blocksize were performed, and an analysis of the performance statistics is presented within.

Introduction

The cache simulator was implemented with MSI (Modified-Shared-Invalid), MESI (Modified-Exclusive-Shared-Invalid), and Dragon (non-invalidation-based) coherence protocols. The MSI protocol stipulates that multiple caches can contain "S" shared data, but the Modified state exists in an "exclusive" state. When a write is received to a shared cache, MSI stipulates such that all shared cachelines should be invalidated except for the line being written to; this line will transition to the "M" modified state. Then, when the cacheline is re-shared, the M line is flushed back to memory.

For the MESI protocol, an new state is introduced where an "E" exclusive cacheline is transitioned into on an initial read, where no other caches hold that cache line. The "E" state does not contain "dirty" data, so a write to this line will present an "intervention" and transition into the "M" state. In a similar fashion, an "E" state line will transition into "S" state when another read is received from another cacheline. When a set of lines in "S" receive a write request, all lines are invalidated except for the cacheline to be written, which is transitioned into the "M" state.

Finally, the Dragon protocol uses updates rather than invalidations to manage shared data. Two new states are introduced "Shared Clean" and "Shared Modified" both of which may contain Dirty cache lines, which can be shared between processors when new blocks are brought into the one of the shared states via reads or writes. In turn, the "SM" state cacheline is responsible for writing back dirty data to main memory, with "SC" lines being permitted to silent evict dirty cachelines.

Methods

Three series of experiments were performed with the SMP Cache simulator, with each series being performed for each protocol in turn. All series of experiments utilized a fixed quantity of processors in the simulated architecture: four cores, each with a single L1 private cache and shared main memory. A Comma-Separated-Value data collection module was implemented within the simulator code, to collect all statistics from each processor core in an easily processed flatfile. A Python script was used to deploy calls to the SMP simulator for each experiment, and to process the resultant data from each experiment.

As each datapoint of the experiments affected the processors symmetrically, the data are presented in aggregate form in the results section; however, data for each processor was collected and the complete raw dataset is available in the appendix of this document.

Results Overview & Tabular Statistics

The experiment result statistics are displayed in tabular numeric form below as a simple aggregate across all statistics. In later sections, results and discussion will be presented as in plot form and discussed. These will be separated into two sections: **exploration of memory hierarchy statistics** (eg, Miss rate, Memory Traffic) which are only loosely coupled with coherence protocol, and **cache-cache transactions** (eg, Invalidations) which are directly coupled with coherence protocol.

Author's Note: Project requirements stipulate that these experiments shall only be run on a fixed quantity of four processors. As such, ***the true scalability of any coherence protocol cannot be directly measured by these methods*** *– as the number of cores is a critical independent variable in any coherence protocol performance calculation. Unfortunately, statistics like memory traffic only paint a partial picture of the coherence performance as changes in associativity, cache size, and so on will directly affect miss rate (by introducing/eliminating conflict or capacity misses). As such, I will infer as much information as possible, given the constraints of these experiments.*

In the following sections, the **AGGREGATE STATISTICS** from all caches combined are presented. Miss Rate is presented as the arithmetic mean across all caches in the system. Please note that **Miss Rate is intentionally calculated and displayed** to a high precision level (10^{-6}) as it is a mean and lower precision sacrifices the presence of data trends. All other statistics are a simple sum across all caches. **Reminder: Raw data for individual caches is included in the Appendix to this report.**

Tabular Results: Varying Cache Size

Size (Bytes)	Reads	Read Misses	Writes	Write Misses	Miss Rate	Write Backs	Cache-Cache Transfers	Memory Traffic	Interventions	Invalidations	Flushes	BusRdX
MSI Protocol												
262144	451857	23164	48143	161	4.6675%	1001	0	27020	259	8076	413	2855
524288	451857	23101	48143	161	4.6525%	736	0	26692	263	8076	417	2855
1048576	451857	23075	48143	161	4.6475%	668	0	26598	265	8076	419	2855
2097152	451857	23069	48143	161	4.6475%	637	0	26561	265	8076	419	2855
MESI Protocol												
262144	451857	23164	48143	161	4.6675%	1001	17663	6663	5848	8076	413	161
524288	451857	23101	48143	161	4.6525%	736	17619	6379	5834	8076	417	161
1048576	451857	23075	48143	161	4.6475%	668	17599	6305	5830	8076	419	161
2097152	451857	23069	48143	161	4.6475%	637	17593	6274	5830	8076	419	161
Dragon Protocol												
262144	451857	22577	48143	7	4.5150%	935	0	23519	5628	0	27	0
524288	451857	22438	48143	7	4.4900%	531	0	22976	5595	0	24	0
1048576	451857	22414	48143	7	4.4825%	445	0	22866	5589	0	24	0
2097152	451857	22403	48143	7	4.4825%	426	0	22836	5586	0	24	0

Table 1: Aggregate Statistics for Varying Cache Sizes Across 4 Caches

Tabular Results: Varying Associativity

Associativity (Ways)	Reads	Read Misses	Writes	Write Misses	Miss Rate	Write Backs	Cache-Cache Transfers	Memory Traffic	Interventions	Invalidations	Flushes	BusRdX
MSI Protocol												
4	451857	23130	48143	161	4.6575%	913	0	26898	260	8076	414	2855
8	451857	23075	48143	161	4.6475%	668	0	26598	265	8076	419	2855
16	451857	23034	48143	161	4.6400%	449	0	26338	266	8076	420	2855
MESI Protocol												
4	451857	23130	48143	161	4.6575%	913	17638	6566	5841	8076	414	161
8	451857	23075	48143	161	4.6475%	668	17599	6305	5830	8076	419	161
16	451857	23034	48143	161	4.6400%	449	17566	6078	5823	8076	420	161
Dragon Protocol												
4	451857	22473	48143	7	4.4950%	597	0	23077	5604	0	24	0
8	451857	22414	48143	7	4.4825%	445	0	22866	5589	0	24	0
16	451857	22341	48143	7	4.4725%	209	0	22557	5571	0	24	0

Table 2: Aggregate Statistics for Varying Associativity Across 4 Caches

Tabular Results: Varying Block Size

Block Size (Bytes)	Reads	Read Misses	Writes	Write Misses	Miss Rate	Write Backs	Cache-Cache Transfers	Memory Traffic	Interventions	Invalidations	Flushes	BusRdX
MSI Protocol												
64	451857	23075	48143	161	4.6475%	668	0	26598	265	8076	419	2855
128	451857	21451	48143	160	4.3250%	1077	0	25446	440	8276	594	2918
256	451857	20181	48143	160	4.0675%	1420	0	24610	636	8544	790	3009
MESI Protocol												
64	451857	23075	48143	161	4.6475%	668	17599	6305	5830	8076	419	161
128	451857	21451	48143	160	4.3250%	1077	16519	6169	5466	8276	594	160
256	451857	20181	48143	160	4.0675%	1420	15723	6038	5197	8544	790	160
Dragon Protocol												
64	451857	22414	48143	7	4.4825%	445	0	22866	5589	0	24	0
128	451857	20315	48143	6	4.0650%	599	0	20920	5066	0	27	0
256	451857	18531	48143	6	3.7100%	779	0	19316	4619	0	32	0

Table 3: Aggregate Statistics for Varying Block Size Across 4 Caches

In the proceeding sections, I will present plots that better illustrate these results, discuss trends, and form conclusions.

Results: Memory Hierarchy Transactions

Varying Cache Size: Read and Write Misses, Miss Rate

The following figures detail the effects of varying L1 private cache sizes (symmetric private caches) from 256KiB to 2MiB on Misses in the cache. Notably, Write Misses are unaffected by varying cache size (as there appear to be no capacity misses at any of the sizes explored in these experiments. A similar trend (resulting from read misses) is observed in the global average miss rate. **Two coherence-related trends appear:** One, MSI and MESI present identical miss rates, as a result of protocol invalidations. And two, Dragon presents a lower overall miss rate at all cache sizes as a result of Dragon being an update-based protocol instead of invalidation-based. As such, invalidations do not happen, which reduces "unneccessary" later cache misses due to invalid cache lines.

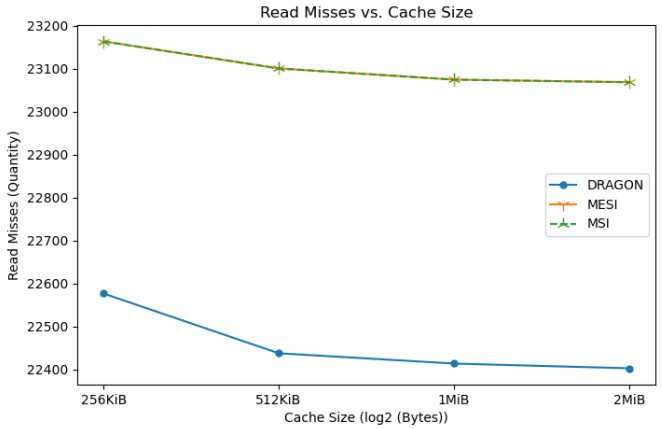

Figure 1: Aggregate Read Misses vs Cache Size

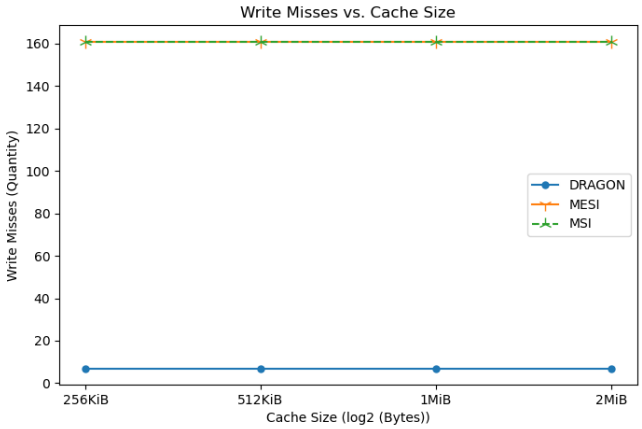

Figure 2: Aggregate Write Misses vs Cache Size

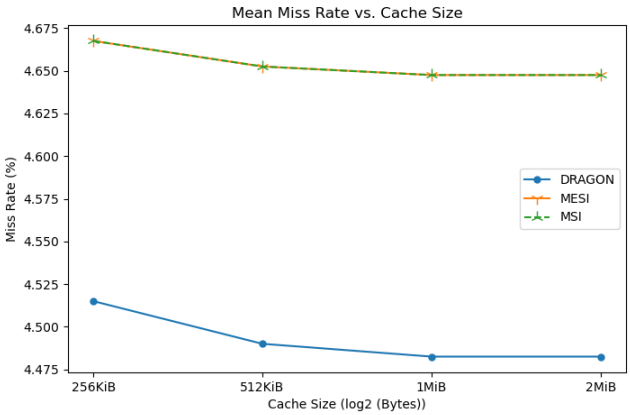

Figure 3: Aggregate Miss Rate vs Cache Size

Varying Associativity: Read and Write Misses, Miss Rate

The following figures detail the effects of varying L1 private cache Associativity (symmetric private caches) from 4 ways to 16 ways, on Misses in the cache. In these plots, there are some similarities to the Cache Size experiments: Dragon presents fewer overall misses for all configurations due to zero coherence invalidations being performed. Also, I note that Write Misses are again unaffected by the associativity, which indicates no Conflict-based write misses in the experiment trace for any associativity. Finally, I observe generally improving (Symmetrically across all protocols) miss rate which indicates that the effect of increasing associativity, w.r.t. miss rate, only resolves cache line conflicts that would be present in a single-core-single-cache architecture – this trend does not present any new information on the coherence protocol performance.

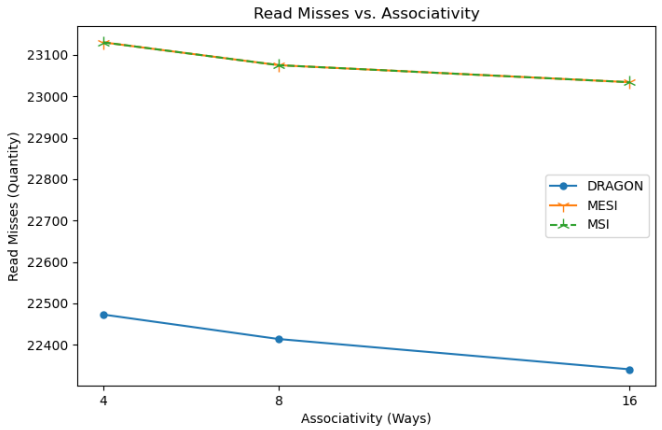

Figure 4: Aggregate Read Misses vs Associativity

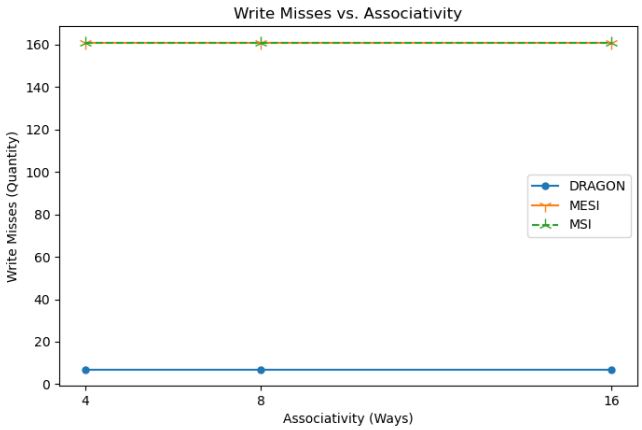

Figure 5: Aggregate Write Misses vs Associativity

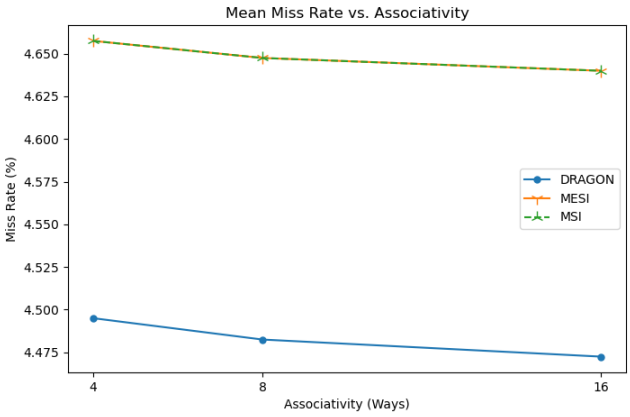

Figure 6: Aggregate Miss Rate vs Associativity

Varying Block Size: Read and Write Misses, Miss Rate

The following figures detail the effects of varying L1 private cache Block Size (symmetric private caches) from 4 ways to 16 ways, on Misses in the cache. In these plots, I again observe that MSI and MESI present identical performance due to the invalidation-basis of these protocols, with dragon performing better overall for all block sizes. Notably, as block size increases, the overall miss rate falls – particularly for Dragon protocol, which takes better advantage of the spatial locality of recently-used data.

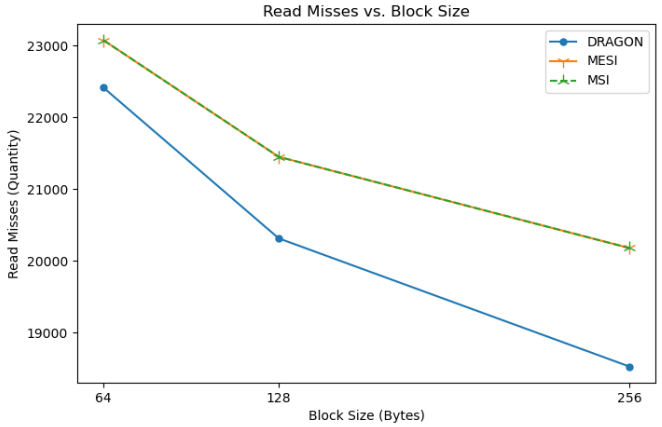

Figure 7: Aggregate Read Misses vs Block Size

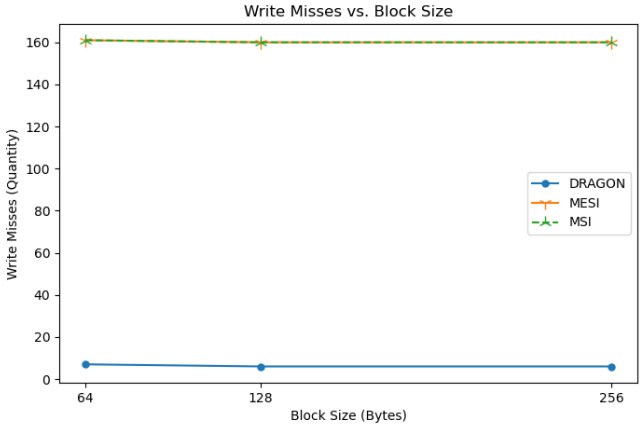

Figure 8: Aggregate Write Misses vs Block Size

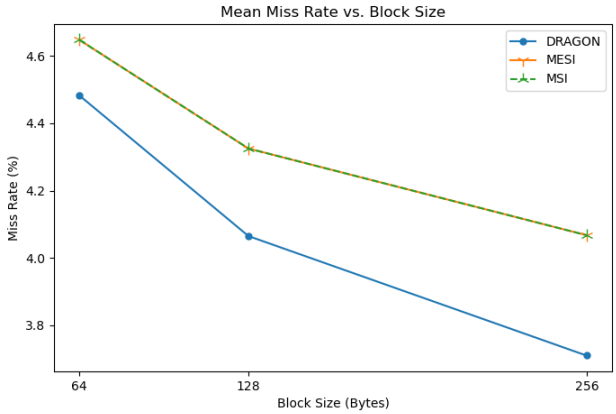

Figure 9: Aggregate Miss Rate vs Block Size

Varying Cache Size: Main Memory Traffic and Writebacks

The following figures detail the effects of varying L1 private cache sizes (symmetric private caches) from 256KiB to 2MiB on traffic to/from Main Memory, as well as writebacks executed from all private caches. In the global memory traffic plot, I find MESI to present a significantly improved reduction in overall memory traffic, for all cache sizes. This is due to MESI permitting cache-to-cache transfers, which significantly reduces the traffic to main memory when coherence invalidations and interventions happen between private caches. MSI presents the worst memory traffic performance, with Dragon performing slightly better but presenting the same trend. These identical curve shapes (with MSI offset) are likely due to resolving capacity misses due to cache size rather than coherence.

Also, I find as cache size grows, writebacks fall on a similar trend as global miss rate, again, due more to resolution of capacity misses than to coherence implementation. I note that Dragon performs better w.r.t. writebacks, as a result of dirty-sharing being permitted between Sc and Sm cache lines.

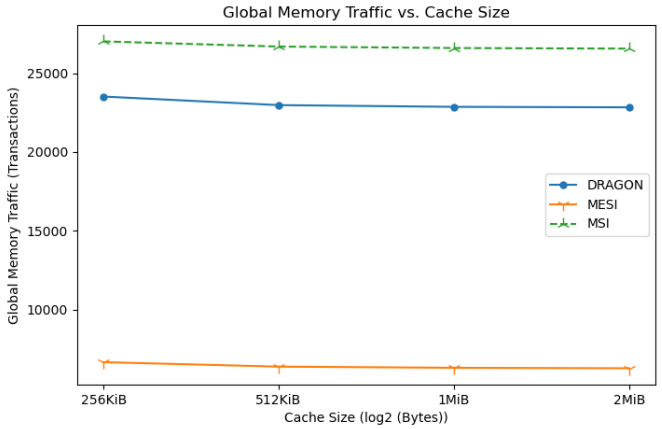

Figure 10: Aggregate Memory Traffic vs Cache Size

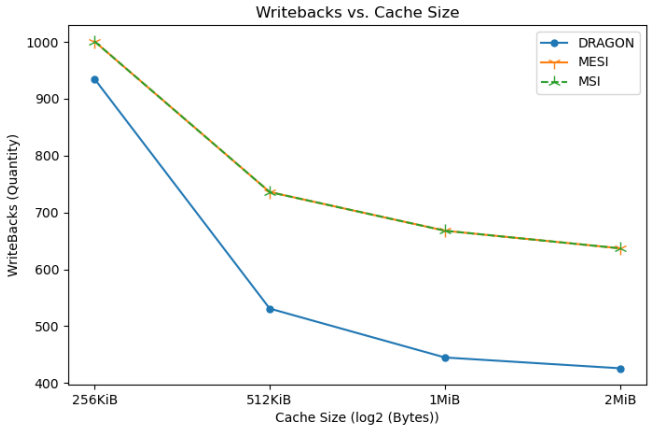

Figure 11: Aggregate WriteBacks vs Cache Size

Varying Associativity: Main Memory Traffic and Writebacks

The following figures detail the effects of varying L1 private cache Associativity (symmetric private caches) from 4 ways to 16 ways, on traffic to/from Main Memory, as well as writebacks executed from all private caches. I note that associativity has minimal effect on global memory traffic, with MSI, MESI, and Dragon presenting nearly-flat curves with similar offsets to those observed in varying cache sizes.

I do not some similar trends in the Writebacks plot to the cache size plot, where identical curves are shows for MSI and MESI as a result of their invalidations, and Dragon outperforming both once again due to dirty sharing.

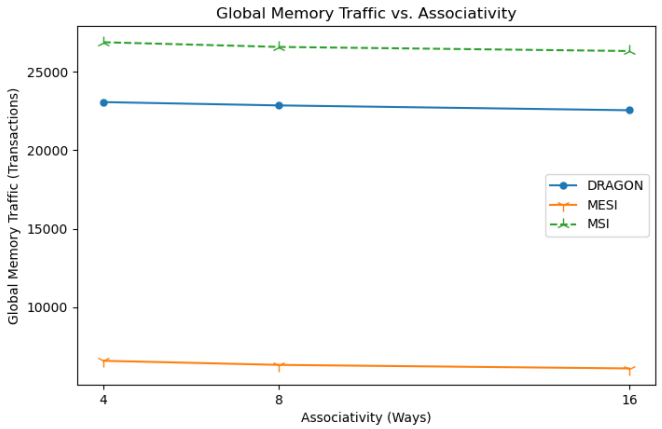

Figure 12: Aggregate Memory Traffic vs Associativity

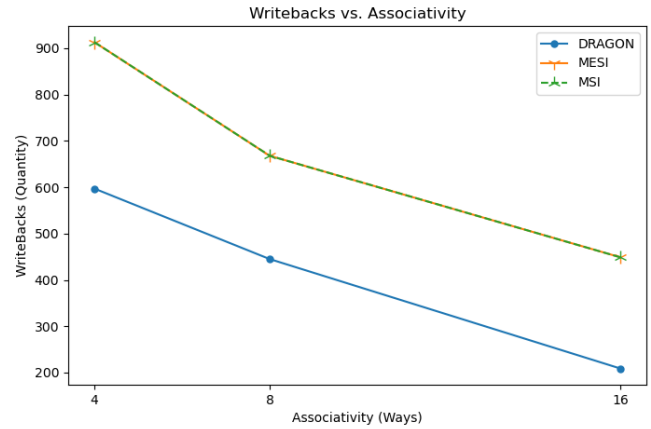

Figure 13: Aggregate WriteBacks vs Associativity

Varying Block Size: Main Memory Traffic and Writebacks

The following figures detail the effects of varying L1 private cache Block Size (symmetric private caches) from 4 ways to 16 ways, on traffic to/from Main Memory, as well as writebacks executed from all private caches. Varying Block Size presents two interesting trends: a small trends towards reduction in global memory traffic for MSI and Dragon, and a signficant trends for all protocols towards more writebacks to main memory. The increasing writebacks due to block size is likely due to fewer overall cache lines for a fixed size of cache, which means more regular writebacks are required to manage the dirty blocks upon evictions.

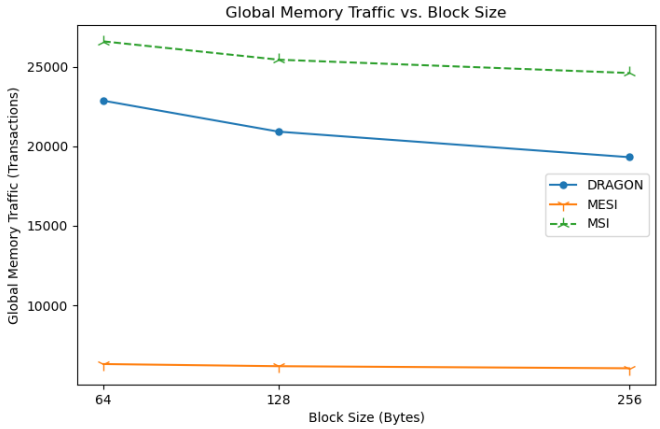

Figure 14: Aggregate Memory Traffic vs Block Size

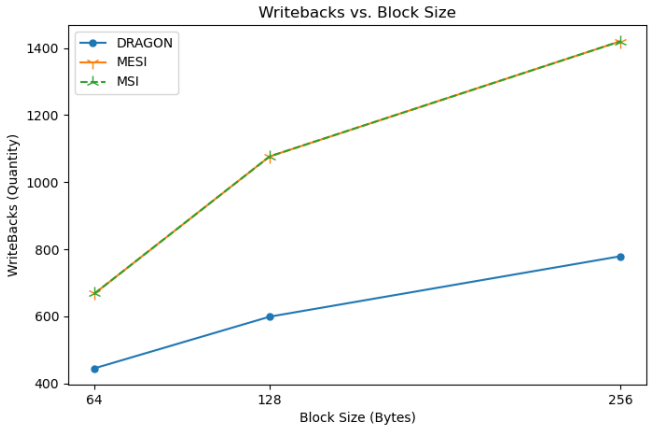

Figure 15: Aggregate WriteBacks vs Block Size

Varying Cache Size, Associativity, Block Size: Cache-Cache Transfers in MESI

The following figures detail the statistics for Cache-to-Cache Transfers of full blocks in MESI (the only protocol studied that allows this specific functionality. It can be noted from all of these plots that there is a fairly strong correlation between falling miss rates as the Cache Size, Associativity, and Block Size parameters grow. This is to be expected as fewer misses lead to fewer evictions, which leads to fewer required transfers to maintain expected cache state.

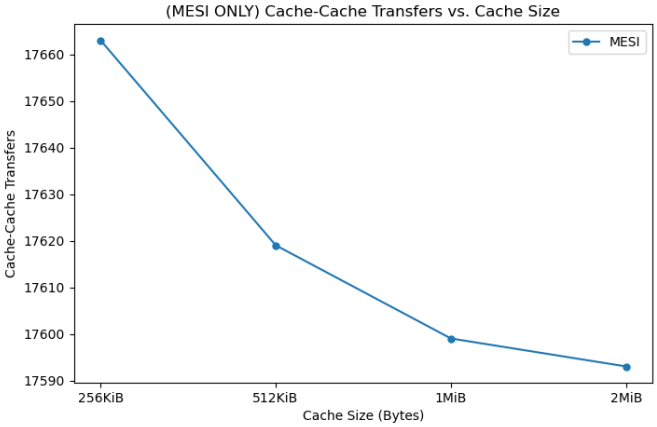

Figure 16: MESI C-C Transfers vs Cache Size

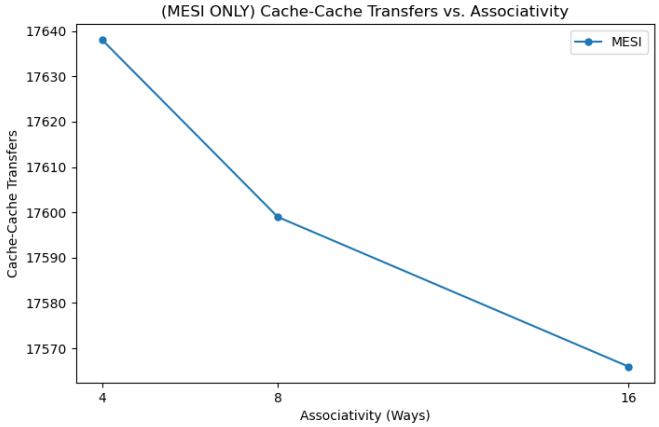

Figure 17: MESI C-C Transfers vs Associativity

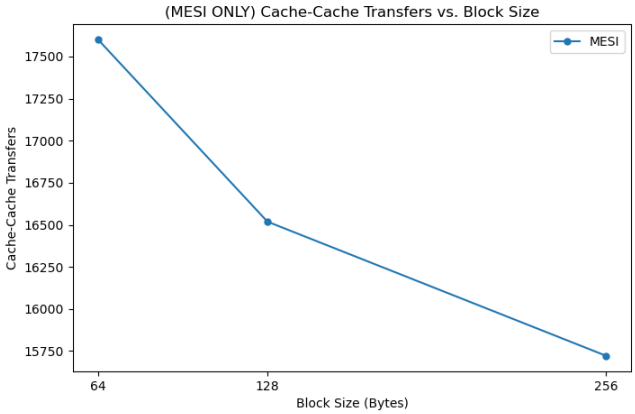

Figure 18: MESI C-C Transfers vs Block Size

Varying Cache Size: Inter-Cache Communication

The following figures detail the effects of varying L1 private cache sizes (symmetric private caches) from 256KiB to 2MiB on inter-cache coherence messages, including Interventions, Invalidations, Flushes, and BusRdX.

These plots reaffirm the prior claims that cache size has minimal effect on coherence activity; I note that quantities of coherence messages remain nearly static for all protocols across all ranges of cache size. By examining the tabulated values in Tables 1 through 3, I find that MSI presents a small growth of interventions and flushes as cache size grows, with MESI presenting a small shrink in Interventions and a small growth in flushes. Flushes for both MSI and MESI present identical small growth as cache size grows. Flushes for Dragon present a small shrinkage as cache size increases. All of these trends present secondary effects resulting from reduced Capacity misses as explored in prior sections.

Furthermore, I note that Invalidations and BusRdX messages remain fixed across all sizes, with Dragon presenting zero of both as Dragon does not use Invalidations and BusRdX to implement its coherence protocol.

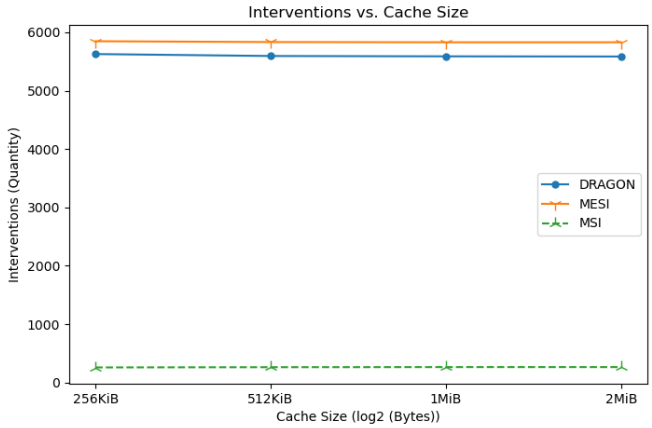

Figure 19: Aggregate Memory Traffic vs Cache Size

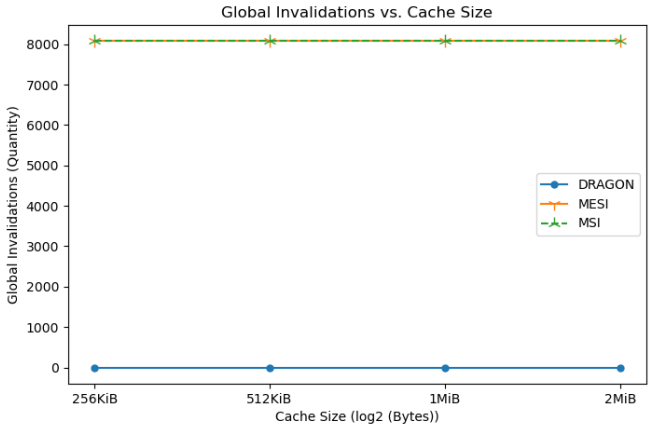

Figure 20: Aggregate WriteBacks vs Cache Size

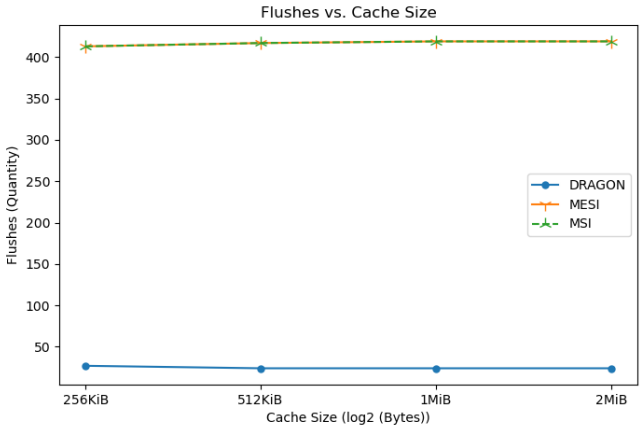

Figure 21: Aggregate Memory Traffic vs Cache Size

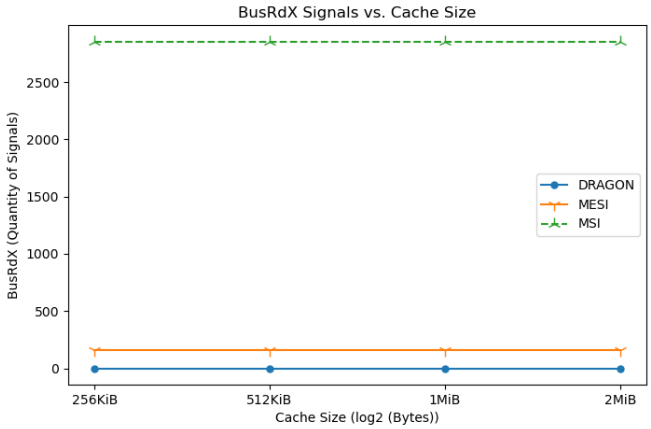

Figure 22: Aggregate WriteBacks vs Cache Size

Varying Associativity: Inter-Cache Communication

The following figures detail the effects of varying L1 private cache Associativity (symmetric private caches) from 4 ways to 16 ways, on inter-cache coherence messages, including Interventions, Invalidations, Flushes, and BusRdX.

Very similar trends may be observed in this section, to the prior experiment on Cache Size. I note that Again, flushes and interventions follow the same trends as associativity grows, further reaffirming the reduced effect of individual private cache associativity on coherence traffic, as compared to a theoretical experiment with varying numbers of processor cores and private caches. Again, Invalidations and BusRdX remain the same for all sizes, with small trends observed for Interventions and Flushes.

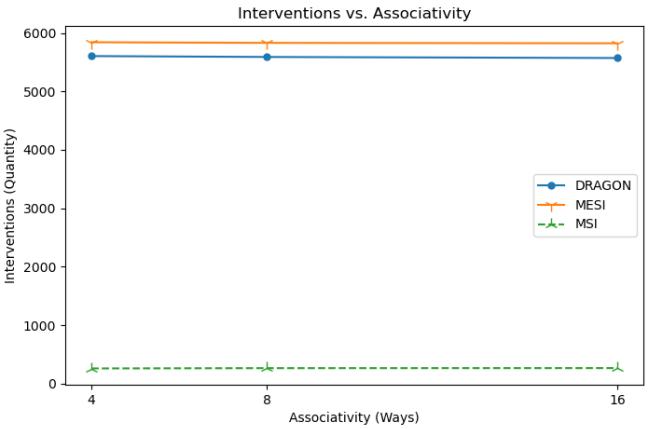

Figure 23: Aggregate Memory Traffic vs Associativity

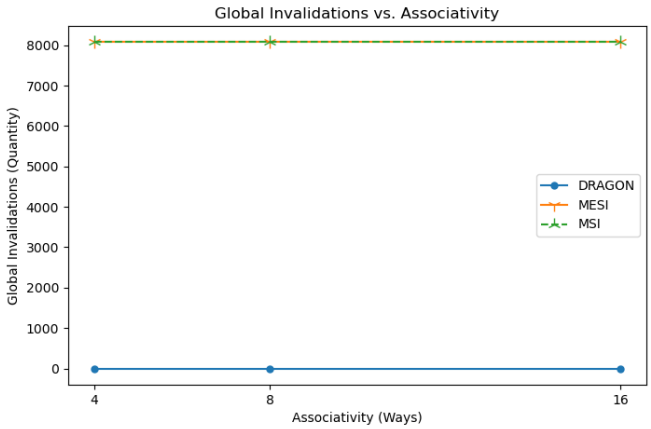

Figure 24: Aggregate WriteBacks vs Associativity

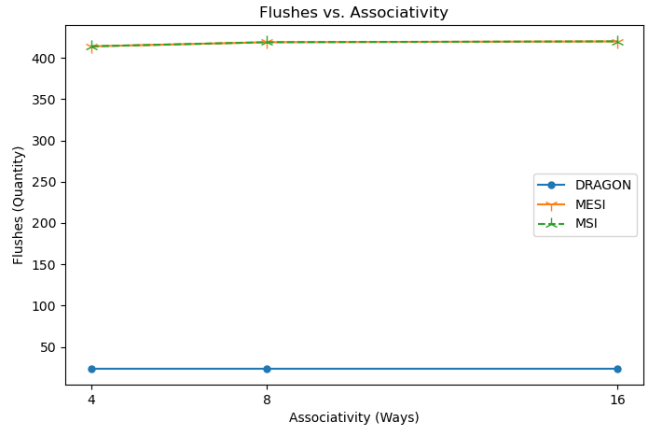

Figure 25: Aggregate Memory Traffic vs Associativity

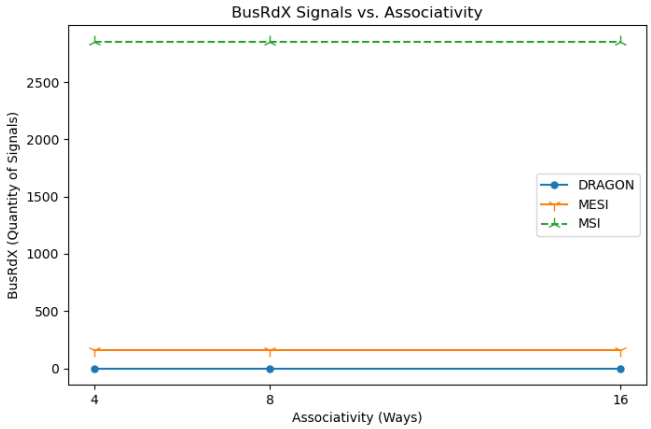

Figure 26: Aggregate WriteBacks vs Associativity

Varying Block Size: Inter-Cache Communication

The following figures detail the effects of varying L1 private cache Block Size (symmetric private caches) from 4 ways to 16 ways, on inter-cache coherence messages, including Interventions, Invalidations, Flushes, and BusRdX.

Block Size presents a much more interesting case for Coherence traffic analysis. As block size grows, Interventions for Dragon and MESI fall, but MSI interventions increase: this is a result of more data being brought in with each eviction and emplacement of a new cacheline. I note that, as expected, Dragon global invalidations are fixed at zero but MSI and MESI present worsening invalidations as cache pollution increases due to the larger block sizes. A similar trend presents in the plot for Flushes, where increased collisions in the cache between requiring individual words located less-than-ideally in larger cache lines forces increasing uses of flushes to transmit data to the requesting core. Finally, I note a similar trend in BusRdX, but with a much reduced slope – as cache pollution increases, we expect to see BusRdX requests increase thanks to pollution-triggered evictions accompanied by new requests for data.

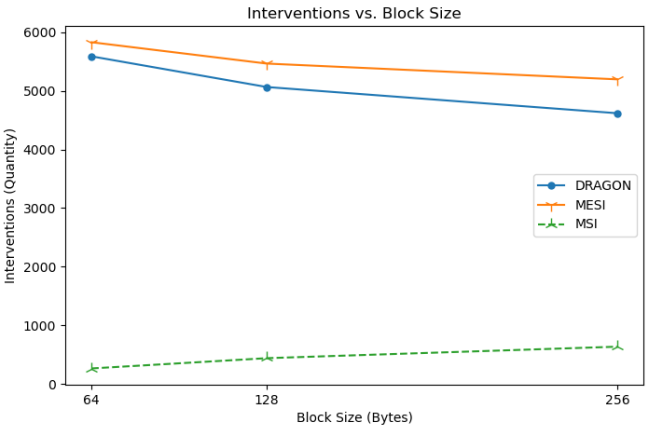

Figure 27: Aggregate Memory Traffic vs Block Size

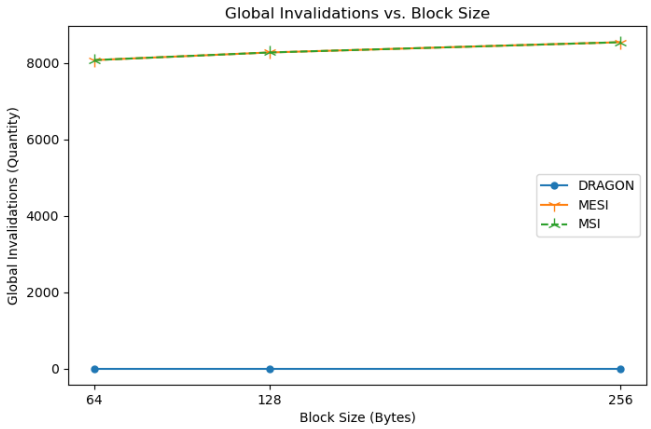

Figure 28: Aggregate WriteBacks vs Block Size

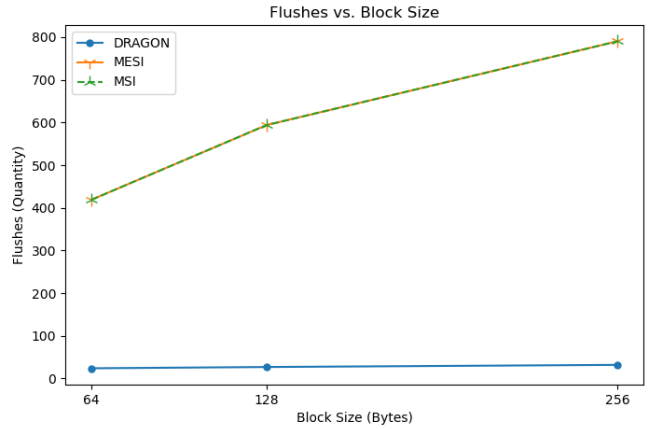

Figure 29: Aggregate Memory Traffic vs Block Size

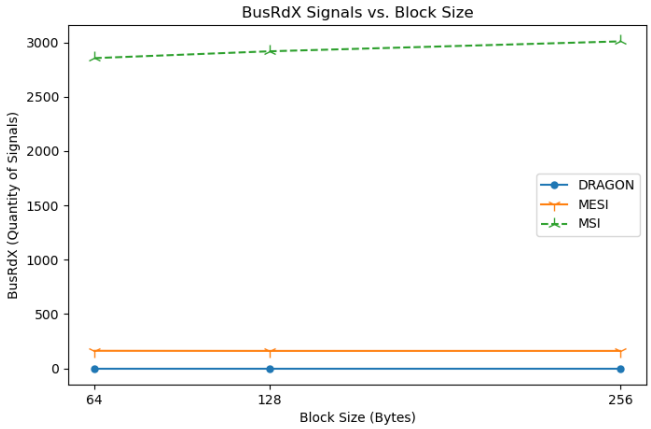

Figure 30: Aggregate WriteBacks vs Block Size

Final Conclusions

The strategies detailed in this paper broadly explore the advantages and disadvantages of coherence protocols vs symmetric private cache configurations. Several broad conclusions may be formed from these data.

First, while Dragon appears to outperform the invalidation-based protocols on Miss Rate, observation of the total memory traffic presents a trend towards MESI outperforming on overall traffic thanks to cache-to-cache transfers. Furthermore, Dragon presents a much lower writeback rate thanks to Dirty sharing, yet does not perform nearly as effectively as MESI when directly comparing Global Memory Traffic.

Second, and difficult to observe from the presented data, I note that the Dragon protocol may present greater implementation complexity thanks to the intricacies of Dirty Sharing, and the ability to move both entire blocks and specific dirty lines. There are considerable tradeoffs when considering an update-based protocol such as Dragon, as compared to the more popular invalidation-based protocols like MSI, MESI, MOESI, and MESIF.

Third, I note that the data on Block Size seems to reinforce the generally accepted best-practice of choosing a 64B cache line size. While overall miss rates are significantly reduced with increasing block size, the effects on main memory traffic are less clear, and the steep increase in Writebacks indicates a possible scalability issue as the quantity of cores increases.

Finally, and most broadly, it is clear from these data that choosing a coherence protocol is not so simple as presenting a single protocol as "best case." Each protocol explored in this project presented tradeoffs, where one could outperform another in one experimental datapoint, then far underperform in a different datapoint. When choosing a coherence protocol design as a Computer Architect, clearly more simulation and experimentation is required as the quantity of cores and private caches grows towards, and past, 128 cores/chip in a datacenter-class architecture. Furthermore, multiple-level caches and the effects of a shared L2 vs Miss penalty vs Miss rate need be explored in depth, as well as exploration of cutting-edge concepts such as locating main memory on-chip, SRAM vs SRAM/NVRAM hybrid designs, and memory-centric architecture.

Appendix A: Raw Experiment Data

Cache Size Data

Protocol	Size	Assc	BS	#	1_read	1_rMiss	1_write	1_wMiss	1_mRate	1_wBs	1_xFer	1_mTraf	1_ints	1_invs	1_flsh	1_RdX
MSI	262144	8	64	0	112661	5775	11942	39	4.67	254	0	6745	68	2014	113	716
MSI	524288	8	64	0	112661	5757	11942	39	4.65	190	0	6663	71	2014	116	716
MSI	1048576	8	64	0	112661	5752	11942	39	4.65	170	0	6638	71	2014	116	716
MSI	2097152	8	64	0	112661	5750	11942	39	4.65	166	0	6632	71	2014	116	716
MESI	262144	8	64	0	112661	5775	11942	39	4.67	254	4405	1663	1468	2014	113	39
MESI	524288	8	64	0	112661	5757	11942	39	4.65	190	4392	1594	1466	2014	116	39
MESI	1048576	8	64	0	112661	5752	11942	39	4.65	170	4389	1572	1464	2014	116	39
MESI	2097152	8	64	0	112661	5750	11942	39	4.65	166	4387	1568	1464	2014	116	39
DRAGON	262144	8	64	0	112661	5635	11942	3	4.52	226	0	5864	1405	0	3	0
DRAGON	524288	8	64	0	112661	5601	11942	3	4.5	128	0	5732	1400	0	3	0
DRAGON	1048576	8	64	0	112661	5595	11942	3	4.49	107	0	5705	1398	0	3	0
DRAGON	2097152	8	64	0	112661	5591	11942	3	4.49	102	0	5696	1396	0	3	0
					2_read	2_rMiss	2_write	2_wMiss	2_mRate	2_wBs	2_xFer	2_mTraf	2_ints	2_invs	2_flsh	2_RdX
MSI	262144	8	64	1	110830	5805	11710	41	4.77	235	0	6740	47	2034	92	700
MSI	524288	8	64	1	110830	5792	11710	41	4.76	170	0	6662	47	2034	92	700
MSI	1048576	8	64	1	110830	5781	11710	41	4.75	155	0	6636	48	2034	93	700
MSI	2097152	8	64	1	110830	5779	11710	41	4.75	143	0	6622	48	2034	93	700
MESI	262144	8	64	1	110830	5805	11710	41	4.77	235	4441	1640	1432	2034	92	41
MESI	524288	8	64	1	110830	5792	11710	41	4.76	170	4431	1572	1429	2034	92	41
MESI	1048576	8	64	1	110830	5781	11710	41	4.75	155	4422	1555	1428	2034	93	41
MESI	2097152	8	64	1	110830	5779	11710	41	4.75	143	4420	1543	1428	2034	93	41
DRAGON	262144	8	64	1	110830	5646	11710	2	4.61	243	0	5891	1396	0	9	0
DRAGON	524288	8	64	1	110830	5610	11710	2	4.58	127	0	5739	1388	0	9	0
DRAGON	1048576	8	64	1	110830	5604	11710	2	4.57	110	0	5716	1387	0	9	0
DRAGON	2097152	8	64	1	110830	5603	11710	2	4.57	105	0	5710	1387	0	9	0
					3_read	3_rMiss	3_write	3_wMiss	3_mRate	3_wBs	3_xFer	3_mTraf	3_ints	3_invs	3_flsh	3_RdX
MSI	262144	8	64	2	114938	5771	12383	42	4.57	278	0	6774	81	2008	120	725
MSI	524288	8	64	2	114938	5756	12383	42	4.55	205	0	6686	82	2008	121	725
MSI	1048576	8	64	2	114938	5752	12383	42	4.55	186	0	6663	82	2008	121	725
MSI	2097152	8	64	2	114938	5751	12383	42	4.55	176	0	6652	82	2008	121	725
MESI	262144	8	64	2	114938	5771	12383	42	4.57	278	4406	1685	1469	2008	120	42
MESI	524288	8	64	2	114938	5756	12383	42	4.55	205	4396	1607	1465	2008	121	42
MESI	1048576	8	64	2	114938	5752	12383	42	4.55	186	4393	1587	1464	2008	121	42
MESI	2097152	8	64	2	114938	5751	12383	42	4.55	176	4392	1577	1464	2008	121	42
DRAGON	262144	8	64	2	114938	5644	12383	2	4.43	232	0	5878	1398	0	6	0
DRAGON	524288	8	64	2	114938	5610	12383	2	4.41	135	0	5747	1389	0	6	0
DRAGON	1048576	8	64	2	114938	5604	12383	2	4.4	105	0	5711	1387	0	6	0
DRAGON	2097152	8	64	2	114938	5601	12383	2	4.4	98	0	5701	1387	0	6	0
					4_read	4_rMiss	4_write	4_wMiss	4_mRate	4_wBs	4_xFer	4_mTraf	4_ints	4_invs	4_flsh	4_RdX
MSI	262144	8	64	3	113428	5813	12108	39	4.66	234	0	6761	63	2020	88	714
MSI	524288	8	64	3	113428	5796	12108	39	4.65	171	0	6681	63	2020	88	714
MSI	1048576	8	64	3	113428	5790	12108	39	4.64	157	0	6661	64	2020	89	714
MSI	2097152	8	64	3	113428	5789	12108	39	4.64	152	0	6655	64	2020	89	714
MESI	262144	8	64	3	113428	5813	12108	39	4.66	234	4411	1675	1479	2020	88	39
MESI	524288	8	64	3	113428	5796	12108	39	4.65	171	4400	1606	1474	2020	88	39
MESI	1048576	8	64	3	113428	5790	12108	39	4.64	157	4395	1591	1474	2020	89	39
MESI	2097152	8	64	3	113428	5789	12108	39	4.64	152	4394	1586	1474	2020	89	39
DRAGON	262144	8	64	3	113428	5652	12108	0	4.5	234	0	5886	1429	0	9	0
DRAGON	524288	8	64	3	113428	5617	12108	0	4.47	141	0	5758	1418	0	6	0
DRAGON	1048576	8	64	3	113428	5611	12108	0	4.47	123	0	5734	1417	0	6	0
DRAGON	2097152	8	64	3	113428	5608	12108	0	4.47	121	0	5729	1416	0	6	0
					Reads	rMiss	Writes	wMiss	mRate	wBs	xFer	mTraf	ints	invs	flsh	RdX
MSI	262144	8	64	ALL	451857	23164	48143	161	4.6675	1001	0	27020	259	8076	413	2855
MSI	524288	8	64	ALL	451857	23101	48143	161	4.6525	736	0	26692	263	8076	417	2855
MSI	1048576	8	64	ALL	451857	23075	48143	161	4.6475	668	0	26598	265	8076	419	2855
MSI	2097152	8	64	ALL	451857	23069	48143	161	4.6475	637	0	26561	265	8076	419	2855
MESI	262144	8	64	ALL	451857	23164	48143	161	4.6675	1001	17663	6663	5848	8076	413	161
MESI	524288	8	64	ALL	451857	23101	48143	161	4.6525	736	17619	6379	5834	8076	417	161
MESI	1048576	8	64	ALL	451857	23075	48143	161	4.6475	668	17599	6305	5830	8076	419	161
MESI	2097152	8	64	ALL	451857	23069	48143	161	4.6475	637	17593	6274	5830	8076	419	161
DRAGON	262144	8	64	ALL	451857	22577	48143	7	4.515	935	0	23519	5628	0	27	0
DRAGON	524288	8	64	ALL	451857	22438	48143	7	4.49	531	0	22976	5595	0	24	0
DRAGON	1048576	8	64	ALL	451857	22414	48143	7	4.4825	445	0	22866	5589	0	24	0
DRAGON	2097152	8	64	ALL	451857	22403	48143	7	4.4825	426	0	22836	5586	0	24	0

Associativity Data

Protocol	Size	Assc	Bs	#	1_read	1_rMiss	1_write	1_wMiss	1_mRate	1_wb	1_xFer	1_mem	1_ints	1_invs	1_flsh	1_RdX
MSI	1048576	4	64	0	112661	5768	11942	39	4.66	239	0	6723	69	2014	114	716
MSI	1048576	8	64	0	112661	5752	11942	39	4.65	170	0	6638	71	2014	116	716
MSI	1048576	16	64	0	112661	5741	11942	39	4.64	120	0	6577	71	2014	116	716
MESI	1048576	4	64	0	112661	5768	11942	39	4.66	239	4402	1644	1465	2014	114	39
MESI	1048576	8	64	0	112661	5752	11942	39	4.65	170	4389	1572	1464	2014	116	39
MESI	1048576	16	64	0	112661	5741	11942	39	4.64	120	4379	1521	1463	2014	116	39
DRAGON	1048576	4	64	0	112661	5609	11942	3	4.5	148	0	5760	1400	0	3	0
DRAGON	1048576	8	64	0	112661	5595	11942	3	4.49	107	0	5705	1398	0	3	0
DRAGON	1048576	16	64	0	112661	5576	11942	3	4.48	47	0	5626	1395	0	3	0
				#	2_read	2_rMiss	2_write	2_wMiss	2_mRate	2_wb	2_xFer	2_mem	2_ints	2_invs	2_flsh	2_RdX
MSI	1048576	4	64	1	110830	5797	11710	41	4.76	211	0	6708	47	2034	92	700
MSI	1048576	8	64	1	110830	5781	11710	41	4.75	155	0	6636	48	2034	93	700
MSI	1048576	16	64	1	110830	5772	11710	41	4.74	101	0	6573	48	2034	93	700
MESI	1048576	4	64	1	110830	5797	11710	41	4.76	211	4434	1615	1431	2034	92	41
MESI	1048576	8	64	1	110830	5781	11710	41	4.75	155	4422	1555	1428	2034	93	41
MESI	1048576	16	64	1	110830	5772	11710	41	4.74	101	4415	1499	1426	2034	93	41
DRAGON	1048576	4	64	1	110830	5619	11710	2	4.59	149	0	5770	1392	0	9	0
DRAGON	1048576	8	64	1	110830	5604	11710	2	4.57	110	0	5716	1387	0	9	0
DRAGON	1048576	16	64	1	110830	5586	11710	2	4.56	43	0	5631	1382	0	9	0
				#	3_read	3_rMiss	3_write	3_wMiss	3_mRate	3_wb	3_xFer	3_mem	3_ints	3_invs	3_flsh	3_RdX
MSI	1048576	4	64	2	114938	5762	12383	42	4.56	239	0	6726	81	2008	120	725
MSI	1048576	8	64	2	114938	5752	12383	42	4.55	186	0	6663	82	2008	121	725
MSI	1048576	16	64	2	114938	5741	12383	42	4.54	130	0	6596	83	2008	122	725
MESI	1048576	4	64	2	114938	5762	12383	42	4.56	239	4401	1642	1465	2008	120	42
MESI	1048576	8	64	2	114938	5752	12383	42	4.55	186	4393	1587	1464	2008	121	42
MESI	1048576	16	64	2	114938	5741	12383	42	4.54	130	4386	1527	1461	2008	122	42
DRAGON	1048576	4	64	2	114938	5619	12383	2	4.41	142	0	5763	1388	0	6	0
DRAGON	1048576	8	64	2	114938	5604	12383	2	4.4	105	0	5711	1387	0	6	0
DRAGON	1048576	16	64	2	114938	5586	12383	2	4.39	62	0	5650	1383	0	6	0
				#	4_read	4_rMiss	4_write	4_wMiss	4_mRate	4_wb	4_xFer	4_mem	4_ints	4_invs	4_flsh	4_RdX
MSI	1048576	4	64	3	113428	5803	12108	39	4.65	224	0	6741	63	2020	88	714
MSI	1048576	8	64	3	113428	5790	12108	39	4.64	157	0	6661	64	2020	89	714
MSI	1048576	16	64	3	113428	5780	12108	39	4.64	98	0	6592	64	2020	89	714
MESI	1048576	4	64	3	113428	5803	12108	39	4.65	224	4401	1665	1480	2020	88	39
MESI	1048576	8	64	3	113428	5790	12108	39	4.64	157	4395	1591	1474	2020	89	39
MESI	1048576	16	64	3	113428	5780	12108	39	4.64	98	4386	1531	1473	2020	89	39
DRAGON	1048576	4	64	3	113428	5626	12108	0	4.48	158	0	5784	1424	0	6	0
DRAGON	1048576	8	64	3	113428	5611	12108	0	4.47	123	0	5734	1417	0	6	0
DRAGON	1048576	16	64	3	113428	5593	12108	0	4.46	57	0	5650	1411	0	6	0
				#	Reads	rMiss	Writes	wMiss	mRate	wb	xFer	mem	ints	invs	flsh	RdX
MSI	1048576	4	64	ALL	451857	23130	48143	161	4.6575	913	0	26898	260	8076	414	2855
MSI	1048576	8	64	ALL	451857	23075	48143	161	4.6475	668	0	26598	265	8076	419	2855
MSI	1048576	16	64	ALL	451857	23034	48143	161	4.64	449	0	26338	266	8076	420	2855
MESI	1048576	4	64	ALL	451857	23130	48143	161	4.6575	913	17638	6566	5841	8076	414	161
MESI	1048576	8	64	ALL	451857	23075	48143	161	4.6475	668	17599	6305	5830	8076	419	161
MESI	1048576	16	64	ALL	451857	23034	48143	161	4.64	449	17566	6078	5823	8076	420	161
DRAGON	1048576	4	64	ALL	451857	22473	48143	7	4.495	597	0	23077	5604	0	24	0
DRAGON	1048576	8	64	ALL	451857	22414	48143	7	4.4825	445	0	22866	5589	0	24	0
DRAGON	1048576	16	64	ALL	451857	22341	48143	7	4.4725	209	0	22557	5571	0	24	0

BlockSize Data

Protocol	Size	Asc	**Bs**	**#**	**1_read**	**1_rMiss**	**1_write**	**1_wMiss**	**1_mRate**	**1_wb**	**1_xFer**	**1_mem**	**1_ints**	**1_invs**	**1_flsh**	**1_RdX**
MSI	1048576	8	64	0	112661	5752	11942	39	4.65	170	0	6638	71	2014	116	716
MSI	1048576	8	128	0	112661	5340	11942	39	4.32	275	0	6344	119	2066	164	729
MSI	1048576	8	256	0	112661	5023	11942	39	4.06	363	0	6137	166	2132	211	751
MESI	1048576	8	64	0	112661	5752	11942	39	4.65	170	4389	1572	1464	2014	116	39
MESI	1048576	8	128	0	112661	5340	11942	39	4.32	275	4124	1530	1367	2066	164	39
MESI	1048576	8	256	0	112661	5023	11942	39	4.06	363	3938	1487	1283	2132	211	39
DRAGON	1048576	8	64	0	112661	5595	11942	3	4.49	107	0	5705	1398	0	3	0
DRAGON	1048576	8	128	0	112661	5069	11942	3	4.07	145	0	5217	1256	0	3	0
DRAGON	1048576	8	256	0	112661	4628	11942	3	3.72	198	0	4829	1125	0	3	0
				#	2_read	2_rMiss	2_write	2_wMiss	2_mRate	2_wb	2_xFer	2_mem	2_ints	2_invs	2_flsh	2_RdX
MSI	1048576	8	64	1	110830	5781	11710	41	4.75	155	0	6636	48	2034	93	700
MSI	1048576	8	128	1	110830	5386	11710	40	4.43	250	0	6347	84	2089	129	711
MSI	1048576	8	256	1	110830	5070	11710	40	4.17	342	0	6147	133	2157	178	735
MESI	1048576	8	64	1	110830	5781	11710	41	4.75	155	4422	1555	1428	2034	93	41
MESI	1048576	8	128	1	110830	5386	11710	40	4.43	250	4155	1521	1337	2089	129	40
MESI	1048576	8	256	1	110830	5070	11710	40	4.17	342	3943	1509	1284	2157	178	40
DRAGON	1048576	8	64	1	110830	5604	11710	2	4.57	110	0	5716	1387	0	9	0
DRAGON	1048576	8	128	1	110830	5080	11710	1	4.15	149	0	5230	1266	0	9	0
DRAGON	1048576	8	256	1	110830	4633	11710	1	3.78	200	0	4834	1175	0	11	0
				#	3_read	3_rMiss	3_write	3_wMiss	3_mRate	3_wb	3_xFer	3_mem	3_ints	3_invs	3_flsh	3_RdX
MSI	1048576	8	64	2	114938	5752	12383	42	4.55	186	0	6663	82	2008	121	725
MSI	1048576	8	128	2	114938	5341	12383	42	4.23	283	0	6369	127	2053	166	745
MSI	1048576	8	256	2	114938	5004	12383	42	3.96	383	0	6167	192	2107	231	780
MESI	1048576	8	64	2	114938	5752	12383	42	4.55	186	4393	1587	1464	2008	121	42
MESI	1048576	8	128	2	114938	5341	12383	42	4.23	283	4115	1551	1377	2053	166	42
MESI	1048576	8	256	2	114938	5004	12383	42	3.96	383	3903	1526	1321	2107	231	42
DRAGON	1048576	8	64	2	114938	5604	12383	2	4.4	105	0	5711	1387	0	6	0
DRAGON	1048576	8	128	2	114938	5080	12383	2	3.99	145	0	5227	1257	0	6	0
DRAGON	1048576	8	256	2	114938	4630	12383	2	3.64	185	0	4817	1143	0	9	0
				#	4_read	4_rMiss	4_write	4_wMiss	4_mRate	4_wb	4_xFer	4_mem	4_ints	4_invs	4_flsh	4_RdX
MSI	1048576	8	64	3	113428	5790	12108	39	4.64	157	0	6661	64	2020	89	714
MSI	1048576	8	128	3	113428	5384	12108	39	4.32	269	0	6386	110	2068	135	733
MSI	1048576	8	256	3	113428	5084	12108	39	4.08	332	0	6159	145	2148	170	743
MESI	1048576	8	64	3	113428	5790	12108	39	4.64	157	4395	1591	1474	2020	89	39
MESI	1048576	8	128	3	113428	5384	12108	39	4.32	269	4125	1567	1385	2068	135	39
MESI	1048576	8	256	3	113428	5084	12108	39	4.08	332	3939	1516	1309	2148	170	39
DRAGON	1048576	8	64	3	113428	5611	12108	0	4.47	123	0	5734	1417	0	6	0
DRAGON	1048576	8	128	3	113428	5086	12108	0	4.05	160	0	5246	1287	0	9	0
DRAGON	1048576	8	256	3	113428	4640	12108	0	3.7	196	0	4836	1176	0	9	0
					Reads	rMiss	Writes	wMiss	mRate	wb	xFer	MemoryTraffic	ints	invs	flsh	RdX
MSI	1048576	8	64	ALL	451857	23075	48143	161	4.6475	668	0	26598	265	8076	419	2855
MSI	1048576	8	128	ALL	451857	21451	48143	160	4.325	1077	0	25446	440	8276	594	2918
MSI	1048576	8	256	ALL	451857	20181	48143	160	4.0675	1420	0	24610	636	8544	790	3009
MESI	1048576	8	64	ALL	451857	23075	48143	161	4.6475	668	17599	6305	5830	8076	419	161
MESI	1048576	8	128	ALL	451857	21451	48143	160	4.325	1077	16519	6169	5466	8276	594	160
MESI	1048576	8	256	ALL	451857	20181	48143	160	4.0675	1420	15723	6038	5197	8544	790	160
DRAGON	1048576	8	64	ALL	451857	22414	48143	7	4.4825	445	0	22866	5589	0	24	0
DRAGON	1048576	8	128	ALL	451857	20315	48143	6	4.065	599	0	20920	5066	0	27	0
DRAGON	1048576	8	256	ALL	451857	18531	48143	6	3.71	779	0	19316	4619	0	32	0