Figure 1: Acceleration module 1.1
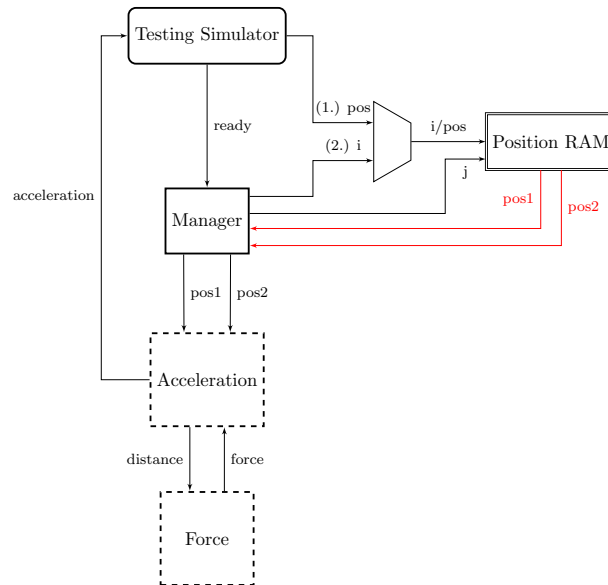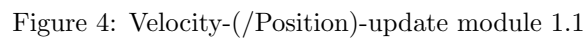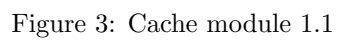

Figure 2: Acceleration module 1.2

1

Figure 3: Cache module 1.1

Figure 4: Velocity-(/Position)-update module 1.1

2

finished

External Simulator

ready

pos

(1.) pos   (2.) i   pos1   Acceleration Manager   pos1   Acceleration   distance   Force

(2.) i   (1.) pos/i   pos2   pos2   reset *from exsim*   force

reset   A   acceleration

P_{prev}

Position RAM   A
B

P_{prev} Cache

Position V_{curr} Position Manager   i/data   data
P_{curr}

B   Acceleration RAM   A

(2.) P_{curr} (1.) j   A

V_{curr} B   B

(2.) i   B   Velocity RAM   A   (1.) V_{init} B   B

(1.) i   (2.) V_{curr}

V_{prev} A_{curr}

ready   reset   Velocity Manager   i
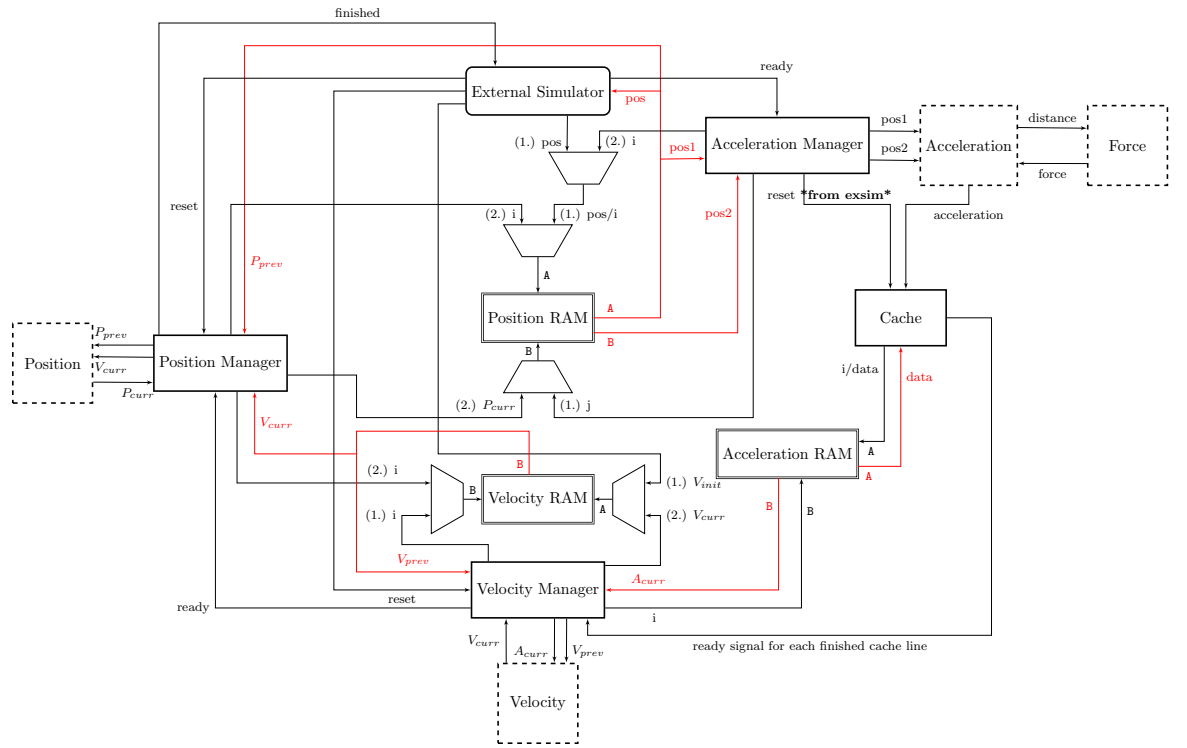
V_{curr} A_{curr} V_{prev} ready signal for each finished cache line

Velocity

Figure 5: Full LJ circuit

3