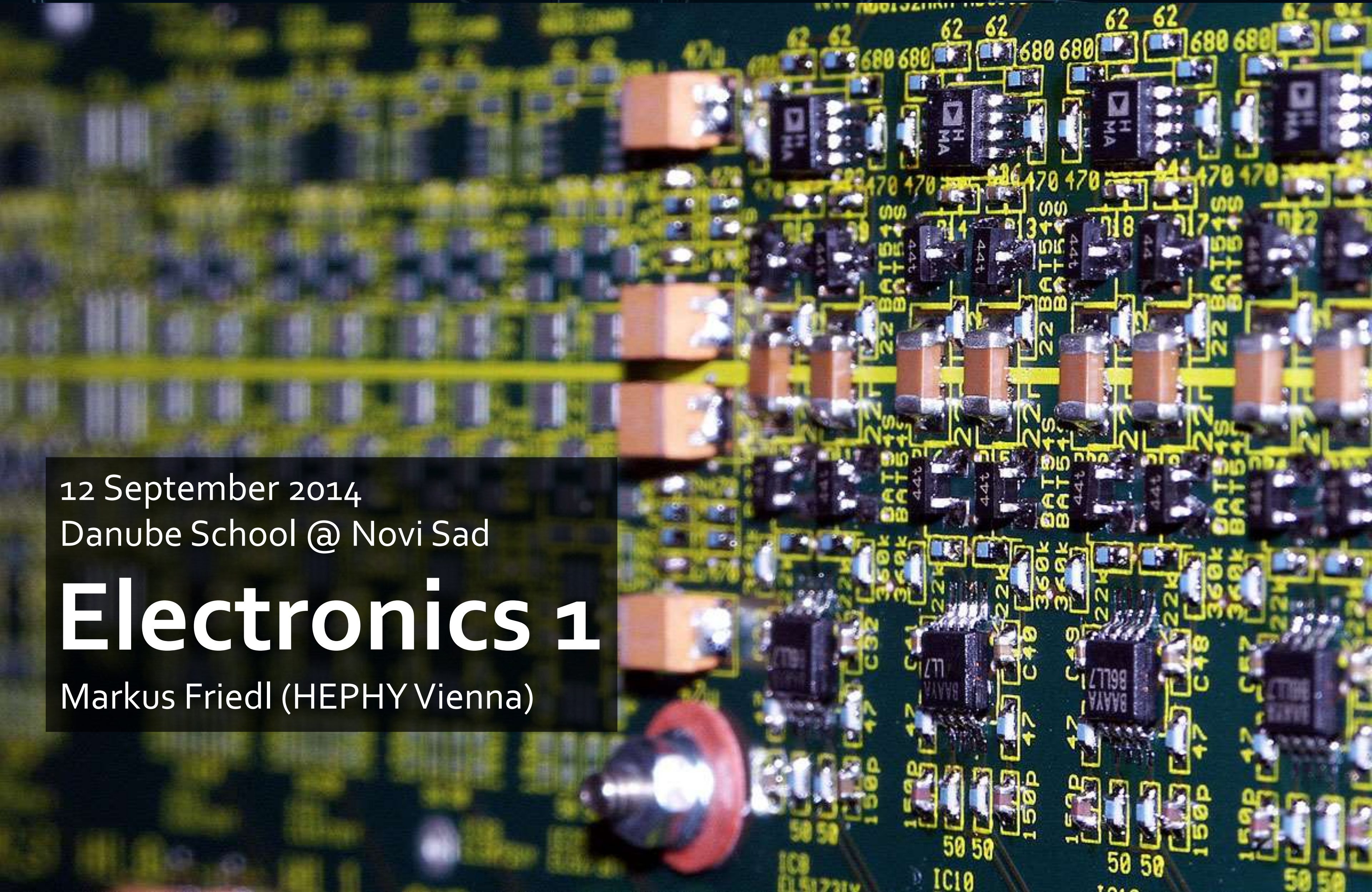
HEPHY Institute of High Energy Physics

ÖAW Austrian Academy of Sciences



12 September 2014

Danube School @ Novi Sad

Electronics 1

Markus Friedl (HEPHY Vienna)

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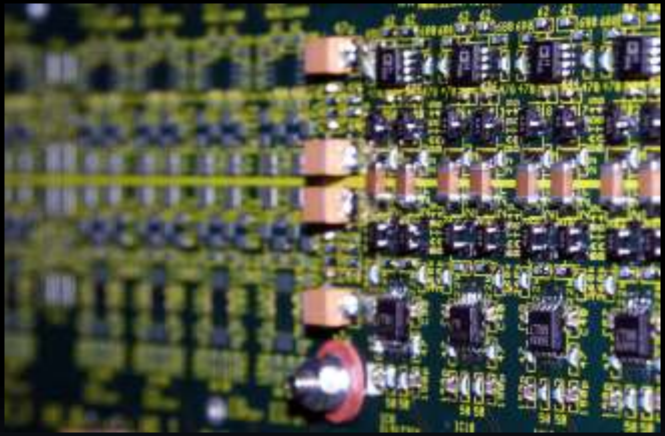
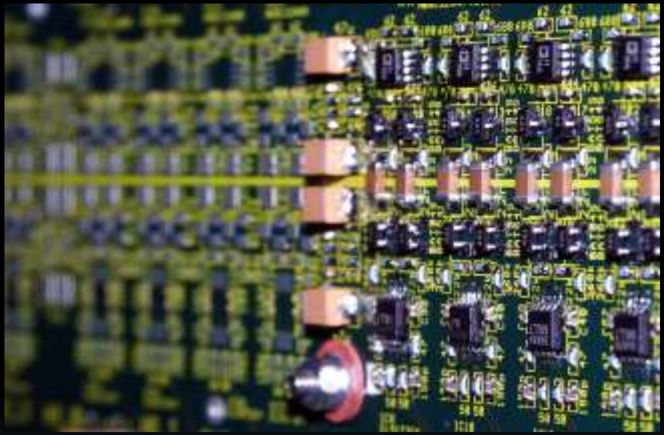


Early Detectors
Modern Detectors
Electronics – Introduction
Detectors and Their Readout
Detectors
Additional Topics



Early Detectors
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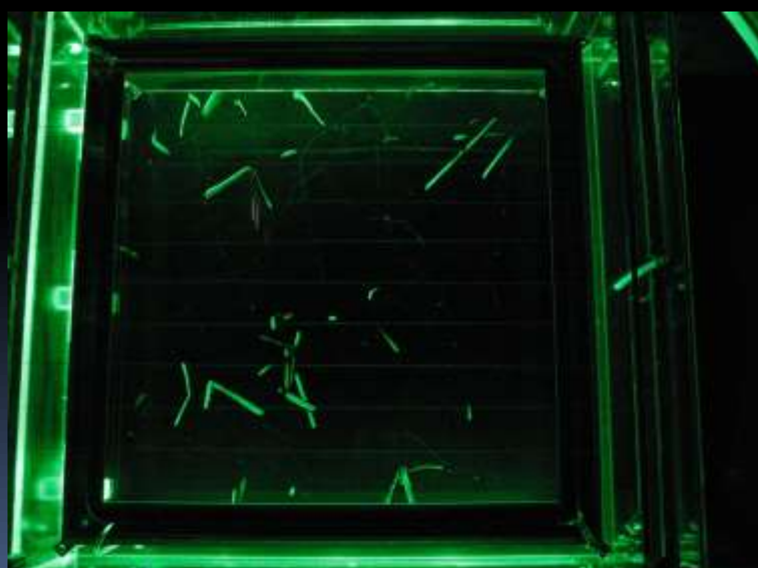
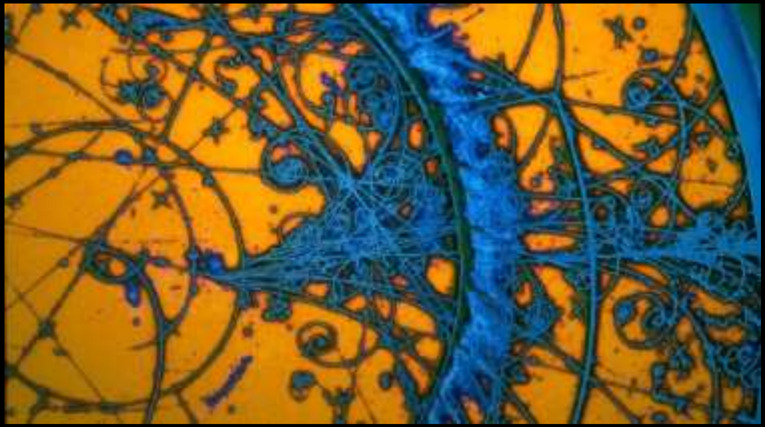
Early Detectors 1/4

- **Cloud chamber**
  - Supersaturated vapor
  - Ionization by charged particle creates condensation
  - Used 1920s…1950s



Early Detectors 2/4

- **Bubble chamber**
  - Like cloud chamber, but with superheated liquid
  - O(1) photo/second
  - Used 1960s…1980s

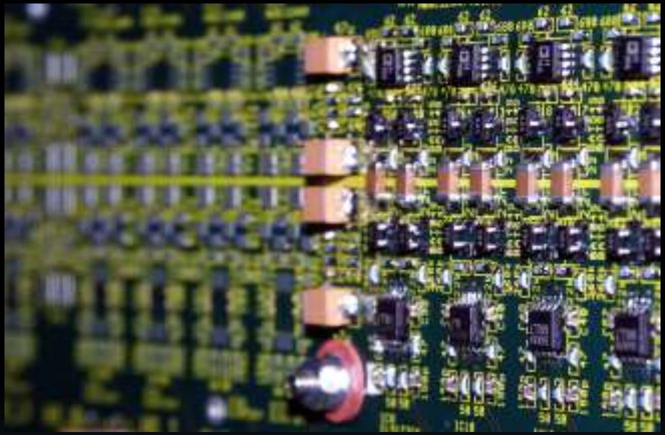


Early Detectors 3/4

- What do those historic detectors have in common?
- Their output is "visual" (captured by photography)
- No electronics involved
  - True for output data
  - Not exactly true in general, as bubble chambers were embedded in a strong magnet to bend charged particles depending on their momentum

Early Detectors 4/4

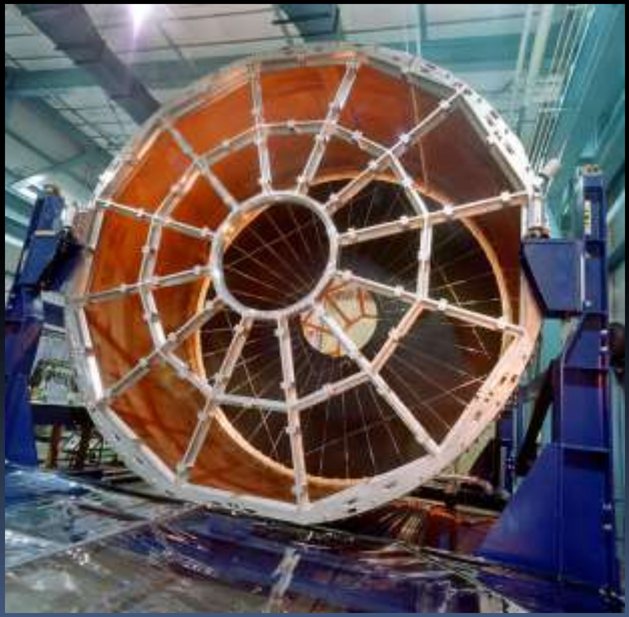
- “Scanning girls” working on bubble chamber photos
- Manual way of analog-to-digital conversion
- To provide particle track data for mainframe computers
- 1970s…1980s



- Early Detectors
- **Modern Detectors**
- Electronics – Introduction
- Detectors and Their Readout
- Detectors
- Additional Topics

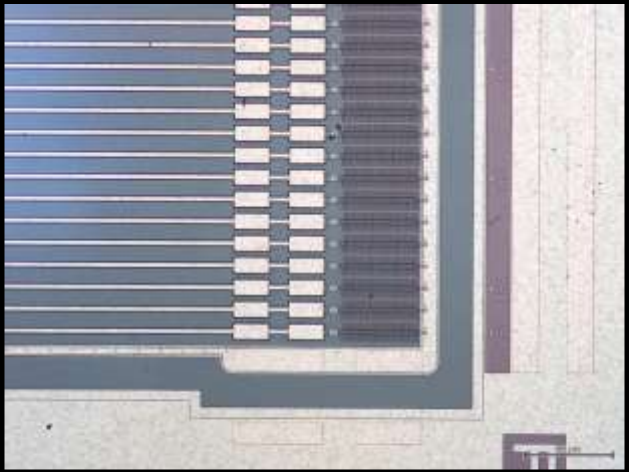
Modern Detectors 1/3

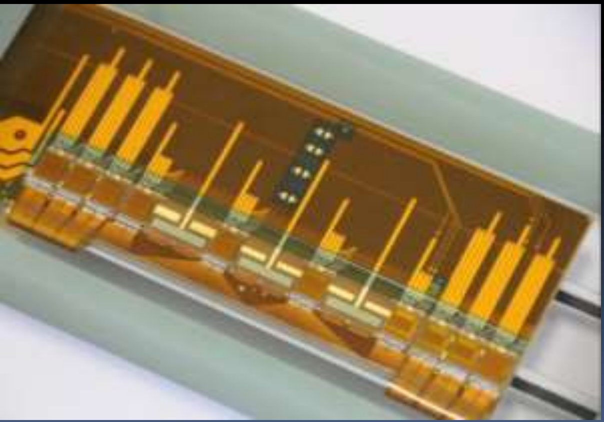
- Gas detectors
  - Multi-wire proportional chamber (MWPC)
    - Array of wires
    - Invented 1968 by Georges Charpak
  - Time projection chamber (TPC)
    - XY measurement by MWPC
    - Z measurement by drift time in gas volume
    - Invented 1974 by David Nygren
  - O(1000) measurements per second

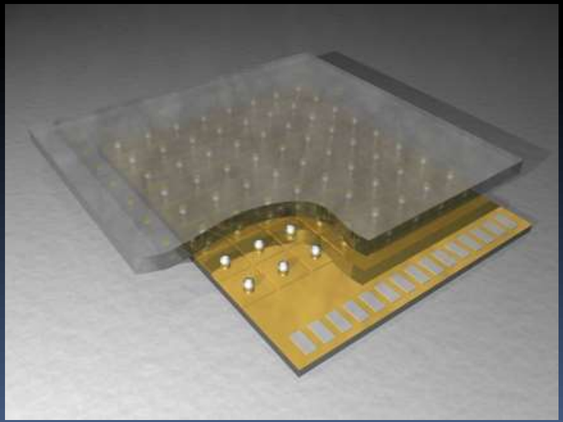


Modern Detectors 2/3

- Silicon detectors
  - Arrays of electrodes
  - Single-sided strips, double-sided strips and pixel geometries
  - Since 1990s
  - O(100k) measurements per second

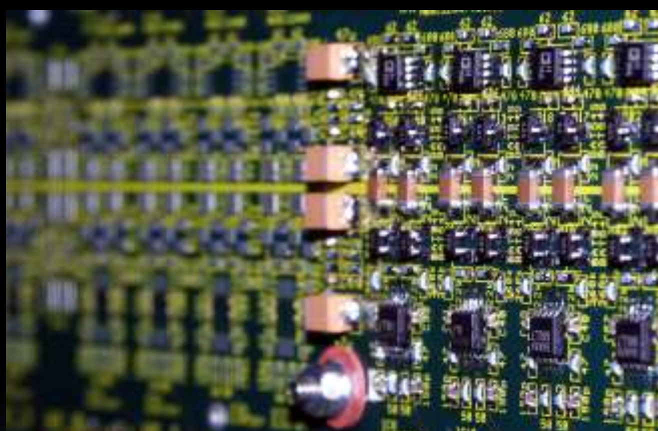






Modern Detectors 3/3

- What do those modern detectors have in common?
- Their output are electrical signals
- Lots of electronics involved



Why Electronics?

- Measure signals from a detector
  - Amplitude
  - Timing
  - Rate
  - …

- **Amplification**, processing, storage of analog signals
- **Digitization**
- **Processing**, storage of digital signals

Ideal Electronics

- We want to have
  - **Amplification**: perfectly linear, infinitely fast, noise-free
  - **Digitization** with infinite speed and as many bits as we can
  - **Processing** with infinite speed, bandwidth and complexity

- German saying: "wool-milk-pig laying eggs"
  - *jack of all trades device*

Back to Reality

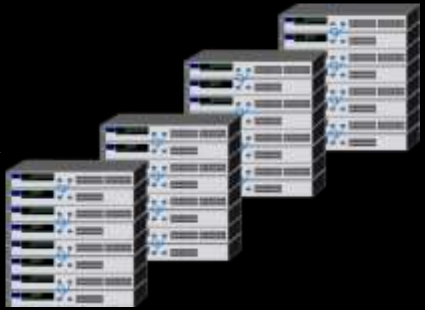
- What we really get
  - Amplifiers always have limited linearity and speed, noise largely depends on bandwidth (faster $\equiv$ noisier)
  - Digitization speed and number of bits are contradictory
  - Processing of course has speed, bandwidth and complexity limitations




Where Is It?

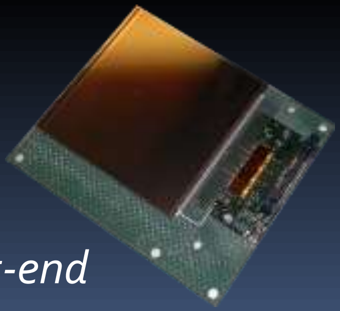
Detector
front-end

Electronics



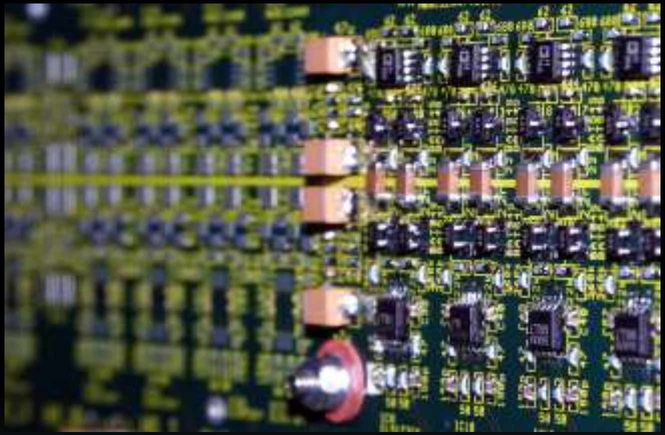
Server Farm / DAQ
back-end

Typically split into 2 parts:



front-end

back-end



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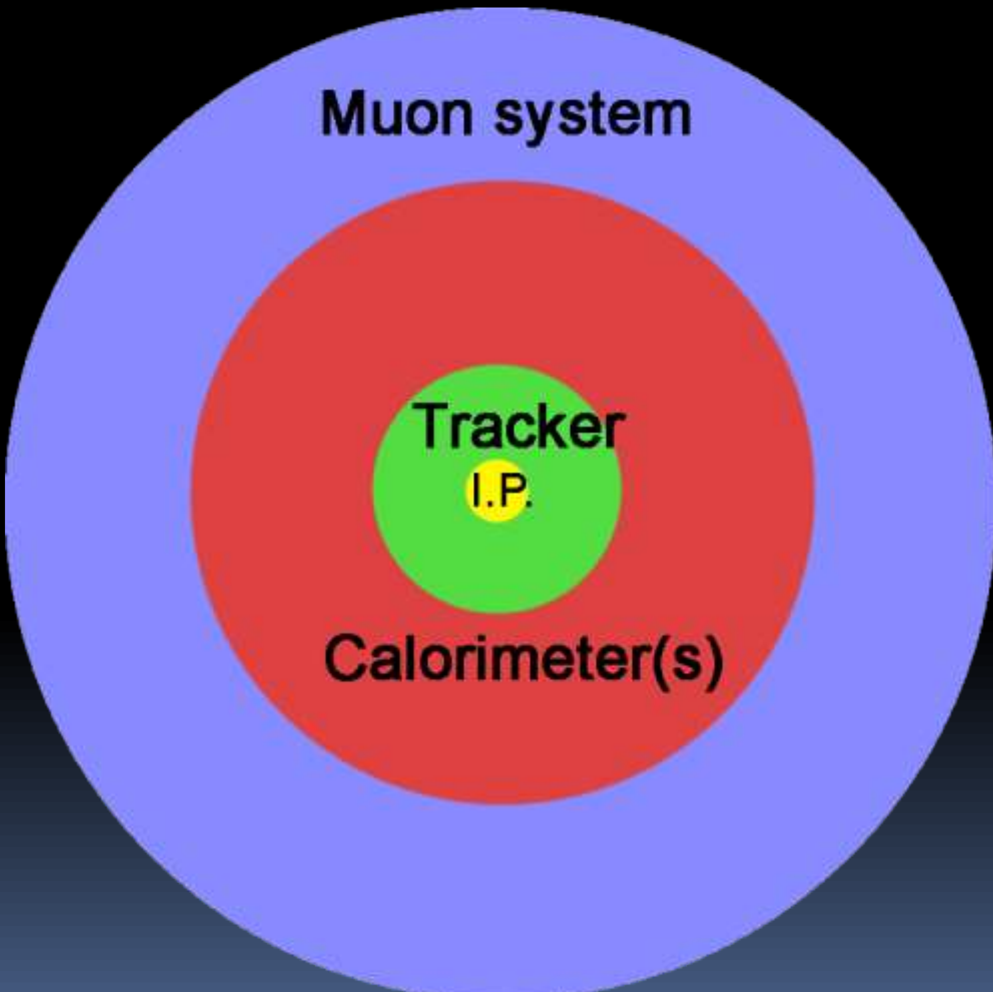
Concentric Layout

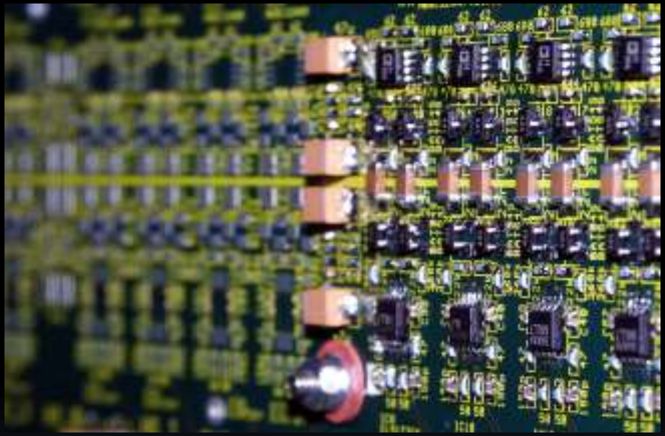


- General detector layout is concentric
- From inside to outside:
  - Interaction point
  - Tracker
    - Silicon/gaseous
  - Calorimeter
    - Electromagnetic
    - Hadronic
  - Muon Detector

Sensor Types

- Ionization (Electrical) – directly
  - Silicon detectors (pixel, strip)
  - Wire chambers (MWPC, TPC, RPC)
- Optical (Photons) – needs photon detector
  - Scintillator
  - Ring-Imaging Cherenkov (RICH)
  - Transition Radiation Detector (TRD)
- Thermal – needs SQUID: Bolometer

- Tracker
  - Silicon
  - Wire Chambers
- Calorimeter
  - Often scintillator, but also others
- Muon Detector
  - Wire chambers



Tracker: Pixels

- Silicon detector segmented in pixels
  - Typical cell size < 100 x 100 μm^2
  - Lots of readout channels $\rightarrow$ high power & cost / area

- Two basic types
  - Hybrid: sensor and electronics are two different pieces bonded together
    - Pro: each manufactured in optimal process, radiation hard
    - Con: much material, difficult to assemble
  - Monolithic: all-in-one, typically using epitaxial layer
    - Pro: little material, easier to produce
    - Con: long integration time, low radiation resistance

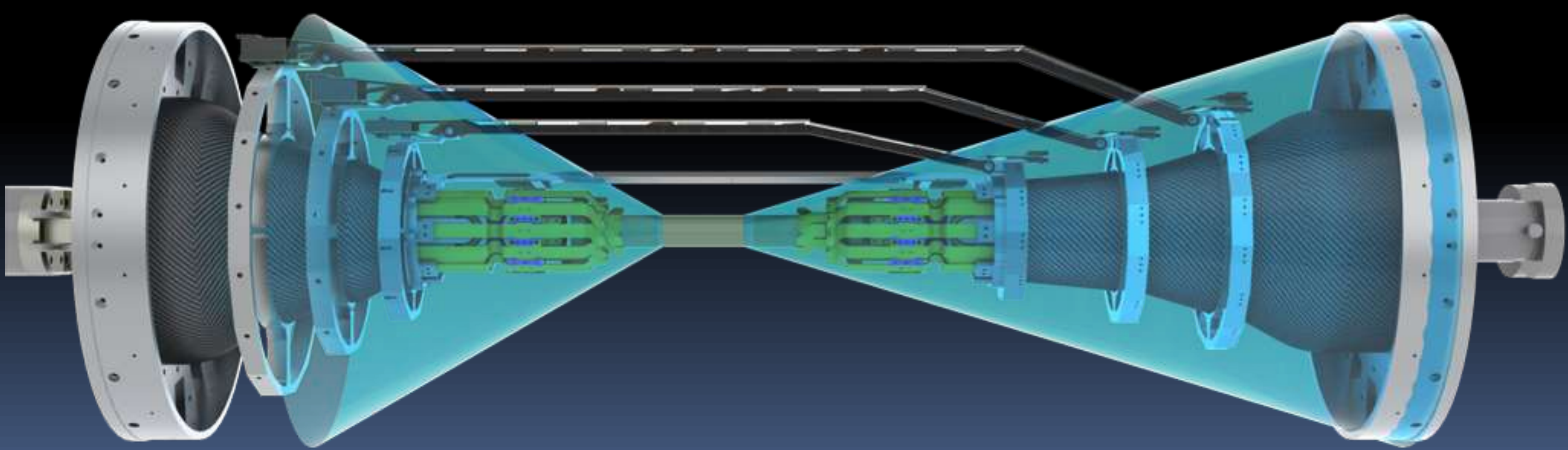
What Is the Material Budget?

- The ideal tracking detector is made of **nothing**
- Any real material interacts with the particle
  - Necessary for detection
  - Not desirable because of potential deflection

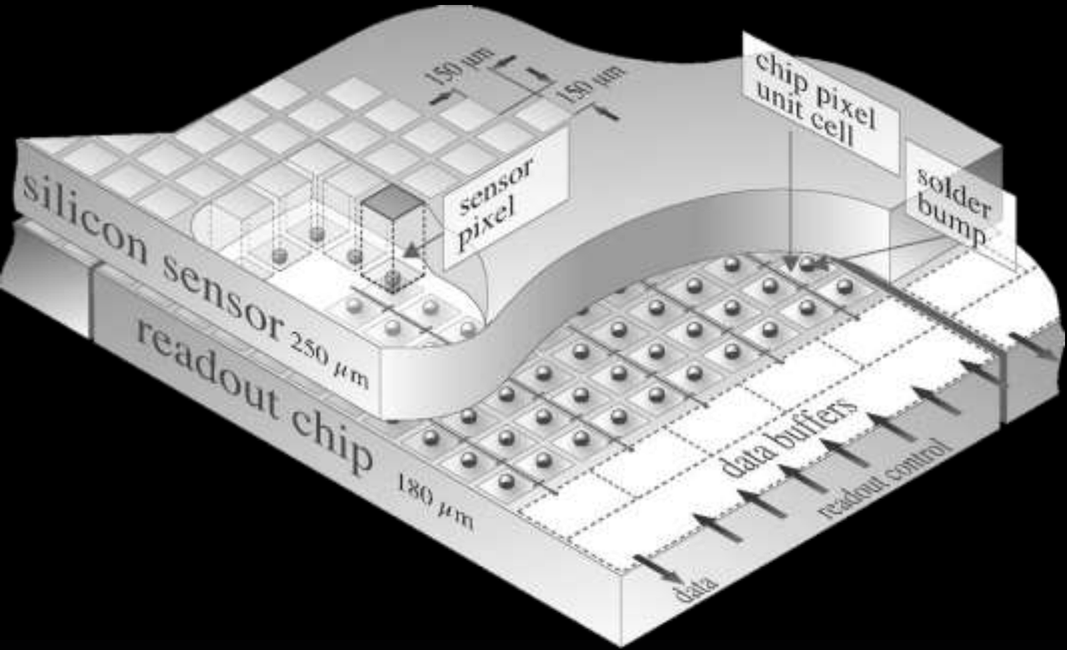
- Material budget:
  - Given as a fraction of X_0 = radiation length
  - Multiple scattering depends on amount of material in units of X_0
  - Example: 300 µm silicon $\equiv$ 0.32% X_0
  - Important especially for low-energy experiments, because scattering is also energy-dependent

Hermetic vs. Non-Hermetic

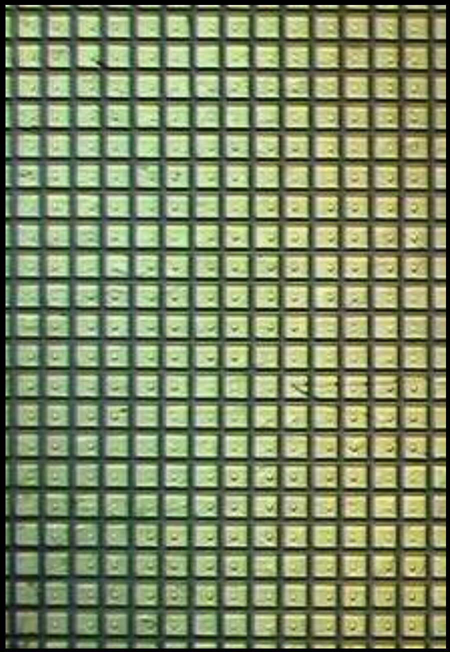
- A hermetic detector has an angular coverage of (almost) 4π
- That means material budget is important everywhere
- Special (low-energy) detectors are non-hermetic
  - E.g. Belle: 17…150° polar angle coverage
  - Heavy materials outside of the sensitive double cone



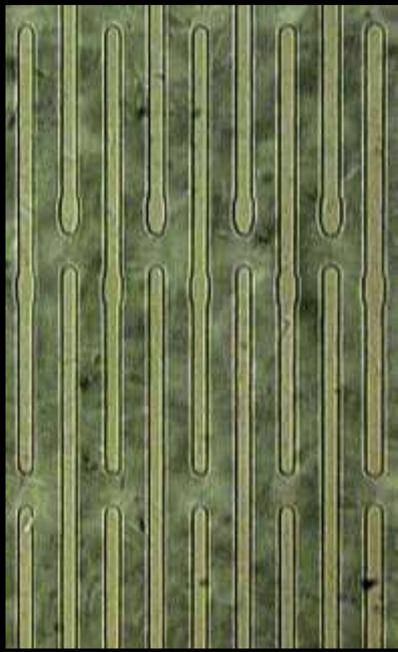
Hybrid Pixel Detectors



CMS Pixel Readout Scheme



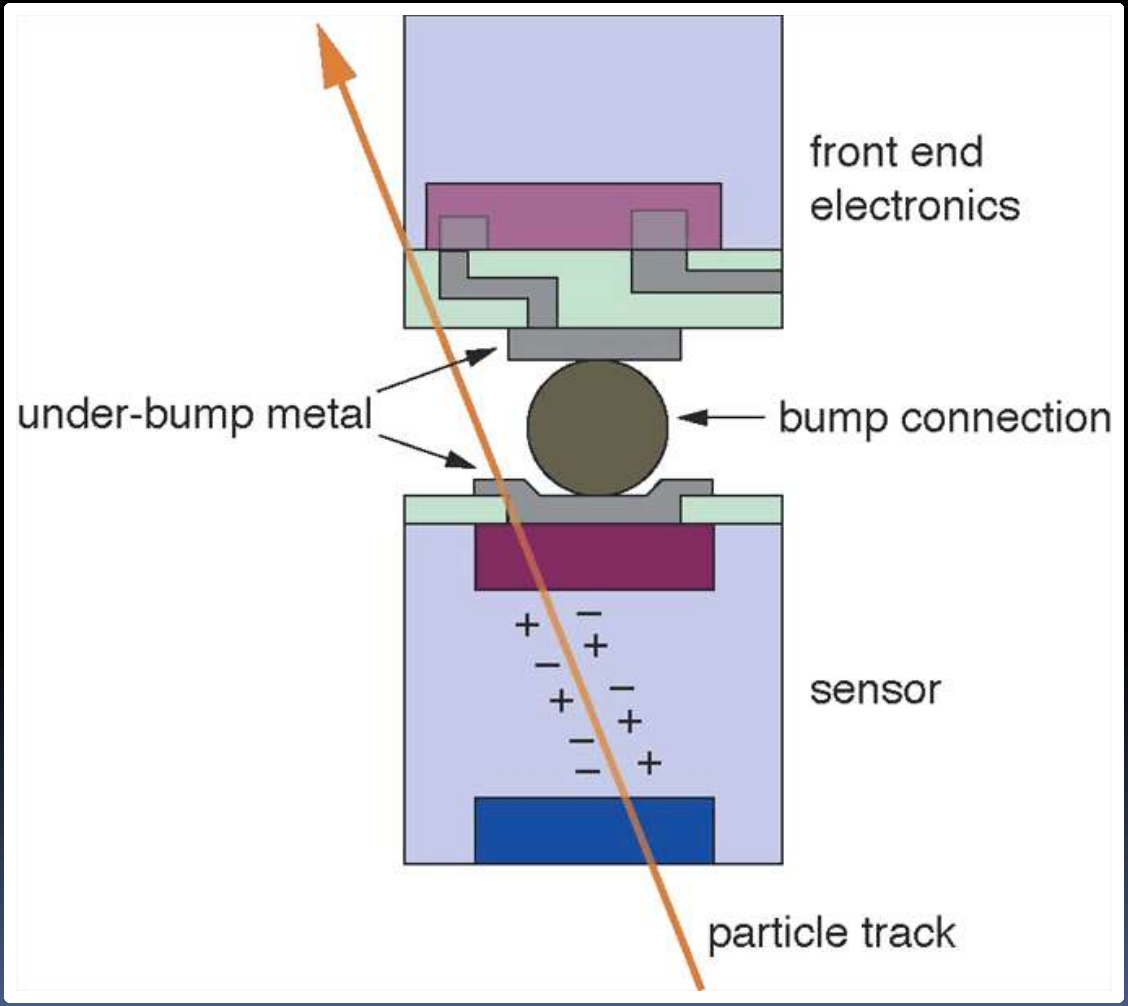
CMS Pixel Sensor

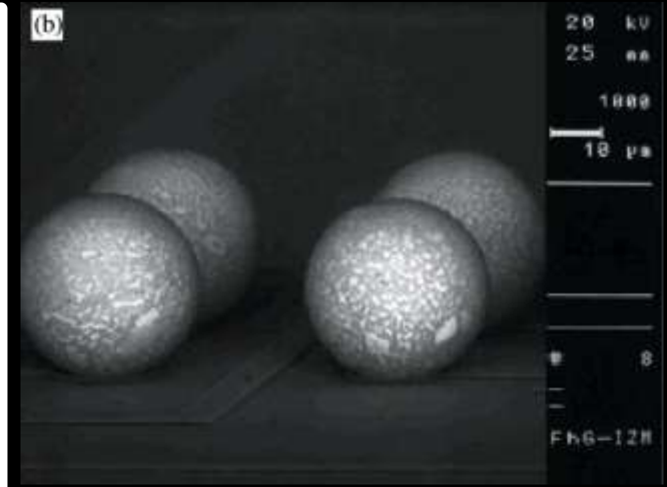


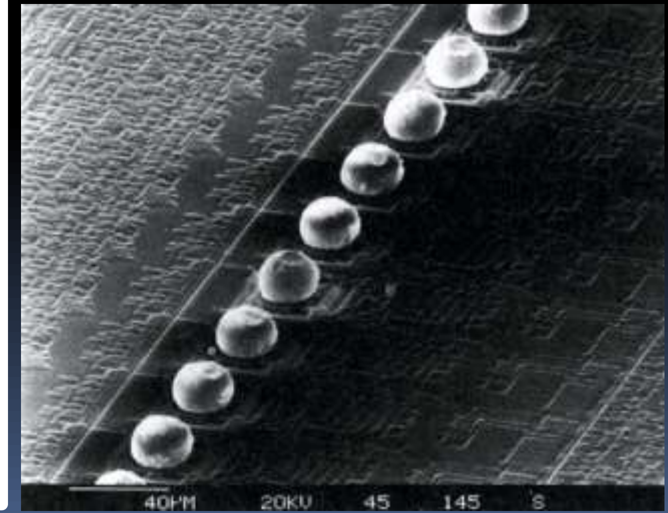
ATLAS Pixel Sensor

- Connection sensor to electronics by bump bonds
- Pixels can be square (CMS) or oblong (ATLAS)

Bump Bonding

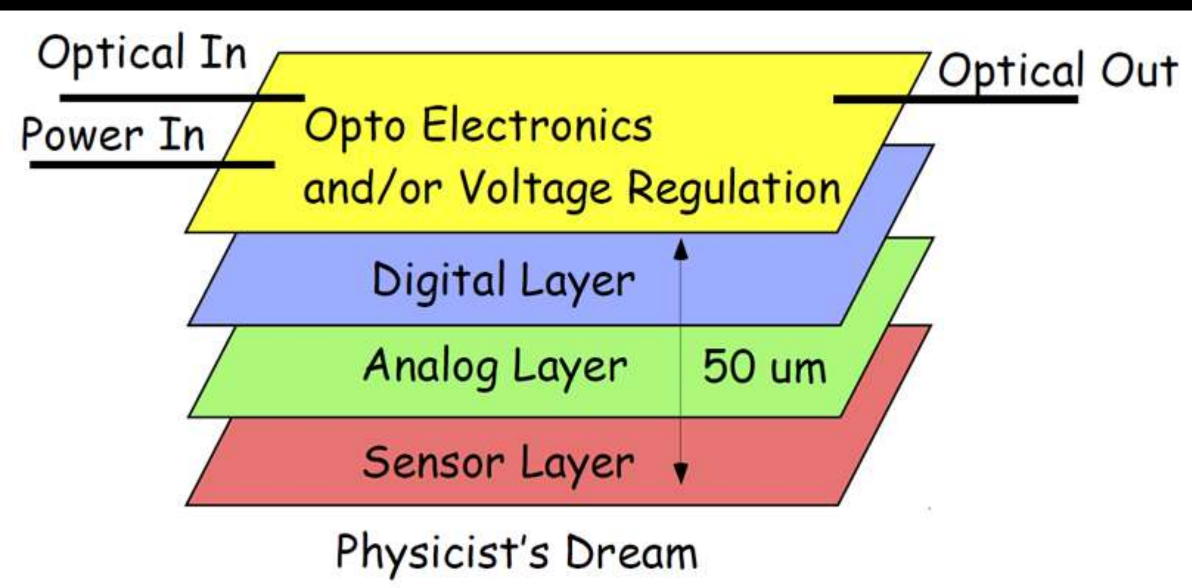


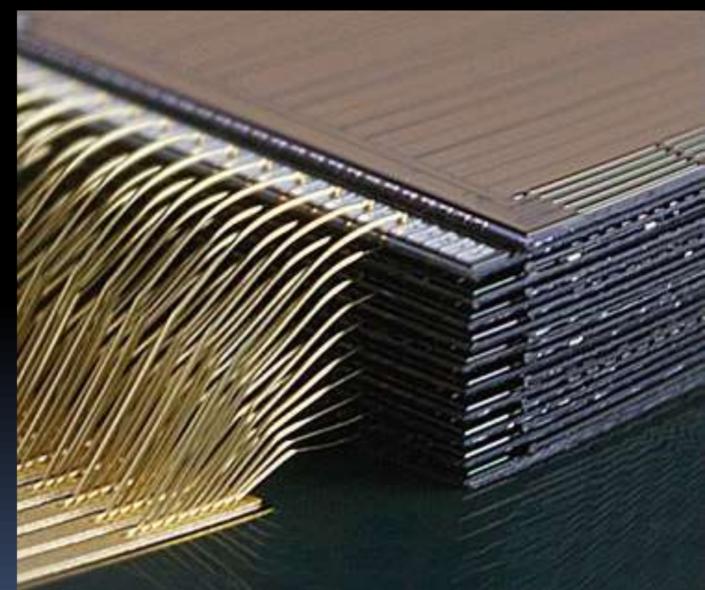




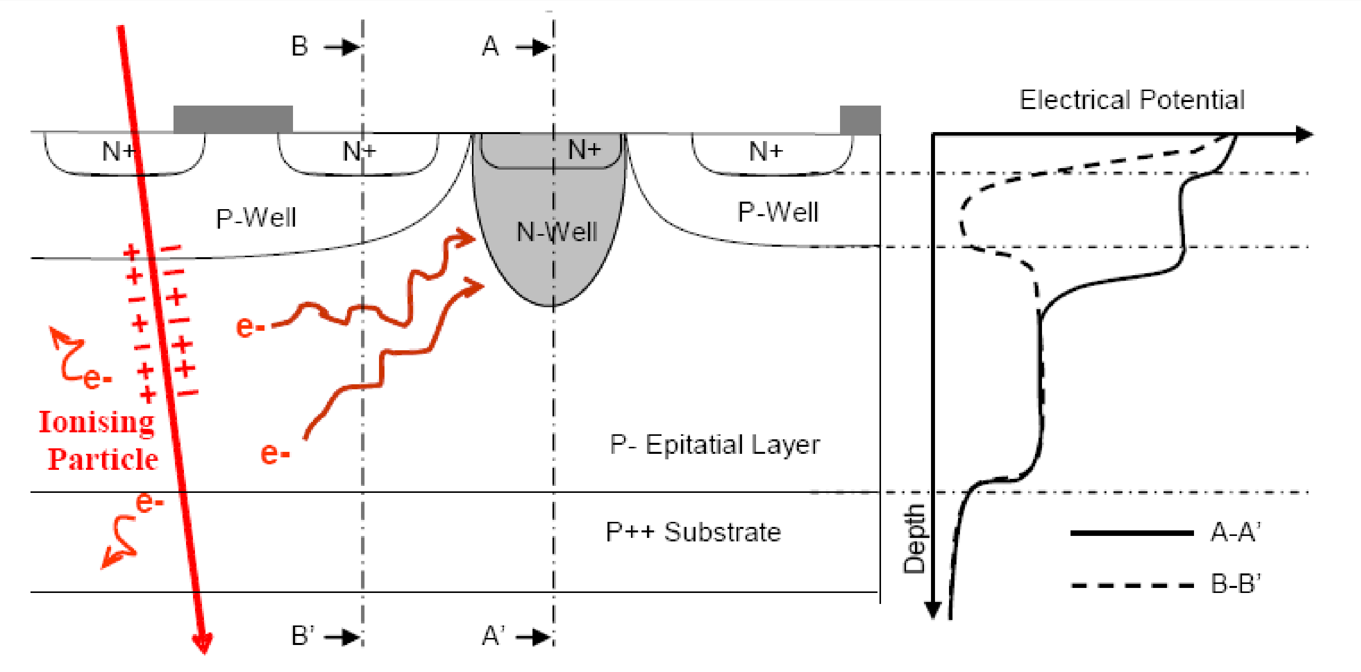
Stacking Multiple Chips?

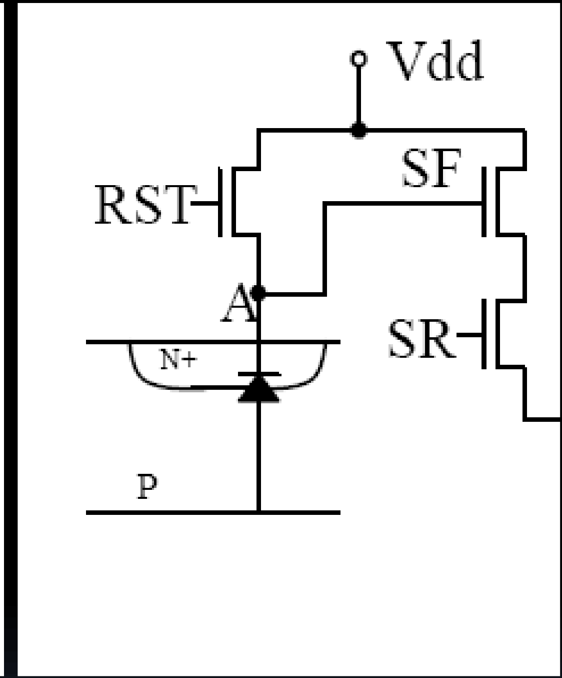
- 3D electronics: stacking multiple dies with different functions
  - Each layer could be made in the optimal technology
- Already done in industry (RAMs)





Monolithic Pixel Detectors



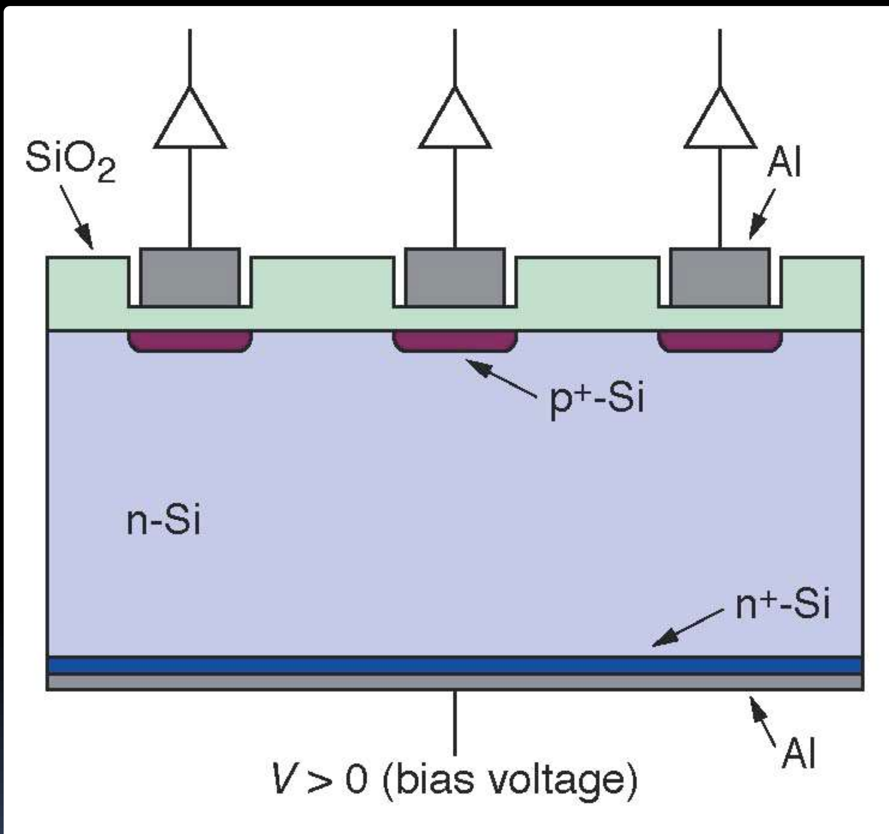


- Electrons move towards electrode by thermal diffusion
- Readout by simple 3-transistor cell
  - Small cell size (~20 x 20 µm²) possible → high spatial resolution

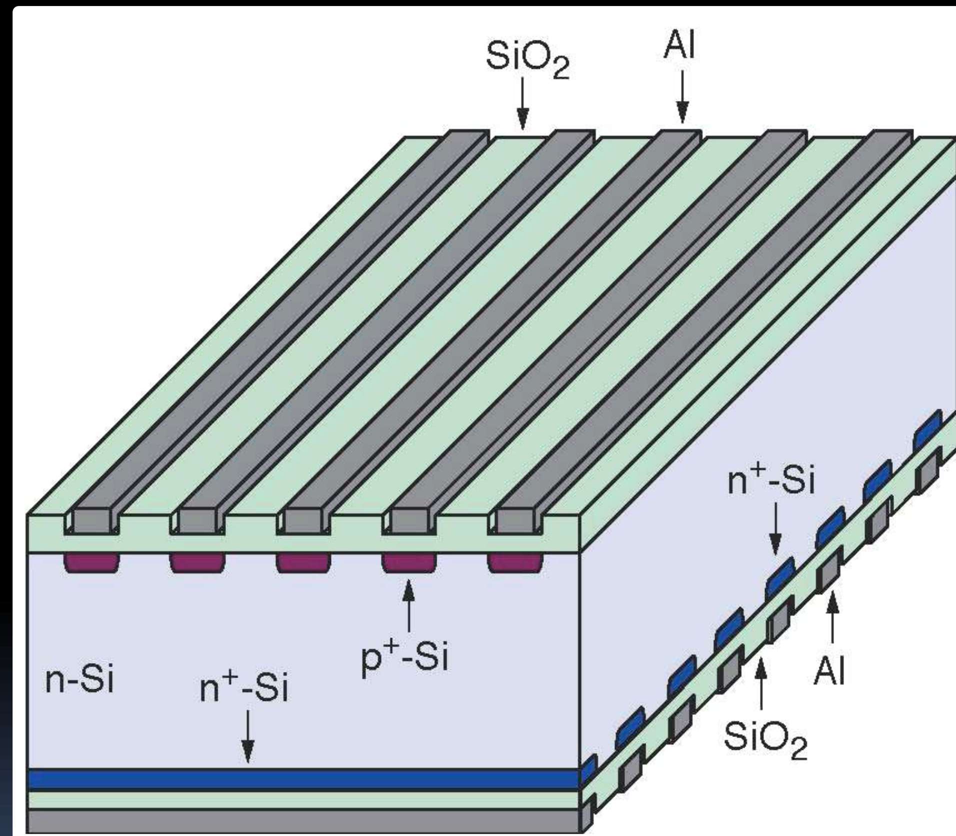
Tracker: Strips

- Silicon detector segmented in strips
  - Typical strip pitch O(100 μm)
  - Only N (instead of N^2) channels → cheaper than pixels
- Two types
  - Single-sided: backplane electrode is fully metallized
    - Pro: easy to manufacture, radiation hard
    - Con: higher material budget for "stereo" (=2 layers → 2D) readout
  - Double-sided: both electrodes have perpendicular strips
    - Pro: little material
    - Con: less radiation tolerance, at least one side not at ground

Single-Sided vs. Double-Sided

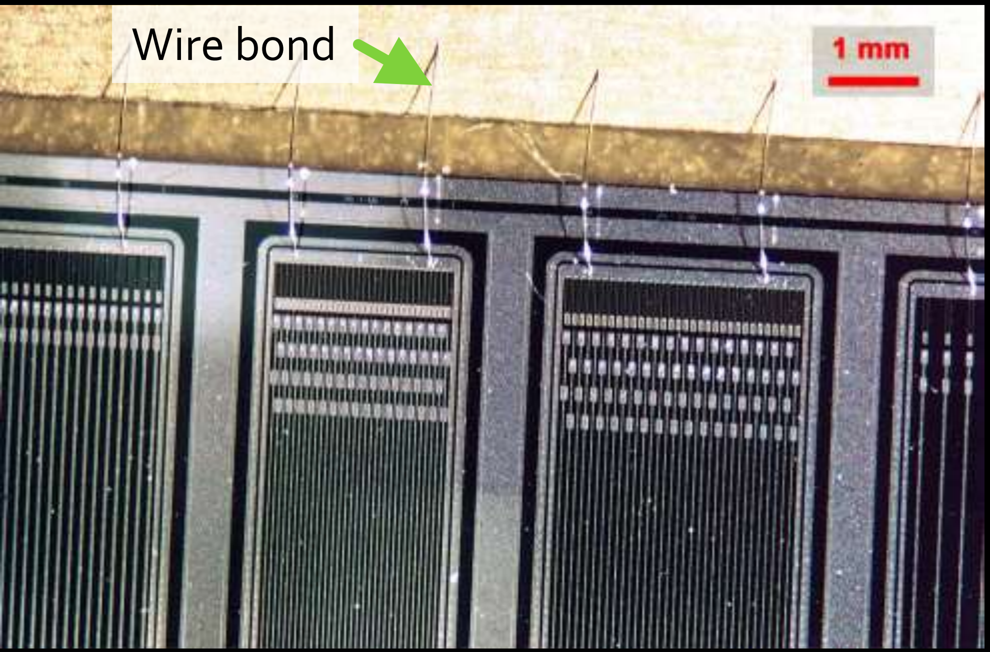


Fully metalized backplane

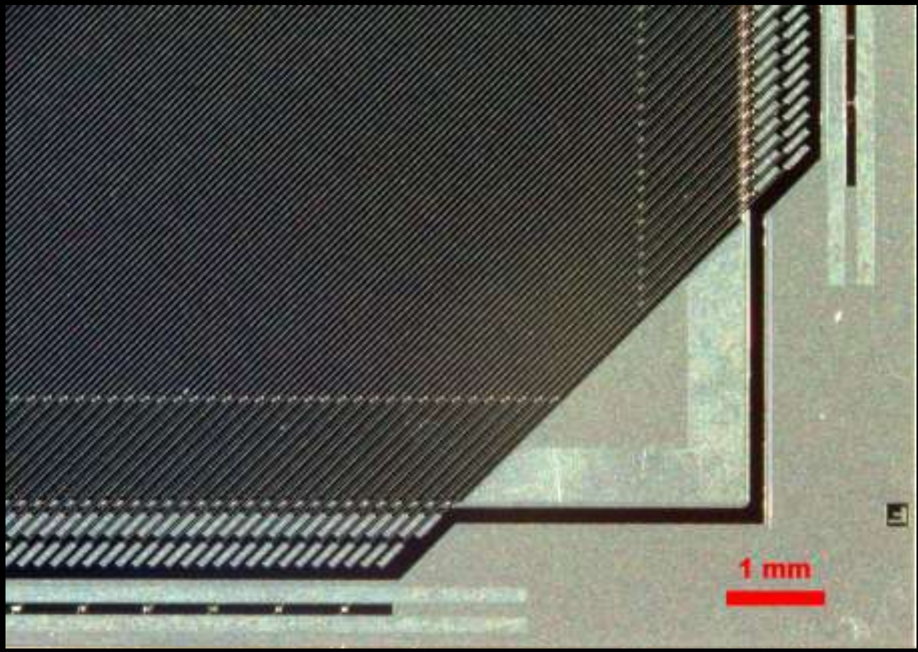


Strips on both sides

Silicon Strip Detectors



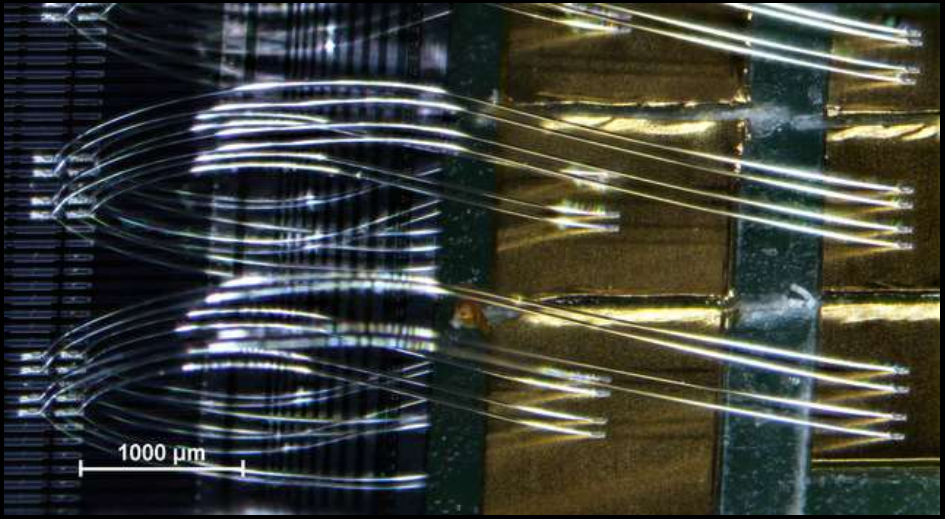
CMS Test Sensor with various geometries (1998)

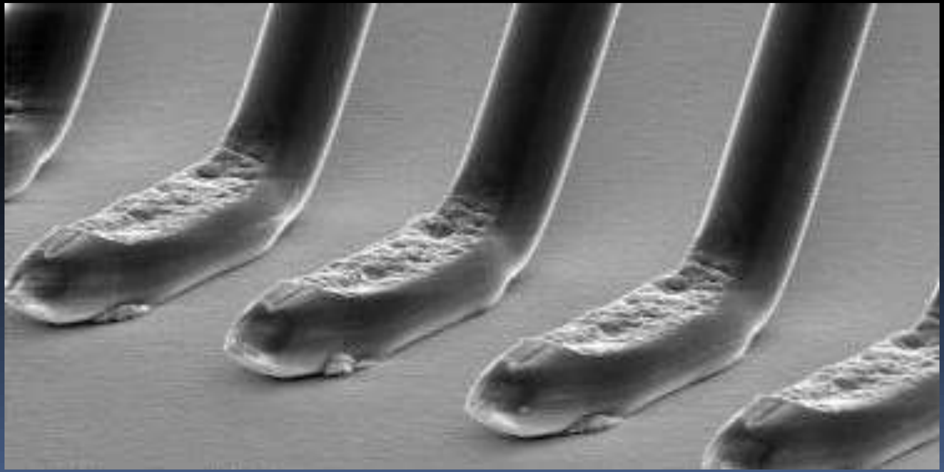


Belle Sensor with 45° strips (2004)

- Typically 300µm thick, strip pitch 50…200µm
- Reverse bias voltage for full depletion 50…500V
- Connection by wire bonds

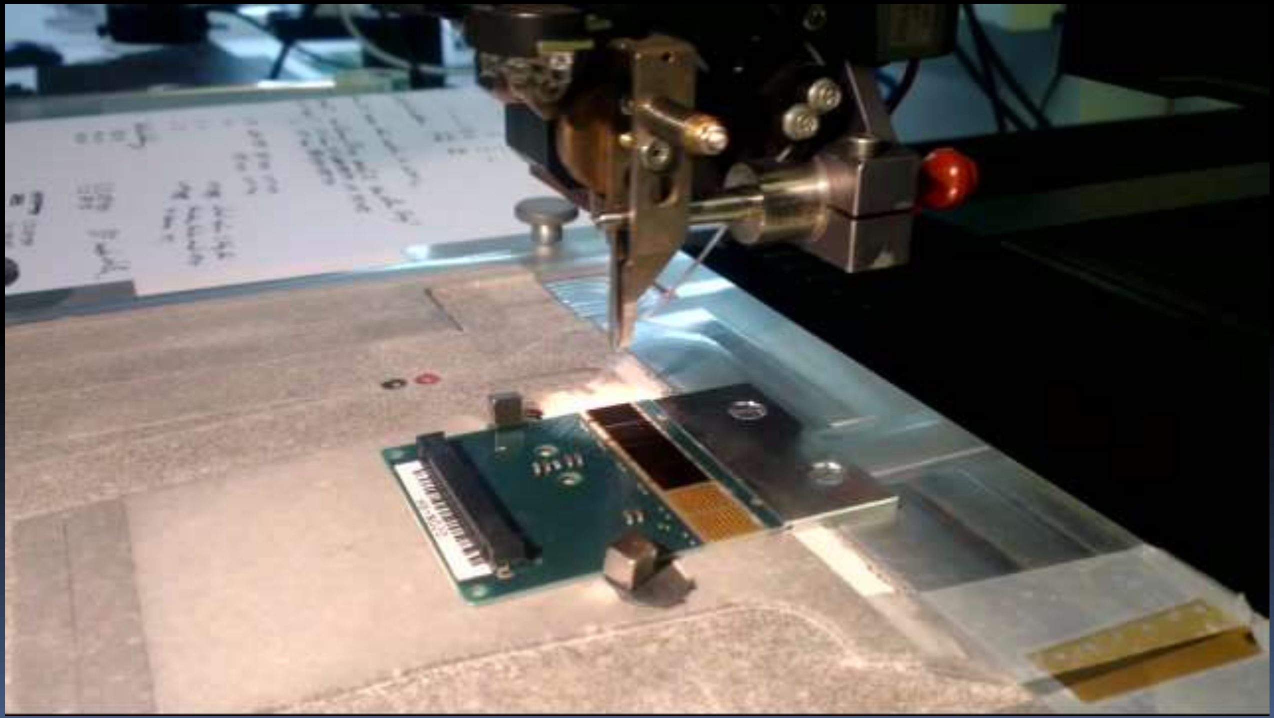
Wire Bonding Machine





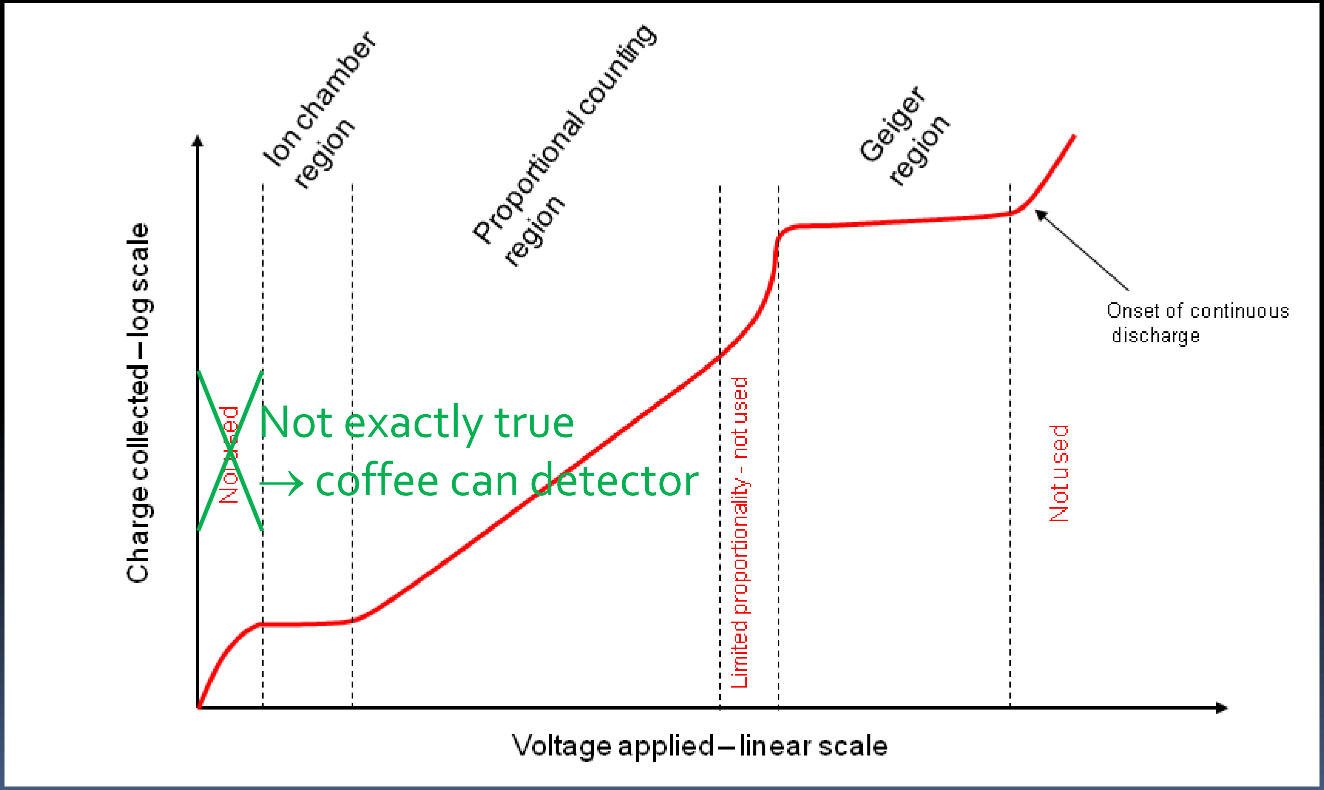
Wire Bonding

- Microscopic kind of sewing machine
- Aluminum (or gold) wire (typical diameter: 25µm) is connected to pads by ultrasonic welding



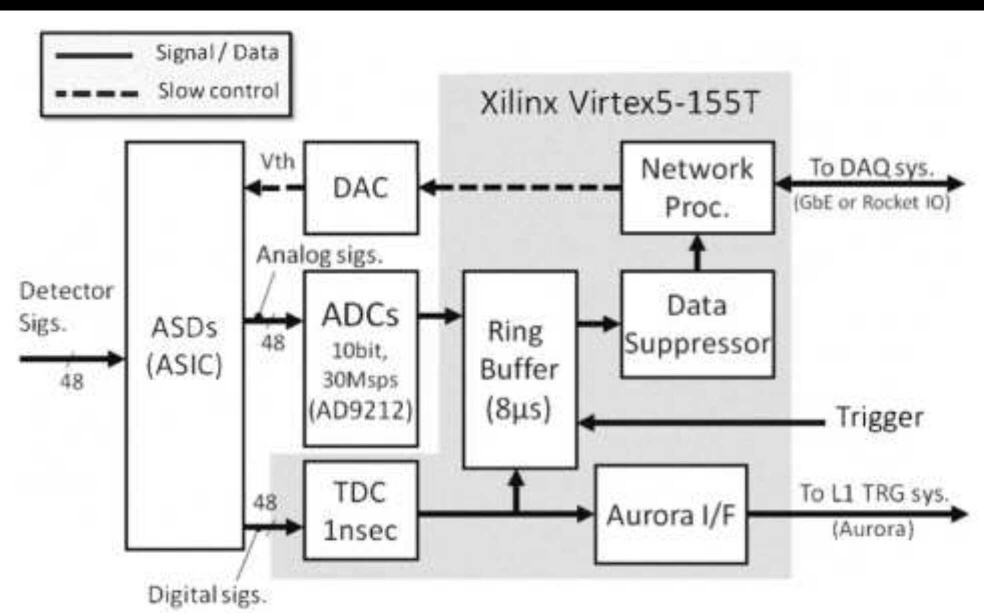
Gas Detectors

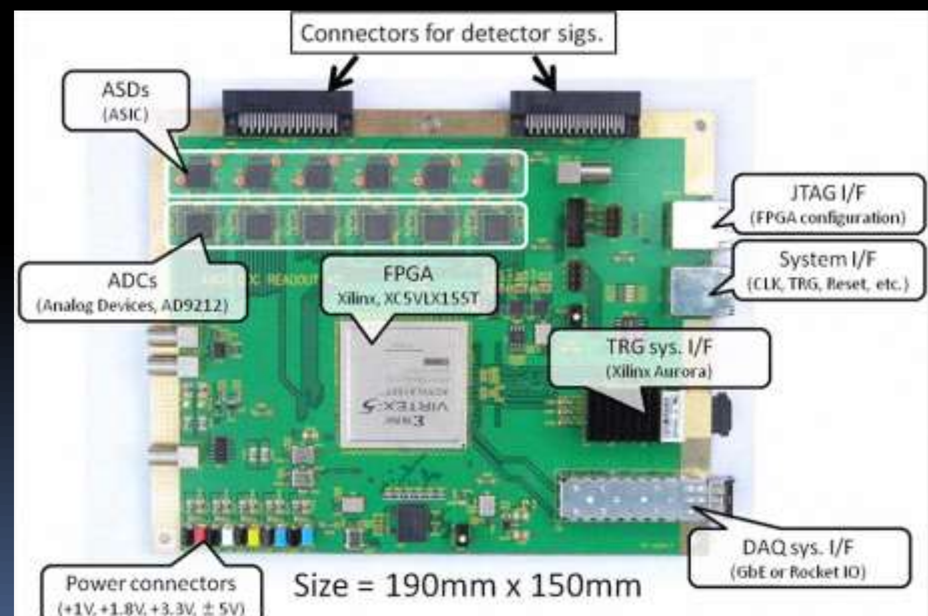
- Various types already mentioned in the beginning
- Operation mode depends on electric field



Example: Belle II Central Drift Chamber

- Gas mixture: helium – ethane (50:50)
- MWPC (proportional mode)
- Uses Amp-Shaper-Discriminator chips (ASDs) ASICS and commercial electronics including FPGA

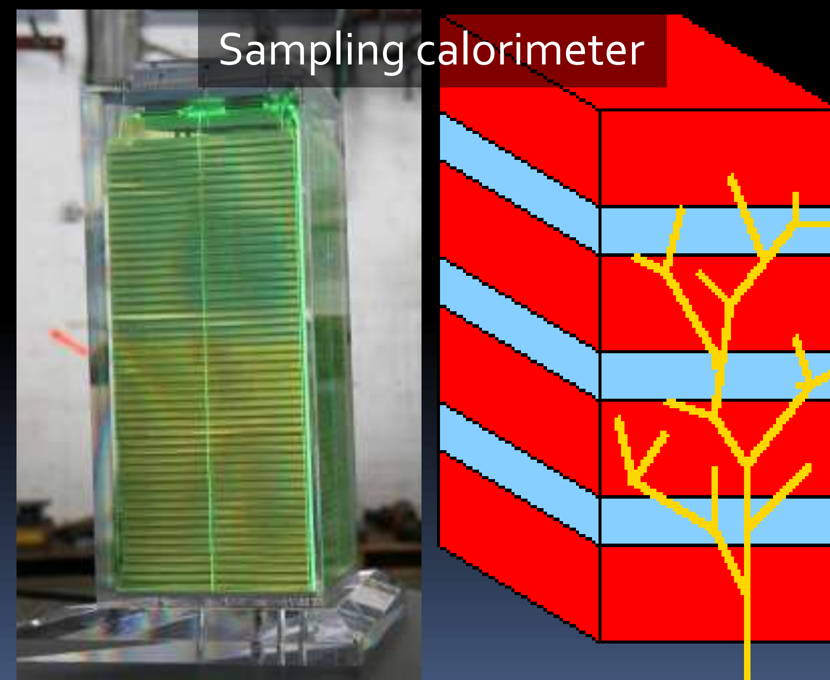




Calorimeter

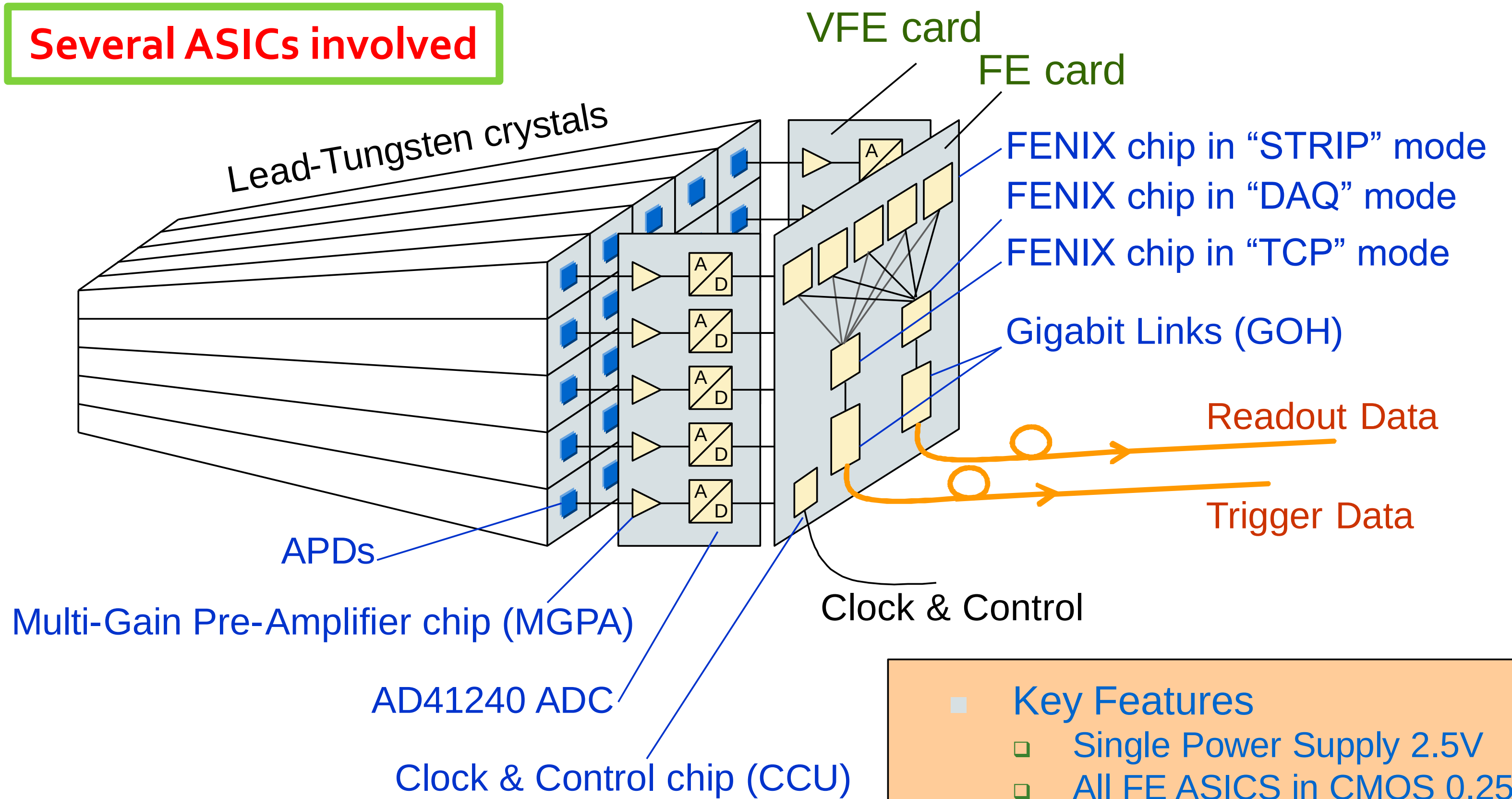
- Two types:
  - Homogenous (absorber = sensitive material), e.g. CMS ECAL
  - Sampling (absorber and detector layers alternate), any HCAL


CMS ECAL: $PbWO_4$ (lead tunstate) crystals


Sampling calorimeter

Example: CMS ECAL Readout

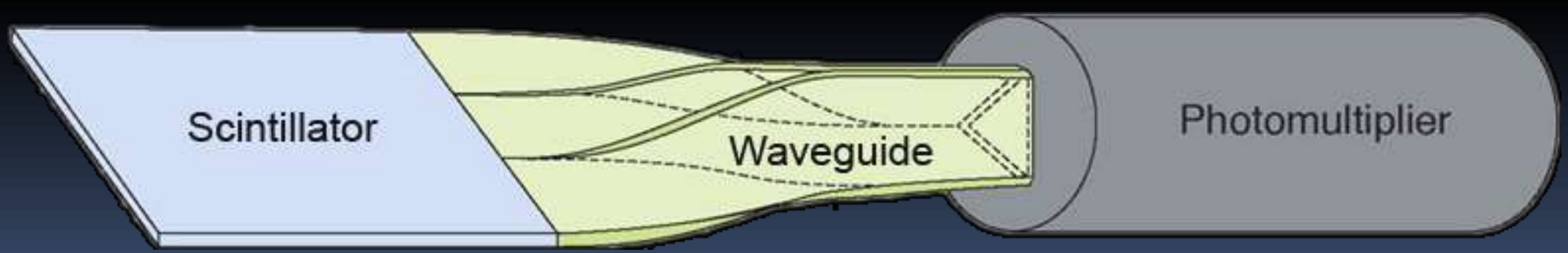
Several ASICs involved



- Key Features
  - Single Power Supply 2.5V
  - All FE ASICS in CMOS 0.25 µm Rad-Tol process

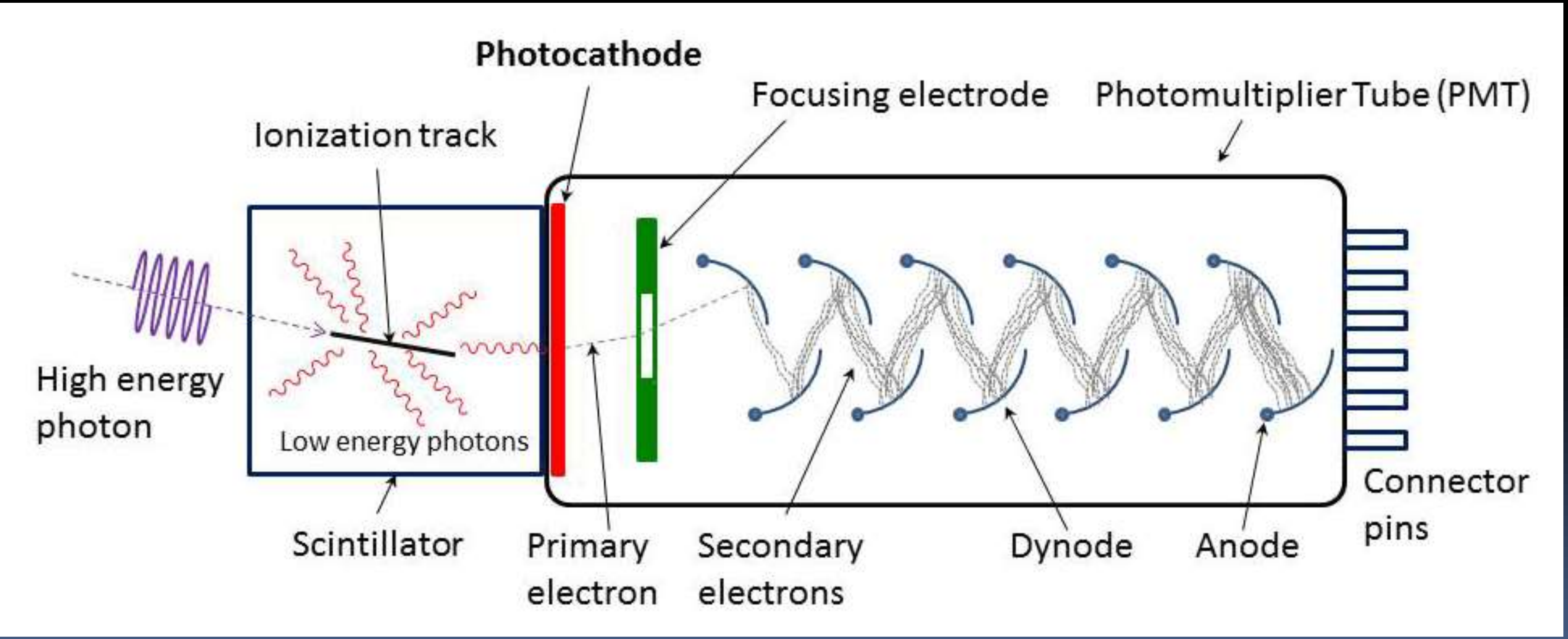
How to Measure Photons?

- Classical arrangement:
  - Scintillator – waveguide – photomultiplier
- Scintillator and waveguide are covered with reflective foil to achieve total reflection
- Everything must be completely light-proof
  - Want to measure scintillation photons, not daylight



Photomultiplier (PM) Tubes 1/2

- Photon extracts electron from photocathode (**Photo effect**)
- **Dynodes** with increasing potential accelerate electrons and knock out additional **secondary electrons** (amplification)



Photomultiplier (PM) Tubes 2/2

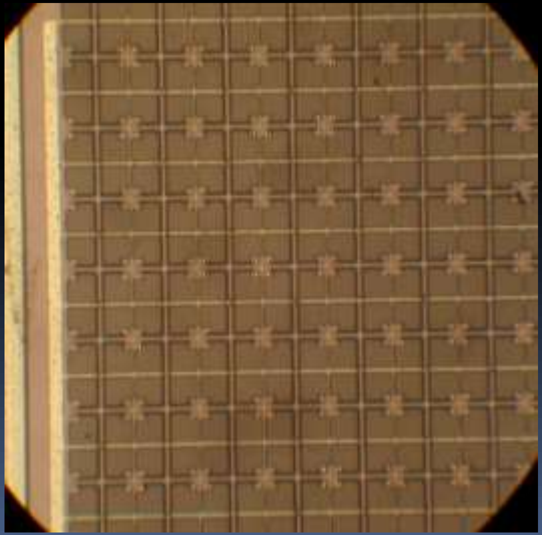
- Several **sizes** and types
- **Amplification** depends on the number of dynodes
  - Typically ~$10^6 \ldots 10^7$

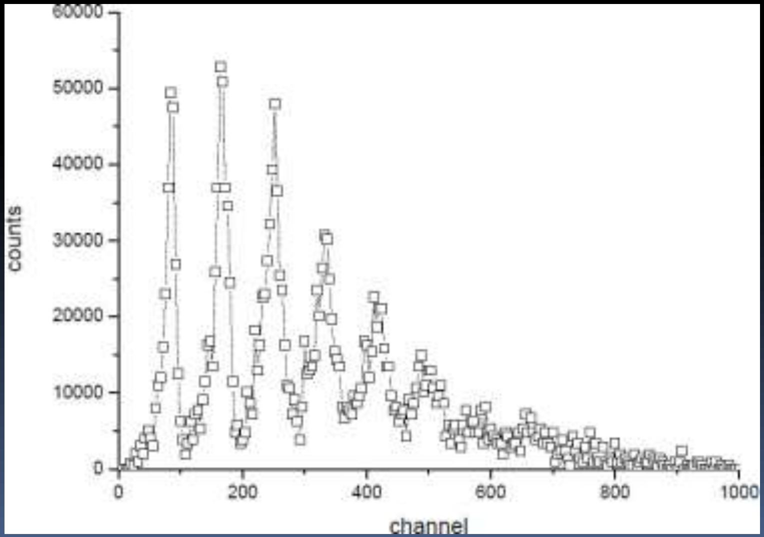
Photomultiplier Made of Semiconductors

- Traditional **PMs** have several cons:
  - Size, high voltage, magnetic field sensitivity
- **Semiconductor diodes** biased slightly under breakthrough
- **APD** = Avalanche Photodiode
- Active area up to 1 cm^2, amplification ~100
- Operating voltage < 500 V

SiPM = Silicon Photomultiplier

- **Array** of many parallel APDs on a chip
- (Discrete) **„analog“ signal** according to the number of incident photons
- Operating voltage < 100 V (Geiger mode)
- Single photon detection



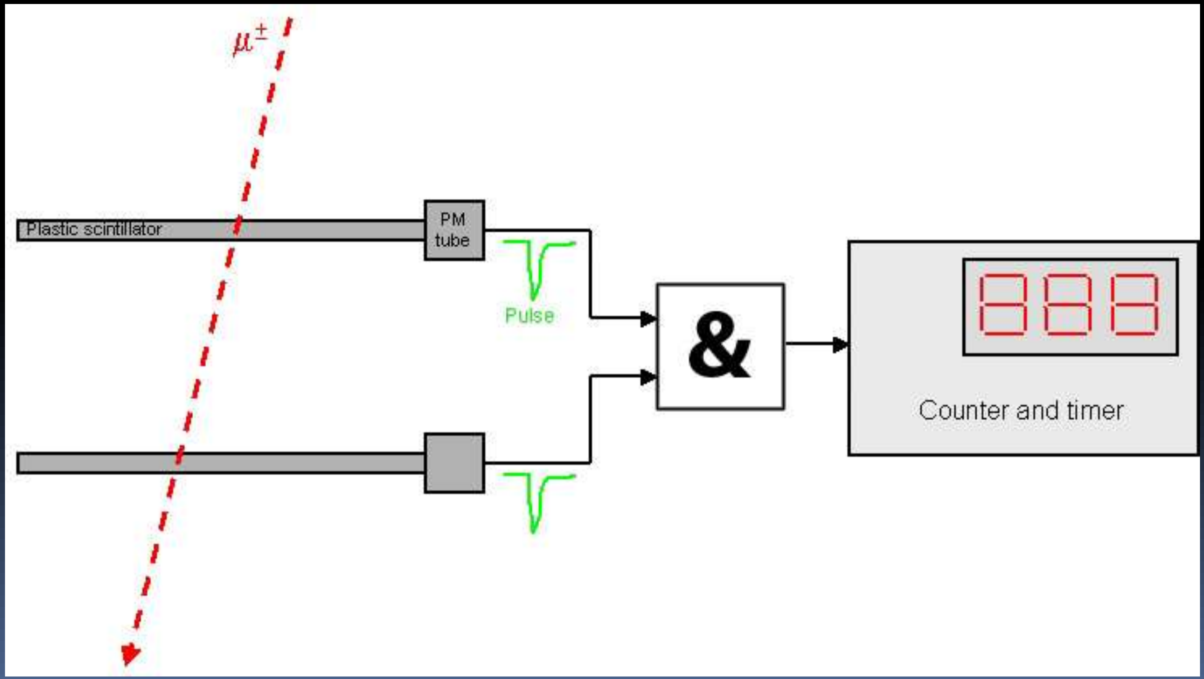


Comparison of Photodetectors

	PM	APD	SiPM
Amplification	$10^6 \ldots 10^7$	~100	$10^5 \ldots 10^6$
Operating voltage	1…2 kV	300…500 V	<100 V
Active area	<200 cm²	<100 mm²	~1 mm²
Dark rate	~1 kHz	-	~1 MHz
Photon efficiency	~30%	~80%	~50%
Magnetic field tolerance	✗	✓	✓

Is the Dark Rate a Problem?

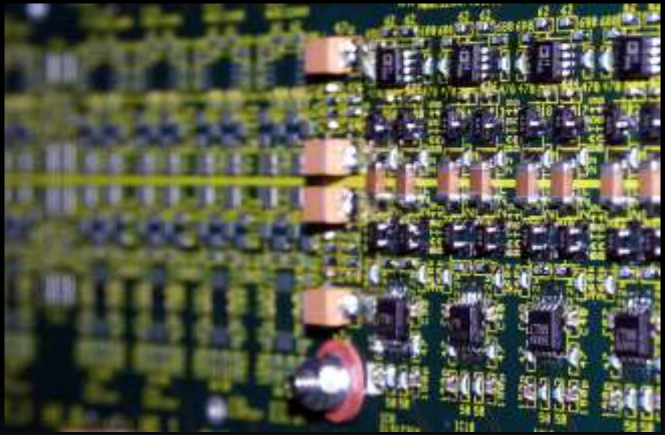
- Thermal **Noise**: A single (Si)PM also delivers counts in absolute darkness
- **Trick**: Using 2 (or more) (Si)PMs and looking at the ANDed signal (**coincidence**)



Detector Summary

- ASICs and specific developments everywhere
  - There is no jack of all trades device

- General issues in front-end:
  - Radiation hardness
    - Only specifically developed active electronics (depending on location and experiment)
  - Magnetic field
    - No iron/ferrite core coils allowed (saturation), no magnetic parts
  - Space and power/cooling budget



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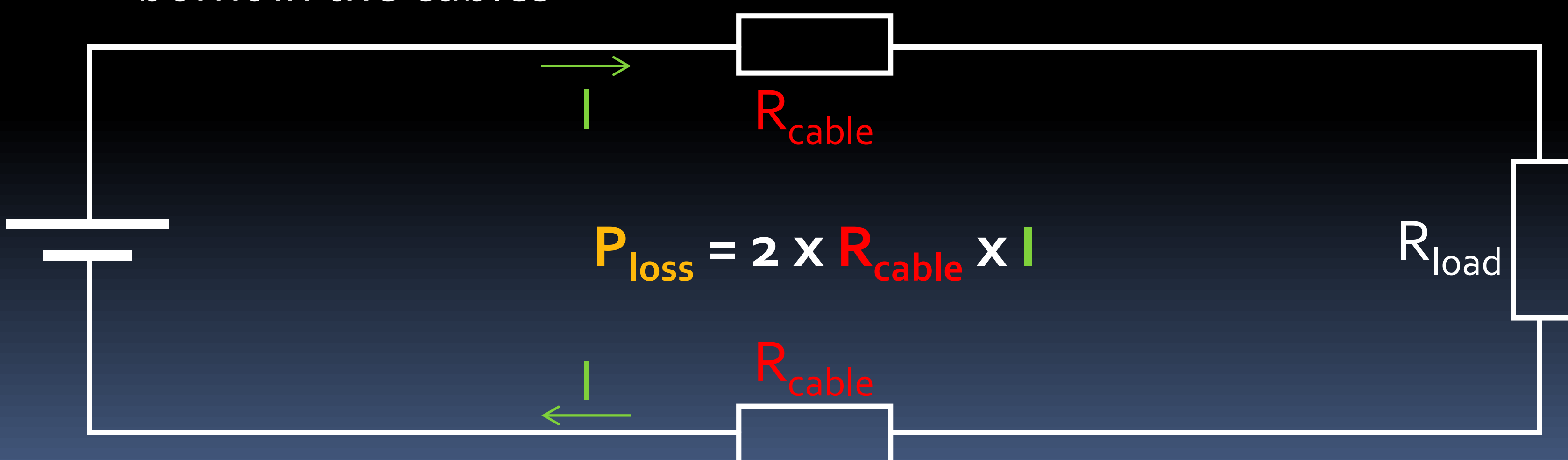
ASICs

- Chip feature size getting smaller and smaller (Moore's law)
  - Mask costs increase
  - Suitability for analog circuitry decreases
- Obsolescence problem
  - LHC ASICs were typically made in 250nm technology
  - Process not available anymore

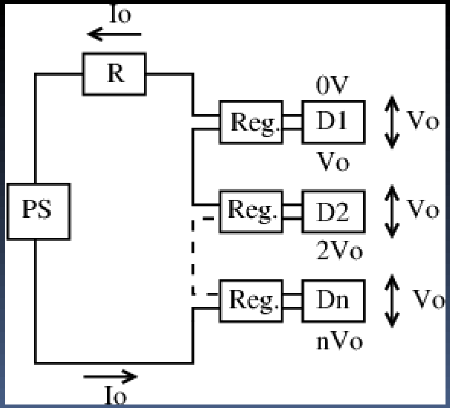
Powering: What's It All About?

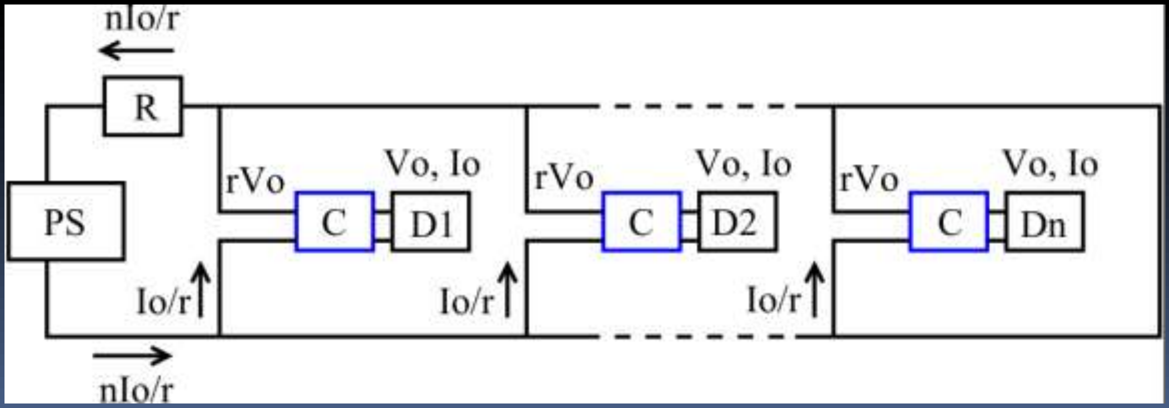
- We need to bring power to the front-end
- There can be a significant power drop in the cables
  - Limited space and material budget
  - Low voltages required by modern electronics
  - In CMS and ATLAS Trackers, ~50% of total power (tens of kW) is burnt in the cables



How to Avoid This?

- **Lower R_{cable}:** hardly possible ☹
- **Serial powering:** deliver constant current at higher voltage, needs shunt regulator for each serially connected unit
- **DC/DC converters:** deliver higher voltage, needs converter for each parallel unit
- Both methods reduce I and thus power loss at constant R_{cable}





Serial Powering vs. DC/DC Converters

- Both options have pros and cons and are intensively studied for S-LHC upgrades

- **Serial powering:**
  - no common ground: requires level translation for I/O
  - generally easier for digital output – ATLAS
- **DC/DC converters:**
  - switching device: requires careful design to avoid noise
  - generally easier for analog output – CMS

- Completely different concept (ILC): pulsed powering (1/200 duty cycle)

Cooling

- Front-end power should be minimized
  - But cannot be avoided
- Why?
  - Dissipated power needs to be removed
  - Necessity of cooling system
  - Adds material budget
- State-of-the art:
  - Two-phase CO_2
  - Pro: high efficiency, minimal material budget
  - Con: Complicated cooling plant, high pressure (~20bar)

Monitoring

- Measuring environmental conditions
- Requires (rad-hard) sensors for temperature, humidity, displacement, …
- Readout of those sensors is slow – O(1 Hz)
- Often neglected and started quite late…

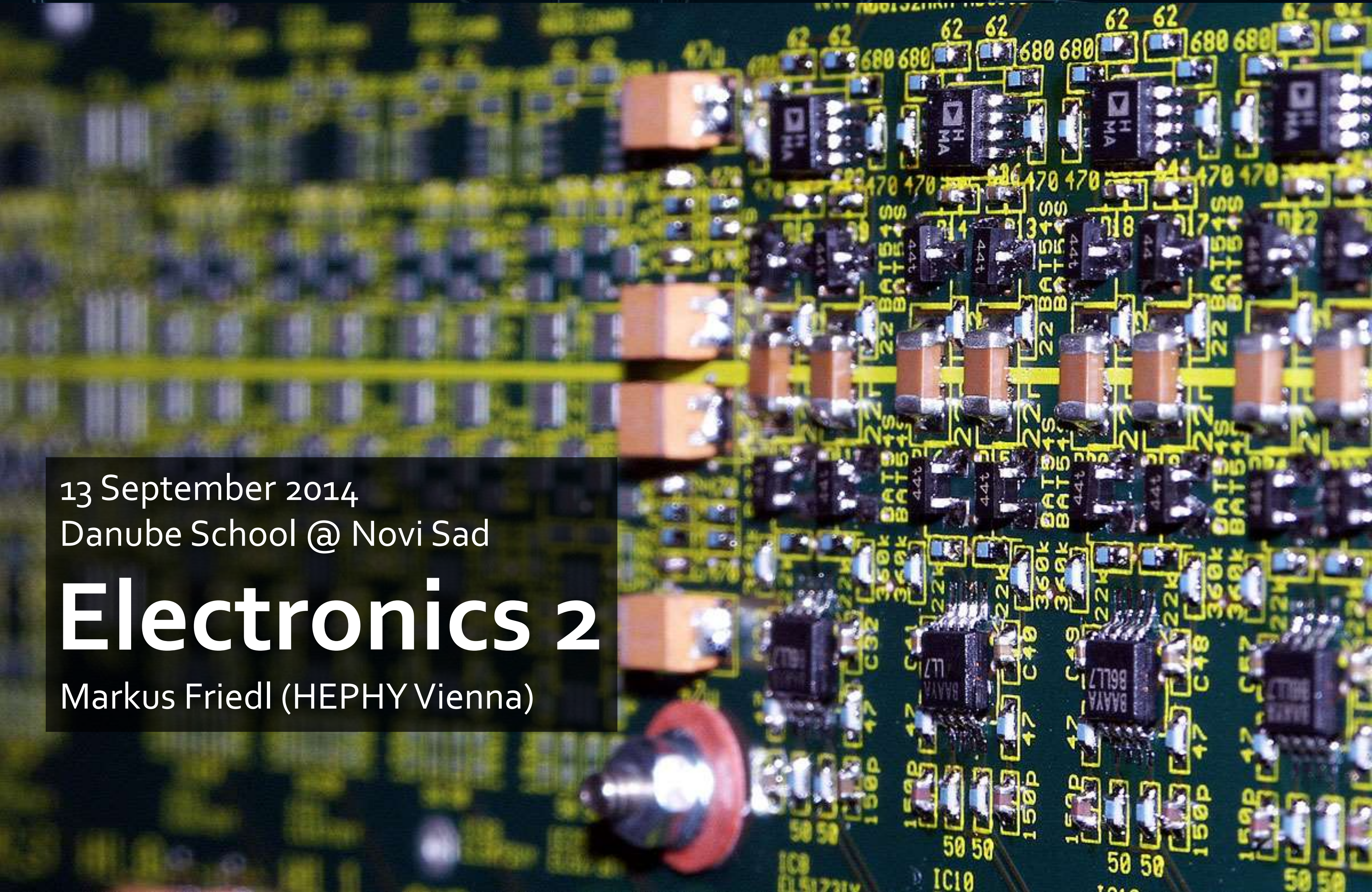
- Monitoring also includes data quality
  - Typically some histograms made with measurement data and compared to reference ones

What else?

Tomorrow, we will have a closer look onto a readout chain example.

HEPHY
Institute of High Energy Physics

ÖAW
Austrian Academy of Sciences

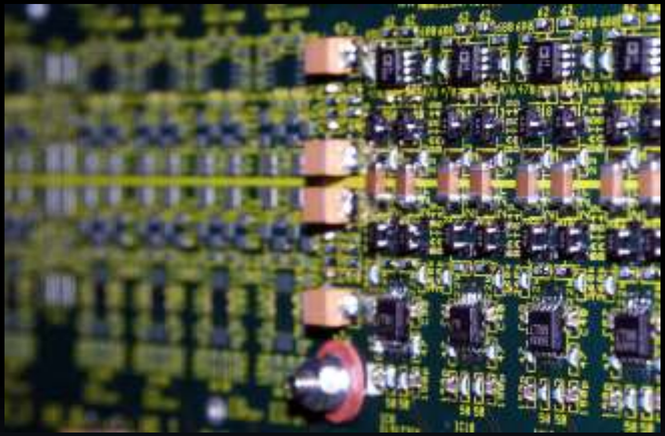


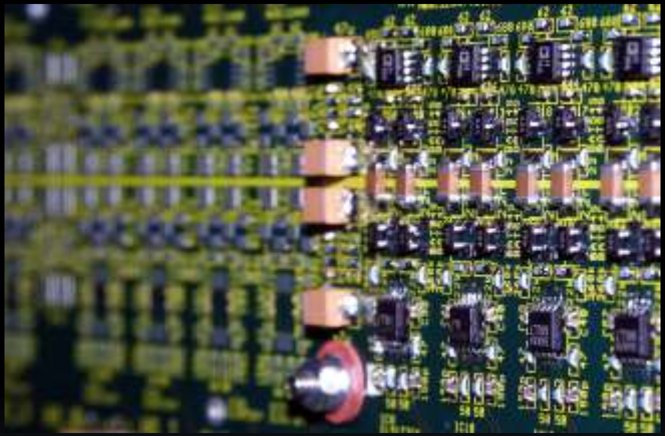
13 September 2014
Danube School @ Novi Sad

Electronics 2

Markus Friedl (HEPHY Vienna)

Contents





Typical Readout Chain

Readout Chain – Front-End

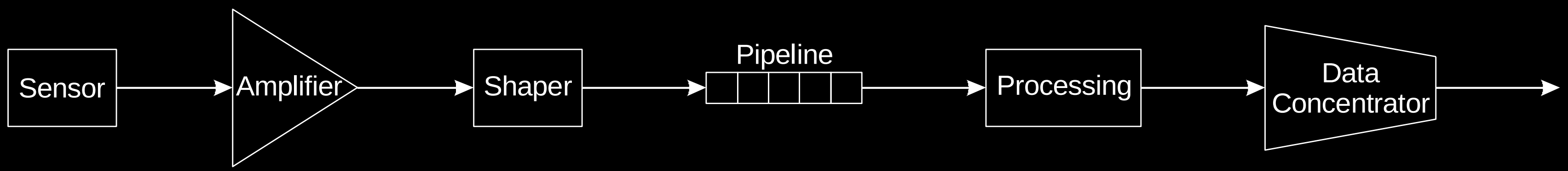
Signal Transmission

Readout Chain – Back-End

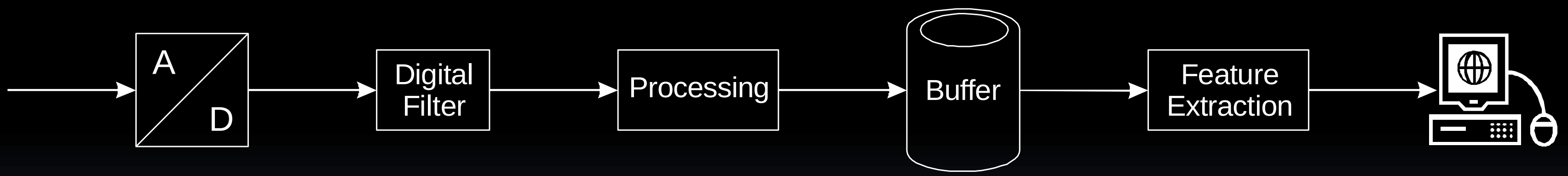
Additional Topics

Typical Readout Chain

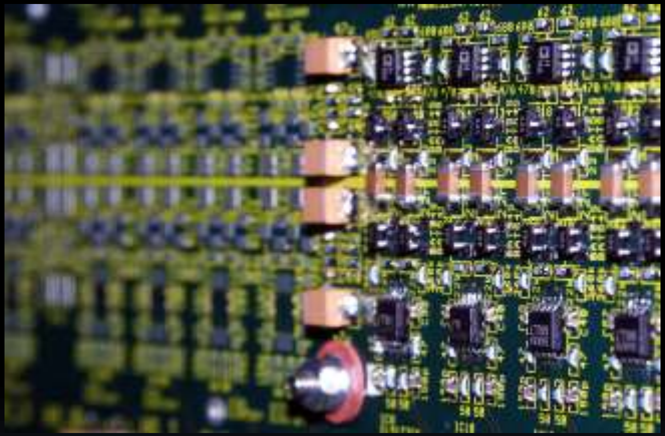
- Front-end part:



- Back-end part:

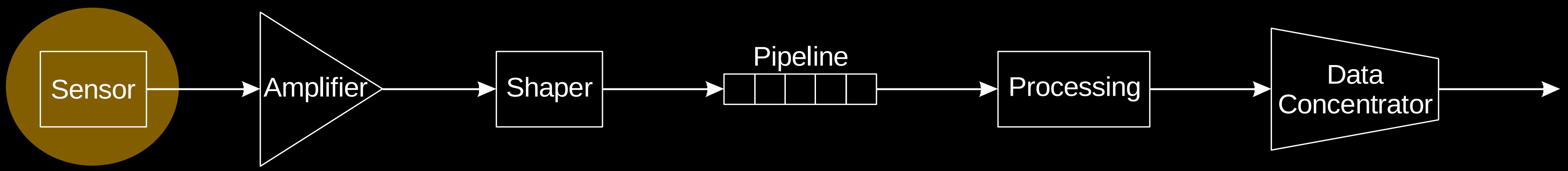


- This is just a typical example, not a law of nature
  - E.g., digitization may already happen in the front-end

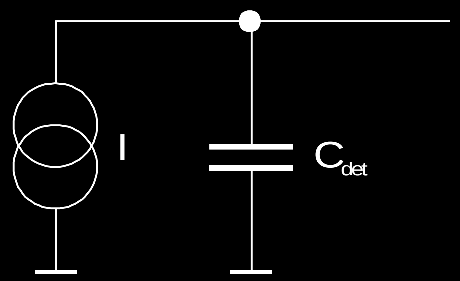


- Typical Readout Chain
- **Readout Chain – Front-End**
- Signal Transmission
- Readout Chain – Back-End
- Additional Topics

Sensor



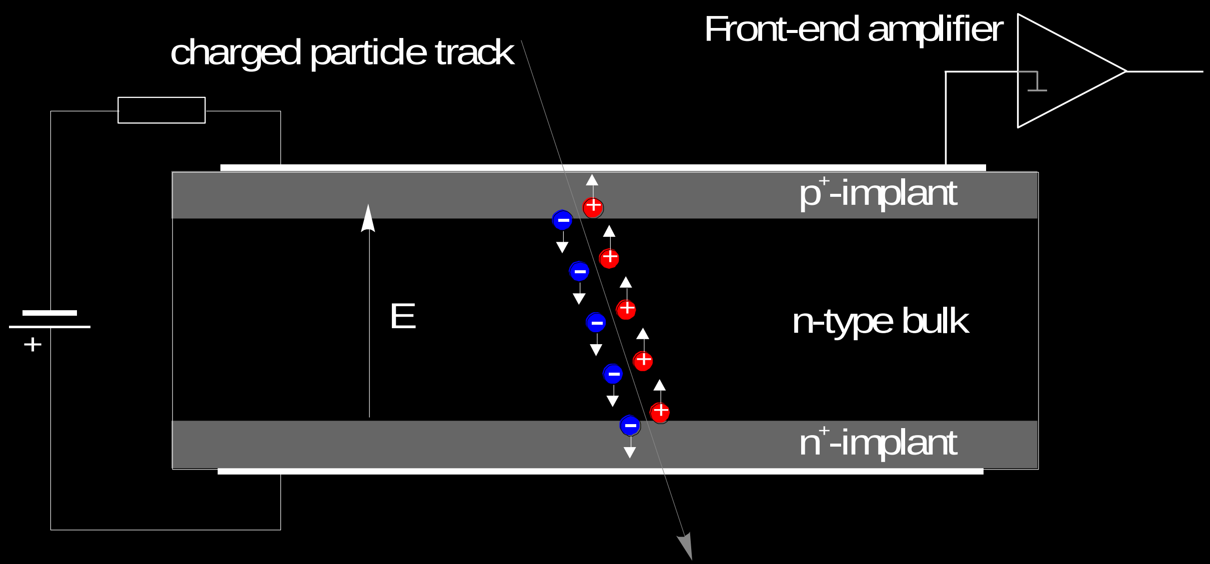
- Equivalent circuit of the sensor:



Current source with capacitor in parallel

- Example 1: wire chamber
  - Coaxial capacitor configuration
  - Moving charges induce current

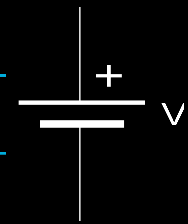
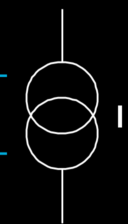
Example 2: Silicon Sensor



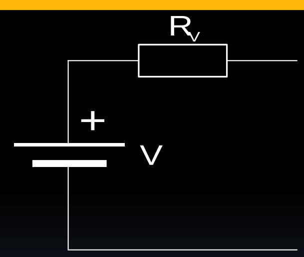
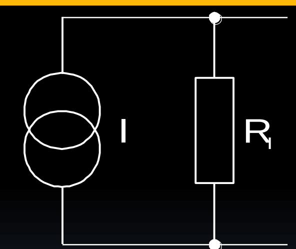
- Traversing charged particle creates electron-hole pairs
- Carriers drift towards electrodes in the electric field
- Moving carriers induce current in the circuit → current source
- Parallel plates act as a capacitor

Comparison: Voltage vs. Current Source

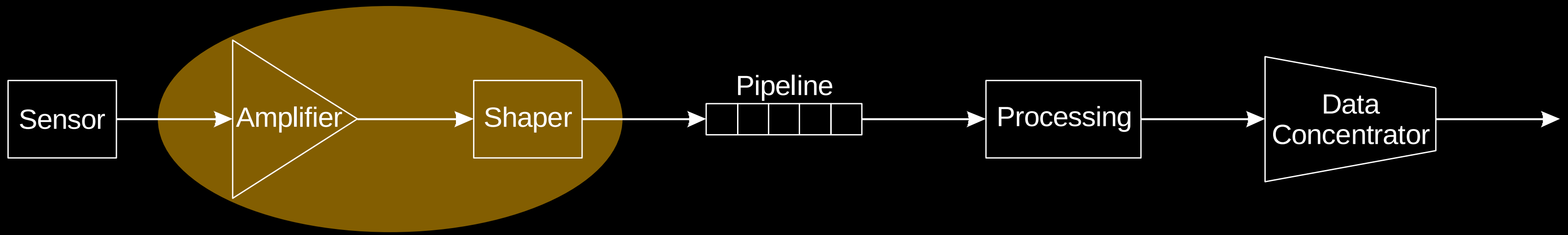
IDEAL

Property	Voltage Source	Current Source
Voltage	constant 	anything 
Current	anything	constant
Idle (no power)	Open (I=0)	Shorted (V=0)

REAL

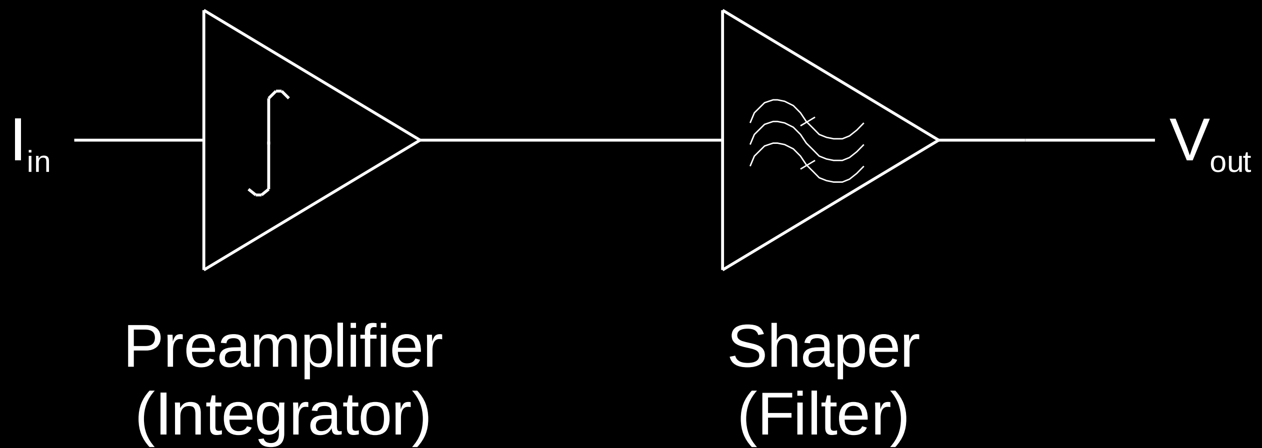
Property	Voltage Source	Current Source
(Linear) equivalent circuit		
Resistor causes	Internal voltage drop	Internal current drop
Conversion	Norton-Thevenin equivalent: $R_V = R_I$; $V = I R_{V/I}$	
Examples	Battery Wall plug (AC)	Detector NIM module outputs

Amplifier & Shaper



- Typically, the amplifier is an integrator
  - Integration of current over time = ?
  - Measuring charge $$\int i\, dt = Q$$
- Signal-to-noise performance of the whole system mainly depends on this very first amplifier stage
- Located as close to sensor as possible

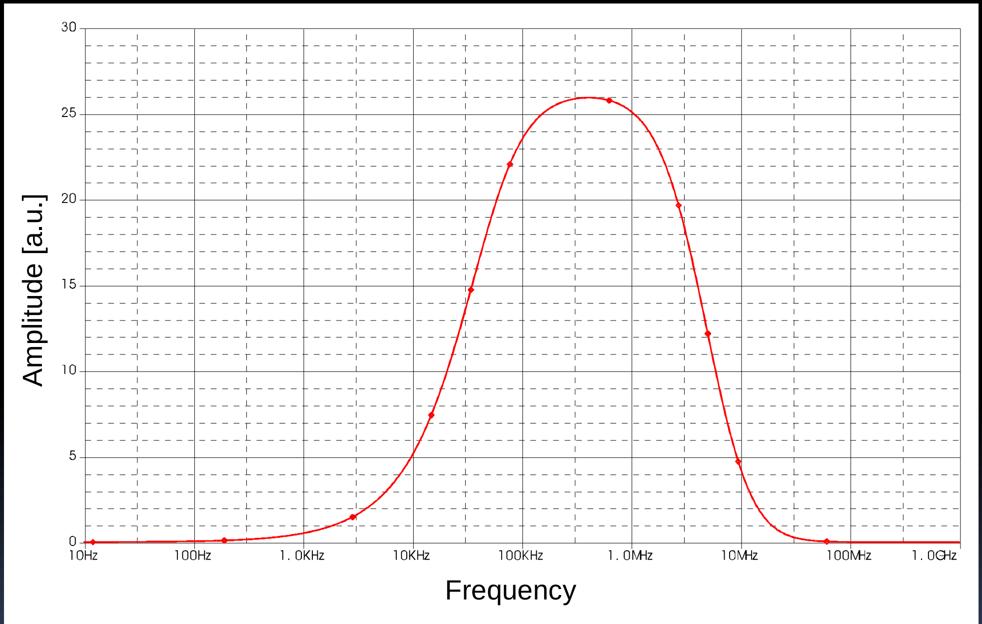
Front-End Amplifier Principle



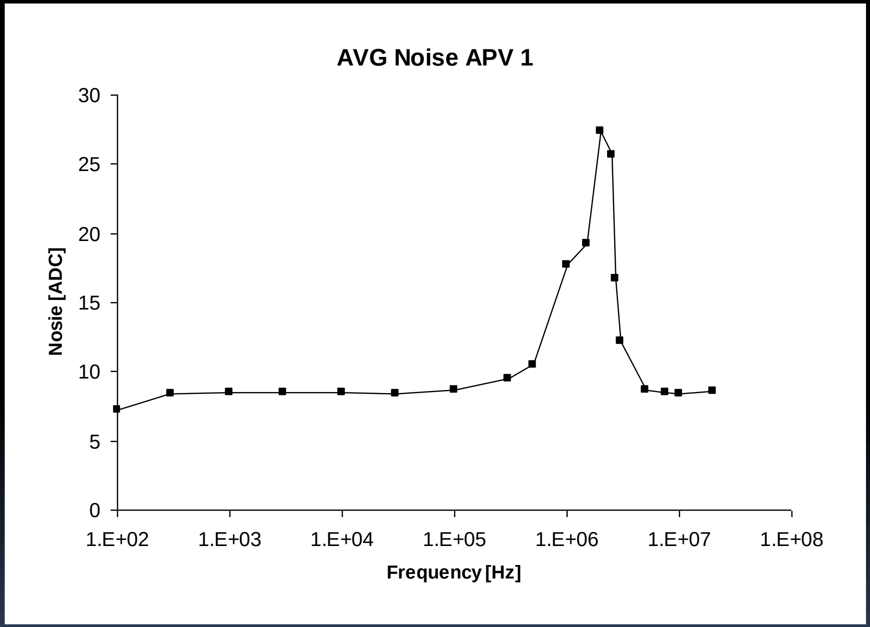
- First stage: Integrator
  - Detector current → charge
- Second stage: Filter
  - Limit bandwidth to reduce noise
  - Let desired signal pass and cut away all the rest

Shaper Bandwidth Reduction

- Example: APV25 Tracker front-end amplifier (CMS)
  - Shaper sensitive around 1 MHz

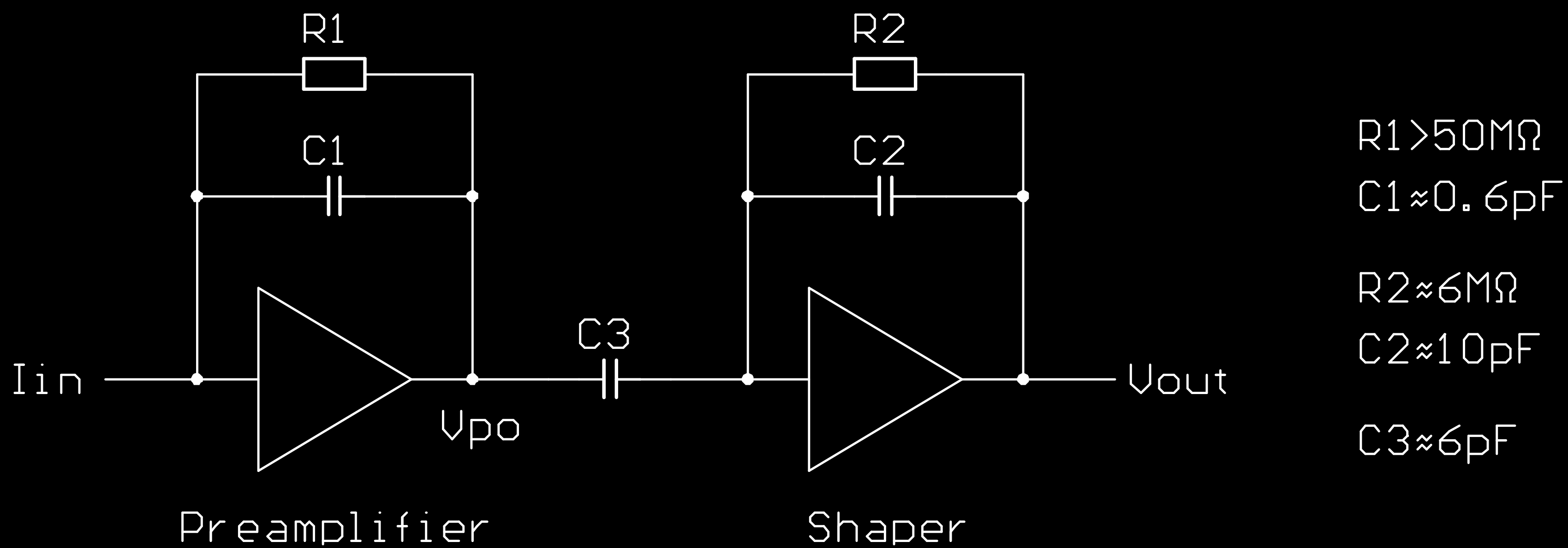


Simulation



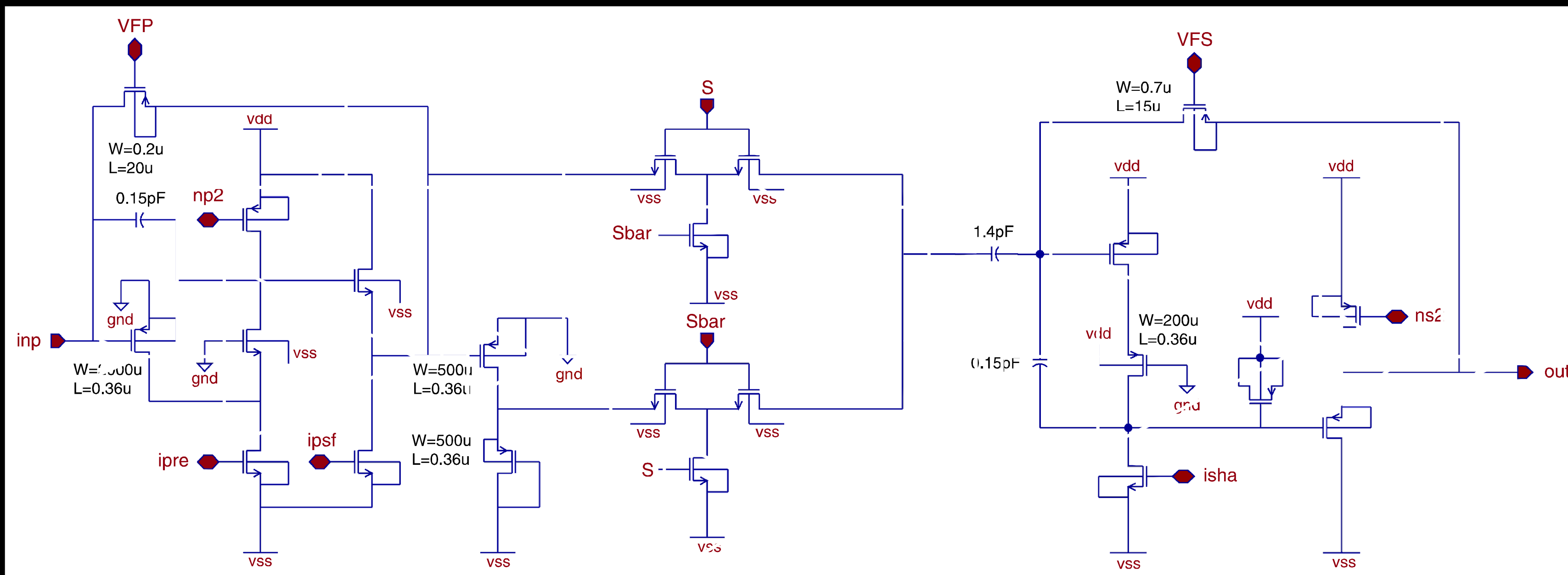
Measurement

Example: VA2 Chip Input Stage



- VA2 is a general-purpose front-end amplifier chip for silicon strip detectors
- "Slow" shaper in the µs range – what does this mean for the noise?

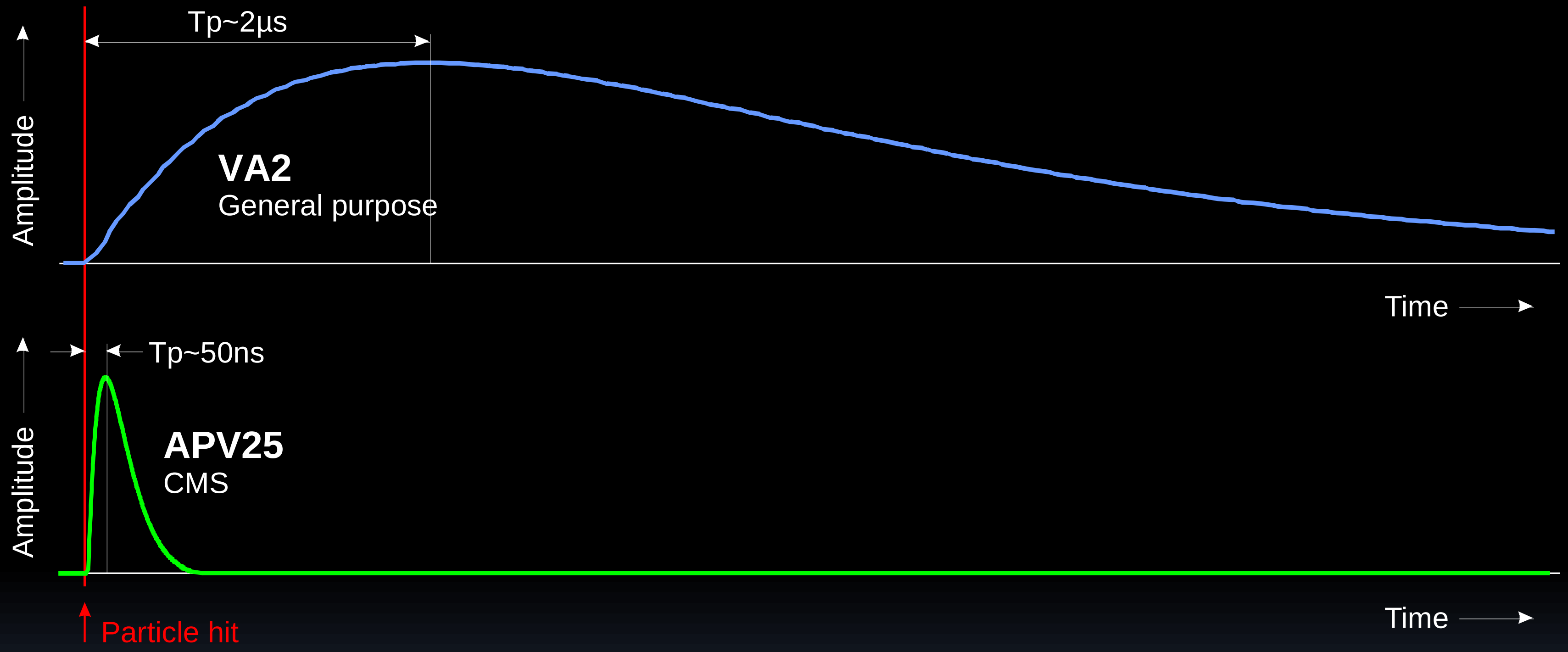
Example: APV25 Chip Input Stage



Preamplifier (optional) Inverter Shaper

- APV25 is the front-end chip for the CMS Tracker
- "Fast" shaper: 50ns – what does this mean for the noise?

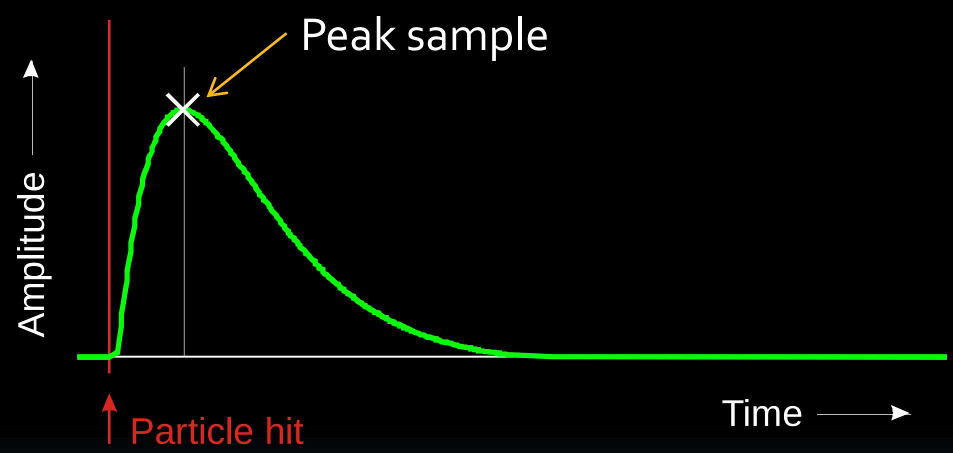
Shaper Output



- T_p...shaping time (or peaking time)
- Faster shaping can be a necessity of the experiment to distinguish subsequent events, but also implies larger noise

Shaper Output Sampling

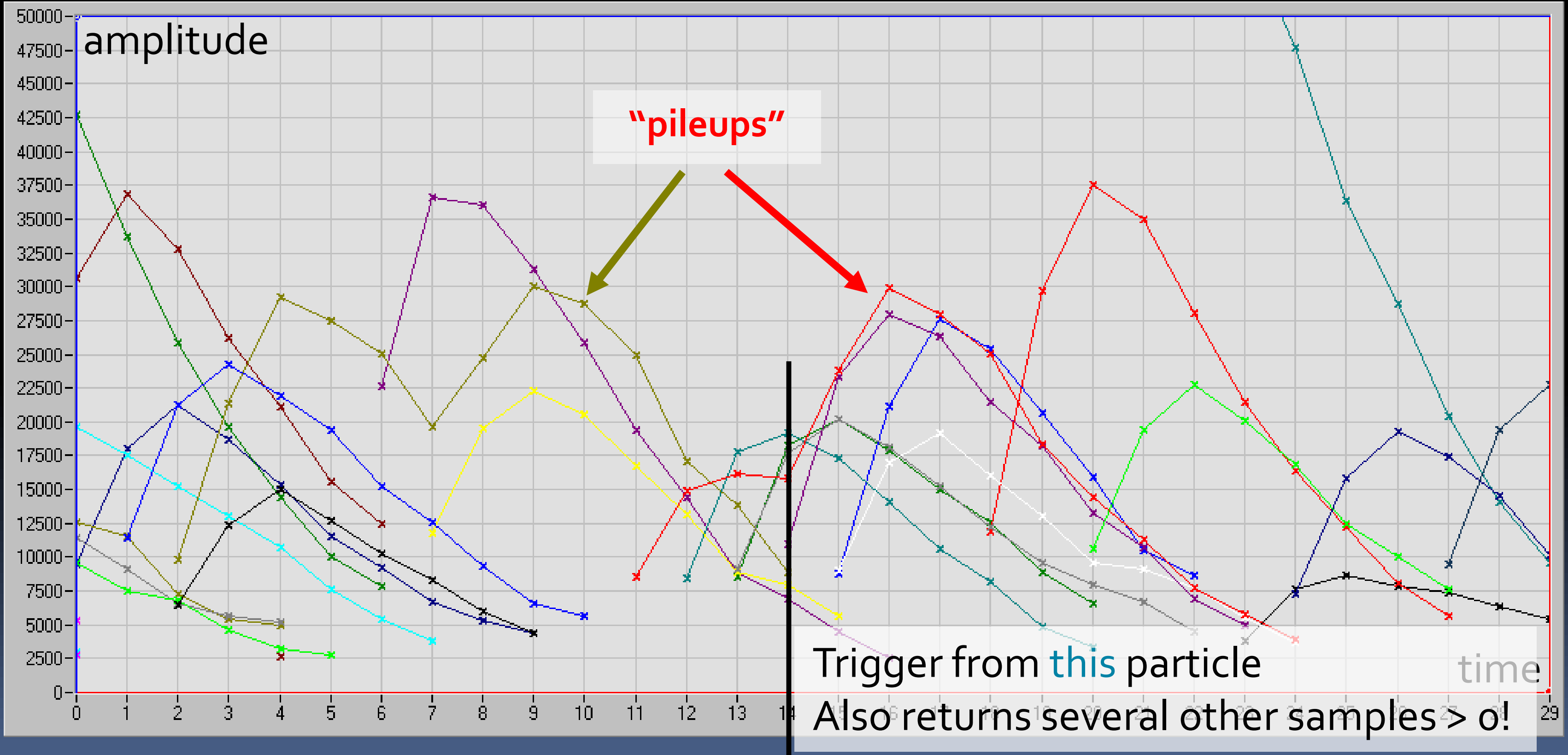
- Usually, shaper output is sampled once at the peak
  - Only sampled value is passed on in the readout chain



- The timing is given by a constant offset from the particle hit (as supplied by an external trigger, e.g. scintillator)
- What happens if there are several particles with different timing?

Pile-up Events

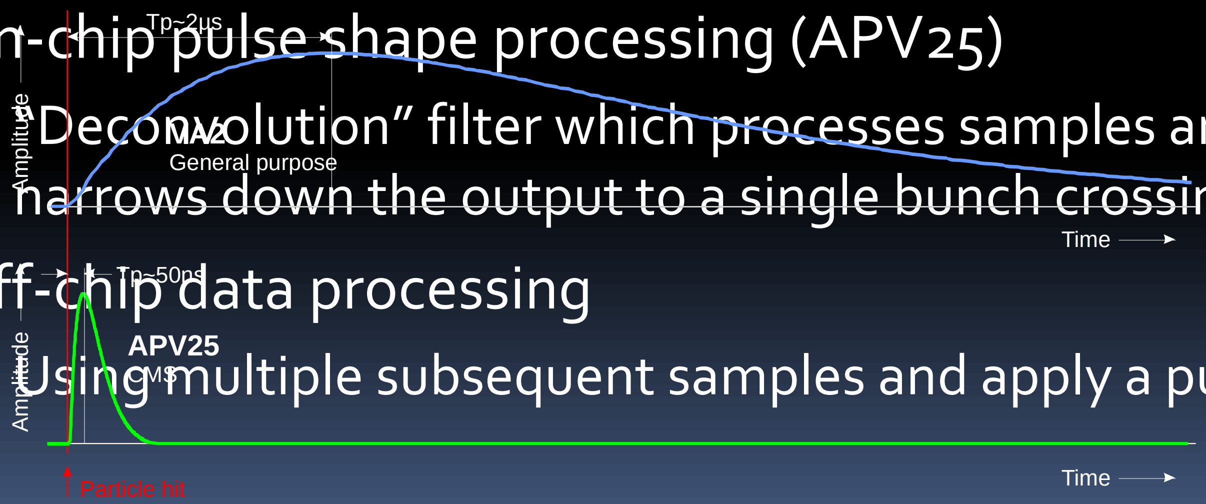
- Strip detector measurement in a high intensity beam
- Ambiguities and non-peak sampling can occur



How to Avoid Such Ambiguities?

- Better timing information implies more data, more energy and/or a higher noise figure

- Faster Shaping = narrower output pulses
  - Limited by noise performance
- On-chip pulse shape processing (APV25)
  - "Deconvolution" filter which processes samples and essentially narrows down the output to a single bunch crossing
- Off-chip data processing
  - Using multiple subsequent samples and apply a pulse shape fit



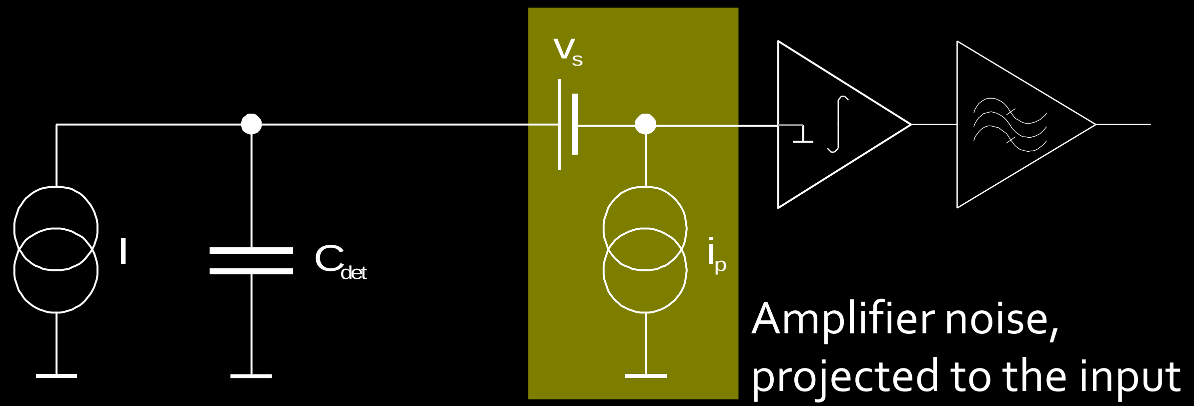
"Low-Noise" Amplifiers

- Nearly all front-end chips are called "low-noise"
- General feature of the integrator+shaper combination
- Noise is typically given by ENC (equivalent noise charge) referred to the input
- $\mathbf{ENC = a + b \cdot C_{det}}$ (a,b…const, C_{det}…detector capacitance)
- Examples:

	T_p [ns]	ENC [e]
VA2 (1993)	2000	60 + 11 / pF
APV25 (CMS, 1999)	50	250 + 36 / pF

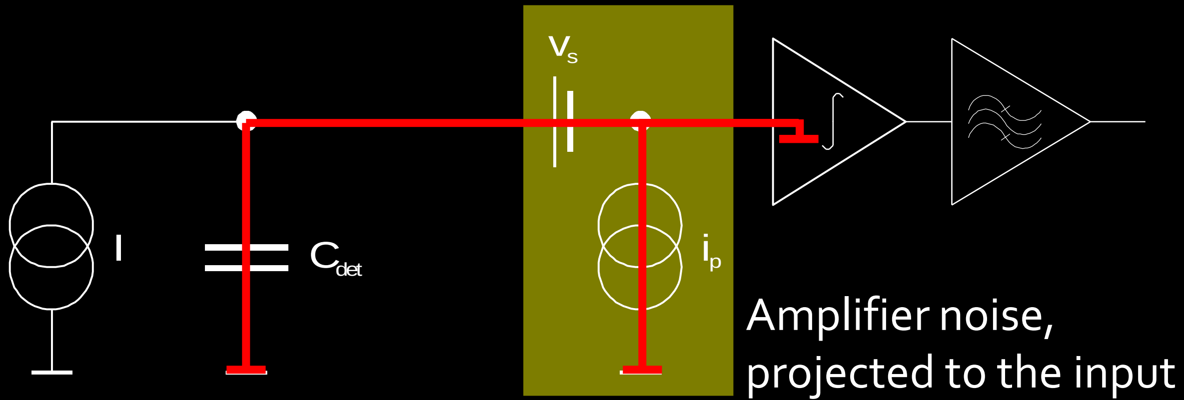
- How can noise depend on the detector capacitance?

Simplified Noise Model (1/2)



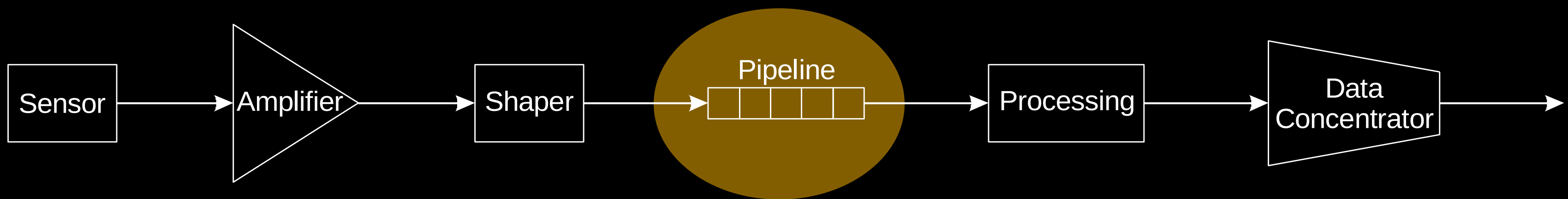
- Amplifier noise is projected to voltage noise source and current noise source at input
- Integrator measures charge, which is equivalent to:
  - $Q = \int i\,dt$
  - $Q = C \cdot V$

Simplified Noise Model (2/2)



- Superposition analysis (one by one, other voltage sources are closed, other current sources are open; **very simplified**):
  - Parallel noise: $Q_p = \int i_p \, dt$
  - Series noise: $Q_s = C_{det} \cdot V_s$
  - Total noise: $Q_n = Q_p + Q_s$ $\quad$ $\mathbf{ENC = a + b \cdot C_{det}}$

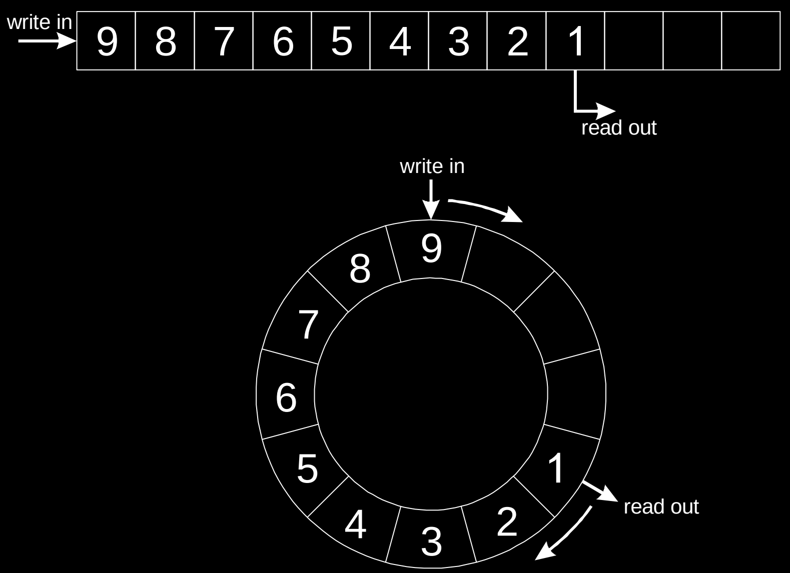
Pipeline

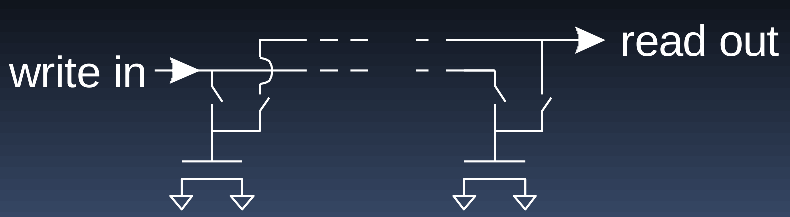


- Modern experiments require that data are retained for a while
- Why?
  - LHC bunch crossings occur every 25 ns (≡ 40 MHz)
  - Only selected events are read out
  - It takes ~3 µs to decide whether or not
  - ~120 bunch crossings happen during that time
  - LHC readout electronics contains a storage for >120 clocks
  - Example: APV25 (CMS Tracker) has a pipeline with 160 cells

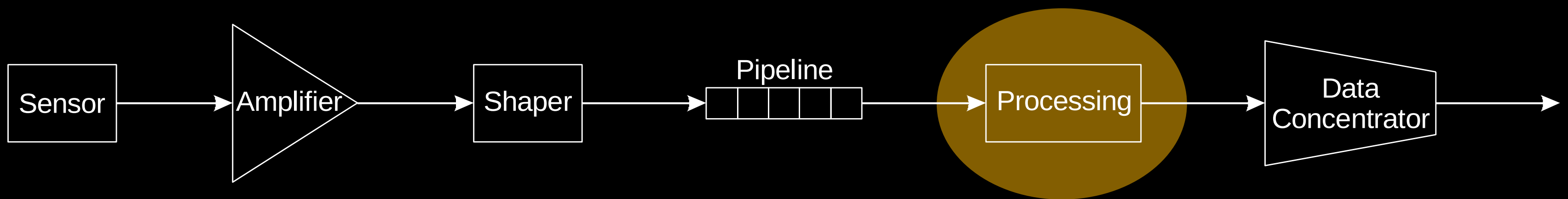
Pipeline Example

- APV25 chip (CMS Tracker):
  - Shaper output is sampled
  - Analog values are stored in the pipeline
  - Noise and losses would not allow real shifting of analog data
  - In fact, it is a ring buffer with moving write/read pointers
  - Storage element: capacitors





Processing



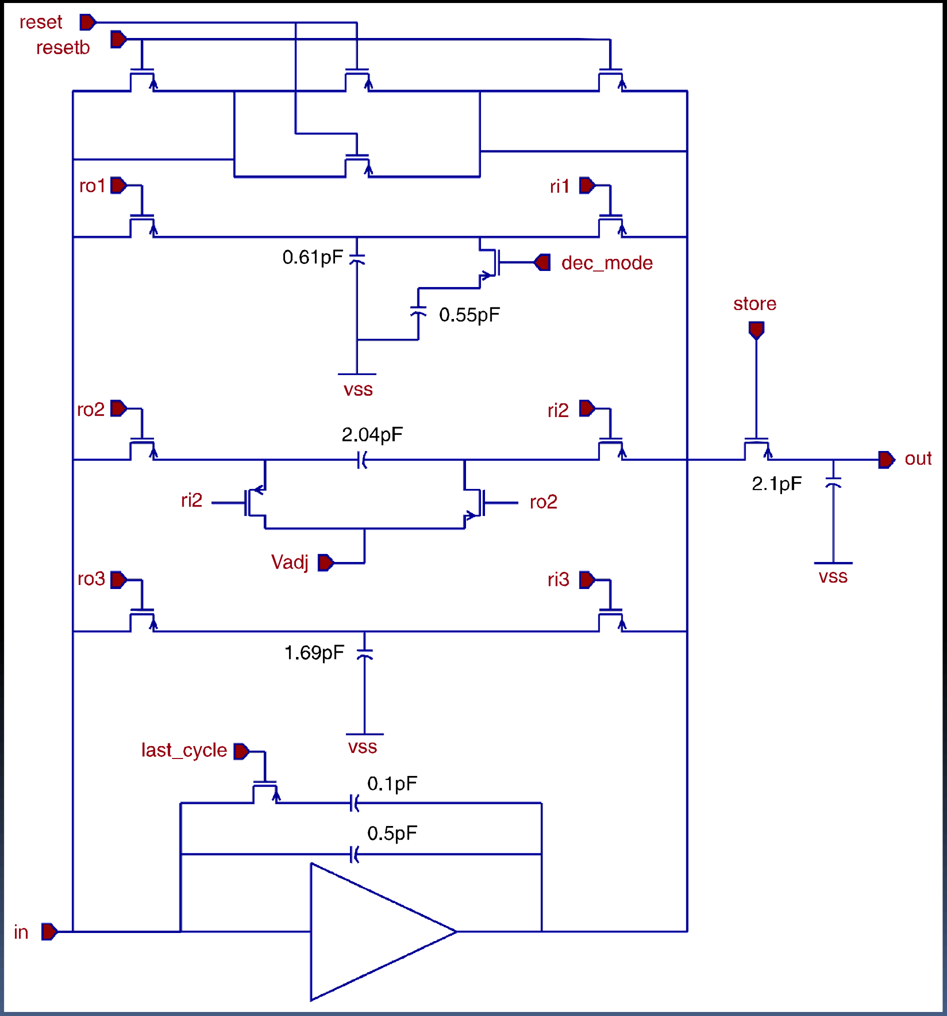
- This is a very individual feature
- Example: APV25
  - "Deconvolution" filter
  - Essentially reverts shaping
  - (Ideally) reduces width of shaper output curve to 1 clock

Deconvolution

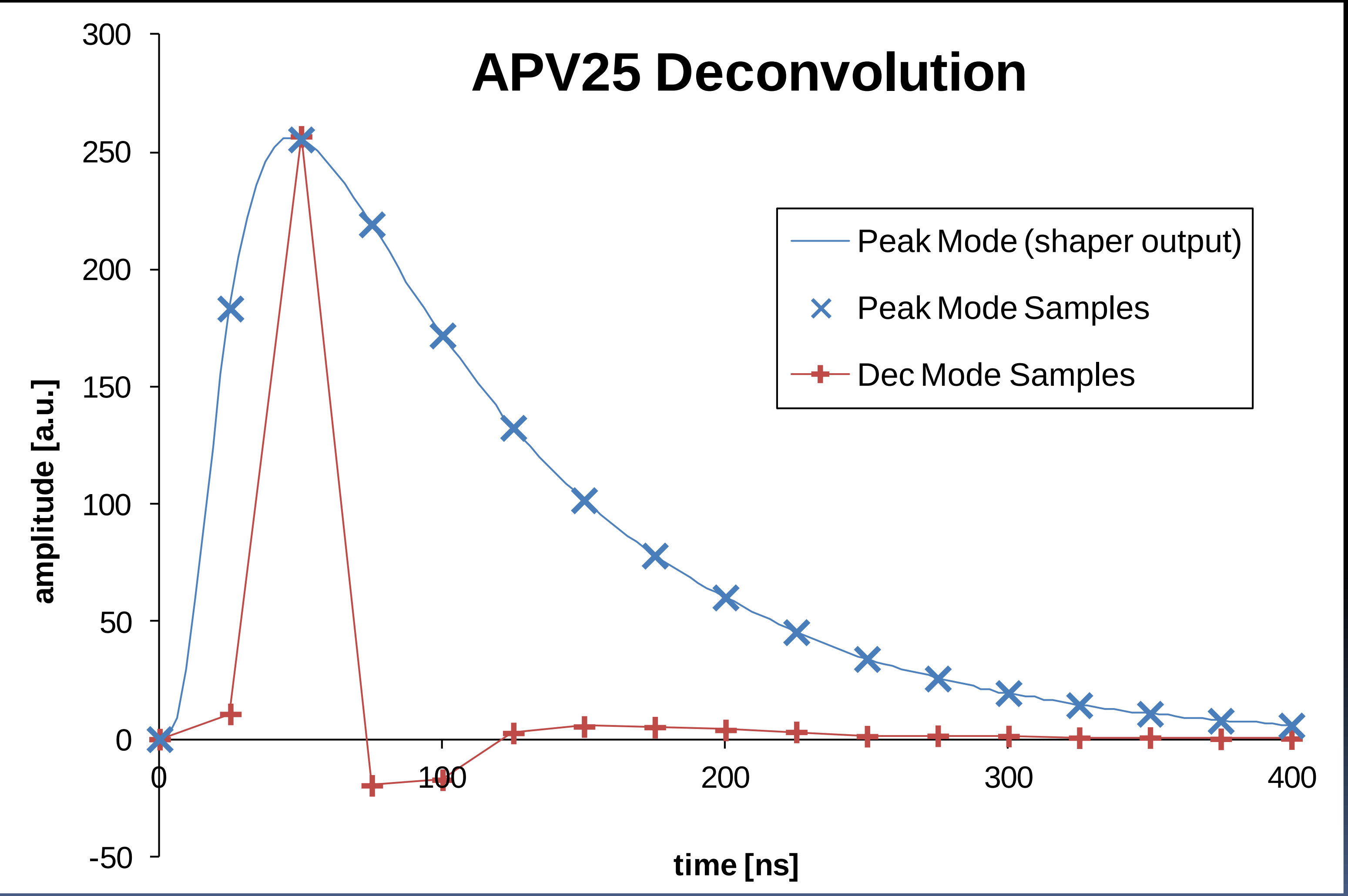
- Switched capacitor filter
- Time-discrete operation
- Weighted sum of 3 consecutive samples

$$d_k = w_3\,p_{k-2} + w_2\,p_{k-1} + w_1\,p_k$$

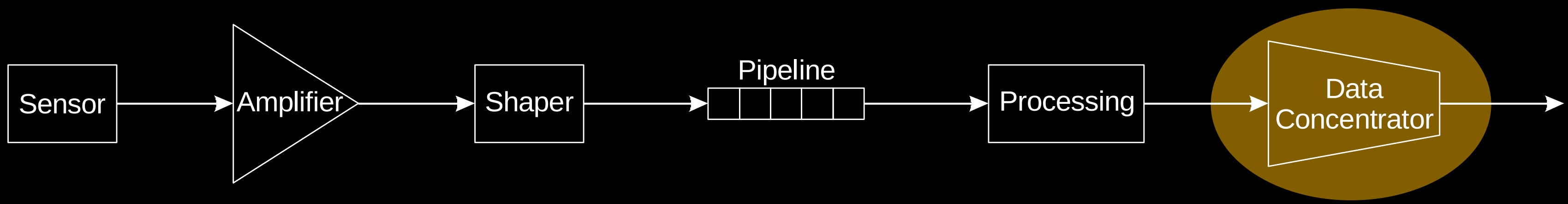
- 3-stage FIR (finite impulse response) filter
- Requires clock-synchronous bunch crossings (=LHC)



Deconvolution Result

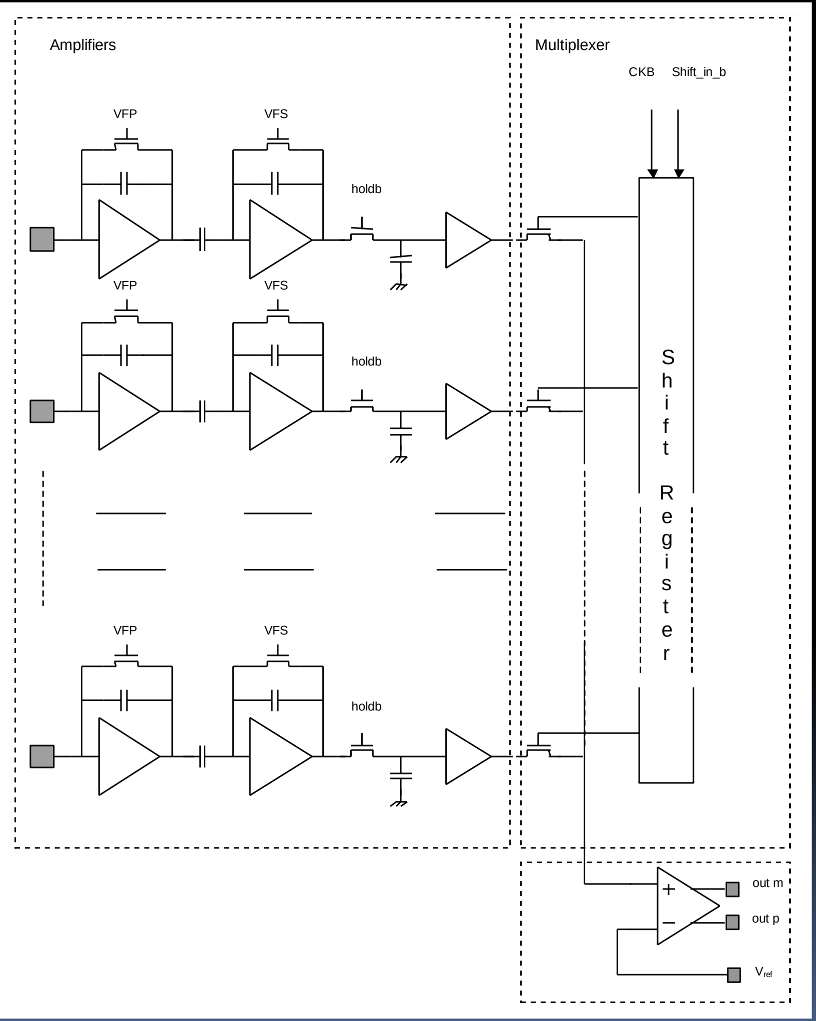


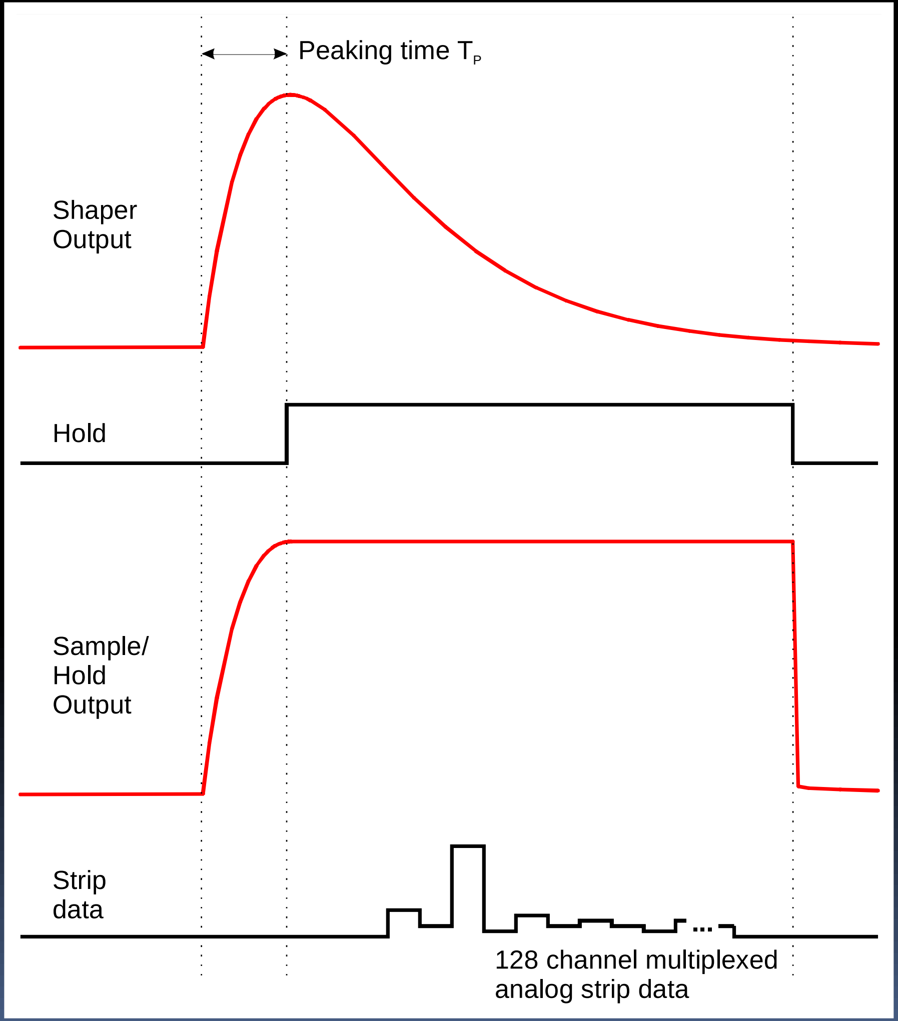
Data Concentrator



- Last stage of front-end chip
- Front-end chip has many channels in parallel (typically 128)
  - Impossible to handle so many output lines
  - Usually only one single (or differential) output line
- Multiple channels to be sent out on a single output
- Typically done with time-multiplexing
  - All 128 channel values sent out one after another

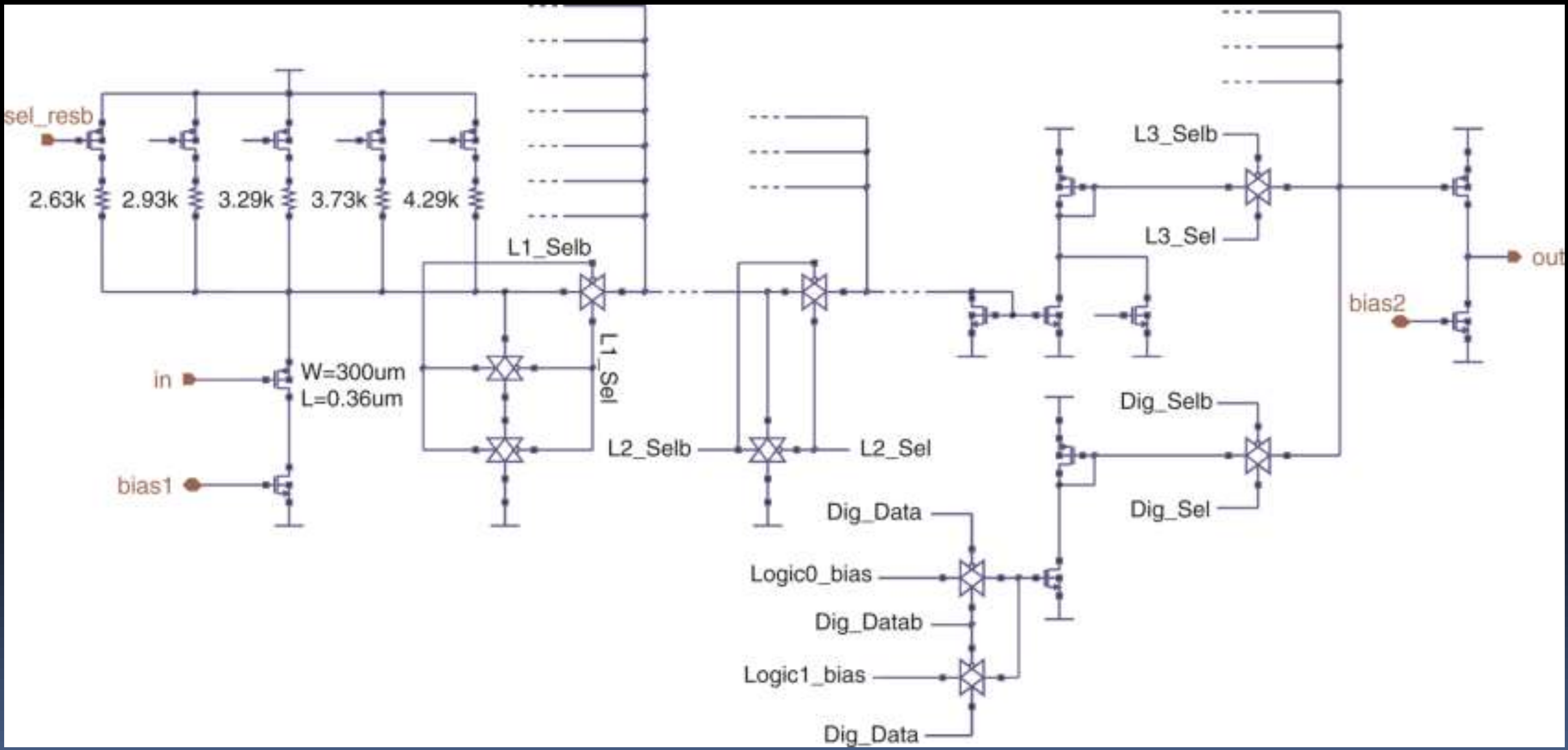
Sample/Hold and Multiplexer



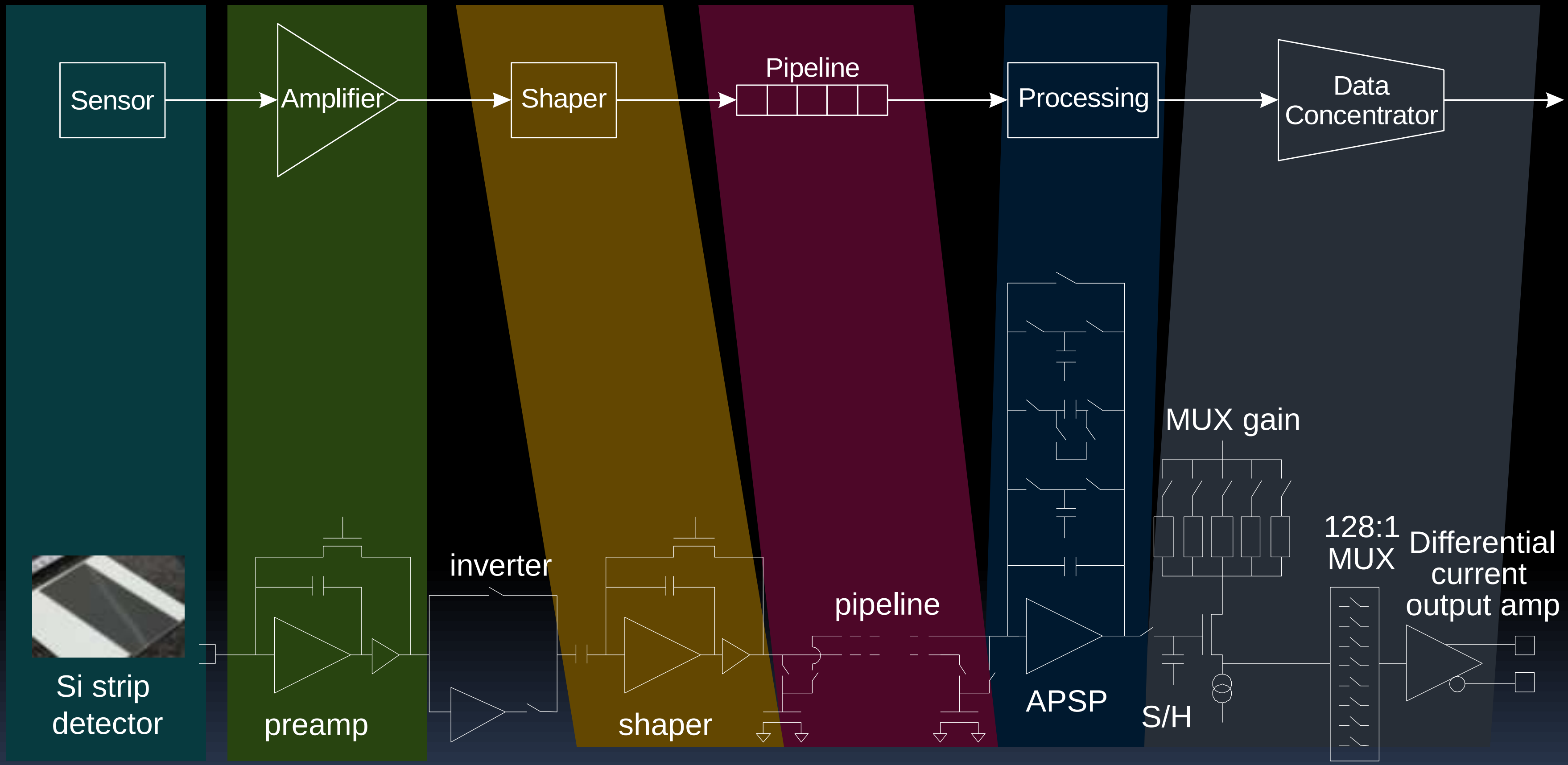


Multiplexer

- Example: APV25 chip with tree-like structure (3 levels)
  - Only final 4:1 stage runs at full speed – lower power consumption



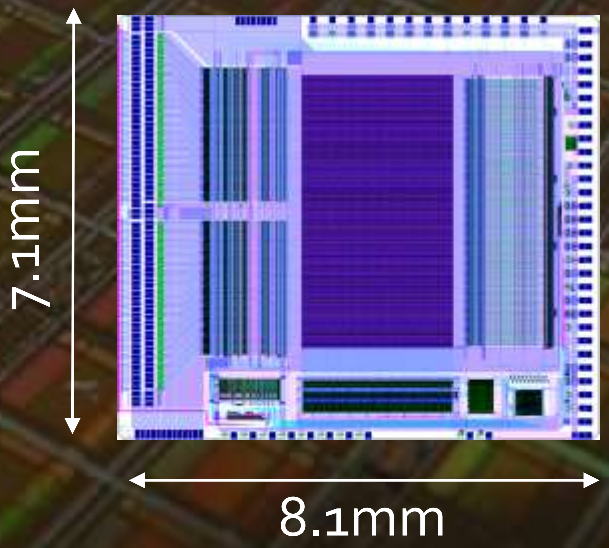
Full Picture



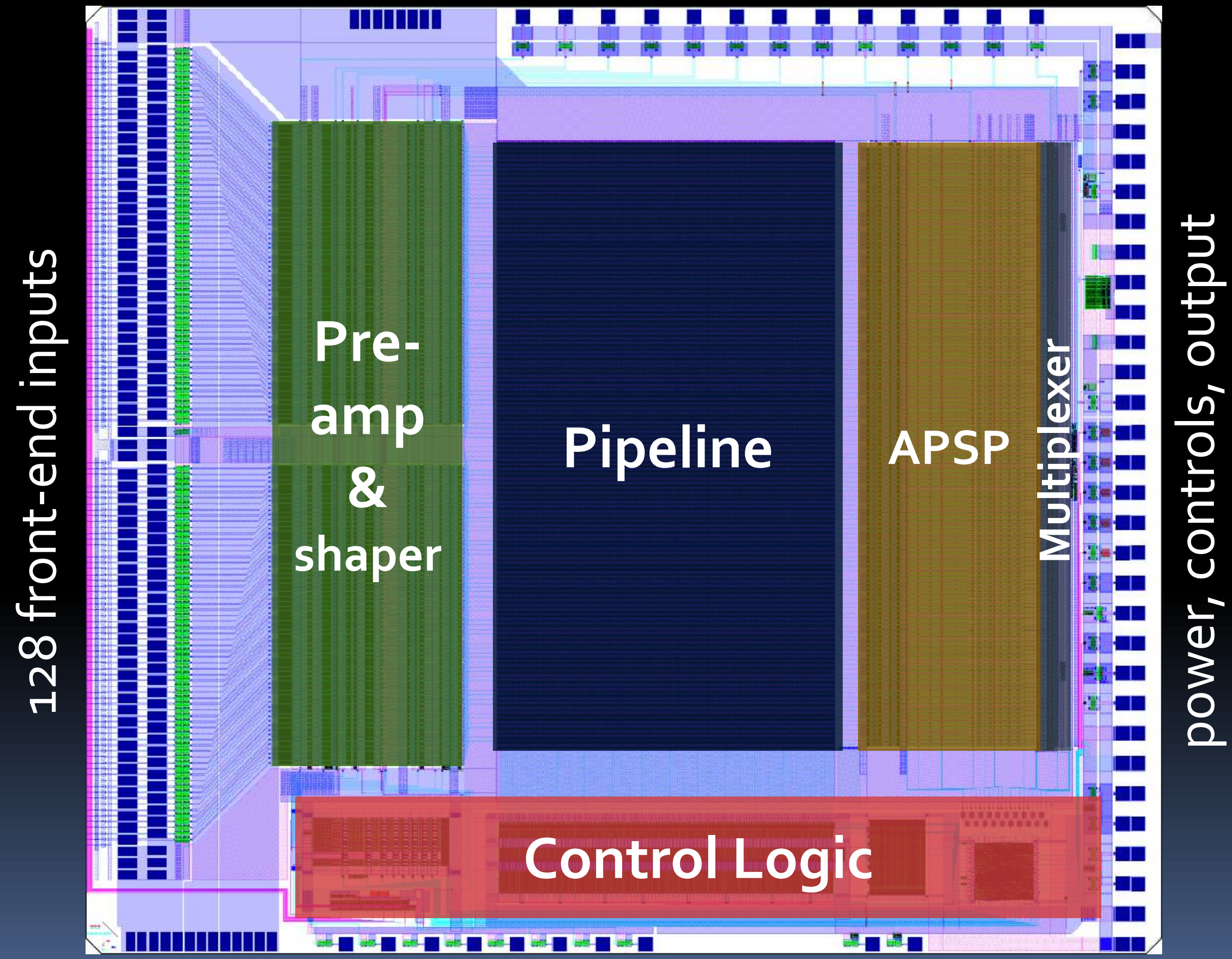
Silicon strip detector + APV25 front-end chip

Full Chip Example: APV25 (CMS)

- Shaping time: 50ns
- Sampling (clock): 40MHz
- Analog pipeline (192 cells) to store data until trigger arrives
- Optional "deconvolution" (APSP=analog pulse shape processing) filter
- 128:1 multiplexer
- Differential output driver



APV25 Chip Layout

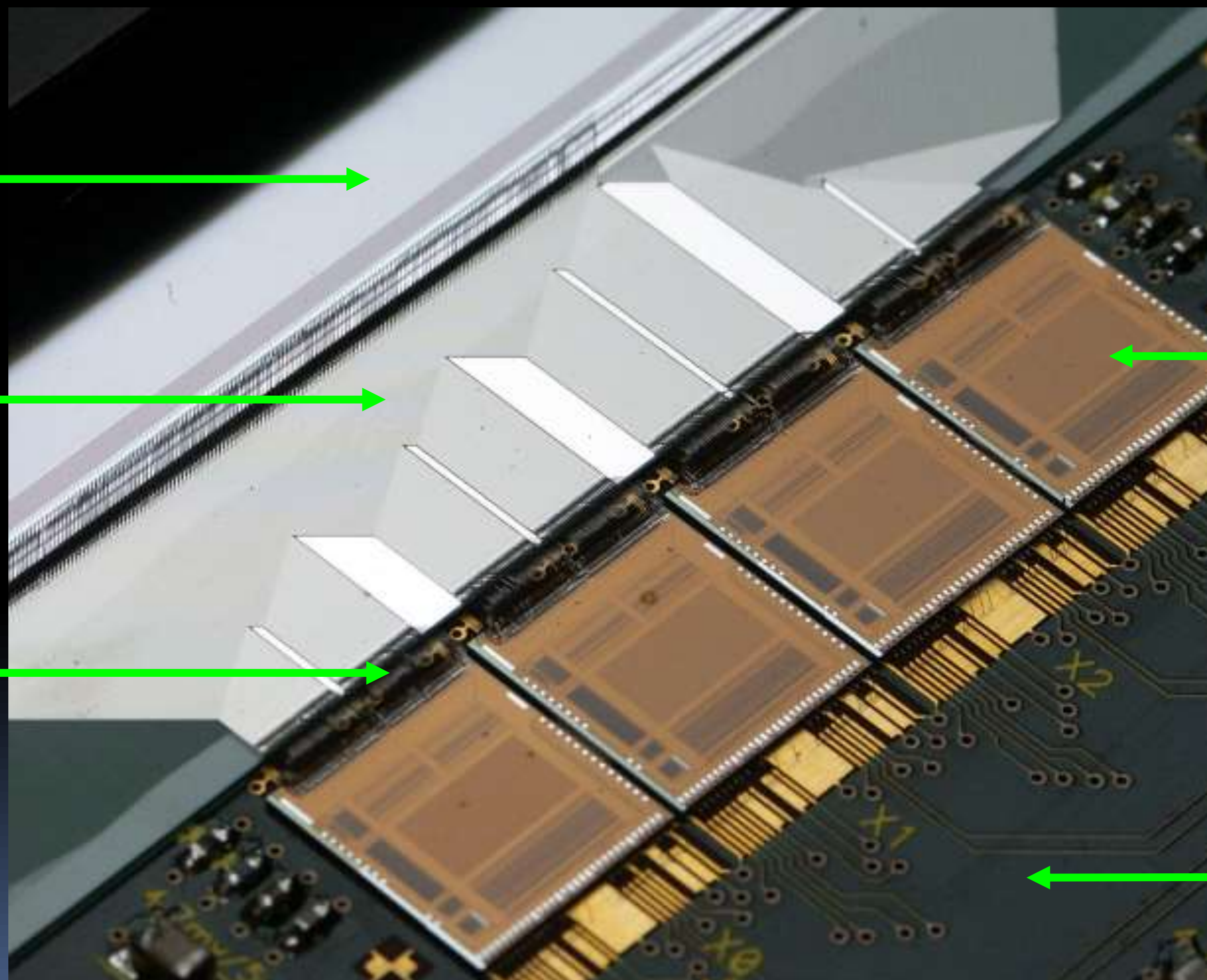


APV25 in Action

Sensor

Pitch adapter

Wire bonds



APV25

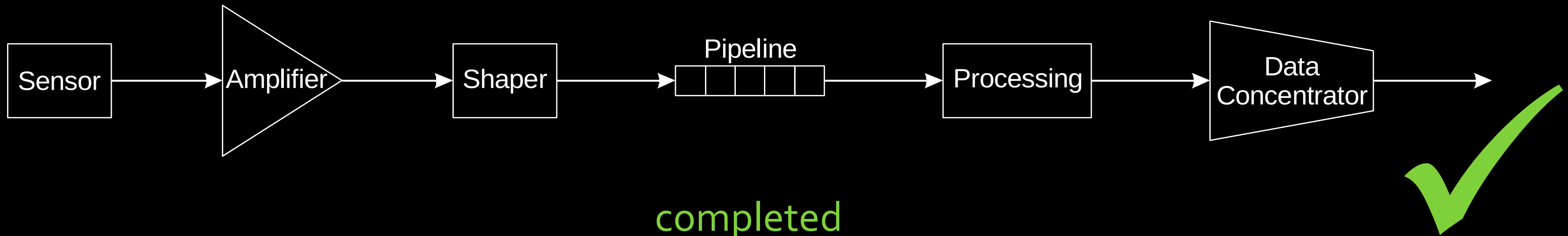
Hybrid board

Front-End Amplifier Summary

- Integrated circuits with typically 128 channels
- 2 stages:
  - Preamplifier (integrator: current $\rightarrow$ charge)
  - Shaper (band-pass filter to reduce noise)
- Noise is referred to input and expressed as charge:
  - **ENC = a + b · C_{det}** (a,b…const, C_{det}…detector capacitance)
- Shaper bandwidth determined speed and noise
  - Fast $\equiv$ large noise; slow $\equiv$ low noise
  - Required speed is usually defined by the experiment
  - Slow shaping and pile-up can lead to ambiguities

Reminder: Typical Readout Chain

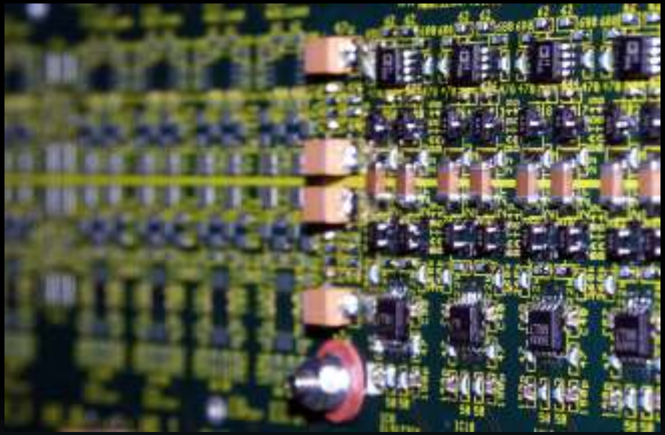
- Front-end part:



completed

- Back-end part:

- Let's first look at the connection between the 2 parts…



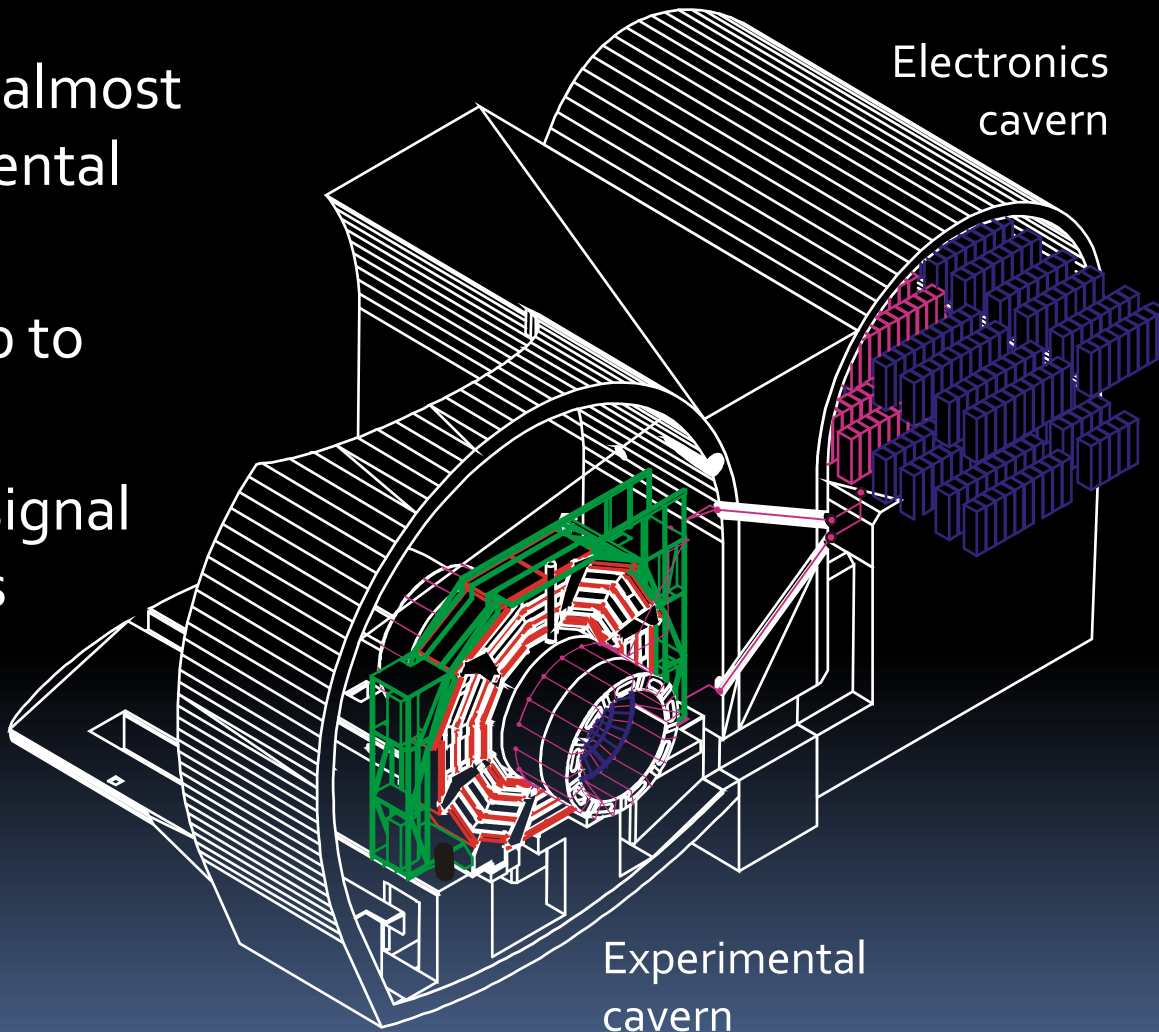
- Typical Readout Chain
- Readout Chain – Front-End
- **Signal Transmission**
- Readout Chain – Back-End
- Additional Topics

Why Don't We Put Everything in One Place?

- Detector front-end is usually quite crowded
- Several restrictions:
  - **Radiation** environment does not allow commercial electronics
  - **Magnetic field** also puts some limitations
  - **Material budget** should be as low as possible
  - **Power consumption** as well (requires cooling = material)
- Thus, only inevitable electronics are put in the front-end
- Everything else is conveniently located in a separate room outside the detector, traditionally called "counting house"
  - Allows access during machine and detector operation

Example: CMS Experiment

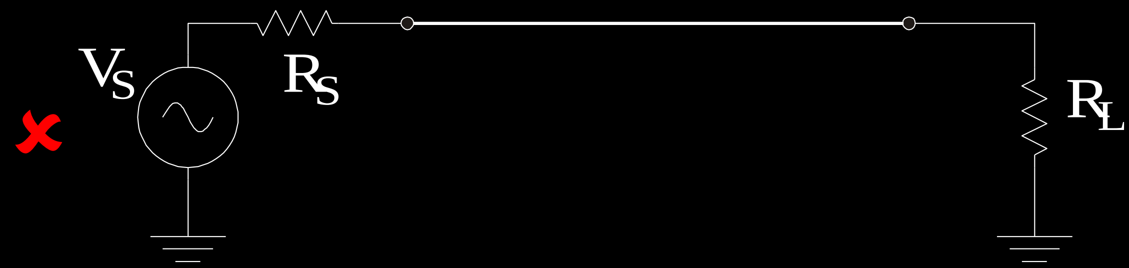
- Electronics hall is almost as big as experimental cavern
- Signal distance up to 100m
- Huge amount of signal transmission lines



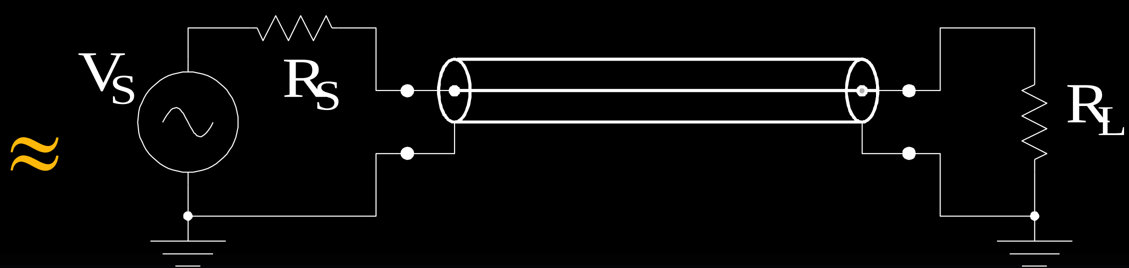
Generic Transmission Chain

- Signal directions
  - Readout (large amount): front-end to back-end, analog or digital
  - Controls (small amount): back-end to front-end, digital (clock, trigger, settings)
- Often, the front-end chips cannot drive the full path
  - Repeater (driver/receiver) is needed to amplify signals

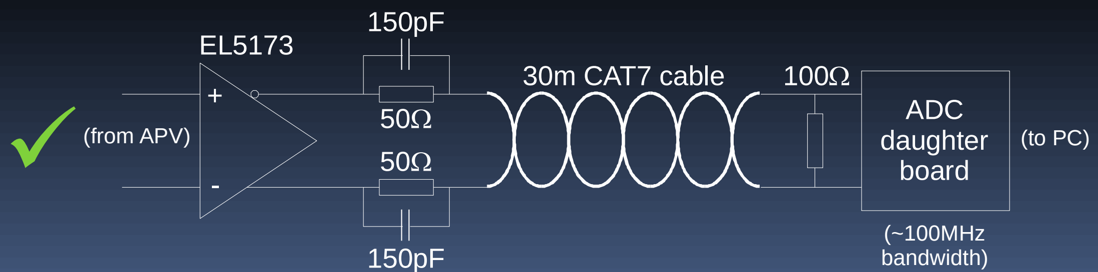
Excursion: Electrical Signal Transmission



- Single-ended against GND
  - Huge ground loop



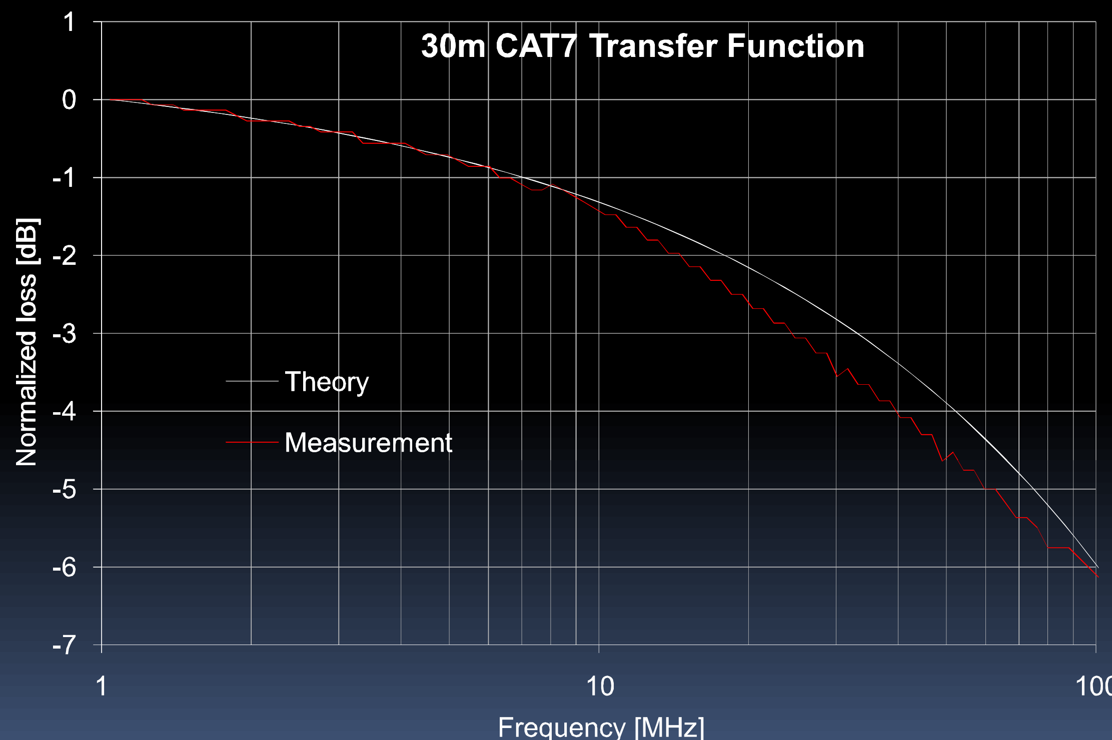
- Single-ended in coaxial cable
  - Ground loop?



- Differential twisted pair (+shield)
  - Largely immune

Cable Bandwidth

- Every cable has a finite bandwidth / damping
  - How does damping depend on frequency?
- Example: CAT7 network cable (shielded twisted pairs)
- Significant especially for analog signal transmission



Alternative: Optical Fiber

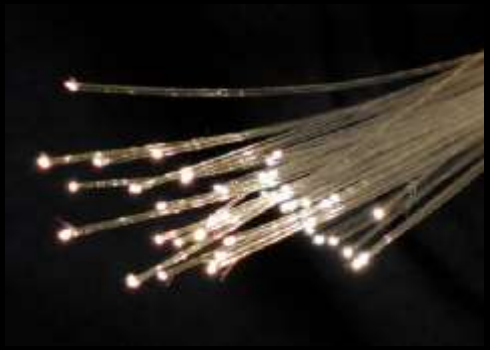
- Benefits:
  - Fibers have extremely high bandwidth and very little loss
  - Automatically provide electrical isolation between ends
- Drawback:
  - require conversion on both ends → more expensive than a cable

- Best suitable for long-haul, high-speed digital data transmission such as telecom
  - Nonetheless also often used in HEP experiments
- Optical transmission usually requires digital signals with AC coding
  - same probability for 0 and 1; average = 0.5
  - Limited number of consecutive 0s or 1s

Electrical vs. Optical Communication

- Which one is more reliable?

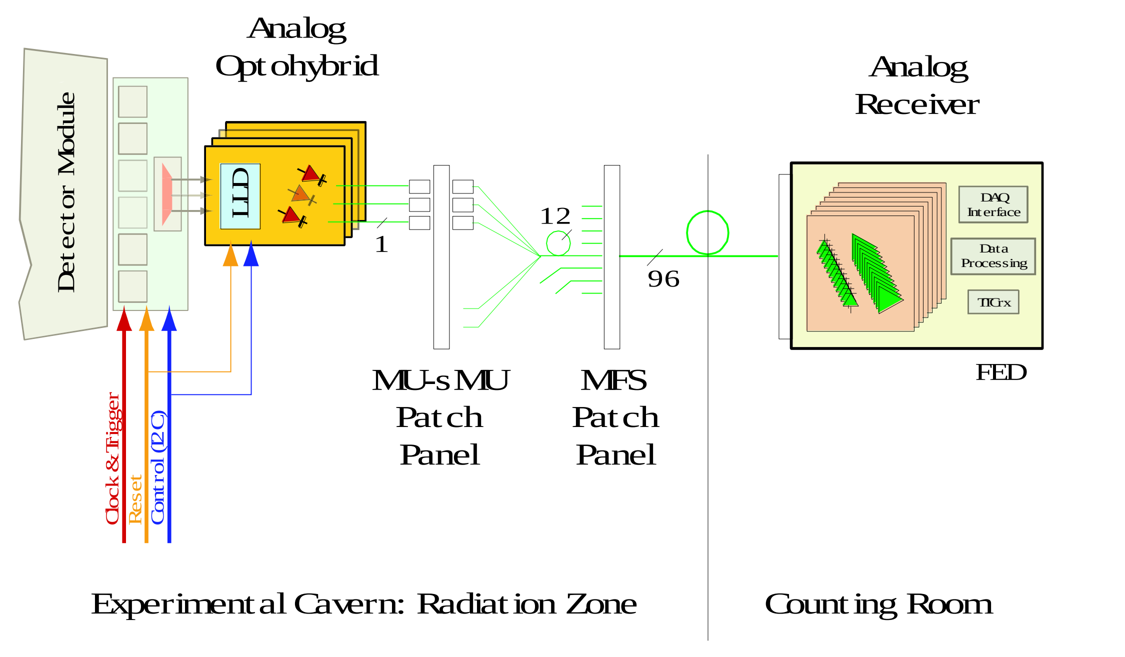
Comparison: Copper vs. Optical Fiber

Property	Copper Cable	Optical Fiber
		
Cable	rigid	delicate (e.g. radius)
Connectors	huge variety	few standards
Size/weight	large	small
Bandwidth	limited	high
Loss	high	low
Driver + receiver	cheap	(slightly) expensive
Level isolation	no	yes

Institute of High Energy Physics

Example: CMS Tracker (1)

- Optical fiber required because of material budget

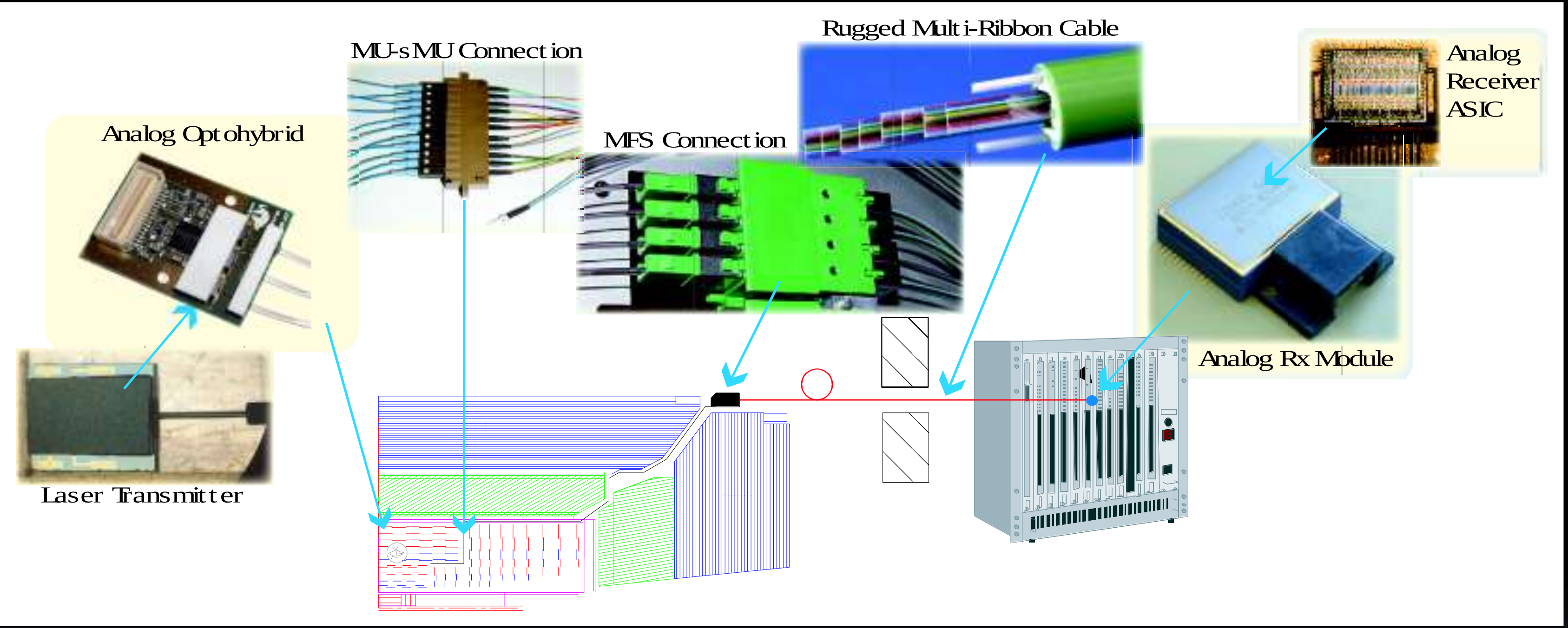


Analog Optical Link Parameters

37,000 channels
100m fiber length
1310nm infrared light
Step-index single-mode fiber
Intensity modulation
40MHz readout speed
I2C control interface

- Exceptional case: **analog** optical transmission
  - Special requirements for linearity, gain stability and noise

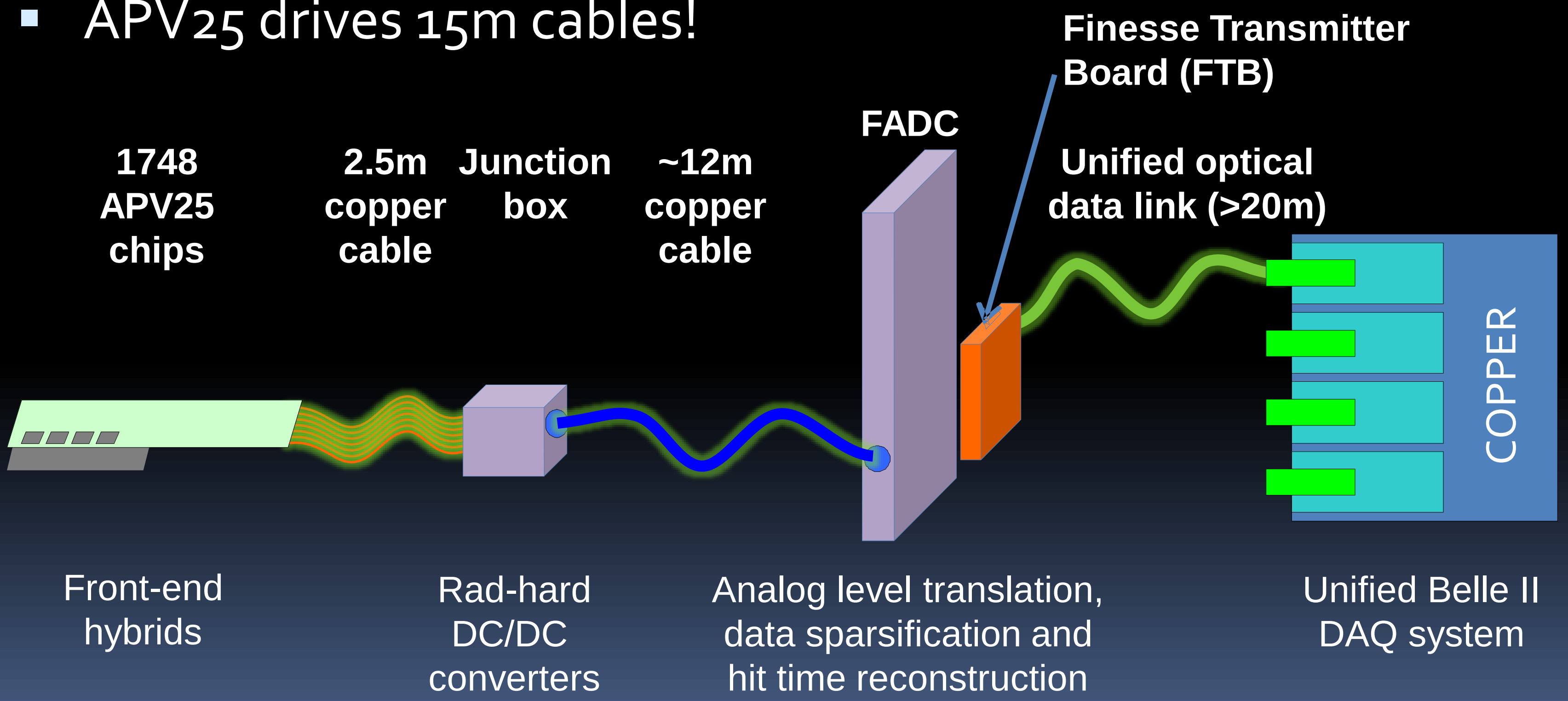
Example: CMS Tracker (2)



- Several components are customized and thus expensive
  - O(10000) are small quantities for industry
- Cost per link: ~150 € (cf. ~15 € with cable)

Example: Belle II Silicon Vertex Detector

- Analog APV25 readout is through copper cable to FADCs
- Junction box provides LV to front-end
- APV25 drives 15m cables!

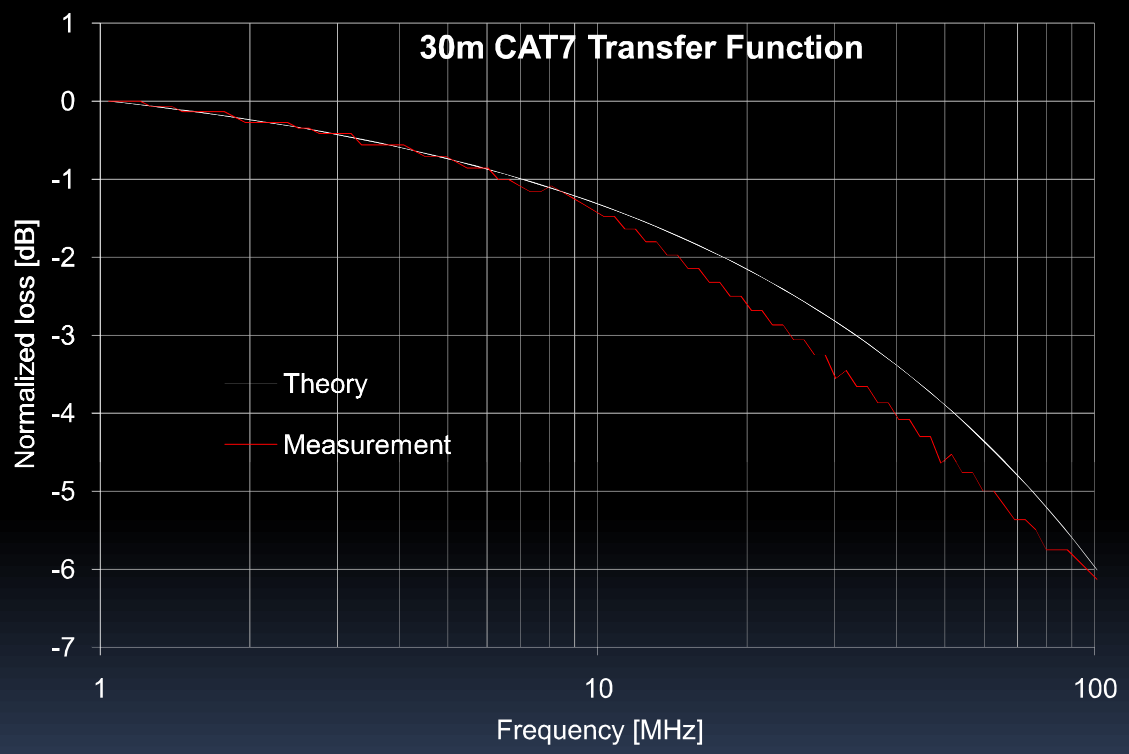


Example: Belle II Silicon Vertex Detector

- Using same APV25 chip as in CMS, but shorter distance → no optical link required
- Analog signals are attenuated in long copper cable – how to compensate this?
  - First attempt was an analog equalizer chip (enhancing higher frequencies) with moderate success
  - Later tried purely digital filter after digitization
  - Perfect regeneration with digital signal processing (FIR=finite impulse response filter) at the back-end inside an FPGA
  - Multiplication of 8 consecutive samples with 8 filter coefficients and summing in real-time (40 MHz)

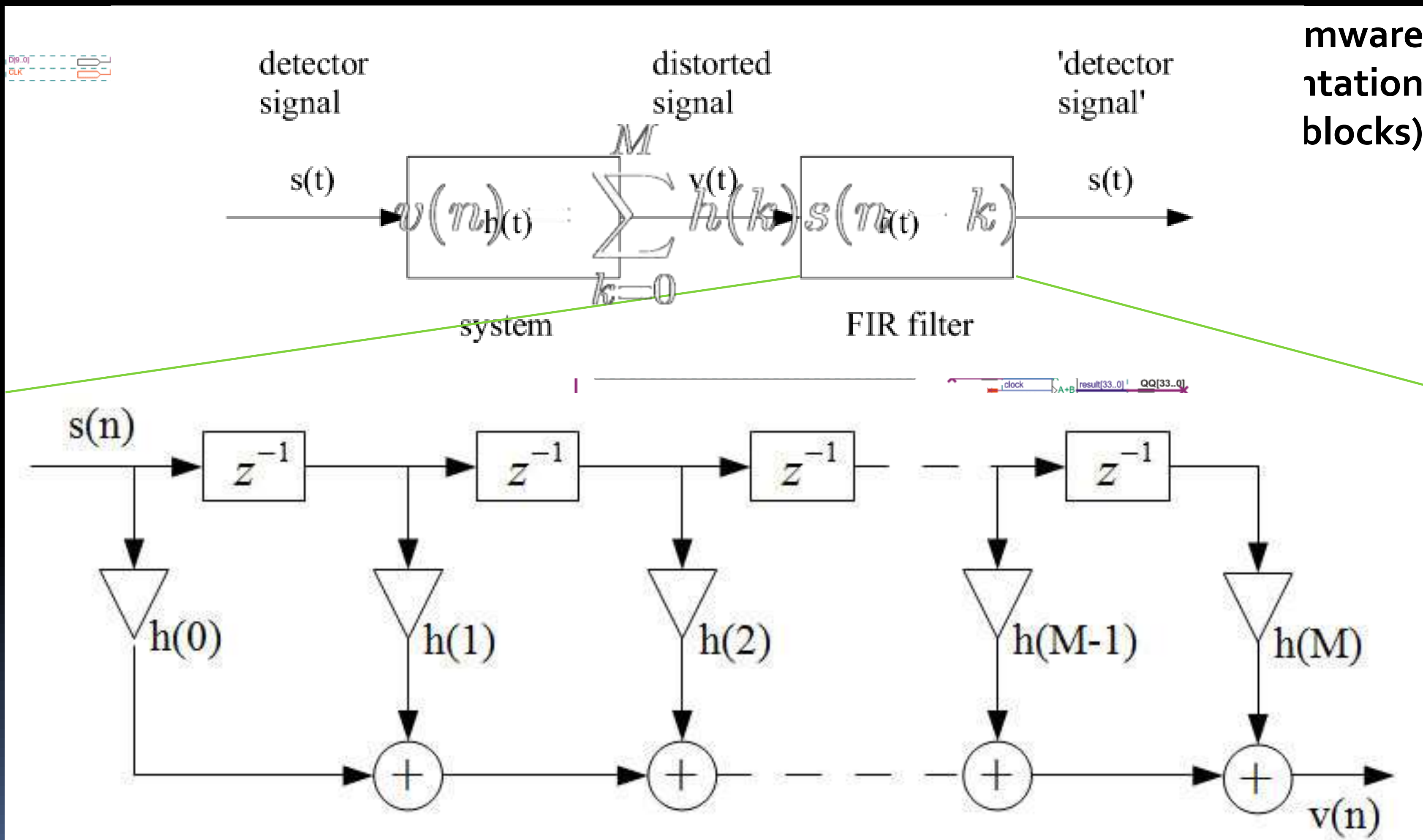
Cable Transfer Function

- Problem: non-linear attenuation depending on cable length



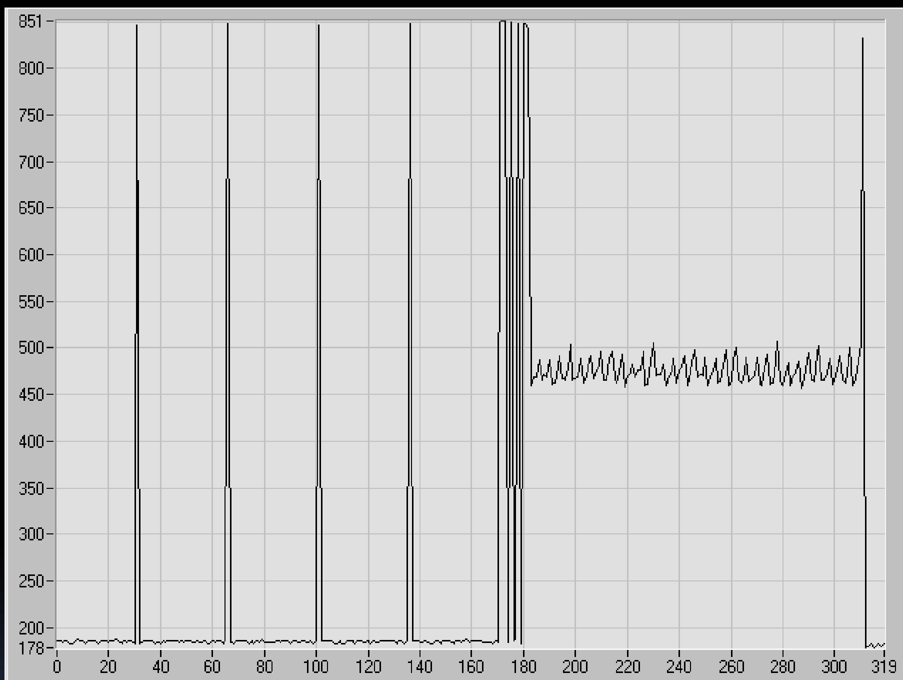
$$H(f) = e^{-kl(1+j)\sqrt{f}}$$

Solution: FIR Filter

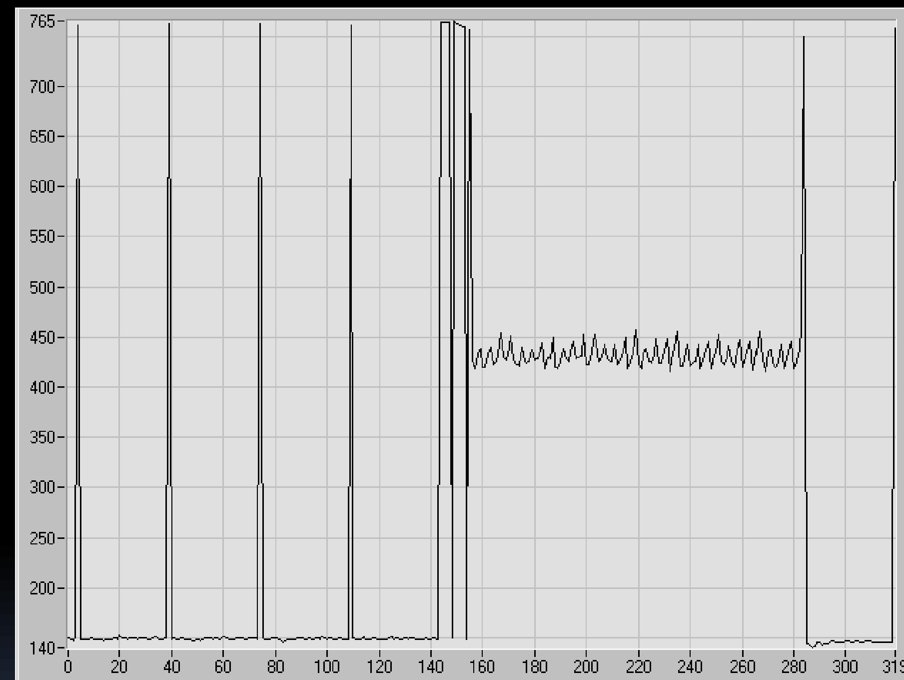


FIR Filter Results

Channel A



Channel B

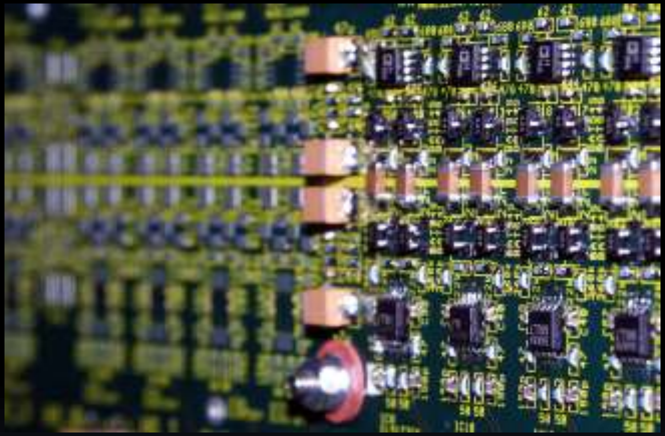


Raw APV25 output **without** FIR

- FIR filter with 8 coefficients operating continuously at 40MHz
- Removes cable loss and reflections due to imperfect termination!

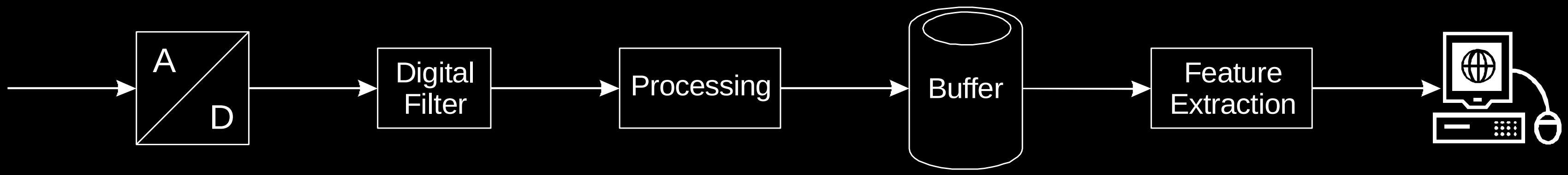
Signal Transmission Summary

- Signals of large number of readout channels to be transmitted to back-end for data processing
- Options: copper cable or optical fiber
- Copper is much cheaper, but has frequency-dependent loss
  - Can be compensated e.g. with digital FIR filter at back-end
- Optical links are more complicated to handle
  - Usually digital with AC coding
  - Exception: CMS Tracker uses analog optical links



Readout Chain – Back-End

- Back-end part:



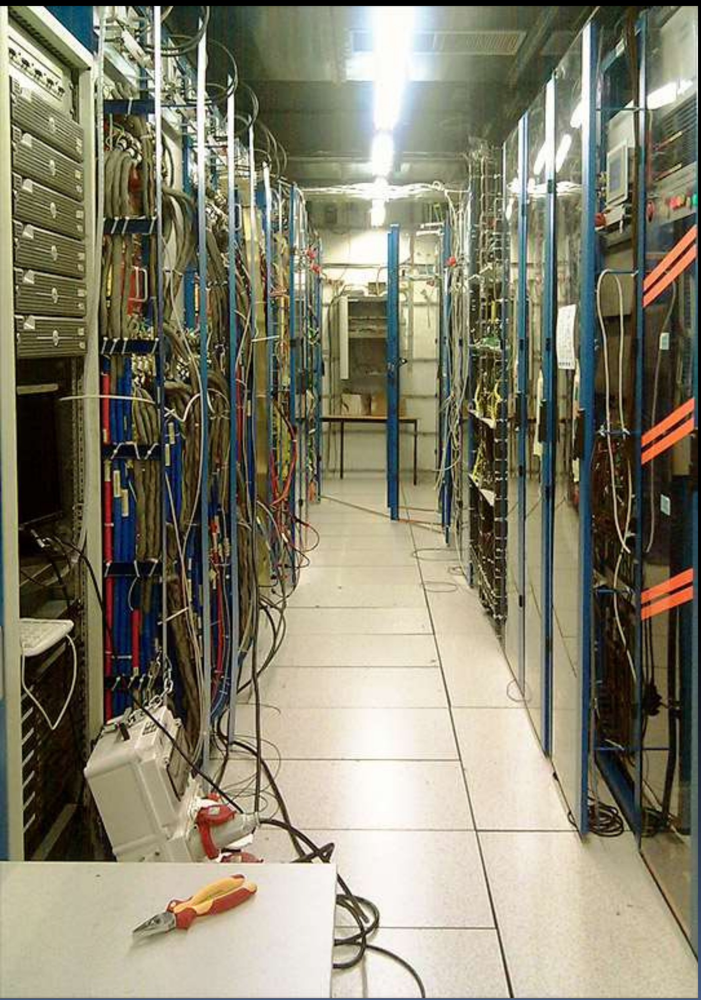
- Back-end is typically built using COTS (components off the shelf) = commercially available parts
  - No radiation
  - No magnetic field
  - Not as crowded as in the detector
- Often using lots of 19” racks

What Is a 19” Rack?

- Standardized mechanical structure (frame)
  - Width is always 19” (48.26cm)
  - Height and depth can vary
  - Many different styles offered by industry
  - Also widely used in computing and audio engineering




19" Racks in Particle Physics



DAQ and electronics-hut of Belle @ KEK (Japan)

Underground electronics cavern of CMS @ CERN

What to Put Into a Rack?

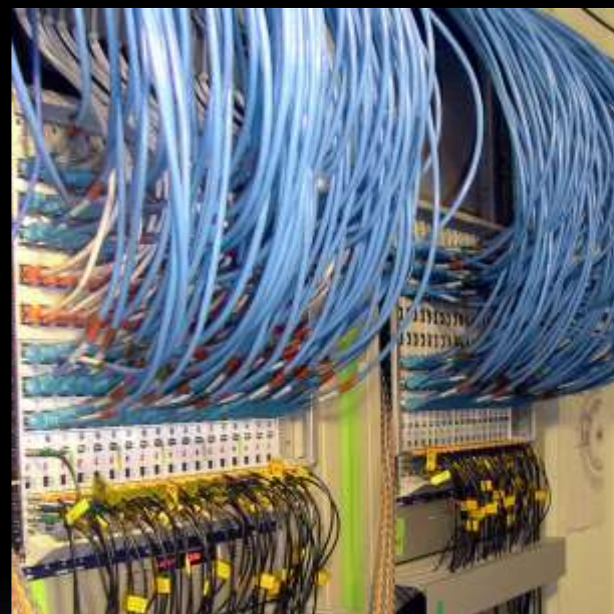
- Electronics:
  - Crates, cooling units
- Computing:
  - Servers, routers, storage (disk arrays), ...
- They are all 19″ wide
- Height is measured in units (“U”)
  - 1 U = 1.75″ = 4.445cm (typical height for a rack server)
- Almost any depth (up to 1m)

What Is a Crate?

- Standardized frame that holds several electronics boards
  - LHC Standard: VME (Versa Module Eurocard), size 9U
  - Obsolete: CAMAC, Fastbus
  - Modern: xTCA
- All those standards describe
  - Geometry of modules
  - Electrical interface, power supply
  - Bus system for communication with crate controller & PC
- Old, but still used everywhere in our community:
  - NIM (logic modules without any data bus)

VME (9U) Crates

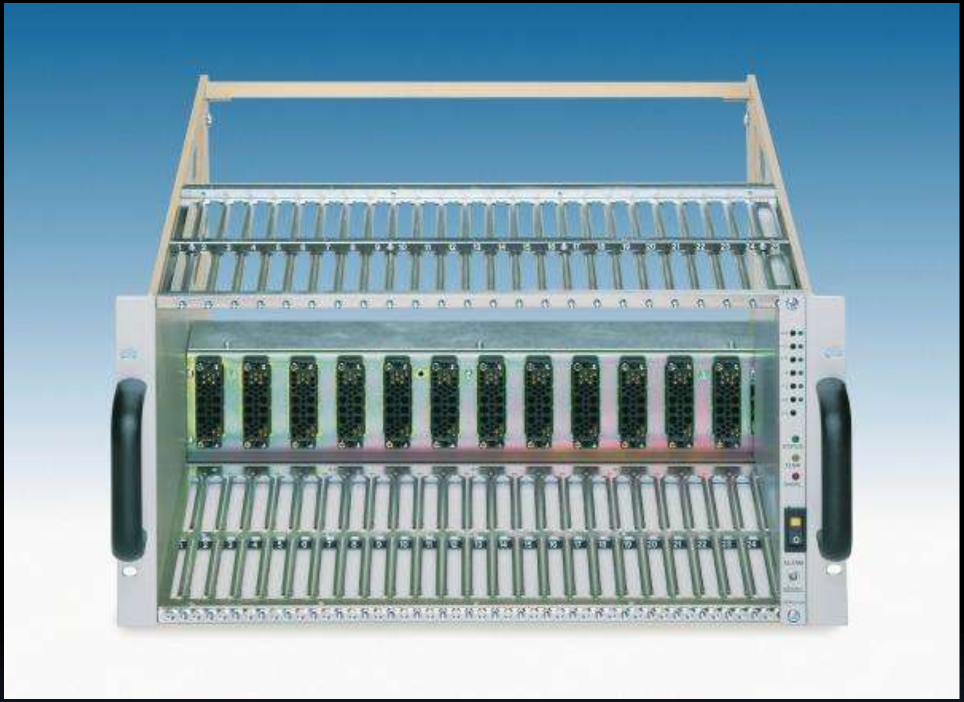
Empty crate
as sold by industry
(3 leftmost slots are 6U)



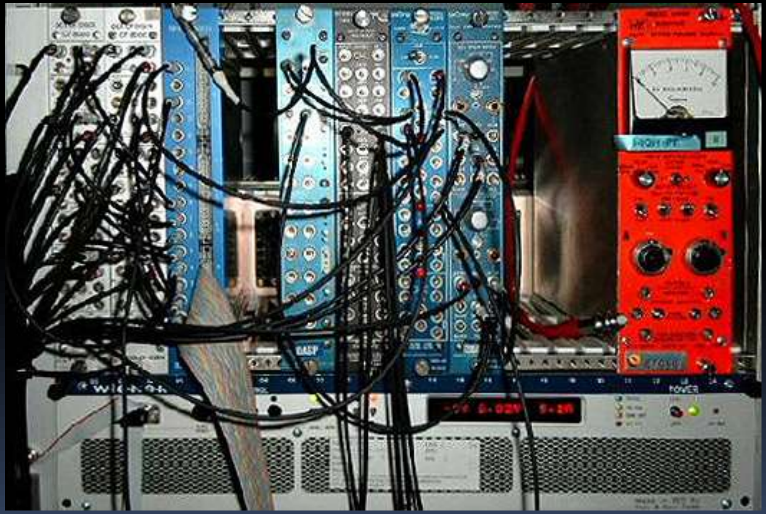
Belle Silicon
Vertex Detector
(cable input)

CMS Pixel-FED
(optical input)

NIM Crates

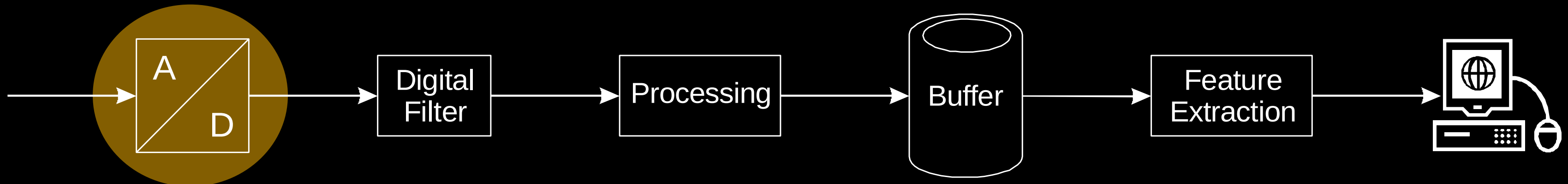


Empty crate
as sold by industry



Crates with modules and cables

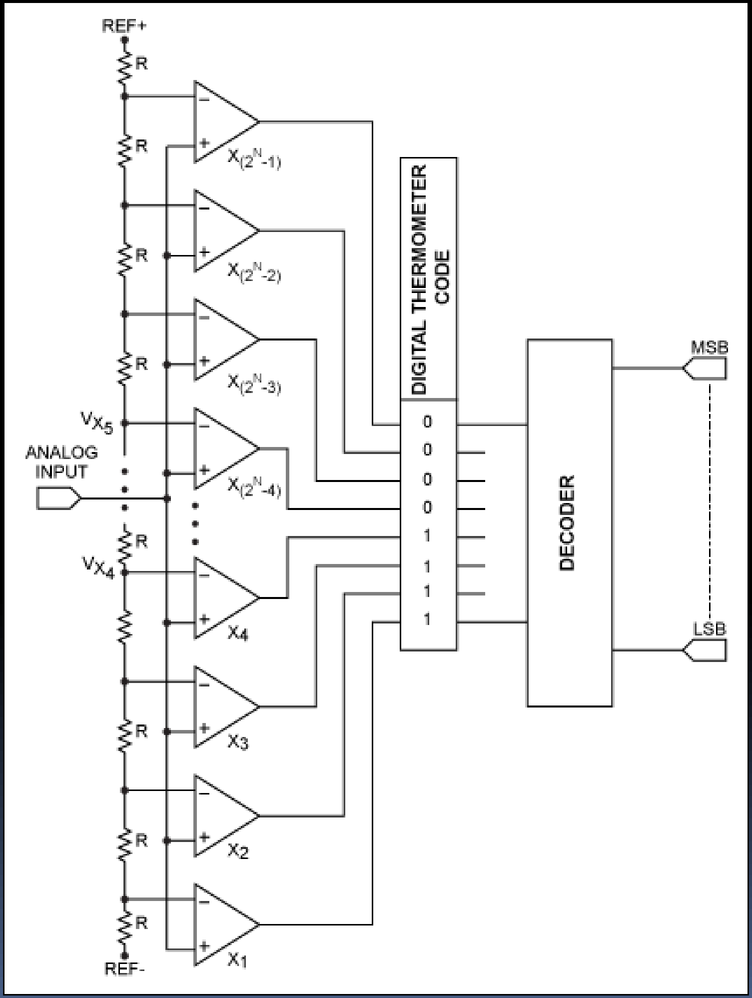
Analog-to-Digital Conversion



- Data have to become digital for computer processing
  - Sometimes, digitization already happens at the front-end
- ADC (Analog-to-Digital Converter) has 3 parameters:
  - Concept (circuitry: how the converter works)
  - Number of bits (8…24)
  - Speed (kS/s…GS/s)
  - Large number of bits implies slow conversion and vice versa
  - In our application, we typically need high-speed FADC (flash ADC) with (for example) 10 bits @ 40 MS/s

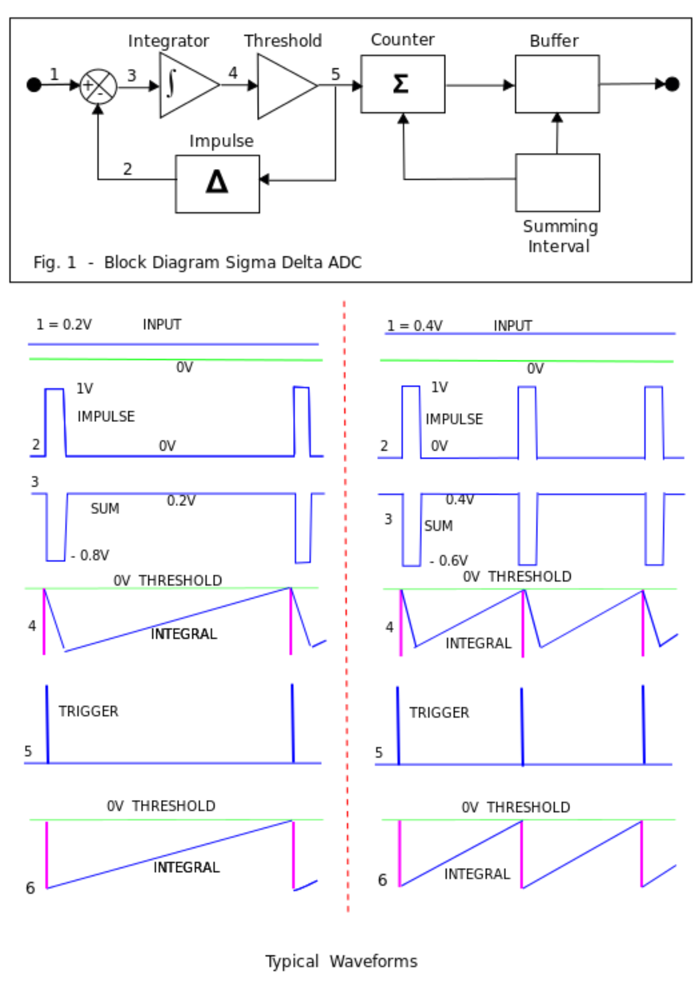
ADC Concept Examples (1/2)

- Flash ADC (our typical choice for readout)
  - High speed
  - Coarse
  - Bank of comparators that produce a "thermometer code"
  - This scheme is not practical for more than ~8 bits
  - Real FADCs use a staged design
  - State-of-the-art:
    2 GS/s @ 12 bits



ADC Concept Examples (2/2)

- Sigma-Delta ADC (typically used for monitoring: precise but slow)
  - Low speed
  - Accurate
  - Ramp with integrator and comparator
  - Integration time to a certain level depends on the input
  - State-of-the-art:
    2.5 MS/s @ 24 bits



However…

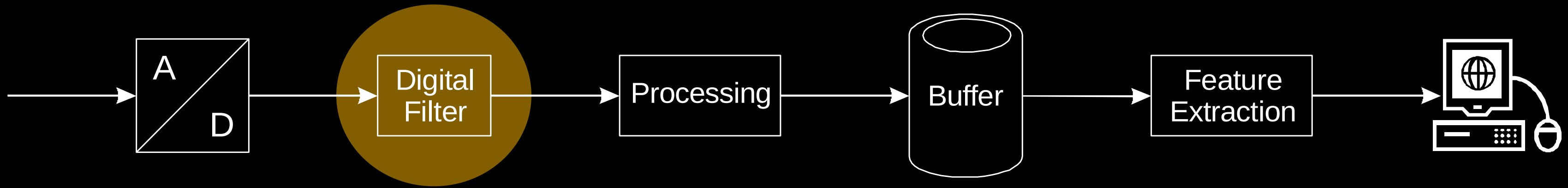
- ENOB (Effective Number of Bits)
  - Describes how many bits actually deliver meaningful data
  - Least significant bits can easily drown in noise – even without any input (noise)
  - ENOB specified in data sheets, e.g. (of a 250kS/s 24bit ΣΔ ADC)
    - 17 noise free bits at 250 kS/S
    - 20 noise free bits at 2.5 kS/s
    - 22 noise free bits at 5 S/S
  - Never delivers 24 meaningful bits!?

- Moreover, we have to consider input noise
  - No sense to digitize with 16 bits if noise is 1/1000 of full range

Digitization Noise

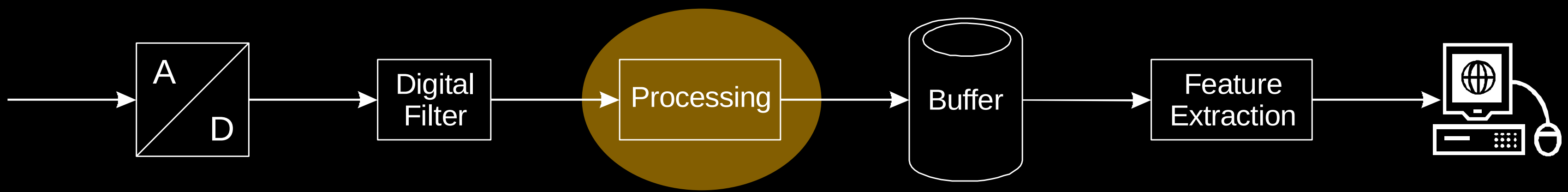
- Even an ideal ADC has a certain noise
- Quantization:
  - Analog input range is mapped to a specific digital value
  - Any input within that range (bin) results in the same digital code
  - This implies an error around the bin center
- Digitization Noise:
  - LSB (least significant bit) quantum = bin width
  - Mean Error = LSB/sqrt(12) ~ 0.29 LSB
  - In measurements, LSB is often called “ADC unit”

Digital Filter



- The purpose of this filter is signal conditioning
- Example: Belle II Silicon Vertex Detector
  - FIR (finite impulse response) filter with 8 coefficients
  - Compensate frequency-dependent damping of cable and eliminate reflections
  - Note: the filter of course cannot physically remove damping or reflections, but polish the signal by numerical calculation such that those effect essentially disappear

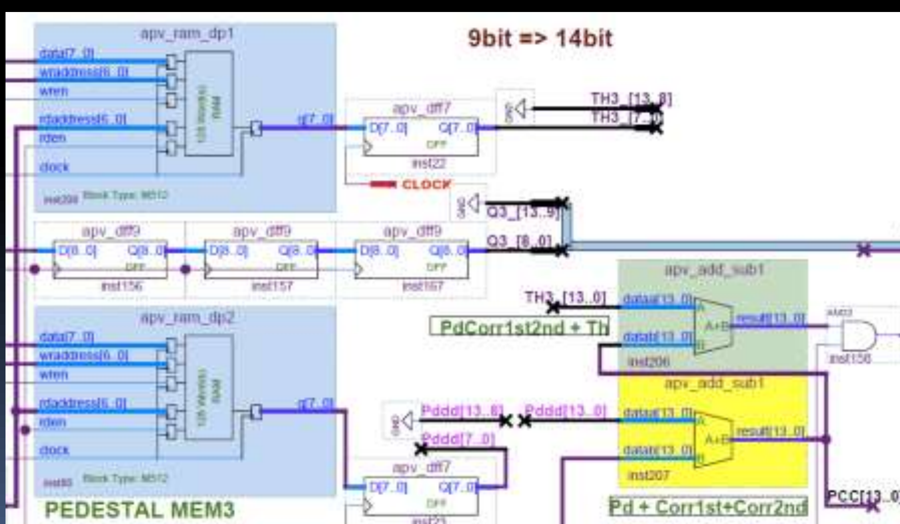
Processing

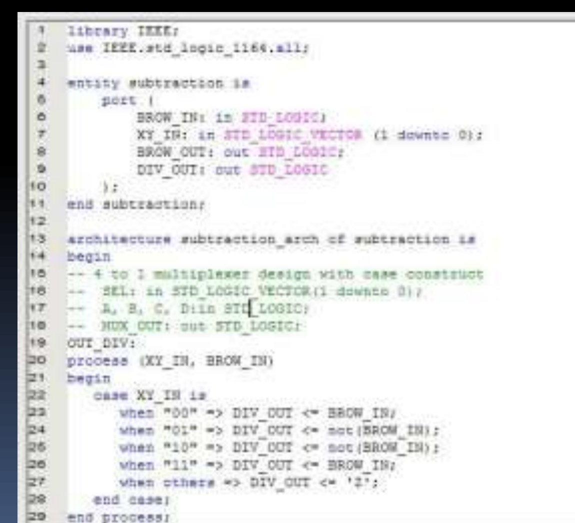


- Digital data processing is a very wide field and obviously depends on the application
- Typically done using an FPGA (Field Programmable Gate Array)
  - This may also include the two subsequent steps (buffer, feature extraction)

What's an FPGA?

- FPGA is a huge array of logical gates which can be combined according to the user's need
- Programming by software using basic gates & library blocks
  - AND, OR, NOT; adder, latch, …, CPU core
  - Either by schematics or by VHDL programming language





```
library IEEE;
use IEEE.std_logic_1164.all;

entity subtraction is
    port (
        BROW_IN: in STD_LOGIC;
        XY_IN: in STD_LOGIC_VECTOR (1 downto 0);
        BROW_OUT: out STD_LOGIC;
        DIV_OUT: out STD_LOGIC
    );
end subtraction;

architecture subtraction_arch of subtraction is
begin
-- 4 to 1 multiplexer design with case construct
--  SEL: in STD_LOGIC_VECTOR(1 downto 0);
--  A, B, C, D:in STD_LOGIC;
--  MUX_OUT: out STD_LOGIC;
OUT_DIV:
process (XY_IN, BROW_IN)
begin
   case XY_IN is
      when "00" => DIV_OUT <= BROW_IN;
      when "01" => DIV_OUT <= not(BROW_IN);
      when "10" => DIV_OUT <= not(BROW_IN);
      when "11" => DIV_OUT <= BROW_IN;
      when others => DIV_OUT <= 'Z';
   end case;
end process;
```

Comparison: FPGA vs. CPU

Property	FPGA	CPU
		
Parallelism	any	a few cores
Speed (clock)	O(100MHz)	O(1GHz)
I/O lines	O(1000)	64
Best suitable for	Fast, simple, massive parallel processing	Complex, serial programs
At the back-end	First low-level data reduction	High-level data processing (DAQ)

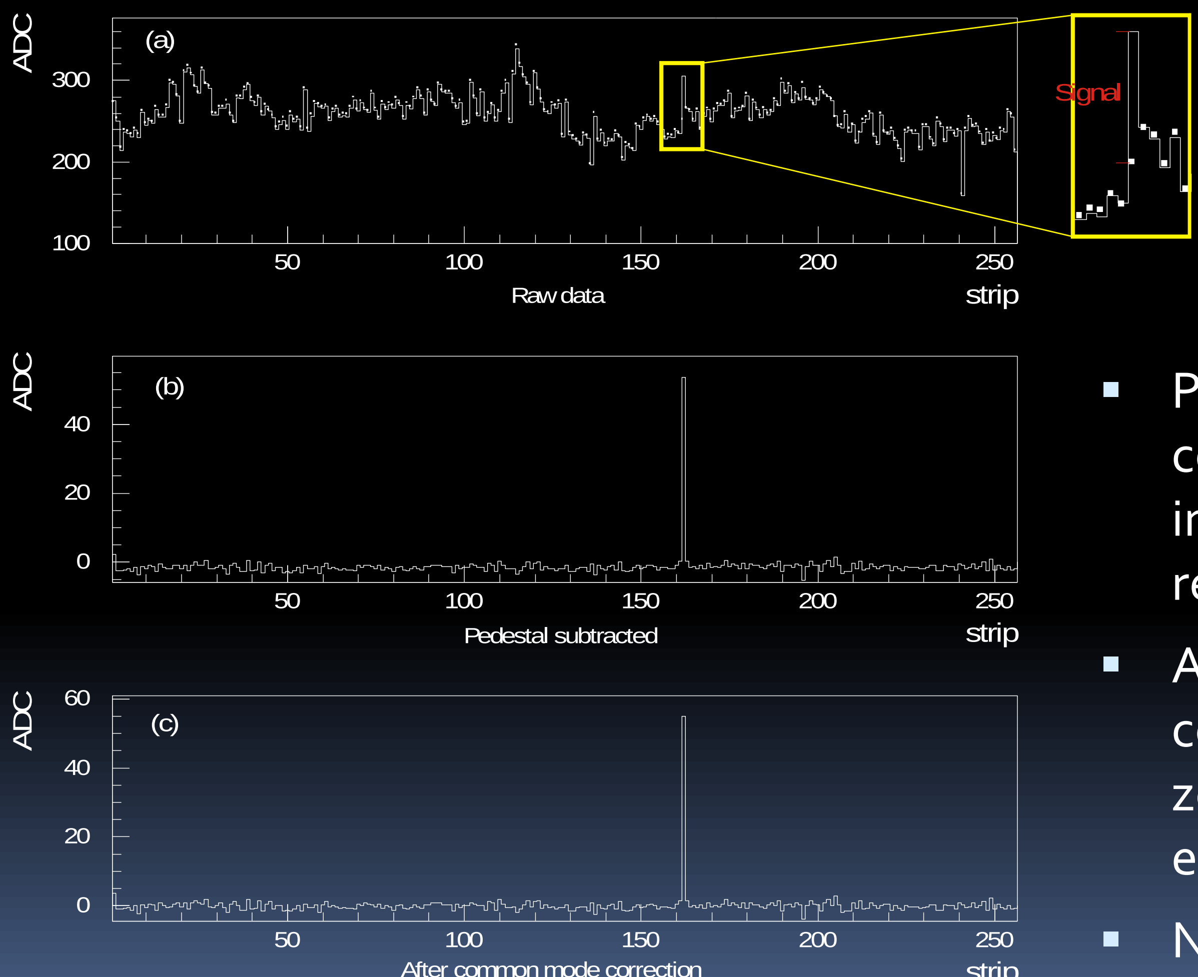
Example: Silicon Strip Data Processing

- Individual processing chain for each input (=front-end chip)
- Analog signal output of one event is a multiplexed stream of 128 data values, but not just the actual strip signal

$$ADC_i = S_i + N_i + P_i + CMN$$

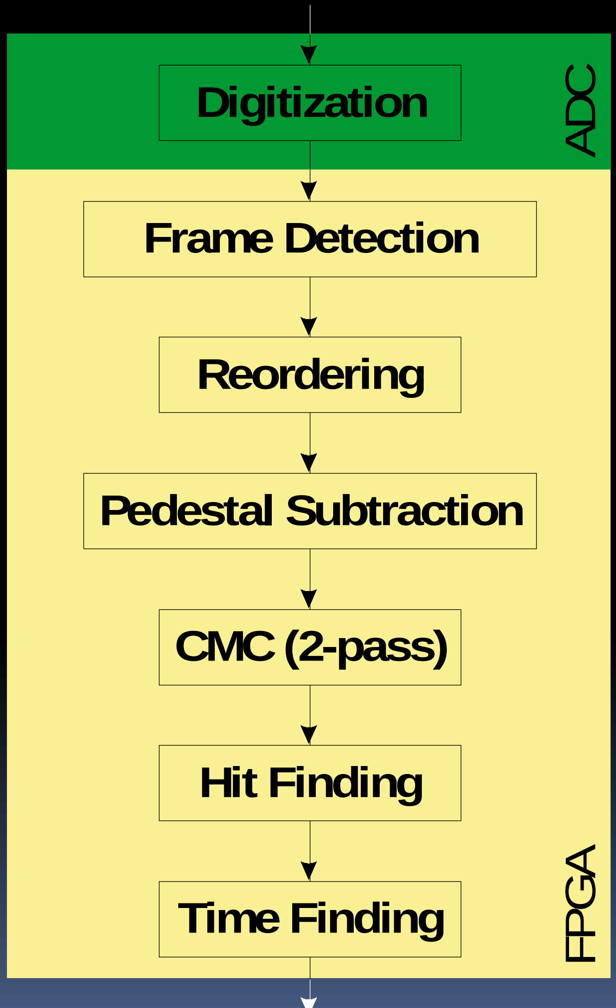
  - i…strip number
  - ADC_i…measured amplitude in ADC units
  - S_i…particle signal (mostly 0 unless particle hit)
  - N_i…noise (random fluctuations)
  - P_i…pedestal (individual "zero" value for each strip)
  - CMN…common mode noise (common to all strips in one event)
- Pedestal and noise can be measured and saved for each channel, CMN is removed event-by-event

How to Process Strip Data?



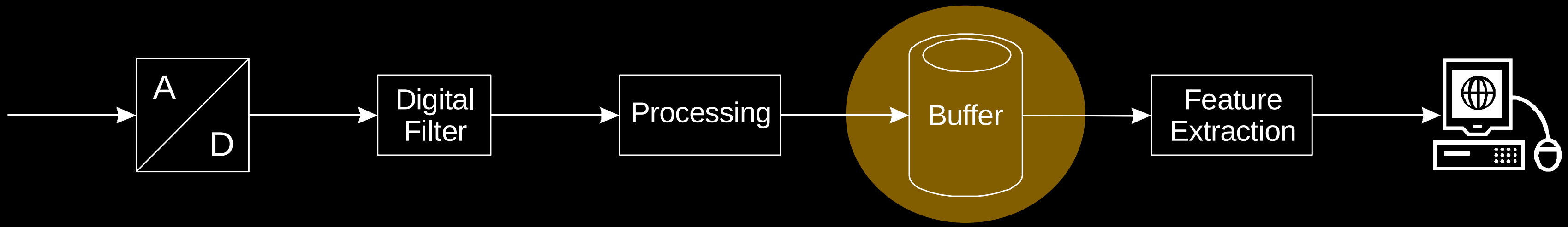
- Data stream with individual pedestals (dots)
- Dominated by pedestal variation
- Pedestals subtracted, common mode noise and individual strip noise remains
- After common mode correction, average is at zero with random noise excursions for each strip
- Next: Apply hit threshold

Typical Tasks for Silicon Strip Detector



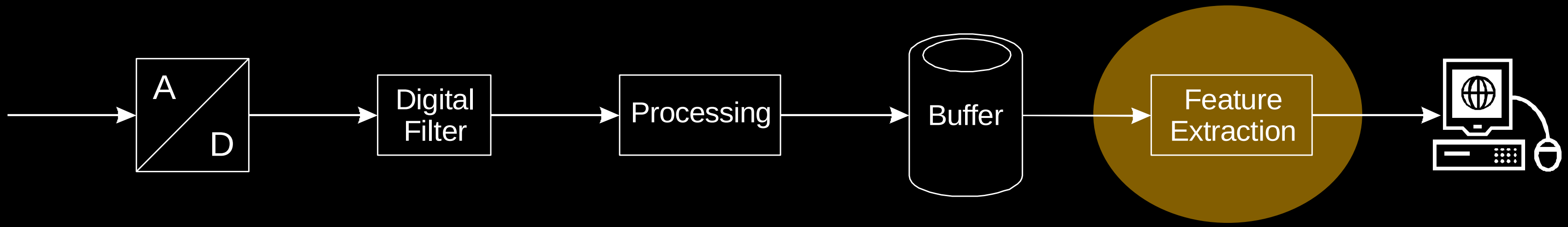
- ADC converts data to digital
- Find and extract strip data
- Put the strip data in natural order (needed if entangled, e.g. APV25)
- Subtract zero value for each strip
- Remove common-mode noise (appears on all strips in common)
- Apply hit threshold (zero suppression, sparsification) = keep only hit data
- Optional post-processing (e.g. APV25)

Processing



- Buffering actually happens in several places in the processing chain
- Should be inserted wherever a delay in data processing can be expected
- Example: Belle II Silicon Vertex Detector
  - ADC to processing is done for up to 48 channels parallel
  - Feature extraction is a centralized feature that exists only once for a group of up to 48 channels $\rightarrow$ delay can occur

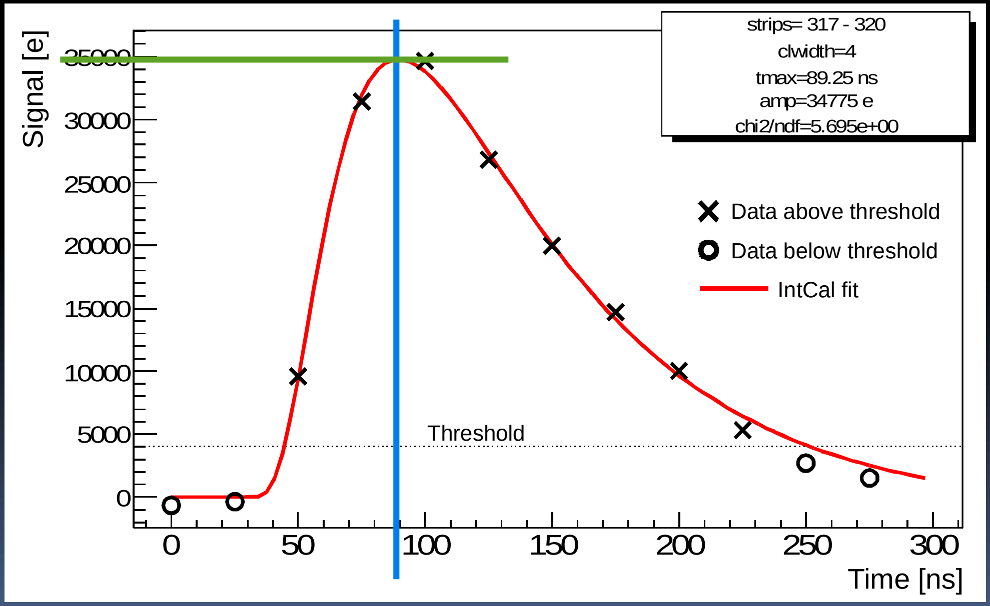
Feature Extraction

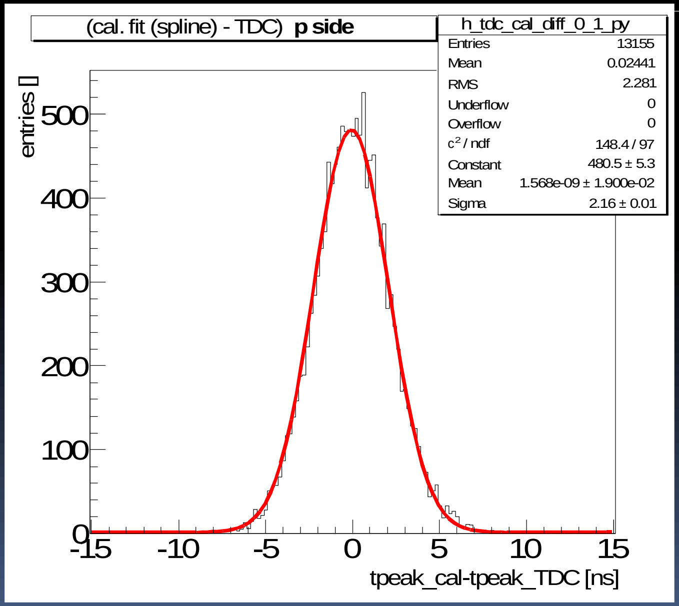


- Final step of hardware data processing
  - All further data treatment is done by software on processors
- Target is to reduce the amount of data by extracting the valuable information
- Example: Belle II Silicon Vertex Detector
  - Reading out several consecutive samples from APV25 pipeline to reconstruct waveform at shaper output

Hit Time Finding

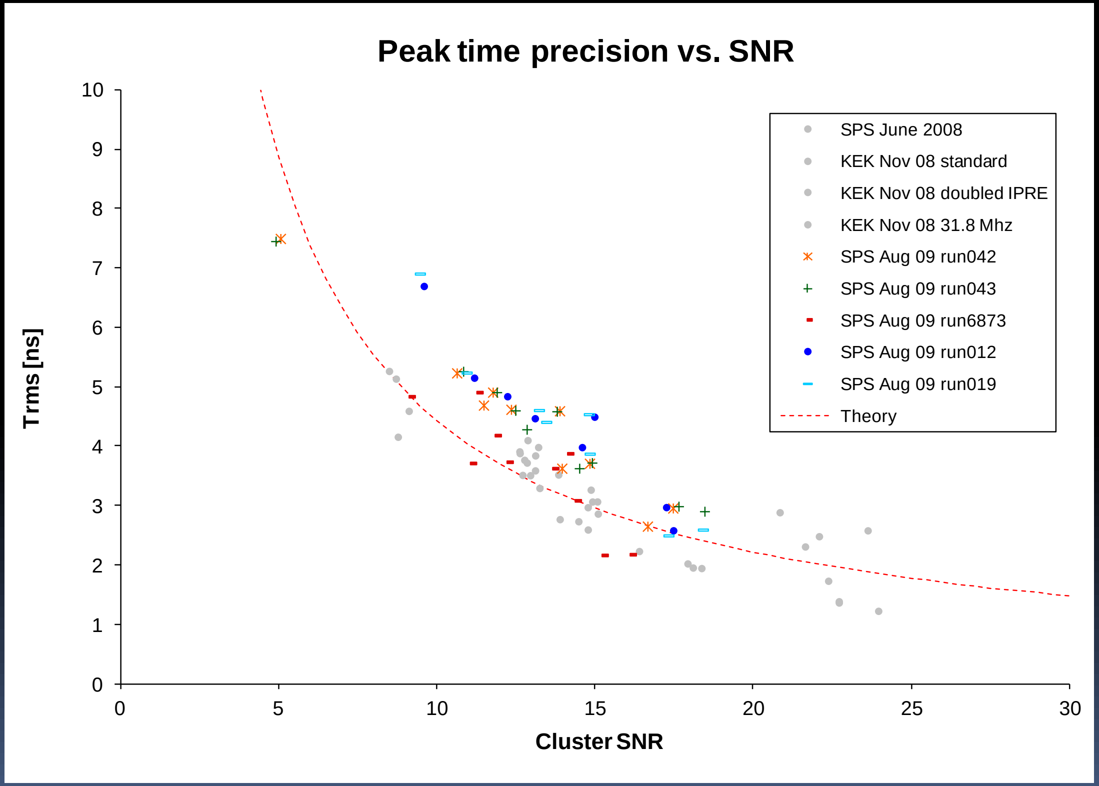
- Shaper output curve is well known with two parameters
  - Peak amplitude, peak timing
- Event-by-event fit of shaping curve determines those two
  - Timing resolution of ~3ns (RMS) measured with APV25





Achieved Hit Time Resolution

- Results achieved in **beam tests** with several different types of Belle II prototype modules (covering a broad range of SNR)
- **2…3 ns RMS** accuracy at typical cluster SNR (14…24)
- **FPGA** implementation is planned



Hit Time Finding Algorithms

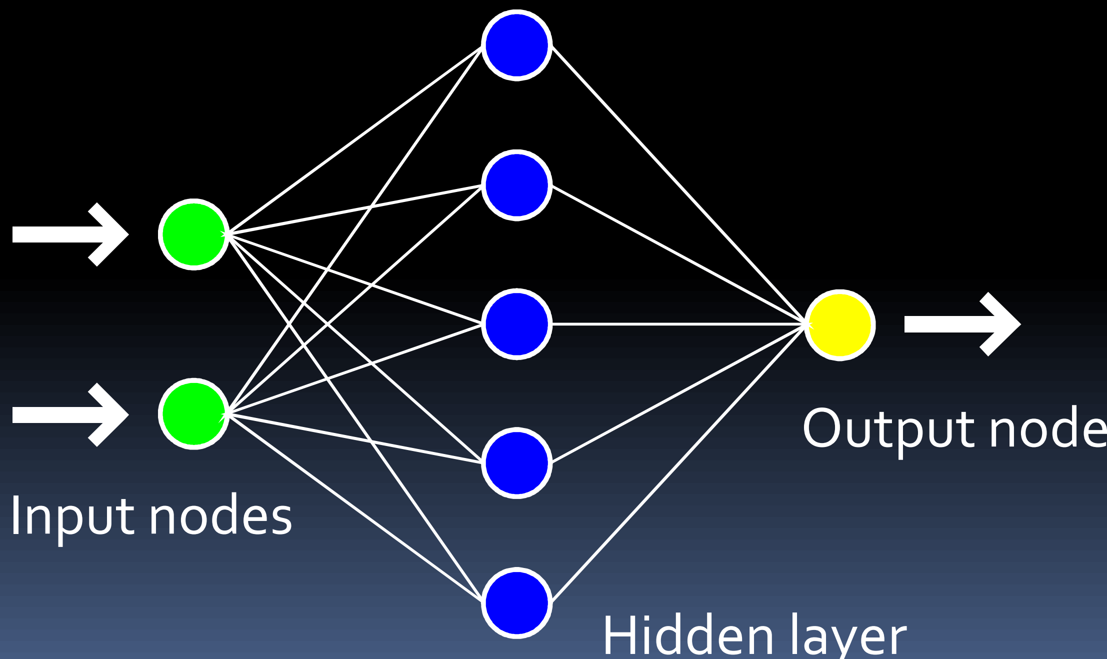
- Almost all the relevant information is contained within the 3 highest samples → enough to consider only those

Method	FPGA?	Comments
Numerical fit	✗	Only for offline software
Lookup table	✓	Consumes lots of memory, but quick Improved efficiency with hash function
Neural network	✓	Can be done using integer multiplications & additions

- All methods were simulated and **neural network** turned out to be most promising
  - Higher precision than numerical fit
  - Only few training events needed
    (many more required to fill lookup table)

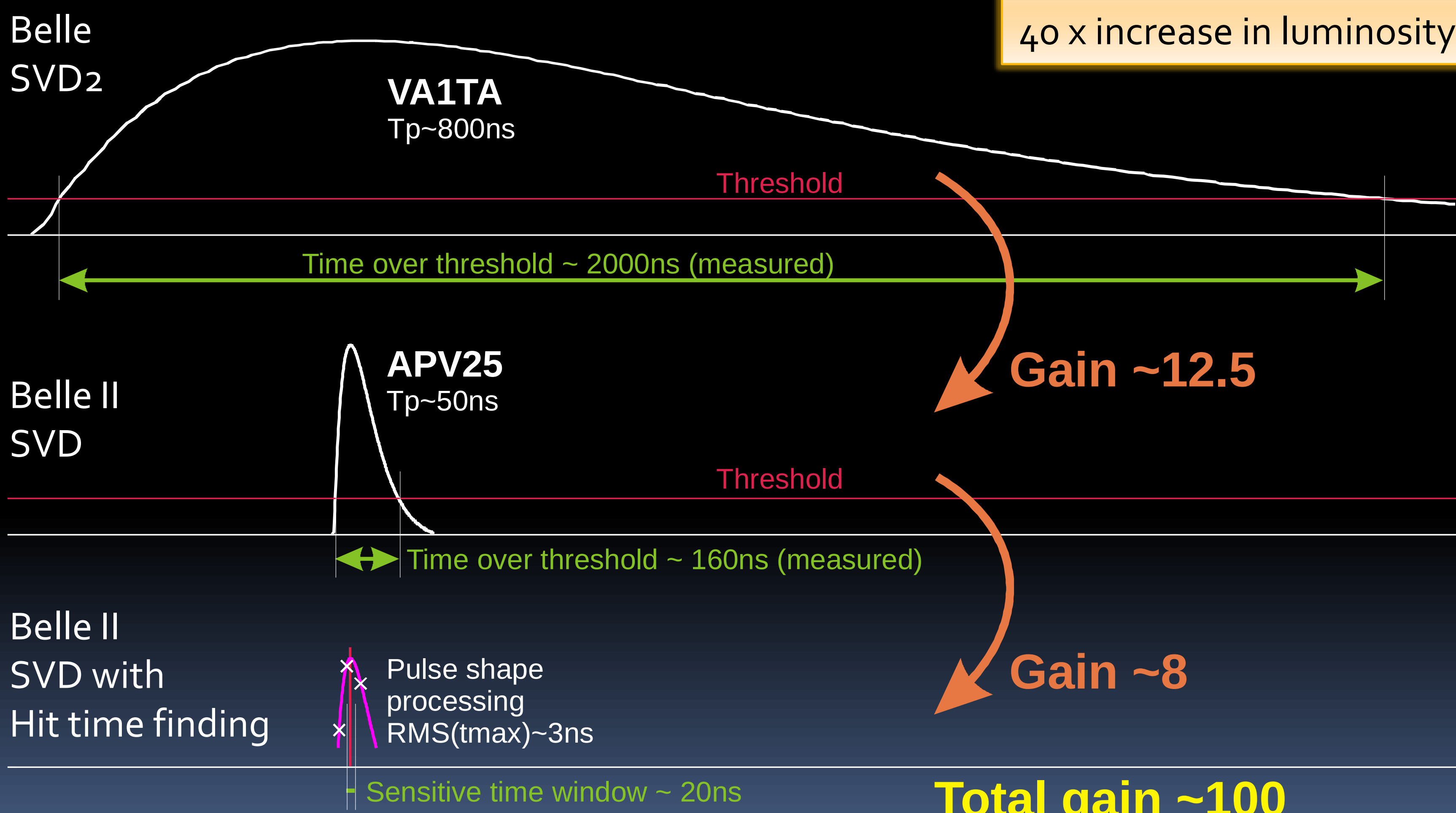
What Is a Neural Network?

- Artificial emulation of the brain
- Weights in each node are adapted (optimized) by training
  - Training = comparing known input/output pairs with actual performance

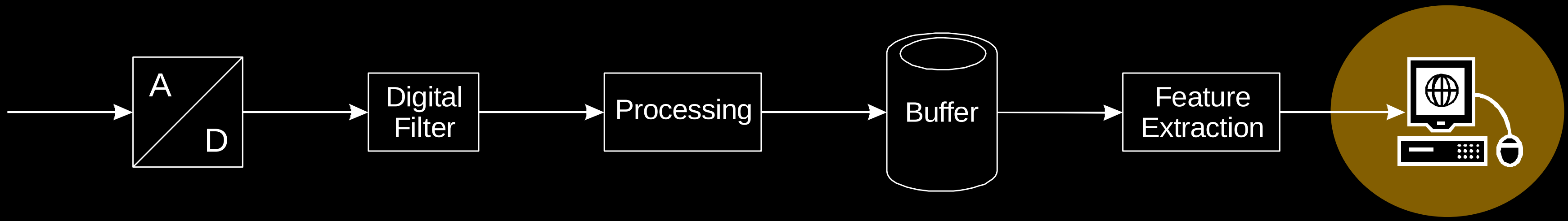


Occupancy Reduction

Belle → Belle II:
40 x increase in luminosity



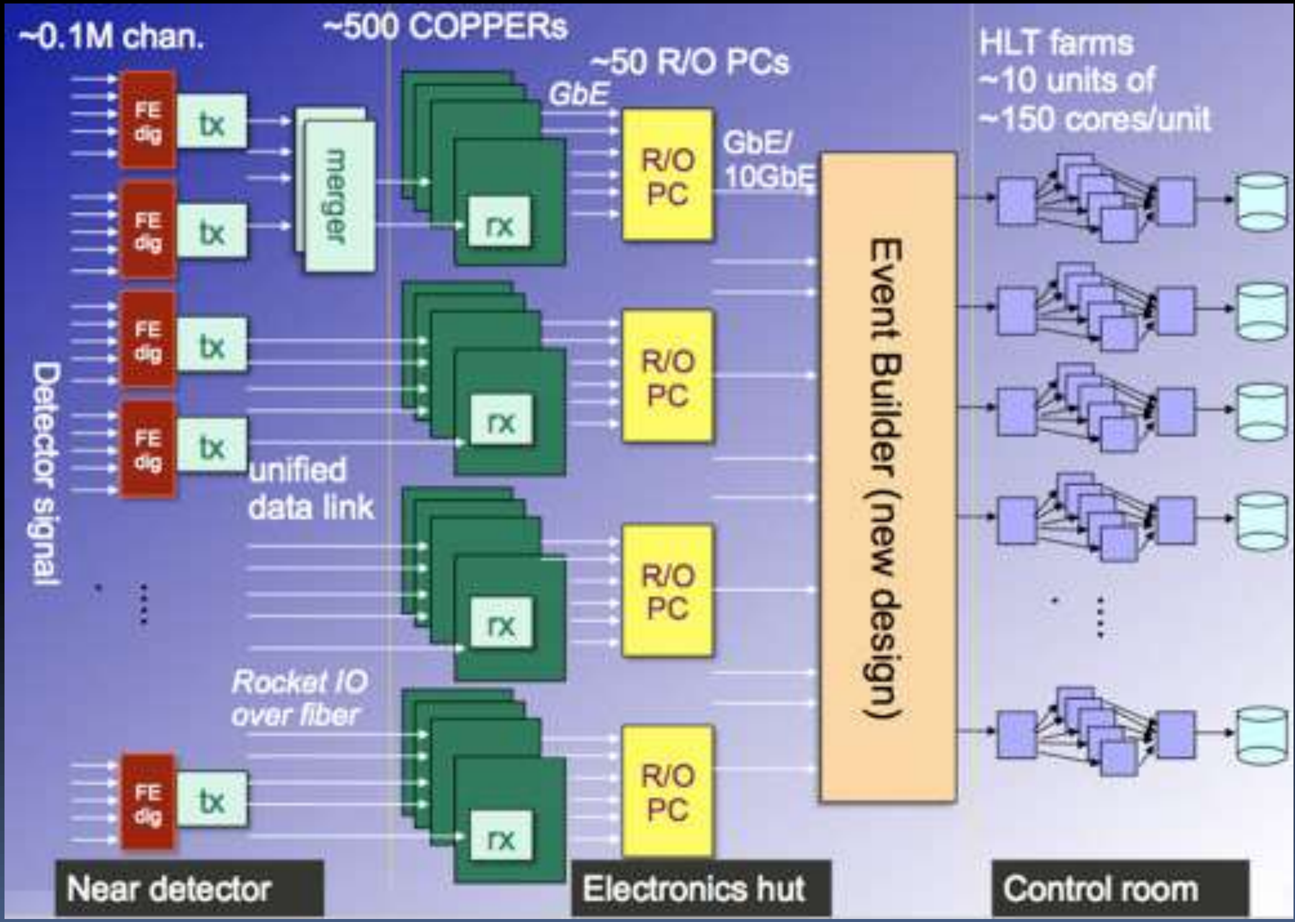
Data Transmission to DAQ



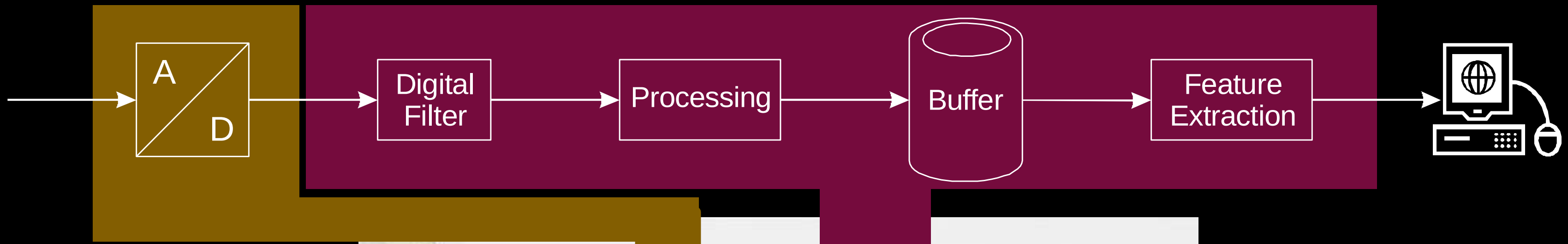
- Digital data interface
  - Elecrical (e.g. GbE or S-Link, a CERN development)
  - Optical (e.g. SONET or GOL, a CERN development)
- DAQ (Data Acquisition) system consists of computer farm and network infrastructure
  - EB (Event Builder): collecting and combining event data from all the different detector elements
  - HLT (High Level Trigger): performs online analysis to find interesting events worth to be stored for offline analysis

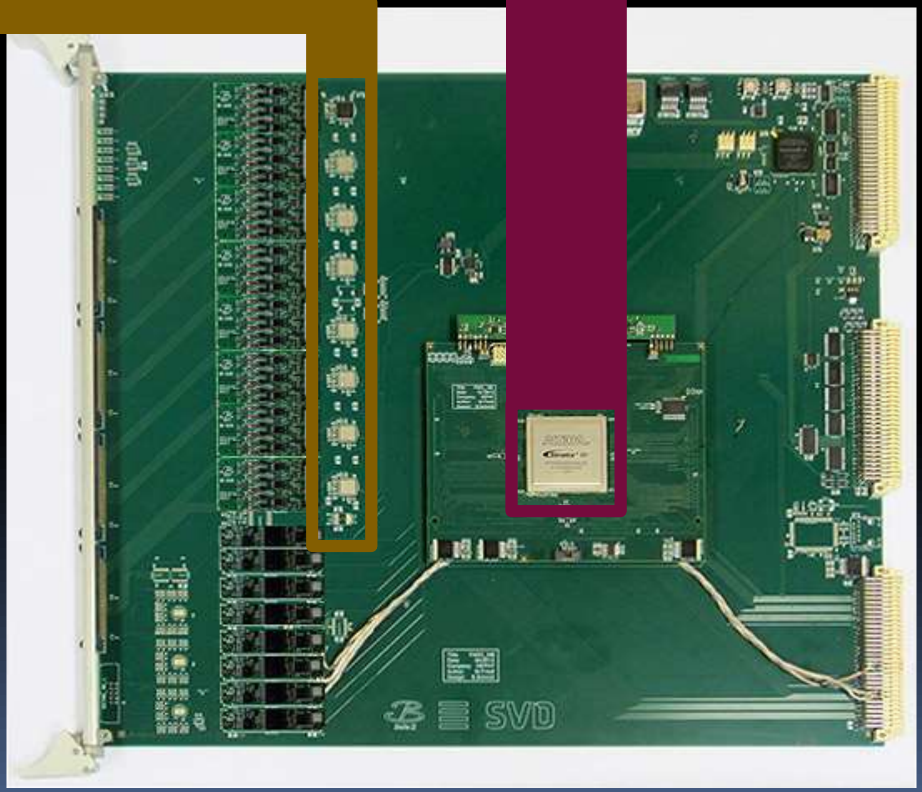
Example: Belle II

HLT Rack | Front-end | Data Collection & EB | HLT



Full Picture

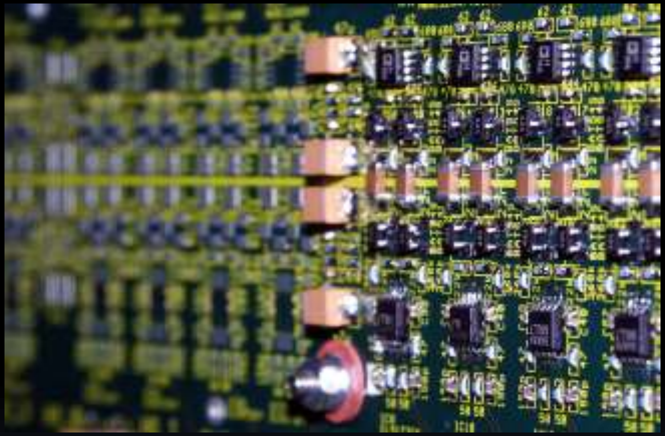




Belle II "FADC" readout board

Back-End Signal Processing Summary

- Performing digitization, data processing (reduction) and output to subsequent DAQ (computer farm) stage
  - Pedestal subtraction, common mode correction, zero suppression
- Boards following a bus module standard
  - E.g. VME (9U)
- Organized in crates and racks
- Typically using FPGAs (field programmable logic arrays)
  - Ideal for low-level massive parallel processing
  - More powerful than CPUs for such tasks
  - Complex calculations are done in subsequent computer farm



Typical Readout Chain

Readout Chain – Front-End

Signal Transmission

Readout Chain – Back-End

Additional Topics

Trigger

- What is it?

Trigger: Introduction

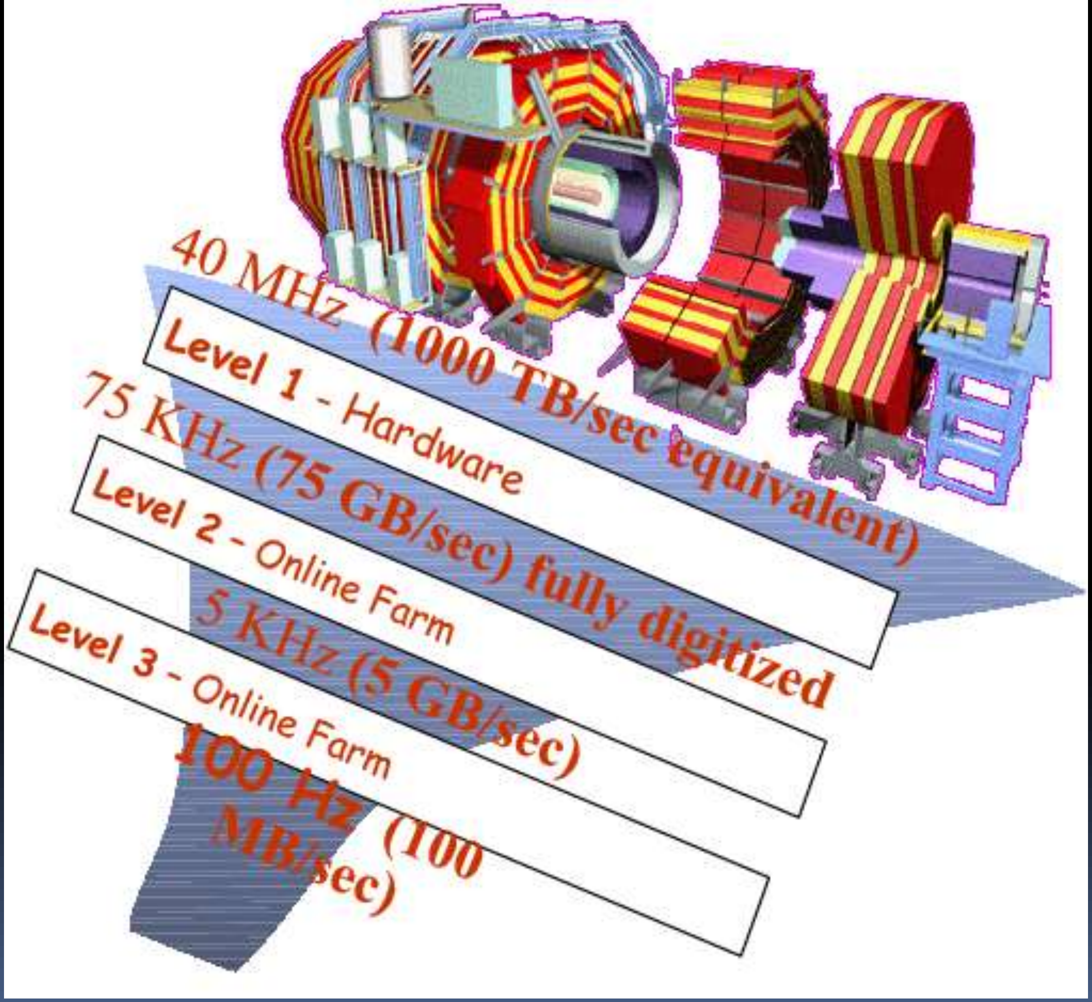
- LHC has 40 Million bunch crossings (events) per second
- Each event (in ATLAS or CMS experiment) produces about 25MB of raw data
- What would be the resulting data rate?
  - **1PB/s = 1000TB/s**
  - Largest hard disk on the market is 6TB
- How to handle such a data rate?
  - Not at all
  - For comparison: presently, **global** internet traffic is about **24TB/s** – very distributed system (source: Cisco VNI)

Trigger: Why? What? Where?

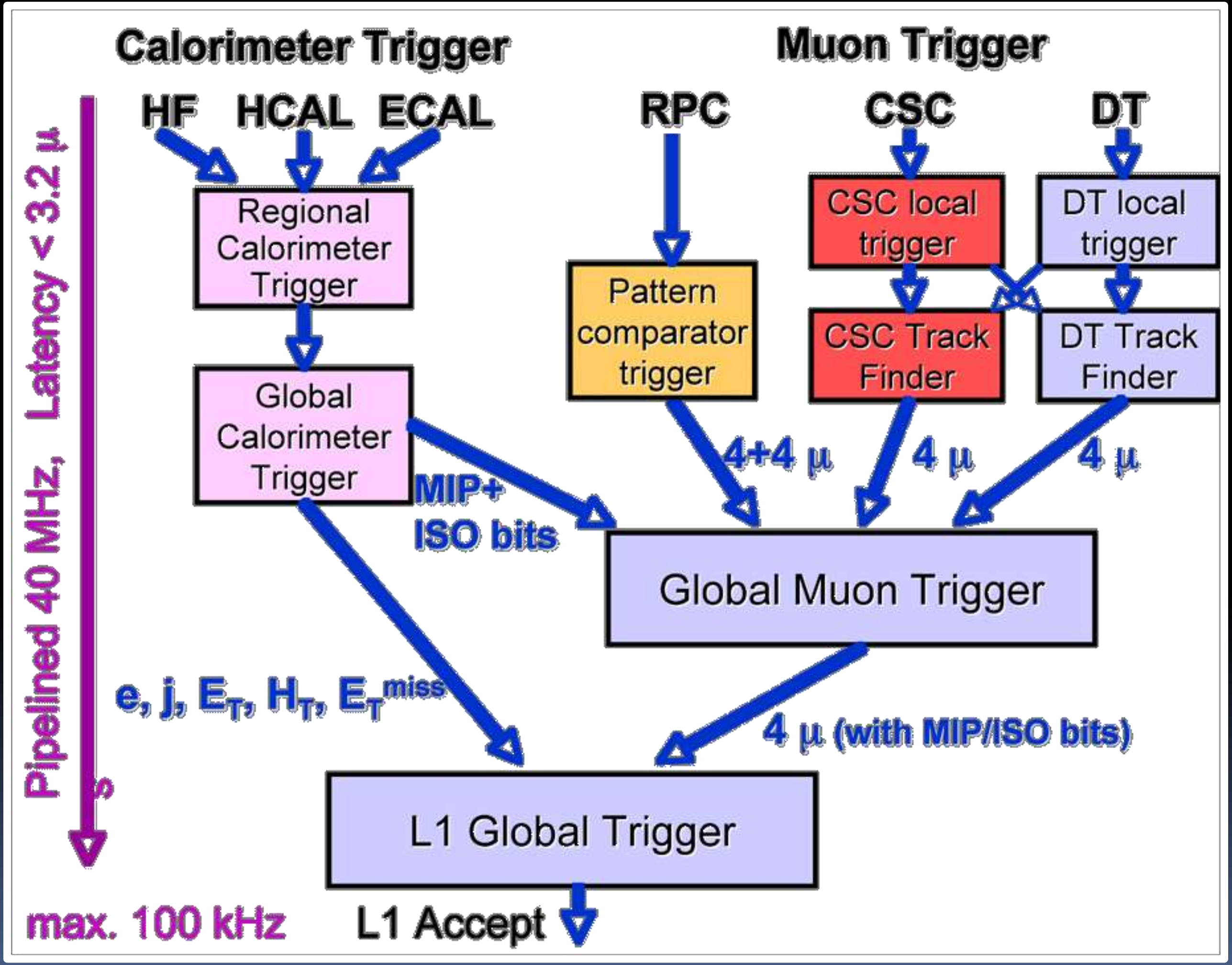
- Conclusion: it is impossible to record all events
- Luckily, most events do not contain new physics
- Trigger must quickly analyze each event to decide whether it could be of interest
  - In the CMS experiment, the trigger latency is about 3μs – 120 events occur during this time
  - Thus, every detector channel must store the last >120 events
  - If decision is yes, then the data are read out and propagated to the next stage
  - Otherwise, data are discarded
  - Reason for pipeline in the APV25 chip

CMS Trigger – Multi-Level Approach

- 3 levels:
  - 1. hardware
  - 2. software
  - 3. software
- Eventually down to 100 events/s
- Data compression down to 1MB/event
- Data rate: 100MB/s



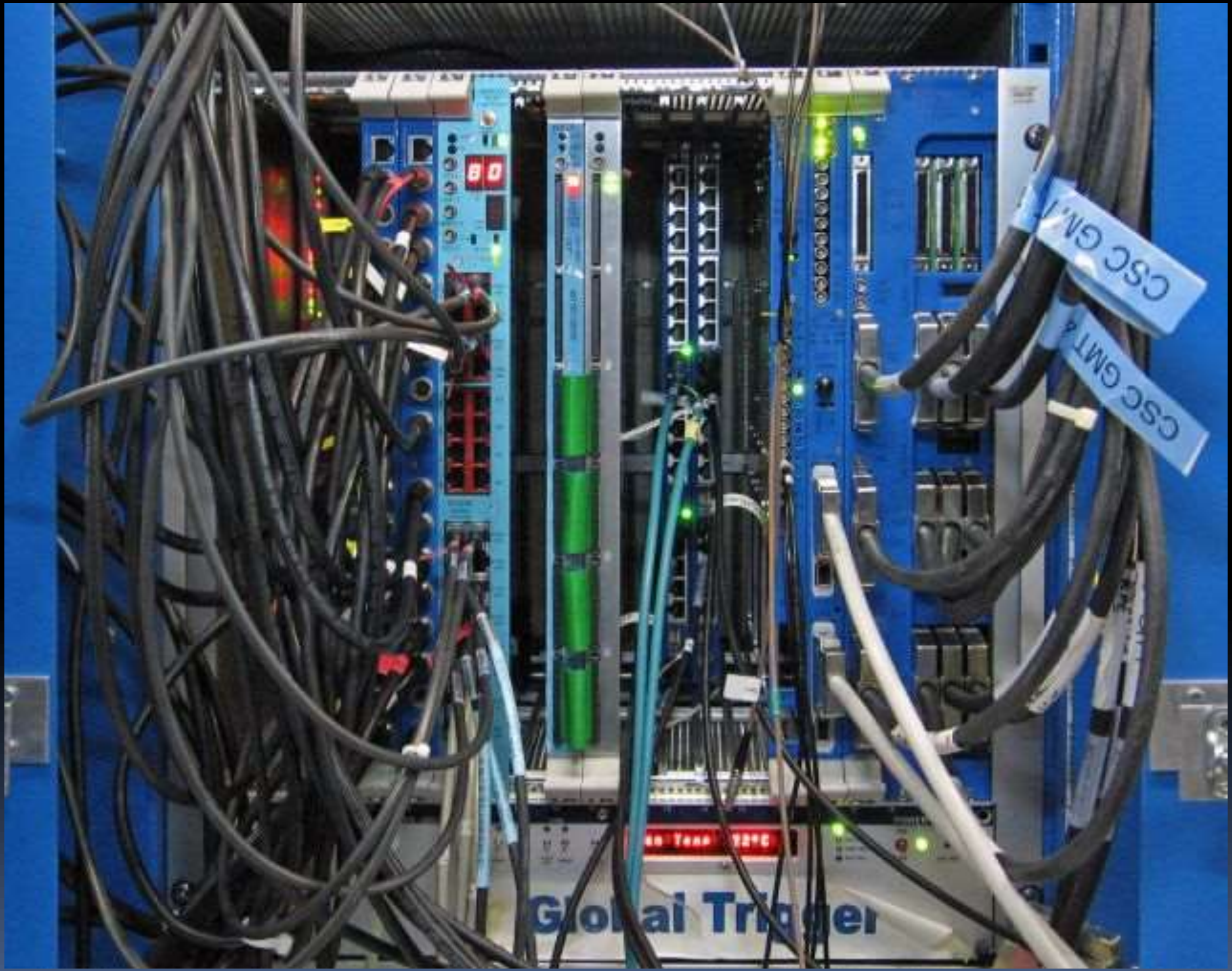
CMS Trigger – Hardware Stage (1/3)



- Receiving and processing data from calorimeters and muon detector (outermost systems)

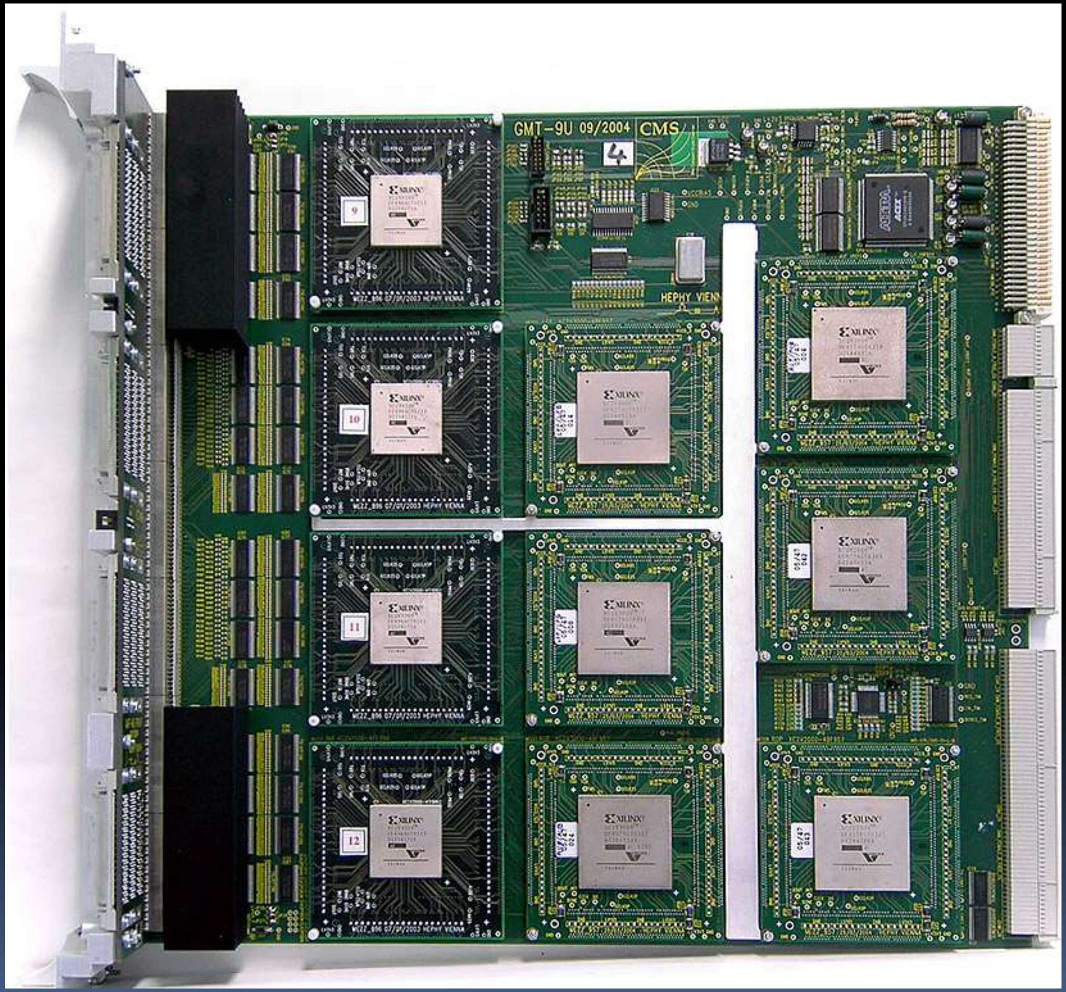
CMS Trigger – Hardware Stage (2/3)

- Final stage: "Global Trigger"
- Crate filled with various electronics boards
- Processing and combining various inputs



CMS Trigger – Hardware Stage (3/3)

- Global Muon Trigger (GMT) board
  - Packed with FPGAs running custom firmware
- Higher levels of trigger are software in computer farms (closely coupled to DAQ)



Thank you for your attention!