

# Experiment 3 - Function Generator

Amirarsalan Shahbazi <sup>a\*</sup>, Mohammad Hossein Mazhari <sup>b</sup>

<sup>a</sup> B.A Student, Department of Computer Engineering, University of Tehran, Tehran, Iran.

\*Corresponding author: Email: shahbaziarsalan@ut.ac.ir. Student ID: 810101451

<sup>b</sup> B.A Student, Department of Computer Engineering, University of Tehran, Tehran, Iran.

Email: smh.mazhari@ut.ac.ir. Student ID: 810101520

## I. Waveform generator

A. Present the simulation outcomes for all waveforms listed in Table 1.

Here we present three waveforms from simple waves module which are square, triangular, reciprocal and three waveforms from DDS module which are sine, half sine and full sine.

Simulation outcomes can be seen in Fig. 1

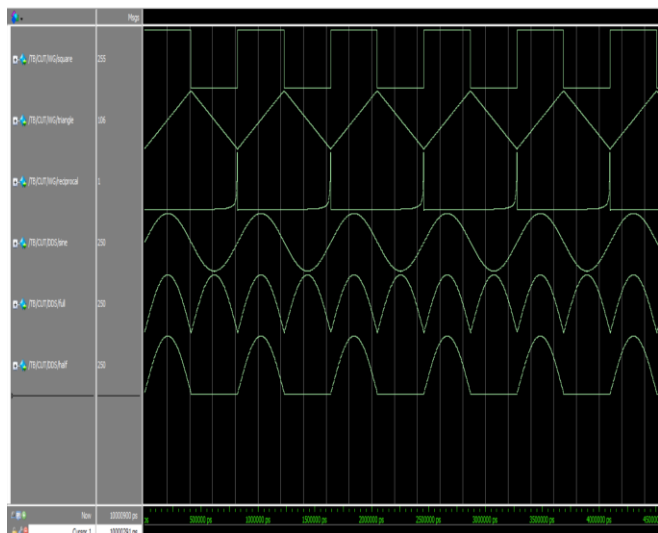


Fig. 1 Table1 waveforms simulation outcome

B. Compare the FPGA resource utilization between the ROM with the romstyle keyword and without it.

When we do not use romstyle FPGA does not consider this part as a memory and does not assign memory bits to it. This is shown in Fig. 2

The scheme of FPGA for this part is also shown in Fig. 3

Flow Summary	
Flow Status	Successful - Sat Apr 13 16:05:15 2024
Quartus II 64-bit Version	12.1 Build 177 11/07/2012 S3 Web Edition
Revision Name	AFG
Top-Level Entity Name	Block1
Family	Cyclone II
Device	EP2K10K10-6AC7
Timing Models	Final
Total logic elements	245 / 18,752 (1 %)
Total combinational functions	244 / 18,752 (1 %)
Dedicated logic registers	29 / 18,752 (< 1 %)
Total registers	29
Total pins	14 / 315 (4 %)
Total virtual pins	0
Total memory bits	0 / 239,616 (0 %)
Embedded Multiplexers 9-bit elements	0 / 52 (0 %)
Total PLLs	0 / 4 (0 %)

Fig. 2 ROM without romstyle

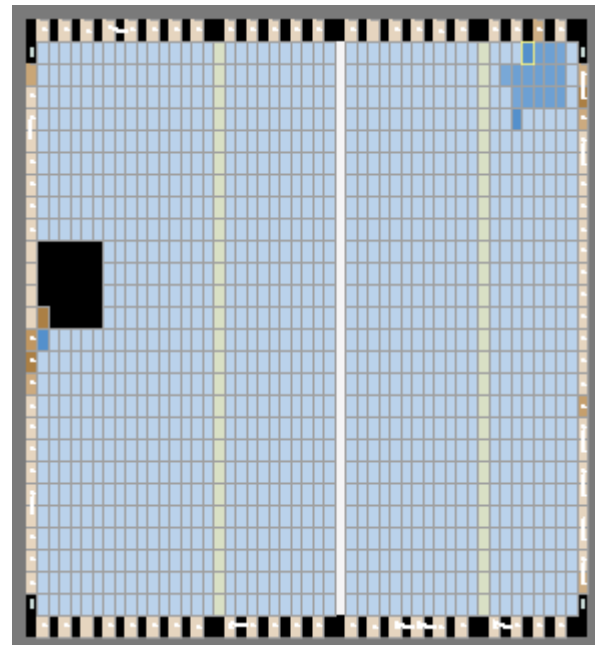


Fig. 3 FPGA without romstyle

As you can see when we use romstyle in FPGA we assign memory bits. This is shown in Fig. 4

Also, FPGA with memory is shown in Fig. 5 which in this figure green cells represent the memories

allocated.

Flow Summary	
Flow Status	Successful - Sat Apr 13 16:53:09 2024
Quartus II 64-Bit Version	12.1 Build 177 11/07/2012 SJ Web Edition
Revision Name	AFG
Top-level Entity Name	Block1
Family	Cyclone II
Device	EP2C20F484C7
Timing Models	Final
Total logic elements	214 / 18,752 ( 1 % )
Total combinational functions	214 / 18,752 ( 1 % )
Dedicated logic registers	29 / 18,752 ( < 1 % )
Total registers	29
Total pins	14 / 315 ( 4 % )
Total virtual pins	0
Total memory bits	512 / 239,616 ( < 1 % )
Embedded Multiplier 9-bit elements	0 / 52 ( 0 % )
Total PLLs	0 / 4 ( 0 % )

Fig. 4 ROM with romstyle

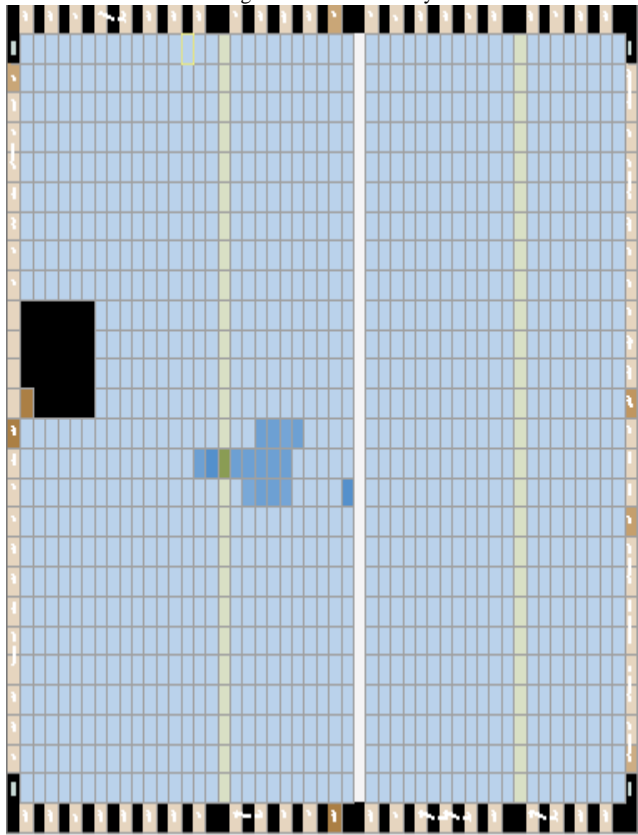


Fig. 5 FPGA with romstyle

C. Provide the synthesis report for the Waveform Generator's design.

Now we show synthesis report of our waveform generator using romstyle in Fig. 6

Flow Summary	
Flow Status	Successful - Sat Apr 13 16:53:09 2024
Quartus II 64-Bit Version	12.1 Build 177 11/07/2012 SJ Web Edition
Revision Name	AFG
Top-level Entity Name	Block1
Family	Cyclone II
Device	EP2C20F484C7
Timing Models	Final
Total logic elements	214 / 18,752 ( 1 % )
Total combinational functions	214 / 18,752 ( 1 % )
Dedicated logic registers	29 / 18,752 ( < 1 % )
Total registers	29
Total pins	14 / 315 ( 4 % )
Total virtual pins	0
Total memory bits	512 / 239,616 ( < 1 % )
Embedded Multiplier 9-bit elements	0 / 52 ( 0 % )
Total PLLs	0 / 4 ( 0 % )

Fig. 6 Synthesis report for the Waveform Generator's design

## II. PWM (Pulse Width Modulation)

### A. Briefly explain the operation of the PWM.

Pulse width modulation (PWM) is a modulation technique that generates variable-width pulses to represent the amplitude of an analog input signal. The output switching transistor is on more of the time for a high-amplitude signal and off more of the time for a low-amplitude signal.

How PWM does that is it uses an 8-bit counter which then if count of that counter is less than the value of the function which comes out of AMP it produces 1 otherwise it produces 0.

*B. Show the simulation results for three data inputs and evaluate the precision of your PWM design.*

First example is the example of a square waveform which its value is always more than the count of counter unless our count reaches to its maximum value which in Fig. 7 it is shown that pwm out is always one except a single clock.

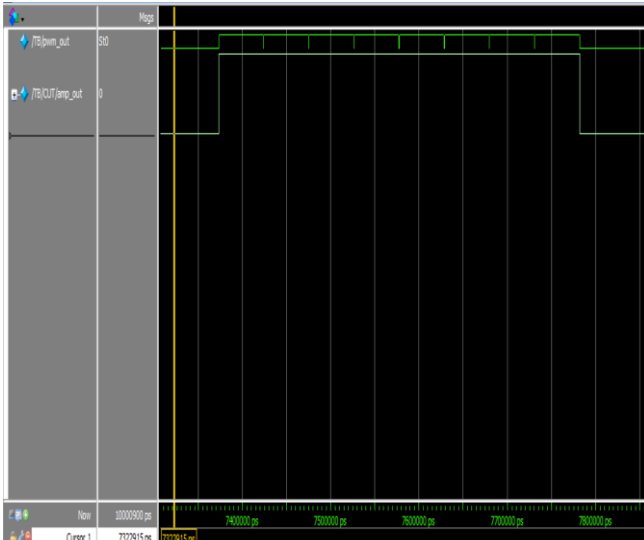


Fig. 7 Square wave PWM simulation

Second example is a triangular waveform which at first has low duty cycle but in the middle when triangle function reaches its maximum it reaches to its highest duty cycle and after that it goes than and makes a symmetrical form for pwm out. Waveform result is shown in Fig. 8.

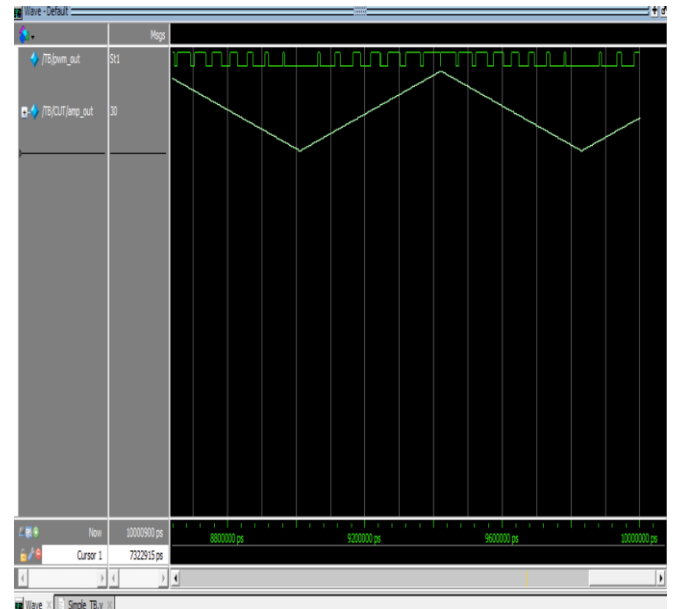


Fig. 8 Triangular wave PWM simulation

Third waveform is reciprocal which as discussed, the result is shown in Fig. 9

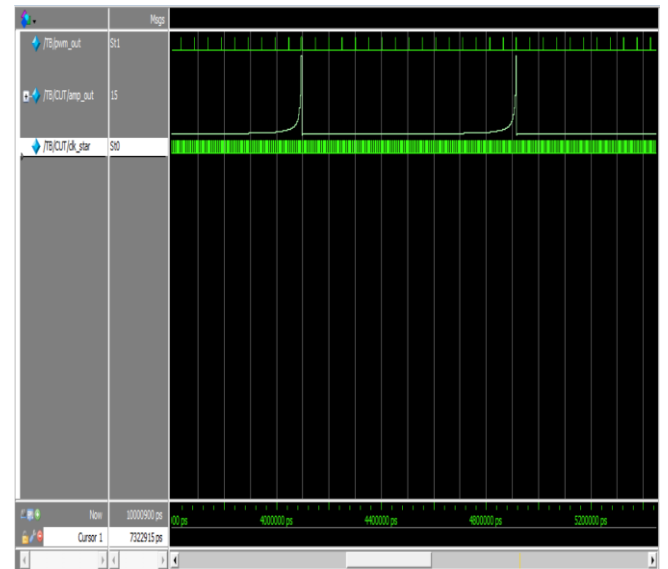


Fig. 9 Reciprocal wave PWM simulation

### III. Frequency Selector

*A. Show the simulation results for three selected frequencies.*

Here by selecting three different parIn for the counter in frequency selector we change the time between signal changes. Here we use a square waveform.

It can be concluded that the more the parIn is the more the frequency will be and the more signal changes in same period of time will happen.

Result for parIn = 11101 is shown in Fig. 10

Result for parIn = 11001 is shown in Fig. 11

Result for parIn = 11111 is shown in Fig. 12

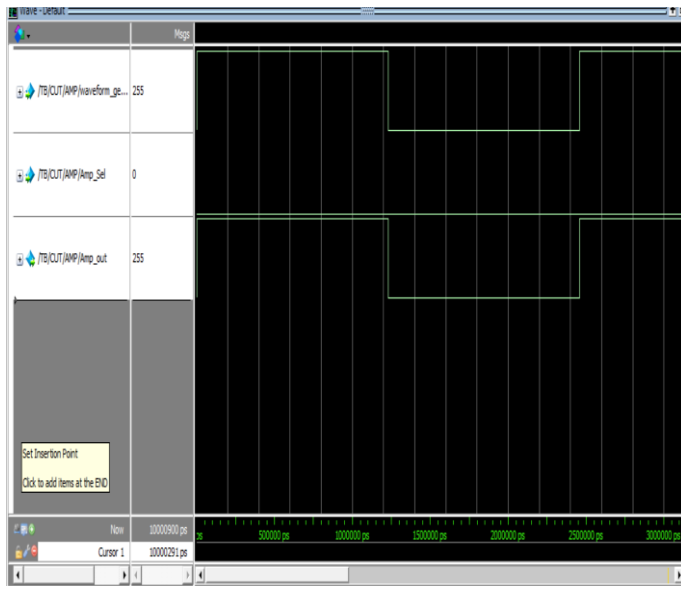


Fig. 10 Frequency selector result 1

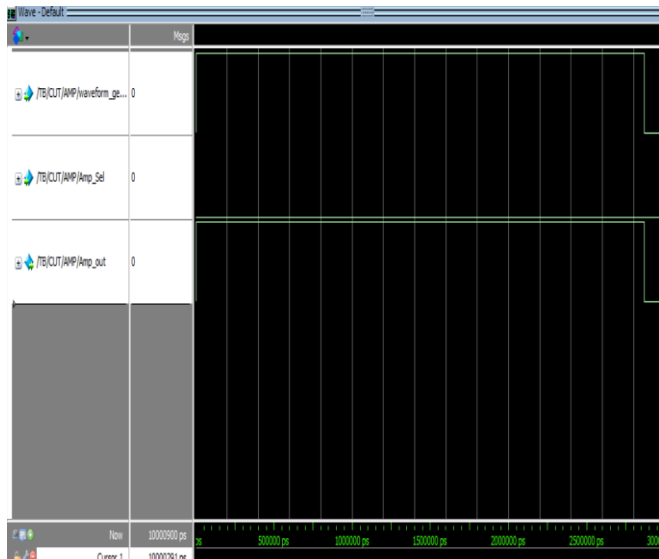


Fig. 11 Frequency selector result 2

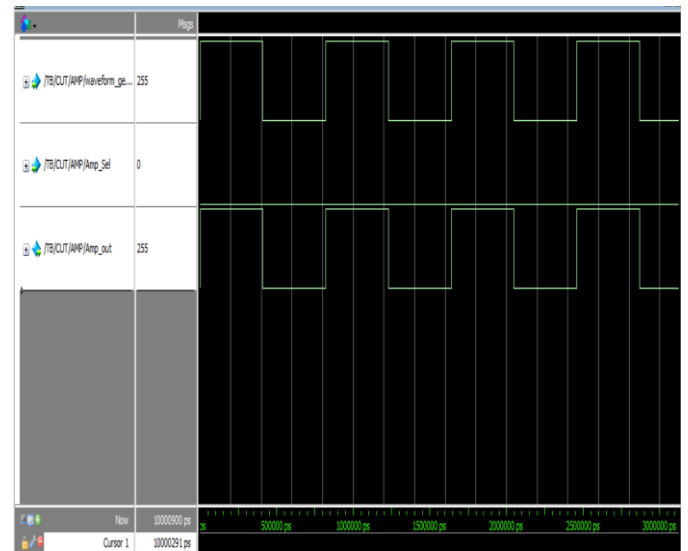


Fig. 12 Frequency selector result 3

#### IV. Amplitude Selector

*A. Confirm the accuracy of your design across three distinct amplitude levels for all waveforms using Modelsim.*

In this part we come up with raw triangular waveform and the try to decrease its amplitude.

$\frac{1}{2}$  amplitude is shown in Fig. 13

$\frac{1}{4}$  amplitude is shown in Fig. 14

$\frac{1}{8}$  amplitude is shown in Fig. 15

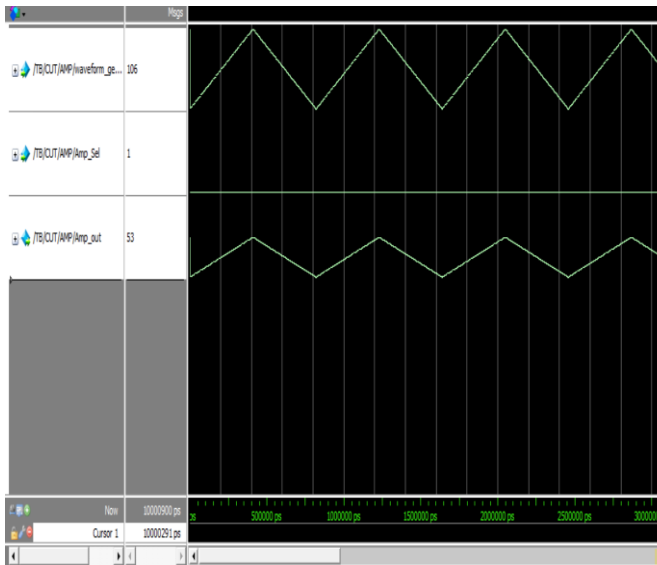


Fig. 13  $\frac{1}{2}$  amplitude triangular

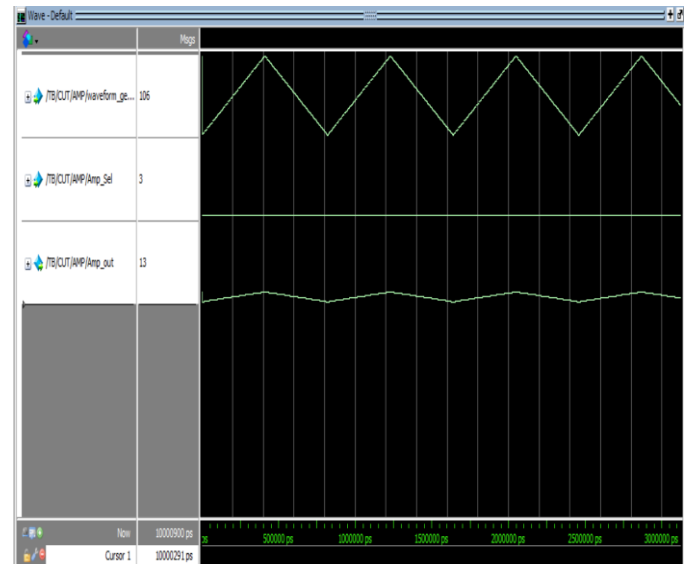


Fig. 15  $\frac{1}{8}$  amplitude triangular

## V. Implementation

*A. Exhibit the schematic diagram of the Function Generator within Quartus.*

The top module which was wired by schematic diagram of Quartus is shown in Fig. 16

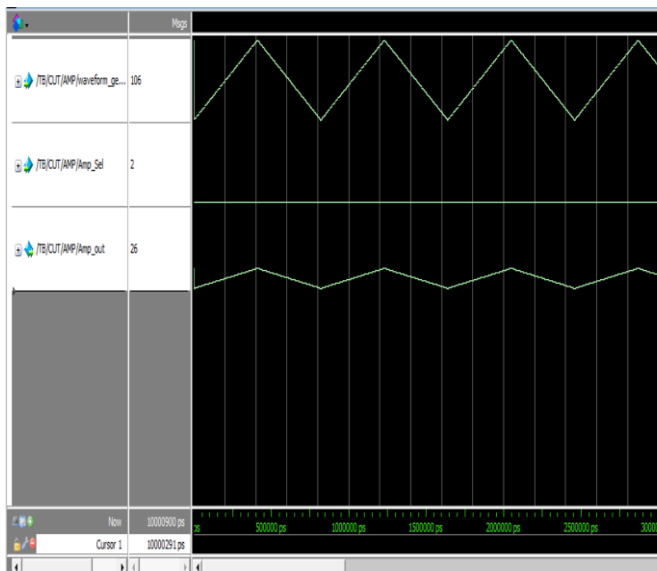


Fig. 14  $\frac{1}{4}$  amplitude triangular

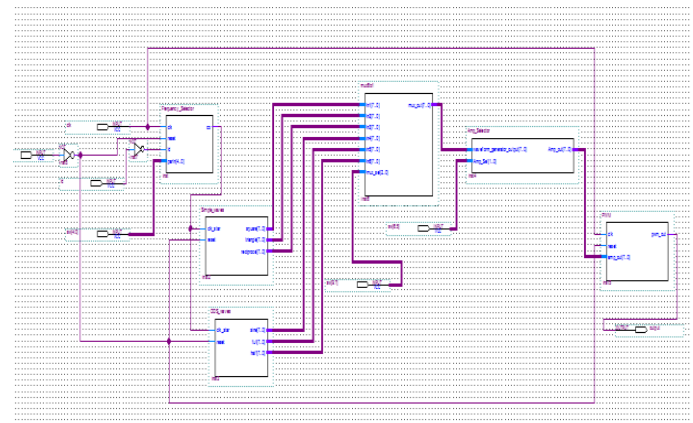


Fig. 16 Schematic diagram of the Function Generator

*B. Demonstrate the Oscilloscope visualization of different waveforms at two distinct amplitude and frequency settings.*

In this part first of all we show waveform of a square wave with amplitude 1x in Fig. 17





Fig. 17 Oscilloscope visualization square 1x

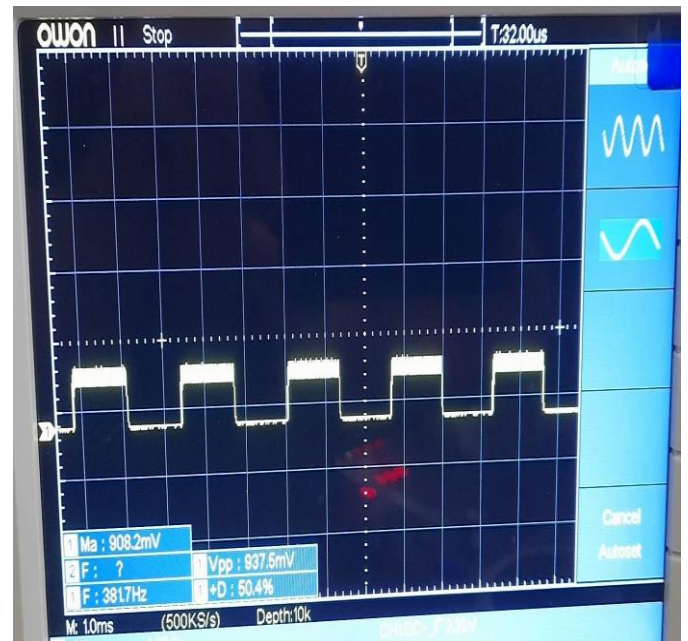


Fig. 19 Oscilloscope visualization square  $\frac{1}{4} \times$

Now in Fig. 18, 19, 20 we show above visualization for different amplitudes.

Fig. 18:  $\frac{1}{2}$

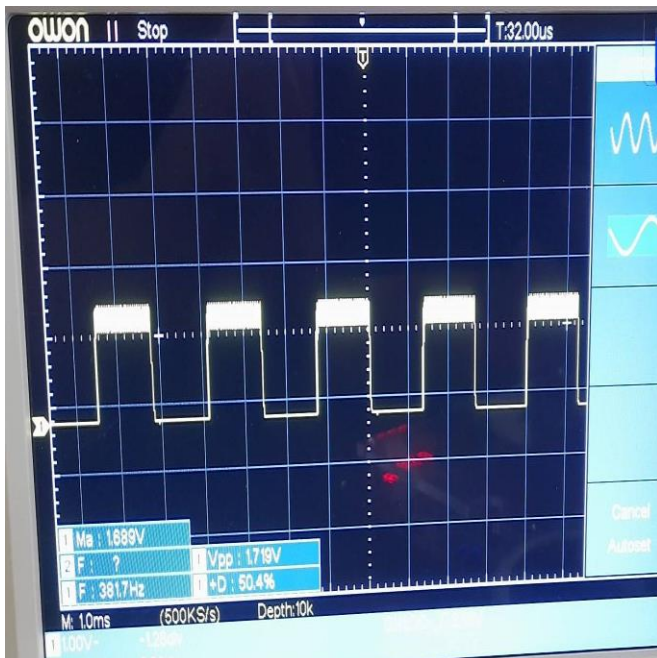


Fig. 18 Oscilloscope visualization square  $\frac{1}{2} \times$

Fig. 19:  $\frac{1}{4}$

Fig. 20:  $\frac{1}{8}$



Fig. 20 Oscilloscope visualization square  $\frac{1}{8} \times$

Now we want to represent different frequencies of visualization of Fig. 17

The figures 21, 22, 23 will be in order of frequency increment.



Fig. 21 Visualization of different frequencies 1

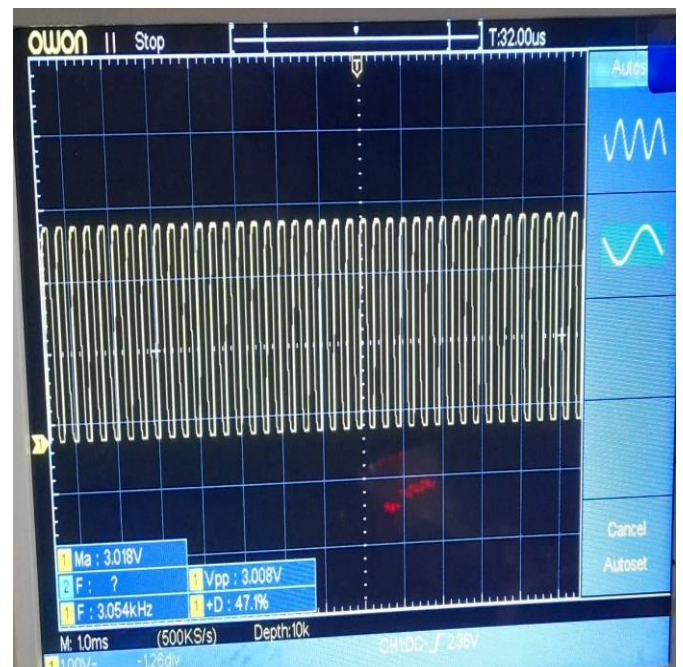


Fig. 23 Visualization of different frequencies 3

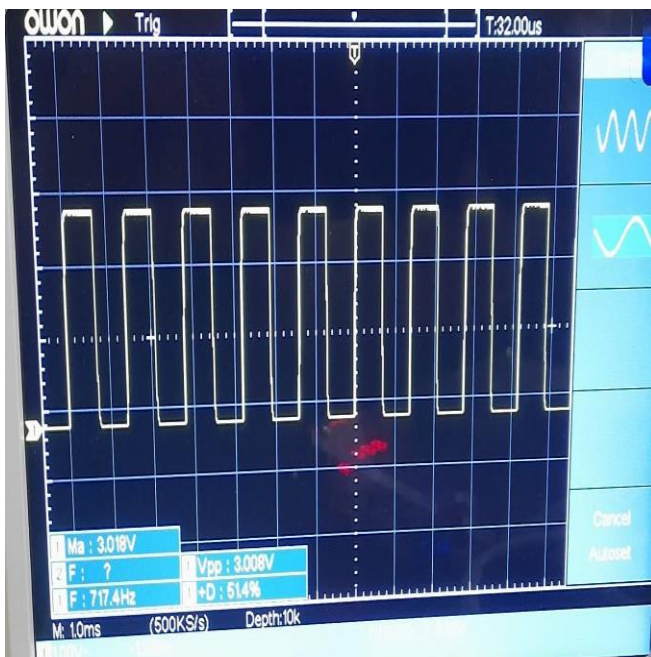


Fig. 22 Visualization of different frequencies 2

Finally, some of the waveforms that was shown in multisim simulation are shown here in below figures using Oscilloscope visualization.

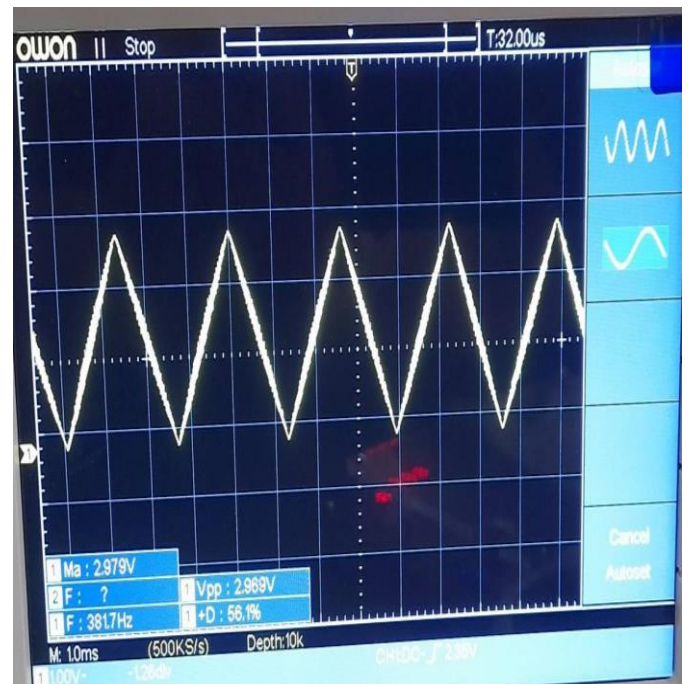


Fig. 24 Triangular



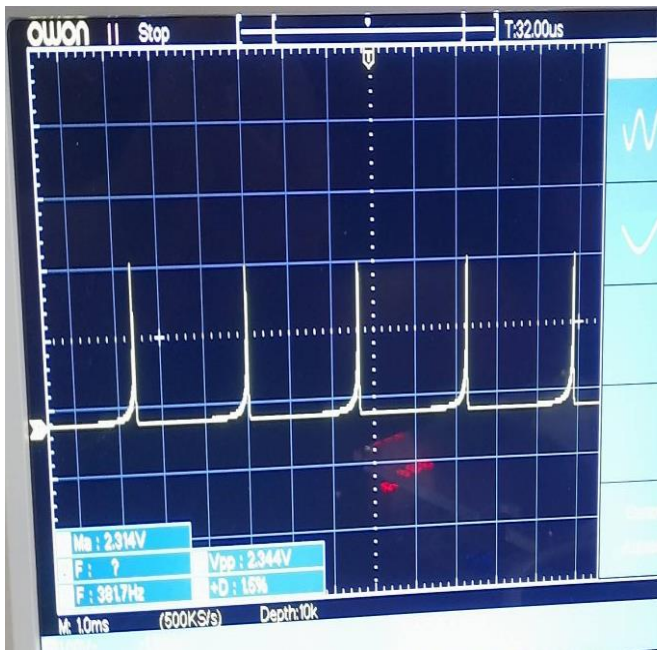


Fig. 25 Reciprocal



Fig. 27 Half sine

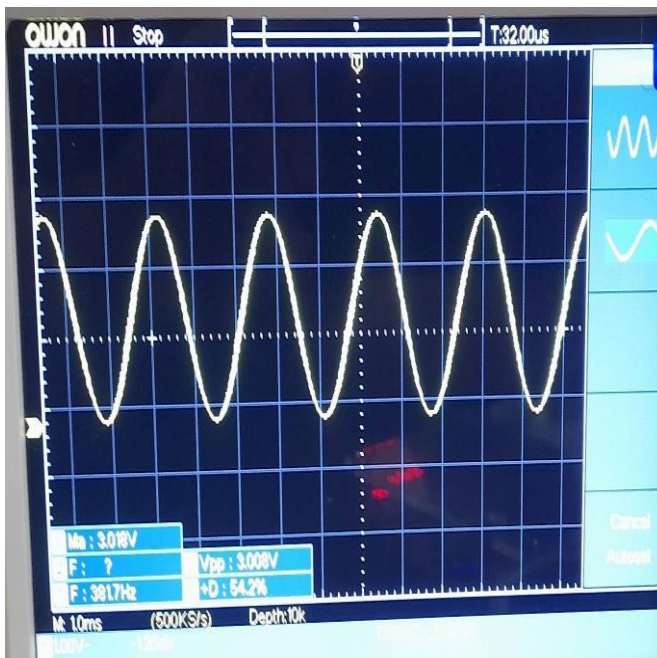


Fig. 26 Sine

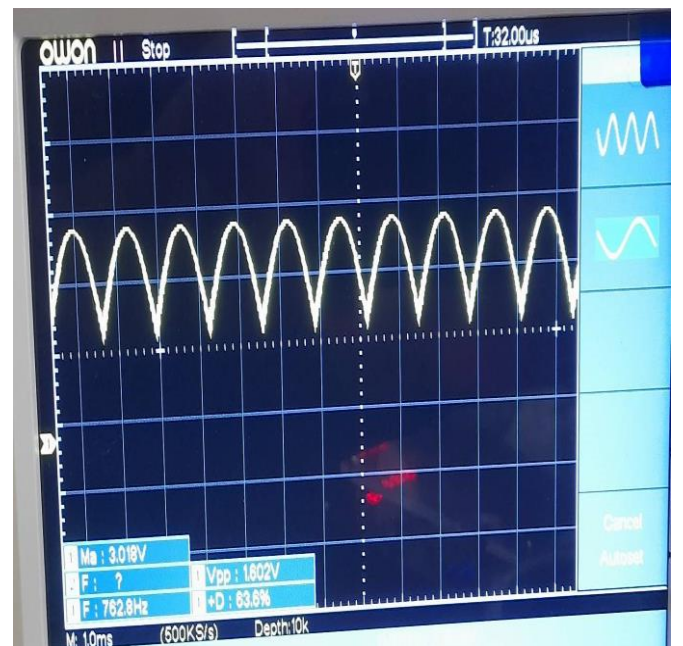


Fig. 28 Full sine