ELECTRONIC CIRCUITS AND LABORATORY Ⅱ Report

A Speaker Driver Circuit with a Low Pass Filter

I. Abstract

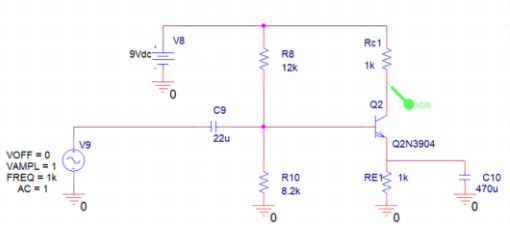
Our experimental goal is to design a filter circuit capable of eliminating 10kHz noise present in the input audio while effectively playing back the input audio. To eliminate the 10kHz noise, we designed a low-pass filter with a pole near 3kHz. The simulation results of our designed circuit in PSPICE were satisfactory. However, during the soldering process, possibly due to poor soldering connections, the circuit failed to output the audio signal.

II. Materials

R1	R2	R3	R4	R5	R6	C1	C2	C3
12k	1k	8.2k	1k	5k	5k	470uF	100nF	10nF

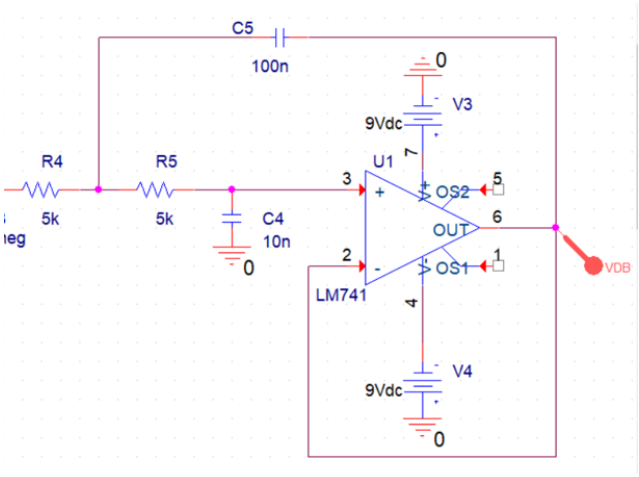
III. Pspice circuit and Simulation

i. Amplifier



The resistance values of R8 and R10 were chosen as 12k and 8.2k, respectively, to ensure that the transistor's base has an appropriate bias voltage and remains in an active state. Both Rc1 and Re1 are 1k, making the CE amplifier in forward active mode and stabilizing the bias operating point through a negative feedback mechanism. The capacitance of C10 is 470μF, which enhances the AC gain and has a certain impact on the frequency characteristics. The gain of the amplifier is going to be adjusted with the potentiometer placed in series with the input voltage.

ii. Salen and Key Low Pass Filter



To achieve the desired cutoff frequency (3kHz), minimize noise at 10kHz and sensitivities to component variations, R4 = R5 = 5.3k ≈ 5kΩ, C5 = 100nF, C4 = 10nF are selected. And the cutoff frequency, fc is given by:

$$f_C = \frac{1}{2\pi * \sqrt{R_1 R_2 C_1 C_2}} = 3\text{kHz}$$

According to the simulation results, a cutoff frequency of 3kHz also meets our requirements and can effectively eliminate the 10kHz noise. This is because the voltage gain decreases relatively slowly between 3kHz and 10kHz. Therefore, selecting 3kHz as the cutoff frequency is the optimal choice.

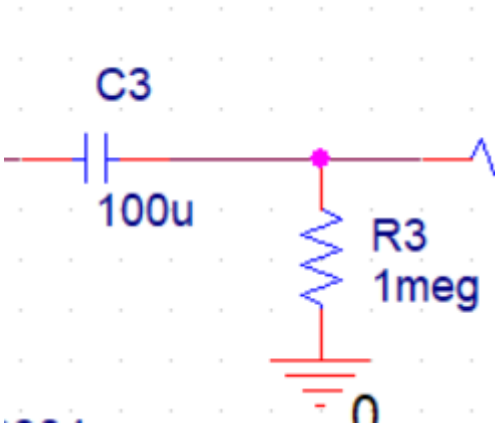
The quality factor Q of the filter (which affects the sharpness of the cutoff) is influenced by the ratio of resistors and capacitors. Quality factor determines the height and width of the peak.

$$Q = \frac{\sqrt{R_1 R_2 C_1 C_2}}{C_2 * (R_1 + R_2)}$$

$$\text{Solving for Q yields; } Q = \frac{1}{2 - \frac{R_3}{R_4}} = \frac{1}{2}$$

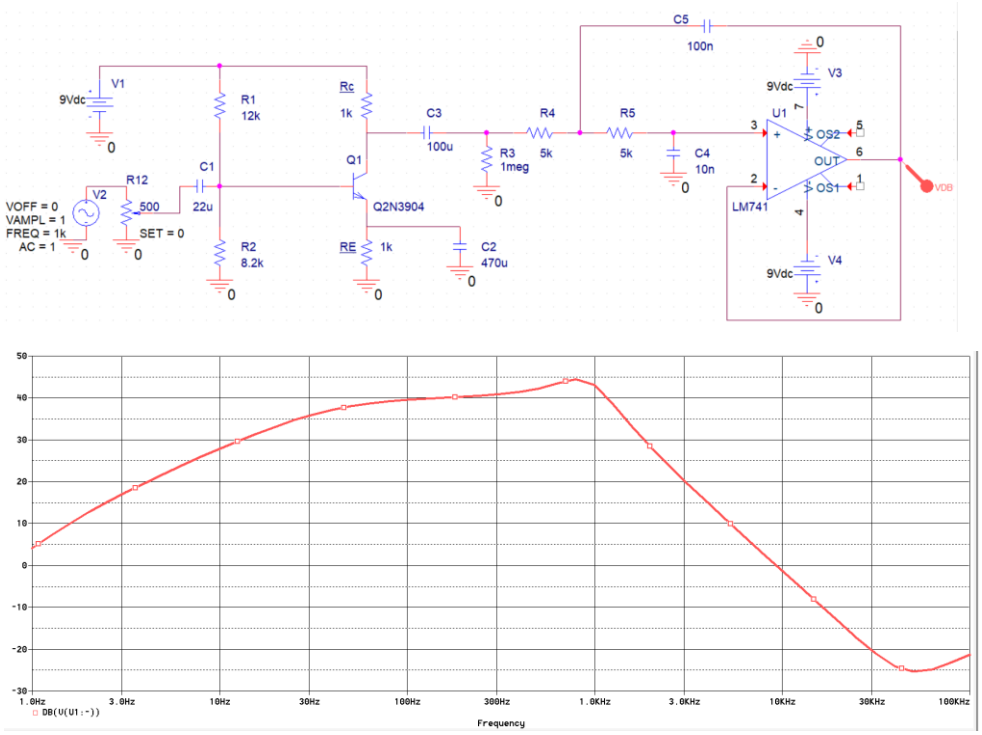
The lower the Q, the greater the width of the peak. The ratio of the capacitors was adjusted to choose the quality Q of the filter and hence, cancel noise at 10kHz.

iii.



The bias circuit is given to block DC offsets from the previous amplifier stage, keeping the Sallen-Key filter centered at 0V for optimal operation. Also allowing only AC signals to pass to the filter, helping in achieving a stable, noise-minimized output across the intended frequency range.

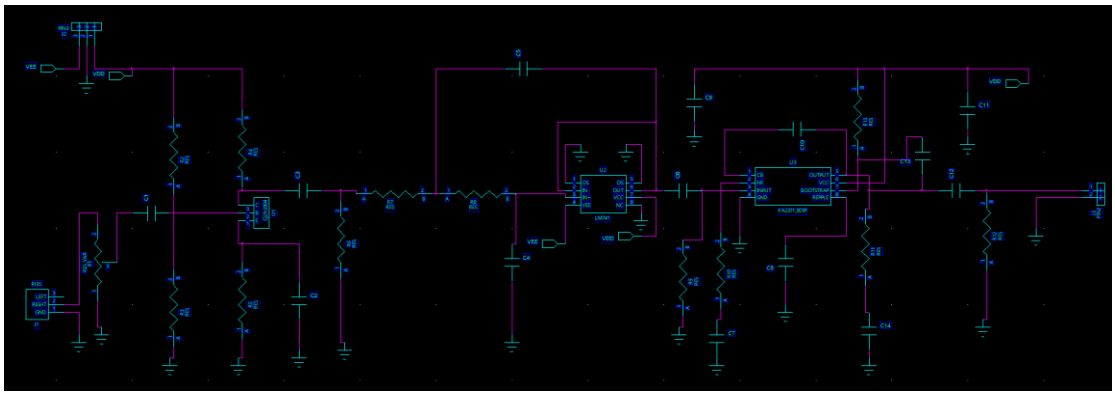
The whole low pass filter and simulation results:

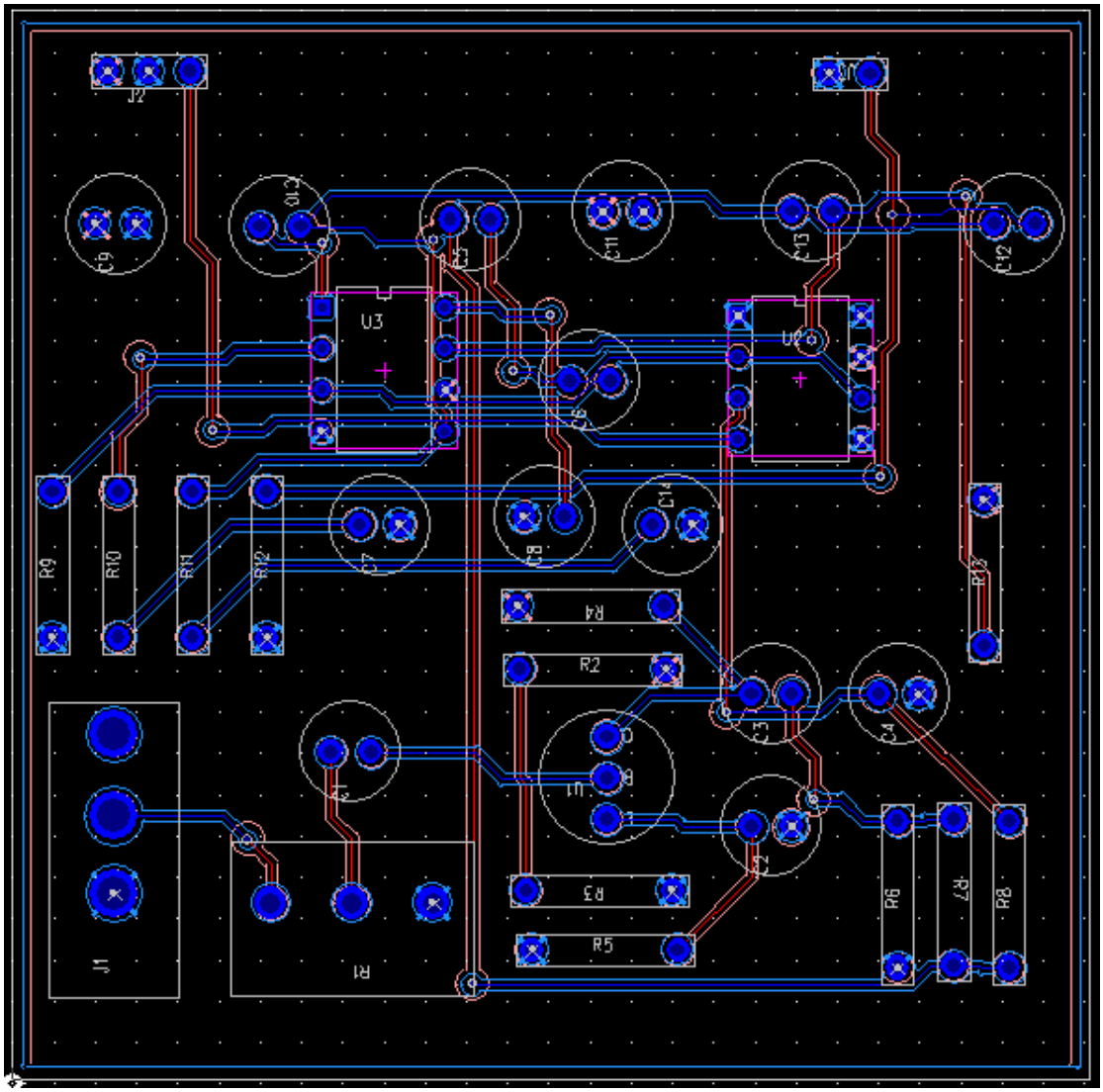


Bode Plot (Gain amplitude Vs Freq) showing minimum noise at 10kHz

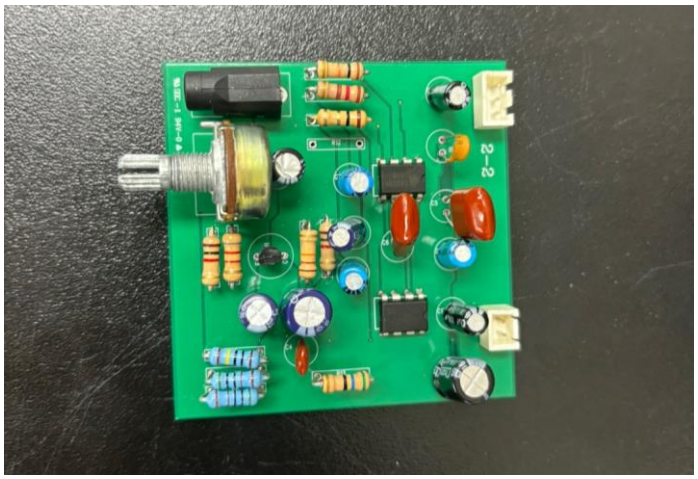
IV. Schematic and Layout

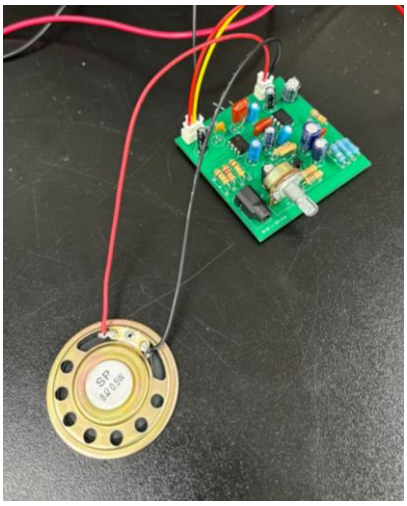
Using the PSPICE circuit as a reference, the schematic and layout can be completed in PADS as shown below.





VI. Soldering and Results Confirmation





After completing the soldering process for all components, we connected VDD to +9V, VEE to -9V, and the speaker to the input sound source to test whether it could play sound normally. However, we found that no sound was produced when input was applied.

After troubleshooting the circuit, we identified two issues: one of the resistors in the BJT collector was shorted during soldering, and the BJT was placed incorrectly due to a layout design error.

VII. Conclusion

We designed a low-pass filter based on the concepts learned in this class to eliminate 10 kHz noise. The simulation results met our expectations; however, the final experimental results did not meet the required specifications. This indicates the need to improve the layout design and soldering process.

When designing the layout, we need to consider additional factors, such as minimizing circuit paths to reduce interference and losses, and ensuring that components in different sections have minimal mutual influence. During the soldering process, to prevent short and open circuits, each component must be soldered with precision, using an appropriate amount of solder.

Although the experiment did not yield successful results, this hands-on experience provided us with a deeper understanding of circuit design and PCB manufacturing processes. It was also our first attempt at PCB soldering, which we believe will be highly valuable for our future learning and practical applications.