CS3120 Introduction of Integrated Circuit Design

Chapter 2 Exercise

[2.1] Suppose that V_{DD} = 5 V and V_{Tn} = 0.7 V. Find the output voltage V_{out} of the nFET in Figure P2.1 for the following input voltage values: (a) V_{in} = 2 V; (b) V_{in} = 4.5 V; (c) V_{in} = 3.5 V; (d) V_{in} = 0.7 V.

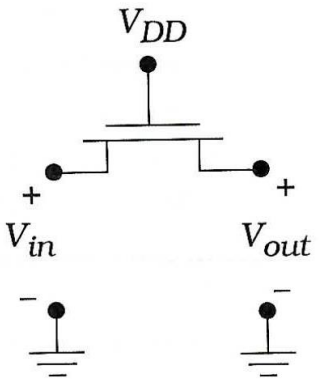

Figure P2.1

[2.2] Consider the two-FET chain in Figure P2.2. The power supply is set to a value of V_{DD} = 3.3 V and the nFET threshold voltage is V_{Tn} = 0.55 V. Find the output voltage V_{out} at the right side of the chain for the following values of V_{in}: (a) V_{in} = 2.9 V; (b) V_{in} = 3.0 V; (c) V_{in} = 1.4 V; (d) V_{in} = 3.1V.

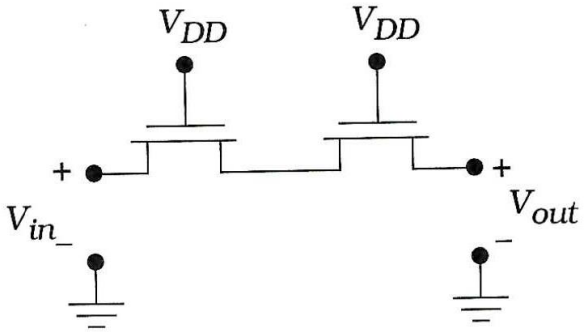

Figure P2.2

[2.3] The output of an nFET is used to drive the gate of another nFET as shown in Figure P2.3. Assume that V_{DD} = 3.3 V and V_{Tn} = 0.60 V. Find the output voltage V_{out} when the input voltages are at the following values: (a) V_a = 3.3 V and V_b = 3.3 V; (b) V_a = 0.5 V and V_b = 3.0 V; (c) V_a = 2.0 V and V_b = 2.5 V; (d) V_a = 3.3 V and V_b = 1.8 V.

[2.4] Design a NAND3 gate using an 8:1 MUX.

[2.5] Design a NOR3 gate using an 8:1 MUX as a basis.

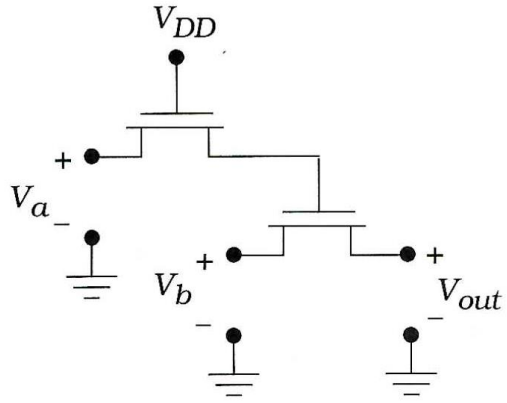

Figure P2.3

[2.6] Consider the 2-input XOR function $a \oplus b$.

(a) Design an XOR gate using a 4:1 MUX.

(b) Modify the circuit in (a) to produce a 2-input XNOR.

(c) A full adder accepts inputs a, b, and c and calculates the sum bit

$$s = a \oplus b \oplus c \tag{2.85}$$

Use your MUX-based gates to design a circuit with this output.

[2.7] Design a CMOS logic gate for the function

$$f = \overline{a \cdot b + a \cdot c + b \cdot d} \tag{2.86}$$

using the smallest number of transistors.

[2.8] Design a CMOS circuit for the OAI expression

$$h = \overline{(a+b) \cdot (a+c) \cdot (b+d)} \tag{2.87}$$

Use the smallest number of transistors in your design.

[2.9] Construct the CMOS logic gate for the function

$$g = \overline{x \cdot (y+z) + y} \tag{2.88}$$

Start with the minimum-transistor nFET network, and then apply bubble pushing to find the pFET wiring.

[2.10] Design a CMOS logic gate circuit that implements

$$F = \overline{a + b \cdot c + a \cdot b \cdot c} \tag{2.89}$$

using series-parallel logic. The objective is to minimize the transistor count.

[2.11] Consider the logic described by the diagram in Figure P2.4. A single, complex logic CMOS gate is to be designed for F.

(a) Construct the nFET array using the logic diagram.

(b) Apply bubble pushing to obtain the pFET logic. Then construct the pFET array using the rules.

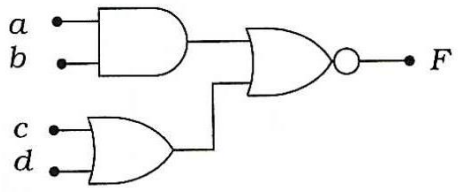

Figure P2.4

[2.12] An AOAI logic gate is described by the schematic in Figure P2.5.

(a) Construct the nFET array using the logic diagram.

(b) Apply bubble pushing to obtain the pFET logic. Use the diagram to construct the pFET array using the pFET rules.

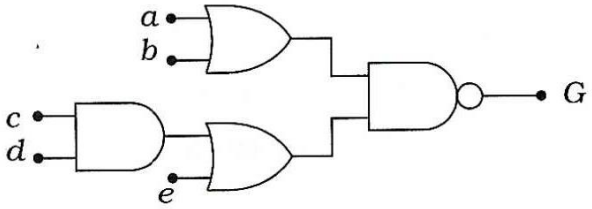

Figure P2.5

[2.13] A pFET logic array is shown in Figure P2.6. Construct the logic diagram using the pFET logic equations. Then construct the nFET circuit.

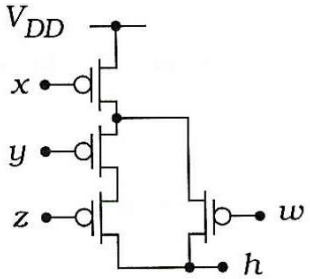

Figure P2.6

[2.14] Design the 4:1 multiplexor circuit that implements the function in equation (2.80) by using TG switches.

[2.15] Use an AOI22 gate to design a 2:1 MUX. Inverters are permitted in your design.

[2.16] Design a 4:1 MUX using three 2:1 TG multiplexors.

[2.17] A CPU clock ϕ has a frequency 2.1 GHz. What is the period T?

[2.18] Suppose that the hold time for a TG is given as t_{hold} = 120 milliseconds (ms). What is the smallest clock frequency that can be used to clock the data flow using a scheme such as that shown in Figure 2.67?