CS3120

Introduction of Integrated Circuit Design

Chapter 11 / 13
Sequential Logic Design and Memory

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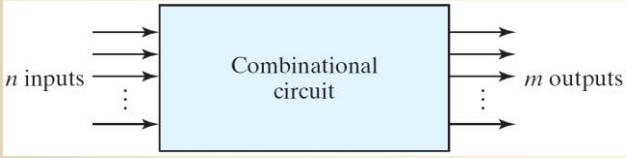
Outline

- Latches
- Flip-Flop
- Static RAM (SRAM) Cells
- Static RAM (SRAM) Arrays
- Memory Architecture

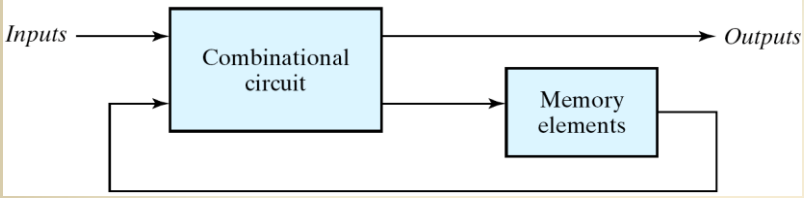
Combinational Circuits

- Combinational circuits
  - Contains no memory elements
  - The outputs depends on the inputs



Sequential Circuits

- Sequential circuits



- A feedback path
- The state of the sequential circuit
- (inputs, current state) ⇒ (outputs, next state)
- Synchronous: the transition happens at discrete instants of time
- Asynchronous: at any instant of time

Synchronous Clocking

Synchronous clocking II

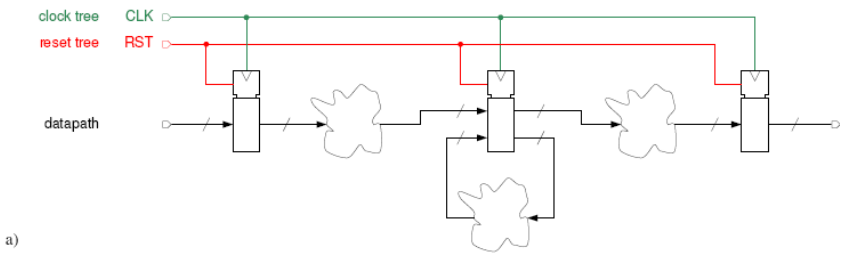


Figure: Toy example of a synchronously clocked circuit.

Latches

- A latch is a device that can receive and hold an input bit
- A simple D-latch forms the basis for memory designs
- A latch is transparent in that a change in D is seen at the output Q and Q'

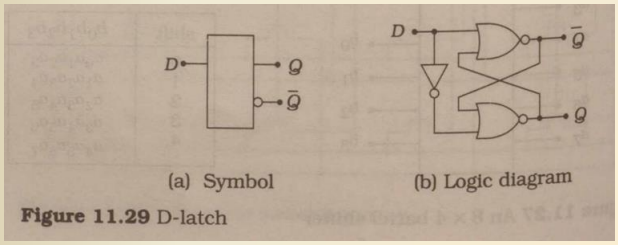


Figure 11.29 D-latch

Latches

- CMOS circuit for a D-latch

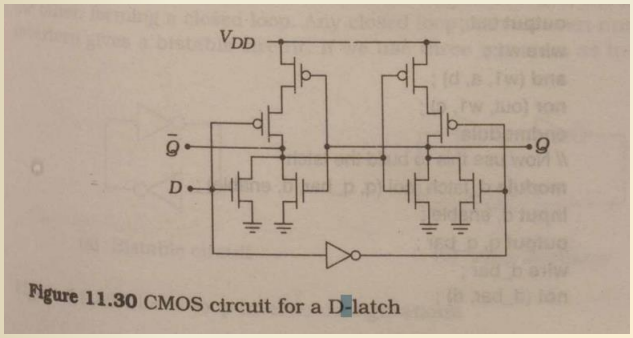
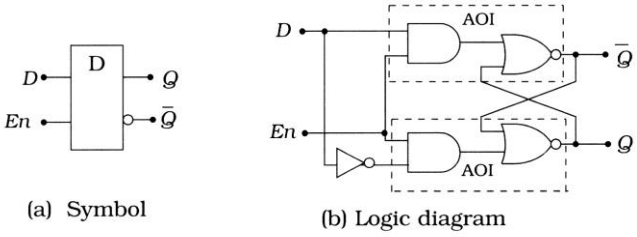


Figure 11.30 CMOS circuit for a D-latch

Latches

- Gated D-latch with Enable control



(a) Symbol (b) Logic diagram

Figure 11.31 Gated D-latch with *Enable* control

Latches

- AOI CMOS gate for D-latch with Enable

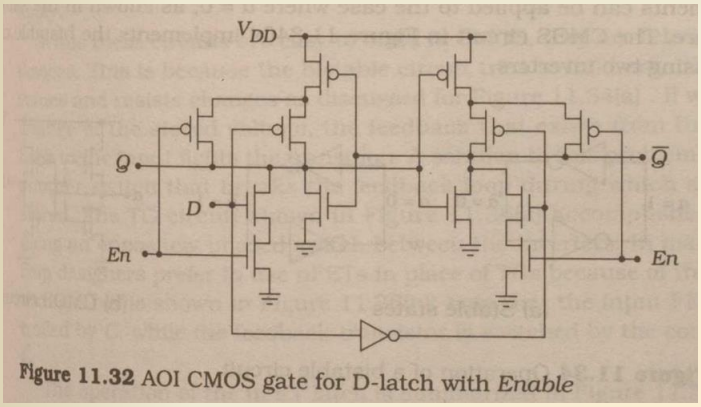
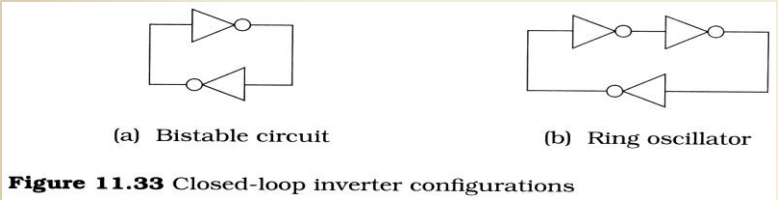


Figure 11.32 AOI CMOS gate for D-latch with *Enable*

CMOS VLSI Latch

- Many static D-latches CMOS VLSI are constructed from inverters and TGs and pass FETs
- These circuits are relatively slow because the bi-stable circuit tries to hold onto the stored values and resists changes

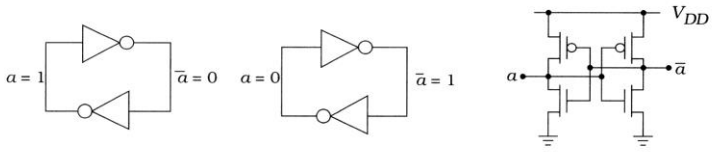


(a) Bistable circuit (b) Ring oscillator

Figure 11.33 Closed-loop inverter configurations

CMOS VLSI Latch

- Operation of a bi-stable circuit

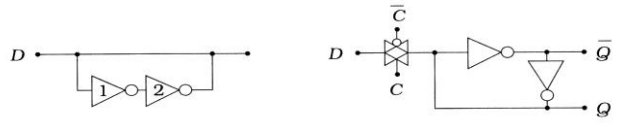


(a) Stable states (b) CMOS circuit

Figure 11.34 Operation of a bistable circuit

CMOS VLSI Latch

- To create a D-latch, we must provide an entry node for the input bit
  - Receiver circuit: value of D is held by the bi-stable circuit formed by the inverter pair
  - Inverter 1 can use relatively large FETs, but Inverter 2 is purposely made weaker by using small transistors
  - Adding a transmission gate at the input gives us the ability to control the loading



(a) Receiver circuit (b) Controlled loading

Figure 11.35 Adding an input node to the bistable circuit

CMOS VLSI Latch

- These circuits are relatively slow
  - The bi-stable circuit tries to hold onto the stored values and resists changes
  - If we force a change of the stored voltage, the feedback that exists from the output back to the input fights the transition
- Solution
  - Add another switch that breaks the feedback loop

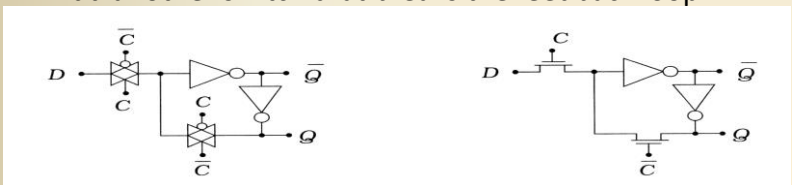


Figure 11.36 D-latch using oppositely phased switches

CMOS VLSI Latch

- Operation of the D-latch

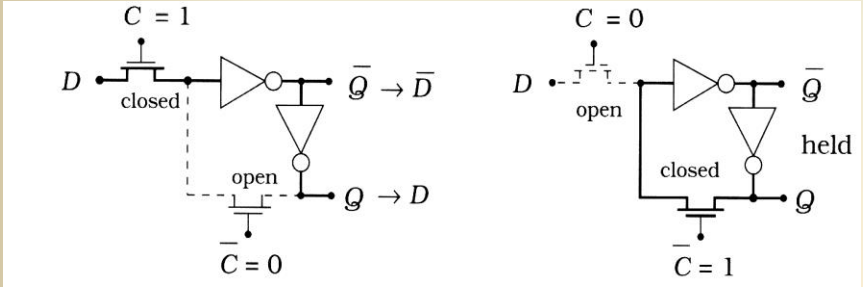
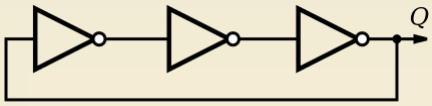


Figure 11.37 Operation of the D-latch

Ring Oscillator

- A **ring oscillator** is a device composed of an odd number of NOT gates in a ring. Simple 3-inverter ring oscillator whose output frequency is 1/(6×inverter delay).



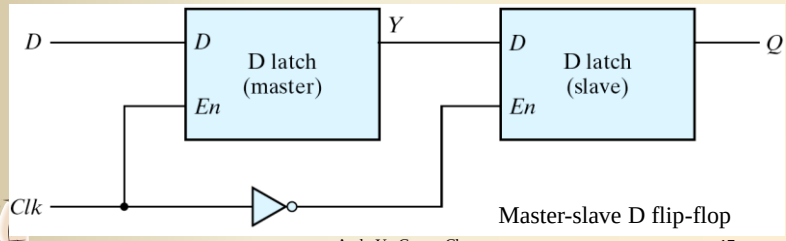
- Applications:
  - Jitter of ring oscillators is commonly used in hardware random number generators
  - Ring oscillators can also be used to measure the effects of voltage and temperature on a chip
  - Measure the effects of manufacturing process variations

D Flip-Flop

- A flip-flop differs from a latch in that it is non-transparent
- The basic DFF design is a master-slave configuration
- The master-slave circuit acts as a positive edge-triggered device since the value of D during the positive clock edge defines the value of the bit

D Flip-Flop

- Edge-triggered flip-flop
  - The state changes during a clock-pulse transition
- Master-slave *D* flip-flop
  - Two separate latches
  - A master latch (positive-level triggered)
  - A slave latch (negative-level triggered)
    - Output change can be triggered only by and during the transition of the clock from 1 to 0



Master-slave D flip-flop

D Flip-Flop

- Master-slave DFF

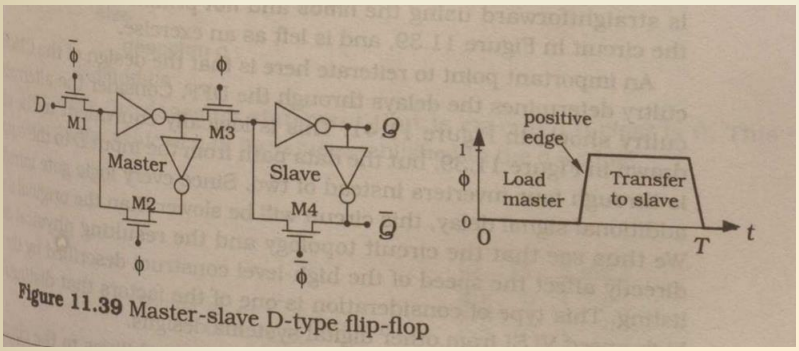
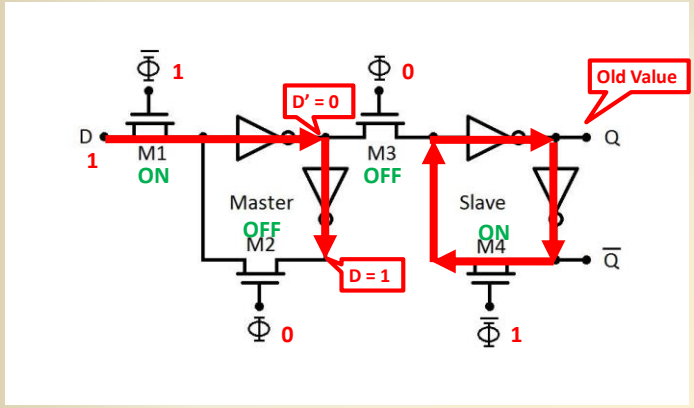
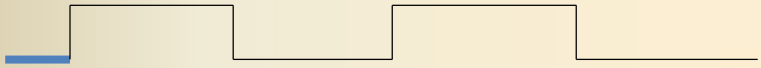


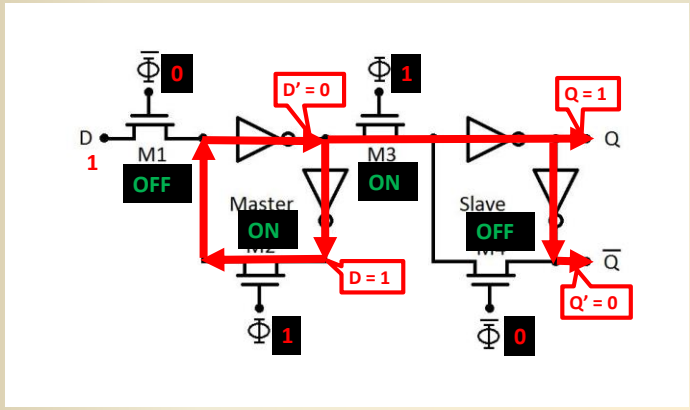
Figure 11.39 Master-slave D-type flip-flop

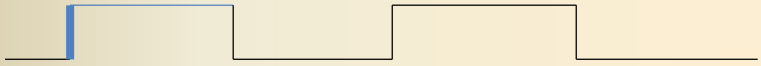
Case: D = 1, Ø = 0



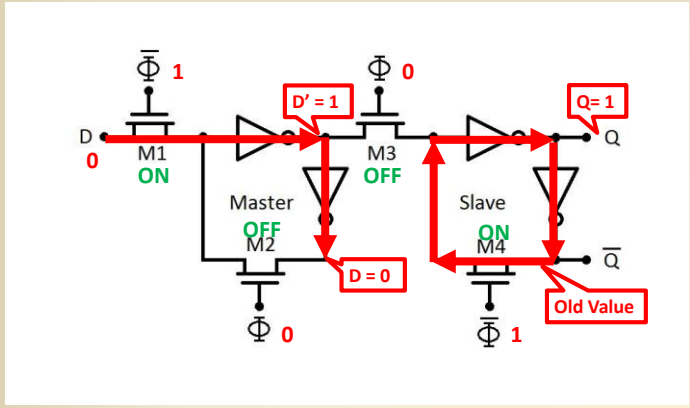


When Ø = 0 → Ø = 1





Case: D = 0, Ø = 0



DFF circuits with assert-low clear

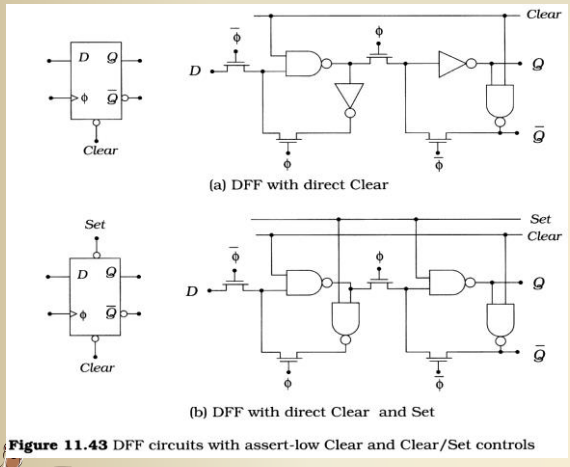


Figure 11.43 DFF circuits with assert-low Clear and Clear/Set controls

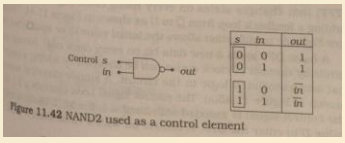
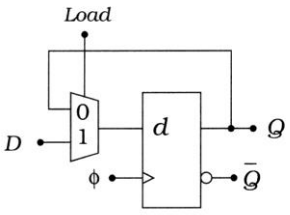
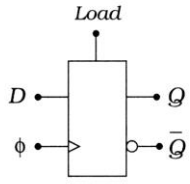


Figure 11.42 NAND2 used as a control element

DFF circuits with Load control



(a) Wiring diagram

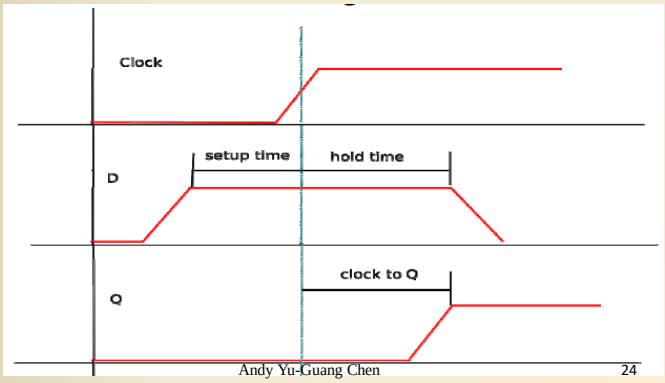


(b) Symbol

Figure 11.45 D-type flip-flop with *Load* control

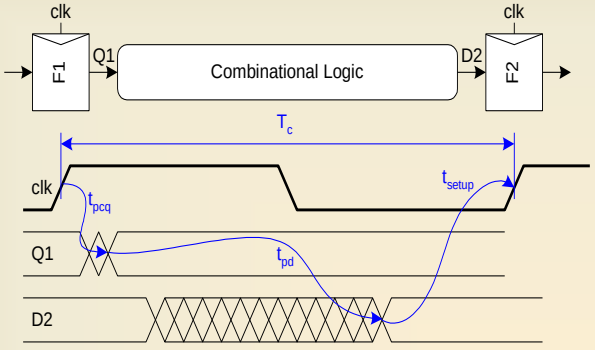
Characterizing Flip Flop Timing

- Setup Time: t_{su}–Time D must remain stable before the clock changes
- Hold Time: t_h–Time D must remain stable after the clock changes
- Clock to Q Time: t_{c2q}–Time from the clock edge until the correct value appears at Q



Max-Delay: Flip-Flops

$$t_{pd} \le T_c - \underbrace{\left(t_{setup} + t_{pcq}\right)}_{\text{sequencing overhead}}$$



Memory

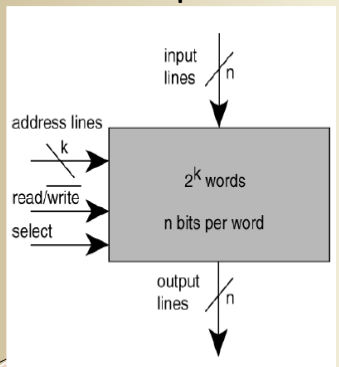
- **The Memory System**
  - **You Can't Avoid It,**
  - **You Can't Ignore It,**
  - **You Can't Fake It**
- The memory system is "the bottleneck."

13.1 Static RAM

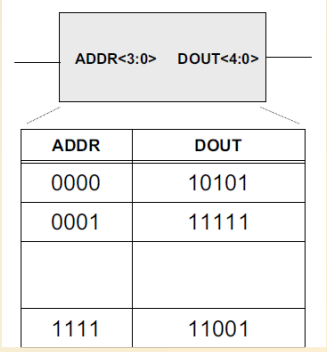
- RAM: read/write vs ROM
- A static RAM cell can hold the stored data bit as long as the power is applied to the circuit.
- SRAM (vs DRAM)
  - Expensive, faster, less power.
  - High bandwidth or low power.
  - RAM, cache, registers, FPGAs, hard disk buffers, router buffers,
- Three states:
  - Hold: the value of bit is stored
  - Write: a logic 0 or 1 is fed into
  - Read: the value of stored bit is transmitted to outside

Memory

- All memory structures have an address bus and a data bus. For each address there is a corresponding data output



16 possible address values with 5 bit output (16 x 5 ROM)



ADDR	DOUT
0000	10101
0001	11111
1111	11001

General SRAM cell

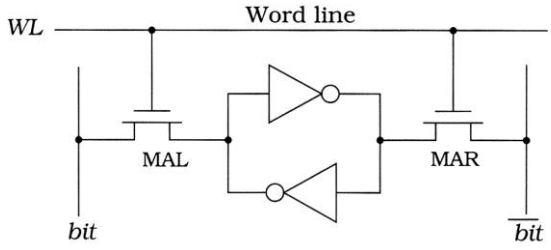


Figure 13.1 General SRAM cell

General SRAM cell

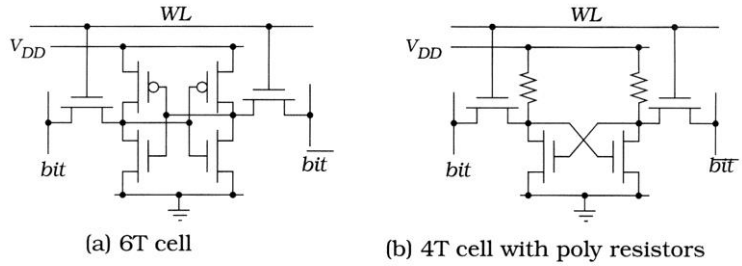


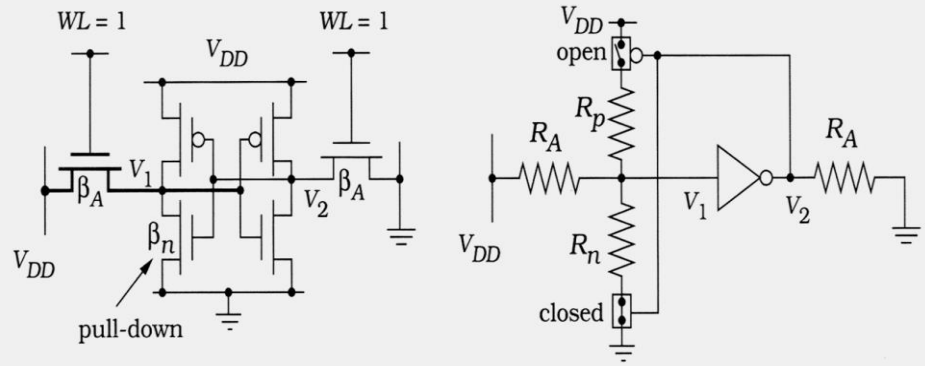
Figure 13.2 CMOS SRAM circuits

- Create resistors by undoped poly.
- Require additional polysilicon layer

SRAM Circuits

- Circuit level design issues :
  - Choose the transistor aspect rations so that the cell can hold a state while allowing it to be changed during a write operation without excessive delay.
- β_A / β_n= is about 2 for the 6T cell. The reason is as follows.
  - The worst case is V_1=0 and V_2=1
  - $\beta_A > \beta_n \Rightarrow R_A < R_n$
  - The access of FET is more effective in increasing V_1 to the level needed to switch the stored state.

SRAM Circuits



(a) Write 1 operation (b) Resistor model

Figure 13.5 Writing to an SRAM

SRAM cell layout

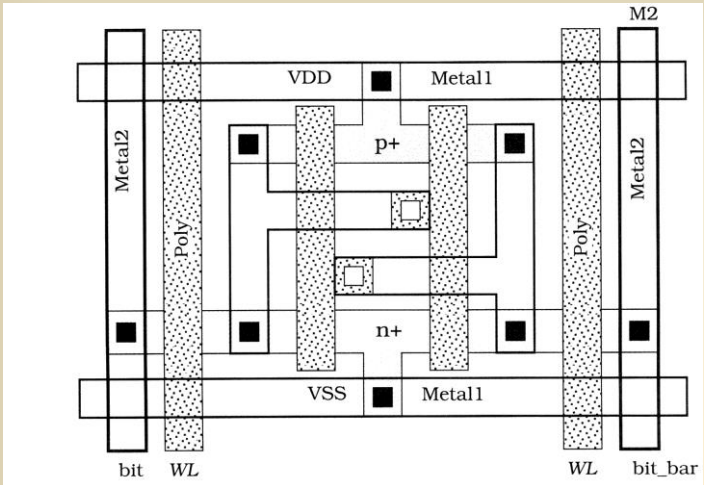


Figure 13.6 Example of a basic SRAM cell layout

Multiple-port SRAM

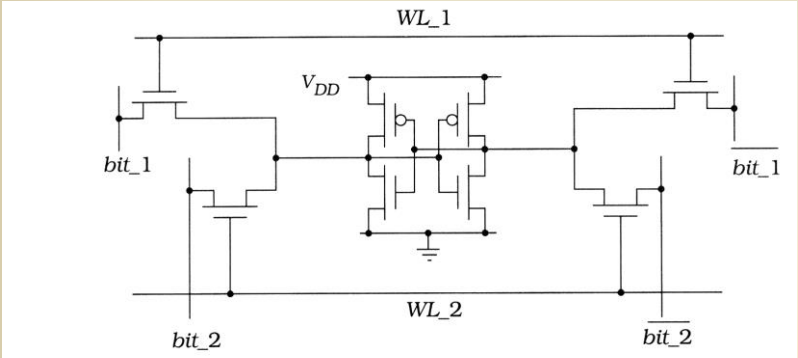


Figure 13.7 A 2-port CMOS SRAM cell

Multiple-port SRAM

- Cells provide cell access to more than one pair of bit/bit-bar lines.
- At the system level, a method for tracking the contents of the memory and priority access scheme must be developed.
- Useful for video memory and register files.

13.2 SRAM arrays

- Static RAM arrays are created by replicating the basic storage cell and adding the necessary peripheral circuitry.
- Objective: highest storage density, short access times.

13.2 SRAM arrays

- A 128K ×8 SRAM holds 128K 8 bit words of a total 1Mb of total storage; m=17

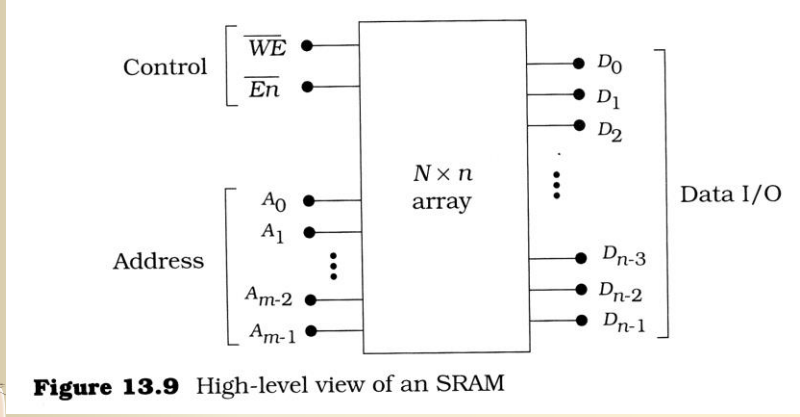


Figure 13.9 High-level view of an SRAM

Central SRAM Block Architecture

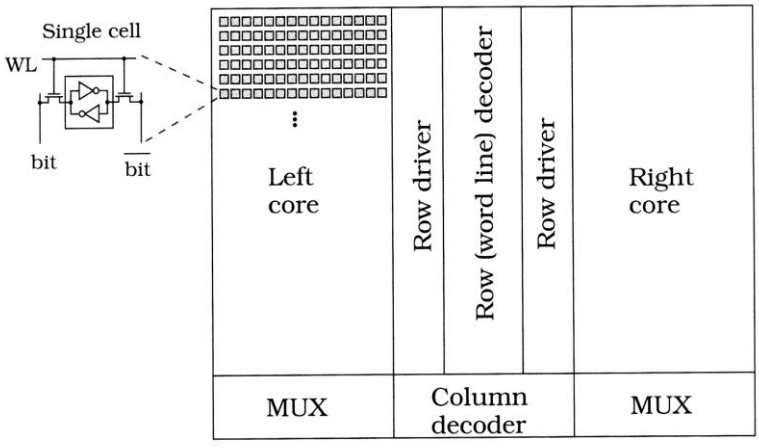
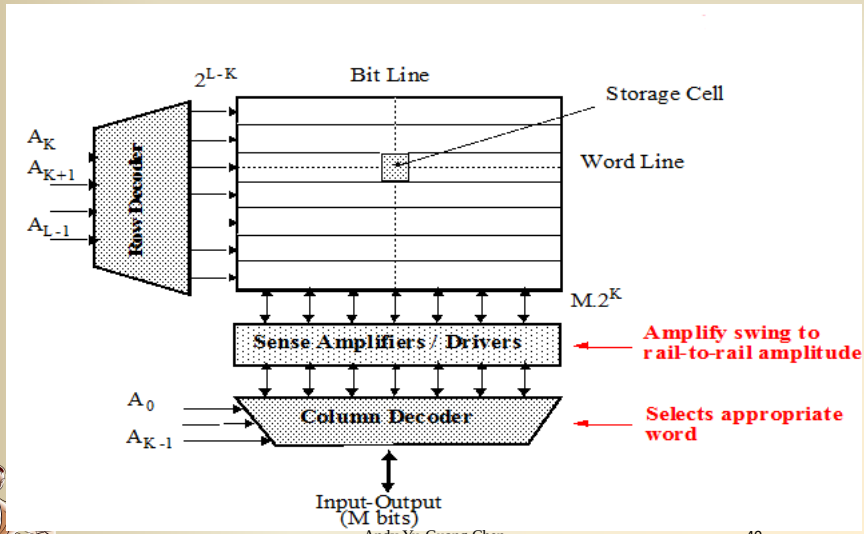


Figure 13.10 Central SRAM block architecture

Memory Architecture

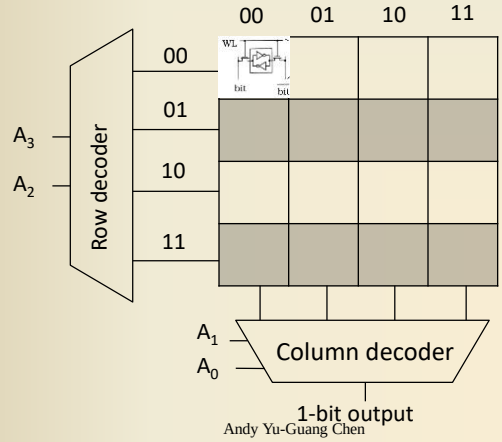
- Word lines are in horizontal direction while bit and bit bar lines are vertically.
- The address word specifies a particular row ➔ the access transistors (could be 8) are turned on ➔ Permitting the read/write operation to take place
- The row decoder outputs are fed into row drivers
- Row drivers are needed because of large load.

Memory Architecture



Memory Architecture

- Example : A 16×1 SRAM holds 16 1-bit words of a total 16-bit storage; address = $A_3A_2A_1A_0$



Memory Architecture

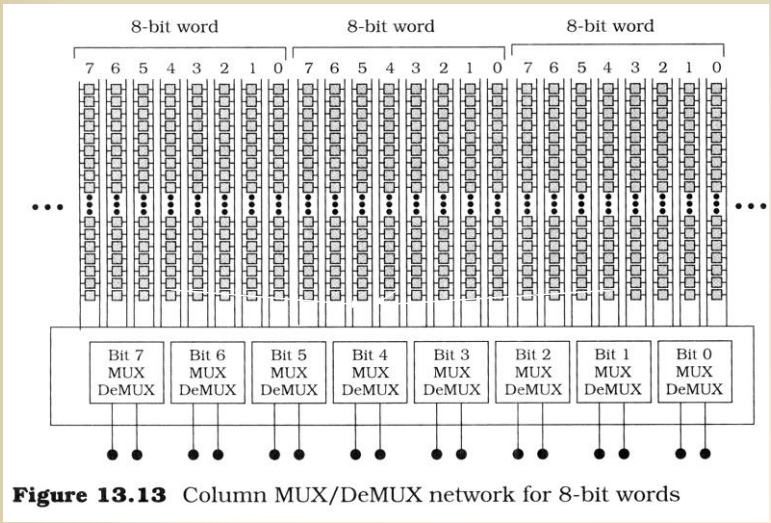


Figure 13.13 Column MUX/DeMUX network for 8-bit words

Column Mux/DeMux network

- Each Mux/Demux block is connected to appropriate data line of each word.
- Bit 4 of each words are connected to the Bit 4 Mux.
- For a write operation, the DeMux mode is used to steered a data word into the right column.

Memory Architecture

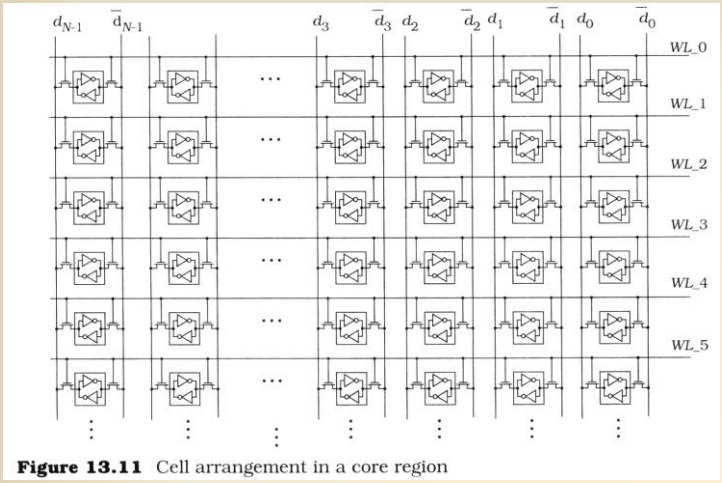


Figure 13.11 Cell arrangement in a core region

Memory Architecture

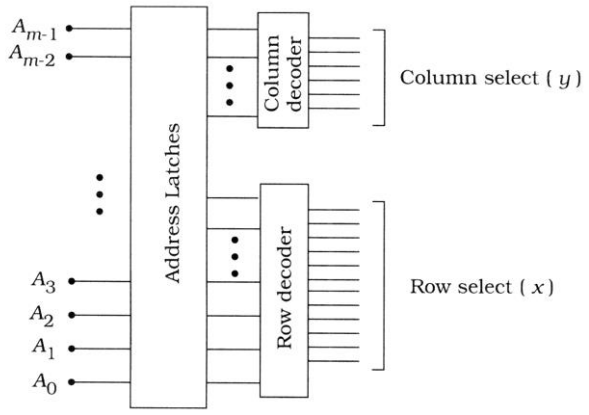


Figure 13.15 Basic addressing scheme

Row and Column driver

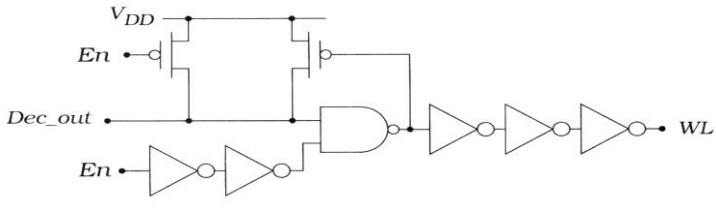


Figure 13.12 Row driver circuit

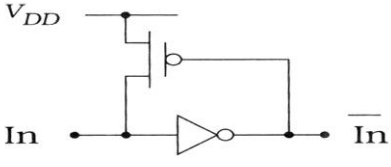


Figure 13.14 Logic 1 column driver

Memory Architecture

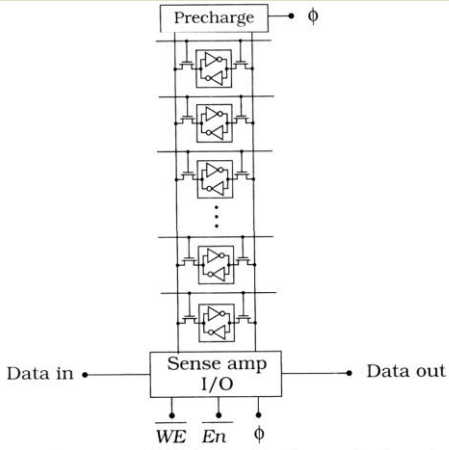


Figure 13.17 Precharge and I/O circuits for a single column

Memory Architecture

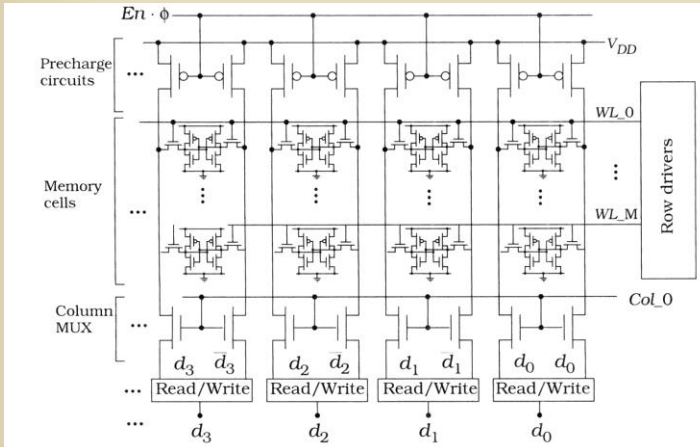


Figure 13.18 Expanded view of column circuitry

Precharge and I/O circuits

- Dynamic circuits to provide faster read operations.
- Phi =0, precharge bit and bit_bar to high.
- Phi=1, evaluation takes place. The bit and bit-bar lines fed to a differential “sense” amplifier.

Differential Amplifier

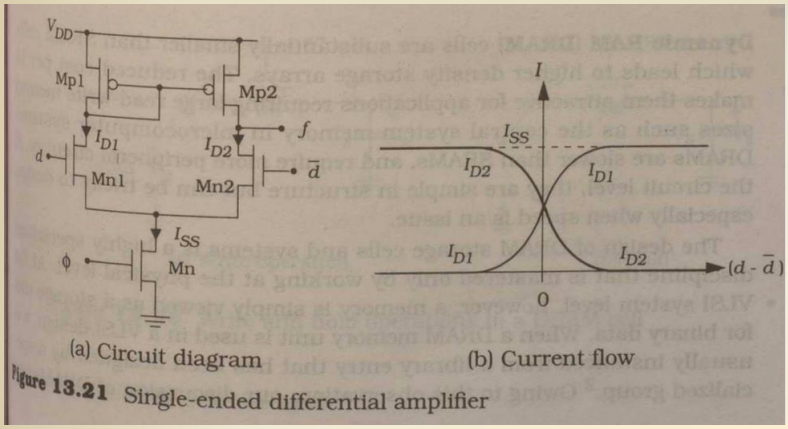


Figure 13.21 Single-ended differential amplifier

Differential Amplifier

- The pFETs Mp1 and Mp2 are used as active load devices and act like non-linear pull-up resistors
- Mn1 and Mn2 that accept complementary inputs
- Iss= Id1+Id2.
- When the voltage associated with d is large, Id1 increases. The total currents are limited by the current through the clock controlled nFET Mn.

Differential Amplifier

- The difference in currents is translated into a low or high output voltage. At the circuit level, the design problem revolves around selecting the aspect ratios of the transistors.

Q&A

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