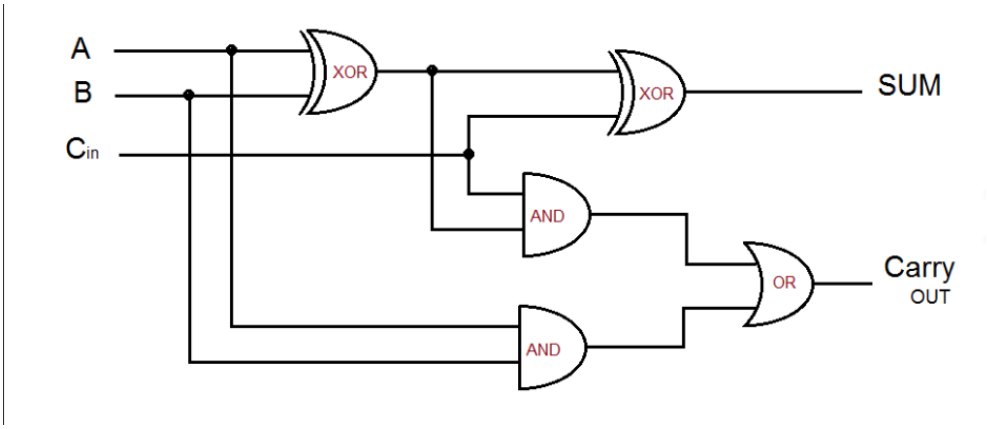
1. The circuit diagram of design and explaining design

下圖為 Full adder 的 circuit diagram



分別實作出 XOR2 、 AND2 、 OR2 三個 logic gate

```
*****************
*** Inverter ***
*****************
.subckt INV in inv_out
mp1 inv_out in vdd vdd P_18 w=0.72u l=0.18u
mn1 inv_out in gnd gnd N_18 w=0.36u l=0.18u
.ends
```

```
***************
*** XOR2 ***
***************
.subckt XOR2 A B Y vdd vss

Xinv1 A A_INV INV
Xinv2 B B_INV INV

mp1 out1  A     vdd  vdd P_18 w=0.72u l=0.18u
mp3 out1  B     vdd  vdd P_18 w=0.72u l=0.18u
mp2 Y     A_INV out1 vdd P_18 w=0.72u l=0.18u
mp4 Y     B_INV out1 vdd P_18 w=0.72u l=0.18u

mn1 out3  A     vss  gnd N_18 w=0.36u l=0.18u
mn2 out4  A_INV vss  gnd N_18 w=0.36u l=0.18u
mn3 Y     B     out3 gnd N_18 w=0.36u l=0.18u
mn4 Y     B_INV out4 gnd N_18 w=0.36u l=0.18u

.ends
```

```
************
*** NOR2 ***
************
.subckt NOR2 x y NOR vdd vss
** Your code **
mpx1 out x vdd vdd P_18 w=0.72u l=0.18u
mpy1 NOR y out vdd P_18 w=0.72u l=0.18u
mnx1 NOR x vss gnd N_18 w=0.36u l=0.18u
mny1 NOR y vss gnd N_18 w=0.36u l=0.18u
.ends
```

```
***********
*** OR2 ***
***********
.subckt OR2 in2 in3 OR vdd vss
** Your code **
Xnor1 in2 in3 out_nor vdd vss NOR2
Xinv1 out_nor OR      INV
.ends
```

```
*************
*** NAND2 ***
*************
.subckt NAND2 x y NAND vdd vss
** Your code **
mpx2 NAND x vdd  vdd P_18 w=0.72u l=0.18u
mpy2 NAND y vdd  vdd P_18 w=0.72u l=0.18u
mnx2 out1 x vss  gnd N_18 w=0.36u l=0.18u
mny2 NAND y out1 gnd N_18 w=0.36u l=0.18u
.ends
```

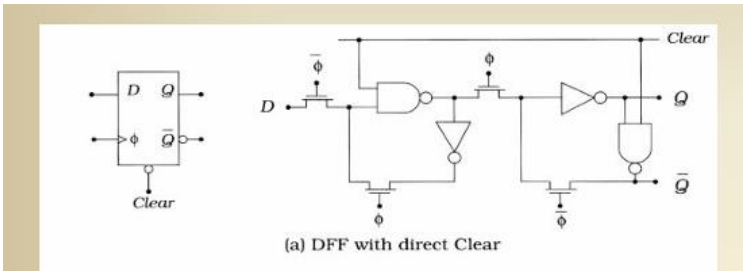
```
************
*** AND2 ***
************
.subckt AND2 in4 in5 AND vdd vss
** Your code **
Xnand1 in4  in5 out_nand vdd vss NAND2
Xinv2  out_nand AND      INV
.ends
```

實作出所有需要的 logic gate 之後，拼湊出 Full adder

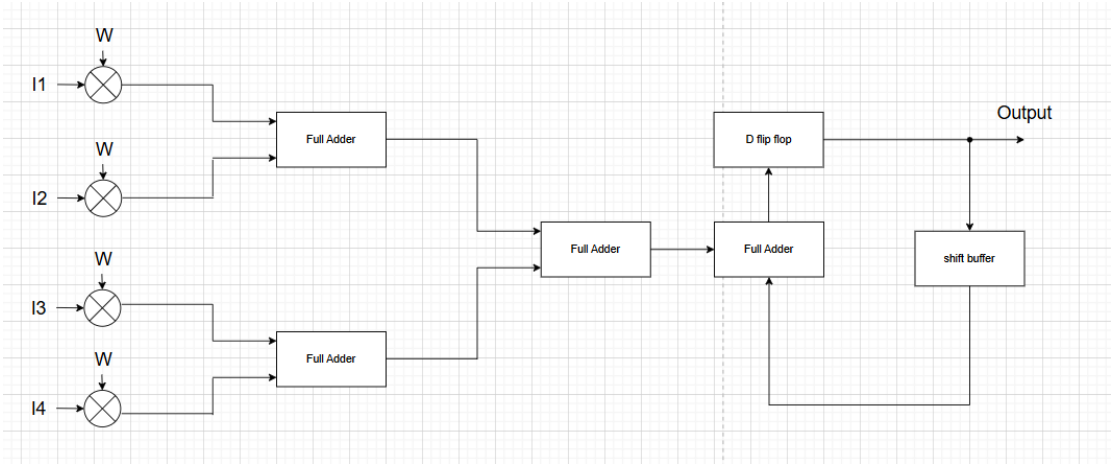
```
**********************
*** full adder ***
**********************
.subckt FADDER a b cin s cout
Xxor0 a    b    net0 vdd gnd XOR2
Xxor1 net0 cin  s    vdd gnd XOR2
Xand0 net0 cin  net2 vdd gnd AND2
Xand1 a    b    net3 vdd gnd AND2
Xor0  net2 net3 cout vdd gnd OR2
.ends
```

再根據題目的意思，參考講義製作 D flip flop，作為 register

```
*******************
*** D flip flop ***
*******************
.subckt DFF D Q RST val CLK vdd vss
Xinv  CLK CLK_INV  INV
Xinv2 RST RST_INV  INV

Xnand0 CLK RST_INV RST_syn vdd vss NAND2

Xmux   val  Q        D    net0 vdd  vss MUX2

mn1    net1 CLK_INV   net0 gnd  N_18 w=0.36u l=0.18u

Xnand1 net1 RST_syn   net2 vdd  vss  NAND2
Xinv3  net2 net3      INV

mn2    net1 CLK net3  gnd N_18 w=0.36u l=0.18u
mn3    net4 CLK net2  gnd N_18 w=0.36u l=0.18u

Xinv4  net4 Q       INV
Xnand4 Q    RST_syn Q_inv vdd vss NAND2

mn4    net4 CLK_INV Q_inv gnd N_18 w=0.36u l=0.18u
.ends
```



完整的 circuit diagram



主程式就是根據上面的 diagram，一個 output 使用 4 個 full adder，其中有 2 個 output 是 5bit，1 個 output 是 6bit，1 個 output 是 10bit。

```
XADDER_5b1 a0 a1 a2 a3 b0 b1 b2 b3 c0 c1 c2 c3 c4 ADDER_05b
XADDER_5b2 d0 d1 d2 d3 e0 e1 e2 e3 f0 f1 f2 f3 f4 ADDER_05b
XADDER_6b1 c0 c1 c2 c3 c4 f0 f1 f2 f3 f4 r0 r1 r2 r3 r4 r5 ADDER_06b

XADDER_5b3 u0 u1 u2 u3 v0 v1 v2 v3 m0 m1 m2 m3 m4 ADDER_05b
XADDER_5b4 x0 x1 x2 x3 y0 y1 y2 y3 n0 n1 n2 n3 n4 ADDER_05b
XADDER_6b2 m0 m1 m2 m3 m4 n0 n1 n2 n3 n4 z0 z1 z2 z3 z4 z5 ADDER_06b

Xbuffers1 r0 r1 r2 r3 r4 b_r0 b_r1 b_r2 b_r3 b_r4 BUFFERS
XBUF1 r5 b_r5 BUFFER
Xbuffers4 z0 z1 z2 z3 z4 b_z0 b_z1 b_z2 b_z3 b_z4 BUFFERS
XBUF2 z5 b_z5 BUFFER

XADDER_7b1 b_r0 b_r1 b_r2 b_r3 b_r4 b_r5 P10_s P11_s P12_s P13_s P14_s P15_s P16_s P17_s P18_s P19_s P10 P11 P12 P13 P14 P15 P16 P17 P18 P19 ADDER_07b
XADDER_7b2 b_z0 b_z1 b_z2 b_z3 b_z4 b_z5 P20_s P21_s P22_s P23_s P24_s P25_s P26_s P27_s P28_s P29_s P20 P21 P22 P23 P24 P25 P26 P27 P28 P29 ADDER_07b

Xcontrol_out1 P10 P11 P12 P13 P14 P15 P16 P17 P18 P19 CLK RST 010 011 012 013 014 015 016 017 018 019 CON_OUT

Xbuffers2 010 011 012 013 014 P11_s P12_s P13_s P14_s P15_s BUFFERS
Xbuffers3 015 016 017 018 gnd P16_s P17_s P18_s P19_s P10_s BUFFERS

Xcontrol_out2 P20 P21 P22 P23 P24 P25 P26 P27 P28 P29 CLK RST 020 021 022 023 024 025 026 027 028 029 CON_OUT

Xbuffers5 020 021 022 023 024 P21_s P22_s P23_s P24_s P25_s BUFFERS
Xbuffers6 025 026 027 028 gnd P26_s P27_s P28_s P29_s P20_s BUFFERS
```

```
.subckt ADDER_05b a0 a1 a2 a3 b0 b1 b2 b3 o0 o1 o2 o3 o4
Xadder0 a0 b0 gnd o0 c1 FADDER
Xadder1 a1 b1 c1  o1 c2 FADDER
Xadder2 a2 b2 c2  o2 c3 FADDER
Xadder3 a3 b3 c3  o3 o4 FADDER
.ends
```

```
.subckt ADDER_06b a0 a1 a2 a3 a4 b0 b1 b2 b3 b4 o0 o1 o2 o3 o4 o5
Xadder0 a0 b0 gnd o0 c1 FADDER
Xadder1 a1 b1 c1  o1 c2 FADDER
Xadder2 a2 b2 c2  o2 c3 FADDER
Xadder3 a3 b3 c3  o3 c4 FADDER
Xadder4 a4 b4 c4  o4 o5 FADDER
.ends
```

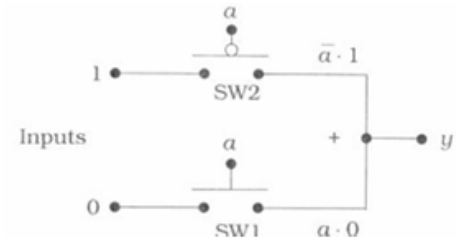
```
.subckt ADDER_10b a0 a1 a2 a3 a4 a5 b0 b1 b2 b3 b4 b5 b6 b7 b8 b9 o0 o1 o2 o3 o4 o5 o6 o7 o8 o9
Xadder0 a0 b0 gnd o0 c1 FADDER
Xadder1 a1 b1 c1  o1 c2 FADDER
Xadder2 a2 b2 c2  o2 c3 FADDER
Xadder3 a3 b3 c3  o3 c4 FADDER
Xadder4 a4 b4 c4  o4 c5 FADDER
Xadder5 a5 b5 c5  o5 c6 FADDER
Xsum6  b6 c6 o6 vdd gnd XOR2
XCout6 b6 c6 c7 vdd gnd AND2
Xsum7  b7 c7 o7 vdd gnd XOR2
XCout7 b7 c7 c8 vdd gnd AND2
Xsum8  b8 c8 o8 vdd gnd XOR2
XCout8 b8 c8 c9 vdd gnd AND2
Xsum9  b9 c9 o9 vdd gnd XOR2
.ends
```

上圖為 5bit、6bit、10bit 的 adder 的個別作法，其中 10bit 因為是 6bit+10bit 的 input，所以後面 4bit 只需用 and xor 判斷有無進位即可。

2. The transistor level view of CIM circuit and adder

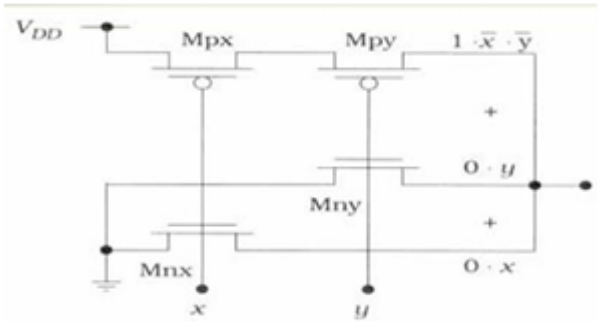
最開始的時候做出了 inverter，使用了 1 個 pmos 及 1 個 nmos 完成

```
****************
*** Inverter ***
****************
.subckt INV in inv_out
mp1 inv_out in vdd vdd P_18 w=0.72u l=0.18u
mn1 inv_out in gnd gnd N_18 w=0.36u l=0.18u
.ends
```



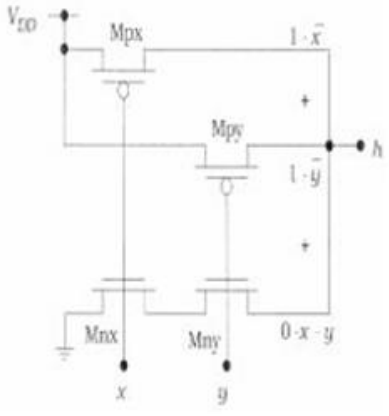
再來實作 NOR 使用了 2 個 pmos 及 2 個 nmos，為了方便辨別，將其標為語課本相同的變數名稱，而 Mpx 傳到 Mpy 那段導線則為 out。

```
************
*** NOR2 ***
************
.subckt NOR2 x y NOR vdd vss
** Your code **
mpx1 out x vdd vdd P_18 w=0.72u l=0.18u
mpy1 NOR y out vdd P_18 w=0.72u l=0.18u
mnx1 NOR x vss gnd N_18 w=0.36u l=0.18u
mny1 NOR y vss gnd N_18 w=0.36u l=0.18u
.ends
```



接著實作 NAND，共使用了 2 個 pmos 及 2 個 nmos，為了方便辨別，一樣 標為課本變數名稱，其中 out1 是 Mnx 傳到 Mny 那一段導線

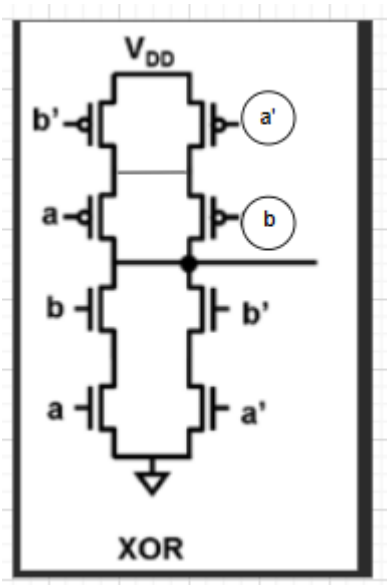
```
*************
*** NAND2 ***
*************
.subckt NAND2 x y NAND vdd vss
** Your code **
mpx2 NAND x vdd  vdd P_18 w=0.72u l=0.18u
mpy2 NAND y vdd  vdd P_18 w=0.72u l=0.18u
mnx2 out1 x vss  gnd N_18 w=0.36u l=0.18u
mny2 NAND y out1 gnd N_18 w=0.36u l=0.18u
.ends
```



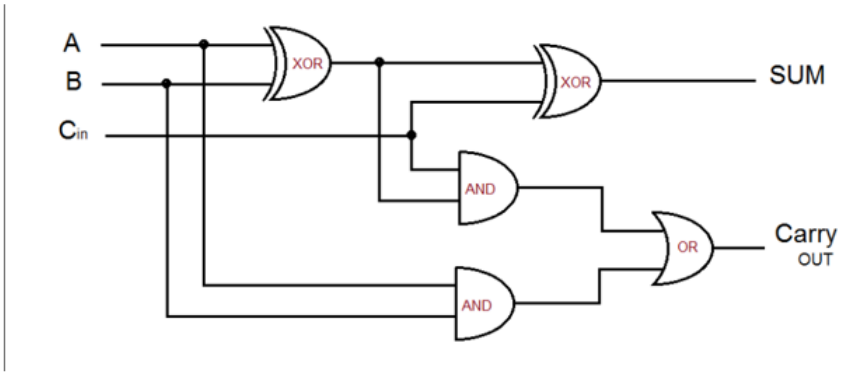
接下來用 NOR2 跟 NAND2 合併 inverter 即為 AND2 跟 OR2

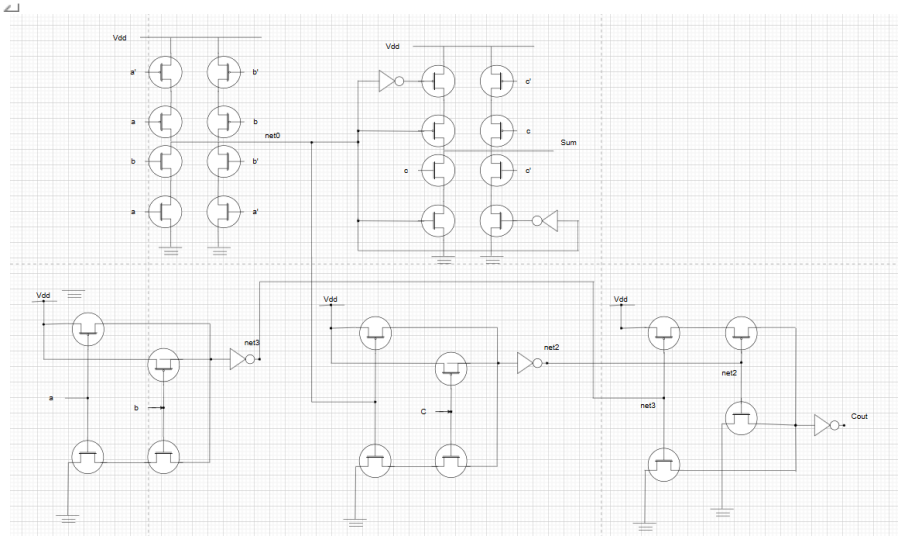
再來是 XOR2 的實作，使用了前面的 inverter，最後將結果導入 Y

```
***************
*** XOR2 ***
***************
.subckt XOR2 A B Y vdd vss

Xinv1 A A_INV INV
Xinv2 B B_INV INV

mp1 out1  A_INV vdd  vdd P_18 w=0.72u l=0.18u
mp3 out1  B_INV vdd  vdd P_18 w=0.72u l=0.18u
mp2 Y     A     out1 vdd P_18 w=0.72u l=0.18u
mp4 Y     B     out1 vdd P_18 w=0.72u l=0.18u

mn1 out3  A     vss  gnd N_18 w=0.36u l=0.18u
mn2 out4  A_INV vss  gnd N_18 w=0.36u l=0.18u
mn3 Y     B     out3 gnd N_18 w=0.36u l=0.18u
mn4 Y     B_INV out4 gnd N_18 w=0.36u l=0.18u
.ends
```

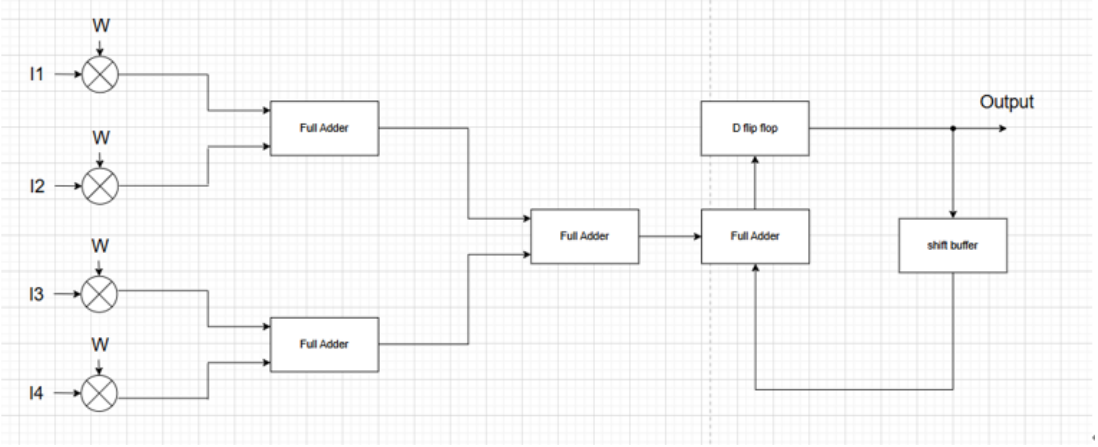


然後將上面 transistor 連成下圖，即完成 full adder，下下圖即為 transistor level

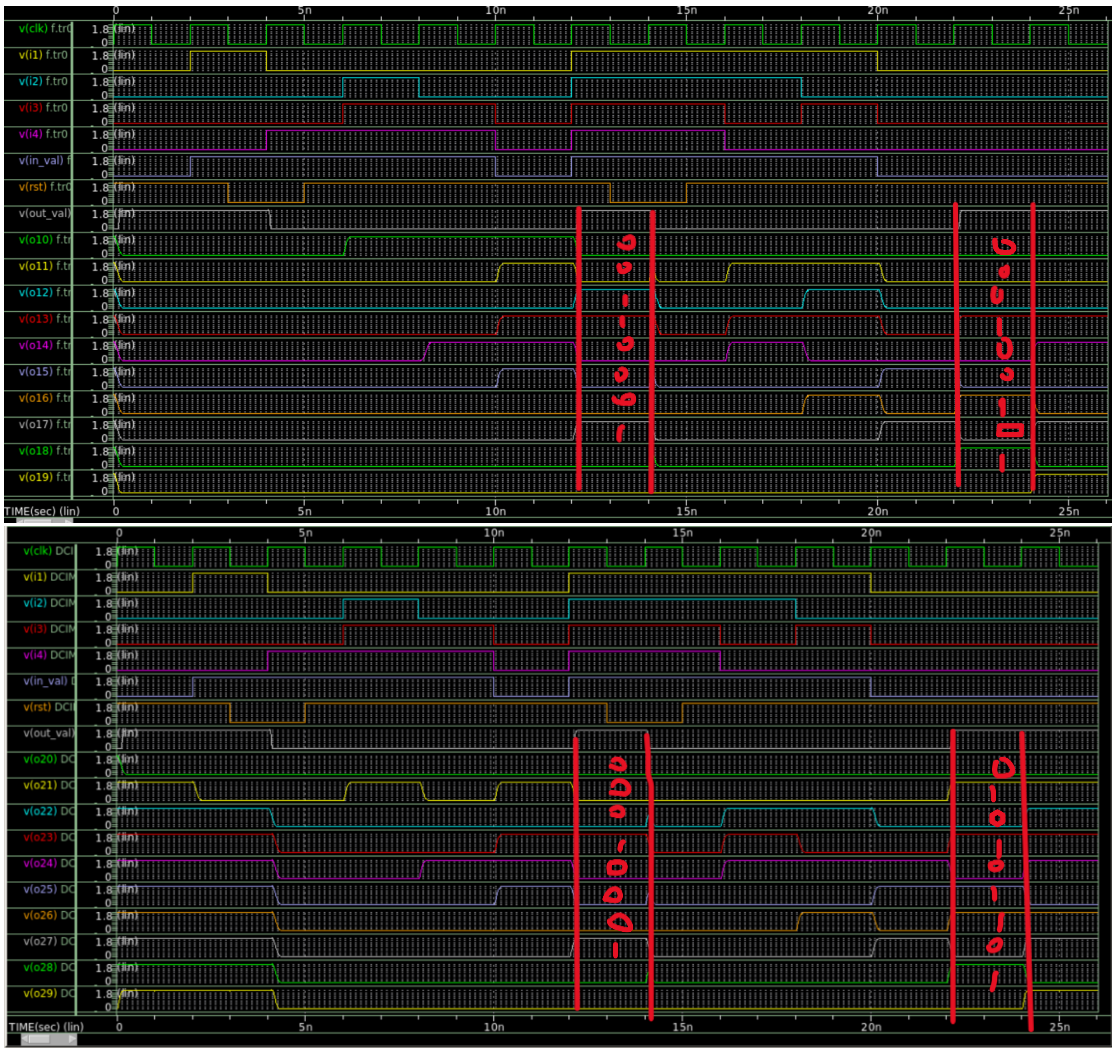




再來將加法器，組成下圖，即完成。



3. Bonus
4. waveform



5. The delay and the power of the circuit

```
****** transient analysis tnom=  25.000 temp=  30.000 ******
td=   1.2156n  targ=   5.3111n   trig=   4.0955n
pwr=   1.4772m  from=   0.             to=  26.0000n
```

6. The total number of transistors (NMOS and PMOS) use in this program

```
******  Circuit Statistics  ******
# nodes       =    7790 # elements   =    3118
# resistors   =       0 # capacitors =       0 # inductors   =       0
# mutual_inds =       0 # vccs       =       0 # vcvs        =       0
# cccs        =       0 # ccvs       =       0 # volt_srcs   =       8
# curr_srcs   =       0 # diodes     =       0 # bjts        =       0
# jfets       =       0 # mosfets    =    3110 # U elements  =       0
# T elements  =       0 # W elements =       0 # B elements  =       0
# S elements  =       0 # P elements =       0 # va device   =       0
# vector_srcs =       0 # N elements =       0
```

7. The hardness of this assignment and how you overcome it

   最難的部分就是明明照著公式打，不知道為什麼在輸出的時候就是不一樣，中間的時候，有發現不能拿 output 當 input，像是 p1 = P1 and p2，這樣打好像會出錯，太習慣軟體 coding 方法，會非常不習慣，所以我後面決定用變數解決他，令了一堆變數找了一堆 buffer，讓線路至少可以成功相連。

8. Any suggestions about this programming assignment

   難度適中，感人肺腑，寫完時不禁潸然淚下，希望成績出來不是另一種落淚

   感覺好像可以把 clock 週期時間調長一點，我前面做了其他方法的加法器速度太慢，但我沒察覺，就花了 10 幾個小時 debug，最後換方法重做一個後，答案才是正確的。