CS3120
Introduction of Integrated Circuit Design

Chapter 1
An Overview of VLSI

Andy, Yu-Guang Chen
Associate Professor, Department of EE, National Central University
Adjunct Assistant Professor, Department of CS, National Tsing Hua University
andyygchen@ee.ncu.edu.tw

Course Objectives

- The objectives of this course
  - Understand the basics of digital VLSI chip design
  - Emphasis is on the details of translating a system specification to a small piece of silicon
- Some materials may not make sense until the later chapter
  - Encompasses several distinct areas of expertise

Outline

- What is VLSI?
- From Semiconductor to VLSI
- VLSI Design Flow and Design Styles

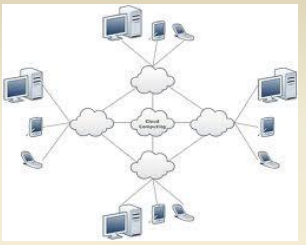
Outline

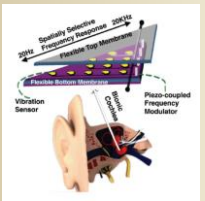
- What is VLSI?
- From Semiconductor to VLSI
- VLSI Design Flow and Design Styles

What is VLSI ?

- VLSI: very large-scale integration
  - The process of integrating or embedding hundreds of thousands of transistors on a single silicon semiconductor microchip
  - Long time ago…
    - ✓ Small scale integration (SSI): 1-100 transistors could be fabricated on a single chip
    - ✓ Medium scale integration (MSI): 100-1000 number of transistors could be integrated on a single chip
    - ✓ Large scale integration (LSI): 1000-10000 transistors….
    - ✓ Very large scale integration (VLSI): 10000-1 Million transistors…
    - ✓ Ultra large scale integration (ULSI): 1 Million-10 Million transistors ….
- Integrated circuit
  - The circuit in which all the Passive and Active components are fabricated onto a single chip
- Now, VLSI and IC are used interchangeable

What Does an IC Do?

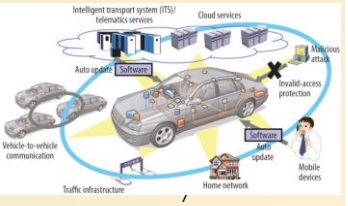




Green Technology

What Does an IC Do?

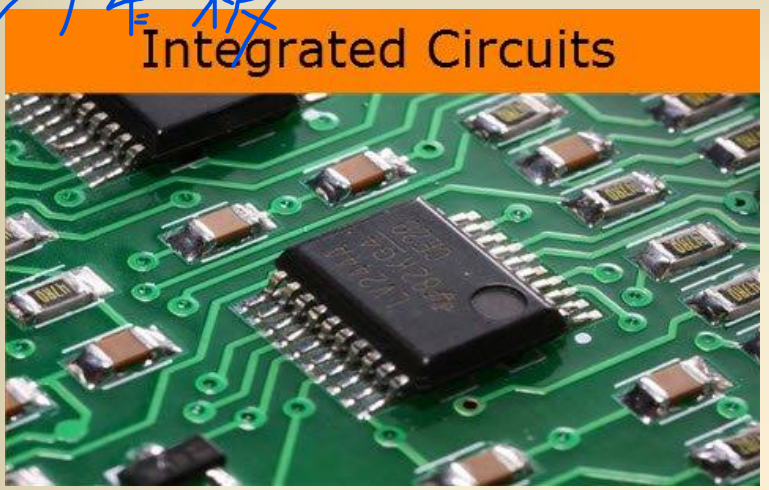
Source: IoT Times



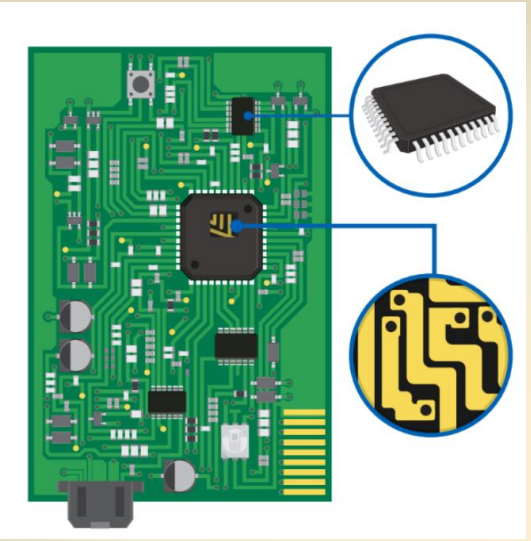
alphago

How IC Looks Like?

門客板

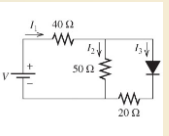


How IC Looks Like?



What is An Integrated Circuits (IC)

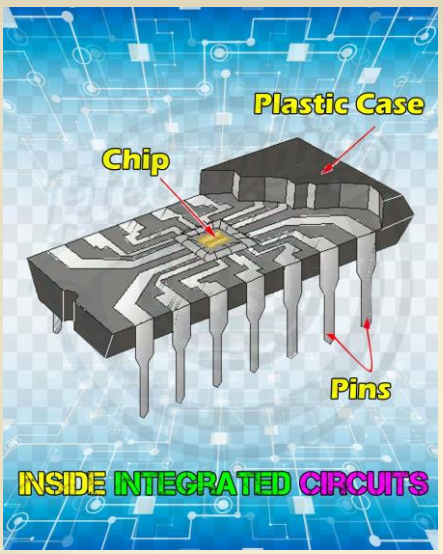
- Electronic Circuit
  - An electronic circuit is composed of individual electronic components, such as resistors, transistors, capacitors, inductors and diodes, connected by conductive wires or traces through which electric current can flow
  - The combination of components and wires allows various simple and complex operations to be performed



What is An Integrated Circuits (IC)

- Integrated Circuits
  - A set of electronic circuits on one small flat piece (or "chip") of semiconductor material that is normally silicon
  - The integration of large numbers of tiny MOS transistors into a small chip results in circuits that are orders of magnitude smaller, faster, and less expensive

What is An Integrated Circuits (IC)

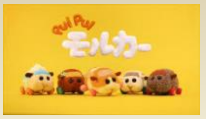


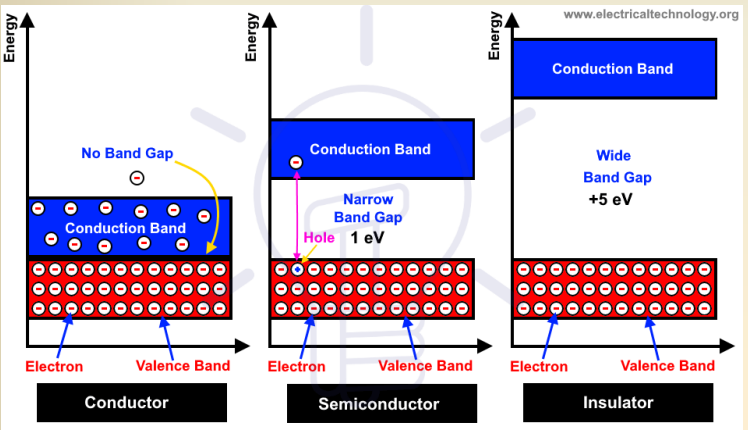
Outline

- What is VLSI?
- From Semiconductor to VLSI
- VLSI Design Flow and Design Styles

Semiconductor and IC

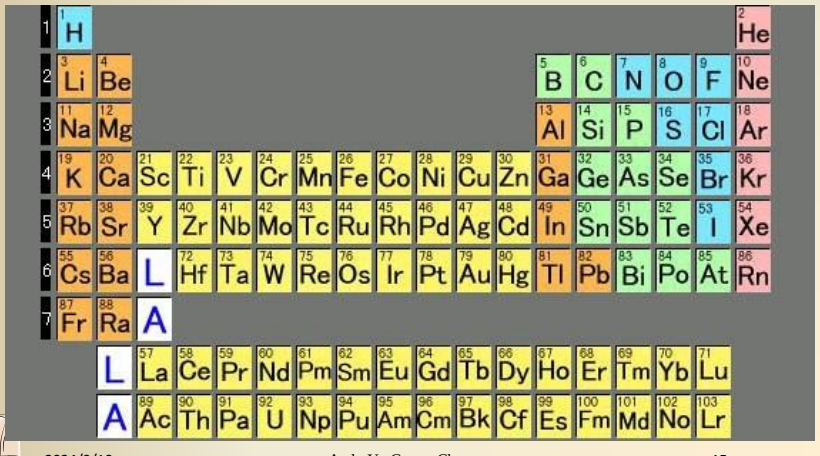
- Semiconductor





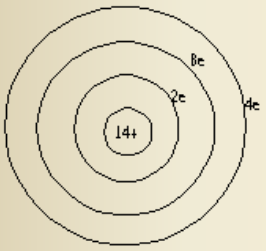
Semiconductor and IC

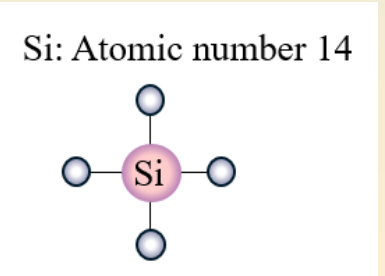
- Recall from your high school…



Semiconductor and IC

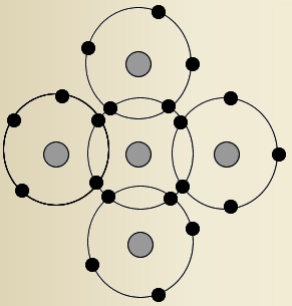
- A silicon atom has 14 electrons around the nucleus
  - There are 4 valence electrons on the outermost orbital

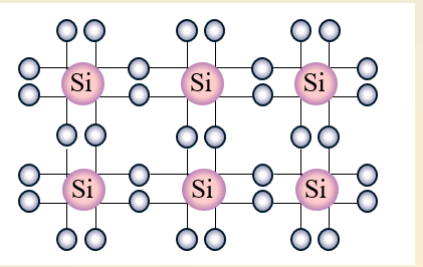




Semiconductor and IC

- When this is made into a single crystal, it can be used as a material for semiconductor products.

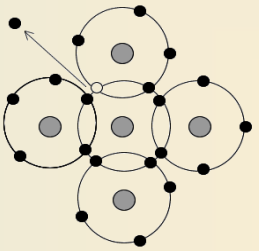




https://www.shindengen.com/products/semi/column/basic/semi/semi_basic.html

Semiconductor and IC

- Semiconductor behaves as an insulator at absolute zero temperature
- With an increase of temperature, the conductivity of semiconductor increases and resistivity decreases

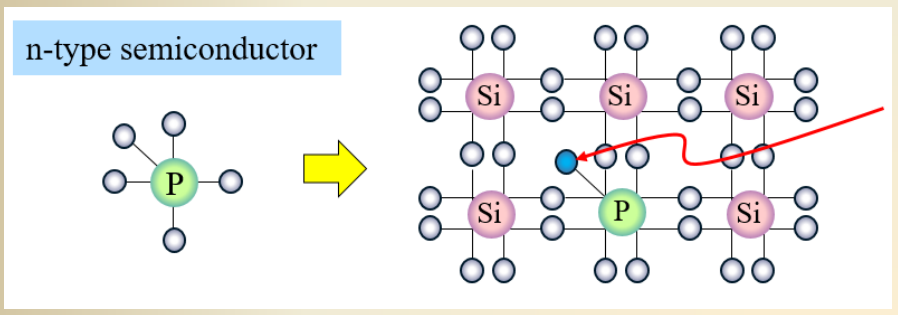


Semiconductor and IC

- Doping silicon with other impurities changes it so it is conductive
- The semiconductor is categorized as a p-type or n-type depending on the type of impurities that are doped
- Junctions based on the p-types and n-types are integrated into one chip in order to use it as an electronic component

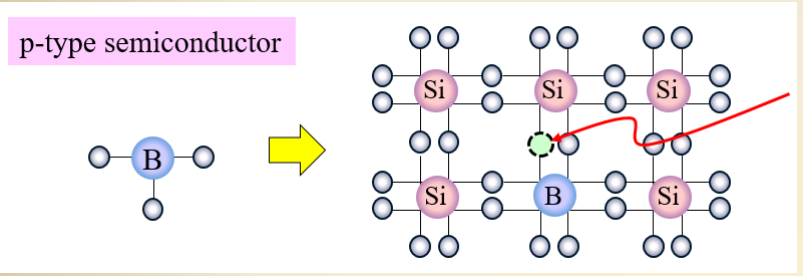
Semiconductor and IC

- Group V: extra electron (n-type)

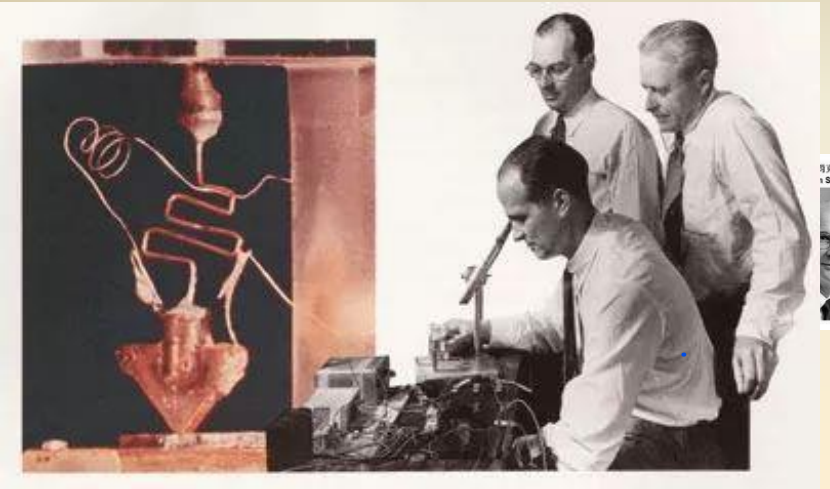


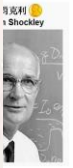
Semiconductor and IC

◆Group III: missing electron, called hole (p-type)



Evolution of Integrated Circuits

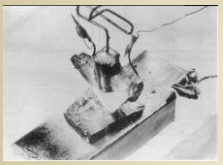




Polysi

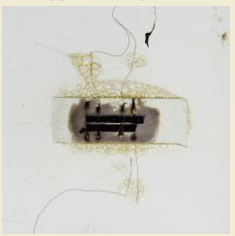
SiO

Evolution of Integrated Circuits

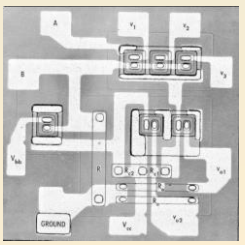


First transistor (Bell Labs, 1948)
Source: J. Rabaey, 2004

On September 12th, 1958, Kilby demonstrated the first working IC and applied for a patent on February 6th, 1959.



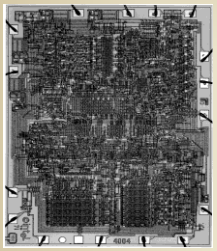
Kilby Phase Shift Oscillator Circuit (1958)
Photo: Christie's Auction House



ECL 3-input Gate (bipolar logic), Motorola 1966

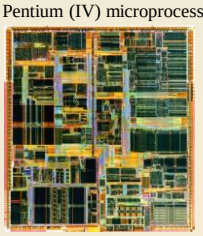
Evolution of Integrated Circuits

Intel 4004 Microprocessor

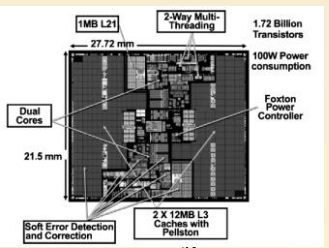


1000 transistors,1 MHz operation, 1971

Intel Pentium (IV) microprocessor



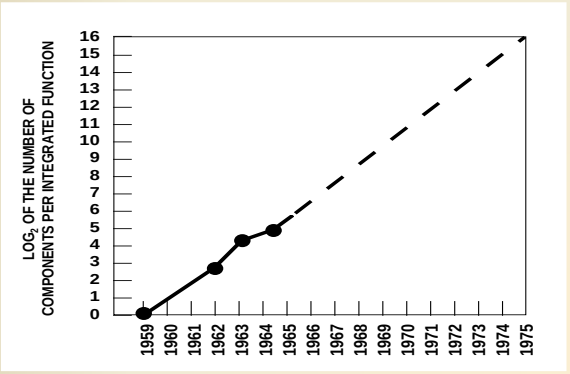
Intel Itanium microprocessor (2006, JSSC)



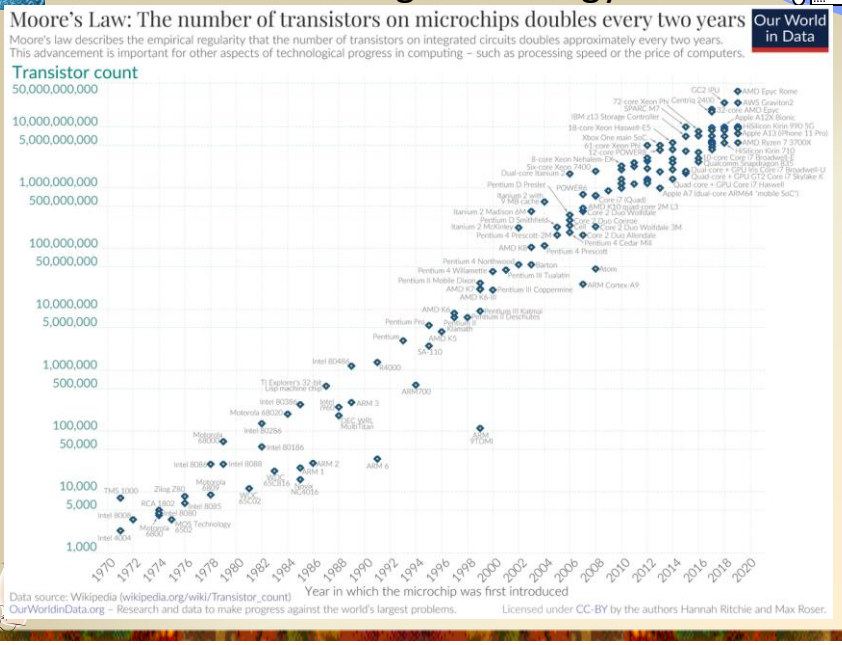
Source: J. Rabaey, 2004

"Moore's" Law: Driving Technology Advances

- In 1965, Gordon Moore noted that the number of transistors on a chip doubled every 18 to 24 months. He made a prediction that semiconductor technology will double its effectiveness every 18 months [Electronics, April 19, 1965]



"Moore's" Law: Driving Technology Advances



Moore's Law

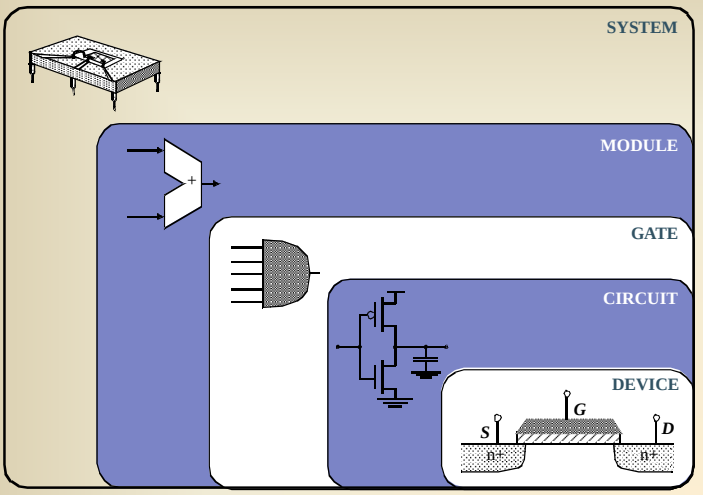
Moore's Law

Moore's Law

Why Scaling?

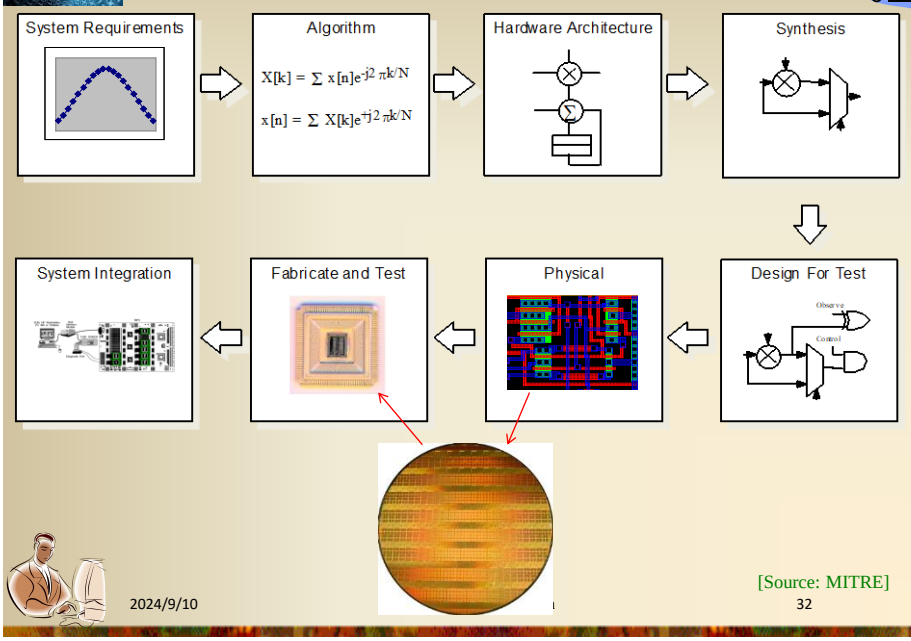
- Technology shrinks by 0.7/generation
- With every generation can integrate 2x more functions per chip; chip cost does not increase significantly
- Cost of a function decreases by 2x
- But …
  - How to design chips with more and more functions?
  - Design engineering population does not double every two years…
- Hence, a need for more efficient design methods
  - Exploit different levels of abstraction

Design Abstraction



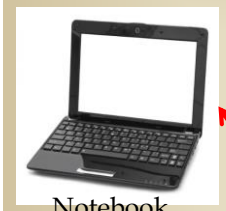
Source: J. Rabaey, 2004

System to Silicon



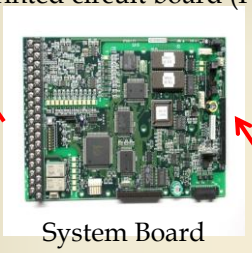
[Source: MITRE]

Integrated Circuit ➔ System Board ➔ Product



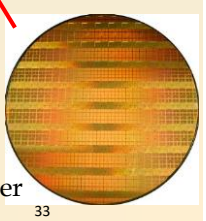
Notebook

Printed circuit board (PCB)



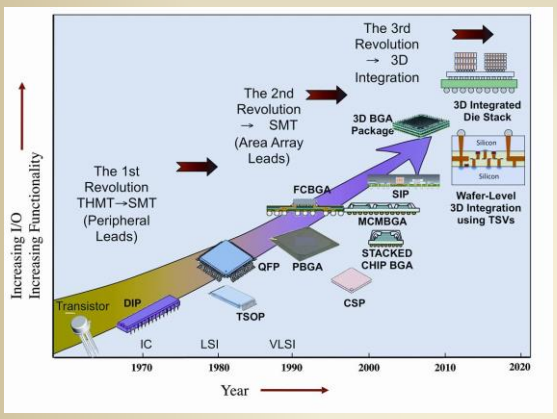
System Board

Integrated Circuit (IC)



Wafer

Packaging Technology Evolution Trends



THMT: through hole mount technology
SMT: surface mount technology
DIP: dual in-line package
TSOP: thin small-outline package
QFP: quad flat package
PBGA: plastic ball grid array
FCBGA: flip chip ball grid array

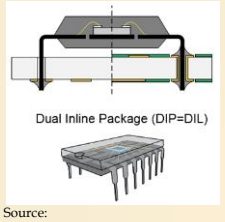
Source: Electronics Cooling

Source: Polymer Innovation blog

QFP

QFN
(quad flat no lead)

PBGA

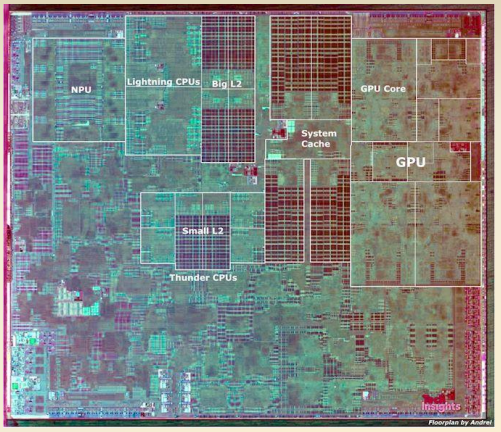


Source:
http://www.ett.bme.hu/meca/courses/TEP/2_1.html

What Does an IC Look Like Today?

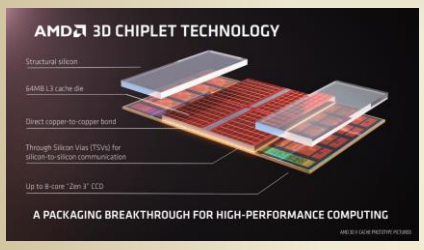
Apple A11 Bionic Processor

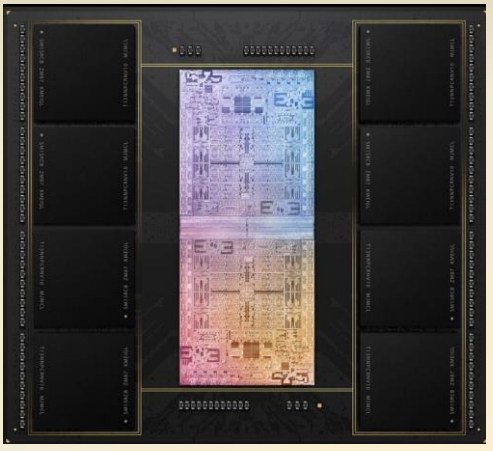
Apple A13 Bionic Processor



1. TSMC 10nm FinFET process
2. Die area=87.66mm^2
3. 4.3 billion transistors
4. Max. freq. of CPU = 2.39 GHz consuming 120W
5. 8MB L2 cache [Source: Wiki]

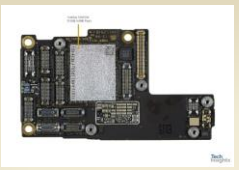
What Does an IC Look Like Today?

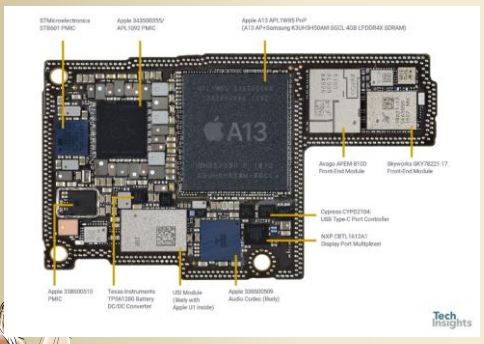




Apple M1 Ultra

Teardown of Apple iPhone 11 Pro Max





	Apple iPhone 11 Pro Max
Applications Processor	**$64.00**
Baseband Processor	$25.50
Battery	$10.50
Camera / Image	$73.50
Connectivity	$10.50
Display / Touchscreen	$66.50
Memory: Non-Volatile**	$58.00
Memory: Volatile	**$11.50**
Mixed Signal	$1.50
Non-Electronics	$61.00
Other	$21.00
Power Management / Audio	$10.50
RF Component	$30.00
Sensor	$1.50
Substrates	$16.50
Supporting Materials	$7.50
Final Assembly & Test	$21.00
Total	$490.50

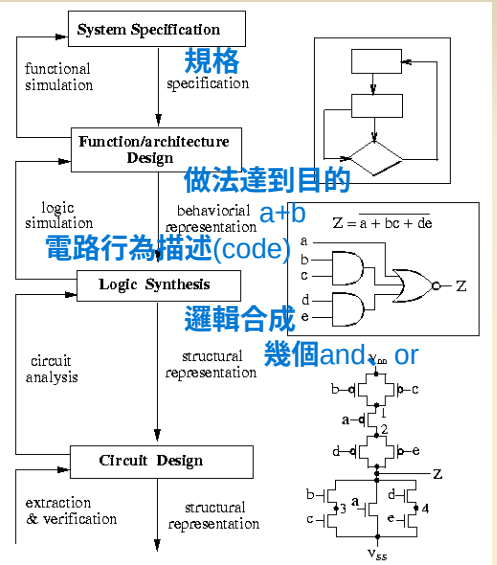
What is This Course all About?

- Scopes of very large-scale integration (VLSI) design
  - Digital circuits
  - Analog circuits
  - Mixed-signal circuits
  - Memory circuits
- This course will cover the following contents
  - CMOS devices and manufacturing technology; CMOS inverters and gates; propagation delay; noise margins; CMOS power dissipation; reliability, sequential circuits
- What will you learn?
  - Understanding, designing, and optimizing digital circuits with respect to different quality metrics: area, speed, and power dissipation

Outline

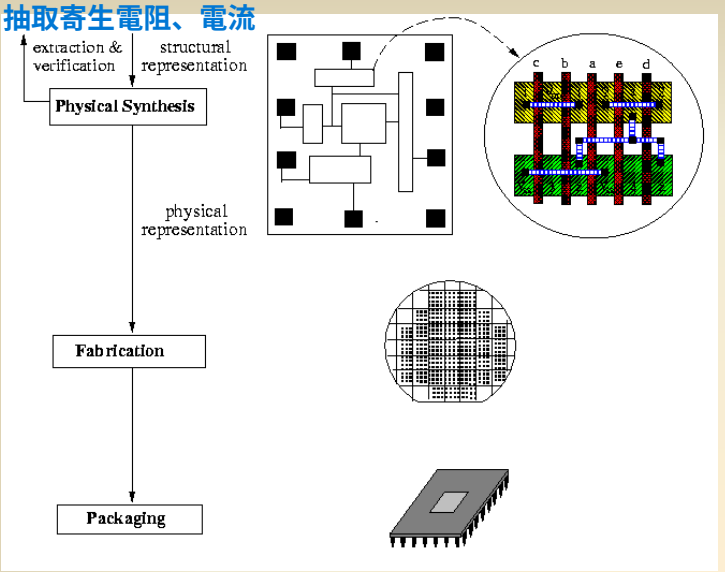
- What is VLSI?
- From Semiconductor to VLSI
- VLSI Design Flow and Design Styles

Traditional VLSI Design Flow



Traditional VLSI Design Flow

抽取寄生電阻、電流



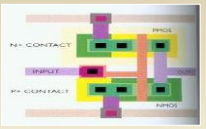
Traditional VLSI Design Flow

- Spec
  - Specifies what the chip should do, how fast and always incomplete, a set of requirements.
    - Function, speed, size, ..etc
- Abstract high-level model
  - Much more precise. Spec is in English while behavior is generally modeled as some executable program such as C or C++.
  - The system's behavior is fully specified. Inputs and outputs values on every clock cycle. (HDL)

Traditional VLSI Design Flow

- Logic synthesis
  - The system is designed in terms of logic gates, latches, and flip flops. Delay cannot make extremely accurate delay
  - Characteristics of the silicon circuits become important.
  - HDL ➔ Logic gates by CAD tool
- Circuit design
  - Transistors are used as switches and Boolean variables are treated as varying voltage signals

Traditional VLSI Design Flow



- Physical Design (Layout)
  - The final design for fabrication or Layout is the lowest level of design abstraction
  - Transistors are defined as 3-dimesional structures
  - Placed and wired using another set of CAD tools
  - The configuration of rectangles in layout determines the circuit topology and the characteristics of components
  - Geometrical patterns on the surface of silicon

Traditional VLSI Design Cycles

1. System specification
2. Functional design
3. Logic synthesis
4. Circuit design
5. Physical design
6. Fabrication
7. Packaging

Micron tehcnology => 1um, 2um, 3um, etc
Sub-micron techology => 0.8um, 0.6um, 0.35um 0.25um etc
Deep sub-micro technology => 0.18um, 0.13um
Nanotechnoogy => 90nm, 65nm, 45nm etc
Nowadays => 2nm, 3nm, 5nm, etc

- Other tasks involved: verification, testing, etc.
- Design metrics: area, speed, power dissipation, noise, design time, testability, etc.
- Design revolution: interconnect (not gate) delay dominates circuit performance in deep submicron era.
  - Interconnects are determined in physical design.
  - Shall consider interconnections in early design stages.

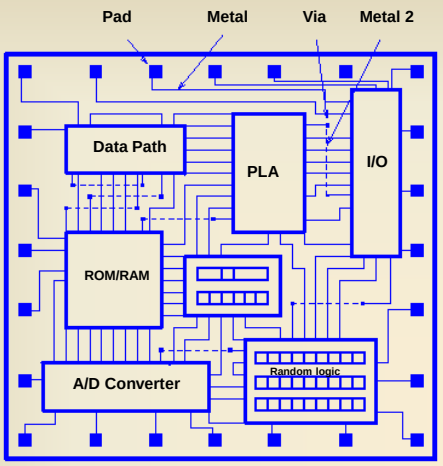
Design Steps

- Specification: function, cost, etc
- Architecture: large blocks
- Logic: gates + registers
- Circuits: transistor sizes for speed, power
- Layout: determines parasites

Design Styles

- Full Custom Design Style 去家具行量身訂做
  - Design every component from scratch
- Standard Cell Design Style 去家具行買家具
  - Selects pre-designed cells (of same height)
- Application specific integrated circuits (ASICs) 針對特定功能所做的design
  - ASICs are very popular for prototyping or low –volume production.
  - Using an extensive suite of CAD tools
- Field Programmable Gate Arrays (FPGA) 先做硬體，再做功能
  - Logic and interconnects are both prefabricated
  - Program the logic functions and interconnects

Full Custom Design Style / ASIC

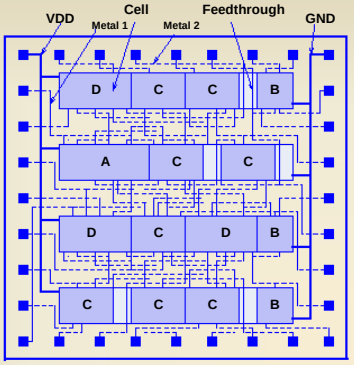


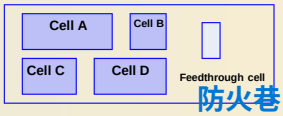
1.IC框框

2.I/O pad

3.連接 I/O pad

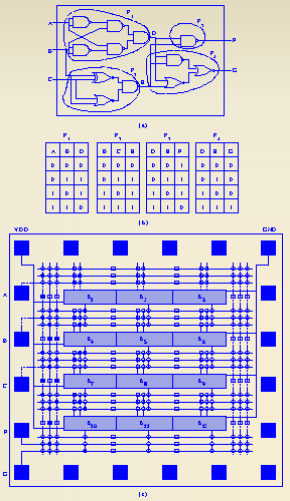
Standard Cell Design Style





防火巷

FPGA Design Style



Comparisons of Design Styles

	Style		
	full-custom	standard cell	FPGA
cell size	variable	fixed height *	fixed
cell type	variable	variable	programmable
cell placement	variable	in row	fixed
interconnections	variable	variable	programmable
design cost	high	medium	low

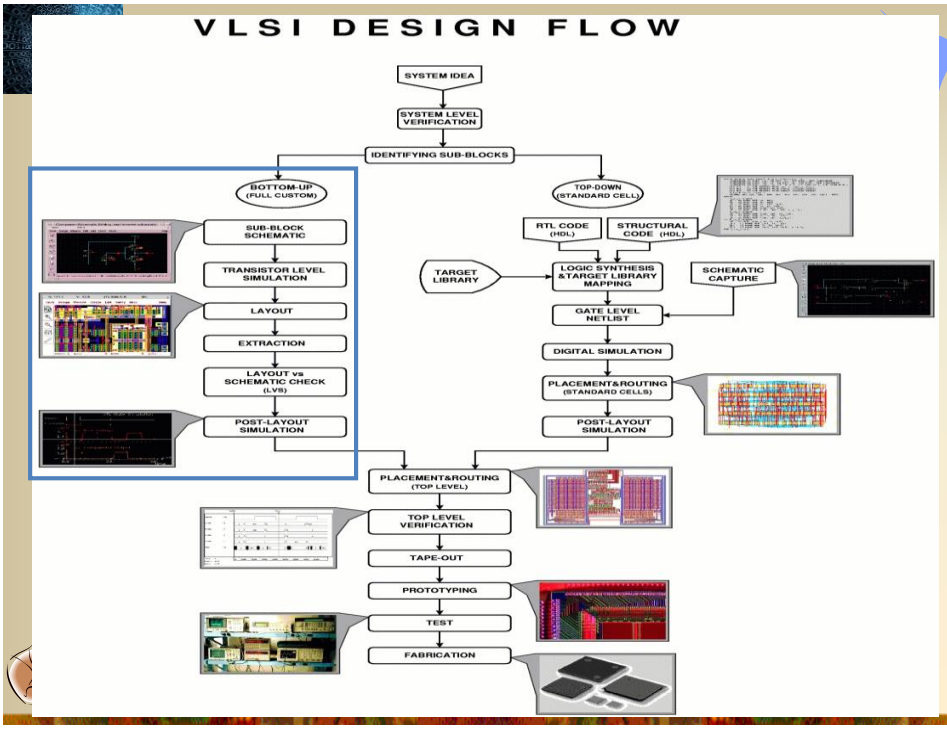
* uneven height cells may be used

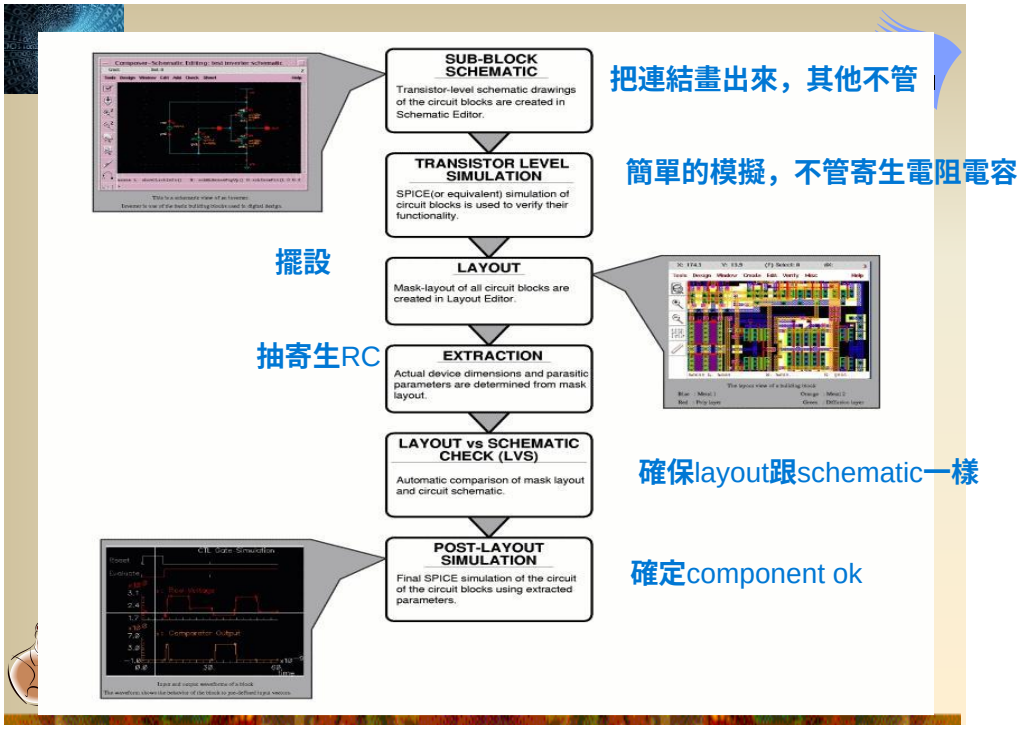
Comparisons of Design Styles

	style			
	full-custom	standard cell	FPGA	
Area	compact	compact to moderate	large	
Performance	high	high to moderate	low	
Fabrication layers	all	all	none	

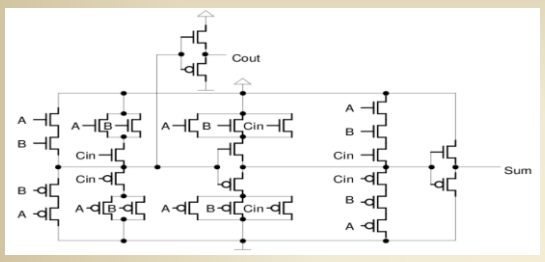
Design Process

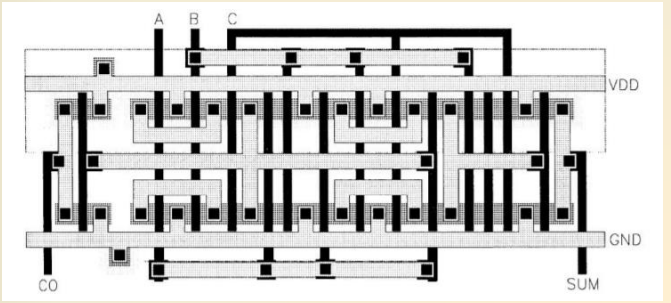
- Top Down
  - Standard-cell based design
  - Easy but not provide full flexibility
- Bottom Up
  - Full-custom based design
  - Acceptable for small projects but impractical
  - Study works well for learning the basics
  - The first half of the book starts simple and evolve into higher levels of complexity

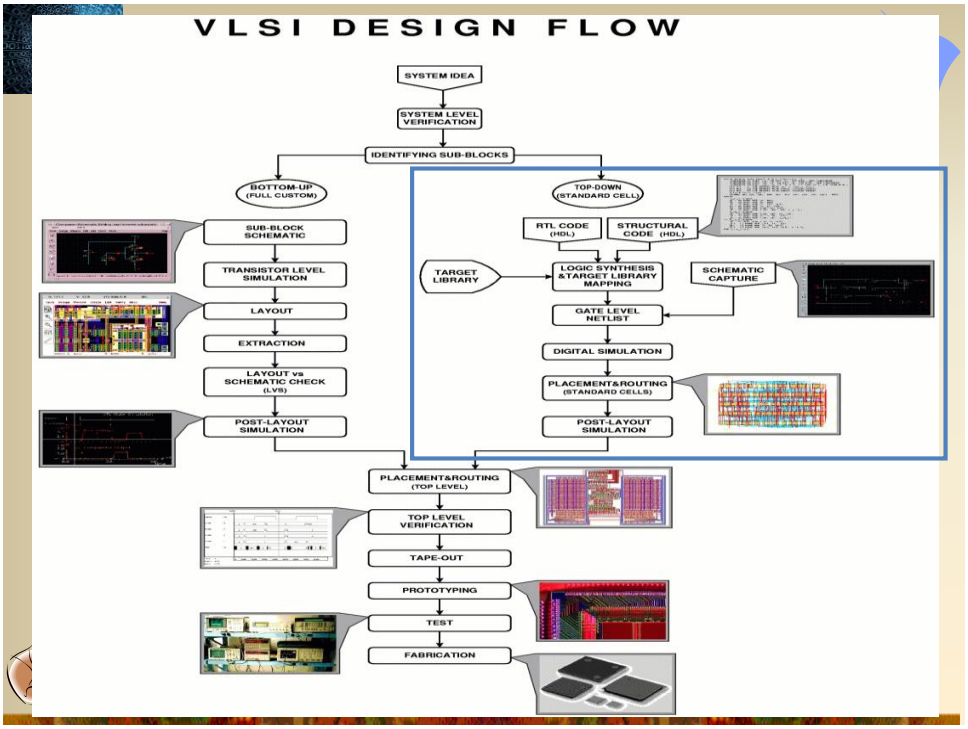


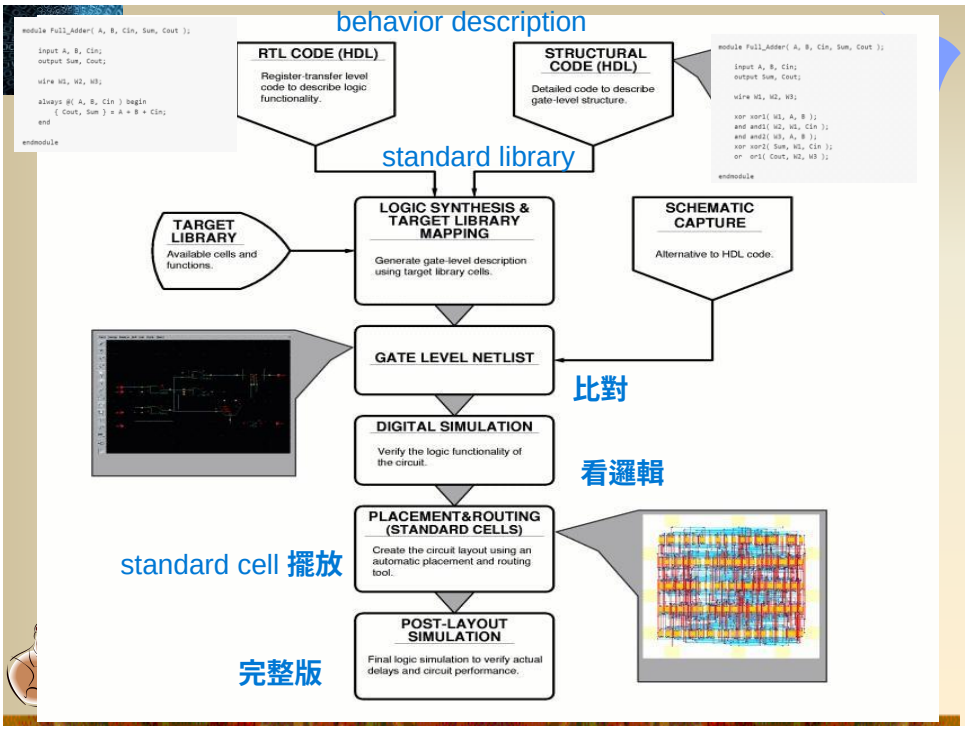


One-bit Mirror Adder Layout

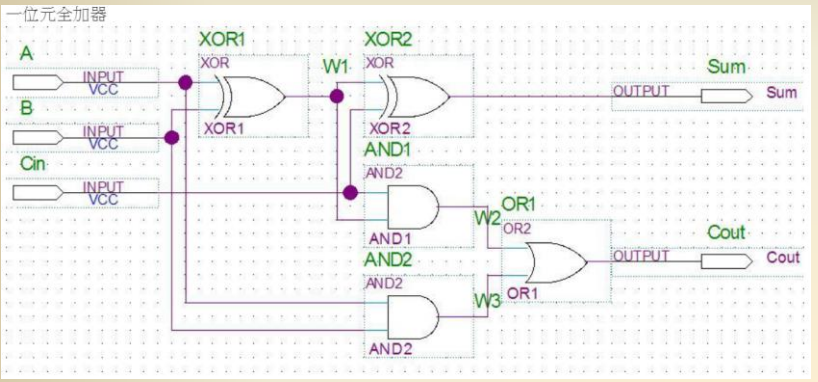


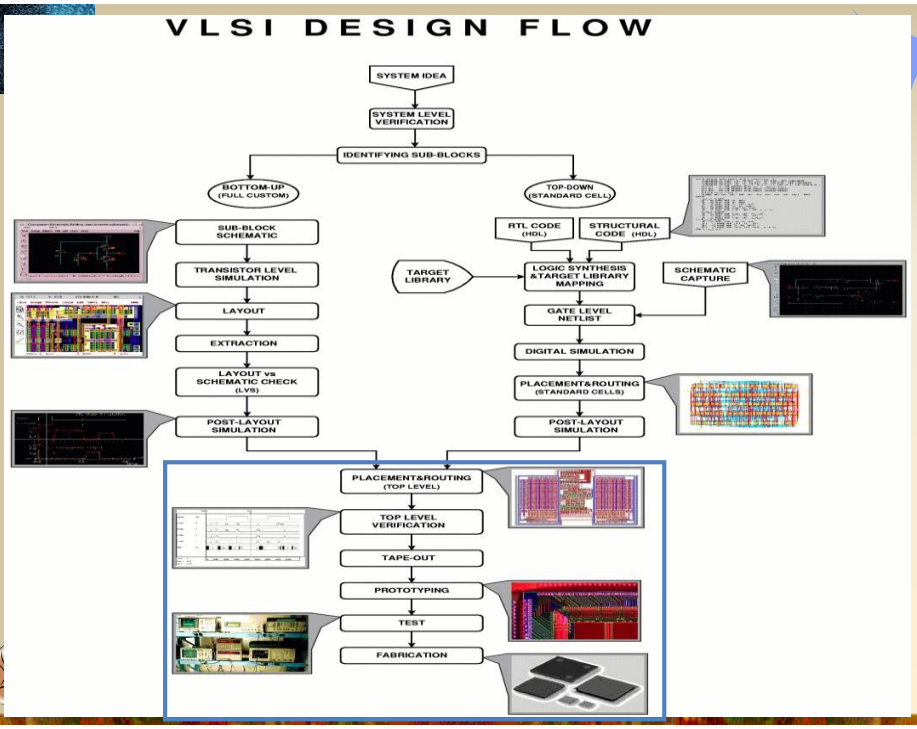


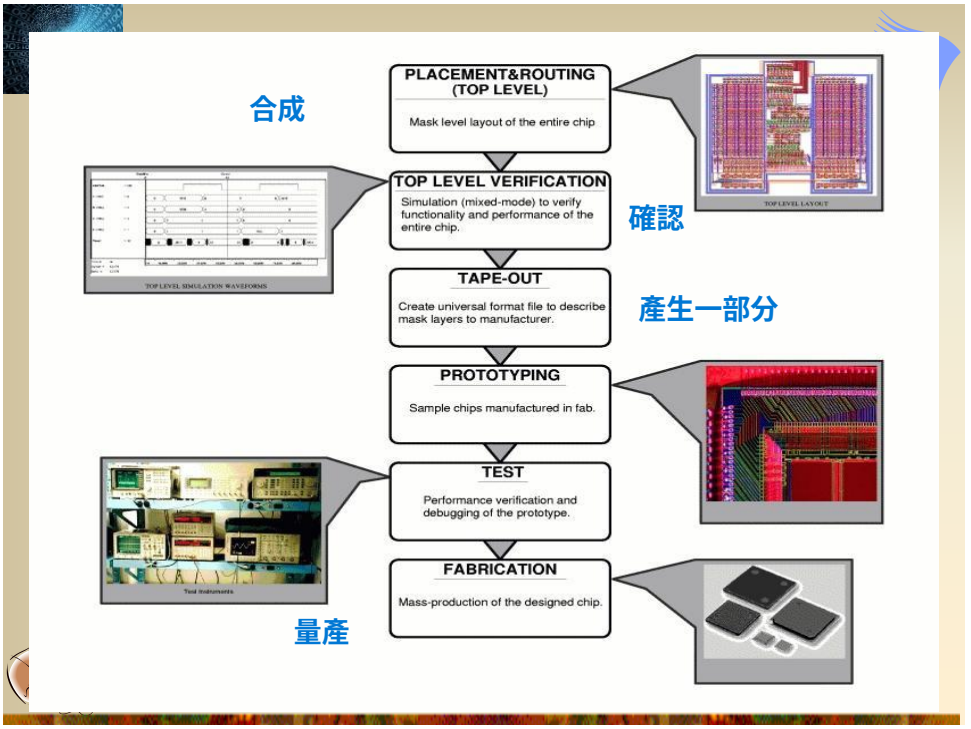

VLSI DESIGN FLOW
SYSTEM IDEA
SYSTEM LEVEL VERIFICATION
IDENTIFYING SUB-BLOCKS
BOTTOM-UP (FULL CUSTOM)
SUB-BLOCK SCHEMATIC
TRANSISTOR LEVEL SIMULATION
LAYOUT
EXTRACTION
LAYOUT vs SCHEMATIC CHECK (LVS)
POST-LAYOUT SIMULATION
TOP-DOWN (STANDARD CELL)
RTL CODE (HDL)
STRUCTURAL CODE (HDL)
TARGET LIBRARY
LOGIC SYNTHESIS &TARGET LIBRARY MAPPING
SCHEMATIC CAPTURE
GATE LEVEL NETLIST
DIGITAL SIMULATION
PLACEMENT&ROUTING (STANDARD CELLS)
POST-LAYOUT SIMULATION
PLACEMENT&ROUTING (TOP LEVEL)
TOP LEVEL VERIFICATION
TAPE-OUT
PROTOTYPING
TEST
FABRICATION

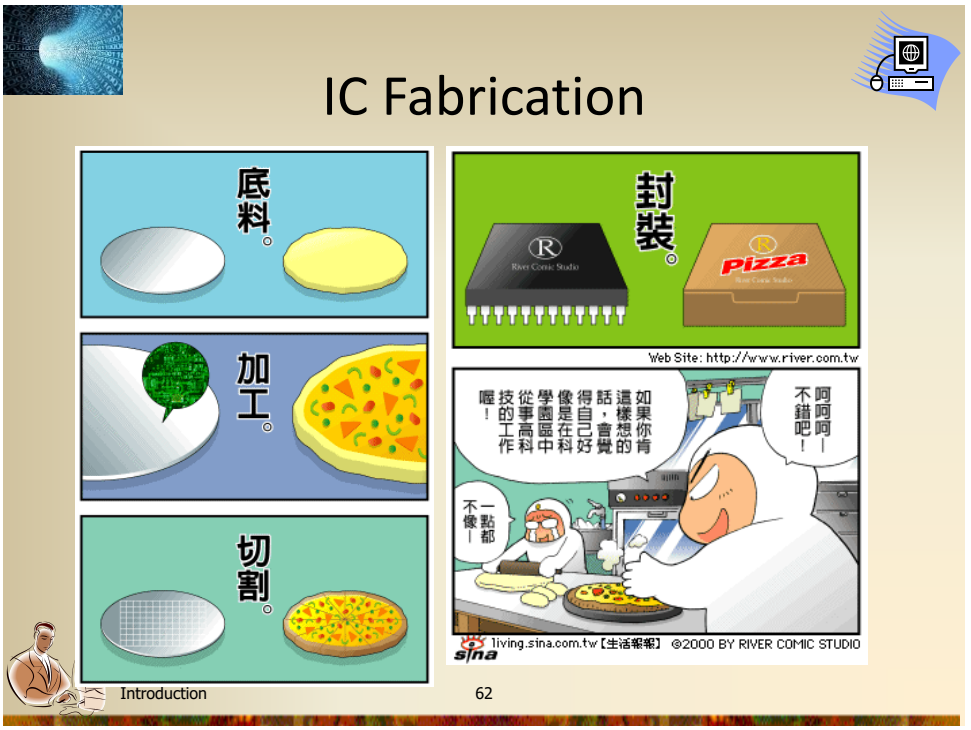

behavior description
RTL CODE (HDL)
Register-transfer level code to describe logic functionality.
STRUCTURAL CODE (HDL)
Detailed code to describe gate-level structure.
standard library
TARGET LIBRARY
Available cells and functions.
LOGIC SYNTHESIS & TARGET LIBRARY MAPPING
Generate gate-level description using target library cells.
SCHEMATIC CAPTURE
Alternative to HDL code.
GATE LEVEL NETLIST
比對
DIGITAL SIMULATION
Verify the logic functionality of the circuit.
看邏輯
PLACEMENT&ROUTING (STANDARD CELLS)
Create the circuit layout using an automatic placement and routing tool.
standard cell 擺放
POST-LAYOUT SIMULATION
Final logic simulation to verify actual delays and circuit performance.
完整版

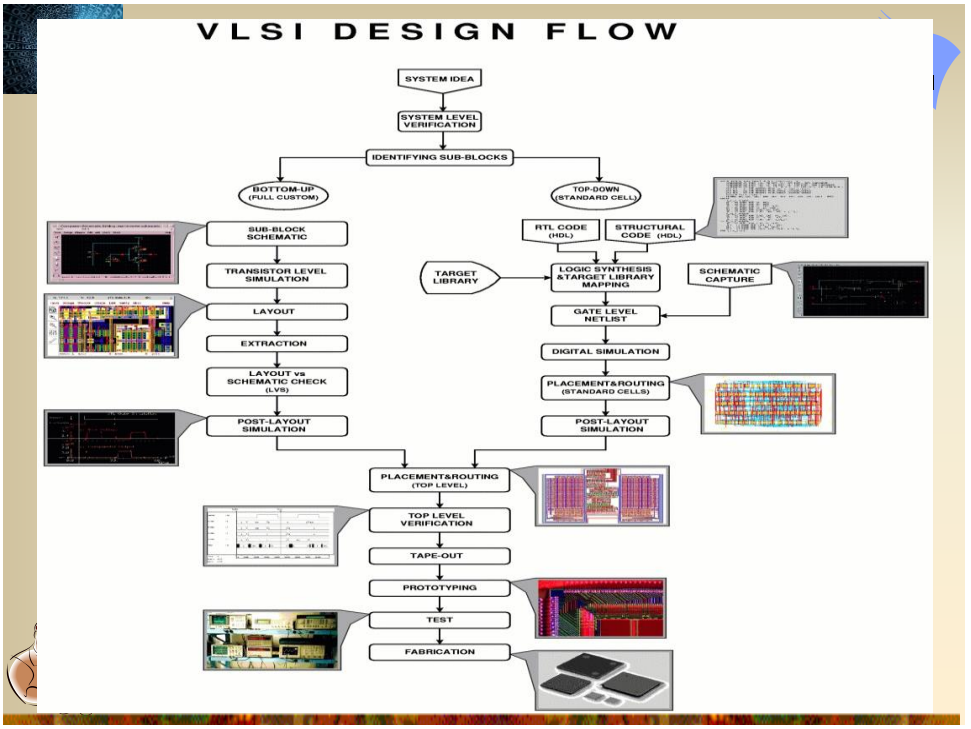
One Bit Full Adder





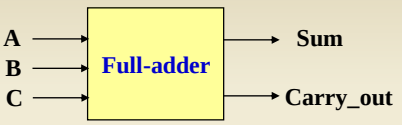

合成
PLACEMENT&ROUTING (TOP LEVEL)
Mask level layout of the entire chip
TOP LEVEL VERIFICATION
Simulation (mixed-mode) to verify functionality and performance of the entire chip.
確認
TAPE-OUT
Create universal format file to describe mask layers to manufacturer.
產生一部分
PROTOTYPING
Sample chips manufactured in fab.
TEST
Performance verification and debugging of the prototype.
FABRICATION
Mass-production of the designed chip.
量產


IC Fabrication
底料
加工
切割
封裝
Pizza
Web Site: http://www.river.com.tw
如果你肯這樣想的話，會覺得自己好像是在科學園區中從事高科技的工作喔！
呵呵呵～不錯吧！
一點都不像！
living.sina.com.tw【生活報報】 ©2000 BY RIVER COMIC STUDIO



A Simple Example

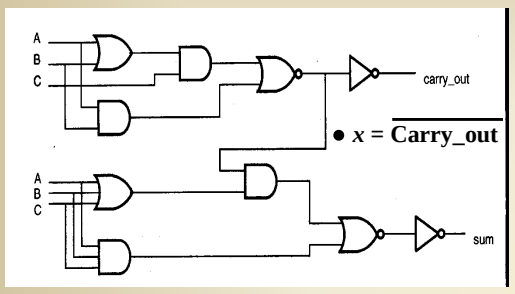
- Functionality
  - One-bit binary full-adder
- Technology
  - 1 μm n-well CMOS technology
- Speed
  - Input to output delay < 5 ns
- Area
  - < 3000 μm^2
- Power Dissipation



Boolean Description

$$Sum = A \oplus B \oplus C$$
$$= \bar{A}\bar{B}C + \bar{A}B\bar{C} + A\bar{B}\bar{C} + ABC$$
$$Carry\_out = AB + BC + CA$$
(majority function)

Logic Design



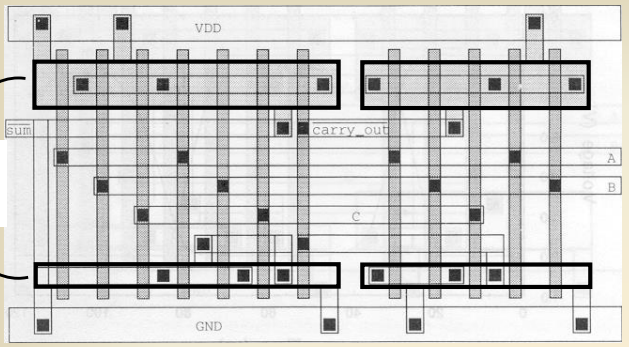
# of '1's In A, B, C	Carry_out	Sum
0	0	0
1	0	1
2	1	0
3	1	1

(A+B+C) *x* => exactly one of A, B,C is '1'

Logic minimization trick:
The *carry_out* signal is used to realize the function of signal *sum* in order to reduce the overall circuit size.

Today's logic synthesis tools (such as Design Compiler) incorporating some advanced algorithms, is able to perform automatic logic minimization.

Initial Layout



Ratio of channel widths 2:1

- Post-layout SPICE simulation
  - includes the "parasitic resistance & capacitance"

Design Actions

- **Synthesis:** increasing information about the design by providing more detail (e.g., logic synthesis, physical synthesis).
- **Analysis:** collecting information on the quality of the design (e.g., timing analysis).
- **Verification:** checking whether a synthesis step has left the specification intact (e.g., layout verification).
- **Testing:** checking whether a fabricated chip has left all functions intact

Design Actions

- **Optimization:** increasing the quality of the design by rearrangements in a given description (e.g., logic optimizer, timing optimizer).
- **Design Management:** storage of design data, cooperation between tools, design flow, etc. (e.g., database).

Design Issues and Tools

- System-level design
  - Partitioning into hardware and software, co-design, co-simulation, etc.
  - Cost estimation, design-space exploration
- Algorithmic-level design
  - Behavioral descriptions (e.g. in Verilog, VHDL)
  - High-level simulation
- From algorithms to hardware modules
  - High-level (or architectural) synthesis
- Logic design:
  - Schematic entry
  - Register-transfer level and logic synthesis
  - Gate-level simulation (functionality, power, etc)
  - Timing analysis
  - Formal verification

high level

所有可能實現的方法，找到一個cost fuction的搜尋

Design Issues and Tools

- Transistor-level design
  - Switch-level simulation
  - Circuit simulation
- Physical (layout) design:
  - Partitioning 切小塊
  - Floorplanning and Placement
  - Routing 空間分配 連接線
  - Compaction 看能不能壓縮
  - Layout editing
  - Design-rule checking 檢查規則
  - Layout extraction
- Design management
  - Data bases, frameworks, etc.
- Silicon compilation: *from algorithm to mask patterns*
  - The *idea* is approached more and more, but still far away from a single *push-button* operation

Summary

- VLSI design flow
  - Spec.->Function->Logic->Circuit(transistor)->Layout
- VLSI design style
  - Full Custom, Cell-based, FPGA
- Design consideration
  - PPA
- Design issues and related tools

Q&A

Andy, Yu-Guang Chen
Associate Professor, Department of EE, NCU
Email: andyygchen@ee.ncu.edu.tw
FB: Yu-Guang Chen
IG: ncu.eda.andy
Google account: andyygchen.ncu