CS3120
Introduction of Integrated Circuit Design

Chap 7
Electronic Analysis of CMOS Logic Gates

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Outline

- 7.1 DC Characteristics of the CMOS Inverter
- 7.2 Inverter Switching Characteristics
- 7.3 Power Dissipation
- 7.4 DC Characteristics: NAND and NOR Gates
- 7.5 NAND and NOR Transient Response
- 7.6 Analysis of Complex Logic Gates
- 7.7 Gate Design for Transient Performance
- 7.8 Transmission Gates and Pass Transistors

Key Ideas

- In the previous chapter we examined the electrical characteristics of MOSFETs
- This sets the foundation for analyzing the behavior of transistors in CMOS logic circuits in this chapter
- The treatment centers on the important areas of switching speed and layout design, and provides the foundation for much of modern chip design

7.1 DC Characteristics of CMOS INV

- The CMOS inverter gives the basis for calculating the electrical characteristics of logic gates

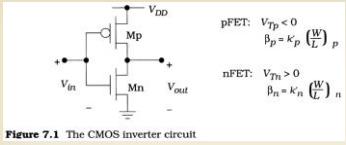


Figure 7.1 The CMOS inverter circuit

- Two types of calculations
  - DC analysis
    - determines V_{out} for a given value of V_{in}
    - Assume V_{in} changes slowly and V_{out} is allowed to stabilize before measurement
    - provides a direct mapping of the input to the output
    - tells us the voltage ranges that define Boolean logic 0 and logic 1 values
  - transient analysis
    - the input voltage is an explicit function of time $V_{in}(t)$
    - the response of the circuit is contained in $V_{out}(t)$
    - the delay between change in the input and the corresponding change at the output **fundamental limiting factor for high-speed design**
- In this section we concentrate on the DC analysis

7.1 DC Characteristics of CMOS INV

- Voltage Transfer Characteristic (VTC)
- VTC is a plot of V_{out} as a function of V_{in}
- Voltage
  - Output high voltage $V_{OH} = V_{DD}$
  - Output low voltage $V_{OL} = 0V$
- Logic switching
  - $V_L = V_{OH} - V_{OL} = V_{DD}$
  - Full-rail output

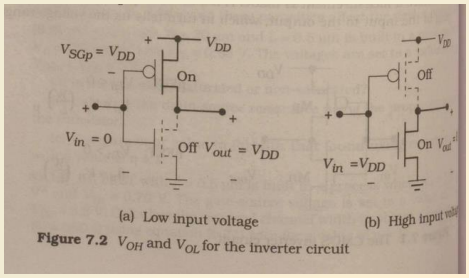


Figure 7.2 V_{OH} and V_{OL} for the inverter circuit

7.1 DC Characteristics of CMOS INV

- Voltages
  - $V_{GSn} = V_{in}$
  - $V_{SGp} = V_{DD} - V_{in}$
- Increasing V_{in}
  - downward transition in the VIC
  - turns the nFET on and the pFET is still conducting
  - Mp goes into cutoff when $V_{in} = V_{DD} - |V_{Tp}|$

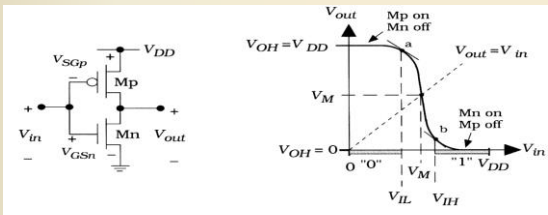


Figure 7.3 Voltage transfer curve for the NOT gate

7.1 DC Characteristics of CMOS INV

- The logic 0 and 1 voltage ranges are defined by the changing slope of the VTC
- Looking for slope = -1
  - Point *a* : input low voltage V_{IL}
  - Logic input 0 is defined as $0 \le V_{in} \le V_{IL}$
  - Point *b* : input high voltage V_{IH}
  - Logic input 1 is defined as $V_{IH} \le V_{in} \le V_{DD}$
- Voltage noise margin
  - Give a quantitative measure
  - High state: $VNM_H = V_{OH} - V_{IH}$
  - Low state: $VNM_L = V_{IL} - V_{OL}$
  - Midpoint voltage
    - $V_M = V_{in} = V_{out}$
    - $I_{Dn} = I_{Dp}$
  - transition region does not represent a Boolean quantity

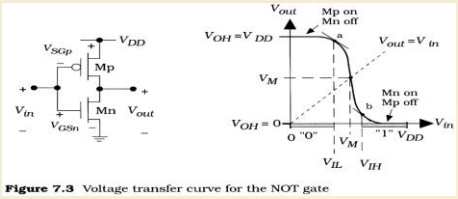


Figure 7.3 Voltage transfer curve for the NOT gate

7.1 DC Characteristics of CMOS INV

- We need to find the operating region (saturation or non-saturation) each FET before we can use the expression
- Saturation of nFET
  - $V_{sat} = V_{GSn} - V_{Tn} = V_M - V_{Tn}$ (where $V_{in} = V_{GSn} = V_M$)
  - $V_{DSn} = V_{out} = V_M$
  - $V_{DSn} > V_{sat} = V_M - V_{Tn}$ ➔ Saturated
- Current calculation
  - $I_{Dn} = \frac{\beta_n}{2}(V_M - V_{Tn})^2 = \frac{\beta_p}{2}(V_{DD} - V_M - |V_{TP}|)^2 = I_{Dp}$
  - $\sqrt{\frac{\beta_n}{\beta_p}}(V_M - V_{Tn}) = V_{DD} - V_M - |V_{TP}|$
  - $V_M = \frac{V_{DD} - |V_{TP}| + \sqrt{\frac{\beta_n}{\beta_p}} V_{Tn}}{1 + \sqrt{\frac{\beta_n}{\beta_p}}}$
- V_M is set by nFET-to-pFET ratio
  - $\frac{\beta_n}{\beta_p} = \frac{k'_n \left(\frac{W}{L}\right)_n}{k'_p \left(\frac{W}{L}\right)_p}$
  - Mobility ratio $\frac{k'_n}{k'_p} = \frac{\mu_n}{\mu_p} = r(\approx 2 \text{ to } 3)$

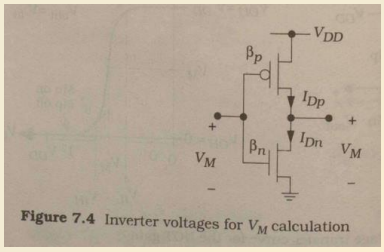


Figure 7.4 Inverter voltages for V_M calculation

7.1 DC Characteristics of CMOS INV

- Symmetric interval
  - Equal '0' and '1' input voltage range
  - By choosing $V_M = \frac{1}{2}V_{DD}$
  - Requires $\beta_n = \beta_p$
- Design equation
  - $I_{Dn} = \frac{\beta_n}{2}(V_M - V_{Tn})^2 = \frac{\beta_p}{2}(V_{DD} - V_M - |V_{TP}|)^2 = I_{Dp}$
  - $\frac{\beta_n}{\beta_p} = \left(\frac{\frac{1}{2}V_{DD} - |V_{Tp}|}{\frac{1}{2}V_{DD} - V_{Tn}}\right)^2$
- PMOS size has 2 to 3 times NMOS size
- The choice of transistor size for a particular V_M

Example 7.1

- Consider a CMOS process with the following parameters
  - K'_n = 140μA/V^2 V_{Tn} = 0.7,
  - K'_p = 60 μA/V^2 V_{Tp} = -0.7V
  - V_{dd}= 3.0 V
- Consider the case where $\beta_n = \beta_p$
- A symmetrical design by calculating
  - $V_M = \frac{1}{2}V_{DD} = 1.5V = \frac{3-0.7+\sqrt{1}(0.7)}{1+\sqrt{1}}$
  - $\frac{\beta_n}{\beta_p} = \frac{k'_n\left(\frac{W}{L}\right)_n}{k'_p\left(\frac{W}{L}\right)_p} = 1$
  - $\left(\frac{W}{L}\right)_p = \frac{k'_n}{k'_p}\left(\frac{W}{L}\right)_n = \left(\frac{140}{60}\right)\left(\frac{W}{L}\right)_n = 2.33\left(\frac{W}{L}\right)_n$
- If $\left(\frac{W}{L}\right)_p = \left(\frac{W}{L}\right)_n$
  - $V_M = \frac{3-0.7+\sqrt{2.33}(0.7)}{1+\sqrt{2.33}} = 1.33V$

7.1 DC Characteristics of CMOS INV

- Figure 7.5 illustrates the difference that uses the two design styles

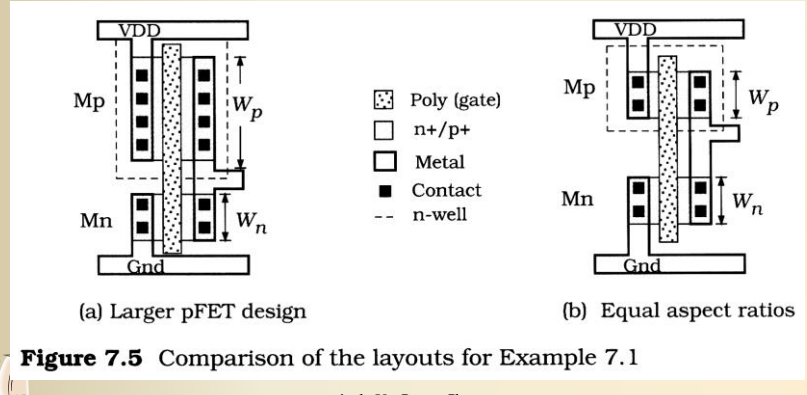


Figure 7.5 Comparison of the layouts for Example 7.1

7.1 DC Characteristics of CMOS INV

- At physical level, the relative device sizes contained in the ratio ($\frac{\beta_n}{\beta_p}$) determine the switching point
- ($\frac{\beta_n}{\beta_p}$) decrease ➔ V_M increases

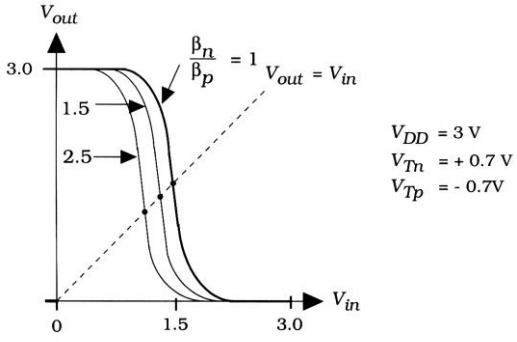


Figure 7.6 Dependence of V_M on the device ratio

7.2 INV Switching Characteristics

- High speed digital system design is based on the ability to perform calculation very quickly
  - Logic gates introduce a minimum amount of time delay when input changes
  - Designing fast logic circuit is a more challenging (but critical) aspect of VLSI design
- Rise and fall time delays
  - Due to the parasitic resistance and capacitances

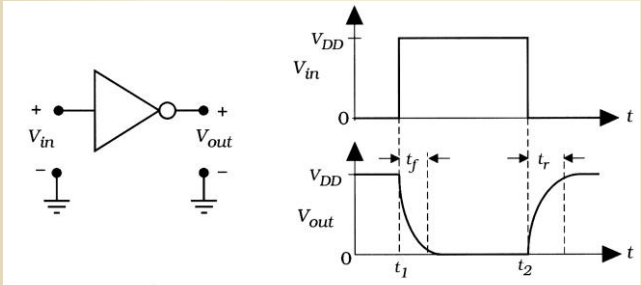


Figure 7.7 General switching waveforms

7.2 INV Switching Characteristics

- A simplified RC model in Fig 7.8b
  - $R_n = \frac{1}{\beta_n(V_{DD}-V_{Tn})}$
  - $R_p = \frac{1}{\beta_p(V_{DD}-|V_{Tp}|)}$
  - $C_{Dn} = C_{GSn} + C_{DBn} = \frac{1}{2} C_{ox} L' W_n + C_{jn} A_n + C_{jswn} P_n$
  - $C_{Dp} = C_{GSp} + C_{DBp} = \frac{1}{2} C_{ox} L' W_p + C_{jp} A_p + C_{jswp} P_p$
- Increase channel width of a FET increases the parasitic capacitance values

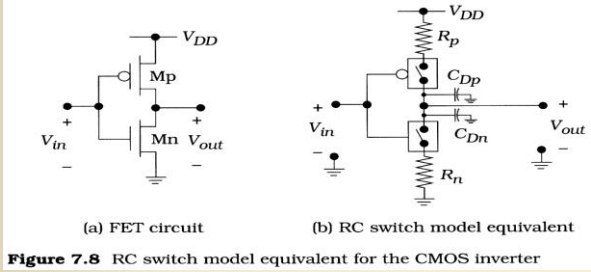


Figure 7.8 RC switch model equivalent for the CMOS inverter

7.2 INV Switching Characteristics

- In a logic chain, every logic gate must drive another gate, or set of gates, to be useful
- Fan-out (FO) gates act as load to the driving circuits because of their input capacitance C_{in}
  - $C_{in} = C_{GP} + C_{Gn}$
- External load capacitance
  - FO = 3
  - $C_L = 3C_{in} = 3 * (C_{Gp} + C_{Gn})$

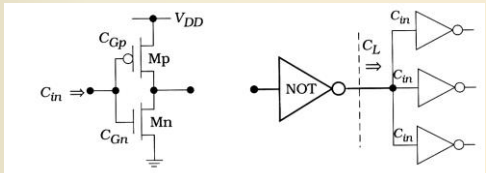


Figure 7.9 Input capacitance and load effects

7.2 INV Switching Characteristics

- We may now calculate the switching times of the inverter
- A CMOS NOT gate is used to drive an external load capacity C_L
  - $C_{out} = C_{FET} + C_L$
  - $C_{FET} = C_{Dn} + C_{Dp}$
  - C_{out} is the load the gate must drive

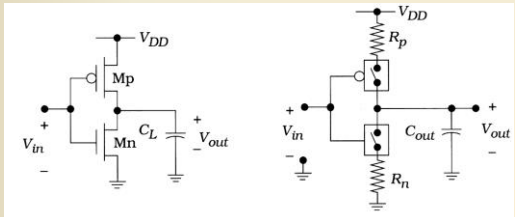


Figure 7.10 Evolution of the inverter switching model

Example 7.2

- Apply this analysis to find capacitances in the NOT gate

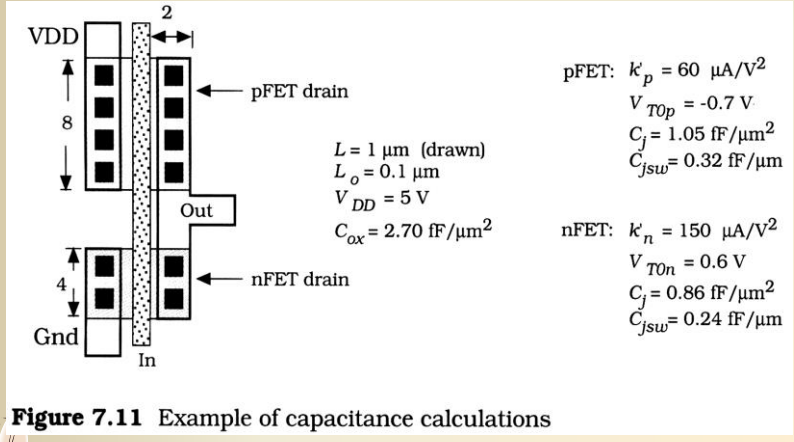


Figure 7.11 Example of capacitance calculations

Example 7.2

- $C_{Gn} = 2.7 * 1 * 4 = 10.8fF$
- $C_{GDn} = ½ * 10.8 = 5.04\ fF$
- $C_{DBn} = 0.86 * 4 * 2.1 + 0.24 * 2 * (4 + 2.1) = 10.15fF$
- $C_{Dn} = 5.04 + 10.15 = 15.55fF.$

- $C_{GP} = 2.7 * 1 * 8 = 21.6fF$
- $C_{GDP} = ½ * 21.6 = 10.8\ fF$
- $C_{DBP} = 1.05 * 8 * 2.1 + 0.32 * 2 * (8 + 2.1) = 24.10fF$
- $C_{DP} = 10.8 + 24.1 = 34.9fF.$

- $C_{FET} = C_{Dp} + C_{Dn} = 15.55 + 34.9 = 50.45fF$
- $C_{out} = 50.45 + C_L$

7.2.1 Fall time Calculation

- Calculating output fall time t_f
  - V_{in} changes from 0 to V_{DD}
  - The nFET switch is closed and the pFET switch is open

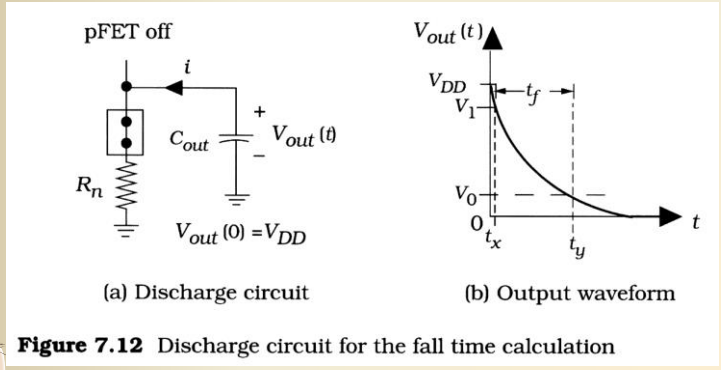


Figure 7.12 Discharge circuit for the fall time calculation

7.2.1 Fall time Calculation

- The capacitor C_{out} is initially charged to V_{DD} and is discharged to 0 V.
- The fall time is traditionally defined to be the time interval
  - $V_1 = 0.9V_{DD}$ *to* $V_0 = 0.1V_{DD}$
- Fall time calculation
  - $I = -C_{out}(dV_{out}/dt) = V_{out}/R_n$ (The current leaving the capacitor)
  - $V_{out}(t) = V_{DD}e^{-t/\tau_n}$ (initial condition $V_{out}(0) = VDD$)
  - time constant $\tau_n = R_nC_{out}$
  - $t = \tau_n \ln\left(\frac{V_{DD}}{V_{out}}\right)$
  - $t_f = t_y - t_x = \tau_n \ln\left(\frac{V_{DD}}{0.1V_{DD}}\right) - \tau_n \ln\left(\frac{V_{DD}}{0.9V_{DD}}\right) = \tau_n \ln(9)$
    - $\ln(a) - \ln(b) = \ln(\frac{a}{b})$
  - $t_f = t_{HL} = \ln(9)\,\tau_n \approx 2.2\tau_n = 2.2R_nC_{out}$
    - t_{HL}: high-to-low time

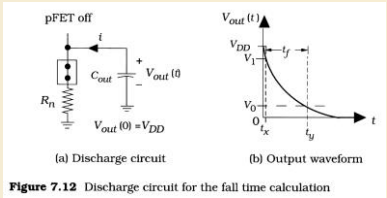


Figure 7.12 Discharge circuit for the fall time calculation

7.2.2 Rise Time Calculation

- Calculating output rising time t_r
  - V_{in} changes from V_{DD} to 0
  - The pFET switch is closed and the nFET switch is open

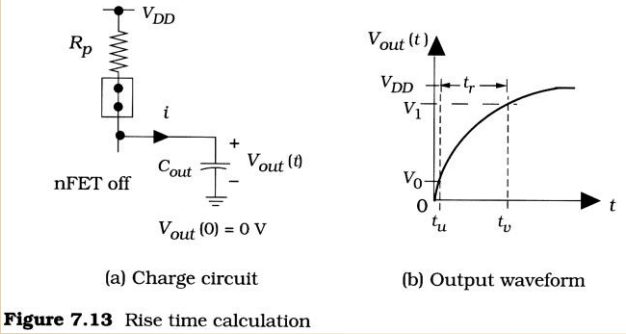


Figure 7.13 Rise time calculation

7.2.2 rise time Calculation

- The capacitor C_{out} is initially 0 V and is charged to V_{DD}
- The rise time is traditionally defined to be the time interval
  - $V_0 = 0.1V_{DD}$ to $V_1 = 0.9V_{DD}$
- Fall time calculation
  - $I = C_{out}\left(\frac{dV_{out}}{dt}\right) = (V_{DD} - V_{out})/Rp$ (The current going into the capacitor)
  - $V_{out}(t) = V_{DD}[1 - e^{-t/\tau_p}]$ (initial condition $V_{out}(0) = 0V$)
  - time constant $\tau_p = R_p C_{out}$
  - $t_r = t_v - t_u = \tau_p \ln(9)$
  - $t_r = t_{LH} = \ln(9)\,\tau_p \approx 2.2\tau_p = 2.2R_pC_{out}$
    - t_{HL}: low-to-high time
- Maximum signal frequency
  - $F_{max} = 1/(tr + tf)$

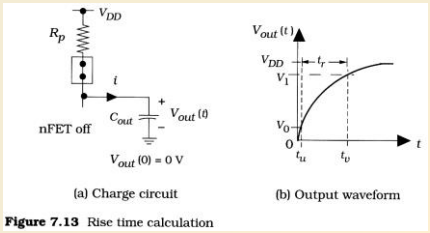


Figure 7.13 Rise time calculation

Example 7.3

- Consider an inverter circuit that has FET aspect ratios
  - $\left(\frac{W}{L}\right)_n$=6, $\left(\frac{W}{L}\right)_p$=8
- Process
  - $k'_n = 150\ {}^{\mu A}/_{V^2}, V_{Tn} = +0.70\ V$
  - $k'_p = 62\ {}^{\mu A}/_{V^2}, V_{Tp} = -0.85\ V$
  - $V_{DD} = 3.3V$
  - C_{out} = $150fF$
- Compute the rise and fall time
  - R_p =1/[(62*10^{-6})(8)(3.3-0.85)]= 822.9Ω
  - τ_p = 822.9*150*10^{-15} = 123.43ps
  - t_r = 2.2 τ_p = 271.55ps
  - R_n= 427.35 Ω
  - τ_n= 64.1 ps
  - t_f=2.2 τ_n=141.0ps
- Compute maximum signal frequency
  - $f_{max} = \frac{1}{t_r + t_f} = \frac{1}{(271.55+141.0)\times 10^{-12}} = 2.45\ GHz$

7.2.3 Propagation Delay

- The propagation delay is use to estimate the reaction delay time from input to output
  - $t_p = \frac{(t_{pf}+t_{pr})}{2}$
  - T_{pf} is the output fall time from the maximum level to the 50% voltage line ($\frac{V_{DD}}{2}$)
  - T_{pr} is is the output rise time from the 0V to the 50% voltage line ($\frac{V_{DD}}{2}$)
  - Using the exponential equations for V_{out}
    - $t_{pf} = \ln(2)\,\tau_n$
    - $t_{pr} = \ln(2)\,\tau_p$
    - $\ln(2) \approx 0.693$
    - $t_p \approx 0.35(\tau_n + \tau_p)$

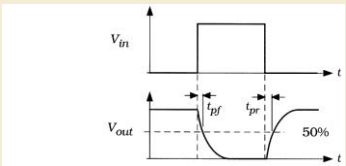
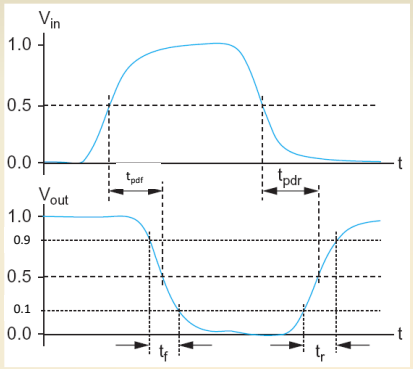


Figure 7.14 Propagation time definitions

- Propagation delay are commonly used in basic logic simulation
  - Not provide details on rise and fall time

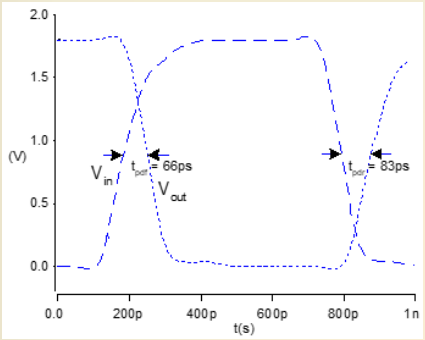
Delay Definitions

- t_{pdr}: *rising propagation delay*
  - From input to rising output crossing $V_{DD}/2$
- t_{pdf}: *falling propagation delay*
  - From input to falling output crossing $V_{DD}/2$
- t_{pd}: *average propagation delay*
  - $t_{pd} = (t_{pdr} + t_{pdf})/2$
- t_r: *rise time*
  - From output crossing 0.1 V_{DD} to 0.9 V_{DD}
- t_f: *fall time*
  - From output crossing 0.9 V_{DD} to 0.1 V_{DD}



Simulated Inverter Delay

- Solving differential equations by hand is too hard
- SPICE simulator solves the equations numerically
  - Uses more accurate I-V models too!
- But simulations take time to run, may hide insight



7.2.4 General Analysis

- We should know how to design single logic gates and then characterize the behavior of the gates when they are cascaded
- Total output capacitance
  - $C_{out} = C_{FET} + C_L$
  - The layout geometry establishes the value of C_{FET}
  - C_L varies with the application
- Rise and fall time
  - $t_r \approx 2.2R_p(C_{FET} + C_L) = tr_0 + \alpha_p C_L$
  - $t_f = 2.2R_n(C_{FET} + C_L) = tf_0 + \alpha_n C_L$
  - Rise and fall time are linear functions of C_L
    - $\alpha_p = 2.2R_p = \frac{2.2}{\beta_p(V_{DD} - |V_{Tp}|)}$
    - $\alpha_n = 2.2R_n = \frac{2.2}{\beta_p(V_{DD} - V_{Tn})}$
    - Inversely proportional to the aspect ratios
  - Under zero-load condition ($C_L = 0$)
    - $t_r = t_{r0} \approx 2.2R_pC_{FET}$
    - $t_f = tr_0 \approx 2.2R_nC_{FET}$

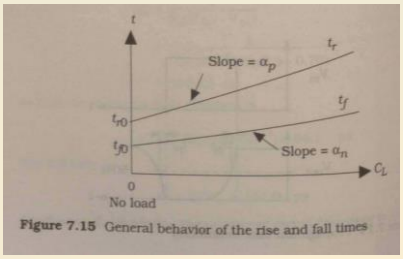


Figure 7.15 General behavior of the rise and fall times

- Large capacitive loads may cause problems because of longer delays
- t_r and t_f can be reduced by using large FETs

Example 7.4

- Use the results of Example 7.3 to find the general delay equations when $C_{FET} = 80fF$
- t_r is controlled by the pFET
  - $R_p = 822.9\Omega$
  - $\alpha_p = 2.2R_p = 1810.4\Omega$
  - $t_{r0} = 2.2R_pC_{FET} = 2.2(822.9)(80 \times 10^{-15}) = 144.9\ ps$
  - $t_r = t_{r0} + \alpha_p C_L = 144.9 + 1.810C_L\ ps$
- t_f is controlled by the nFET
  - $R_n = 427.35\Omega$
  - $\alpha_n = 2.2R_p = 940.2\Omega$
  - $t_{f0} = 2.2R_nC_{FET} = 2.2(940.2)(80 \times 10^{-15}) = 165.5\ ps$
  - $t_f = t_{f0} + \alpha_n C_L = 165.5 + 0.940C_L\ ps$
- Assume $C_L = 150\ fF$
  - $t_r = 144.9 + 1.810(150) = 416.4\ ps$
  - $t_f = 165.5 + 0.940(150) = 306.5\ ps$
  - Maximum signal frequency $= f_{max} = \frac{1}{t_r + t_f} = 1.38GHz$

7.2.5 Summary of Inverter

- Electrical characteristic are established by
  - The processing variables: k', V_T, and parasitic capacitances
  - The transistor aspect rations $\left(\frac{W}{L}\right)_n$ and $\left(\frac{W}{L}\right)_p$
- VLSI designers do not have control over processing parameters
- Device sizing becomes the critical issue

7.3 Power Dissipation

- The current I_{DD} flowing from power supply to ground gives a dissipated power $P = V_{DD}I_{DD}$
- Current can be divided into DC and dynamic (or switching) contributions $P = P_{DC} + P_{dyn}$
- Ideally, the DC current is 0 when $V_{in} = 0$
  - Quiescent leakage current I_{DDQ}
  - DC power at stable 0 or 1 state
    - $P_{DC} = V_{DD}I_{DDQ}$

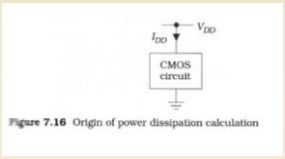


Figure 7.16 Origin of power dissipation calculation

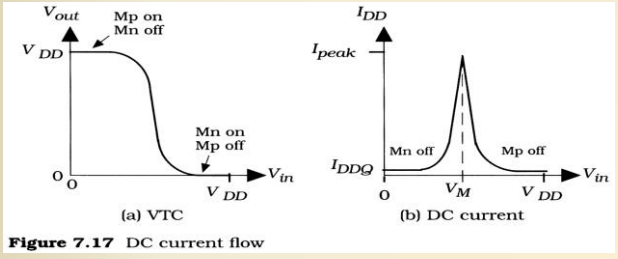


Figure 7.17 DC current flow

7.3 Power Dissipation

- Dynamic power dissipation
  - A complete cycle effectively creates a path for current to flow from the power supply to ground
  - Discharge
    - $Q_e = C_{out}V_{DD}$
    - $P_{av} = V_{DD}I_{DD} = V_{DD}\left(\frac{Q_e}{T}\right)$: average power dissipated over a single cycle T
    - $P_{sw} = C_{out}V_{DD}^2 f$
    - The dynamic power is proportional to the signal frequency
- $P = P_{DC} + P_{dyn} = V_{DD}I_{DDQ} + C_{out}V_{DD}^2 f$

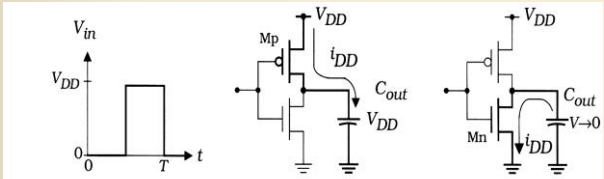


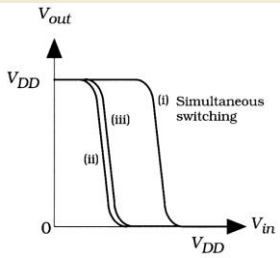
Figure 7.18 Circuit for finding the transient power dissipation

7.4 DC Characteristics: NAND and NOR
7.4.1 NAND Analysis

- In this section we will examine the relationship between device sizes and transitions described by the VTC
- NAND2
  - Like-polarity FETs have the same aspect ratio: $\beta_n and\ \beta_p$

	V_A	V_B	V_{out}
(i)	0	0	V_{DD}
(ii)	0	V_{DD}	V_{DD}
(iii)	V_{DD}	0	V_{DD}
	V_{DD}	V_{DD}	0

(a) Transition table



(b) VTC family

Figure 7.20 NAND2 VTC analysis

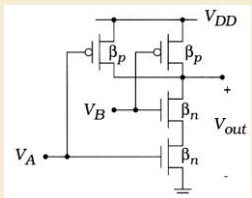


Figure 7.19 NAND2 logic circuit

7.4.1 NAND Analysis

- Calculate the value of midpoint voltage V_M for the case of simultaneous switching

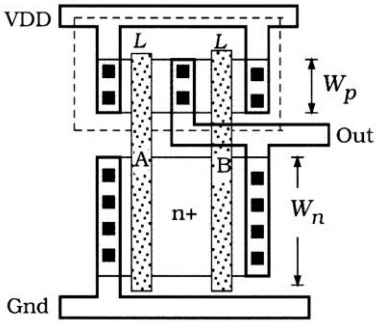


Figure 7.21 Layout of NAND2 for V_M calculation

7.4.1 NAND Analysis

- "Merge" the two gates together into one
- nFET
  - The structure can be approximated as a single nFET with an aspect ratio of $(\frac{W_n}{2L})$
    - single equivalent transistor is described by the value $\frac{\beta_n}{2}$
- pFET
  - The structure can be simplified into the single gate with an aspect ratio of $(\frac{2W_p}{L})$
    - single equivalent transistor is described by the value $2\beta_p$

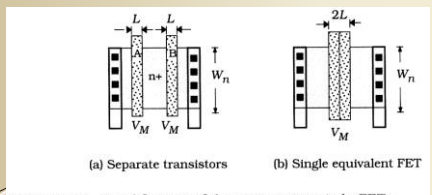


Figure 7.22 Simplification of the series-connected nFETs

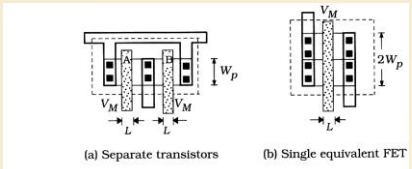


Figure 7.23 Simplification of parallel-connected pFETs

7.4.1 NAND Analysis

- Find V_M
  - Replacing the transistor pairs by their single-FET
  - Recall: $I_{Dn} = \frac{\beta_n}{2}(V_M - V_{Tn})^2 = \frac{\beta_p}{2}(V_{DD} - V_M - |V_{TP}|)^2 = I_{Dp}$
  - $\frac{\beta_n/2}{2}(V_M - V_{Tn})^2 = \frac{2\beta_p}{2}(V_{DD} - V_M - |V_{TP}|)^2$
  - $V_M = \frac{V_{DD} - |V_{TP}| + \frac{1}{2}\sqrt{\frac{\beta_n}{\beta_p}}V_{Tn}}{1 + \frac{1}{2}\sqrt{\frac{\beta_n}{\beta_p}}}$
  - The $\frac{1}{2}$ reduces the denominator, which is why the VTC curveis shifted toward the right
- For N-input NAND gate
  - $V_M = \frac{V_{DD} - |V_{TP}| + \frac{1}{N}\sqrt{\frac{\beta_n}{\beta_p}}V_{Tn}}{1 + \frac{1}{N}\sqrt{\frac{\beta_n}{\beta_p}}}$

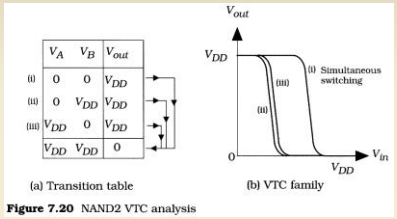


Figure 7.20 NAND2 VTC analysis

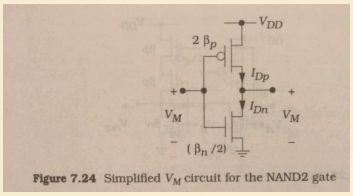


Figure 7.24 Simplified V_M circuit for the NAND2 gate

7.4.2 NOR Analysis

- The NOR2 gate can be analyzed using the same techniques
  - $V_{out} = V_{DD}$ requires $V_A = V_B = 0$
  - nFET are in parallel: $2\beta_n$
  - pFET are in serial: $\frac{\beta_p}{2}$
  - $\frac{2\beta_n}{2}(V_M - V_{Tn})^2 = \frac{(\beta_p/2)}{2}(V_{DD} - V_M - |V_{TP}|)^2$
  - $V_M = \frac{V_{DD} - |V_{TP}| + 2\sqrt{\frac{\beta_n}{\beta_p}}V_{Tn}}{1 + 2\sqrt{\frac{\beta_n}{\beta_p}}}$

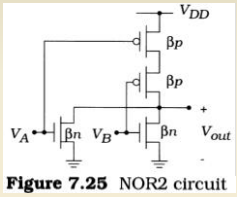


Figure 7.25 NOR2 circuit

- the NAND and NORgates tend have opposite behaviors with respect to the reference NOT gate VTC

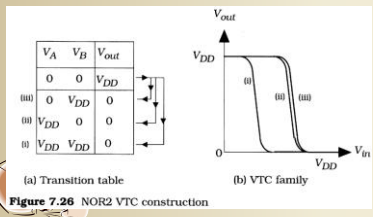


Figure 7.26 NOR2 VTC construction

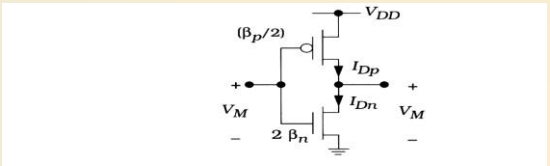


Figure 7.27 NOR2 V_M calculation for simultaneous switching

7.4 DC Characteristics: NAND and NOR

- Both the NAND and NOR gates exhibit low DC power dissipation values
  - $P_{DC} = V_{DD} I_{DDQ}$
  - No direct current flow path from the power supply to ground when the inputs are stable logic 0 or logic 1 values
- Dynamic power is still present in the general form
  - $P_{sw} = C_{out} V_{DD}^2 f_{gate}$
  - f_{gate} is different from the basic Switching frequency used for the inverter

7.5 NAND and NOR Transient Response

- Transient switching times often represent the limiting factor in designing a digital logic chain
- Examine how the FET topology and device sizing affect the operational speed of the gate

7.5.1 NAND2 Switching Times

- The transient calculations are based on finding RC time constants
- We will concentrate estimating the worst-case values of the switching times
  - $C_{out} = C_{FET} + C_L$
  - $C_{FET} = C_{Dn} + 2C_{Dp}$
    - two pFETs are connected to the output node
  - The drawing identifies the transistors by their resistance values
    - $R_n = \frac{1}{\beta_n(V_{DD} - V_{Tn})}$
    - $R_p = \frac{1}{\beta_p(V_{DD} - |V_{Tp}|)}$

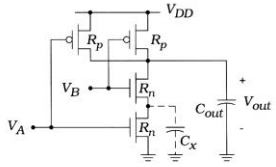


Figure 7.28 NAND2 circuit for transient calculations

7.5.1 NAND2 Switching Times

- Rising time t_r
  - If only one pFET is conducting
  - C_{out} charges through a pFET resistance R_p
  - $V_{out(t)} = V_{DD}[1 - e^{-t/\tau_p}]$ (initial condition $V_{out}(0) = 0V$)
  - $t_r = 2.2\tau_p = 2.2R_pC_{out} = t_0 + \alpha_0 C_L$
  - $t_0 = 2.2R_pC_{FET}$: zero-load value
  - $\alpha_0 = 2.2R_p$: slope of t_r
  - Best case: both pFET are conducting
    - $R_p/2$

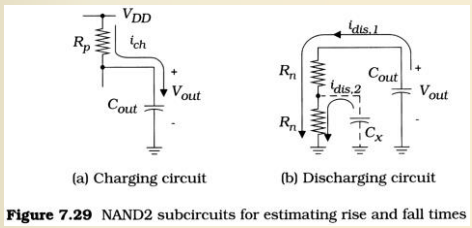


Figure 7.29 NAND2 subcircuits for estimating rise and fall times

7.5.1 NAND2 Switching Times

- Fall time t_f
  - C_{out} discharges through the series-connected nFET chain
  - RC modeling of each device leads to the "ladder" network
  - Consider the presence of the inter-FET capacitance C_x
  - In worst case, C_x will have charge that will flow through lower nFET (MnA)to ground
    - The discharge rate is limited by the current that MnA can maintain
  - $V_{out}(t) = V_{DD}e^{-t/\tau_n}$
  - Time constant is given by the Elmore formula
    - $\tau_n = \tau_{n1} + \tau_{n2} = C_{out}(R_n + R_n) + C_x R_n$
  - $t_f = 2.2\tau_n = 2.2[(C_{FET} + C_L)(2R_n) + C_x R_n]$
  - $t_f = t_1 + \alpha_1 C_L$
  - $t_1 = 2.2R_n(2C_{FET} + C_x)$: zero-load value
  - $\alpha_1 = 4.4R_n$: slope of t_f

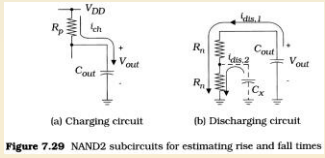


Figure 7.29 NAND2 subcircuits for estimating rise and fall times

- Series-connected FETs lead to longer delays in CMOS circuits
  - $\tau_n = R_n(2C_{out} + C_x)$
  - $C_{eff} = 2C_{out} + C_x$

7.5.2 NOR2 Switching Times

- The analysis of the NOR2 transients proceeds in the same manner
- We will concentrate estimating the worst-case values of the switching times
  - $C_{out} = C_{FET} + C_L$
  - $C_{FET} = 2C_{Dn} + C_{Dp}$
    - two nFETs are connected to the output node
  - The drawing identifies the transistors by their resistance values
    - $R_n = \frac{1}{\beta_n(V_{DD} - V_{Tn})}$
    - $R_p = \frac{1}{\beta_p(V_{DD} - |V_{Tp}|)}$

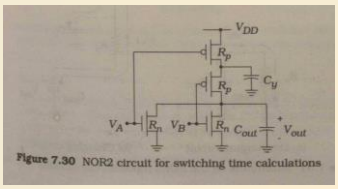


Figure 7.30 NOR2 circuit for switching time calculations

7.5.2 NOR2 Switching Times

- Fall time t_f
  - If only one nFET is conducting
  - C_{out} discharges through a nFET resistance R_n
  - $V_{out}(t) = V_{DD}e^{-t/\tau_n}$ (initial condition $V_{out}(0) = VDD$)
  - $t_f = 2.2\tau_n = 2.2R_nC_{out} = t_1 + \alpha_1 C_L$
  - $t_1 = 2.2R_nC_{FET}$: zero-load value
  - $\alpha_1 = 2.2R_p$: slope of t_f

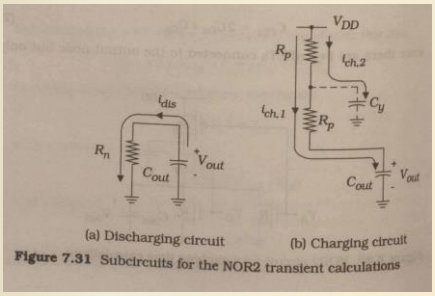
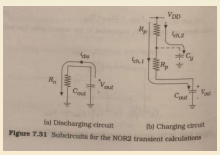


Figure 7.31 Subcircuits for the NOR2 transient calculations

7.5.2 NOR2 Switching Times

- Rising time t_r
  - C_{out} charges through the series-connected pFET chain
  - RC modeling of each device leads to the "ladder" network
  - Consider the presence of the inter-FET capacitance C_y
  - C_y will be charged during rising event
  - $V_{out(t)} = V_{DD}[1 - e^{-t/\tau_p}]$ (initial condition $V_{out}(0) = 0V$)
  - Time constant is given by the Elmore formula
    - $\tau_p = \tau_{p1} + \tau_{p2} = C_{out}\left(R_p + R_p\right) + C_yR_p$
  - $t_r = 2.2\tau_p = 2.2[(C_{FET} + C_L)(2R_p) + C_yR_p]$
  - $t_r = t_0 + \alpha_0 C_L$
  - $t_0 = 2.2R_p(2C_{FET} + C_y)$: zero-load value
  - $\alpha_0 = 4.4R_p$: slope of t_r

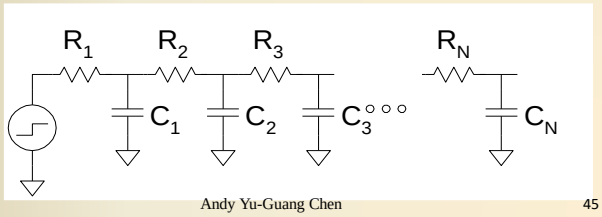


- Series-connected FETs lead to longer delays in CMOS circuits
  - $\tau_n = R_n(2C_{out} + C_x)$
  - $C_{eff} = 2C_{out} + C_x$

Elmore Delay

- ON transistors look like resistors
- Pullup or pulldown network modeled as *RC ladder*
- Elmore delay of RC ladder

$$t_{pd} \approx \sum_{\text{nodes } i} R_{i-to-source} C_i$$
$$= R_1 C_1 + (R_1 + R_2) C_2 + \ldots + (R_1 + R_2 + \ldots + R_N) C_N$$



7.5.3 Summary

- The analyses above illustrate that the NAND and NOR gates exhibit complementary characteristics at both the DC and transient levels
- General statements about NAND and NOR gates as compared to the simpler NOT circuit
  - Rise time
    - $t_r = t_0 + \alpha_0 C_L$
  - Fall time
    - $t_f = t_1 + \alpha_1 C_L$
  - The constant depend upon the parasitic transistor resistances and capacitances
  - Adding complementary transistor pairs increases the delay time because C_{FET} is increased
- Switching delay increase with the # of fan-Ins (FIs)
- Switching delay increase with the external load

7.6 Analysis of Complex Gates

- The analysis techniques developed for the NAND and NOT circuits may be extended to analyze complex CMOS logic gates with AOI and OAl structure
  - series-connected FETs
- Consider the function $f = \overline{x \cdot (y + z)}$

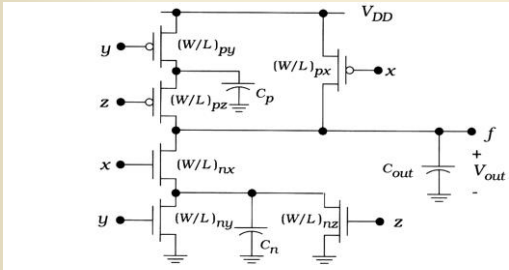


Figure 7.32 Complex logic gate circuit

7.6 Analysis of Complex Gates

- Fall time analysis
  - Assume they are all the same size $\left(\frac{W}{L}\right)_{nx} = \left(\frac{W}{L}\right)_{ny} = \left(\frac{W}{L}\right)_{nz}$
  - Resistance: R_n can be used
  - Worst case fall time: x = 1, but only one of the ORed inputs y or z is 1
    - 2-FET series pair
    - $C_{out} = C_{FET} + C_L$
    - $\tau_n = R_n C_n + 2R_n C_{out}$
    - $t_f = 2.2\tau_n = 2.2R_n[C_n + 2(C_{FET} + C_L)] = t_1 + \alpha_1 C_L$
    - Zero load time: $t_1 = 2.2R_n(C_n + 2C_{FET})$
    - Slop: $\alpha_1 = 2.2R_n$

7.6 Analysis of Complex Gates

- Rise time analysis
  - Assume they are all the same size $\left(\frac{W}{L}\right)_{px} = \left(\frac{W}{L}\right)_{py} = \left(\frac{W}{L}\right)_{pz}$
  - Resistance: R_p can be used
  - the limiting series chain is with the y and z input p-channel transistors
  - the x-input pFET provides the fast switching, and could be decreased to half-size without affecting the result
  - The series chain gives
    - $\tau_p = R_p C_p + 2R_p C_{out}$
    - $t_r = t_0 + \alpha_0 C_L$
    - Zero load time: $t_0 = 2.2R_p(C_p + 2C_{FET})$
    - Slop: $\alpha_0 = 2.2R_p$
- An arbitrary gate yields equations of the same form for both the rise fall times, illustrating the generality of the procedure

7.6.1 Power Dissipation

- Power is proportional to the **activity coefficient** α
  - which represents the probability that an output 0->1 transition takes places during one period.
  - $P = VddID_{DQ} + C_{out}V_{dd}{}^2 f$ (P_{dyn})
  - $P_{dyn} = \alpha C_{out} Vdd^2 f$
- For a network that consists of *N* gates, the total dynamic power is
  - $P_{dyn} = \sum_{i=1}^{N} \alpha_i C_i V_i V_{DD} f$
    - α_i: activity coefficient
    - C_i: node capacitance that charges to a maximum value of V_i.
- Activity coefficients can be determined from truth tables
  - $\alpha = p_0 p_1$
  - $\alpha_{NOR2} = 3/4 * 1/4 = 3/16$
  - $\alpha_{NAND2} = 3/4 * 1/4 = 3/16$
  - $\alpha_{NOR3} = 1/8 * 7/8 = 7/64$
  - $\alpha_{XOR2} = 1/2 * 1/2 = 1/4$

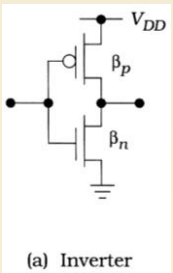
A	B	$\overline{A+B}$	$\overline{A \cdot B}$
0	0	1	1
0	1	0	1
1	0	0	1
1	1	0	0

7.7 Gate Design for Transient Performance

- High-speed circuits are limited by the switching time of individual gates
- The aspect ratios are the critical design parameters for the DC and transient switching times
- The DC switching characteristics are often considered less important than the switching speed
- The design philosophy used to select aspect ratios varies with situation
  - use the inverter as a reference and then attempt to design other gates that have approximately the same switching times

7.7 Gate Design for Transient Performance

- device transconductance as being equivalent to the aspect ratio
  - $\beta = k'\left(\frac{W}{L}\right)$
- In Fig 7.34(a)
  - both transistors drive the same capacitance, the difference is in the resistance values
  - $R_p = \frac{1}{\beta_p(V_{DD}-|V_{Tp}|)}$ $R_n = \frac{1}{\beta_n(V_{DD}-V_{Tn})}$
  - symmetrical inverter: $\beta_p = \beta_n$
  - requires the device sizes: $\left(\frac{W}{L}\right)_p = r\left(\frac{W}{L}\right)_n$
  - Process transconductance ratio: $r = \frac{k'_n}{k'_p}$



(a) Inverter

7.7 Gate Design for Transient Performance

- Find the device sizes β_P and β_N for the NAND2 gate with similar rise and fall times
  - rise time
    - worst situation is where only one transistor contributes to the rise time
    - $\beta_P = \beta_p$
  - fall time
    - series-connected nFET chain: two series-connected resistors between the output and ground
    - $R = R_N + R_N, R_N = \frac{1}{\beta_N(V_{DD}-V_{Tn})}$
    - using the inverter as a reference
      - $R = R_n = 2R_N$
      - $\frac{1}{\beta_n(V_{DD}-V_{Tn})} = \frac{2}{\beta_N(V_{DD}-V_{Tn})}$
      - $\beta_N = 2\beta_n$
    - the series-connected nFETs are twice as large as the inverter
      - $\left(\frac{W}{L}\right)_N = 2\left(\frac{W}{L}\right)_n$

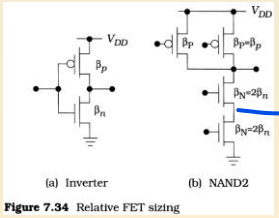
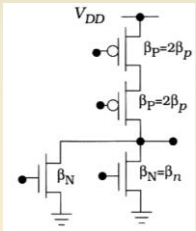


Figure 7.34 Relative FET sizing

  - The resulting fall time will be larger because of the larger output capacitance and the FET-FET internal capacitance

7.7 Gate Design for Transient Performance

- Find the device sizes β_P and β_N for the NOR2 gate with similar rise and fall times
- With the similar idea
  - fall time
    - $\beta_N = \beta_n$
  - rise time
    - $\frac{1}{\beta_p(V_{DD}-|V_{Tp}|)} = \frac{2}{\beta_P(V_{DD}-|V_{Tp}|)}$
    - $\beta_P = 2\beta_p$
    - $\left(\frac{W}{L}\right)_P = 2\left(\frac{W}{L}\right)_p$



7.7 Gate Design for Transient Performance

- This technique can be extended to larger chains.

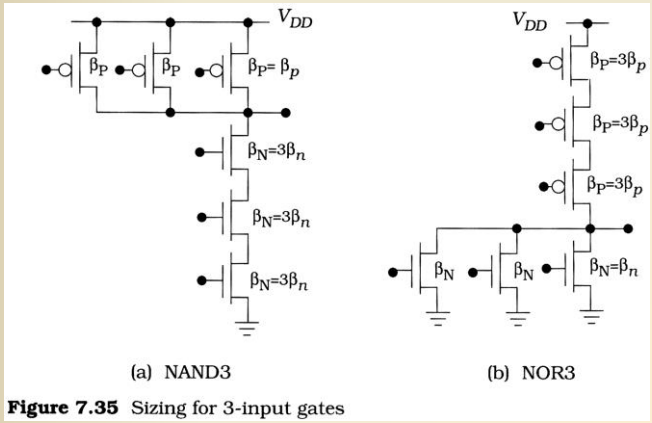


Figure 7.35 Sizing for 3-input gates

7.7 Gate Design for Transient Performance

- Complex logic gates can be designed in the same manner

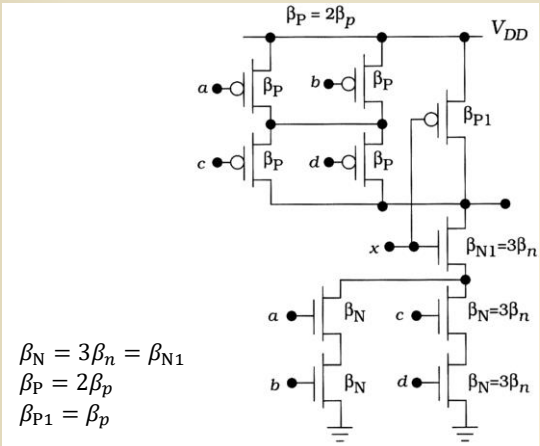


Figure 7.36 Sizing of a complex logic gate

7.8 Transmission Gates & Pass Transistor

- Transmission gates consist of an nFET/pFET pair wired in parallel

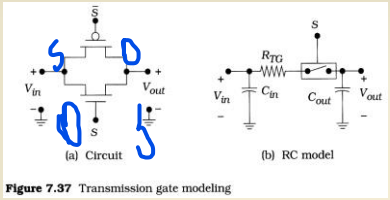


Figure 7.37 Transmission gate modeling

- Even though the FETs are in parallel, one usually dominates the conduction process at any given time
  - logic 0 transmission is controlled by the nFET
  - $R_{TG} = \max(R_n, R_p)$
  - $C_{in} = C_{S,n} + C_{D,p}$
- large values of (W/L) decrease the resistance, but a large W implies large capacitances

7.8 Transmission Gates & Pass Transistor

注重特定方向，另一方向不在乎，差距可達6倍

- **Pass transistors** are single FETs that pass the signal between the drain and source terminals instead of a fixed power supply value

$T_r = 18\,\tau_n$
$T_f = 2.94\,\tau_n$
$t_r = 6t_f$

$\tau_n = R_n C_{out}$

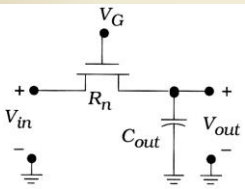


Figure 7.38 nFET pass transistor

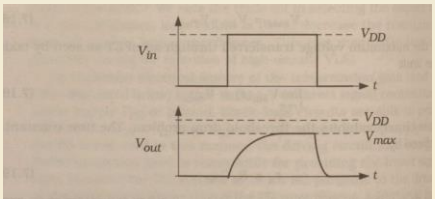


Figure 7.39 Voltage waveforms for a nFET pass transistor

Conclusions

- DC Characteristics of CMOS Inverters and Gates
- Switching Characteristics and Propagation Delay
- Power Dissipation
- Transient Response of NAND and NOR Gates
- Complex Gate Analysis and Design for Transient Performance
- Transmission Gates and Pass Transistors

Q&A

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