CS3120

Introduction of Integrated Circuit Design

Chap 6
Electrical Characteristics of MOSFETs

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Outline

- 6.1 MOS Physics
- 6.2 nFET Current-Voltage Equations
- 6.3 The FET RC Model
- 6.4 pFET Characteristics
- 6.5 Modeling of Small MOSFETs

Key Idea

- This chapter centers on MOSFET characteristics and initiates the "electronics" side of VLSI where electrical currents and voltages are the most important quantities
- The emphasis, however, is not on studying electronics for its own sake, but to emphasize the link between physical design and logic networks

6.1 MOS Physics

- MOSFETs conduct electrical current by using an applied voltage to move charge from the source side to the drain side of the device
- It is important to determine the current versus voltage (I-V) relation
  - $I_{Dn} = I_{Dn}(V_{GSn}, V_{DSn})$

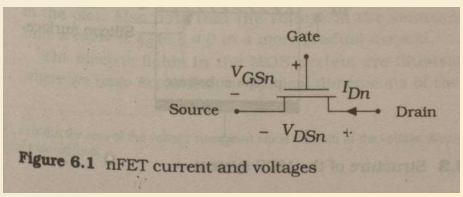

Figure 6.1 nFET current and voltages

6.1 MOS Physics

- Oxide capacitance $C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}}$
  - t_{ox}: the thickness of the oxide in cm < 10nm = 10^-6 cm
  - $\varepsilon_{ox} = 3.9\varepsilon_0$
  - $\varepsilon_0 = 8.854 \times 10^{-14}\ F/cm$
- Surface charge density $Q_s = -C_{ox}V_G\ C/cm^2$

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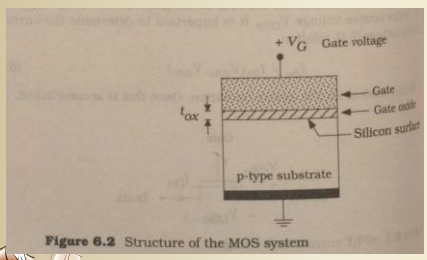

Figure 6.2 Structure of the MOS system

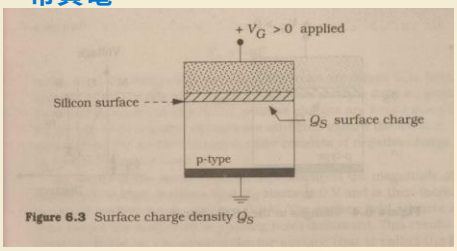

Figure 6.3 Surface charge density Q_S

6.1 MOS Physics

- Threshold voltage
  - $V_G = V_{ox} + \emptyset_s$
  - V_{ox}: voltage drop across the oxide layer
  - $\emptyset_s$: surface potential

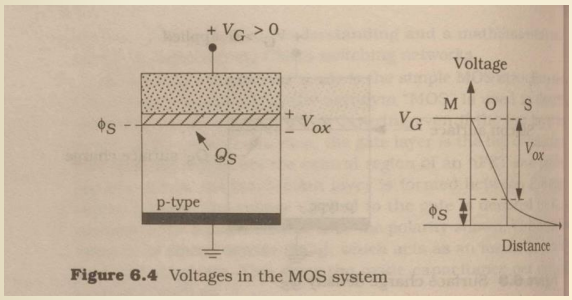

Figure 6.4 Voltages in the MOS system

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6.1 MOS Physics

- Oxide electric field: E_{ox}
- $F = Q_{partical}E$: Force on a charge particle
  - $Q_{partical}$: the charge on the particle
  - $F_h = +qE$; $F_e = -qE$
- Positive charges are forced away from the surface while negative charges are attracted toward the surface

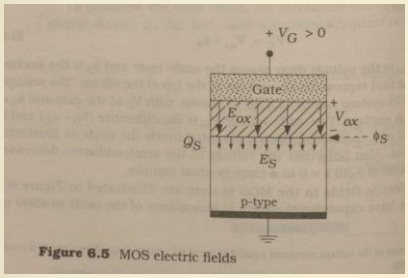


Figure 6.5 MOS electric fields

6.1 MOS Physics

- The nature of the surface charge depends upon the magnitude of the applied gate voltage
  - Bulk charge

    硼會抓電子
    - Bulk charge is trapped by the silicon crystal lattice and cannot move
    - $Q_B = -\sqrt{2q\varepsilon_{si}N_a\varphi_s} = -C_{ox}V_{ox}$ 解離參值?
    - ε_{si}: silicon permittivity $\approx 11.8\varepsilon_0$
  - Ionized dopant
  - Depletion region

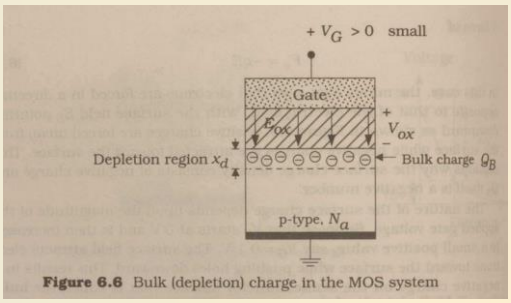


Figure 6.6 Bulk (depletion) charge in the MOS system

6.1 MOS Physics

- Threshold voltage V_{Tn}
  - If we increase the gate voltage to a special value, we observe a change in the charge properties
  - $V_G < V_{Tn}$
    - Charge is immobile bulk charge
    - $Q_s = Q_B$ bulk charge不會動
  - $V_G > V_{Tn}$
    - Charge is made up two distinct components
    - $Q_e = -C_{ox}(V_G - V_{Tn})$ 更多自由電子
    - $Q_s = Q_B + Q_e < 0$ 都是電子，Qe讓她動
    - Electrons are mobile
  - $V_G = V_{Tn}$
    - Q_e just start to form

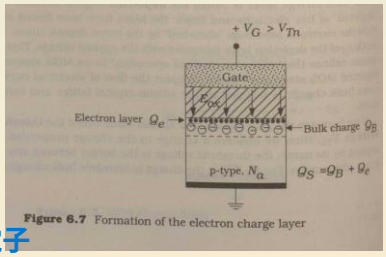


Figure 6.7 Formation of the electron charge layer

6.1 MOS Physics

- We must subtract the threshold voltage from V_g to obtain the effective voltage across the insulator after the electron layer has formed
- Q_B does not increase for gate voltages $V_{GS} > V_{Tn}$
- Typically, $0.5 \leq V_{Tn} \leq 0.8$

6.2 nFET Current-Voltage Equations

- Channel length L
  - Smallest feature size in the FET
- Channel width W
- Aspect ratio $\frac{W}{L}$
- The values used for W and L in this chapter are the electrical or "effective" values
  - $L = L' - \Delta L$
  - $W = W' - \Delta W$

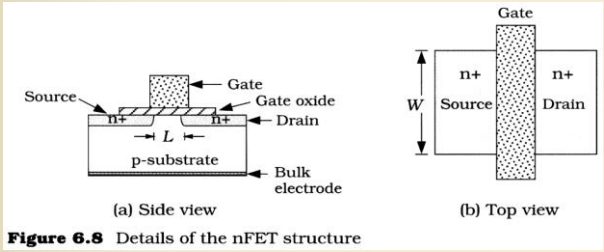


Figure 6.8 Details of the nFET structure

6.2 nFET Current-Voltage Equations

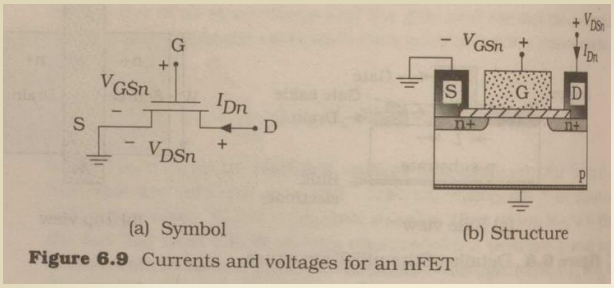


Figure 6.9 Currents and voltages for an nFET

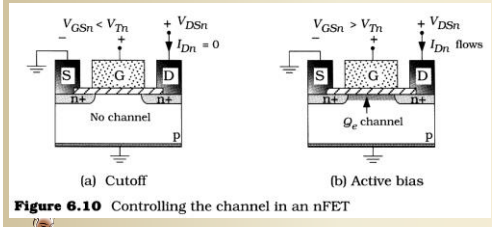


Figure 6.10 Controlling the channel in an nFET

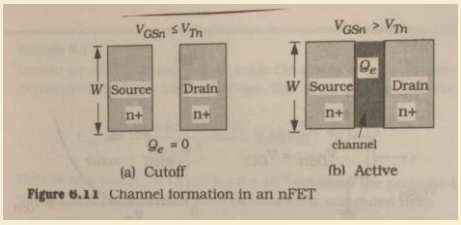


Figure 6.11 Channel formation in an nFET

6.2 nFET Current-Voltage Equations

- Since switching speed is critical in modern chip design, it is worth complete the effort to dig deeper into the operation of MOSFETs to provide a picture of the VLSI design environment
- The sizing of transistors provides the link between the physical design of logic gate
- I_{Dn} *vs* $V_{GSn}(V_{DSn}$ fixed)

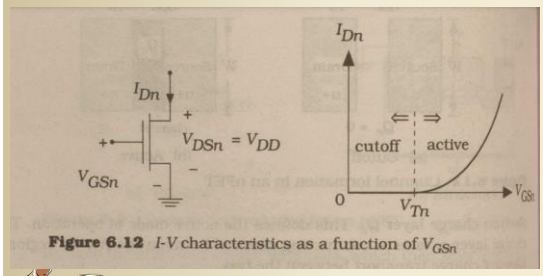


Figure 6.12 *I-V* characteristics as a function of V_{GSn}

- Square-law model
  - $I_{Dn} = \frac{\beta_n}{2}(V_{GSn} - V_{Tn})^2$
- Device transconductance parameter (device conductance) 元件轉換參數
  - $\beta_n = k'_n\left(\frac{W}{L}\right)$ 製程
- Process transconductance parameter (process conductance)
  - $k'_n = \mu_n C_{ox}$
  - $C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}}$

6.2 nFET Current-Voltage Equations

- I_{Dn} *vs* V_{DSn} (V_{GSn}fixed, $V_{GSn} > V_{Tn}$)
- Small value of V_{DSn} : parabola
  - $I_{Dn} = \frac{\beta_n}{2}[2(V_{GSn} - V_{Tn})V_{DSn} - {V_{DSn}}^2]$
- Saturation voltage
  - $V_{sat} = V_{DSn}|_{peak\ current} = V_{GSn} - V_{Tn}$
- Large value of V_{DSn} : $V_{DSn} \geq V_{sat}$
  - Saturation current
  - The largest I_{Dn} for a given V_{GSn}
  - $I_{Dn} = \frac{\beta_n}{2}(V_{GSn} - V_{Tn})^2$

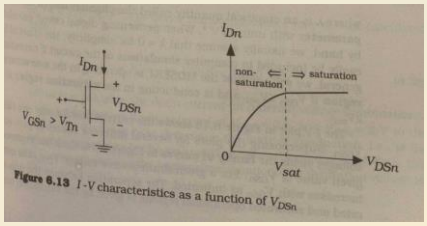


Figure 6.13 *I-V* characteristics as a function of V_{DSn}

- Increase slightly for $V_{DSn} \geq V_{sat}$
  - $I_{Dn} = \frac{\beta_n}{2}(V_{GSn} - V_{Tn})^2[1 + \lambda(V_{DSn} - V_{sat})]$
  - λ: empirical quantity called channel-length modulation parameter (V^{-1})
  - Use in simulation but not in hand calculation

6.2 nFET Current-Voltage Equations

- MOSFET
  - Non-saturation region: $V_{DSn} \leq V_{sat}$
  - Saturation region: $V_{DSn} > V_{sat}$
- nFET family of curves
  - Saturation current: $I_{Dn} = \frac{\beta_n}{2}(V_{sat})^2$

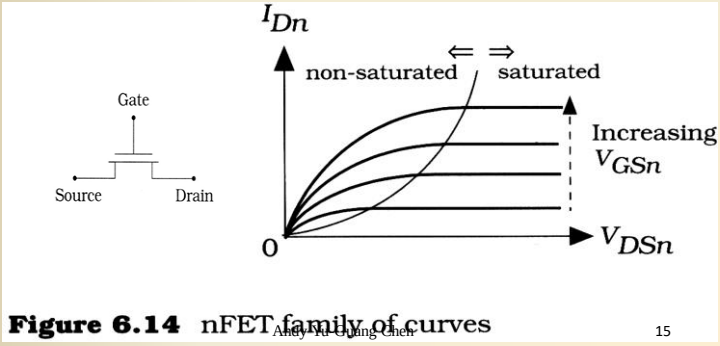


Figure 6.14 nFET family of curves

Example 6.2

- Consider an n-channel MOSFET with the following characteristics
  - t_{ox}=10nm, μ_n= 520 cm^2/V-sec, $\frac{W}{L} = 8, V_{Tn} = 0.7V$
- Find oxide capacitance (Cox)
  - $Cox = (\varepsilon_{ox}/t_{ox})$= 3.9*8.854*$10^{-14}$/(10*$10^{-7}$) = 3.45*$10^{-7} F/cm^2$
- Find process transconductance (k'_n)
  - $k'_n = \mu_n * C_{ox}$ = (520) * (3.45*10^{-7}) = 1.79*10^{-4} A/V^2 (process conductor)
  - k'_n = 0.179 mA/V^2
- Find device transconductance (β'_n)
  - $\beta'_n = k'_n(W/L)$ = 0.179*8 = 1.432 mA/V^2 (device conductor)
- Drain Current
- If V_{GSn} = 2V and V_{ds} = 2V
  - $V_{sat} = V_{GSn} - V_{Tn}$ = 2 – 0.7 = 1.3 V
  - $V_{DS} = 2V > V_{sat} = 1.3V$ ➔Saturation region
  - $I_{Dn} = \frac{\beta_n}{2}(V_{GSn} - V_{Tn})^2 = \left(\frac{1.432}{2}\right)(2 - 0.7)^2 = 1.21$ mA
- If V_{gs} = 2V and V_{DS} = 1.2V
  - $V_{DS} = 1.2V < V_{sat} = 1.3V$ ➔Non-saturation region
  - $I_{Dn} = \frac{\beta_n}{2}\left[2(V_{GSn} - V_{Tn})V_{DSn} - V_{DSn}^2\right]$ = (1.432/2)(2*1.3*1.2-$(1.2)^2$) = 1.21mA

6.2.2 Body Effect

- In reality, the MOSFET is **a four-terminal** device with the substrate being the (B) bulk terminal of the device
- **Body Bias effects** occur when a voltage V_{SBn} exists between the source and bulk terminals of a nFET in Figure 6.15.

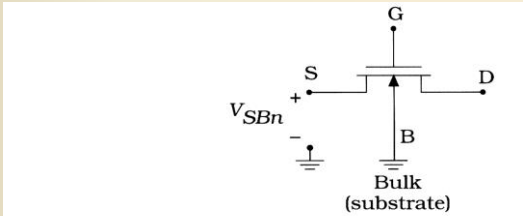


Figure 6.15 Bulk electrode and body-bias voltage

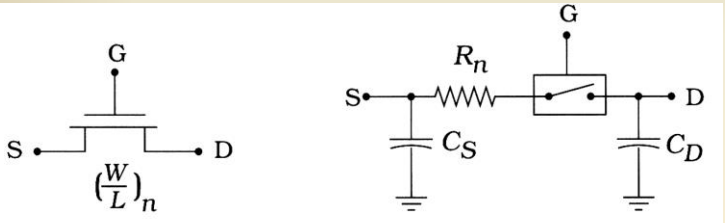
6.2.2 Body Effect

- The body-bias V_{SBn} voltage increases the threshold voltage
  - $V_{Tn} = V_{T0n} + r\left(\sqrt{2|\phi_F| + V_{SBn}} - \sqrt{2|\phi_F|}\right)$
  - $r = \frac{\sqrt{2q\varepsilon_{si}N_a}}{C_{ox}}$: body-bias coefficient ($V^{1/2}$)
    - $q = 1.6 * 10^{-19}\ C$; N_a:acceptor doping in p-type substrate
  - $2|\phi_F|$: bulk Fermi potential term
- $V_{Tn} = V_{T0n}\ when\ V_{SBn} = 0$
- Body effect can make 25% difference in threshold voltage

6.3 FET RC model

- The equations of current flow shows a **non-linear *I-V* characteristics**
  - Difficult to analyze electrical circuits
- Analysis and Design
  - Analysis
    - Analyze a resulting new network
    - Use CAD tool or SPICE
  - Design
    - Builds a new systems
    - Create a simplified **linear** model useful for estimating at the logic and system level
    - Ignore details
  - If we can work at least some of the important transistor characteristics into the model, then it can be used to provide a basis for the first design phase

6.3 FET RC model

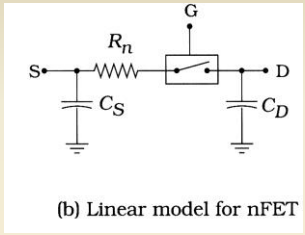


(a) nFET Symbol (b) Linear model for nFET

Figure 6.19 RC model of an nFET

6.3.1 Drain-Source FET Resistance

- Assume $V_{GS} > V_{Tn}$
- Drain-source resistance
  - $R_n = \frac{V_{DSn}}{I_{Dn}}$
  - I_{Dn} varies with V_{DSn}
- Resistance equation
  - $R_n = \frac{\eta}{\beta_n(V_{DD} - V_{Tn})}$ Idn = B(Vgs - Vtn)
  - η: account for some of the variation as the transistor is switched through various operation regions
  - $1 \leq \eta \leq 6$, 1 for simplicity



(b) Linear model for nFET

6.3.1 Drain-Source FET Resistance

- Resistance equation
  - Point a
    - $I_{Dn} = \frac{\beta_n}{2}[2(V_{GSn} - V_{Tn})V_{DSn}]$ by ignoring ${V_{DSn}}^2$
    - $\boldsymbol{R_n = \frac{1}{\beta_n(V_{GSn} - V_{Tn})}}$
  - Point b
    - $I_{Dn} = \frac{\beta_n}{2}[2(V_{GSn} - V_{Tn})V_{DSn} - {V_{DSn}}^2]$
    - $\boldsymbol{R_n = \frac{2}{\beta_n[2(V_{GSn} - V_{Tn}) - V_{DSn}]}}$
  - Point c
    - $I_{Dn} = \frac{\beta_n}{2}(V_{GSn} - V_{Tn})^2$
    - $\boldsymbol{R_n = \frac{2V_{DSn}}{\beta_n(V_{GSn} - V_{Tn})^2}}$
  - In all cases
    - $\boldsymbol{R_n \propto \frac{1}{\beta_n}}$
    - Device with a large β_n conducts current than one with a small β_n
    - $\beta_n = k'_n\left(\frac{W}{L}\right)$

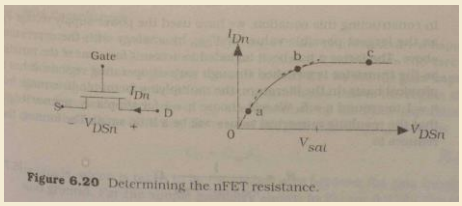


Figure 6.20 Determining the nFET resistance.

Example 6.4

- Consider an nFET
  - Channel width W= 8 μm, channel length L=0.5μm, $k'_n = 180\mu\, A/V^2$, $V_{Tn} = 0.7$V, $V_{DD} = 3.3V$,
- Find R_n
  - $R_n = \frac{1}{\beta_n(V_{DD}-V_{Tn})}$
  - R_n= 1/{(180*10^{-6})($\frac{8}{0.5}$)(3.3-0.7)}=133.5 Ω
- If we shrink Channel width to W= 5 μm, find R_n
  - R_n = 133.5*(8/5) = 213.6 Ω

6.3.2 FET capacitance

- A MOSFET has several parasitic capacitances
- The maximum switching speed of a CMOS circuit is determined by the capacitances

6.3.2 FET capacitance

- Gate capacitance
  - $C_G = C_{ox}A_G$
  - $A_G = WL'$
  - gate capacitance is proportional to the width of the channel

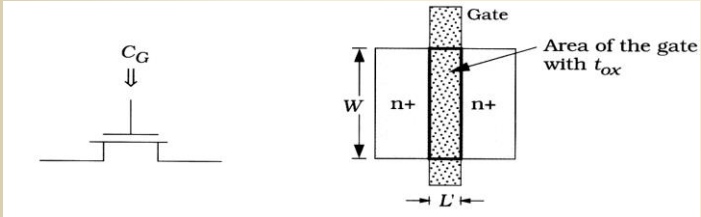


Figure 6.21 Gate capacitance in a FET

6.3.2 FET capacitance

- Gate capacitance
  - C_{GS}: gate-source capacitance
  - C_{GD}: gate-drain capacitance
  - Their value changes with the voltages due to the changing shape of the channel region
    - $C = C(V)$ ➔ non-linear
  - Estimation
    - $C_{GS} \approx \frac{1}{2}C_G \approx C_{GD}$

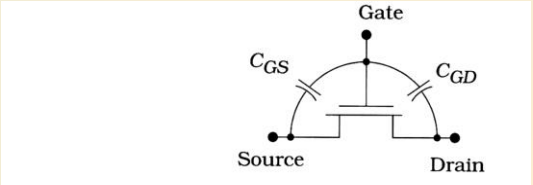


Figure 6.22 Gate-source and gate-drain capacitance

6.3.2 FET capacitance

- Junction (Depletion) Capacitance
  - PN junction automatically exhibits capacitance due to the opposite polarity charged involved
  - C_{SB}: source-bulk
  - C_{DB}: drain-bulk
- Two complications
  - Capacitance also varies with the voltage
  - Calculating the PN junction capacitance is the geometry of PN junction
- Capacitance VS. Voltage
  - $C_0 = C_j A_{pn}$ F
    - C_0 : zero-bias capacitance
    - C_j: parameter (F/cm²)
    - A_{pn} : area of the junction in units of cm^2
  - $C = \frac{C_0}{\left(1+\frac{V_R}{\phi_0}\right)^{m_j}}$
- Linearly graded junction

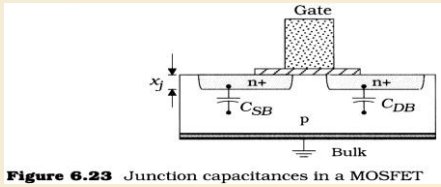


Figure 6.23 Junction capacitances in a MOSFET

6.3.2 FET capacitance

- Bottom and side contributions
  - Bottom
    - $A_{bot} = XW$
    - $C_{bot} = C_j XW$
  - Sidewall
    - $A_{sw} = 2(W \times x_j) + 2(X \times x_j) = x_j P_{sw}$
    - P_{sw} = 2 (W + X): sidewall perimeter
    - $C_{sw} = C_{jsw} P_{sw}$ (F)
    - $C_{jsw} = C_j X_j$: sidewall capacitance per unit perimeter
  - $C_n = C_{bot} + C_{sw} = C_j A_{bot} + C_{jsw} P_{sw}$

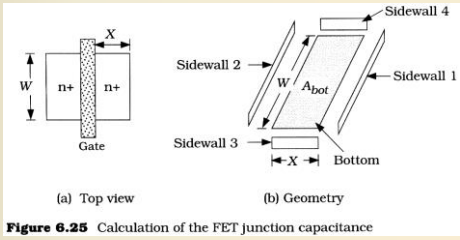


Figure 6.25 Calculation of the FET junction capacitance

6.3.3 Construction of The Model

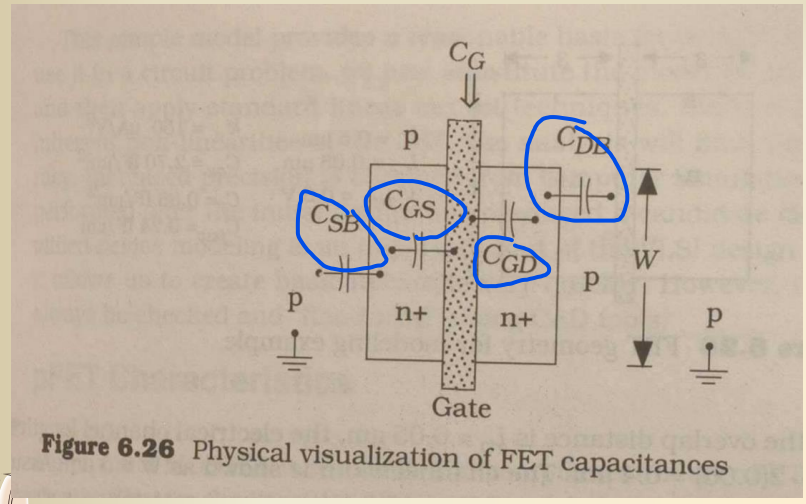


Figure 6.26 Physical visualization of FET capacitances

6.3.3 Construction of the model

- The parasitic resistance and capacitance combined to construct the simple RC model of nFET
  - $C_S = C_{GS} + C_{SB}$
  - $C_D = C_{GD} + C_{DB}$
- Simple model provides a reasonable basis for design estimates
- Checked and fine-tuned using CAD tools

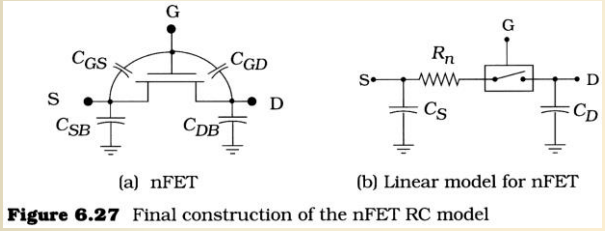


Figure 6.27 Final construction of the nFET RC model

6.3.3 Construction of the model

- C_n = 0.86*5*3.05 +0.24*2*(5+3.05) = 16.98fF
- C_G= 2.7*5*0.5 = 6.75fF
- C_{gd}=C_{gs}=1/2 C_G = 3.375 fF
- C_d=C_s= 16.98+3.375 = 20.36 fF

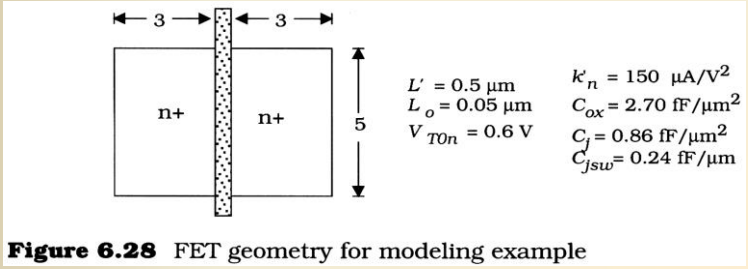


Figure 6.28 FET geometry for modeling example

Q&A

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