CS3120

Introduction of Integrated Circuit Design

Chap 4
Fabrication of CMOS Integrated Circuits

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Outline

- 4.1 Overview of Silicon Processing
- 4.2 Material Growth and Deposition
- 4.3 Lithography
- 4.4 The CMOS Process Flow
- 4.5 Design Rules

Fabrication of CMOS Integrated Circuits

- An integrated circuit consists of several patterned layers of materials for transistors and interconnections
- We have understood the structure of CMOS now
- In this chapter, we discuss how the circuits are fabricated in the manufacturing process

4.1 Overview of Silicon Processing

- Wafers are typically 100-300mm in diameter and 0.4-0.7 mm thick
- Start with a bare polished surface
- The wafer is subjected to thousands of individual steps
  - Most important are the creating and patterning the layers materials
  - Others are cleaning and rinsing of the wafer
- Several weeks to make it through the entire processing line

4.1 Overview of Silicon Processing

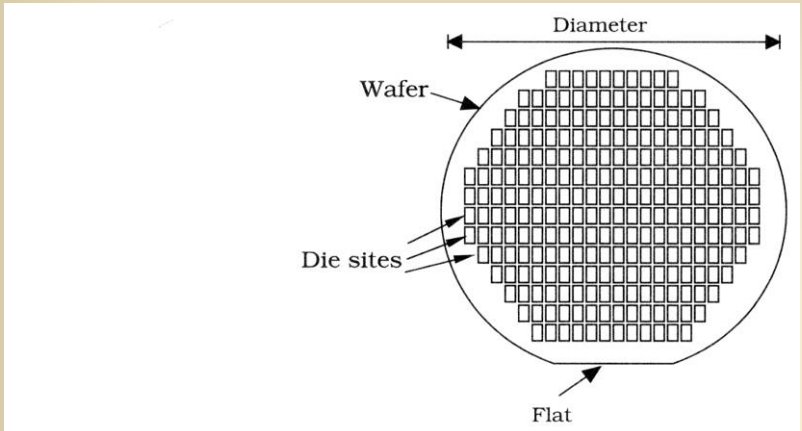


Figure 4.1 Silicon wafer showing die sites

4.1 Overview of Silicon Processing

- Fabrication yield
  - Not every site is functional
  - Fabrication Yield $Y = \frac{N_G}{N_T}$
    - N_G :number of good site
    - N_T :number of total site
  - A yield of Y= 85% means that 85% of the chips operate as they should
  - Empirical analysis shows that $Y = e^{-\sqrt{DA}}$ where A is the area and D is the defect density
    - Defect density: Average # of defects per cm^2

4.2 Material Growth and Deposition

- Stacking layers of various materials in a pre-specified sequence
- Most layers are created first and then patterned using lithographic sequence
- We discuss materials growth and deposition

4.2.1 Silicon Dioxide

- Critically important in IC processing
  - Excellent electrical insulator
  - Adheres well to all material
  - Thermal oxide: Grown on a wafer
    - $Si+O_2 \rightarrow SiO_2$
    - Depends on temperature, crystal orientation, and growth time
  - Wet oxidation
    - $Si + 2H_2O \rightarrow SiO_2 + 2H_2$
  - Deposited on the top (a.k.a CVD oxide)
    - Create SiO_2 and deposit them on the surface
    - $SiH_4(gas) + 2O_2(gas) \rightarrow SiO_2$ (solid) + $2H_2O$ (gas)
    - Chemical Vapor Deposition (CVD)

4.2.1 Silicon Dioxide

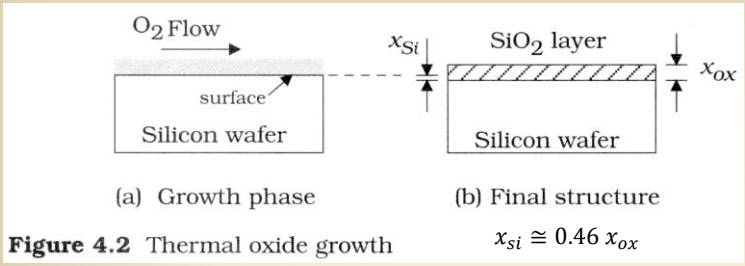


Figure 4.2 Thermal oxide growth

$x_{si} \cong 0.46\, x_{ox}$

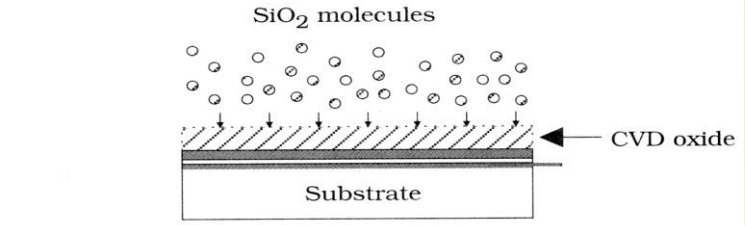


Figure 4.3 CVD oxide process

4.2.2 Silicon Nitride

- Silicon Nitride (Si_3N_4)
  - $3SiH_4(gas) + 4NH_3(gas) \rightarrow Si_3N_4\ (solid) + 12H_2\ (gas)$
  - Strong barrier to most atoms
  - Use as an overglass layer
  - Final protective coating on a chip

4.2.3 Polysilicon

- Deposit silicon on top of SiO_2
  - The silicon attempts to crystallize but can't find a crystal structure for reference
  - Result in the formation of small crystallites
  - The material is then called **polycrystal silicon** or **polysilicon**
- Polysilicon is universally used as gate material in FETs
- Add Ti or Pt to reduce the sheet resistance

4.2.4 Metals

- Aluminum (Al) is the most common metal for interconnect wiring
  - Al has good adhesion and is easy to pattern
  - The problem is electromigration (EM)

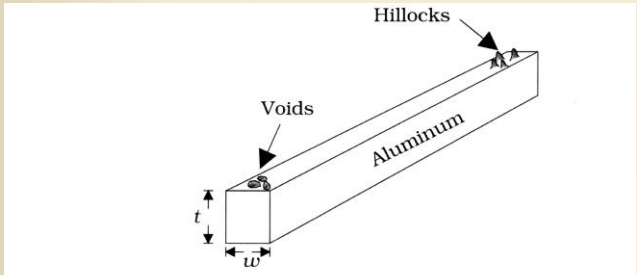
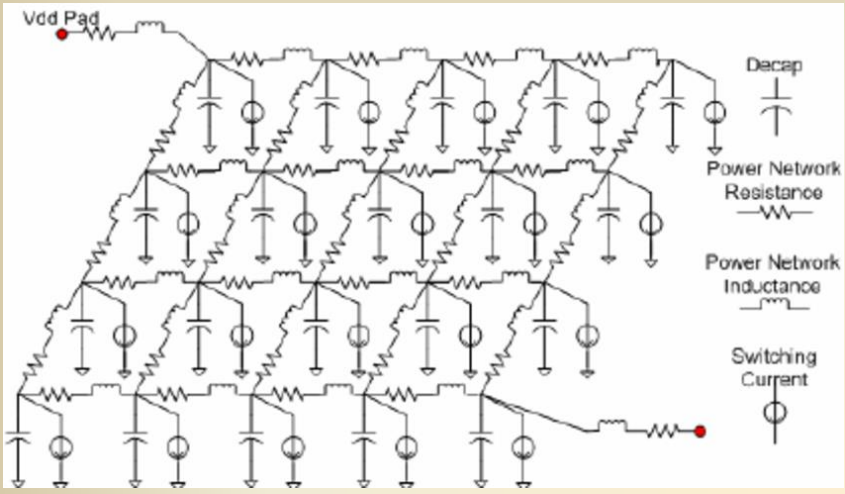


Figure 4.4 Visualization of electromigration effects in aluminum

4.2.4 Electromigration

- High current flow densities tend to literally move atoms from one end and creates pits called voids
- Currently density: $J = \frac{I}{A}$ where A is the cross-sectional area
- Electromigration is controlled by specifying the minimum line width w needed to keep J below a maximum value J_{max}
  - This is **design rule**
- Copper has been introduced as a replacement to aluminum. Resistivity is one-half the value of Al

4.2.4 VDD Ground Network



4.2.5 Doped Silicon Layers

- Introduce donor or acceptor
- A doped silicon layer is a patterned *n* or *p* type
- Ion implantation: the atoms are first ionized in a chamber, and then accelerated to high energies
- Ions smashed into the substrate

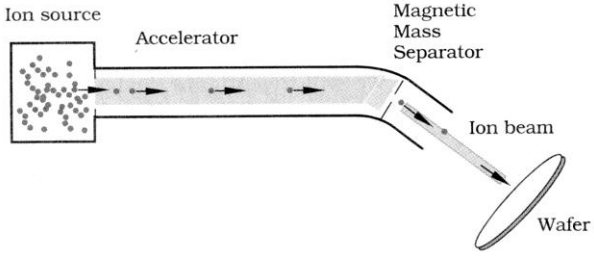


Figure 4.5 Basic sections of an ion implanter

4.2.6 Chemical-Mechanical Polishing

- Chemical etching and mechanical "sanding" to produce planar surfaces

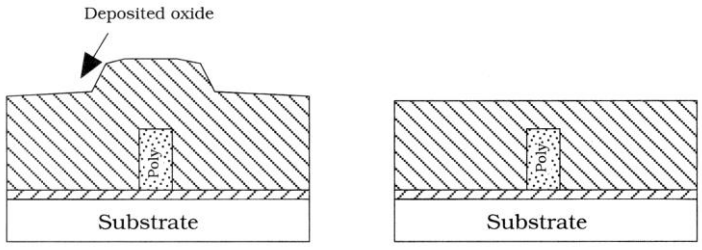


Figure 4.8 Surface planarization

4.3 Lithography

- Photolithography: optically project the shadow of the pattern onto the surface of the chip
- The same process to make printed circuit boards
- Start with a desired pattern defined for each layer
- Mask (reticle) is typically 5-10x the size of the actual chip
  - Transparent (no metal) and opaque (metal)

4.3 Lithography

- First, coat the wafer with a light-sensitive liquid plastic material **photoresist** (or called resist)
  - Sensitive to light
- Exposure step. (Figure 4.9- 4.14)
- After the resist is developed, **hardened layers** remain in the regions that were shielded from the light
  - Hardened layer: protect underlying regions from the **etching** process

4.3 Lithography

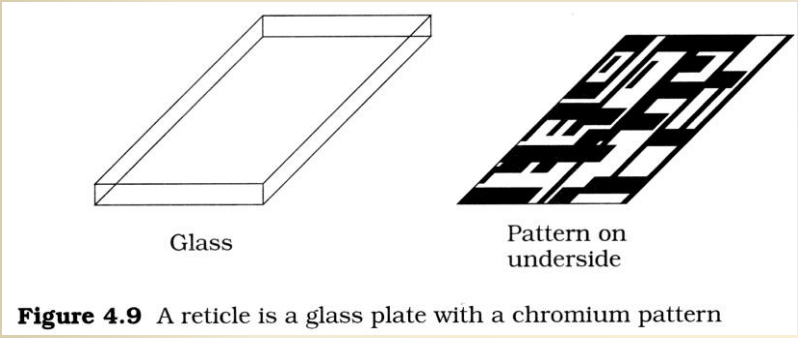


Figure 4.9 A reticle is a glass plate with a chromium pattern

4.3 Lithography

- Coat the surface with light-sensitive liquid material
- Spin the wafer for uniform coating

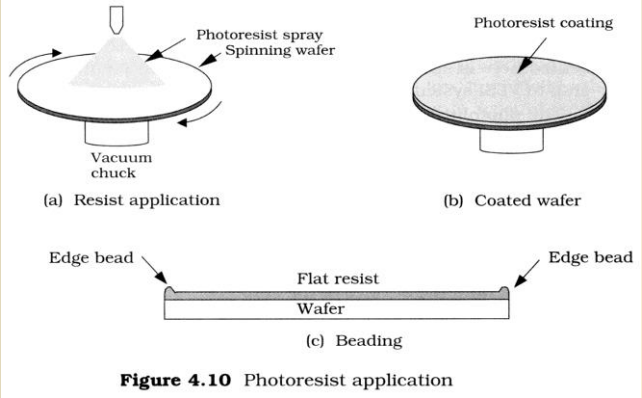


Figure 4.10 Photoresist application

4.3 Lithography

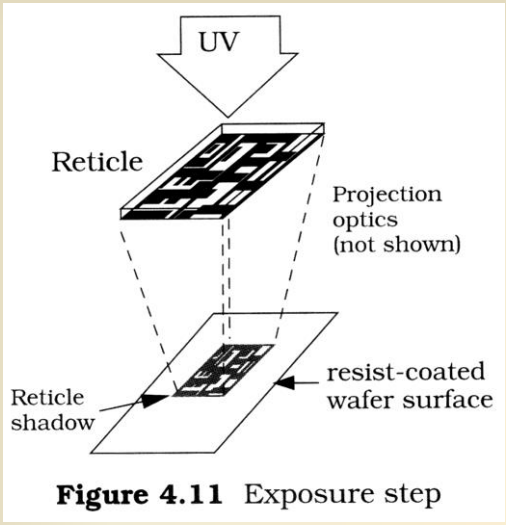


Figure 4.11 Exposure step

4.3 Lithography

- The region shield from light is harden and others are rinsed away

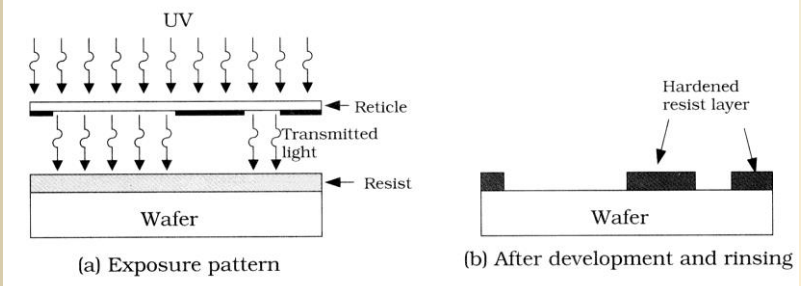


Figure 4.12 Characteristics of positive photoresist

4.3 Lithography

- Hardened resist layer is used protect underlying regions from the etching process
- The etching step removes oxide in the unprotected regions
- This technique is used to pattern layer including poly, CVD oxides, metals

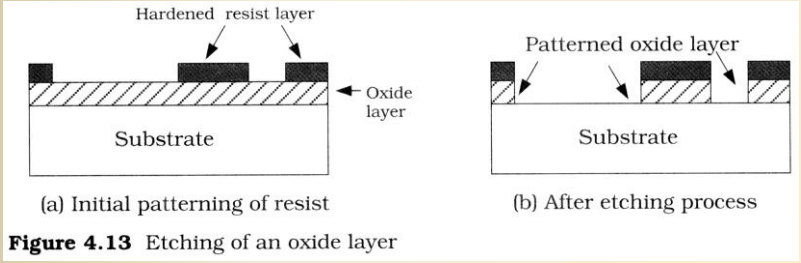


Figure 4.13 Etching of an oxide layer

4.3 Lithography

- The resist-oxide layers are used to shield from an ion implantation step

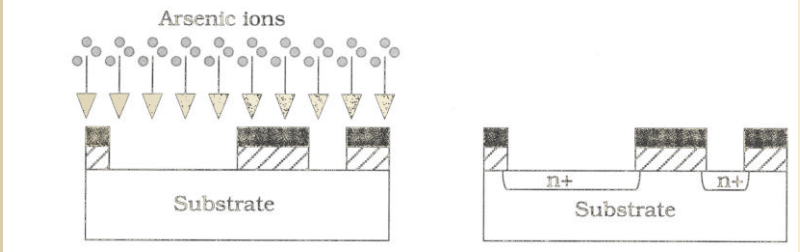


Figure 4.14 Creation of doped silicon patterns

4.3 Lithography

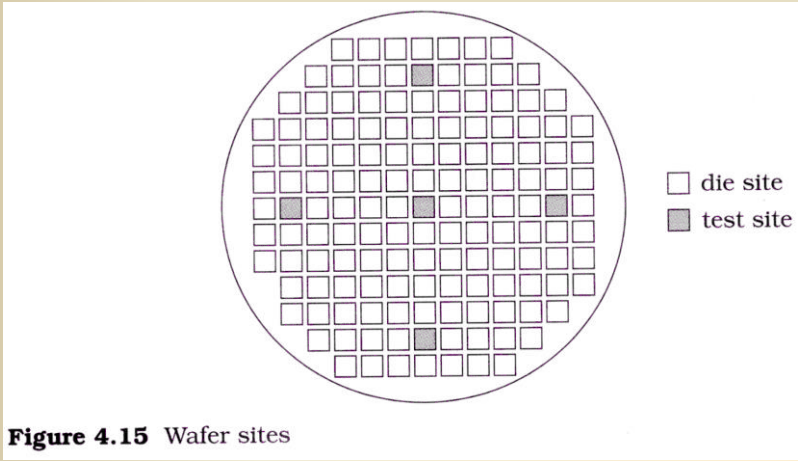


Figure 4.15 Wafer sites

4.3.1 Clean Room

- Lithographic process is sensitive to dust particles and is performed in clean room environment
- HEPA (high-efficient particulate air) filter with 99.97%

4.4 The CMOS Process Flow

- Study the main steps in a “standard” silicon CMOS process
- Device and circuit engineers view processing parameters as the fundamental limit to how fast transistors can operate
- The system architect understands that logic blocks need to be created in silicon, and that the processing dictates area allocations, interconnect levels, delays, clock speeds, and dozens of other system-level considerations
- Initial steps are shown in Figure 4.16 (see next page)

4.4 The CMOS Process Flow

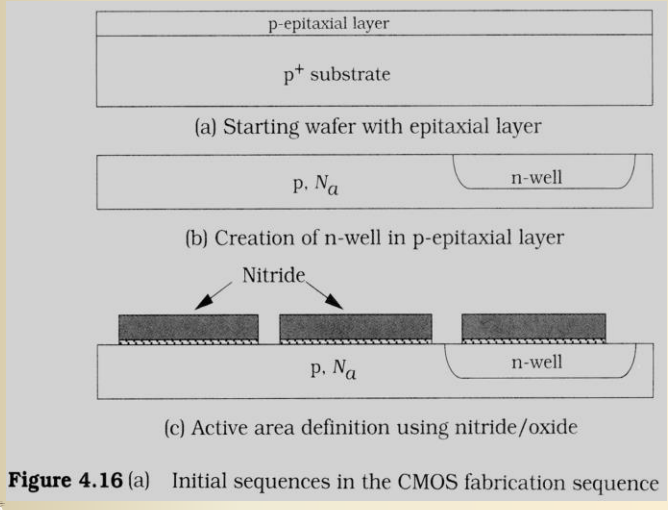


Figure 4.16 (a) Initial sequences in the CMOS fabrication sequence

4.4 The CMOS Process Flow

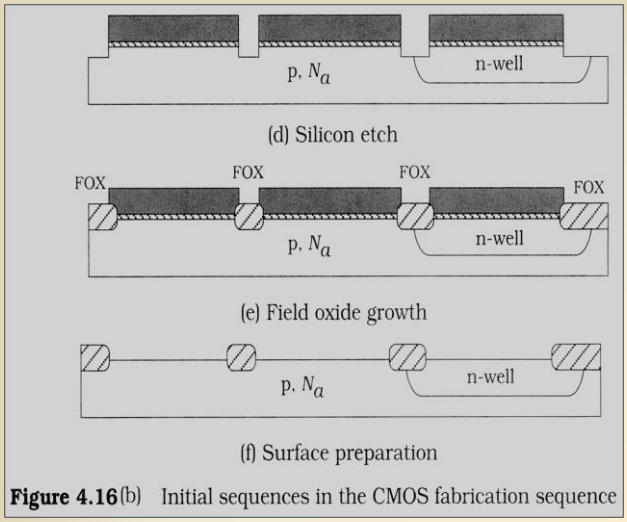


Figure 4.16(b) Initial sequences in the CMOS fabrication sequence

4.4 The CMOS Process Flow

- Self-aligned gate process

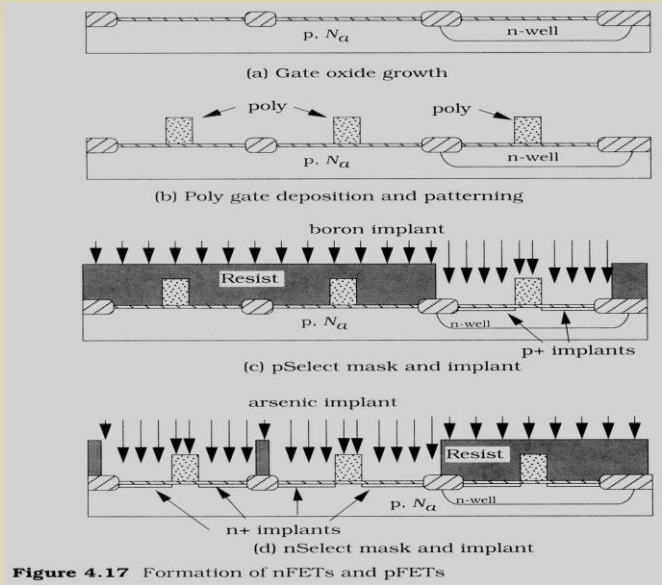


Figure 4.17 Formation of nFETs and pFETs

4.4 The CMOS Process Flow

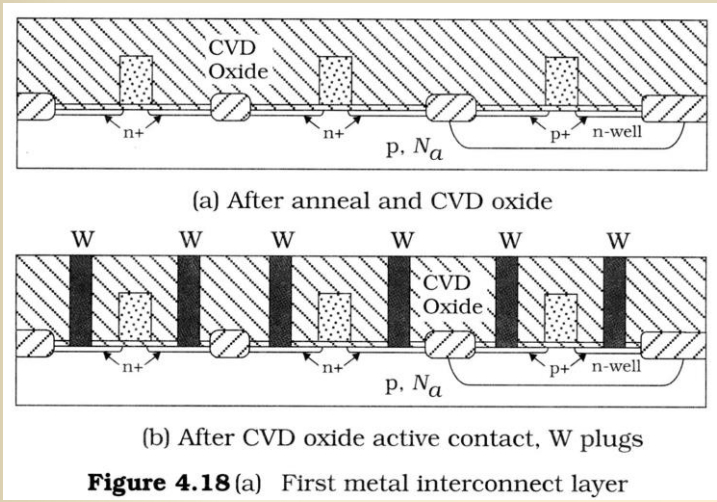


Figure 4.18 (a) First metal interconnect layer

4.4 The CMOS Process Flow

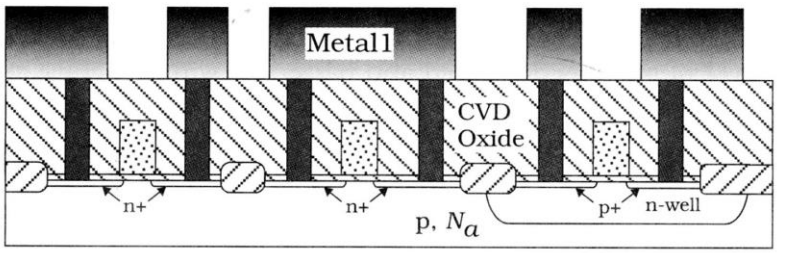


Figure 4.18 (b) First metal interconnect layer

4.4 The CMOS Process Flow

- After all of the metal layers have been added, the entire chip is covered with the overglass layer that protects the surface from external contaminants
  - Silicon nitride is the most common overglass material
- The simplest way to interface the silicon circuitry with the outside world is to use a pad frame arrangement where large metal bonding pads surround the central chip core area

4.4 The CMOS Process Flow

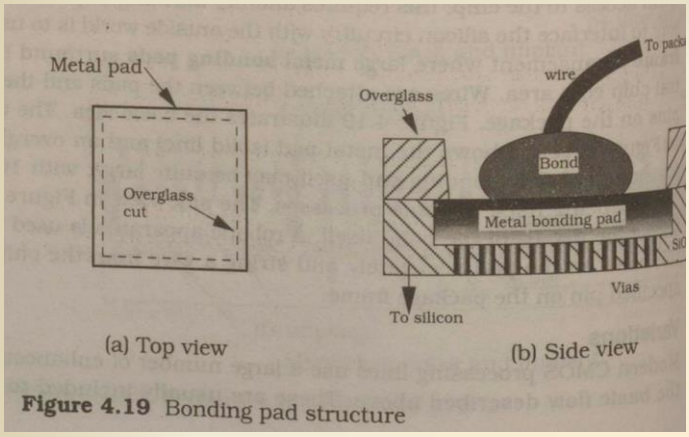
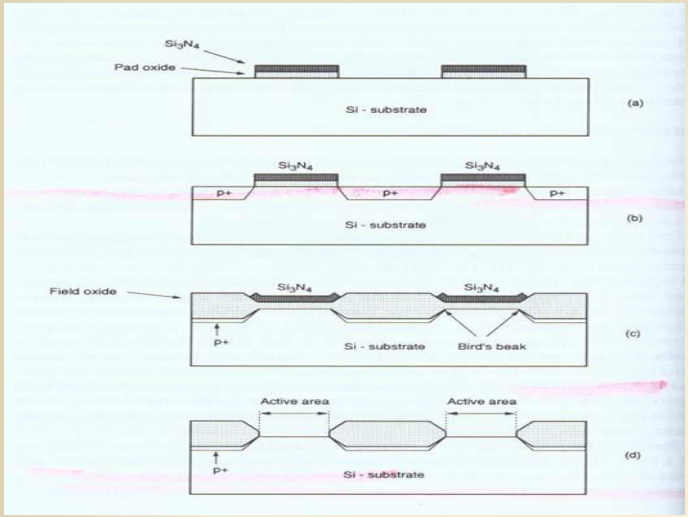
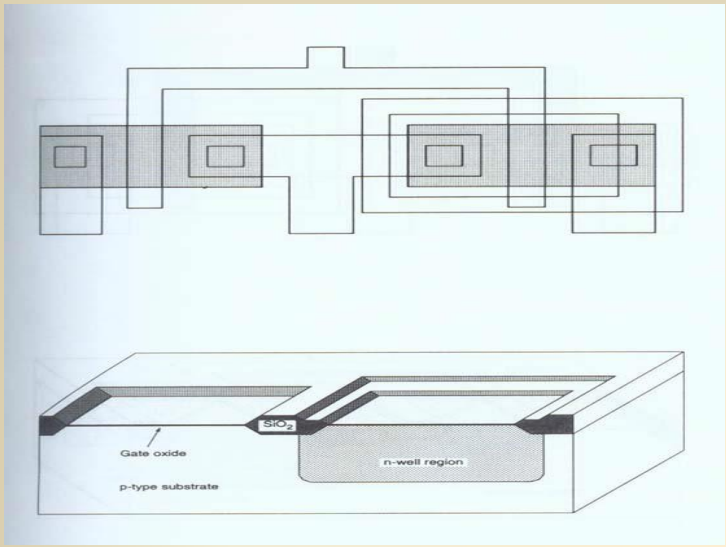


Figure 4.19 Bonding pad structure

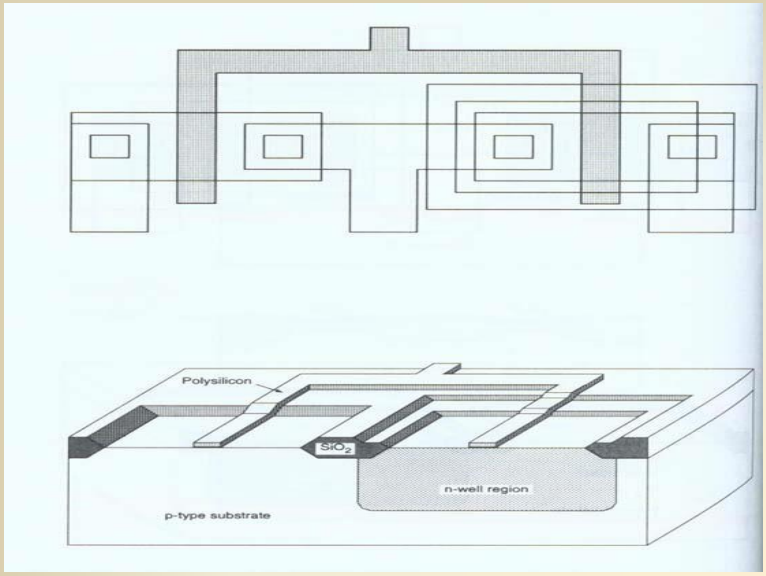
4.4 The CMOS Process Flow



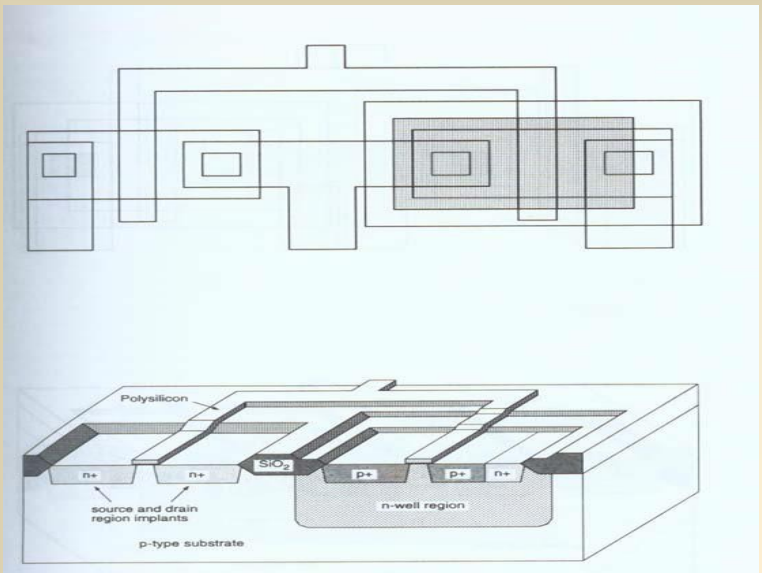
4.4 The CMOS Process Flow



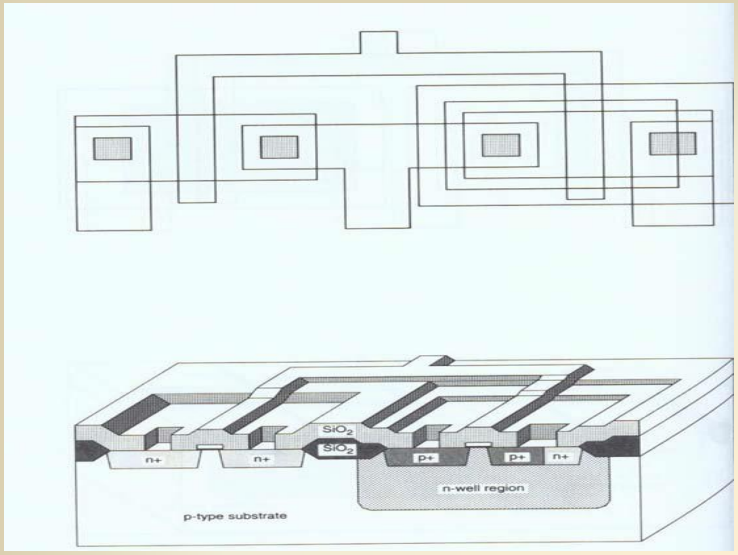
4.4 The CMOS Process Flow



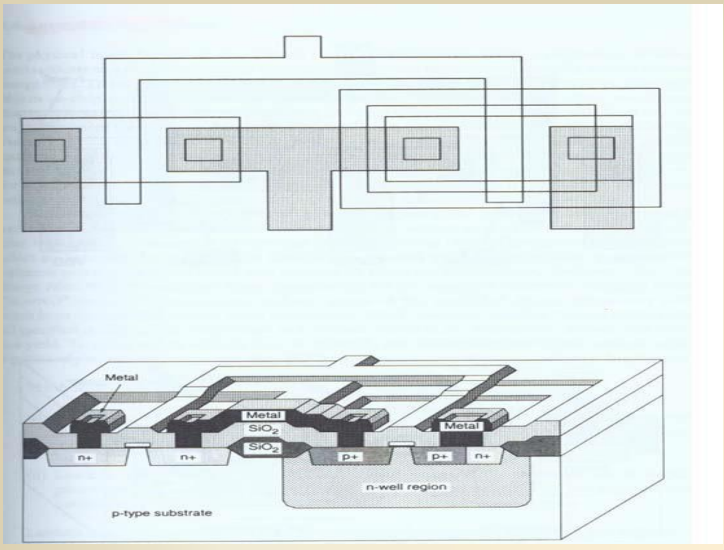
4.4 The CMOS Process Flow



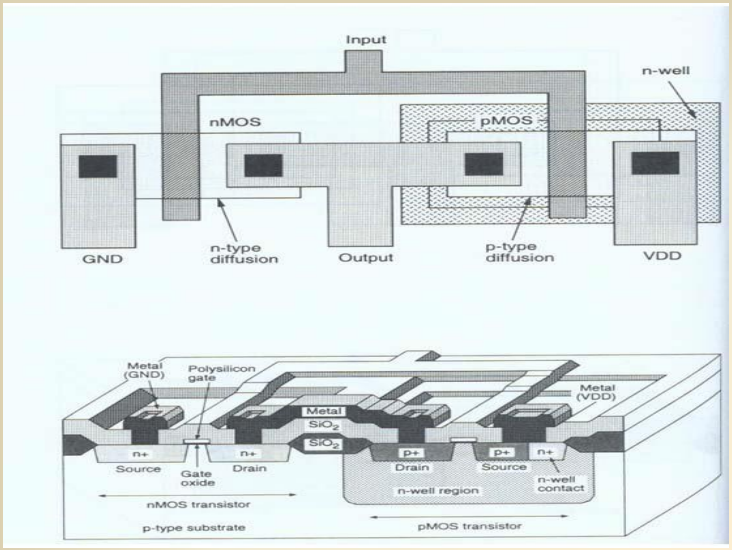
4.4 The CMOS Process Flow



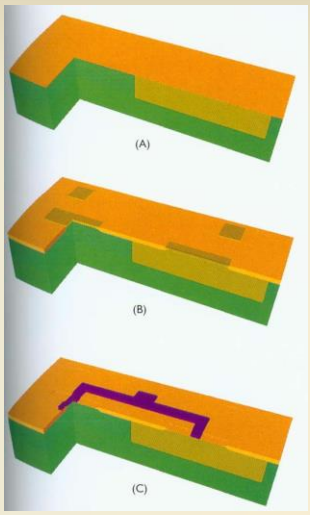
4.4 The CMOS Process Flow



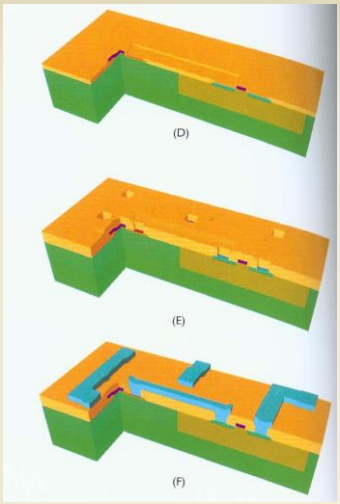
4.4 The CMOS Process Flow



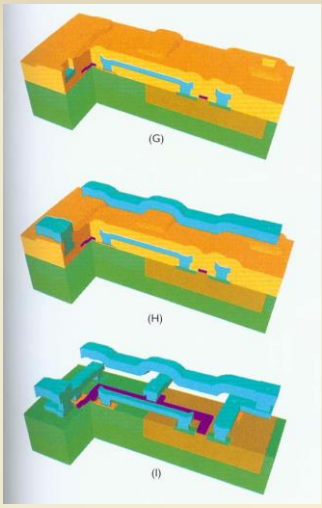
4.4 The CMOS Process Flow



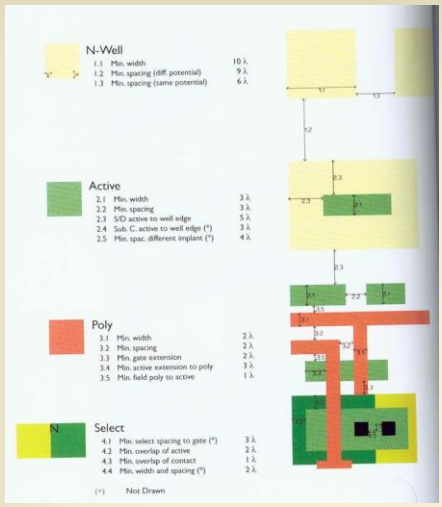
4.4 The CMOS Process Flow



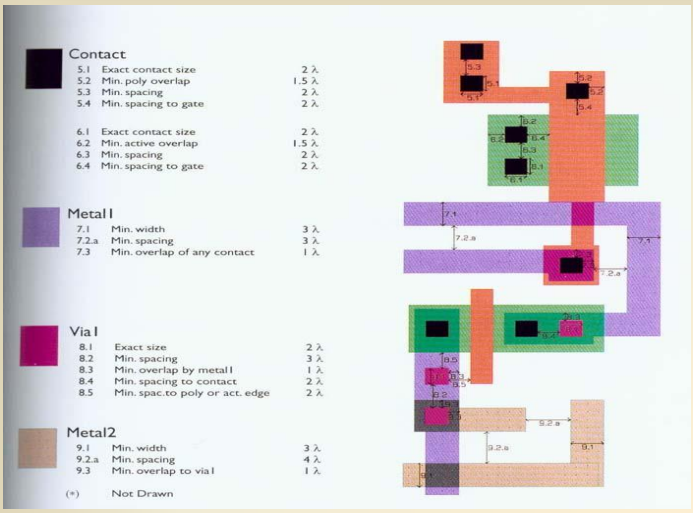
4.4 The CMOS Process Flow



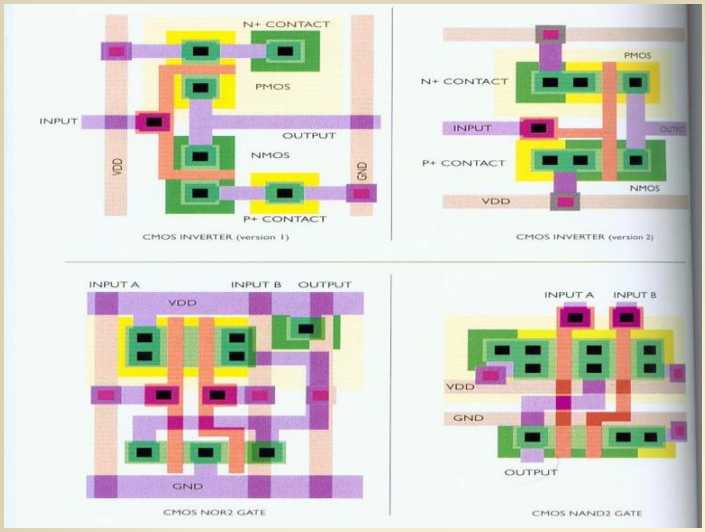
4.4 The CMOS Process Flow



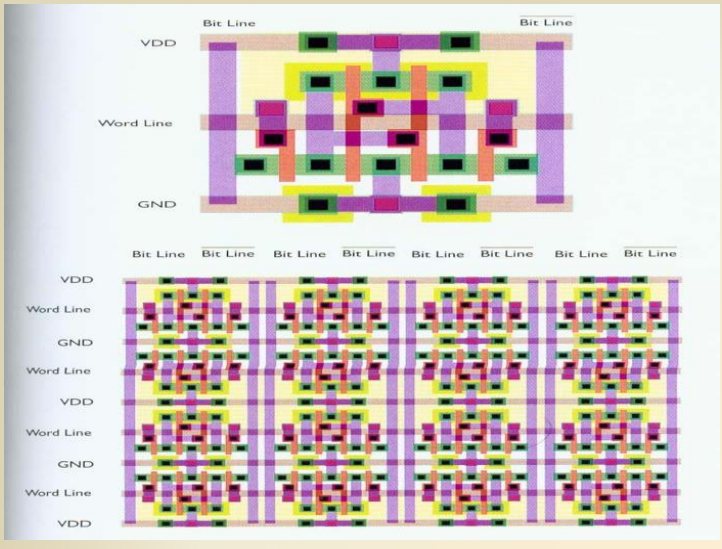
4.4 The CMOS Process Flow



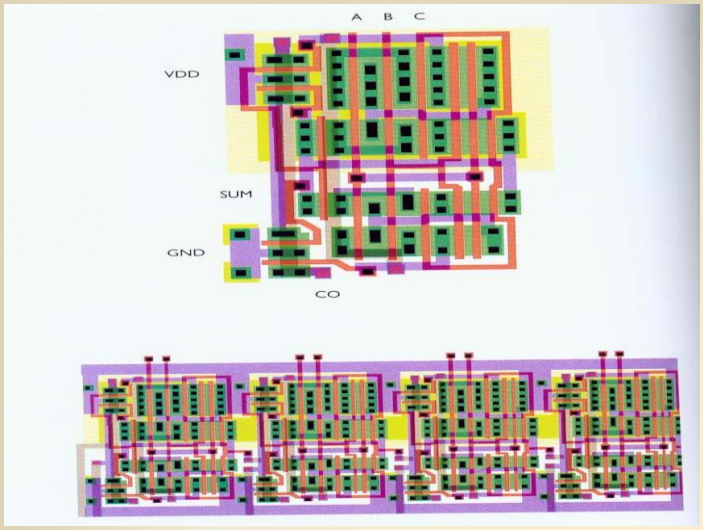
4.4 The CMOS Process Flow



4.4 The CMOS Process Flow



4.4 The CMOS Process Flow



4.4 The CMOS Process Flow

- Lightly doped drain (LDD) FETs

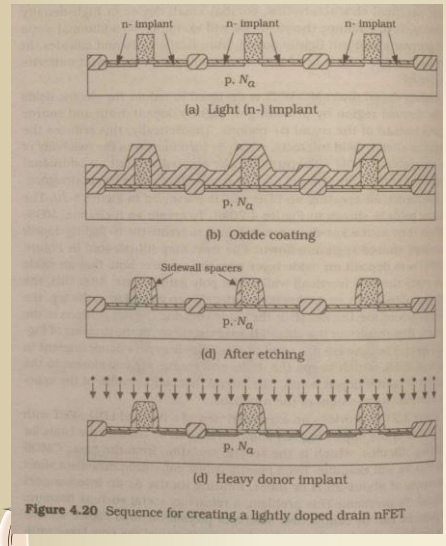


Figure 4.20 Sequence for creating a lightly doped drain nFET

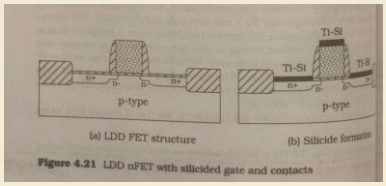


Figure 4.21 LDD nFET with silicided gate and contacts

4.4 The CMOS Process Flow

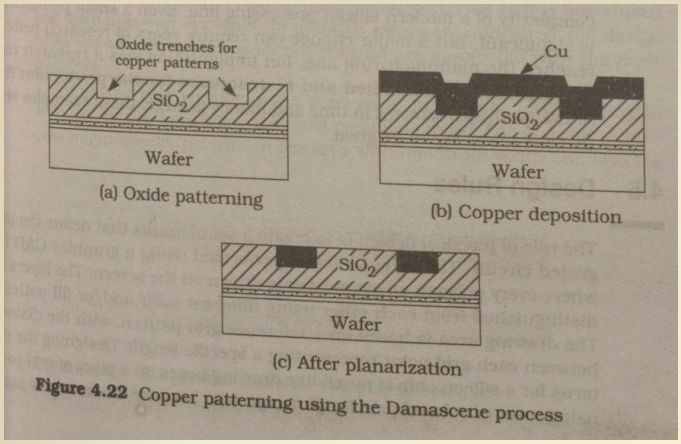


Figure 4.22 Copper patterning using the Damascene process

4.5 Design Rule

- The role of physical design is to create a set of masks that define the integrated circuit
- The drawing area is based on a reference grid pattern with the distance between each grid point representing a specific length
- Fabrication equipment process limited **accuracy**

4.5 Design Rule

- Topological design rules
  - a set of geometrical specifications that dictate the design of the layout masks
- A design rule set provides numerical values for minimum dimensions, line spacing, and other geometrical quantities.
  - w = minimum width specification
  - s = minimum spacing value
  - d = generic minimum distance
  - Ex: w_{m1} minimum width of a metal1 line
    $s_{m1\text{-}m1}$ minimum spacing between metal1 line

4.5 Design Rule

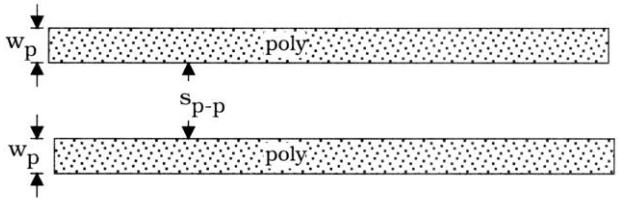


Figure 4.24 Design rule limits for two polysilicon lines

4.5 Design Rule

- Lambda design rule
  - a simpler set of design rules that can be easily scaled.
- Spacing, width, distances are written in the form of value = m*λ
  - Ex. W = 2 λ, s = 3 λ
- The draw back is the low packing density using the integer value of m

4.5 Design Rule

- Design rules can be classified into 4 types: minimum width, minimum spacing, surround, and extension.
  - Surround: when a feature must be placed inside of an existing feature. Ex.: active contact.
  - Extension rule: requires that portion of the pattern to be extended beyond the edge of a border. Ex.: poly.

4.5 Design Rule

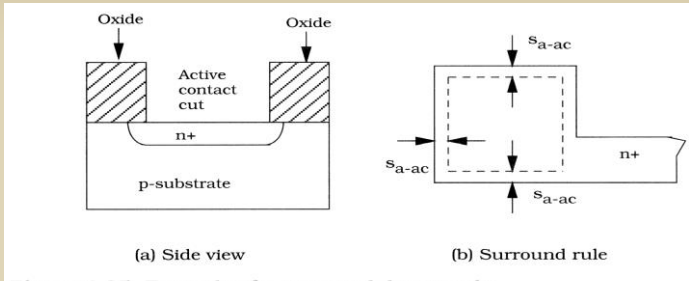


Figure 4.25 Example of a surround design rule

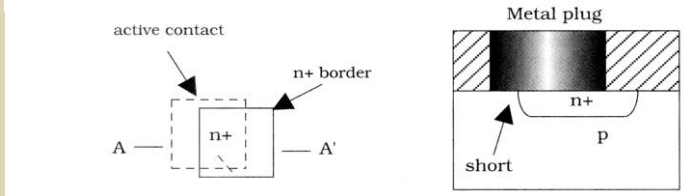


Figure 4.26 Misalignment-induced defect

4.5 Design Rule

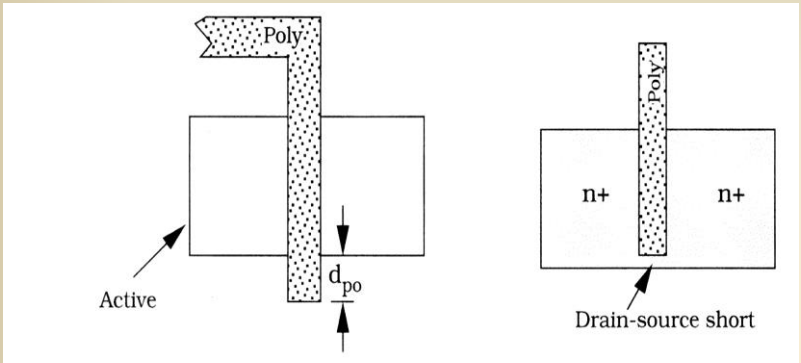


Figure 4.27 Example of an extend (gate overhang) design rule

4.5.1 Physical Limitations

- Line width limitation: reticle shadow does not have sharp edges due to optical diffraction. Feature size should be much less than optical wavelength
- Etching profiles

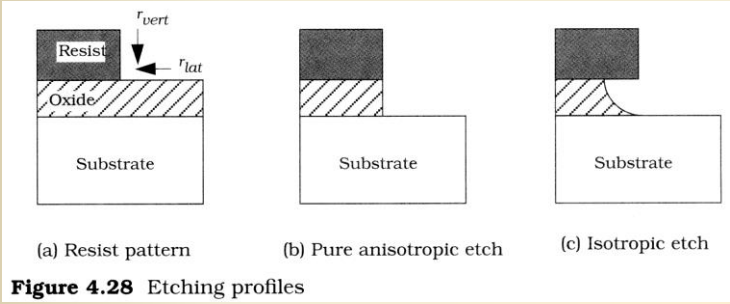


Figure 4.28 Etching profiles

4.5.1 Physical Limitations

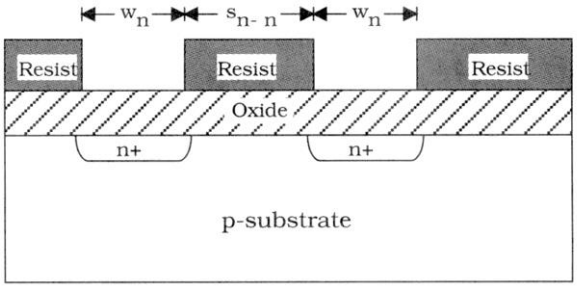
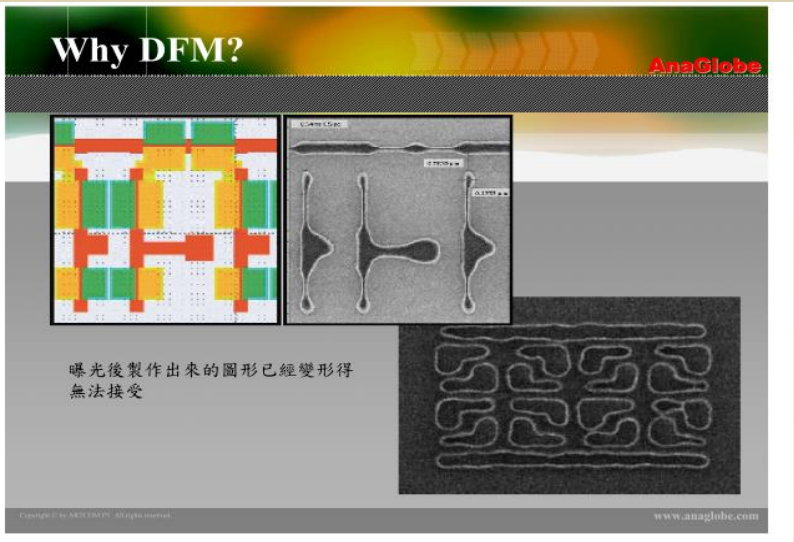
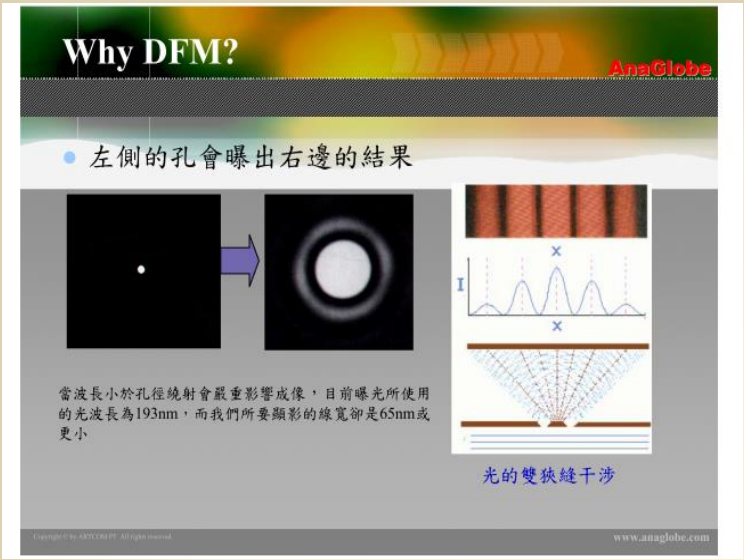


Figure 4.29 Limits on n+ spacings

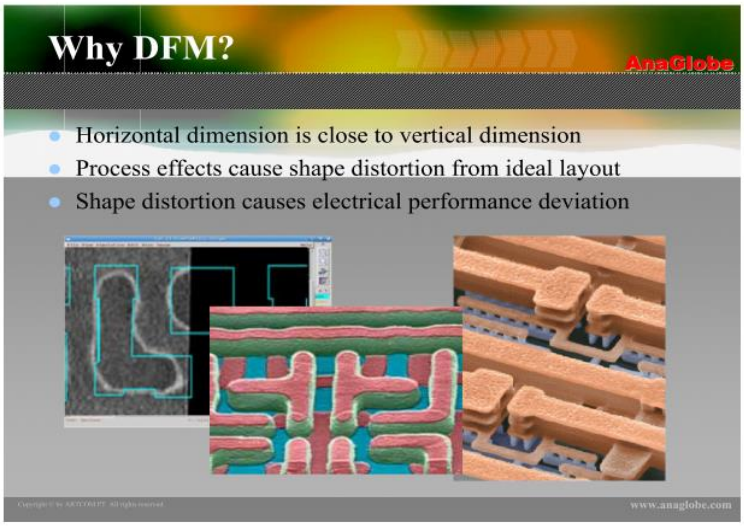
4.5.1 Physical Limitations



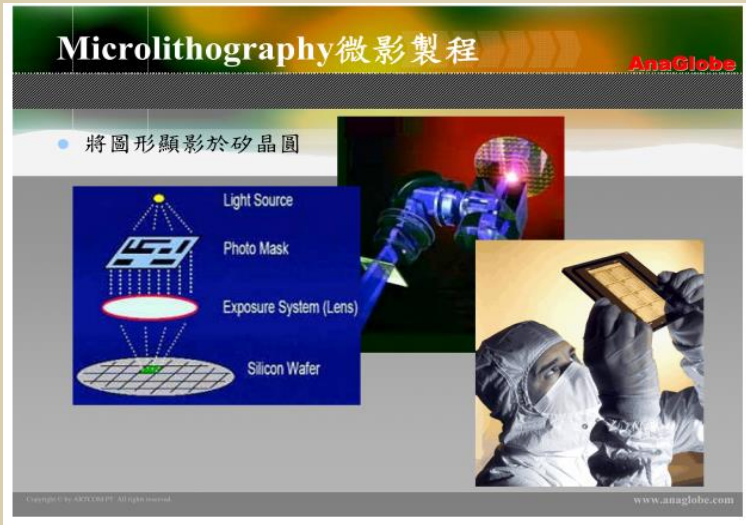
4.5.1 Physical Limitations



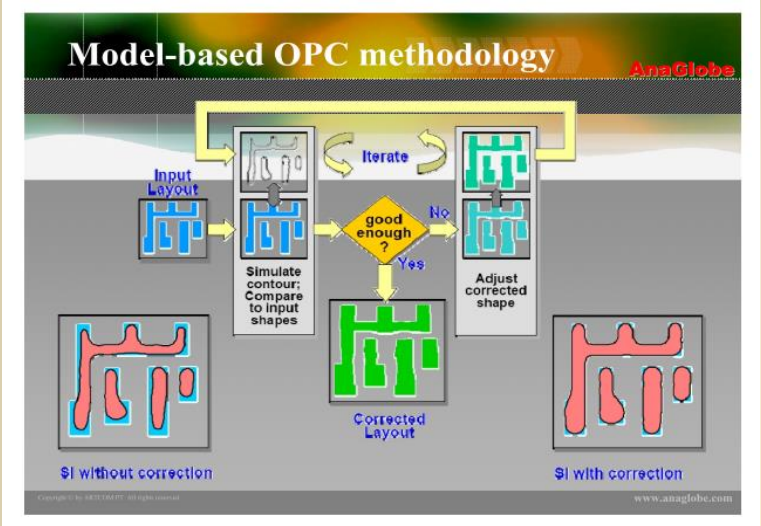
4.5.1 Physical Limitations



4.5.1 Physical Limitations



4.5.1 Physical Limitations



4.5.2 Physical Limitations

- A CMOS process provide electrical layout rules
- These tend to be in the form of changes to the basic rule values when certain electrical conditions occur
- Electrical rules be provided directly in the general set, or as an addendum
- An example of an electrical rule is the allowed width of interconnect line

Summary

- Fabrication process and fabrication yield
- Material Growth and Deposition
- Lithography
- The CMOS Process Flow
- Design Rules

Q&A

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