CS3120
Introduction of Integrated Circuit Design

Chap 3
Physical Structure of CMOS Integrated Circuits

Andy, Yu-Guang Chen
Associate Professor, Department of EE, National Central University
Adjunct Assistant Professor, Department of CS, National Tsing Hua University
andyygchen@ee.ncu.edu.tw

Outline

- 3.1 Integrated Circuit Layers
- 3.2 MOSFETS
- 3.3 CMOS Layers
- 3.4 Designing FET Arrays

From Logic To Physical

- CMOS integrated circuits are electronic switching networks
- A primary task of VLSI designer is to translate circuit schematics into silicon form
- Physical design separates VLSI from general digital engineering
- In this chapter, we will examine the structure of a CMOS integrated circuit as seen at the microscopic silicon level in the design hierarchy

3.1 Integrated Circuit Layers

- A silicon integrated circuit can be viewed as a collection of patterned material layers.
  - Metal (copper, aluminum), insulators (silicon dioxide(SiO2) known as quartz glass), silicon (semiconductor or "partial" conductor)
  - Silicon IC: stacking different layers of materials in a specific order to form three dimensional structures

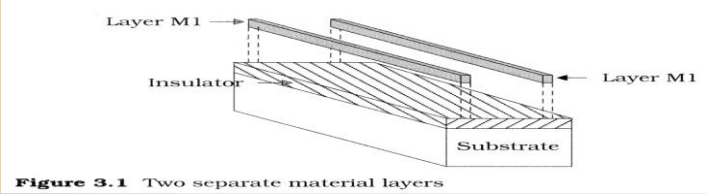


Figure 3.1 Two separate material layers

3.1 Integrated Circuit Layers

- Layers after the stacking process
  - VLSI chip: employ several conducting layers of aluminum or copper
  - Pattern conducting layers on the top of insulators
  - Insulators are often (assumed) omitted from top views (SiO2)

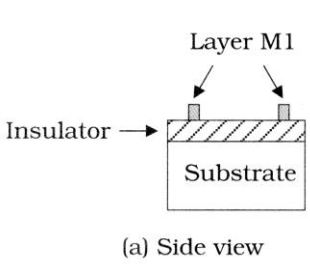


Figure 3.2 Layers after the stacking process is completed

5

3.1 Integrated Circuit Layers

- Add more layers
  - First, coat the surface with another of insulating glass
  - To provide a flat surface, do CMP (chemical-mechanical planarization)
    - Etched and sanded for a flat surface
  - Next, we coat the surface with the second metal layer (M2)
    - Two do not touch

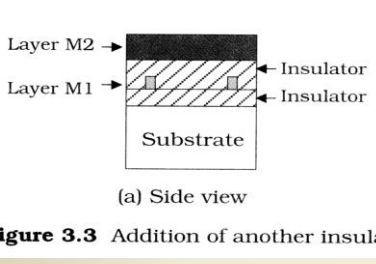


Figure 3.3 Addition of another insulator and a second metal layer

6

3.1 Integrated Circuit Layers

- Visualize the three-dimensional structure
  - The side view illustrate the order of the stacking
    - In the manufacturing process
  - Insulating layers separate the two metals so that they are electrically distinct
  - The patterning of each layer is shown by a top view perspective
    - By a VLSI designer

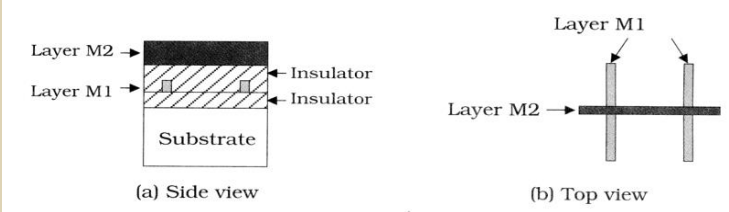
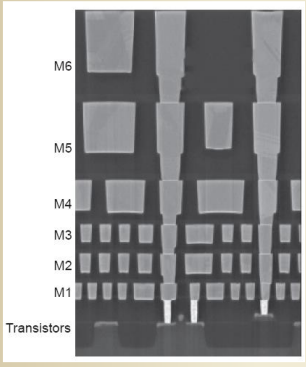


Figure 3.3 Addition of another insulator and a second metal layer

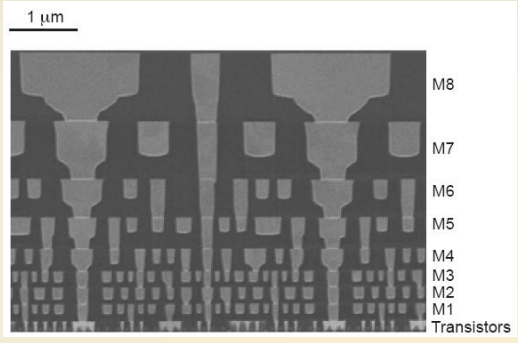
3.1 Integrated Circuit Layers

- Visualize the three-dimensional structure



Intel 90 nm Stack

[Thompson02]



Intel 45 nm Stack

[Moon08]

3.1 Integrated Circuit Layers

- The stacking order is established in the manufacturing process and can not be altered by the VLSI designer
- Creating the pattern for each layer is a critical part of the chip design sequence
  - It defines the locations and sizes of all MOSFETs and specifies how the transistors are connected together

3.1.1 Interconnect Resistance & Capacitance

- The logic gates communicate each other by wires (interconnects)
- Signal transfer speed is directly affected physical implementation of the wiring
  - Making it a very important of chip design.
- Resistance (R) measured by Ohm (Ω)
  - $V = I \cdot R$ ➔ $R = {}^{V}/_{I}$ (volts/amperes)
- Parasitic (unwanted) electrical element
- Line resistance R_{line} should keep as small as possible
- $R_{line} = \frac{l}{A\sigma}$,where σ is the conductivity
  - large σ means that the layer conducts well (see Fig 3.5)

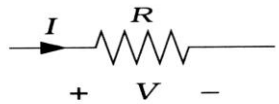


Figure 3.4 Symbol for a linear resistor

3.1.1 Interconnect Resistance & Capacitance

- Designer cannot control t or σ
- $R_{line} = \frac{l}{A\sigma} = \left(\frac{1}{\sigma t}\right) \cdot \left(\frac{l}{w}\right) = Rs \cdot \left(\frac{l}{w}\right)$
- If $l = w$, $R_{line} = R_s =$ sheet resistance
  - Unit/per ohms, or ohms per square
  - $R_{line} = R_s * n$,where $n = \frac{l}{w}$
- The line resist depends upon the ratio $(\frac{l}{w})$ of the patterned line

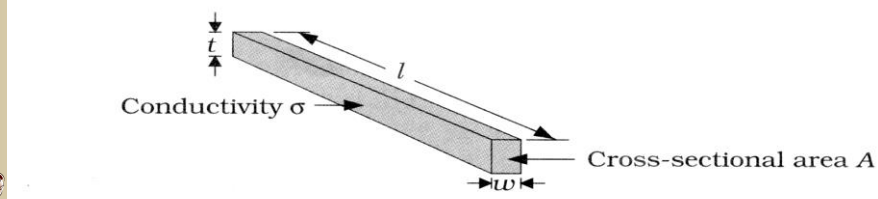
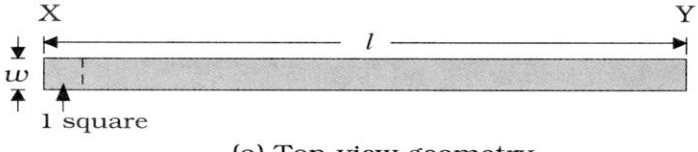


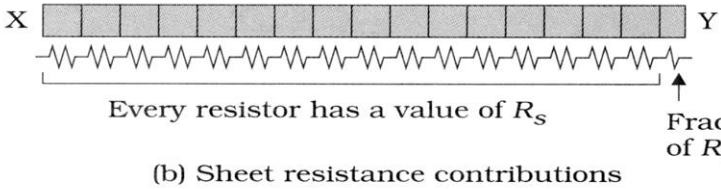
Figure 3.5 Geometry of a conducting line

3.1.1 Interconnect Resistance & Capacitance

- Compute the resistance of a wire



(a) Top-view geometry



(b) Sheet resistance contributions

Figure 3.6 Top-view geometry of a patterned line

3.1.1 Interconnect Resistance & Capacitance

- Capacitance: the ability to store electric charge and energy
  - $C = \frac{Q}{V}$ (1 farad = 1coulomb/volt).
- $I = C\frac{dV}{dt}$

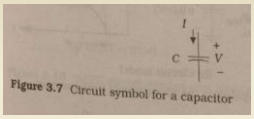


Figure 3.7 Circuit symbol for a capacitor

- Capacitance exists between any two conducting bodies that electrically separated
- Parallel-plate formula $C_{line} = \frac{\varepsilon_{ox} wl}{T_{ox}}$; wl is the area; ε_{ox} is the permittivity of insulating oxide with unit F/cm.
- Dielectric constant $\varepsilon_{ox} = k\varepsilon_0$
  - ε_0 = 8.85 x 10^{-14} F/cm
  - k = 3.9 for SiO_2
  - low-k dielectrics

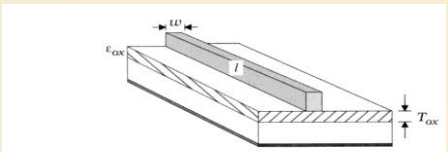


Figure 3.8 Geometry for calculating the line capacitance

high K 低leak，leak都被電容吃掉
low K 高leak

critical pass用low k

3.1.1 Interconnect Resistance & Capacitance

- Delay (Time constant)
  - Time constant $\tau = R_{line} * Cl_{ine}$
  - If $V_s(t)$ makes 0->1, $V(t)$ also rises but is delayed by τ and is not as sharp as V_s
  - VLSI processing are directed toward minimizing both R_{line} and C_{line} ➔ fast chip

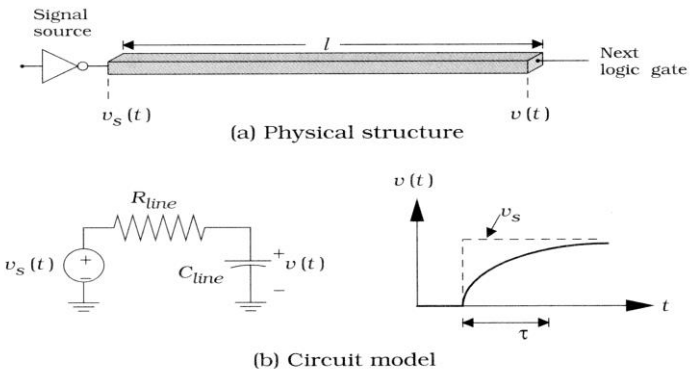
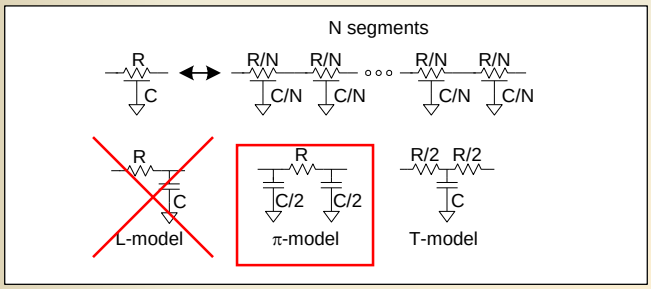


Figure 3.9 Time delay due to the interconnect time constant

3.1.1 Interconnect Resistance & Capacitance

- Lumped Element Models
- Wires are a distributed system
  - Approximate with lumped element models



- Use single segment π-model for Elmore delay

3.2 MOSFET

- What the MOSFET looks like at the physical level
- An MOSFET is a set of two basic patterned layers
- Use the concept of integrated circuit layers to create a silicon FET

3.2 MOSFET

- Recall the circuit symbol for an nFET shown in Figure 3.10(a)
- We have drawn a simple representation of the nMOS using conducting layers in 3.10(b)
  - The vertical line represents the gate layer and divides another layer into source and drain
- The gate G is responsible for the absence or presence between S and D.

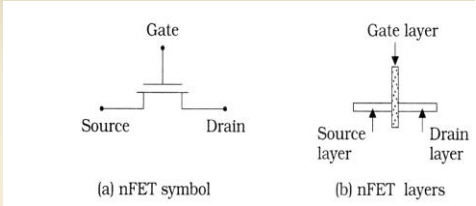


Figure 3.10 nFET circuit symbol and layer equivalents

Figure 3.11 Simplified operational view of an nFET

17

3.2 MOSFET

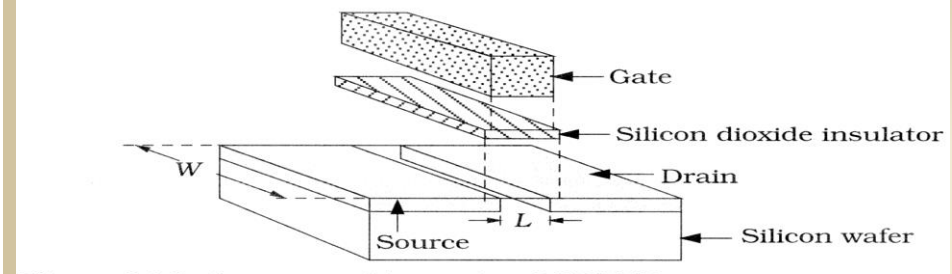


Figure 3.12 Layers used to create a MOSFET

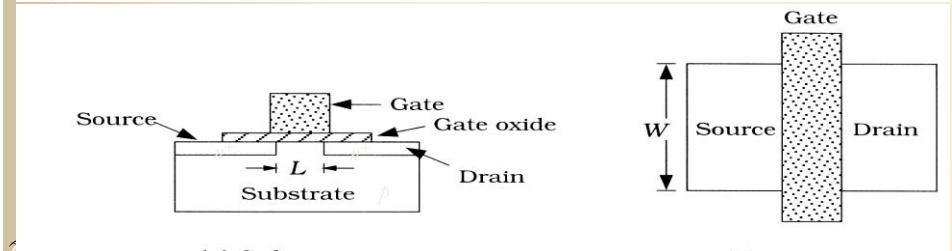


Figure 3.13 Views of a MOSFET

3.2 MOSFET

- Source and drain are on the same layer and separated by a distance called "channel length" *L*
- The width of the drain and source region is called the "channel width" W
- The aspect ratio of the FET is most important parameter to VLSI designer
  - $\frac{W}{L}$
- The gate layer is separated by a silicon dioxide (glass) layer acts as an insulator

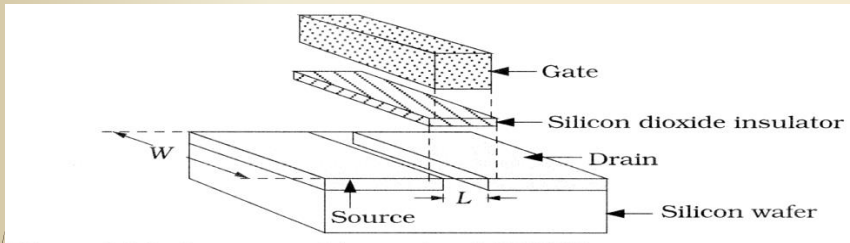


Figure 3.12 Layers used to create a MOSFET

3.2 MOSFET

- The 3-dimensional structure
- Silicon dioxide ➔ gate oxide
  - reside directly under the gate
- nFET and pFET is the same except that the layers used for the drain and source regions
- nFET has excess # of negatively charged electrons while pFET has positive charges

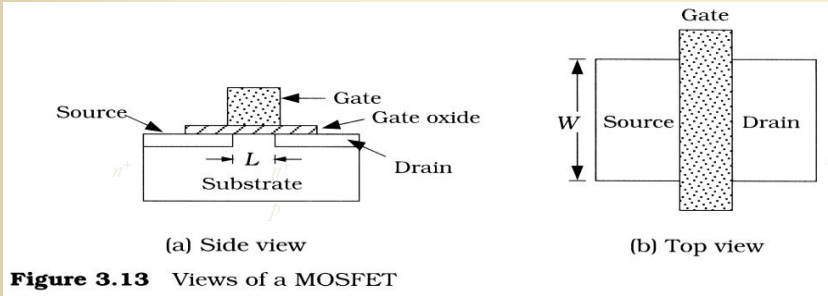
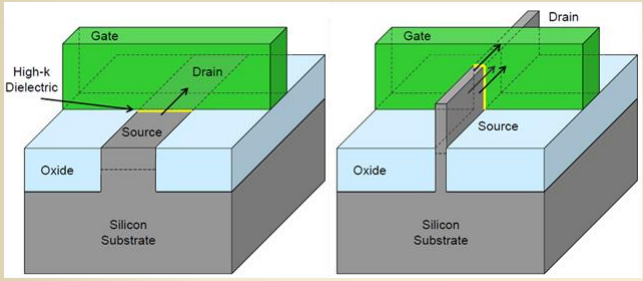
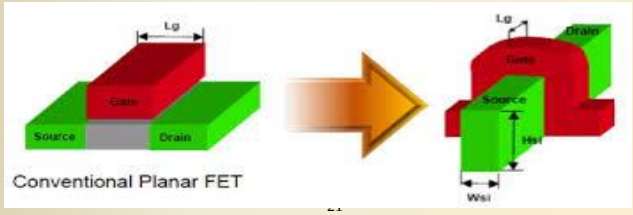


Figure 3.13 Views of a MOSFET

Appendix: Fin FET



Traditional 2D FET 3D FinFET



3.2.1 Electrical Conduction in Silicon

- Silicon is relative poor conductor (partial conductor)
- Only a small number of electrons are available to conduct electricity due to thermal excitations
- An electron gains sufficient energy to break away its atom, it becomes free and leaves behind a hole

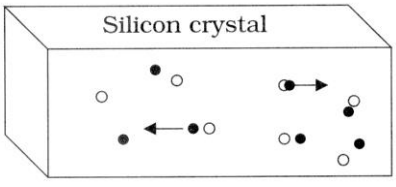


Figure 3.14 Creation of electron-hole pairs in silicon

22

3.2.1 Electrical Conduction in Silicon

- The ability of a material to conduct current depends on the number of free electrons and holes.
- Mass-action law: $np = {n_i}^2$
  - n: the number of free electrons per cm^3
  - p: the number of free hold per cm^3
  - $n_i = 1.45 * 10^{10}$.
- Pure silicon does not conduct well

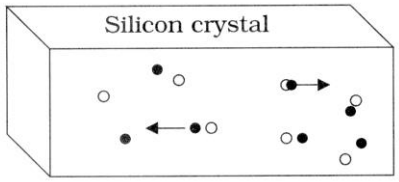
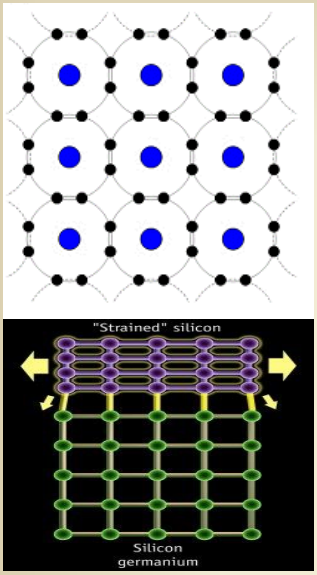
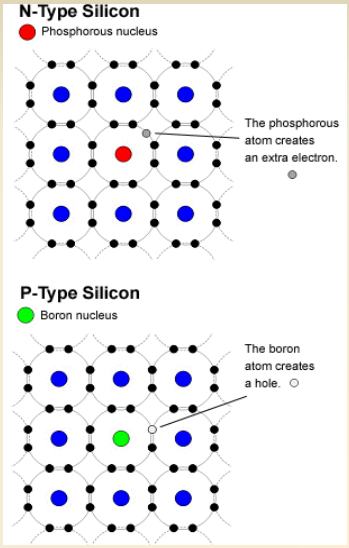


Figure 3.14 Creation of electron-hole pairs in silicon

3.2.1 Electrical Conduction in Silicon



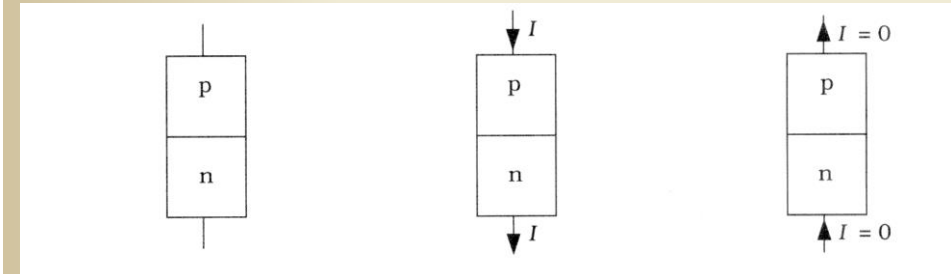


3.2.1 Electrical Conduction in Silicon

- n-type
  - Add donors: arsenic 五價砷 or phosphorus磷
  - Electrons are the majority carriers; μ_n =1360 (electron mobility)
  - $\sigma_n = q\mu_n n_n$; n_n: doping density of 五價 **越大，電阻越小，越易導電**
- p-type
  - Add acceptor: boron 三價硼
  - Holes are majority carriers; μ_p =480 (Hole mobility)
  - $\sigma_p = q\mu_p n_p$; n_p: doping density of 三價
- Doping density determines the conductivity in n-type or p-type silicon

3.2.1 Electrical Conduction in Silicon

- The pn junction allows conduction in only one direction (diode)



(a) A pn junction (b) Forward current (b) Reverse blocking

Figure 3.15 Formation and characteristics of a pn junction

3.2.2 nFETs and pFETs

- Define the structure of nFET and pFET
- Several PN junctions; all prevent unwanted current flow
- Choose p-substrate
  - nFET is built directly
  - pFET need n well

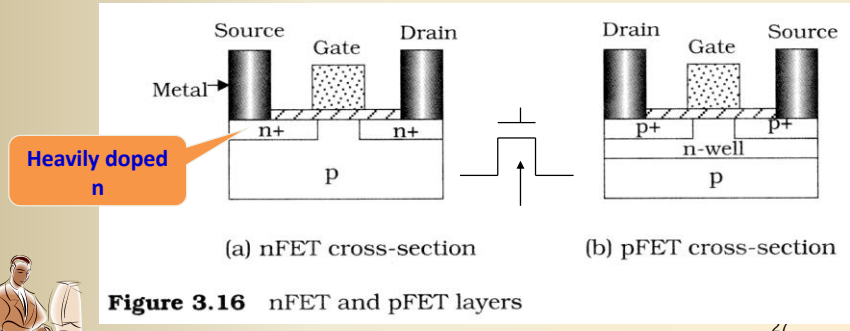
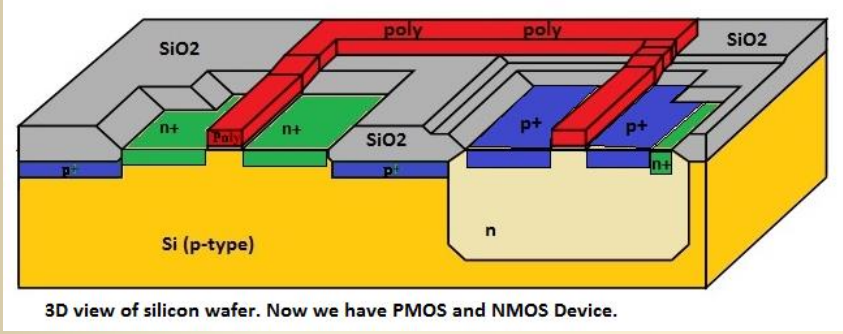


Figure 3.16 nFET and pFET layers

3.2.2 nFETs and pFETs



3D view of silicon wafer. Now we have PMOS and NMOS Device.

3.2.2 nFETs and pFETs

- n+ heavily doped with donors
- PN junctions are formed between n+ region and the p type substrate used to block current flow between the substrate and n+ layer
- p+ section are embedded in an n-type "well" layer.
- PN junctions all are used to prevent current flow

29

3.2.3 Current flow in a FET

- MOSFETs are voltage controlled switches
- The creation of conduction layer underneath the gate is due to the capacitance
- Polycrystal silicon, polysilicon, poly.

- Oxide capacitance
  - $C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}}$
- Gate capacitance
  - $C_G = C_{ox} * A_G$
- Permittivity
  - $\varepsilon_{ox} = 3.9 * \varepsilon_0$
  - $\varepsilon_0 = 8.85 * 10^{-14}$

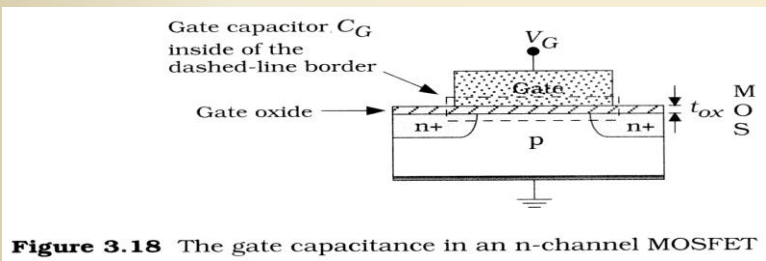


Figure 3.18 The gate capacitance in an n-channel MOSFET

3.2.3 Current flow in a FET

- N-type is physically separated by p-type substrate
- In (a), no current flow due to PN junction
- Applying a positive voltage to the gate in (b), induce electrons
- The formation requires the voltage larger than V_{Tn}

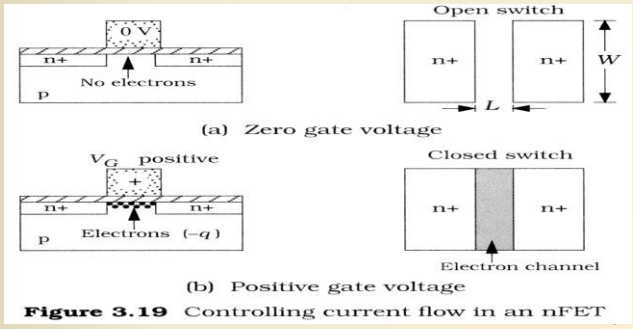


Figure 3.19 Controlling current flow in an nFET

3.2.3 Current flow in a FET

- Driving the current voltage equation
  - The formation requires $V_{gs} \geq V_{Tn}$
  - Current: $I_{dn} \cong \mu_n C_{ox} (\frac{W}{L})(V_G - V_{Tn})V_{DS}$
    - Electron mobility or surface mobility : μ_n
  - Device conductance : $\beta_n = \mu_n C_{ox} (\frac{W}{L})$:
  - Linear resistance : $R_n = \frac{1}{\beta_n(V_G - V_{Tn})}$

Q = CVol
Qc = Cg(Vgs - Vtn)
I = Qc / t
t = L / Vel
I = Cg(Vgs - Vtn) / (L / Vel)

- pFET behaves in a similar manner except the polarities are reversed
  - $\beta_p = \mu_p C_{ox} \left(\frac{W}{L}\right)$
  - $R_p = \frac{1}{\beta_n(V_G - |V_{Tp}|)}$

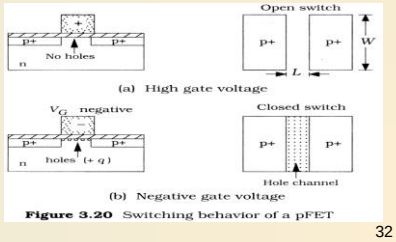


Figure 3.20 Switching behavior of a pFET

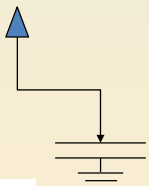
3.2.3 Current flow in a FET

- MOSFETs are non-linear device in that current *I* is a non-linear function of the voltage across it
- This relationship will be examined in more detail in Chapter 6
- For simple modeling, however, we often treat the transistor as a linear resistor

33

3.2.4 Driving the Gate Capacitance

- The value of the capacitance C_G determine the amount of charge necessary to charge the voltage, so a large capacitance implies a long delay
  - $Q=C_GV_G$
- Both the energy stored in a capacitor and the power dissipated is $E_e = \frac{1}{2}C_GVdd^2$
- Resistors dissipates power by changing it into heat
- Charge and discharge will be $2*E_e=C_GVdd^2$



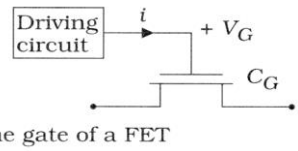


Figure 3.22 Driving the gate of a FET

34

3.2.4 Driving the Gate Capacitance

- Energy stored in capacitance C is E_e
- Energy provided from the Vdd is $2E_e$
- Energy loss during the transfer is E_e

$$P = V(C\frac{dV}{dt}) = \frac{d}{dt}(C\frac{V^2}{2})$$

$$E_e = \frac{1}{2}CV_{DD}^2$$

3.2.4 Driving the Gate Capacitance

- Computation causes switching
- Switching delay are due to the physical characteristics of the devices and interconnect
  - Understand the nature of switching for fast circuit
- Every switching event requires energy transfer in the circuit
  - This implies that power dissipation

3.3 CMOS Layers

- There are countless variations due to complicated manufacturing process
- We choose a rather simple process to study
  - n-well process　p當基底
- We have seen how patterned layers of materials are used to create nFET
- CMOS fabrication process
  - The sequence of steps that use to take a bare "wafer" of silicon to the finished form of an IC.
- The n-well process starts with a p-type substrate
  - nFET can be fabricated in the p-type substrate while n-well has to accommodate the pFETs

3.3 CMOS Layers

- From this drawing, we can identify the following layer types
  - p-substrate
  - n-well
  - n+ (nFET drain/source)
  - p+ (pFET drain/source)
  - gate oxide
  - gate (polysilicon)

field oxide
silcon oxide

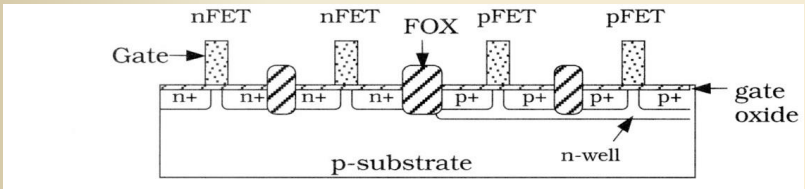


Figure 3.23 MOSFET layers in an n-well process

3.3 CMOS Layers

- Layer implies a region distinct electrical characteristics even though it may be physically at the same geometrical level
- **FOX**: Field OXide (silicon dioxide) to provide electrical isolation
- Once base transistor layers are defined, next, we add conducting layers

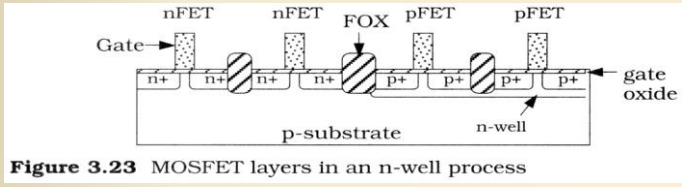


Figure 3.23 MOSFET layers in an n-well process

39

3.3 CMOS Layers

- The top view is shown in Figure 3.24
- FOX surrounds every transistor so there is an FOX everywhere except at the transistor site
  - Usually not shown explicitly

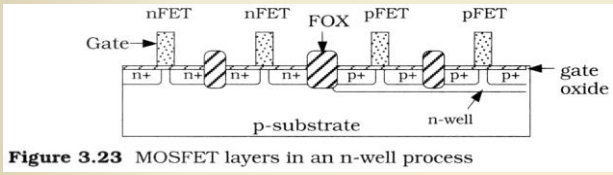


Figure 3.23 MOSFET layers in an n-well process

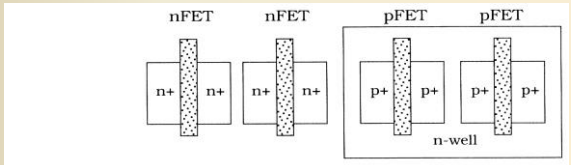


Figure 3.24 Top view FET patterning

40

3.3 CMOS Layers

- Metal interconnect layer
  - Modern process allow five or more metal interconnect layers to ease the problem of massive wiring in complex circuits
  - Metal layers are electrically isolated from each other.
  - A hole called **contact cut** is **etched** in the oxide
  - Electrical contact requires **contact cuts** and **vias**

metal跟metal叫via
metal跟substrate叫contact

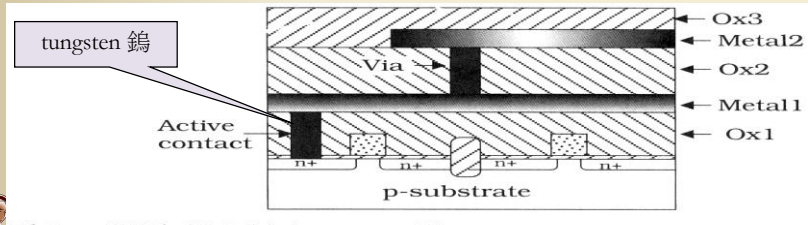


Figure 3.25 Metal interconnect layers

41

3.3 CMOS Layers

- These Imply that we can “cross" conducting layers without creating an electrical path between them
- Metal2 lines can cross over every other layer
  - a via is needed to contact M1

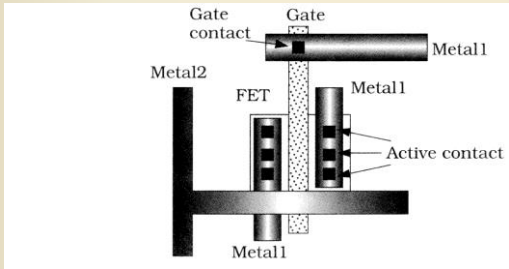


Figure 3.26 Interconnect layout example

3.3 CMOS Layers

- Metal interconnect layers
  - Metal to metal: via
  - Metal to the gate: gate contact
  - Metal to drain/source: active contact

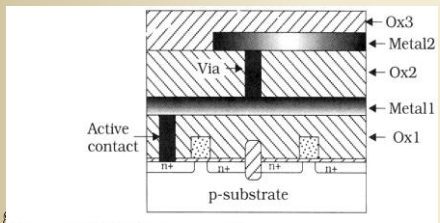


Figure 3.25 Metal interconnect layers

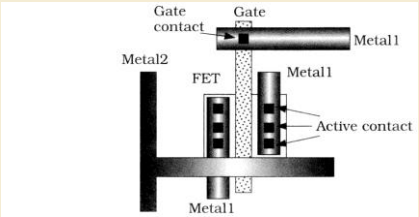


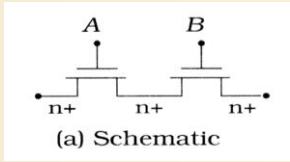
Figure 3.26 Interconnect layout example

3.3 CMOS Layers

- CMOS digital circuits
  - CMOS circuits are designed by creating **nFETs** and **pFETs** in silicon and then **wiring** them together using interconnect lines formed on the conducting layers
  - CMOS digital circuits consist **only** transistors and wires
  - No other devices are needed, regardless of the complexity of the system
- Once we learn how to design basic FETs and add the interconnect wiring, then we will understand the basics of CMOS VLSI!

3.4 Designing FET Arrays

- CMOS logic gats are switching networks that are controlled by the input variables
- These must be translated into silicon patterns for the final design
- Let us start with the simplest case of an n-stack where two nFETs are in series
  - Devices can share patterned regions to reduce layout area or complexity
  - Combine n+ regions
  - Color coding is easier



45

3.4 Designing FET Arrays

- Silicon patterning for series-connected nFETs

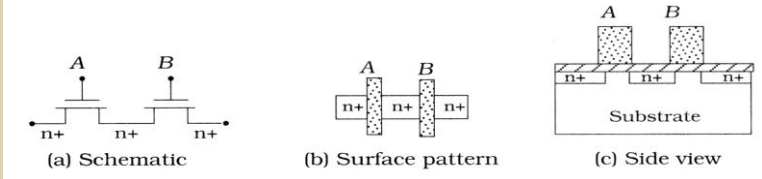


Figure 3.27 Silicon patterning for two series-connected nFETs

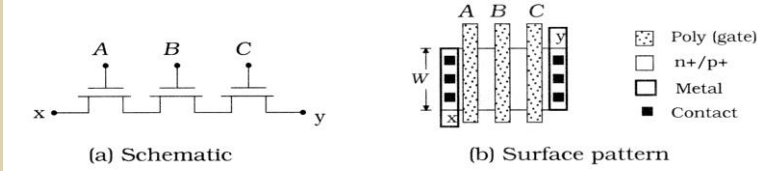
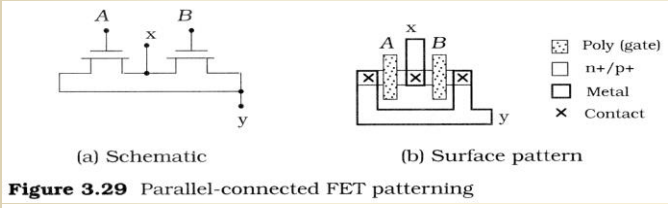


Figure 3.28 Three series-connected nFETs

46

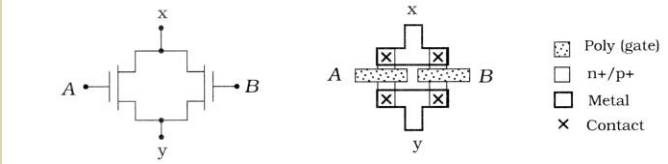
3.4 Designing FET Arrays

- Parallel-connected FETs can be patterned in the same manner



(a) Schematic (b) Surface pattern

Figure 3.29 Parallel-connected FET patterning



(a) Schematic (b) Surface pattern

Figure 3.30 Alternate layout strategy for parallel FETs

3.4.1 Basic Gate Designs

- For initial stage of crating a CMOS layout design, patterned lines on conducting layers are viewed as paths that "steer" electrical current and establish voltages
  - The widths of the lines are not important at this level
  - Only the topology of the network is needed to trace the logic
  - We are usually more interested in the **signal flow path** and the **circuit topology** than the details of the transistors
- Some of the important aspects
  - Both the **power supply (VDD)** and **ground (GND)** are routed using metal layer
  - N+ and p+ regions are denoted using the same fill pattern.
    - pFETs are embedded within an n-well boundary.
  - Contacts are needed from metal to n+ or p+ since they are at different levels in the structure

IR drop, VDD離太遠

3.4.1 Basic Gate Designs

- Translating a NOT gate circuit to silicon

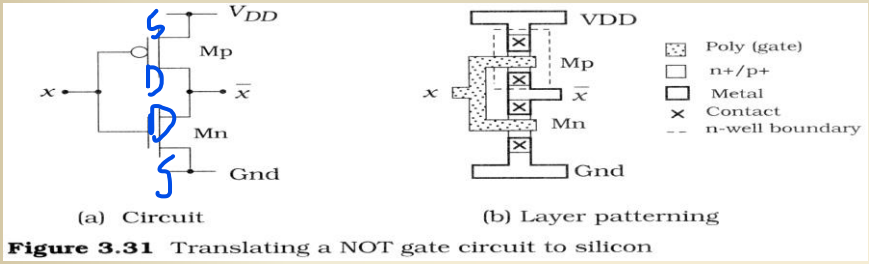


Figure 3.31 Translating a NOT gate circuit to silicon

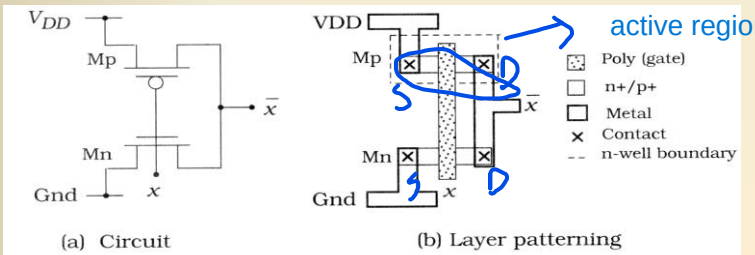


Figure 3.32 Alternate layout for a NOT gate

active region

能share Vdd or Gnd就share降低area

3.4.1 Basic Gate Designs

- One goal of physical design is to minimize the area of overall chip area
- Two NOT circuits share the same power supply and ground to reduce area

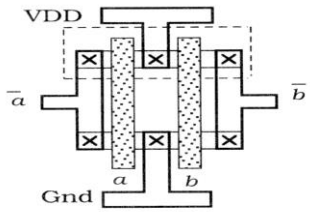
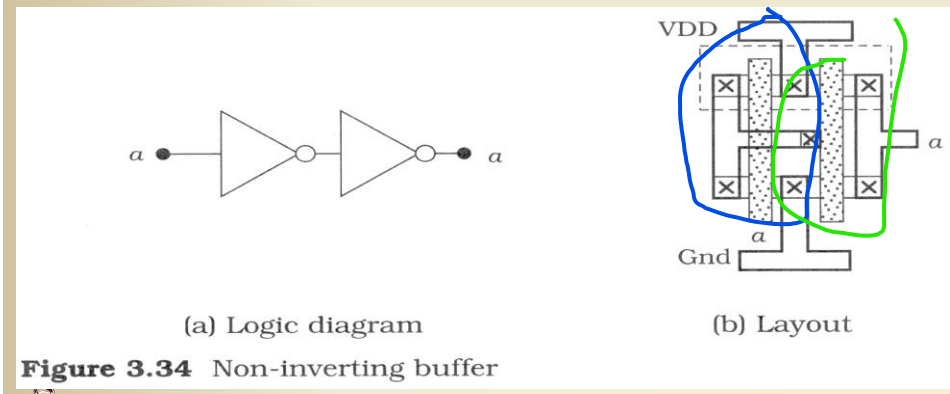


Figure 3.33 Two NOT gates that share power supply and ground

3.4.1 Basic Gate Designs

- Non-inverting buffer



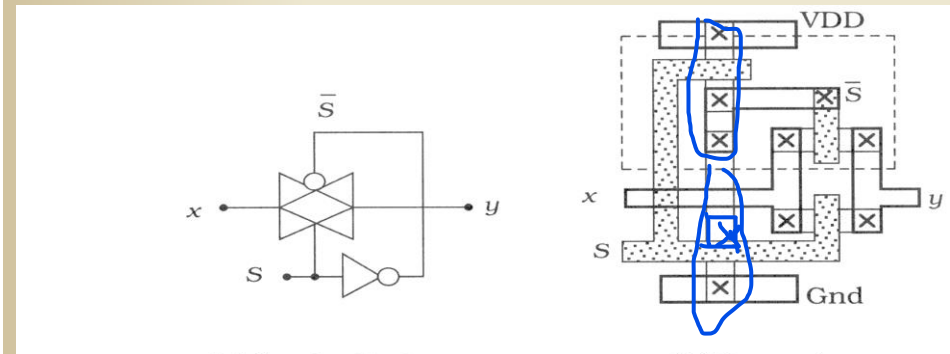
(a) Logic diagram (b) Layout

Figure 3.34 Non-inverting buffer

51

3.4.1 Basic Gate Designs

- Layout of a transmission gate with a driver
  - Interconnect routing problems



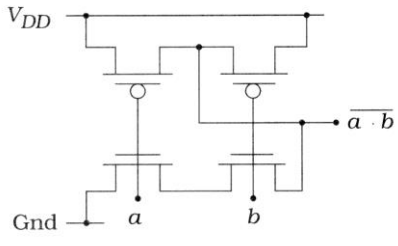
(a) Logic diagram (b) Layout

Figure 3.35 Layout of a transmission gate with a driver

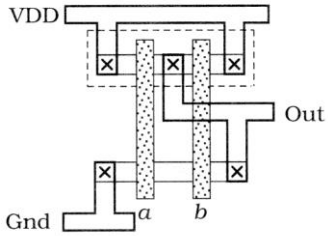
52

3.4.1 Basic Gate Designs

◆NAND2



(a) Circuit

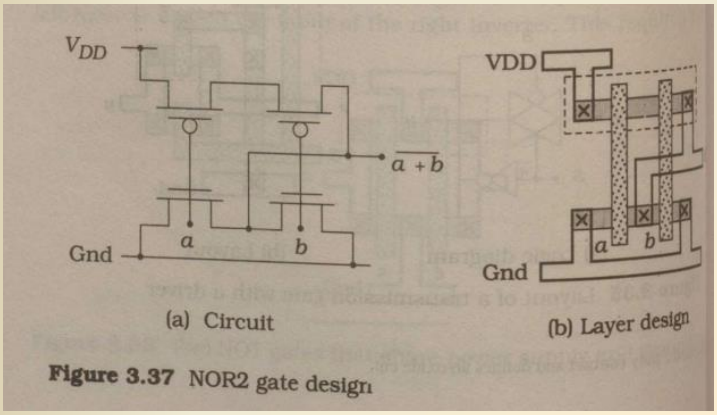


(b) Layer design

Figure 3.36 NAND2 layout

3.4.1 Basic Gate Designs

◆NOR2



(a) Circuit

(b) Layer design

Figure 3.37 NOR2 gate design

3.4.1 Basic Gate Designs

◆NAND2-NOR2 layout comparison

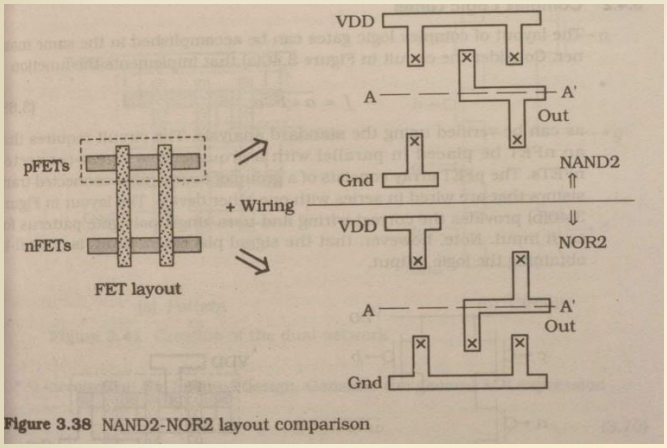
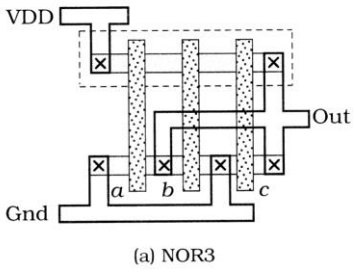


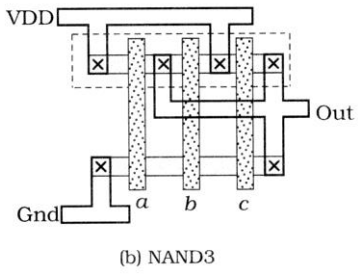
Figure 3.38 NAND2-NOR2 layout comparison

3.4.1 Basic Gate Designs

◆Layout for 3-input gates



(a) NOR3



(b) NAND3

Figure 3.39 Layout for 3-input gates

3.4.2 Complex Logic Gates

- Consider the circuit that implements the function $f = \overline{a + b \cdot c}$

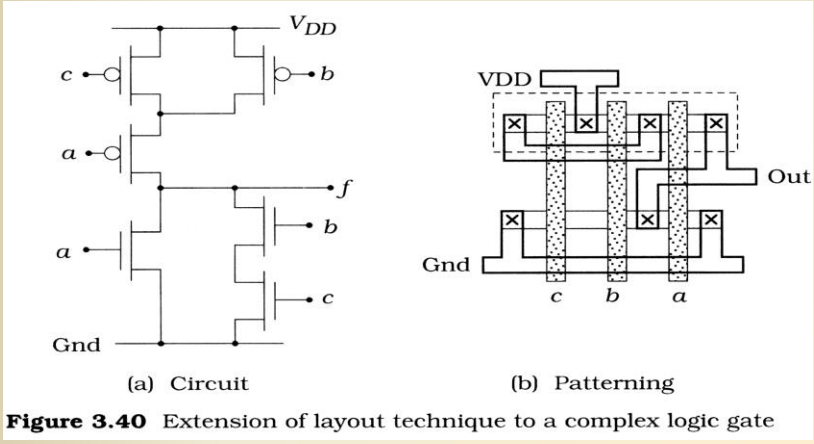


Figure 3.40 Extension of layout technique to a complex logic gate

3.4.2 Complex Logic Gates

- Suppose that we flip the metal wiring pattern around an imaginary horizontal line
- Tracing out the circuit yields the schematic in Figure 3.41(b)
  - $g = \overline{a \cdot (b + c)}$
  - Logical dual of f

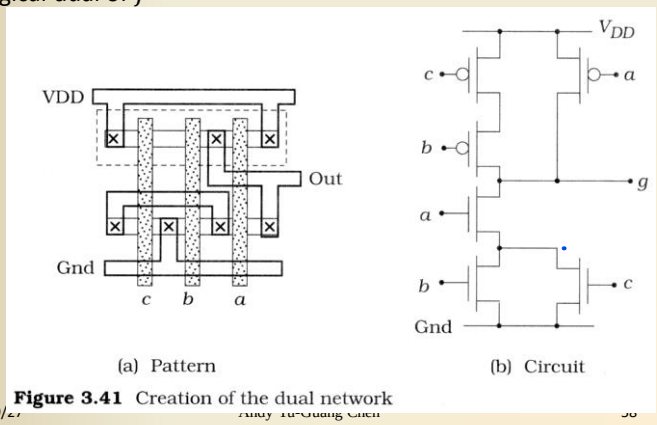


Figure 3.41 Creation of the dual network

3.4.2 Complex Logic Gates

- General AOI expression $F = \overline{x \cdot y + z \cdot w}$

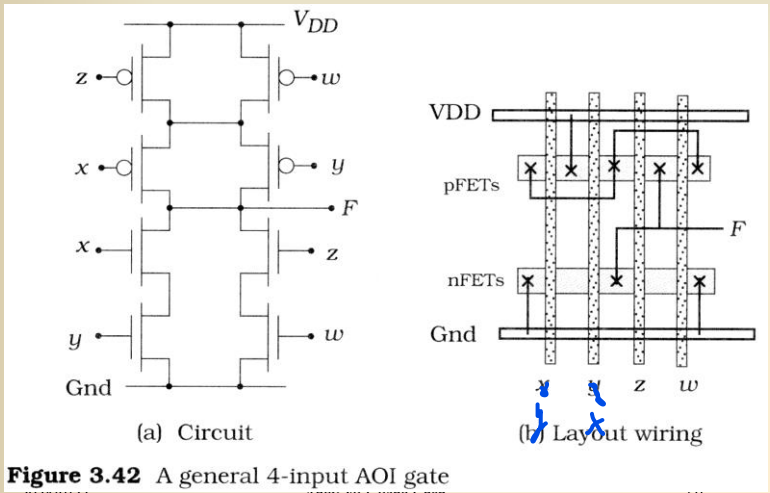


Figure 3.42 A general 4-input AOI gate

3.4.3 General Discussion

- It is possible to share n+ and p+ regions to reduce area
  - This is not always possible, especially in complicated arrangements
- Regular patterns yields the best packing density
- Every gate requires a VDD and VSS which runs into horizontal metal lines

3.4.3 General Discussion

- General gate layout geometry

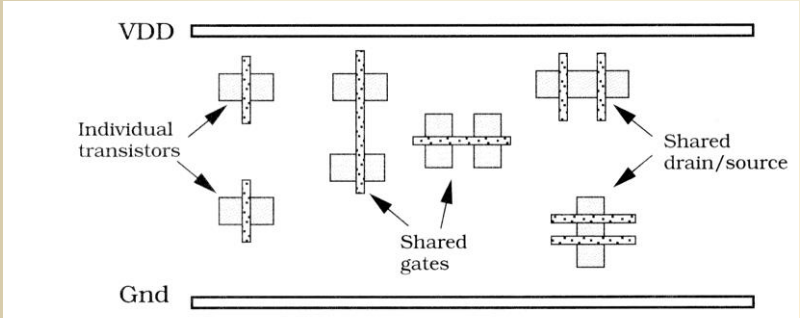


Figure 3.43 General gate layout geometry

3.4.3 General Discussion

- Simple **stick diagrams**
  - Each layer is represented by a distinct color
    - the drawing can be monochrome and layers have been represented by different line features such as varying the linewidth or using a dashed line
  - The routing consists of colored lines that obey the rules of chip formation
- Most commonly used colors
  - Polysilicon (gates): Red
  - Doped n+/p+ (active): Green
  - N-Well: Yellow (varies)
  - Metal 1: Blue
  - Metal2: Grey (varies)
  - Contacts: Black X's

3.4.3 General Discussion

- Basic stick layout diagram

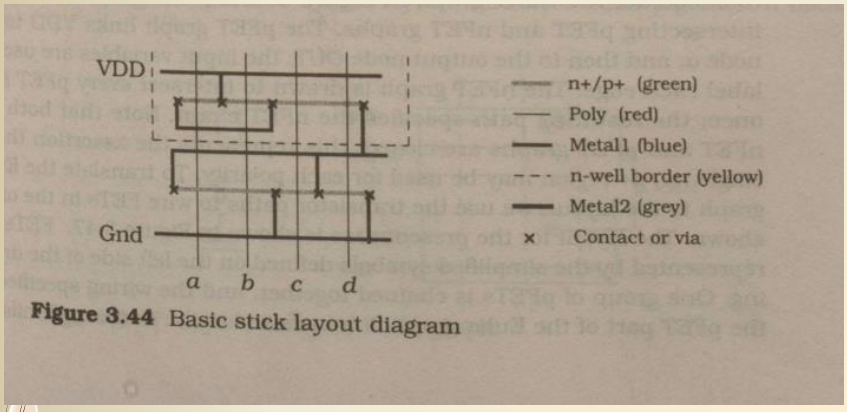


Figure 3.44 Basic stick layout diagram

3.4.3 General Discussion

- Rules
  - A red line crossing a green line creates a transistor
  - Red over green inside a yellow border region is a pFET; otherwise it is an nFET
  - Red may cross blue or grey
  - Blue may cross red, green, or gray
  - Grey may cross red, green, or blue
  - Transistor contacts must be placed from blue to green
  - Vias must be specified to contact blue to grey
  - A (poly) contact must be used to connect blue to red

3.4.3 General Discussion

- A more structured technique is to apply graph theory
  - Using graph element to represent a FET

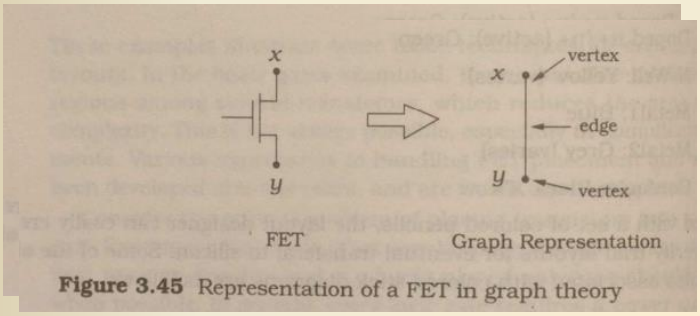


Figure 3.45 Representation of a FET in graph theory

3.4.3 General Discussion

- Euler graphs aid in the placement and wiring of circuits when transistors have shared drain/source regions
- Eulerian path
  - The path starts at the vertex shown and follows the arrow to the end vertex, and passes over every edge only once

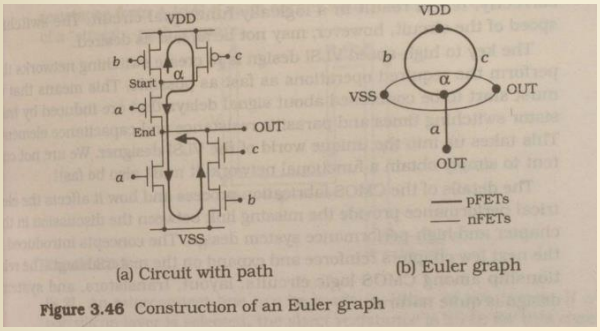


Figure 3.46 Construction of an Euler graph

3.4.3 General Discussion

- Layout using an Euler graph

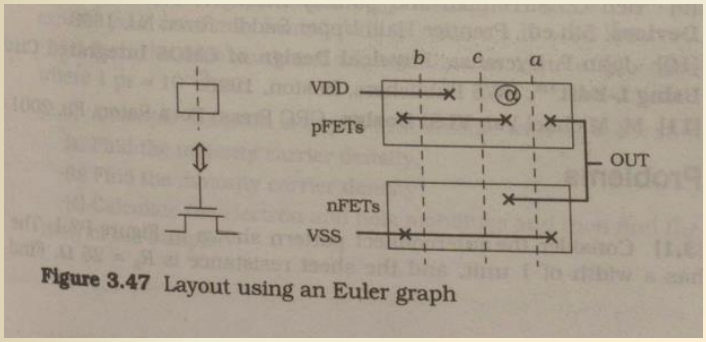


Figure 3.47 Layout using an Euler graph

Summary

- In this chapter we have seen the basics of translating FET logic circuits to silicon
- The layout considerations presented here are sufficient to create complex logic networks using a set of standard MOSFETs as building blocks
- In many designs it is possible to simply place reasonably sized transistors as specified by the layout, and wire them together
- The key to high-speed VLSI design is to create switching network perform the required operations as fast as possible
- This takes us into the unique world of the VLSI designer. We are not content to simply obtain a functional network: it must also be fast!
- The concepts introduced the next few chapters reinforce and expand on the material here

Q&A

Andy, Yu-Guang Chen
Assistant Professor, Department of EE, NCU
Email: andyygchen@ee.ncu.edu.tw
FB: Yu-Guang Chen
IG: ncu.eda.andy
Google account: andyygchen.ncu