# CS3120 Introduction of Integrated Circuit Design

# Chapter 3 Exercise

## 3.6 Problems

**[3.1]** Consider the interconnect pattern shown in Figure P3.1. The line has a width of 1 unit, and the sheet resistance is $R_s$ = 25 Ω. Find the resistance from A to B if each corner square contributes a factor of 0.625 of a "straight-path" square.

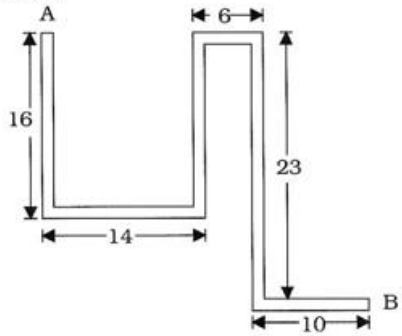


**Figure P3.1**

**[3.2]** An interconnect line can be made in either of two layers. If a gate polysilicon layer is selected, the sheet resistance is 25 Ω; for this case, the interconnect will have a width of 0.5 μm and a length of 27.5 μm. A metal layer can also be used. It has a sheet resistance of 0.08 Ω. The metal line has a width of 0.8 μm but requires a different routing length of 32.4 μm.

Calculate the line resistance $R_{line}$ for each case and determine the lower resistance alternate. What is the percentage increase in resistance if the larger resistance line is used instead?

**[3.3]** An interconnect line is made from a material that has a resistivity of ρ = 4 μΩ-cm. The interconnect is 1200 Å thick, where 1 Angstrom (Å) is $10^{-8}$ cm. The line has a width of 0.6 μm.

(a) Calculate the sheet resistance $R_s$ of the line.

(b) Find the line resistance for a line that is 125 μm long.

**[3.4]** Consider equation (3.14) for the interconnect time constant τ. Prove that τ has units of seconds by expressing ohms and farads in fundamental MKS units and reducing.

**[3.5]** An interconnect line runs over an insulating oxide layer that is 10,000 Å thick. The line has a width of 0.5 μm and is 40 μm long. The sheet resistance is known to be 25 Ω.

(a) Find the line resistance $R_{line}$.

(b) Find the line capacitance $C_{line}$. Use $\varepsilon_{ox} = 3.453 \times 10^{-13}$ F/cm, and express your answer in femtofarads (fF) where 1 fF = $10^{-15}$ F.

(c) Find the time constant τ for the line in units of picoseconds (ps) where 1 ps = $10^{-12}$ sec.

**[3.6]** A sample of silicon is doped with arsenic with $N_d = 4 \times 10^{17}$ cm$^{-3}$.

(a) Find the majority carrier density.

(b) Find the minority carrier density.

(c) Calculate the electron and hole mobilities and then find the conductivity of the sample.

**[3.7]** A region of silicon is doped with both phosphorus and boron. The P-doping is $N_d = 2 \times 10^{16}$ cm$^{-3}$ while the B-doping level is $N_a = 6 \times 10^{18}$ cm$^{-3}$. Determine the polarity (n or p) of the region, and find the carrier densities.

**[3.8]** A sample of silicon is doped with boron atoms at an acceptor density of $N_a = 4 \times 10^{14}$ cm$^{-3}$.

(a) Find the majority and minority carrier densities.

(b) Find the resistivity ρ of the sample.

(c) Suppose that the region has dimensions of 2 μm × 0.5 μm × 100 μm. Find the largest resistance of an end-to-end block of the region.

**[3.9]** Consider a doped semiconductor where

$$\sigma = q(\mu_n n + \mu_p p) \tag{3.71}$$

and $np=n_i^2$. Suppose we wish to minimize the conductivity.

(a) Use the mass-action law to write in terms of $p$ only.

(b) Compute the derivative ($d\sigma/dp$) and set it equal to 0 to find the hole concentration that minimizes σ.

(c) Noting that $\mu_n > \mu_p$, what polarity (n-type or p-type) is required for the highest resistivity? Then use your equations to find the doping type and density that give the highest resistivity.

**[3.10]** An n-channel MOSFET has a mobility value of $\mu_n = 560$ cm$^2$/V-sec and uses a gate oxide with a thickness of $t_{ox} = 90$ Å. The gate voltage is given as $V_G = 2.5$ V, and the threshold voltage is 0.65 V.

(a) Calculate the value of $C_{ox}$ in units of F/cm$^2$.

(b) Find the process transconductance $k'_n$.

(c) Find the device transconductance $\beta_n$ if the FET has a channel length of 0.25 μm and a channel width of 2 μm.

**[3.11]** Use equation (3.57) for $R_n$ to find the units of the electron mobility $\mu_n$.Then suppose that $\mu_n = 500$ cm$^2$/V-sec and $(V_G - V_{Tn}) = (3.3 - 0.7)$ V is known.

(a) Find the nFET resistance if $W = 10$ μm, $L = 0.5$ μm, and $t_{ox} = 10$ nm.

(b) Find $R_n$ if the channel width is increased to a value of $W = 22$ μm while the channel length remains the same.

**[3.12]** A pFET is described by $\mu_p = 220$ cm$^2$/V-sec and $(V_G - |V_{Tp}|) = (3.3 - 0.8)$ V, $W = 14$ μm, $L = 0.5$ μm, and $t_{ox} = 11.5$ nm. Find the pFET resistance $R_p$ of the device.

**[3.13]** Consider a process that has an oxide thickness of $t_{ox} = 9.5$ nm. The particle mobilities are given as $\mu_n = 540$ and $\mu_p = 220$ cm$^2$/V-sec. An nFET and a pFET are made, both with $W = 12$ μm, $L = 0.35$ μm. Both have gate voltages of $V_G = 3.3$ V, while the threshold voltages are $V_{Tn} = 0.65$ V and $V_{Tp} = -0.74$ V.

(a) Find the values of $R_n$ and $R_p$ for the two transistors.

(b) Suppose that we want to keep the nFET the same size, but increase

the width of the pFET to the point where $R_p = 0.8\ R_n$. Find the required width of the pFET.

**[3.14]** Design a CMOS logic gate that provides the function

$$Out = \overline{x \cdot (y \cdot z + z \cdot w)} \tag{3.72}$$

Then perform the basic layout of circuit.

**[3.15]** Design the circuit and layout for a CMOS gate that implements the function

$$F = \overline{a \cdot b \cdot c + a \cdot d} \tag{3.73}$$

using the fewest number of transistors and a compact layout style.

**[3.16]** Consider the OAI logic function

$$g = \overline{(a + b) \cdot (c + d) \cdot e} \tag{3.74}$$

Design the CMOS logic gate and then construct a basic layout for the circuit.

**[3.17]** Expand the function $g$ given in equation (3.74) [Problem 3.16 above] into AOI form. Then design the CMOS logic circuit and layout.

**[3.18]** Examine the stick diagram in Figure 3.44. Is this a functional logic gate? If so, determine the logic operation it provides.

**[3.19]** Consider the logic function

$$g = \overline{a \cdot b \cdot c + d} \tag{3.75}$$

(a) Design the CMOS logic gate that provides this function.

(b) Is it possible to find an Euler graph for the circuit? If so, construct the graph and use it to perform a stick-level layout. If not, find a layout strategy for the gate.