CS3120 Introduction of Integrated Circuit Design

Chapter 6 Exercise

[6.1] A CMOS process produces gate oxides with a thickness of t_{ox} = 100 Å. The FET carrier mobility values are given as μ_n = 550 cm^2/V-sec and μ_p = 210 cm^2/V-sec.

(a) Calculate the oxide capacitance per unit area in units of fF/μm^2.

(b) Find the process transconductance values for nFETs and pFETs. Place your answer in units of $\mu A/V^2$.

[6.2] An nFET with W = 10 μm and L = 0.35 μm is built in a process where k'_n = 110 $\mu A/V^2$ and V_{Tn} = 0.70 V. Assume V_{SBn} = 0 V.

(a) Find the current if the voltages are set to V_{GSn} = 2 V, V_{DSn} = 1.0 V.

(b) Find the current if the voltages are set to V_{GSn} = 2 V, V_{DSn} = 2 V.

[6.3] An nFET has a device transconductance of β_n = 2.3 mA/V^2 and a threshold voltage of 0.76 V. Assume V_{SBn} = 0 V.

(a) Find the current if the voltages are set to V_{GSn} = 1 V, V_{DSn} = 2.5 V.

(b) Find the current if the voltages are set to V_{GSn} = 2 V, V_{DSn} = 2.5 V.

(c) Find the current if the voltages are set to V_{GSn} = 3 V, V_{DSn} = 2.5 V.

[6.4] Consider a pFET that has a gate oxide thickness of t_{ox} = 60 Å. The hole mobility is measured to be 220 cm^2/V-sec, and the aspect ratio is (W/L) = (12/1). Assume that V_{DD} = 3.3 V and $|V_{Tp}|$ = 0.7 V.

(a) Calculate the process transconductance k'_p in units of mA/V^2

(b) Find the device transconductance β_p and the resistance R_p

[6.5] An nFET has a gate oxide with a thickness of t_{ox} = 120 Å. The p-type bulk region is doped with boron at a density of $N_a = 8 \times 10^{14}$ cm^{-3}. given that V_{T0n} = 0.55 V and (W/L) = 10. $N_a = 8 \times 10^{-14} cm^{-3}$

(a) Calculate the body bias coefficient γ.

(b) What is the device threshold voltage if a body bias voltage of V_{SBn} = 2 V is applied?

(c) The electron mobility is μ_n = 540 cm^2/V-sec. Calculate the drain current with bias voltages of V_{GSn} = 3 V, V_{DSn} = 3 V, and V_{SBn} = applied to the device. $V_{SBn} = 3V$

[6.6] Construct the RC switch model for the FET layout in Figure P6.1. Assume a power supply voltage of 3 V and that the dimensions are units of microns.

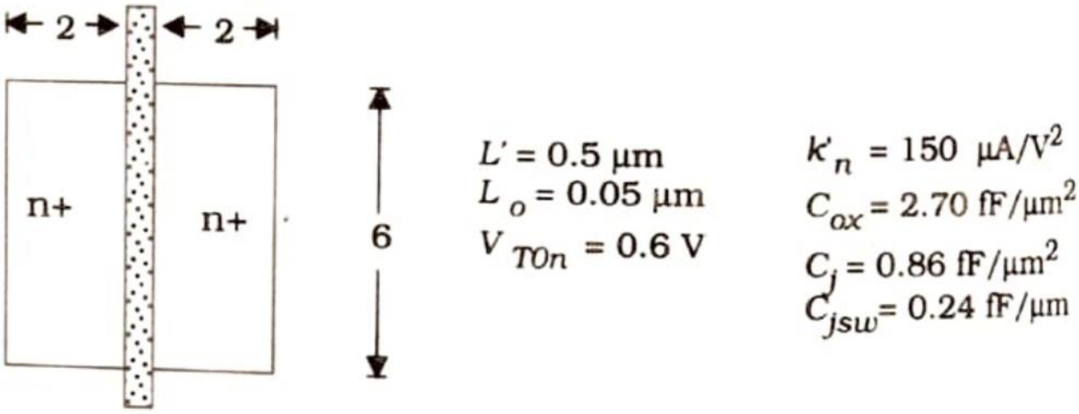

Figure P6.1 Transistor layout geometry for Problem 6.6

[6.7] Write a SPICE description of the nFET in Figure P6.1. Use your listing to obtain the family of I_D versus V_{DS} curves.

[6.8] Consider the FET geometry shown in Figure P6.1 where the sheet resistance of the n+ regions is 30 Ω, and the poly gate has a sheet resistance of 26 Ω. Compute the parasitic resistances R_{n+} and R_{poly} associated with these parameters by determining the appropriate geometry that applies for each. How would these parasitics affect the device operation

[6.9] An nFET with $W = 20\ \mu m$ and $L = 0.5\ \mu m$ is built in a process whe $k'_n = 120\ \mu A/V^2$ and $V_{Tn} = 0.65$ V. The voltages are set to a value of V_{GS} $V_{DSn} = V_{DD} = 5$ V. $V_{GS} =$

(a) Is the transistor saturated or non-saturated?

(b) Calculate the drain-source resistance using the proper equation the transistor.

(c) Compare your value in (b) with that found using equation (6. with a value of $\eta = 1$.

[6.10] An nFET with $L = 0.5\ \mu m$ is built in a process where $k'_n = 100\ \mu$ $= 100\mu A/$ V^2 and $V_{Tn} = 0.70$ V. The gate-source voltage is set to a value of V_{GS} $V_{GS} =$ $V_{DD} = 3.3$ V. Calculate the required channel width to obtain a resistance $R_n = 950\ \Omega$ using equation (6.71) with for a value of $\eta = 1$.