CS3120
Introduction of Integrated Circuit Design

Chap 5
Elements of
Physical Design

Andy, Yu-Guang Chen
Associate Professor, Department of EE, National Central University
Adjunct Assistant Professor, Department of CS, National Tsing Hua University
andyygchen@ee.ncu.edu.tw

Outline

- 5.1 Basic Concept
- 5.2 Layout of Basic Structure
- 5.3 Cell Concept
- 5.4 FET Sizing and the Unit Transistor
- 5.5 Physical Design of Logic Gates
- 5.6 Design Hierarchies

Elements of Physical Design

- In the previous chapter, we examined the basic fabrication sequence
- In this chapter, study the details of translating logic circuits into silicon called **physical design**
  - Details such as the minimum size specifications allowed for a patterned region become critical
  - The use of CAD tools and database structures that describe the silicon masks

5.1 Basic Concept

- Physical design
  - Creating circuits on silicon
  - Schematic diagrams are translated into sets of geometric patterns
  - Every layer is defined by a distinct pattern
- The topology of the transistor network establishes the logic function

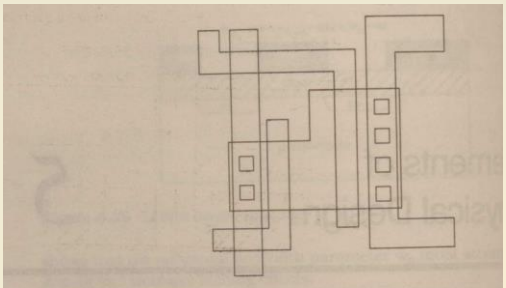


Figure 5.1 Examples of polygons in physical design

5.1 Basic Concept

- The process of physical design is performed using tool called layout editor
- Specify the shape, dimensions and placement of every polygon on every layer of the chip
- Reduce the complexity by using the concept of library
- Library cells are used as building blocks by creating copies of the basic cells.
  - A copy of a cell is called an instance

5.1 Basic Concept

- Designer's goal is to obtain a fast circuit in the minimum amount of area
- Small changes in the shape will affect the electrical characteristics of the circuit
- Circuit simulation also help to insure that the layout is accurate and provides a network that meets specification

5.1.1 CAD toolsets

- Layout editor: draw transistors and wiring patterns made up of polygon. Each layer has a distinct color or fill pattern on the screen.
- The electrical behavior of the design is simulated by first using an extraction tool which translate the polygon patterns into equivalent electrical network in SPICE format.
- Extraction provide important parameters such as the drawn channel width and length for each FET. And how transistors are wired together.

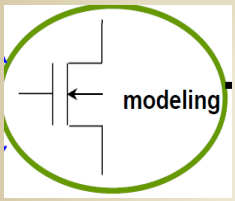
5.1.1 CAD toolsets

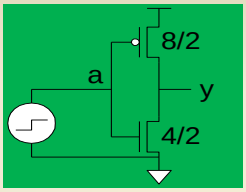
- Circuit simulation by SPICE.
- **Layout versus schematic (LVS)**: check the layout against the schematic diagram. To verify the layout corresponds the intended circuit.
- **Design rule checker (DRC)**: check every occurrence of the design rule list on the layout. Design can fabricated within the limitation of the process.

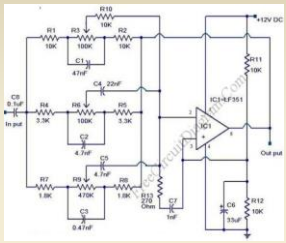
Introduction to SPICE

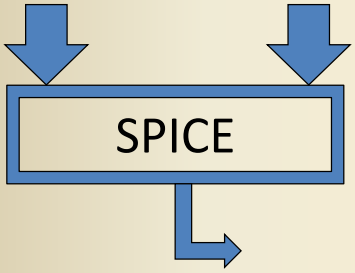
- **S**imulation **P**rogram with **I**ntegrated **C**ircuit **E**mphasis
  - Developed in 1970's at Berkeley
  - Many commercial versions are available
  - HSPICE is a robust industry standard
    - Has many enhancements that we will use

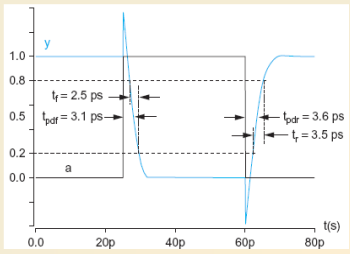
SPICE











SPICE

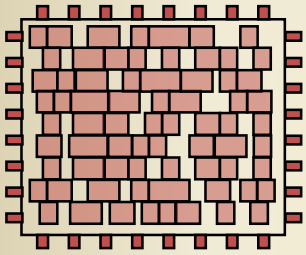
- Take a text netlist describing the circuit elements (transistors, resistors, capacitors, etc.) and their connections, and translate this description into equations to be solved.
- The general equations produced are nonlinear differential algebraic equations which are solved using implicit integration methods, Newton's method and sparse matrix techniques.

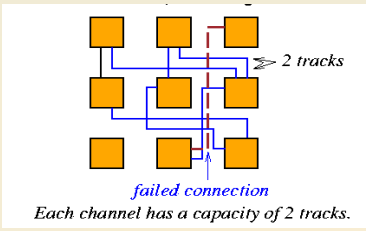
Writing SPICE Decks

- Writing a SPICE deck is like writing a good program
  - Plan: sketch schematic on paper or in editor
    - Modify existing decks whenever possible
  - Code: strive for clarity
    - Start with name, email, date, purpose
    - Generously comment
  - Test:
    - Predict what results should be
    - Compare with actual
    - *Garbage In, Garbage Out!*

5.1.1 CAD toolsets

- Place and Routing (P&R): find viable routing for a net.

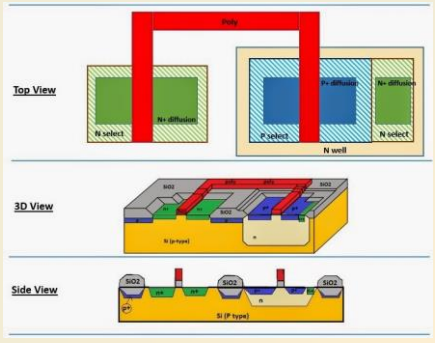




- Electrical rule checker (ERC): Electrical continuity can be seen using ERC

5.2 Layout of Basic Structure

- The mask sequence (Based on p-substrate (n-well) technology)
  - Start with p-type substrate
  - nWell
  - Active (Diff)
  - Poly
  - pSelect (pImp)
  - nSelect (nImp)
  - Active contact
  - Poly contact
  - Metal1
  - Via
  - Metal2
  - Overglass



5.2 Layout of Basic Structure

- Study how to design basic structures on the chip such as n+ and p+ regions and MOSFETs using the basic masking sequence.
- The actual values for minimum line width *w* and minimum line spacing *s* depend on the layer
  - Design rules apply only to the features on the mask (a generic term for the reticle) for that layer.
- The layout sizes as the **drawn** value while the resulting size on the finished chip have effective or final value
- Our discussion will consider only Manhattan geometries where all turns are multiples of 90°.
  - Manhattan is not necessary

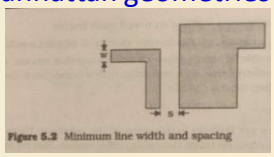


Figure 5.2 Minimum line width and spacing

5.2.1 n-Wells

- An n-well is required for a pFET
  - nwell mask
- Design rules
  - W_{nw} = minimum width of an n-well mask feature
  - $S_{nw\text{-}nw}$ = minimum edge-to-edge spacing of adjacent n-wells
- N-well must have a connection to the power V_{DD}

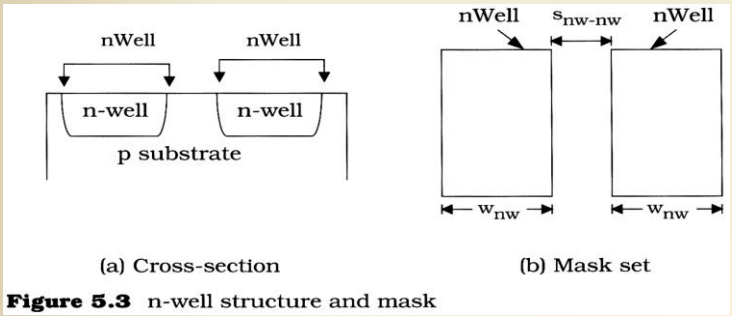


Figure 5.3 n-well structure and mask

5.2.2 Active Areas

- Silicon devices are built on active areas of the substrate
  - Active mask
- Design rules
  - W_a = minimum width of an Active feature
  - $S_{a\text{-}a}$ = minimum edge-to-edge spacing of Active mask
- FOX = NOT (Active)
- FOX +Active = Surface

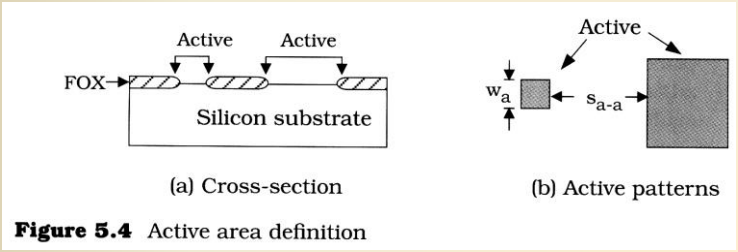


Figure 5.4 Active area definition

5.2.3 Doped Silicon Region

- Create n+ and p+ regions
  - Also known as **ndiff** and **pdiff**
  - Carryover from the days when dopants were introduced into the wafer using a thermal technique called **diffusion** instead of ion **implantation**
- nSelect and pSelect masks
- n+ = (nSelect) ∩ (Active)
  - w_a = minimum width of an Active area
  - $S_{a\text{-}n}$= minimum Active-to-nSelect spacing
- p+ = (pSelect) ∩ (Active) ∩(nWell)
  - w_a = minimum Active area width
  - $S_{a\text{-}p}$ = minimum Active-to-pSetect spacing
  - $S_{p\text{-}nw}$ = minimum pSelect-to-nWell spacing

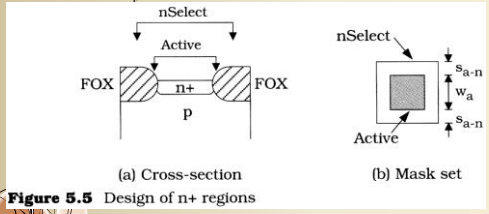


Figure 5.5 Design of n+ regions

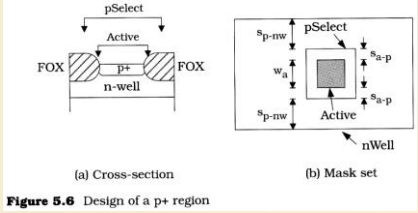


Figure 5.6 Design of a p+ region

5.2.4 MOSFET

- Self-aligned MOSFET structures exist every time a poly gate line completely crosses an n+ or p+ region
- FETs thus require the use of polygons on the **Poly mask** layer
- Design rules
  - $L=w_p$ = minimum poly width
    - The minimum poly linewidth w_p is the same as the drawn channel length for a FET
  - S_{p-p} = minimum poly-to-poly spacing
  - d_{po} = minimum extension of Poly beyond Active ➔ **gate overhang**
- nFET = (nSelect) n (Active) n (Poly)
- n+ = (nSelect) ∩ (Active) ∩ (NOT [Poly])

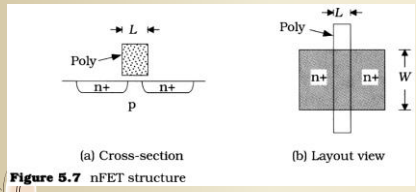


Figure 5.7 nFET structure

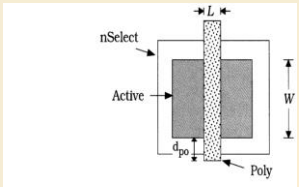


Figure 5.8 Masks for the nFET

5.2.4 MOSFET

- A pFET is created in the same manner
- n-well region is surrounded by implied p-substrate; this is shown explicitly in the top-view drawing
- pFET = (pSelect) ∩ (Active) ∩ (Poly) ∩ (nWell)
- p+ = (pSelect) ∩ (Active) ∩(nWell) ∩(NOT[Poly])

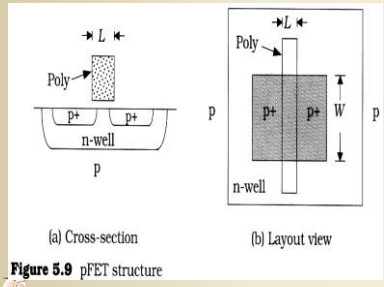


Figure 5.9 pFET structure

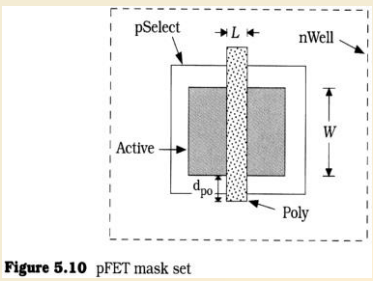


Figure 5.10 pFET mask set

5.2.4 Drawn and Effective Dimensions

- The critical dimensions of a MOSFET are the channel length *L* and the channel width *W*
- Electrical or Effective channel length
- L_{eff} =L-2L_0 or L_{eff}= L- Δ L where Δ L is the total reduction in channel length due to **overlay** and other effect
  - L_0: overlap distance
  - When the wafer is heated, the dopants move toward the other side
- W_{eff} = W – ΔW
  - ΔW : total reduction in channel length from all effect
  - Due to the field oxide grow
- The electrical characterization is the ratio of effective values W_{eff}/L_{eff}
  - Not the drawn value of W/L

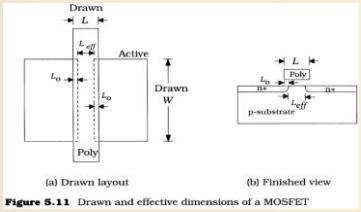


Figure 5.11 Drawn and effective dimensions of a MOSFET

5.2.5 Active Contacts

- An active contact is a cut in the oxide Ox1 that allows the first layer of metal to contact an active n+ or p+ region
- Defined by Active Contact Mask shown in 5.12(b)
- The contact is placed to fall inside of an n+ or p+ region, it is subject surround design rule
  - $S_{a\text{-}ac}$ = minimum spacing between Active and Active Contact
- The dimensions of the contact are given by
  - $d_{ac,\,v}$ = vertical size of the contact
  - $d_{ac,\,h}$ = horizontal size o f the contact
- A square contact is obtained if
  - $d_{ac,\,v} = d_{ac,\,h} = d_{ac}$

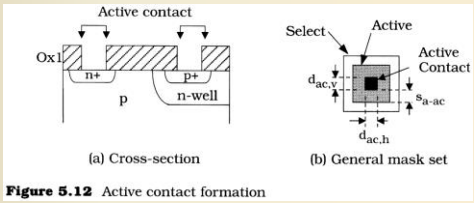


Figure 5.12 Active contact formation

5.2.6 Metal 1

- Metal1 is applied to the wafer after the Ox1 oxide
  - It is used as interconnect for signal and also for power supply distributions
- Metal1 mask feature overlapping the Active Contact to attain the electrical connection
- Design rules
  - w_{m1} = minimum width of a Metal1 line
  - $s_{m1\text{-}ac}$ = minimum spacing from Metal1 to Active Contact
  - $s_{m1\text{-}m1}$ is not shown

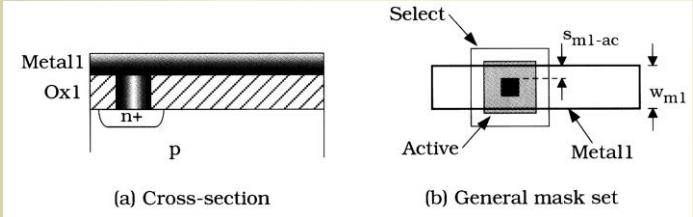


Figure 5.13 Metal1 line with Active Contact

5.2.6 Metal 1

- Every contact is characterized by a resistance due to the metal connections
  - R_c = contact resistance Ω
- To limit the overall resistance, it is common to use as many contacts as the design rules permit
- Effective resistance
  - $R_{c,eff} = \frac{1}{N} R_c$

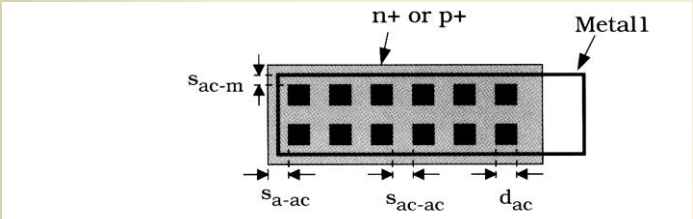


Figure 5.14 Multiple contacts to reduce contact resistance

5.2.6 Metal 1

- Metal1 allows access to the active regions of MOSFETs using the Active Contact oxide cut
- Design rules
  - $s_{p\text{-}ac}$ = minimum spacing from Poly to Active Contact
    - Insure Active Contact does not destroy any of the polysilicon gate
  - $s_{a\text{-}p}$ = minimum spacing from Active to Poly

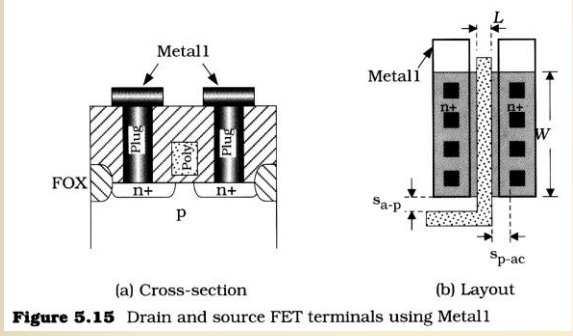


Figure 5.15 Drain and source FET terminals using Metal1

5.2.6 Metal 1

- A **Poly Contact Mask** is used to allow electrical connections Metal1 and the polysilicon gate
- The Poly Contact mask defines the oxide cut as indicated by the "empty" square shown in the upper part of the layout in Fig 5.16(a)

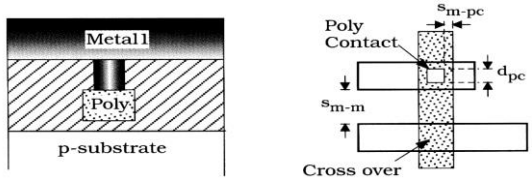


Figure 5.16 Poly Contact

5.2.6 Metal 1

- Let us construct a pair of series-connected FETs
- cross-sectional view for two nFETs
  - Series wiring is achieved by sharing the central n+ region
- Design rules
  - $S_{p\text{-}p}$ = minimum Poly-to-Poly spacing
  - $S_{g\text{-}g} = d_{ac} + 2\,S_{p\text{-}ac}$ (derive by design rule)

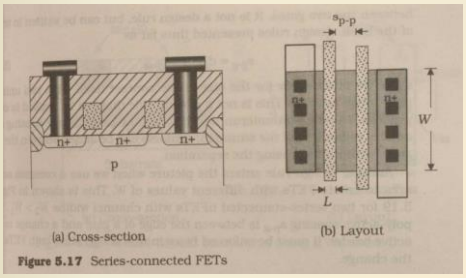


Figure 5.17 Series-connected FETs

5.2.6 Metal 1

- To obtain a pair of parallel-connected FETs, we add the contacts
- Design rules
  - $S_{g\text{-}g} = d_{ac} + 2\,S_{p\text{-}ac}$ (derive by design rule)
- Use a common active area to create FETs with different values of W
  - The poly-active spacing $S_{p\text{-}a}$ is between the edge of a gate and a change in the active border

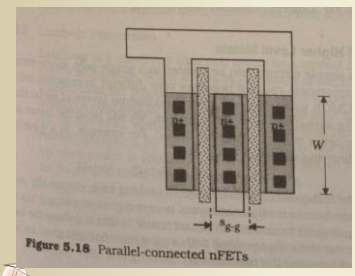


Figure 5.18 Parallel-connected nFETs

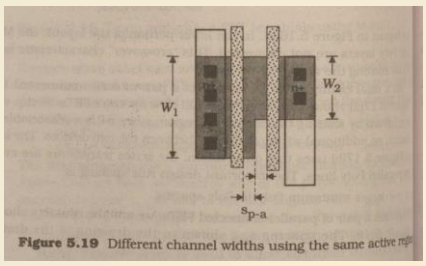


Figure 5.19 Different channel widths using the same active re

5.2.7 Vias

- Figure 5.20(a) illustrates the use of a via to connect Metal1 to Metal2
- The m ask layout is shown in Figure 5.20(b)
- Design Rules
  - d_v = dimension of a Via (may be different for vertical direction)
  - w_{m2} = minimum width of Metal2 feature
  - $s_{m2\text{-}m2}$ = minimum spacing between adjacent Metal2 features
  - $s_{v\text{-}m1}$ = minimum spacing between Via and Metal1 edges
  - $s_{v\text{-}m2}$ = minimum spacing between Via and Metal2 edges

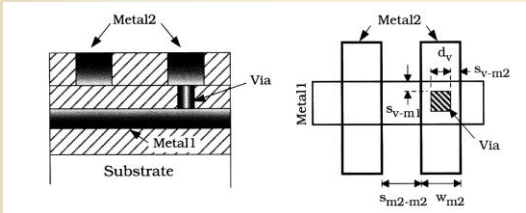


Figure 5.20 Metal1-Metal2 connection using a Via mask

5.2.8 Latch-up Prevention

- Latch up is a condition that can occur in a circuit fabricated in a bulk CMOS technology
- It draws a large current from the power supply but does not function in response to input stimuli
  - A chip may be operating normally and then enter a state of latch-up
  - Removing and reconnecting may restore operations
  - The chip may enter latch-up when power is applied and never be functional
  - If Vdd reaches **breakover voltage** V_{BO}, blocking is overwhelmed by internal electric field

5.2.8 Latch-up Prevention

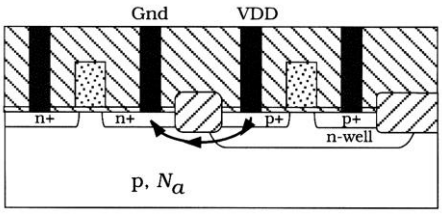


Figure 5.21 Latch-up current flow path

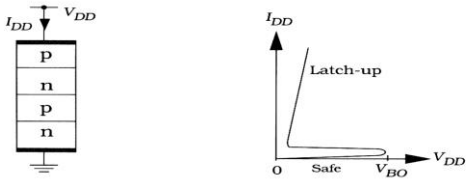
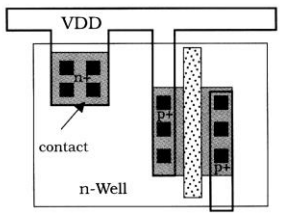


Figure 5.22 Characteristics of a 4-layer pnpn device

5.2.8 Latch-up Prevention

- Include an n-well contact every time a pFET is connected to the power supply Vdd.
- Include a p-substrate contact every time an nFET is connected to a ground rail



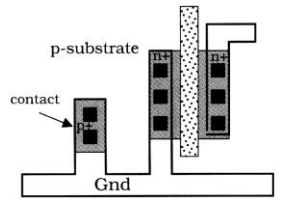


Figure 5.23 n-Well and substrate contacts for latch-up prevention

5.3 Cell Concepts

- Design VLSI chips are based on the idea of **hierarchical design**
- The basic building block are called **cells**
  - Can be a FET or an ALU
  - It may be used as a component to create a larger logic network
- **Cell-based design** is popular now
- At the cell level of design, do not care about the internal details
  - Replaced all of the layout by an equivalent logic symbol

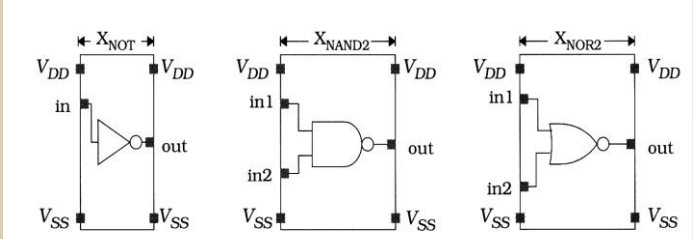


Figure 5.26 Logic gates as basic cells

5.3 Cell Concepts

- Input and output terminals are called **ports**
- Create more complex networks by cells
  - $f = \bar{a} \cdot b$

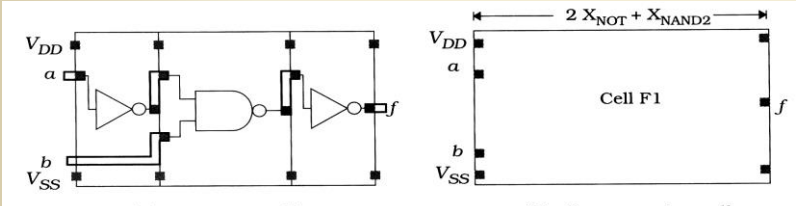


Figure 5.27 Creation of a new cell using basic units

5.3 Creating cells at the physical level

- The placement of the power lines VDD and VSS
  - $D_{m1\text{-}m1}$: Edge-to-edge distance between VDD and VSS
  - $P_{m1\text{-}m1}= D_{m1\text{-}m1+}W_{DD,}$: The pitch

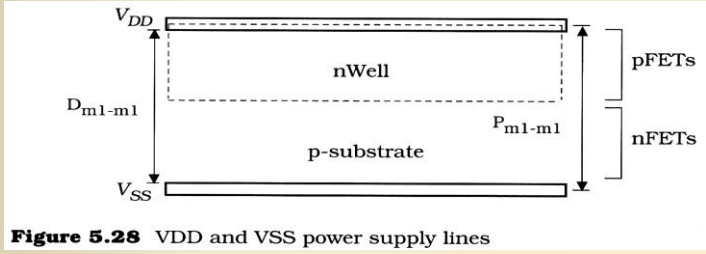


Figure 5.28 VDD and VSS power supply lines

5.3 Creating cells at the physical level

- Place FETS in between VDD and VSS lines.
  - Horizontal: limit by pitch
  - Vertical: Cell width is larger
- Since we want to choose a set of $D_{m1\text{-}m1}$ that is used for every cell, we should investigate the effect of the FET placement on the cell dimensions

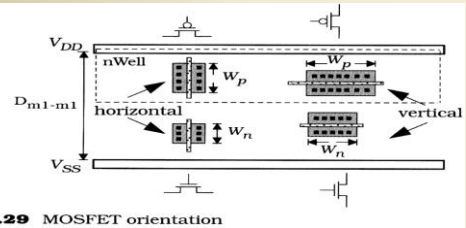


Figure 5.29 MOSFET orientation

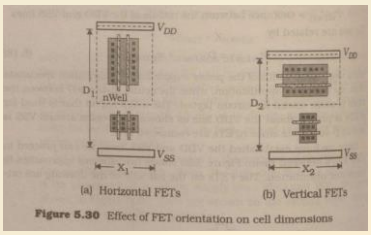


Figure 5.30 Effect of FET orientation on cell dimensions

5.3 Cell Concepts

- The shape of the cells affects how the cells fit together in logic cascades and determines what the more complex units may look like
- Tiling

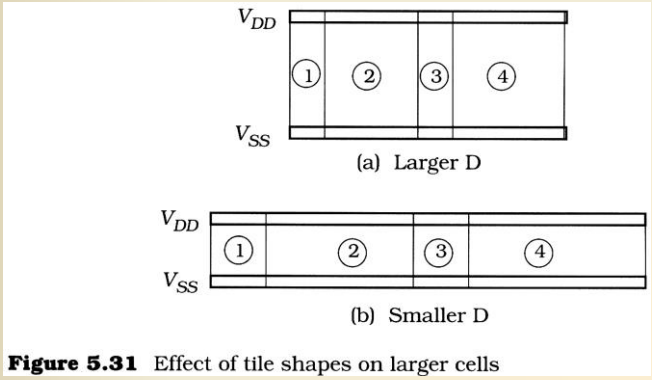


Figure 5.31 Effect of tile shapes on larger cells

5.3 Cell Concepts

- Interconnect routing considerations are important
  - **Wiring** is often more complicated than designing the **transistor** array
  - Wiring problems have a tendency of appearing at critical time

5.3 Cell Concepts

- One approach is to place rows of logics in parallel and allocate space in between rows for routing

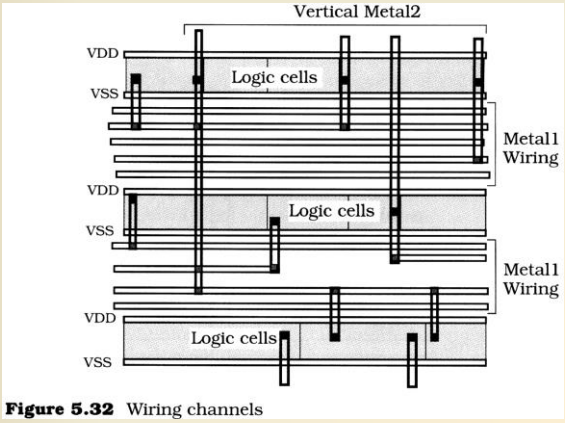


Figure 5.32 Wiring channels

5.3 Cell Concepts

- Alternate V_{dd} and V_{SS} power lines
  - Weinberger image
  - Inverted logic cells

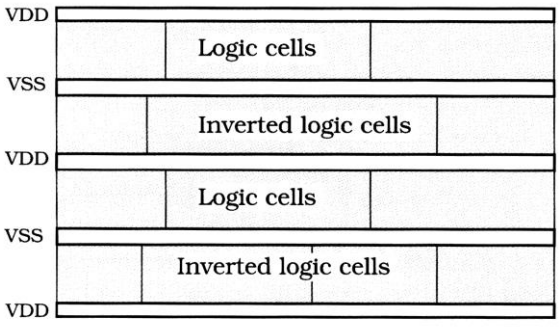


Figure 5.33 Weinberger image array

5.3 Cell Concepts

- Weinberger image

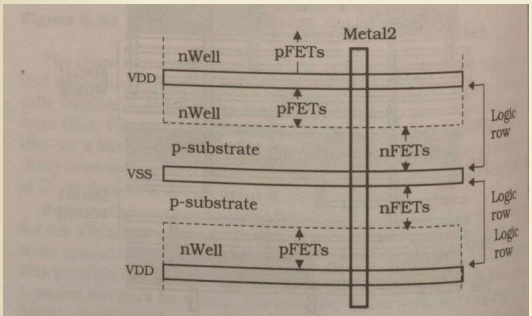


Figure 5.34 FET placement in a Weinberger array

5.3 Cell Concepts

- **Port** Placement
  - The input and output ports of a cell must be placed at convenient points to facilitate the interconnect wiring
  - Since FET gates are at the polysilicon level, we must provide a poly contact to connect the output of a cell to the input of another cell

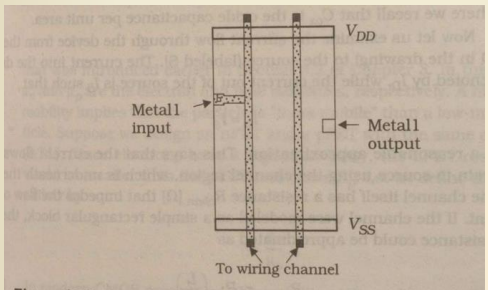


Figure 5.35 Port placement in a cell

5.4 FET Sizing and The Unit Transistor

- FET are specified by aspect ratio $\frac{W}{L}$
- Layout-dependent electrical properties
  - A_G = LW
  - $C_G = C_{ox}$*WL
  - $R_{chan} = R_{s,c}(L/W) \propto 1/W$
  - $R_{s,c}$: the sheet resistance of the channel region
- Electrons can move more easily than holes
  - Let **mobility ratio** r = μ_n/μ_p in modern CMOS, 2<r<3
  - So for equal size FETs r = R_p/R_n
- In order for $R_n = R_p$, the use the aspect ratio of p >n that compensates for the difference in mobility
  - $(W/L)_p = r*(W/L)_n$
  - Ex 5.1: $(W/L)_n$=4 and r=2.4
  - $(W/L)_p$= 2.4*4 = 9.6 ➔10

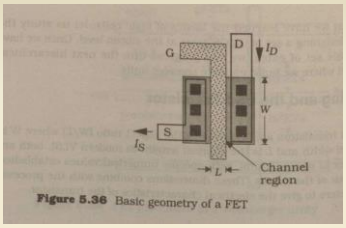


Figure 5.36 Basic geometry of a FET

5.4 Unit Transistor

- Minimum-size MOSFET
  - Both W and L have the minimum size=> 1X transistor
  - Scaling factor S
  - $W_{SX} = SW_{1X}$
    - $W_{4X} = 4W_{1X}$
  - $R_{SX} = R_{1X}/S$ $C_{Sx} = SC_{1X}$
    - $R_{2X} = R_{1X}/2$ $C_{2x} = 2C_{1X}$

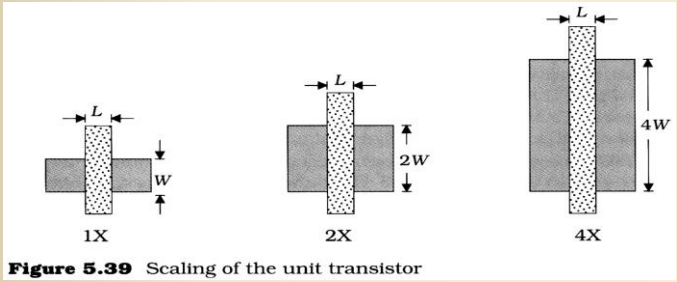


Figure 5.39 Scaling of the unit transistor

5.4 Scaling

- Useful to define series and parallel groups
- Series
  - 2 R_{1X} for series group with 1X
  - R_{1X} for series group with 2X
    - 2 (R_{1X}/2)
- Series-connected FETs are usually made larger than individual FETs to reduce the overall end-to-end resistance

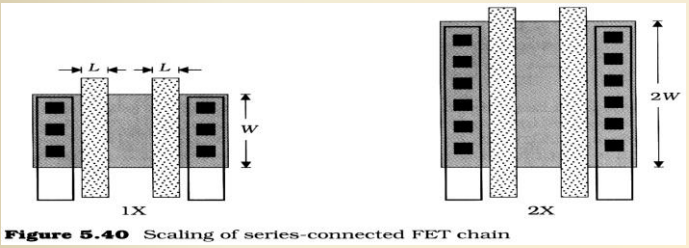


Figure 5.40 Scaling of series-connected FET chain

5.4 Scaling

- Useful to define series and parallel groups
- Parallel
  - Effective channel length = 4W
  - R_{4X}= R_{1X}/4
- The overall layout geometry can be adjusted to square or nearly square shapes

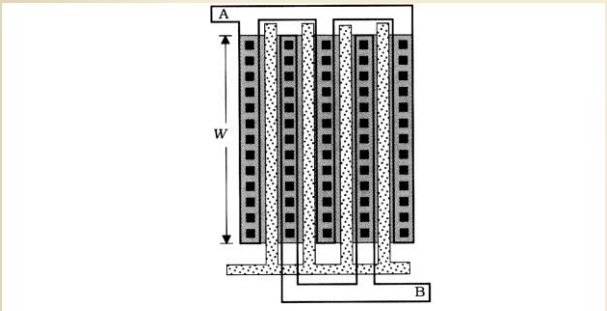


Figure 5.41 A large FET created from parallel-connected transistors

5.5 Physical Design of Logic Gates

◆ 5.5.1 Not Cell

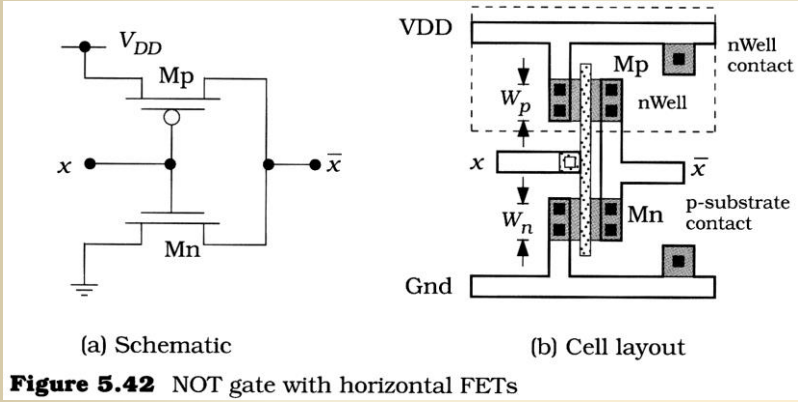


Figure 5.42 NOT gate with horizontal FETs

5.5 Physical Design of Logic Gates

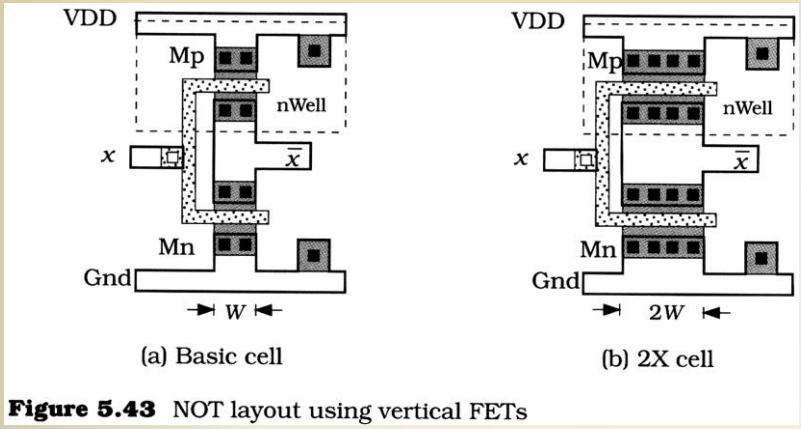


Figure 5.43 NOT layout using vertical FETs

5.5 Physical Design of Logic Gates

◆Symmetric inverter

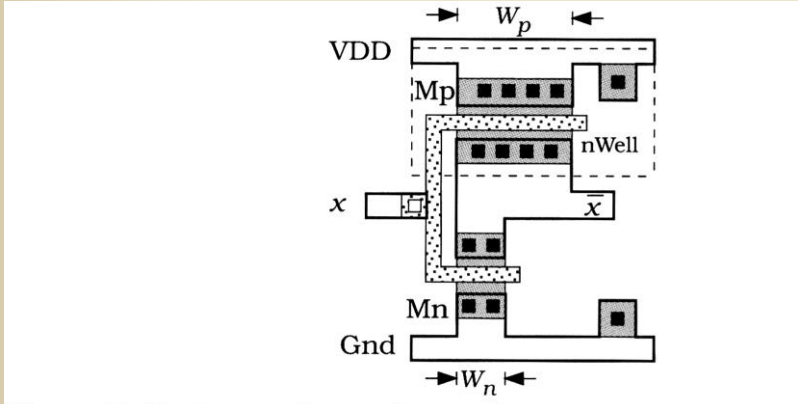


Figure 5.44 Layout for an electrically symmetric NOT gate

5.5 Physical Design of Logic Gates

◆5.5.2 NAND and NOR Cell

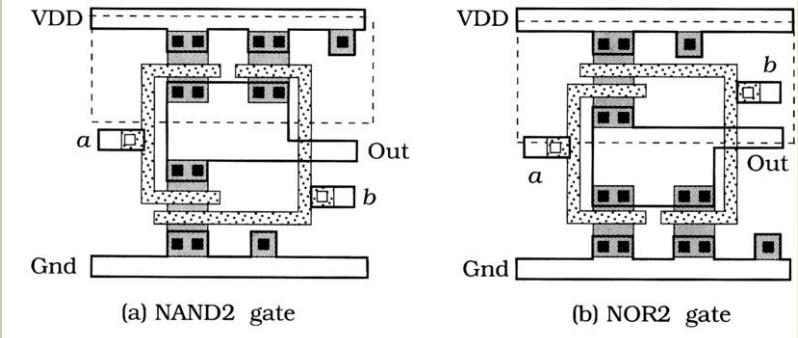


Figure 5.45 NAND2 and NOR2 layouts using vertical FETs

5.5 Physical Design of Logic Gates

◆5.5.2 NAND and NOR Cell

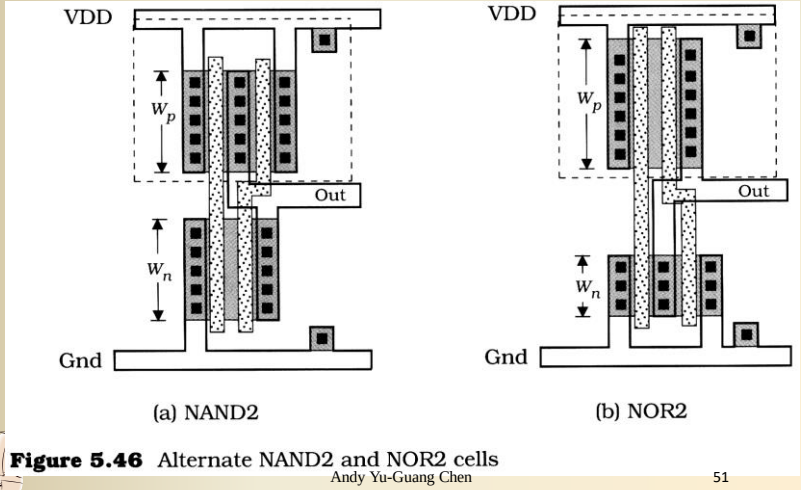


Figure 5.46 Alternate NAND2 and NOR2 cells

5.5 Physical Design of Logic Gates

◆5.5.3 Complex Logic Gates

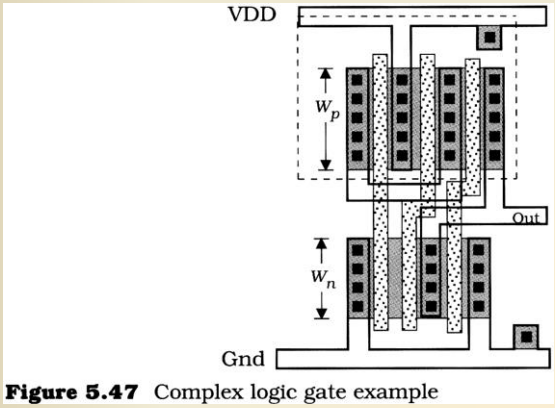


Figure 5.47 Complex logic gate example

5.6 Design Hierarchies

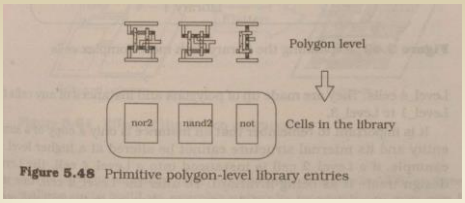


Figure 5.48 Primitive polygon-level library entries

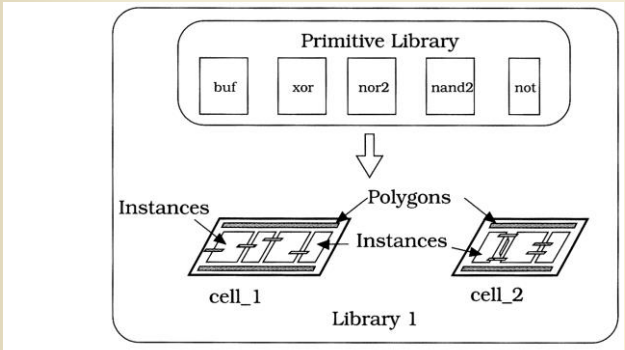


Figure 5.49 Expanding the library with more complex cells

5.6 Design Hierarchies

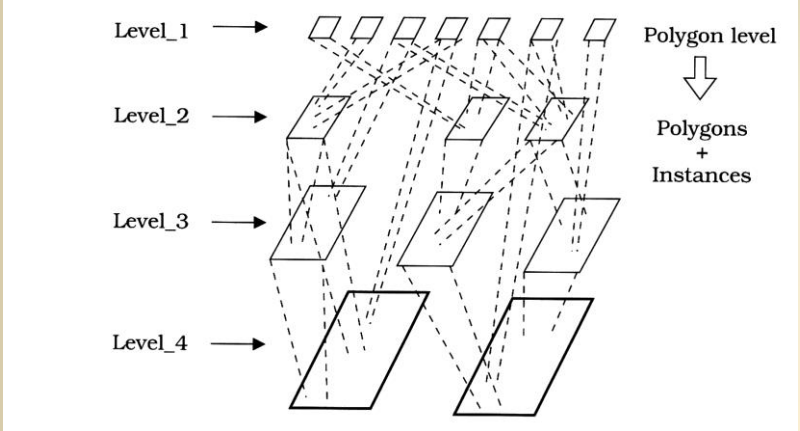


Figure 5.50 Cell hierarchy

5.6 Design Hierarchies

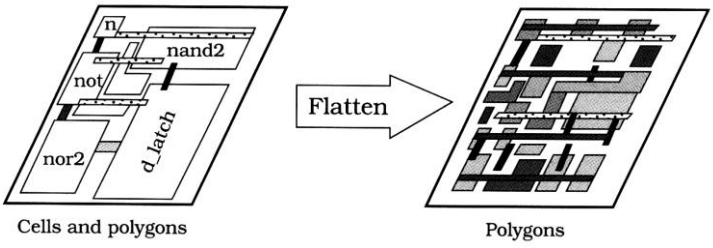


Figure 5.51 Effect of the flatten operation

Summary

- VLSI systems are created using the concept of design hierarchies where simple building blocks are used to design more complex units
- The layout is process dependent
- A new library must be built every time a new fabrication plant goes on line

Q&A

Andy, Yu-Guang Chen
Associate Professor, Department of EE, NCU
Email: andyygchen@ee.ncu.edu.tw
FB: Yu-Guang Chen
IG: ncu.eda.andy
Google account: andyygchen.ncu