

Student ID : 111062307, Name : 陳大佑

```
__data __at (0x30) char saved_SP[MAXTHREADS];
__data __at (0x34) ThreadID cur_ID;
__data __at (0x35) char bitmap_ID;
__data __at (0x36) char temp_SP; // temporary save the SP
__data __at (0x37) ThreadID new_ID;
```

```
__data __at (0x38) char sharedBuffer;
__data __at (0x39) char bufferFull; // 0: empty, 1: full
__data __at (0x3A) char nextChar;
```

Set some parameters on manually allocated memory.

```
void myTimer0Handler(void) {
    __critical {
        SAVESTATE;
        if (!bitmap_ID) ;
        else if (cur_ID == 0) {
            if (bitmap_ID & 0x2) cur_ID = 1;
            else if (bitmap_ID & 0x4) cur_ID = 2;
            else if (bitmap_ID & 0x8) cur_ID = 3;
        } else if (cur_ID == 1) {
            if (bitmap_ID & 0x4) cur_ID = 2;
            else if (bitmap_ID & 0x8) cur_ID = 3;
            else if (bitmap_ID & 0x1) cur_ID = 0;
        } else if (cur_ID == 2) {
            if (bitmap_ID & 0x8) cur_ID = 3;
            else if (bitmap_ID & 0x1) cur_ID = 0;
            else if (bitmap_ID & 0x2) cur_ID = 1;
        } else if (cur_ID == 3) {
            if (bitmap_ID & 0x1) cur_ID = 0;
            else if (bitmap_ID & 0x2) cur_ID = 1;
            else if (bitmap_ID & 0x4) cur_ID = 2;
        }

        RESTORESTATE;
    }
    __asm
    RETI
__endasm;
}
```

If bitmap_ID can't match anything then do nothing.

If cur_ID is 0 then check whether exists other thread or not.

If so, switch to it.

And if cur_ID is 1 or 2 or 3 do same thing like cur_ID = 0.

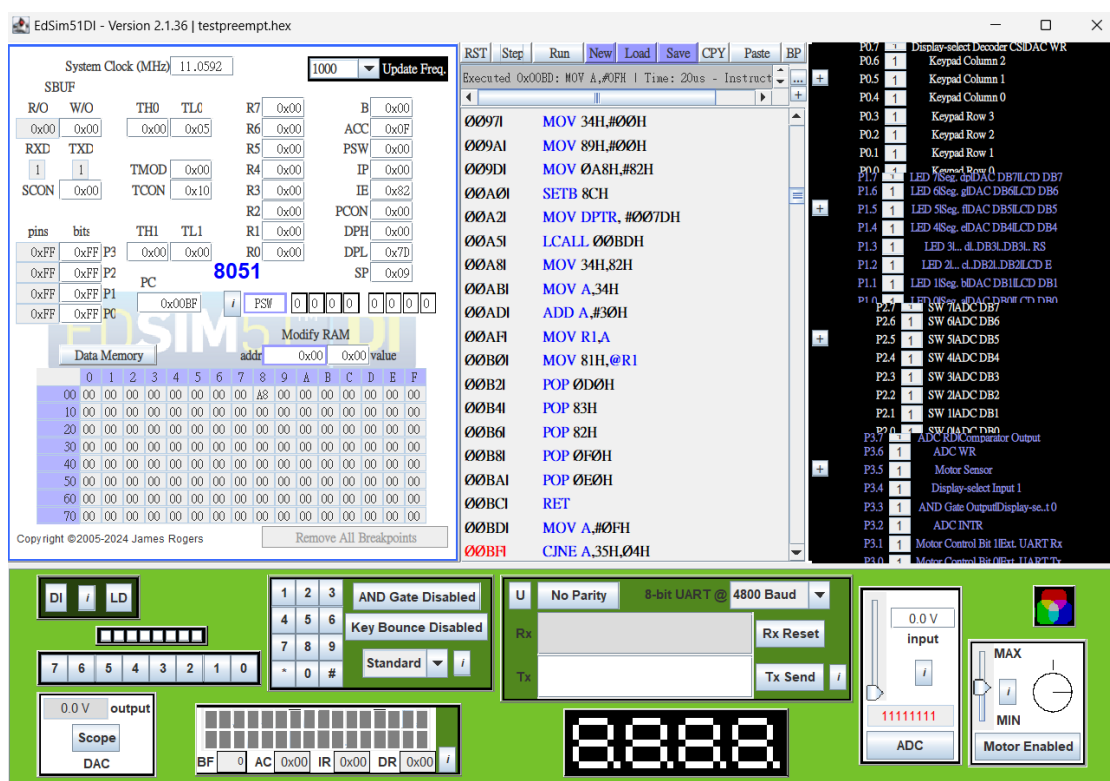
Screenshots for compilation.

```
dyllan@LAPTOP-S5F0LV5V ~/os/ppc2
$ make clean
rm *.hex *.ihx *.lnk *.lst *.map *.mem *.rel *.rst *.sym *.asm *.lk
rm: cannot remove '*.ihx': No such file or directory
rm: cannot remove '*.lnk': No such file or directory
make: *** [clean] Error 1

dyllan@LAPTOP-S5F0LV5V ~/os/ppc2
$ make
sdcc -c testpreempt.c
sdcc -c preemptive.c
preemptive.c:161: warning 85: in function ThreadCreate unreferenced function argument : 'fp'
sdcc -o testpreempt.hex testpreempt.rel preemptive.rel
```

Screenshots and explanation:

Before the main thread was created, since by default the SP = 0x07, the 0x08 was numbered by first instruction(bootstrap).



After main thread had been created, the address of 40H was stored for main's address, and 42H, 43H, 44H, 45H, 46H are ACC, B, DPL, DPH, PSW, respectively.

EdSim51DI - Version 2.1.36 | testpreempt.hex

System Clock (MHz): 11.0592 | 1000 Update Freq.

SBUF: R/O 0x00, W/O 0x00, TH0 0x01, TL0 0x09, RXD 0x00, TXD 0x00, SCON 0x00, TCON 0x10, pins 0xFF, bits 0xFF, TH1 0x00, TL1 0x00, PC 0x011B, PSW 0x0000, Modify RAM: addr 0x00, value 0x00.

Registers: R7 0x00, R6 0x00, R5 0x00, R4 0x00, R3 0x00, R2 0x00, R1 0x00, R0 0x00, B 0x00, ACC 0x00, PSW 0x00, IP 0x00, IE 0x02, PCON 0x00, DPH 0x00, DPL 0x7D, SP 0x45.

Instruction List: 00F7 ORL 35H, #08H; 00FA MOV 37H, #03H; 00FD MOV A, 37H; 00FF SWAP A; 0100 ANL A, #0F0H; 0102 MOV R7, A; 0103 ADD A, #3FH; 0105 MOV 81H, A; 0107 MOV A, 82H; 0109 PUSH 0E0H; 010B MOV A, 83H; 010D PUSH 0E0H; 010F MOV A, #00H; 0111 PUSH 0E0H; 0113 PUSH 0E0H; 0115 PUSH 0E0H; 0117 PUSH 0E0H; 0119 MOV A, 37H; 011B MOV R7, A.

Hardware Interface: Keypad (DI, LD, 1-9, *, #), AND Gate Disabled, Key Bounce Disabled, Standard, 8-bit UART @ 4800 Baud, Rx Reset, Tx Send, Scope, DAC, ADC, Motor Enabled.

And after producer was created, the address of the 50H was stored for producer's address. and 52H~56H are ACC, B, DPL, DPH, PSW, respectively.

EdSim51DI - Version 2.1.36 | testpreempt.hex

System Clock (MHz): 11.0592 | 1000 Update Freq.

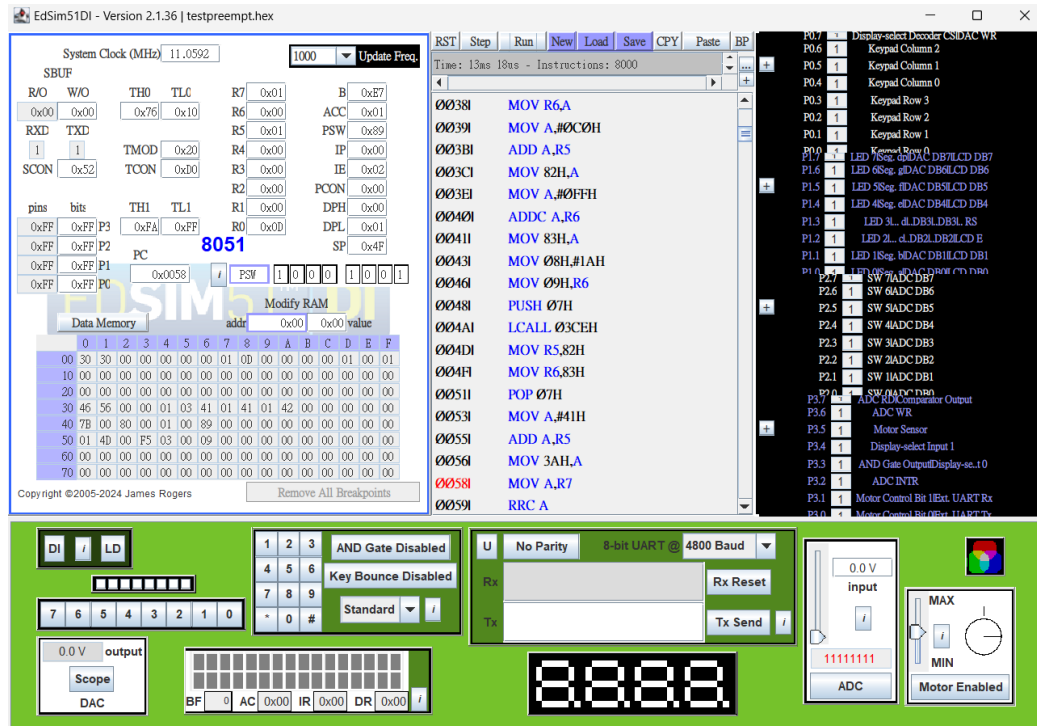
SBUF: R/O 0x00, W/O 0x00, TH0 0x03, TL0 0x1C, RXD 0x00, TXD 0x00, SCON 0x00, TCON 0x10, pins 0xFF, bits 0xFF, TH1 0x00, TL1 0x00, PC 0x0119, PSW 0x0000, Modify RAM: addr 0x00, value 0x00.

Registers: R7 0x10, R6 0x00, R5 0x00, R4 0x00, R3 0x00, R2 0x00, R1 0x30, R0 0x30, B 0x00, ACC 0x00, PSW 0x00, IP 0x00, IE 0x02, PCON 0x00, DPH 0x00, DPL 0x22, SP 0x55.

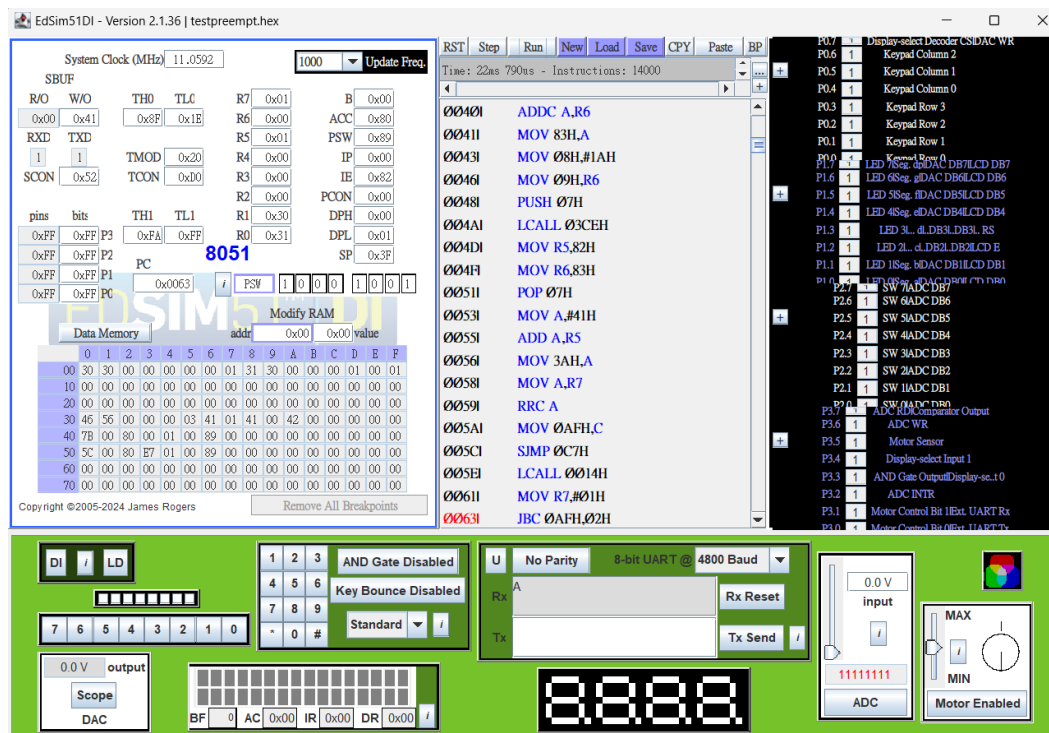
Instruction List: 00F4 JB 0E3H, 06H; 00F7 ORL 35H, #08H; 00FA MOV 37H, #03H; 00FD MOV A, 37H; 00FF SWAP A; 0100 ANL A, #0F0H; 0102 MOV R7, A; 0103 ADD A, #3FH; 0105 MOV 81H, A; 0107 MOV A, 82H; 0109 PUSH 0E0H; 010B MOV A, 83H; 010D PUSH 0E0H; 010F MOV A, #00H; 0111 PUSH 0E0H; 0113 PUSH 0E0H; 0115 PUSH 0E0H; 0117 PUSH 0E0H; 0119 MOV A, 37H.

Hardware Interface: Keypad (DI, LD, 1-9, *, #), AND Gate Disabled, Key Bounce Disabled, Standard, 8-bit UART @ 4800 Baud, Rx Reset, Tx Send, Scope, DAC, ADC, Motor Enabled.

We can know the producer is running, since cur_ID on address(34H) is 01 which means producer and compare to previous picture we can find the addresses of(38H, 39H, 3AH) are replaced by other number(char'A').



We can know the consumer is running, since cur_ID on address(34H) is 00 which means it switches. And the address(39H) is changed from 1 to 0.



We can see the running time of the producer is at 45, 28, and 13,

and the running time of consumer is at 56, 39, and 23, which difference is regular about 10. So interrupt is triggering on a regular basis.

EdSim51DI - Version 2.1.36 | testpreempt.hex

System Clock (MHz): 11.0592 | 1000 Update Freq.

SBUF: R/O W/O TH0 TL0 R7 B 0xE8
0x00 0x41 0x1C 0x0B R6 ACC 0x01
RXD TXD R5 PSW 0x89
1 1 TMOD 0x20 R4 0x00 IP 0x00
SCON 0x52 TCON 0xD0 R3 0x00 IE 0x02
pins bits TH1 TL1 R2 PCON 0x00 DPH 0x00
0xFF 0xFF P3 0xFA 0xFE R1 0x00 DPL 0x02
0xFF 0xFF P2 0xFF 0xFF PC 8051 PSW 1 0 0 0 1 0 0 1
0xFF 0xFF P1 0xFF 0xFF
0xFF 0xFF P0 0xFF 0xFF

Data Memory: addr 0x00 0x00 value
0 0 1 2 3 4 5 6 7 8 9 A B C D E F
00 30 30 00 00 00 00 00 01 00 00 00 00 00 02 00 01
10 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
20 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
30 46 56 00 00 01 03 41 01 42 01 43 00 00 00 00 00
40 61 00 80 00 01 00 89 00 00 00 00 00 00 00 00 00
50 01 40 00 F5 03 00 89 00 00 00 00 00 00 00 00 00
60 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
70 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00

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Hardware Panel: DI, LD, AND Gate Disabled, Key Bounce Disabled, Standard, 8-bit UART @ 4800 Baud, No Parity, Rx Reset, Tx Send, 0.0 V input, 11111111, ADC, Motor Enabled, 8888 display, Scope DAC.

EdSim51DI - Version 2.1.36 | testpreempt.hex

System Clock (MHz): 11.0592 | 1000 Update Freq.

SBUF: R/O W/O TH0 TL0 R7 B 0x00
0x00 0x42 0x64 0x15 R6 ACC 0x80
RXD TXD R5 PSW 0x89
1 1 TMOD 0x20 R4 0x00 IP 0x00
SCON 0x52 TCON 0xD0 R3 0x00 IE 0x82
pins bits TH1 TL1 R2 PCON 0x00 DPH 0x00
0xFF 0xFF P3 0xFA 0xFE R1 0x30 DPL 0x01
0xFF 0xFF P2 0xFF 0xFF PC 8051 PSW 1 0 0 0 1 0 0 1
0xFF 0xFF P1 0xFF 0xFF
0xFF 0xFF P0 0xFF 0xFF

Data Memory: addr 0x00 0x00 value
0 0 1 2 3 4 5 6 7 8 9 A B C D E F
00 30 30 00 00 00 00 00 01 31 30 00 00 00 02 00 01
10 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
20 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
30 46 56 00 00 00 03 41 01 42 00 43 00 00 00 00 00
40 61 00 80 00 01 00 89 00 00 00 00 00 00 00 00 00
50 5C 00 80 E8 02 00 89 00 00 00 00 00 00 00 00 00
60 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
70 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00

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Hardware Panel: DI, LD, AND Gate Disabled, Key Bounce Disabled, Standard, 8-bit UART @ 4800 Baud, No Parity, Rx Reset, Tx Send, 0.0 V input, 11111111, ADC, Motor Enabled, 8888 display, Scope DAC.

EdSim51DI - Version 2.1.36 | testpreempt.hex

System Clock (MHz) 11.0592 1000 Update Freq.

SBUF

R/O	W/O	TH0	TL0	R7	B
0x00	0x42	0x1F	0x1E	0x01	0xB9

R6	ACC	R5	PSW	R4	IP
0x00	0x01	0x03	0x99	0x00	0x00

R3	IE	R2	PCON	R1	DPH
0x00	0x02	0x00	0x00	0x00	0x00

R0	DPL	SP
0x00	0x03	0x4F

pins bits TH1 TL1 PC PSW 1 0 0 0 1 0 0 1

8051

Data Memory

addr	0x00	0x00	value
0	0	1	2

Modify RAM

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RST Step Run New Load Save CPY Paste BP

Time: 45ms 567us - Instructions: 28000

00401 ADDC A,R6
00411 MOV 83H,A
00431 MOV 08H,#1AH
00461 MOV 09H,R6
00481 PUSH 07H
004A1 LCALL 03CEH
004D1 MOV R5,82H
004F1 MOV R6,83H
00511 POP 07H
00531 MOV A,#41H
00551 ADD A,R5
00561 MOV 3AH,A
00581 MOV A,R7
00591 RRC A
005A1 MOV 0AFH,C
005C1 SIMP 0C7H
005E1 LCALL 0014H
00611 MOV R7,#01H
00631 JBC 0AFH,02H

P0.7 Display-select Decoder CS/DAC WR
P0.6 Keypad Column 2
P0.5 Keypad Column 1
P0.4 Keypad Column 0
P0.3 Keypad Row 3
P0.2 Keypad Row 2
P0.1 Keypad Row 1
P0.0 Keypad Row 0
P1.7 LED 7Seg. a/DAC DB7/LCD DB7
P1.6 LED 6Seg. g/DAC DB6/LCD DB6
P1.5 LED 5Seg. f/DAC DB5/LCD DB5
P1.4 LED 4Seg. e/DAC DB4/LCD DB4
P1.3 LED 3L. d/DB3L/DB3L RS
P1.2 LED 2L. c/DB2L/DB2L CD E
P1.1 LED 1Seg. b/DAC DB1/LCD DB1
P1.0 LED 0Seg. a/DAC DB0/LCD DB0
P2.7 SW 7ADC DB7
P2.6 SW 6ADC DB6
P2.5 SW 5ADC DB5
P2.4 SW 4ADC DB4
P2.3 SW 3ADC DB3
P2.2 SW 2ADC DB2
P2.1 SW 1ADC DB1
P2.0 SW 0ADC DB0
P3.7 ADC 0/0-Compendium Output
P3.6 ADC WR
P3.5 Motor Sensor
P3.4 Display-select Input 1
P3.3 AND Gate Output/Display-se.10
P3.2 ADC INTR
P3.1 Motor Control Bit 1/Ext. UART Rx
P3.0 Motor Control Bit 0/Ext. UART Tx

DI LD

AND Gate Disabled

Key Bounce Disabled

Standard

U No Parity 8-bit UART @ 4800 Baud

Rx Reset

Tx Send

0.0V input

11111111

ADC

MAX MIN

Motor Enabled

0.0V output

Scope

DAC

BF 0 AC 0x00 IR 0x00 DR 0x00

8888

EdSim51DI - Version 2.1.36 | testpreempt.hex

System Clock (MHz) 11.0592 1000 Update Freq.

SBUF

R/O	W/O	TH0	TL0	R7	B
0x00	0x43	0x68	0x09	0x01	0x00

R6	ACC	R5	PSW	R4	IP
0x00	0x80	0x03	0x99	0x00	0x00

R3	IE	R2	PCON	R1	DPH
0x00	0x82	0x00	0x00	0x30	0x00

R0	DPL	SP
0x31	0x01	0x3F

pins bits TH1 TL1 PC PSW 1 0 0 0 1 0 0 1

8051

Data Memory

addr	0x00	0x00	value
0	0	1	2

Modify RAM

Copyright ©2005-2024 James Rogers Remove All Breakpoints

RST Step Run New Load Save CPY Paste BP

Time: 56ms 968us - Instructions: 35000

00401 ADDC A,R6
00411 MOV 83H,A
00431 MOV 08H,#1AH
00461 MOV 09H,R6
00481 PUSH 07H
004A1 LCALL 03CEH
004D1 MOV R5,82H
004F1 MOV R6,83H
00511 POP 07H
00531 MOV A,#41H
00551 ADD A,R5
00561 MOV 3AH,A
00581 MOV A,R7
00591 RRC A
005A1 MOV 0AFH,C
005C1 SIMP 0C7H
005E1 LCALL 0014H
00611 MOV R7,#01H
00631 JBC 0AFH,02H

P0.7 Display-select Decoder CS/DAC WR
P0.6 Keypad Column 2
P0.5 Keypad Column 1
P0.4 Keypad Column 0
P0.3 Keypad Row 3
P0.2 Keypad Row 2
P0.1 Keypad Row 1
P0.0 Keypad Row 0
P1.7 LED 7Seg. a/DAC DB7/LCD DB7
P1.6 LED 6Seg. g/DAC DB6/LCD DB6
P1.5 LED 5Seg. f/DAC DB5/LCD DB5
P1.4 LED 4Seg. e/DAC DB4/LCD DB4
P1.3 LED 3L. d/DB3L/DB3L RS
P1.2 LED 2L. c/DB2L/DB2L CD E
P1.1 LED 1Seg. b/DAC DB1/LCD DB1
P1.0 LED 0Seg. a/DAC DB0/LCD DB0
P2.7 SW 7ADC DB7
P2.6 SW 6ADC DB6
P2.5 SW 5ADC DB5
P2.4 SW 4ADC DB4
P2.3 SW 3ADC DB3
P2.2 SW 2ADC DB2
P2.1 SW 1ADC DB1
P2.0 SW 0ADC DB0
P3.7 ADC 0/0-Compendium Output
P3.6 ADC WR
P3.5 Motor Sensor
P3.4 Display-select Input 1
P3.3 AND Gate Output/Display-se.10
P3.2 ADC INTR
P3.1 Motor Control Bit 1/Ext. UART Rx
P3.0 Motor Control Bit 0/Ext. UART Tx

DI LD

AND Gate Disabled

Key Bounce Disabled

Standard

U No Parity 8-bit UART @ 4800 Baud

Rx Reset

Tx Send

0.0V input

11111111

ADC

MAX MIN

Motor Enabled

0.0V output

Scope

DAC

BF 0 AC 0x00 IR 0x00 DR 0x00

8888