Eclectronics Mini-Project 1 Analysis and Design Choices

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1 Circuit Design Choices

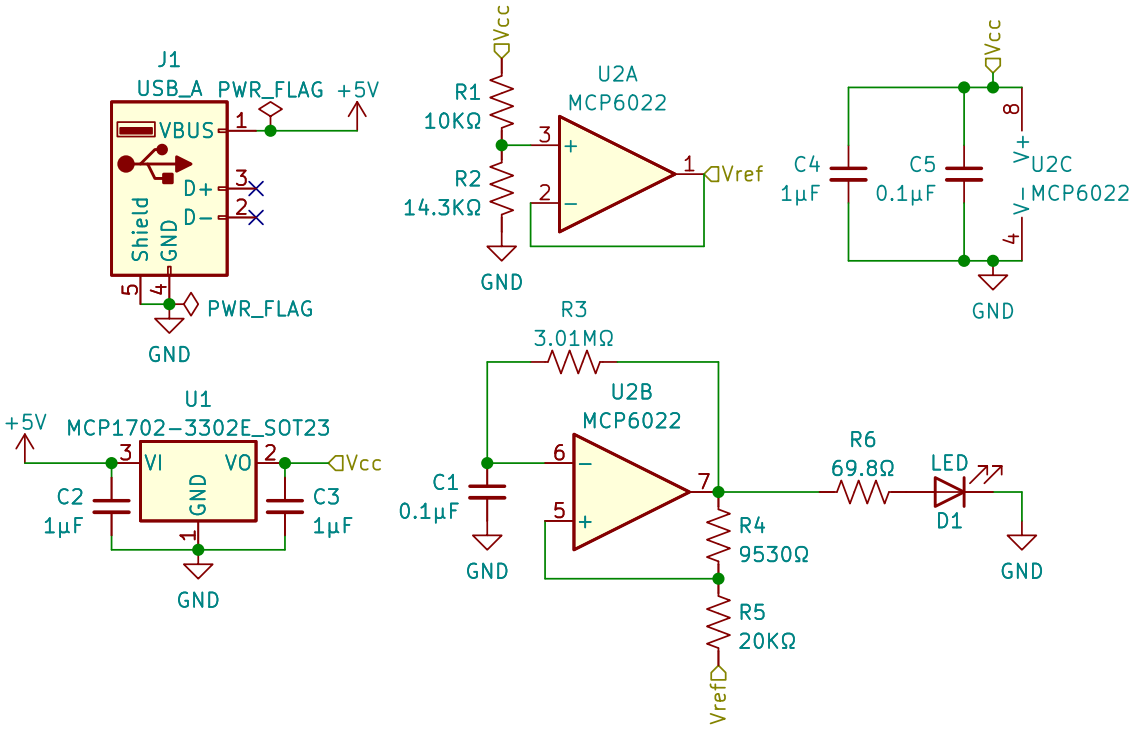


Figure 1: The schematic of my circuit in KiCad.

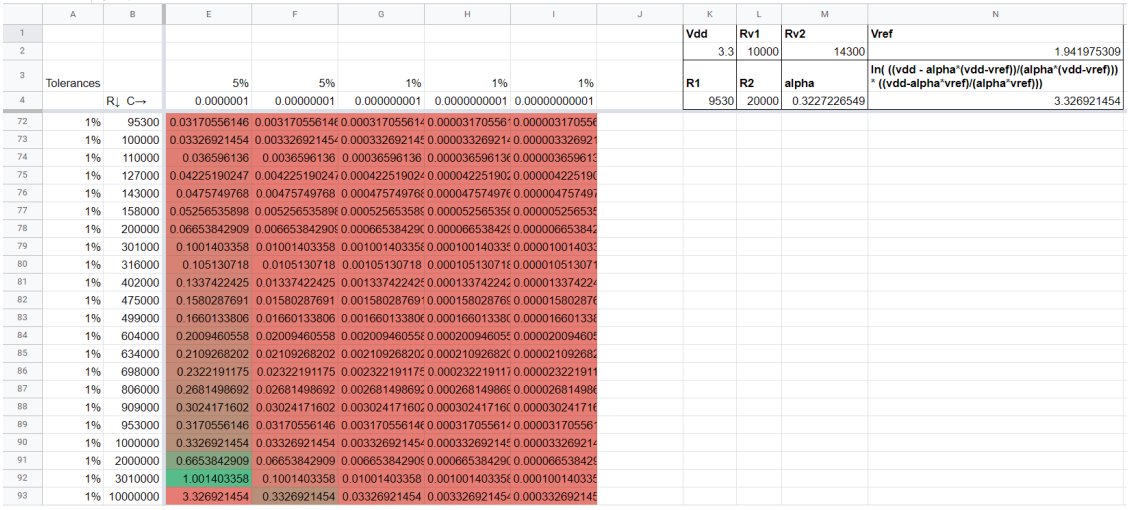
When designing my circuit for this mini-project, I began with a hysteretic oscillator since it's simple and uses a minimal number of components. This required me to generate a separate voltage V_{ref} in addition to the 3.3 V regulator output. This is formed by sending the output of a voltage divider created by R1 and R2 through a unity-gain buffer. This buffer prevents V_{ref} from fluctuating with V_{out}. The output of the oscillator is connected to the current-limiting resistor R6, which is connected to a red LED. I also placed bypass capacitors on the power pins of the op-amp and voltage regulator according to their datasheets.

With the essential structure out of the way, I began selecting component values that would keep the period of oscillation T within ±10% of 1 second. I did this based on equation 4.16 from the provided draft copy of *Another Book on Circuits*:

$$T = \tau \log \frac{V_{dd} - \alpha\left(V_{dd} - V_{ref}\right)}{\alpha\left(V_{dd} - V_{ref}\right)} \frac{V_{dd} - \alpha V_{ref}}{\alpha V_{ref}} \tag{1}$$

In this case, $\alpha = R_4/\left(R_4 + R_5\right)$, $V_{dd} = 3.3\,\text{V}$, $V_{ref} = V_{dd} * R_2/\left(R_1 + R_2\right)$, and $\tau = R_3 * C_1$. To start, I figured that τ would have the largest effect on T, followed by α with a smaller effect, and V_{ref} having a

relatively minor effect. Thus, my approach would be finding values for R3 and C1 that result in a nominal period close to 1 second using voltage divider ratios of 0.5 for α and V_{ref} (resulting in $V_{ref} = 1.65\,\text{V}$). To do this, I created a spreadsheet with a matrix of all of the allowed component values to calculate the period for all combinations of a single resistor and capacitor (Figure 2).



	A	B	E	F	G	H	I	J	K	L	M	N
1									Vdd	Rv1	Rv2	Vref
2									3.3	10000	14300	1.941975309
3	Tolerances		5%	5%	1%	1%	1%		R1	R2	alpha	ln(((vdd - alpha*(vdd-vref))/(alpha*(vdd-vref))) * ((vdd-alpha*vref)/(alpha*vref)))
4		R↓ C→	0.0000001	0.00000001	0.000000001	0.0000000001	0.00000000001		9530	20000	0.3227226549	3.326921454
72	1%	95300	0.03170556146	0.003170556146	0.0003170556146	0.00003170556	0.000003170556					
73	1%	100000	0.03326921454	0.003326921454	0.0003326921454	0.00003326921	0.000003326921					
74	1%	110000	0.036596136	0.0036596136	0.00036596136	0.00003659613	0.000003659613					
75	1%	127000	0.04225190247	0.004225190247	0.0004225190247	0.00004225190	0.000004225190					
76	1%	143000	0.0475749768	0.00475749768	0.0004757497680	0.00004757497	0.000004757497					
77	1%	158000	0.05256535898	0.005256535898	0.0005256535898	0.00005256535	0.000005256535					
78	1%	200000	0.06653842909	0.006653842909	0.0006653842909	0.00006653842	0.000006653842					
79	1%	301000	0.1001403358	0.01001403358	0.001001403358	0.00010014033	0.000010014033					
80	1%	316000	0.105130718	0.0105130718	0.001051307180	0.00010513071	0.000010513071					
81	1%	402000	0.1337422425	0.01337422425	0.001337422425	0.00013374224	0.000013374224					
82	1%	475000	0.1580287691	0.01580287691	0.001580287691	0.00015802876	0.000015802876					
83	1%	499000	0.1660133806	0.01660133806	0.001660133806	0.00016601338	0.000016601338					
84	1%	604000	0.2009460558	0.02009460558	0.002009460558	0.00020094605	0.000020094605					
85	1%	634000	0.2109268202	0.02109268202	0.002109268202	0.00021092682	0.000021092682					
86	1%	698000	0.2322191175	0.02322191175	0.002322191175	0.00023221911	0.000023221911					
87	1%	806000	0.2681498692	0.02681498692	0.002681498692	0.00026814986	0.000026814986					
88	1%	909000	0.3024171602	0.03024171602	0.003024171602	0.00030241716	0.000030241716					
89	1%	953000	0.3170556146	0.03170556146	0.003170556146	0.00031705561	0.000031705561					
90	1%	1000000	0.3326921454	0.03326921454	0.003326921454	0.00033269214	0.000033269214					
91	1%	2000000	0.6653842909	0.06653842909	0.006653842909	0.00066538429	0.000066538429					
92	1%	3010000	1.001403358	0.1001403358	0.01001403358	0.00100140335	0.000100140335					
93	1%	10000000	3.326921454	0.3326921454	0.03326921454	0.00332692145	0.000332692145					

Figure 2: A screenshot of part of the spreadsheet used for calculating the period. The calculated period for the selected values is in cell E92.

I avoided using the two largest capacitor values, since their high tolerance range of $\pm 10\%$ would leave me little room for other component variation. With that limitation, the closest period to 1 second was about 0.66 seconds using $R_3 = 3.01\,\text{M}\Omega$ and $C_1 = 0.1\,\mu\text{F}$. I then decreased alpha to around 0.32 by using $R_4 = 9530\,\Omega$ and $R_5 = 20\,\text{k}\Omega$, which brought the period closer to 1 s (approx 0.99 s). I then increased V_{ref} to around 1.94 V using $R_1 = 10\,\text{k}\Omega$ and $R_2 = 14.3\,\text{k}\Omega$, which brought the nominal period to 1.001 40 s. I figured this would be close enough to try worst-case analysis.

2 Worst-Case Tolerance Analysis in LTspice

To determine whether the component values would satisfy the tolerance requirement, I simulated my circuit in LTspice (Figure 3) for every combination of the most extreme tolerance variations for each component. I did not include the voltage regulator in the simulation. I processed the resulting data in MATLAB to extract the longest and shortest period from the simulations. The code used can be found in Appendix A. The results showed the range of the periods to be $[0.9309\,\text{s}, 1.0733\,\text{s}]$, which is within $\pm 10\%$ of 1 second.

A MATLAB Code

The following code extracts the longest and shortest oscillation periods from LTspice simulation output. Line 6 obtains a the highest value in the differential of the list of times where $dV/dt > 1000$ (all up-going transitions of the oscillation), which is the period.

```
1 loadspice('simulation.txt');
2 periods = zeros(1,length(time));
3 for i=1:length(time)
4     t = time{1,i};
5     v = vout{1,i};
6     periods(i)=max(diff(t((diff(v)./diff(t))>1000)));
7 end
```

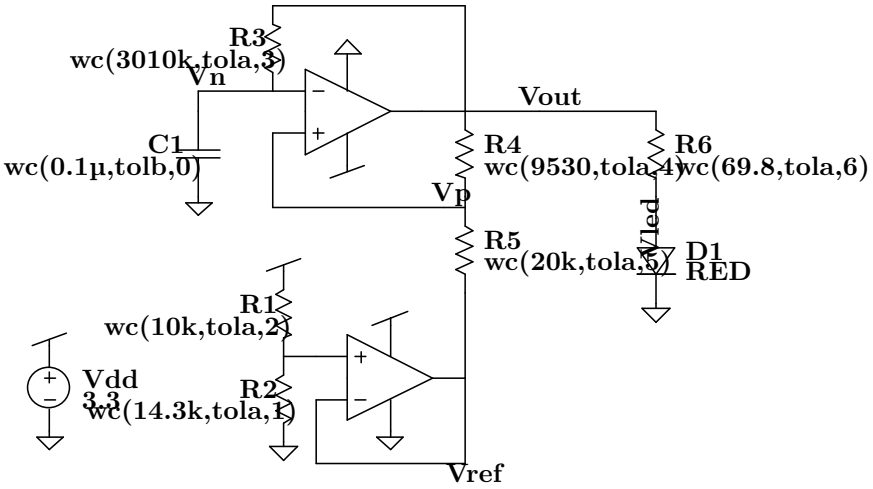


Figure 3: The schematic constructed in LTspice for simulation.

```
8 min(periods)
9 max(periods)
```