ENGR3426: Miniproject 1

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1 Schematic Capture and Simulation

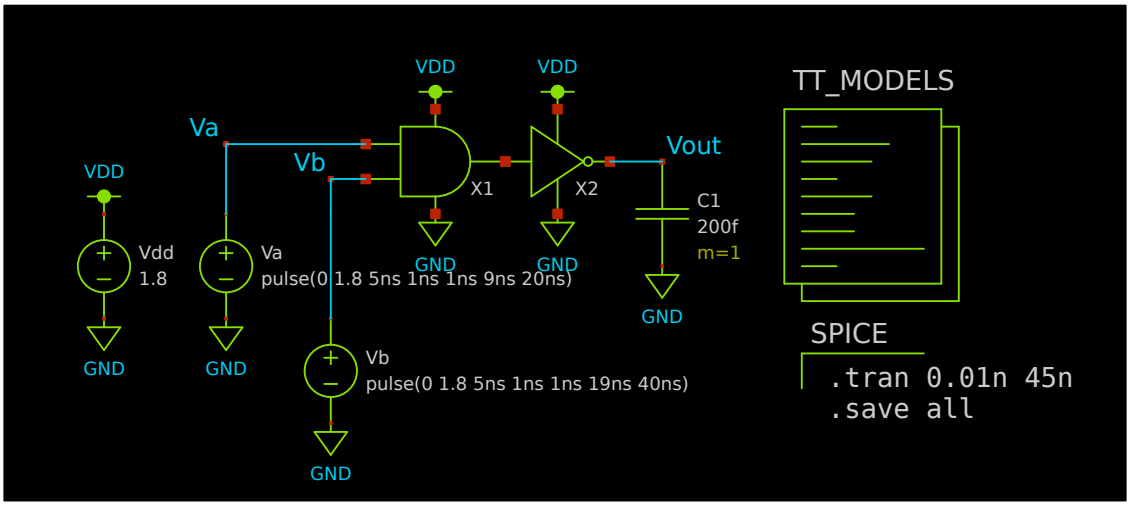
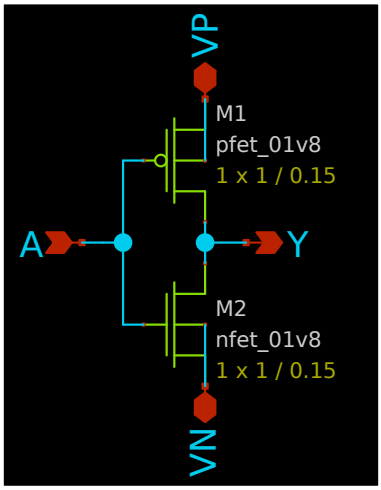
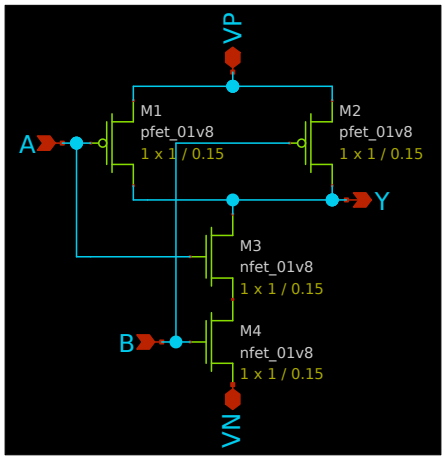


Figure 1: Schematic of my 2-input AND gate simulation test harness created in Xschem. The parameters used for `pulse()` for sources Va and Vb were chosen such that they will cycle through all possible input combinations.



(a) Schematic of my CMOS inverter created in Xschem.



(b) Schematic of my 2-input NAND gate created in Xschem.

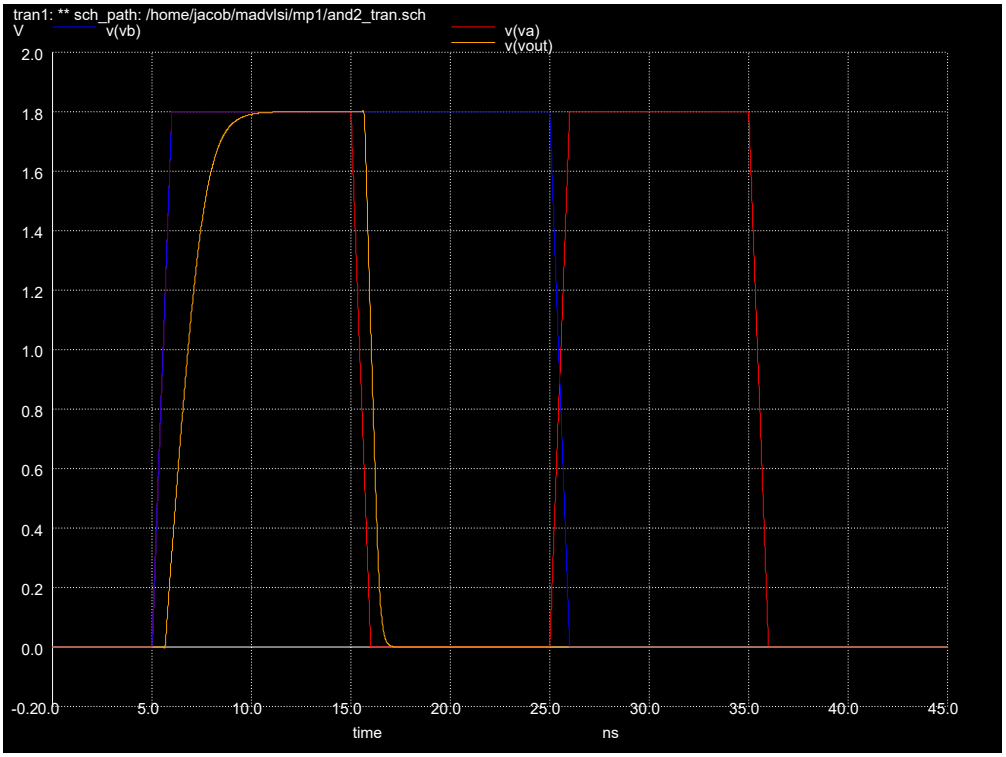


Figure 3: A plot of the output of the simulation of Figure 1. The AND gate behaves as expected; its output is only high when Va and Vb are high, and there is a small delay (approximately 1ns) between the input and output.

2 Layout Design

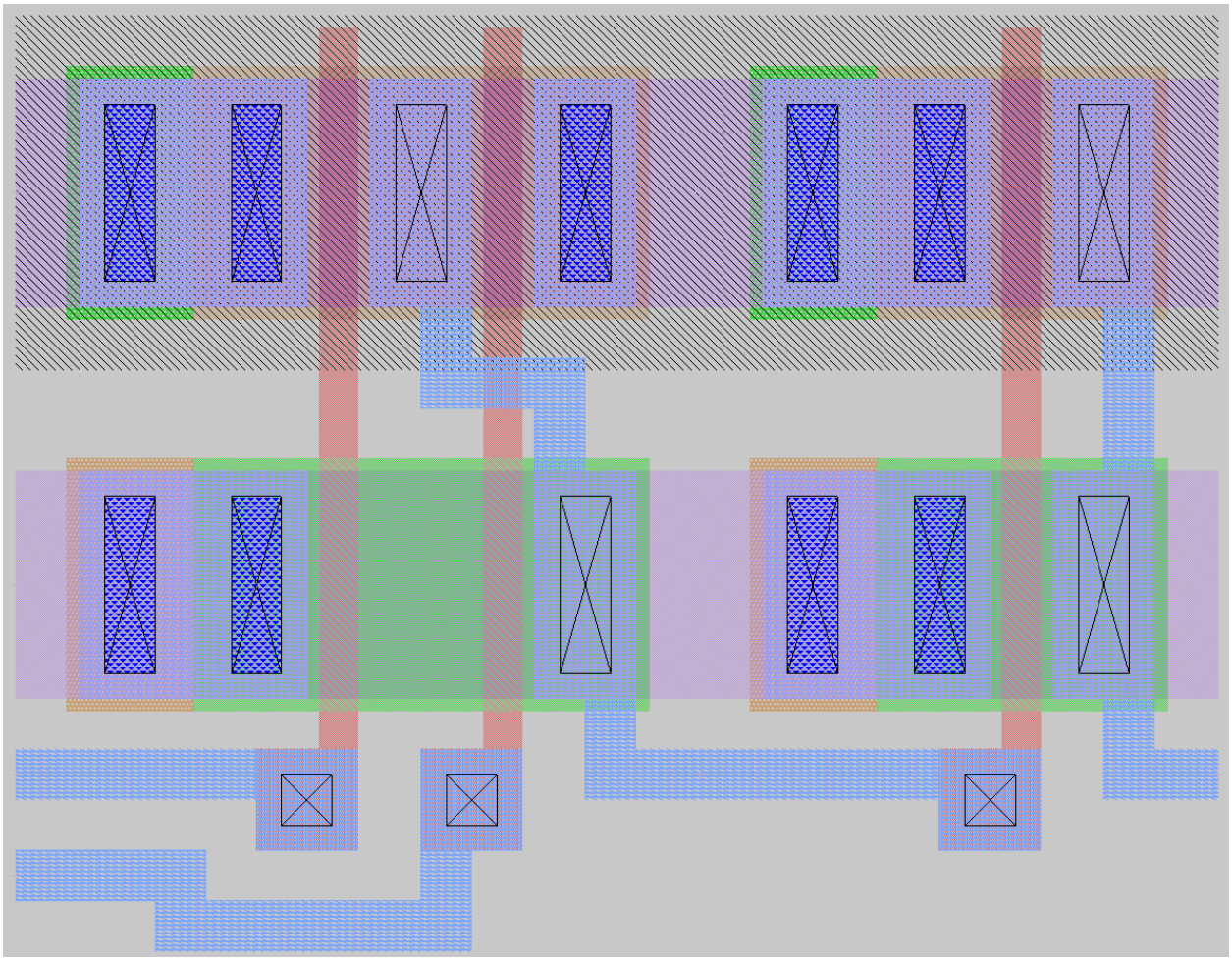


Figure 4: A screenshot of the top-level cell layout of my 2-input AND gate.

3 Layout Versus Schematic

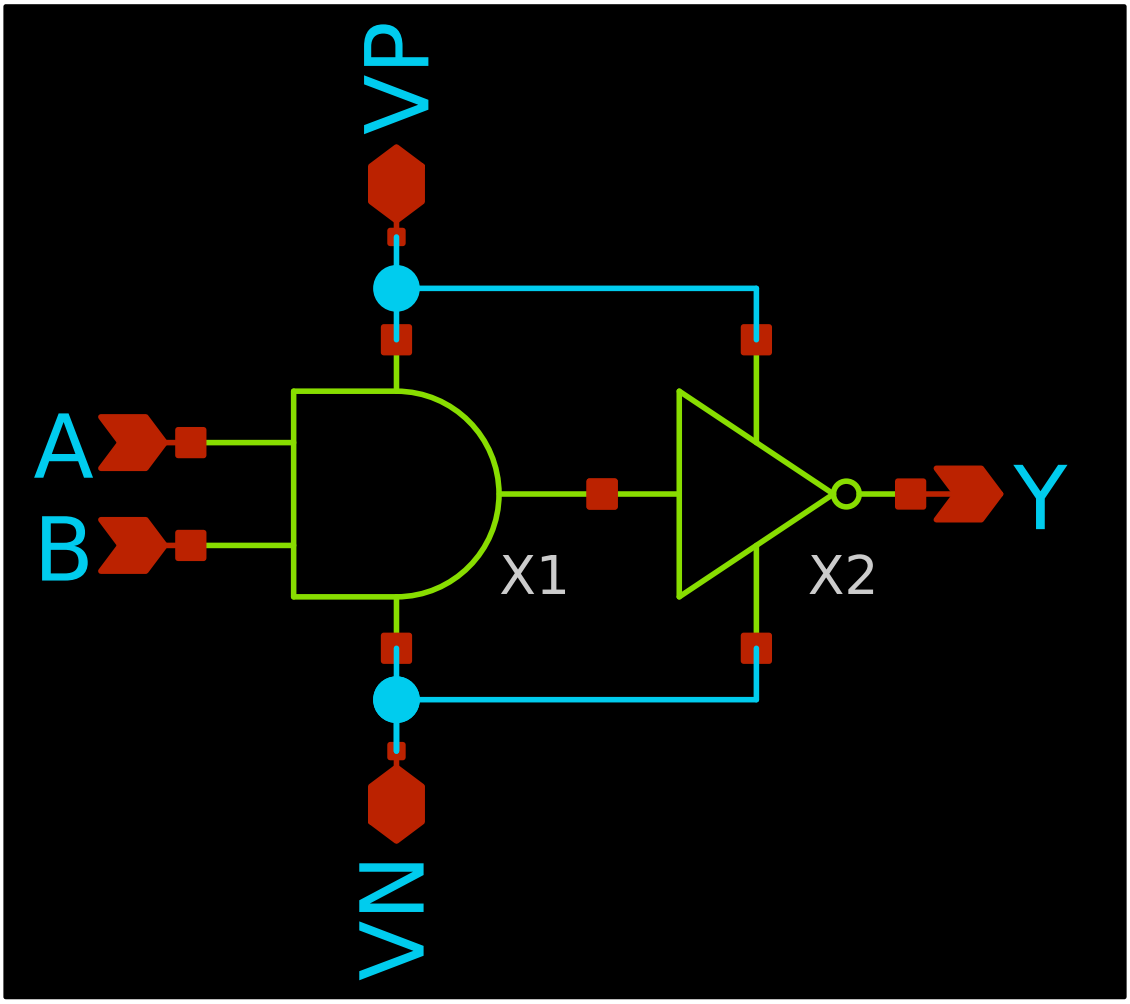


Figure 5: Schematic of my 2-input AND gate separated from the simulation test harness for LVS. Note that the bulk connections of the NAND gate MOSFETs were manually set to VP and VN in the symbol properties to prevent extraneous VDD and GND nets from being created.

3.1 LVS Output Log

The following is the contents of the file `mp1/layout/comp.out` obtained from running the netgen LVS program comparing `mp1/layout/AND2.spice` (Magic netlist) and `mp1/simulation/AND2.spice` (Xschem netlist). It shows that the layout and schematic match.

```
Circuit 1 cell sky130_fd_pr__pfet_01v8 and Circuit 2 cell
   sky130_fd_pr__pfet_01v8 are black boxes.
Equate elements:  no current cell.
Device classes sky130_fd_pr__pfet_01v8 and sky130_fd_pr__pfet_01v8 are
   equivalent.

Circuit 1 cell sky130_fd_pr__nfet_01v8 and Circuit 2 cell
   sky130_fd_pr__nfet_01v8 are black boxes.
Equate elements:  no current cell.
Device classes sky130_fd_pr__nfet_01v8 and sky130_fd_pr__nfet_01v8 are
   equivalent.

Subcircuit summary:
Circuit 1: NAND2                          |Circuit 2: NAND2
------------------------------------------|------------------------------------------
sky130_fd_pr__pfet_01v8 (2)               |sky130_fd_pr__pfet_01v8 (2)
sky130_fd_pr__nfet_01v8 (2)               |sky130_fd_pr__nfet_01v8 (2)
Number of devices: 4                      |Number of devices: 4
Number of nets: 6                         |Number of nets: 6
-------------------------------------------------------------------------------
Netlists match uniquely.

Subcircuit pins:
Circuit 1: NAND2                          |Circuit 2: NAND2
------------------------------------------|------------------------------------------
VP                                        |VP
B                                         |A **Mismatch**
A                                         |B **Mismatch**
Y                                         |Y
VN                                        |VN
-------------------------------------------------------------------------------
Cell pin lists for NAND2 and NAND2 altered to match.
Device classes NAND2 and NAND2 are equivalent.

Subcircuit summary:
Circuit 1: inverter                       |Circuit 2: inverter
------------------------------------------|------------------------------------------
sky130_fd_pr__pfet_01v8 (1)               |sky130_fd_pr__pfet_01v8 (1)
sky130_fd_pr__nfet_01v8 (1)               |sky130_fd_pr__nfet_01v8 (1)
Number of devices: 2                      |Number of devices: 2
Number of nets: 4                         |Number of nets: 4
-------------------------------------------------------------------------------
Netlists match uniquely.

Subcircuit pins:
Circuit 1: inverter                       |Circuit 2: inverter
------------------------------------------|------------------------------------------
Y                                         |Y
```

```
A                                                  |A
VP                                                 |VP
VN                                                 |VN
---------------------------------------------------------------------------

Cell pin lists are equivalent.
Device classes inverter and inverter are equivalent.

Subcircuit summary:
Circuit 1: ../simulation/AND2.spice                |Circuit 2: AND2.spice
---------------------------------------------------|-----------------------
NAND2 (1)                                          |NAND2 (1)
inverter (1)                                       |inverter (1)
Number of devices: 2                               |Number of devices: 2
Number of nets: 6                                  |Number of nets: 6
---------------------------------------------------------------------------

Netlists match uniquely.
Cells have no pins;  pin matching not needed.
Device classes ../simulation/AND2.spice and AND2.spice are equivalent.

Final result: Circuits match uniquely.
.
```

4 Design Files

All of the files for this miniproject can be found at https://github.com/smilg/madvlsi-fa23/tree/main/mp1.