ENGR3426: Miniproject 2

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1 Schematic Capture and Simulation

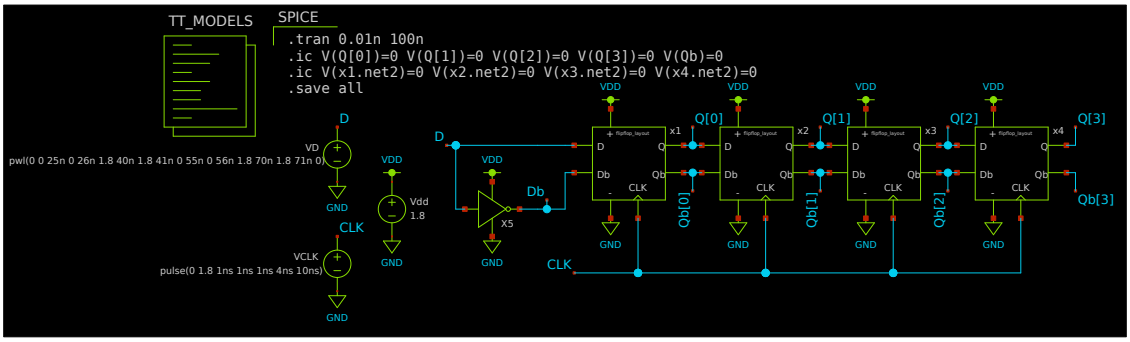

Figure 1: Schematic of my four-bit shift register simulation test harness created in Xschem.

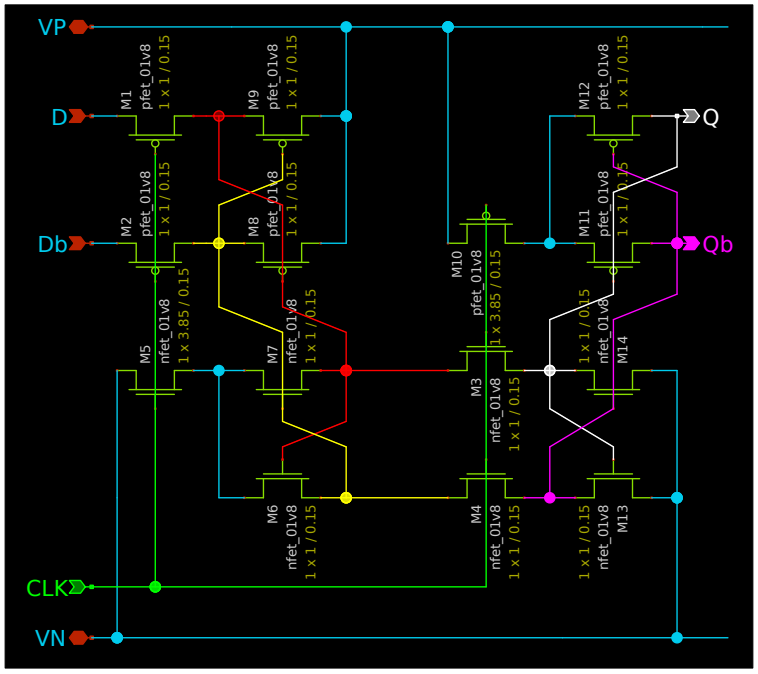

Figure 2: Layout-driven schematic of my D flip-flop created in Xschem. The dimensions of M5 and M10 are altered to account for the non-ratio-less-ness of the CSRL design.

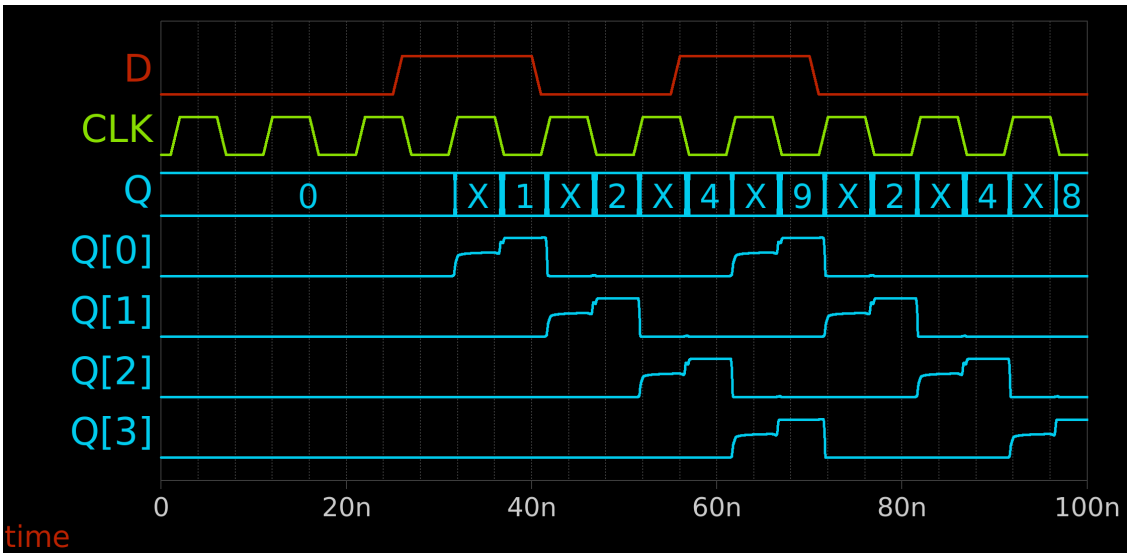

Figure 3: A plot of the output of the simulation of Figure 1. The shift register behaves as expected; the state of D propagates through the flip-flops on each rising edge of CLK.

2 Layout Design

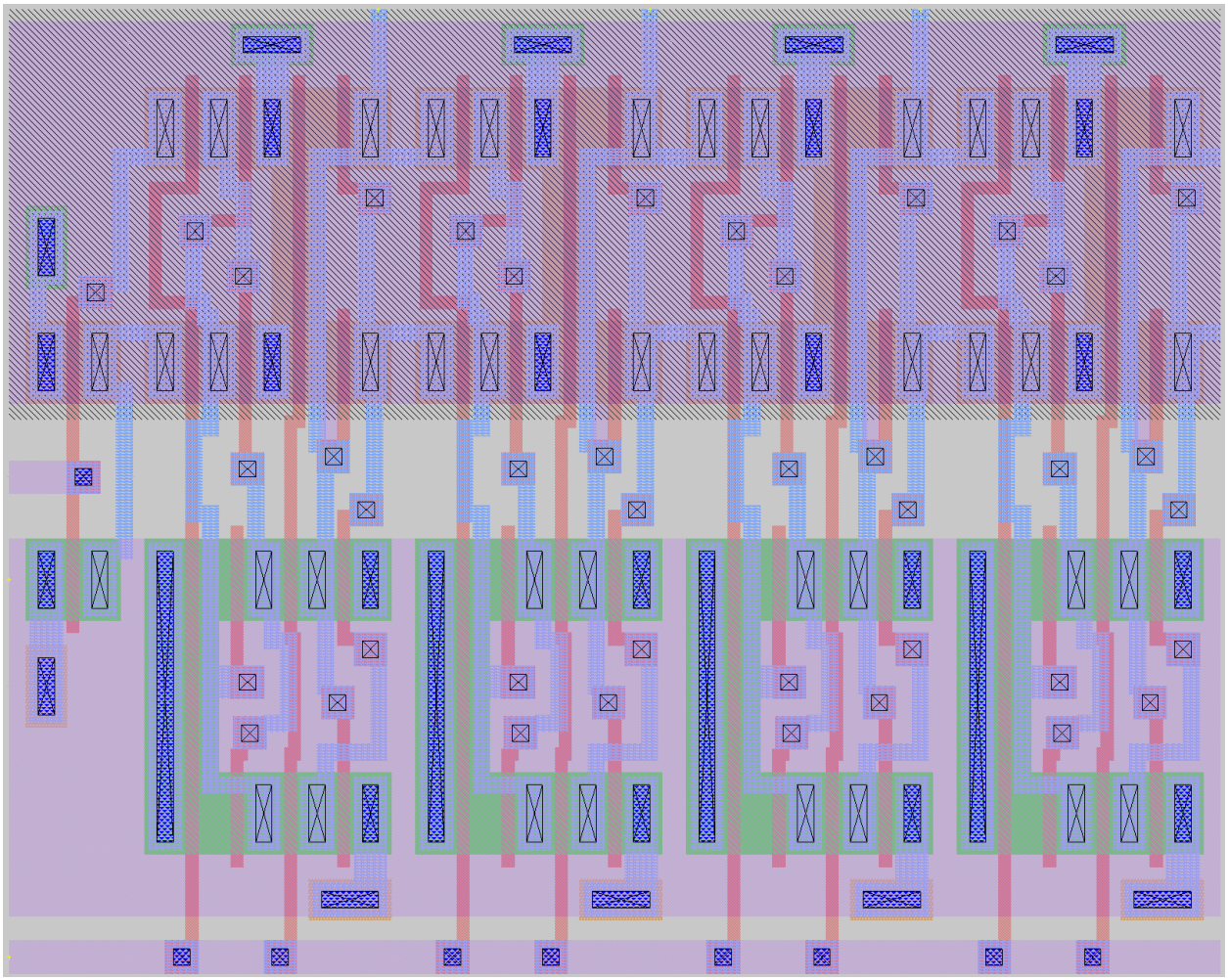

Figure 4: A screenshot of the top-level layout of my four-bit shift register. The overall width of the shift register is 14.750 microns, and the height is 11.750 microns.

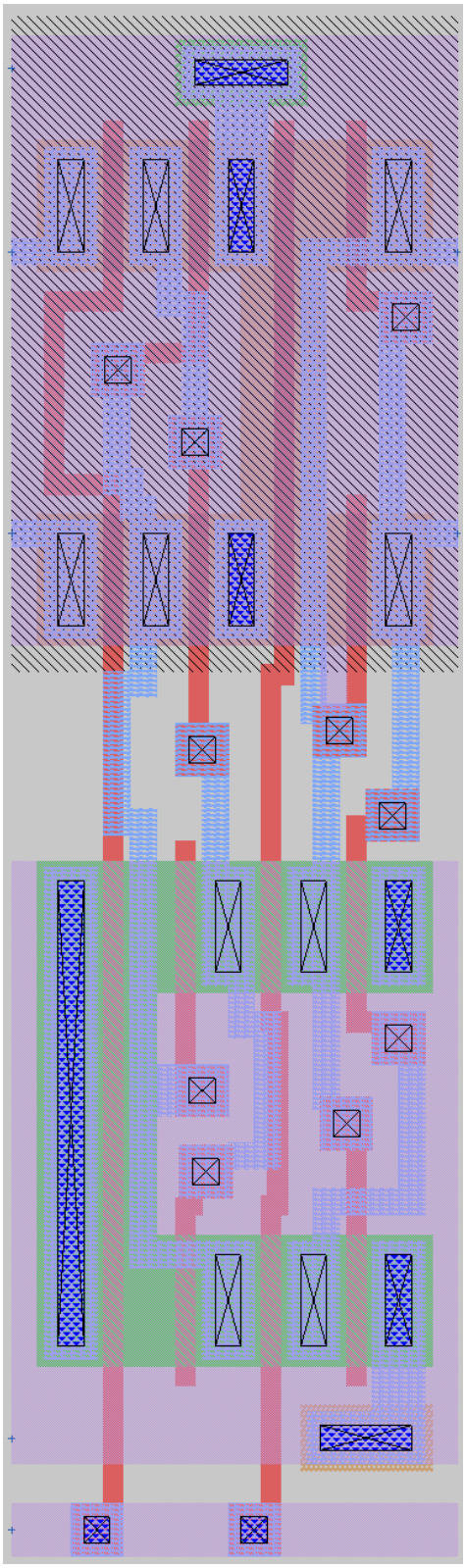

Figure 5: A screenshot of the cell layout of my D flip-flop. The clock signal and power and ground rails are routed horizontally in a metal layer, and the input enters the cell on the left and propagates to the right.

3 Layout Versus Schematic

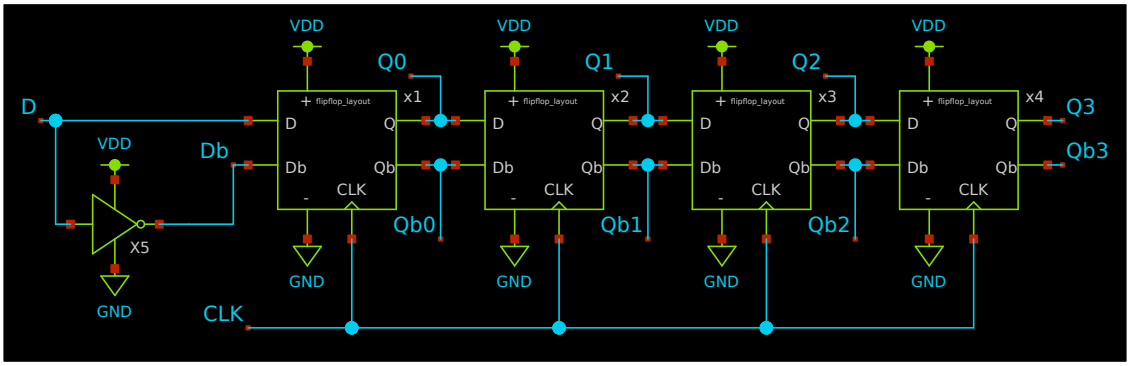

Figure 6: Schematic of my shift register separated from the simulation test harness for LVS.

3.1 LVS Output Log

The following is the contents of the file `mp2/comp.out` obtained from running the netgen LVS program comparing `mp2/layout/shiftreg.spice` (Magic netlist) and `mp2/simulation/shiftreg.spice` (Xschem netlist). It shows that the layout and schematic match.

```
Circuit 1 cell sky130_fd_pr__nfet_01v8 and Circuit 2 cell
    sky130_fd_pr__nfet_01v8 are black boxes.
Equate elements:  no current cell.
Device classes sky130_fd_pr__nfet_01v8 and sky130_fd_pr__nfet_01v8 are
    equivalent.

Circuit 1 cell sky130_fd_pr__pfet_01v8 and Circuit 2 cell
    sky130_fd_pr__pfet_01v8 are black boxes.
Equate elements:  no current cell.
Device classes sky130_fd_pr__pfet_01v8 and sky130_fd_pr__pfet_01v8 are
    equivalent.

Subcircuit summary:
Circuit 1: inverter                     |Circuit 2: inverter
----------------------------------------|----------------------------------------
sky130_fd_pr__nfet_01v8 (1)             |sky130_fd_pr__nfet_01v8 (1)
sky130_fd_pr__pfet_01v8 (1)             |sky130_fd_pr__pfet_01v8 (1)
Number of devices: 2                    |Number of devices: 2
Number of nets: 4                       |Number of nets: 4
----------------------------------------------------------------------------
Netlists match uniquely.

Subcircuit pins:
Circuit 1: inverter                     |Circuit 2: inverter
----------------------------------------|----------------------------------------
Y                                       |Y
A                                       |A
VN                                      |VN
VP                                      |VP
----------------------------------------------------------------------------
```

```
Cell pin lists are equivalent.
Device classes inverter and inverter are equivalent.
Flattening unmatched subcell flipflop_layout in circuit
   simulation/shiftreg.spice (0)(4 instances)
Flattening unmatched subcell flipflop in circuit layout/shiftreg.spice (1)(4
   instances)

Subcircuit summary:
Circuit 1: simulation/shiftreg.spice       |Circuit 2: layout/shiftreg.spice
-------------------------------------------|-------------------------------
inverter (1)                               |inverter (1)
sky130_fd_pr__pfet_01v8 (28)               |sky130_fd_pr__pfet_01v8 (28)
sky130_fd_pr__nfet_01v8 (28)               |sky130_fd_pr__nfet_01v8 (28)
Number of devices: 57                      |Number of devices: 57
Number of nets: 29                         |Number of nets: 29
-------------------------------------------------------------------------

Netlists match uniquely.
Cells have no pins;  pin matching not needed.
Device classes simulation/shiftreg.spice and layout/shiftreg.spice are
   equivalent.

Final result: Circuits match uniquely.
.
```

4 Design Files

All of the files for this miniproject can be found at https://github.com/smilg/madvlsi-fa23/tree/main/mp2.