Parity flag

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In computer processors the **parity flag** indicates if the number of set bits is odd or even in the binary representation of the result of the last operation. It is normally a single bit in a processor status register.

For example, assume a machine where a set parity flag indicates even parity. If the result of the last operation were 26 (11010 in binary), the parity flag would be 0 since the number of set bits is odd. Similarly, if the result were 102 (1100110 in binary) then the parity flag would be 1.

x86 processors

In x86 processors, the parity flag reflects the parity only of the *least significant byte* of the result, and is set if the number of set bits of ones is even. According to 80386 Intel manual, the parity flag is changed in the x86 processor family by the following instructions:

- All arithmetic instructions;
- Compare instruction (equivalent to a subtract instruction without storing the result);
- Logical instructions - XOR, AND, OR;
- the TEST instruction (equivalent to the AND instruction without storing the result).
- the POPF instruction
- the IRET instruction
- an instruction or interrupt that causes a hardware task switch

The parity flag is usually used in conditional jumps, where e.g. the JP instruction jumps to the given target when the parity flag is set and the JNP instruction jumps if it is not set. The flag may be also read directly with instructions such as PUSHF, which pushes the flags register on the stack.

One common reason to test the parity flag is to check an unrelated FPU flag. The FPU has four condition flags (C0 to C3), but they can not be tested directly, and must instead be first copied to the flags register.

When this happens, C0 is placed in the carry flag, C2 in the parity flag and C3 in the zero flag.[1] The C2 flag is set when e.g. incomparable floating point values (NaN or unsupported format) are compared with the FUCOM instructions.

References

1. "Intel 64 and IA-32 Architectures Software Developer's Manual Volume 1: Basic Architecture" (http://www.intel.com/products/processor/manuals/index.htm). January 2011. pp. 97–98.

See also

- x86 architecture
- x86 assembly language
- x86 Flags Register

Categories: Central processing unit