LAB mst worksheet.

Digital eletronics

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* Aim -

Validation of truth tables of logic gates (NOR, NOT, X-OR)

Validate truth table for:-

NOR gate → HD74LS02
NOT gate → HD74LS04
X-OR gate → HD74LS86

* Requirements :-

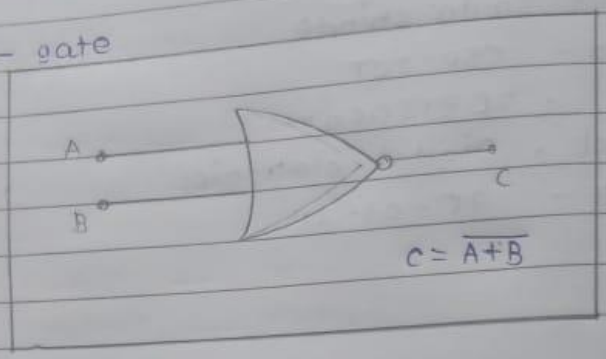
software → thinker-cad

Hardware →

1) Ic 7402, 7404, 7486
2) Breadboard, power supply resistor, LED, connecting wires.

* circuit diagram :-

NOR - gate




logic table :-

logic expression - $\overline{A+B}$

| Input | | Output |
|---|---|---|
| A | B | C |
| 0 | 0 | 1 |
| 0 | 1 | 0 |
| 1 | 0 | 0 |
| 1 | 1 | 0 |

simulation result :-

1) Both in-puts → High
output → low

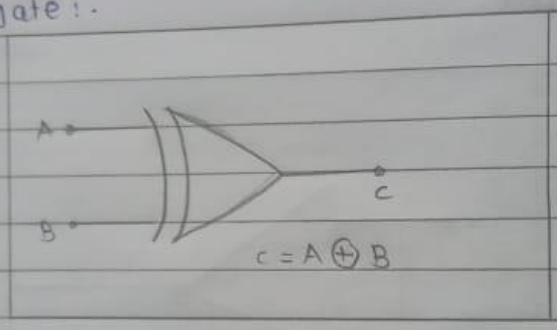
2) one input → low
another input → high
output → low

simulation result :-

1) input → High
   output → Low

2) Input → low
   output → High.

X-OR gate :-




logical table :-

logical expression = $A \oplus B$

$\bar{A} \cdot B + A \cdot \bar{B}$

| input | | Output |
|---|---|---|
| A | B | C |
| 0 | 0 | 0 |
| 0 | 1 | 1 |
| 1 | 0 | 1 |
| 1 | 1 | 0 |

simulation result -

1) Both inputs → High
   output → low

2) one input → low
   another input → High
   output → High

3) one input → High
   anothe input → low
   output → High

4) Both inputs → low
   output → low

consept used →

.) The concept used here are none other than binary logic like low and high at 0 & 1 how to deal with binary logic with the variables to get a logical meaning out of them.

2) In this experiment we are using different Ic gates for different gate.

3) with this ballast resistor is used with LED for checking Ic working or not.

* Learning / observation

1) using their logical expression and logic truth table we design circuit diagram on software thinker-cad.

2) According to their validation when we give input output is showing. acording to their logic table.

* precautions -

1) when we disigning a circuit all connection should be connected accuratly without any sorted connection.

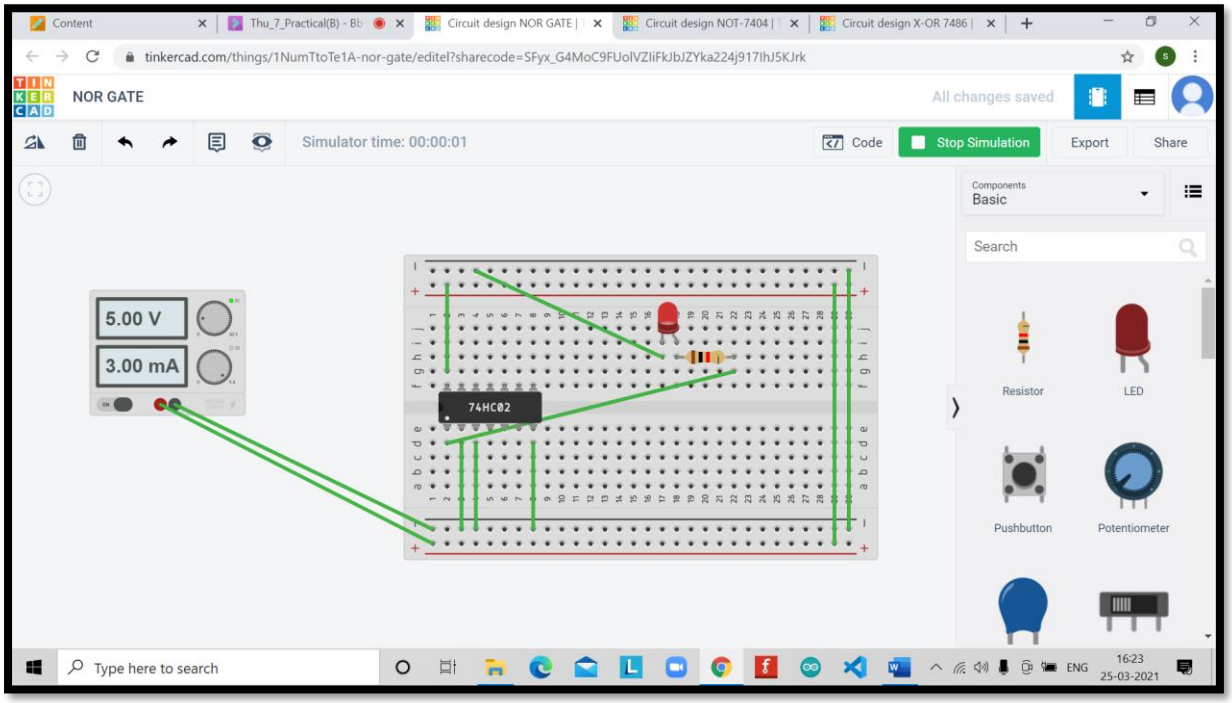
2) input pin should be connected to their IC desining structure.

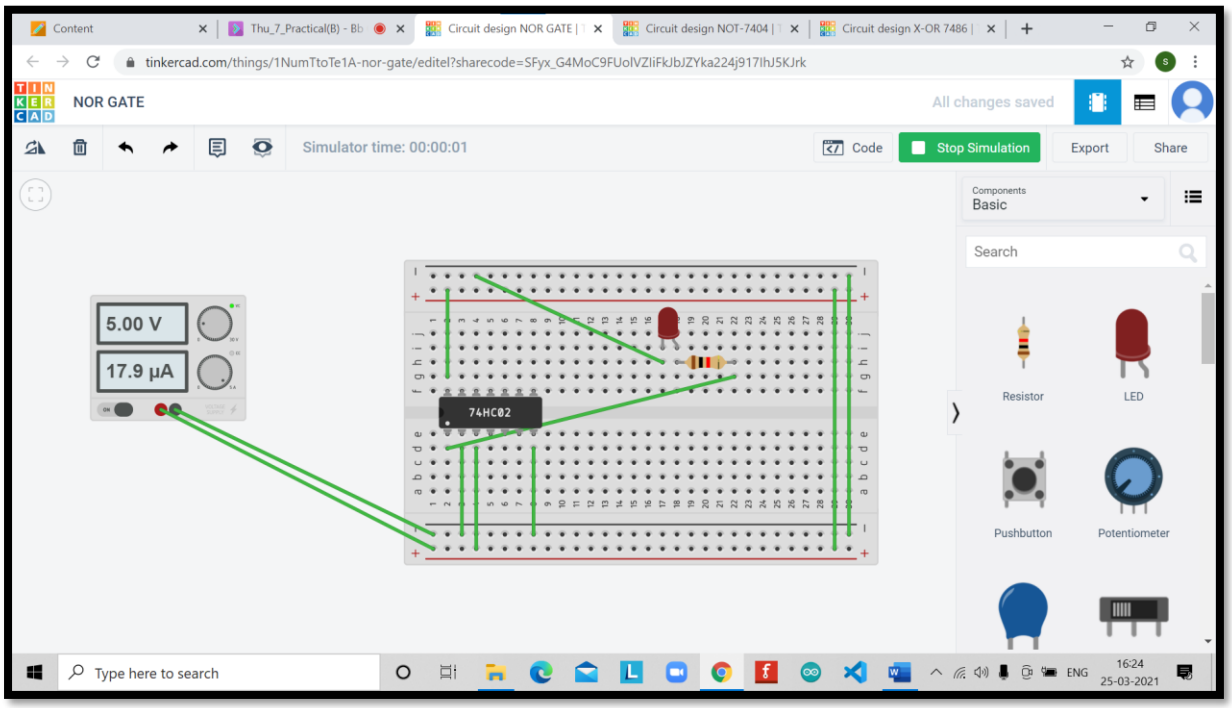
3) grounded pins must be grounded.

* * *

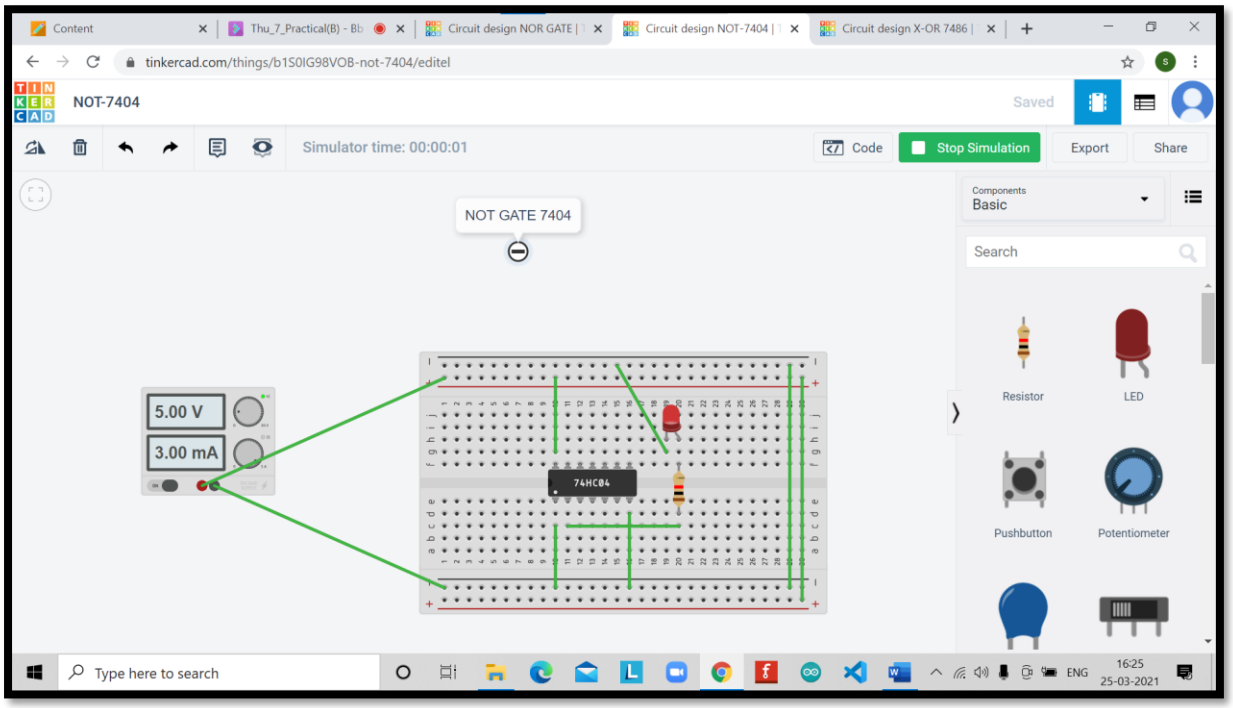
Thank you.

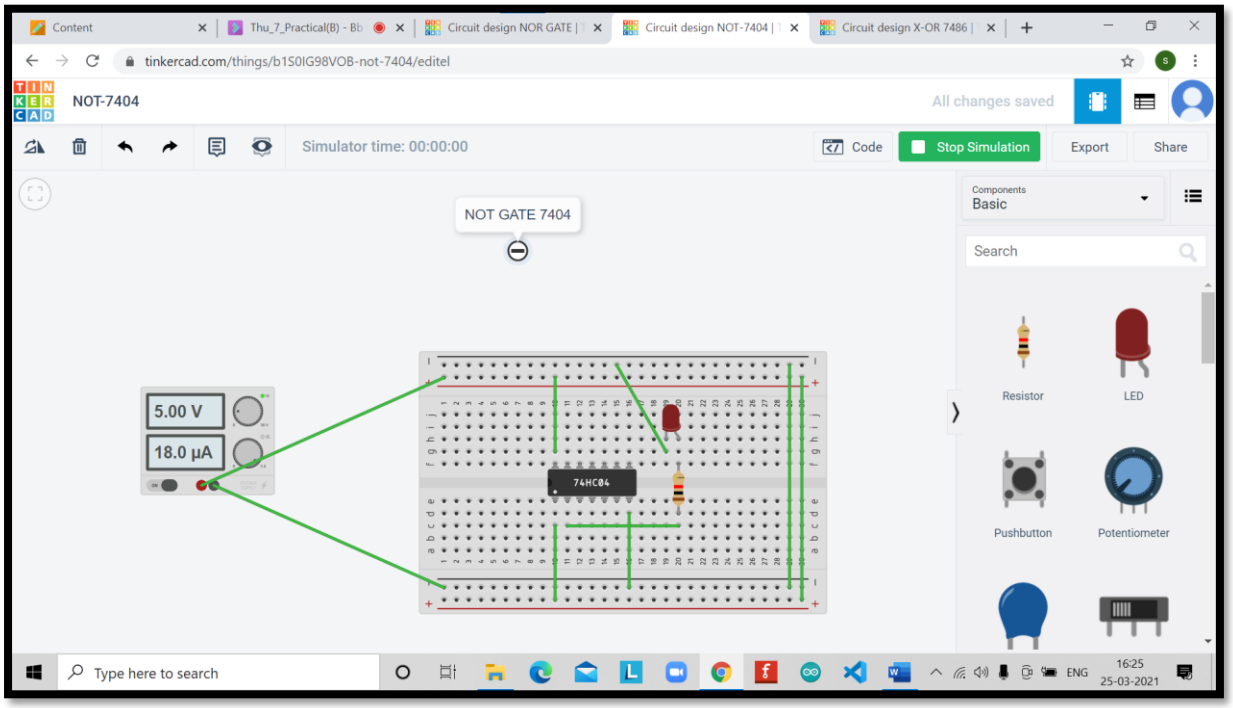
# Simulation result of NOR gate



# Simulation result of NOT gate



# Simulation result of X-OR gate