Ryerson University

Department of Electrical, Computer, & Biomedical Engineering
Faculty of Engineering & Architectural Science

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Instructor:	Dr. Fei Yuan

Assignment/Lab Number:	8
Assignment/Lab Title:	Amplifier Design Project

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Summary & Objective:

The goal of this design project is to design, simulate, analyze, implement, and test a single-supply, multistage, inverting, transistor amplifier which fulfils a set of specifications. The task at hand is to create a circuit that completes all the below tasks efficiently and simply, one where the least components are used to apply real-world understanding as in companies, we'd always be looking to supply the cheapest and most efficient way to implement circuitry. Here in this report, I'll outline what circuit I've gone with, along with other details.

Specifications:

- Power supply: **+10V** relative to the ground;
- Quiescent current drawn from the power supply: **no larger than 10 mA**
- No-load voltage gain (at 1 kHz): **$|A_{vo}|$ = 50 (± 10%);**
- Maximum no-load output voltage swing (at 1 kHz): **no smaller than 8 V peak to peak;**
- Loaded voltage gain (at 1 kHz and with R_L = 1 $k\Omega$): **no smaller than 90% of the no-load voltage gain;**
- Maximum loaded output voltage swing (at 1 kHz and R_L = 1 $k\Omega$): **no smaller than 4 V peak to peak;**
- Input resistance (at 1 kHz): **no smaller than 20 $k\Omega$;**
- Amplifier type: **inverting or non-inverting;**
- Frequency response: **20 Hz to 50 kHz ($-3\ dB$ response);**
- Type of transistors: **BJT;**
- Number of transistors (stages): **no more than 3;**
- Resistances permitted: **values smaller than 220 $k\Omega$ from the E24 series;**
- Capacitors permitted: **0.1 μF, 1.0 μF, 2.2 μF, 4.7 μF, 10 μF, 47 μF, 100 μF, 220 μF;**
- Other components (BJTs, diodes, Zener diodes, etc.): **only from your ELE404 lab kit.**

- The output voltage must be free from distortions (clipping, etc.) in all test conditions.
- The source resistance, Rs, must be 600 Ω for all tests.

The designed amplifier must be AC-coupled for the load and the signal source, but the coupling between its intermediate stages may be of AC or DC type as per the designer's choice. There are no restrictions in terms of using NPN or PNP transistors.

Parameters & Assumptions:

Parameters	Assumptions
- Vcc = 10 V - Vo_pk = 4 V - Vo_pk_load = 2 V - Rin = 20 kΩ - RS = 600 Ω - RL = 1 kΩ - fLow = 20 kHz - fHigh = 50 kHz - Avo = 50 V/V ± 5 V/V - Avsl = 45 V/V ± 5 V/ V - IC_max = 10 mA	- Rout = 100 Ω - VBE_ON = 0.7 V - VCE_SAT = 0.3 V - VT = 25 mV - β = 100

Modes of Operations:

1) Cut - Off	2) Saturation	3) Active
VCE_SAT < 0.3 V	0.1 V < VCE_SAT < 0.3 V	VCE > VCE_SAT

Descriptions of Each Amplifier:

1) CE Amplifier	2) CC Amplifier	3) CB Amplifier
- Rin is large - Ro depends on RE and usually relatively large - The voltage gain is large	- Rin is small - Ro is very small - The voltage gain with or without gain is at most 1	- Non-inverting amplifier - Voltage gain is the same (in magnitude) as a CE; an amplifier that doesn't have emitter degeneration - Small input resistance, if it isn't buffered, It will heavily load the signal or preceding stage

NPN & PNP Transistors:

NPN	PNP
VCE_NPN = VC - VE	VEC_PNP = VE - VC

Project Approach	
1	I decided to go with a CC, CE and CC configuration after thorough analysis. The first CC allowed the Avo value to be near 1, then the next stage CE amplifier will help increase the Avo and help maintain it at near 50V, which is the desired voltage outlined in the design project manual. Lastly, I went with another CC amplifier at the end to ensure that the Avo stayed at the 50V to meet the specifications. There will be more details below, along with all the equations, assumptions, and calculations I've done for this project below, however this is the general approach I started off with.
2	Based on Figure 1, I first made all the resistors unknown (for example, R1, R2…etc) and assumed some values to help me solve and build the circuit.
3	I made a DC circuit and wrote all the equations for each transistor Q1, Q2, Q3 without any values yet, only variables for me to plug and dump.
4	I made an AC circuit and wrote the equations for Ri1, Ri2 and Ri3 (Ri means input resistance for each transistor) and wrote the equations for the voltage gain across each transistor.
5	I used an arbitrary value for all the resistors and based on the equations I wrote and I could do simple increase and decrease relationships (Ohm's Law) to find the suitable resistors for the entire circuit that meets the specifications mentioned in the lab manual.

Trial Design Resistor Values;

Stage 1 CC: Q1 npn 2N3904	Stage 2 CE: Q2 npn 2N3904	Stage 3 CC: Q3 npn 2N3904
- R1= 220 kΩ - R2= 220 kΩ - RE1= 20 kΩ - RC1= 0 Ω - RCS= 100 µF - C12= 100 µF	- R3= 220 kΩ - R4= 220 kΩ - RE2= 220 Ω - RE3= 10 Ω - RC2= 1.0 kΩ - CE2= 10 µF - RE3'= 10 Ω - C12 = C23 = 100 µF	- R5 = 220 kΩ - R6 = 220 kΩ - RE4 = 20 kΩ - RC3 = 0 Ω - RL = 1 kΩ - C23= 100 µF

About Re:

Re is in series with the emitter junction resistance. The early effect, Ro, must be taken into account when we're designing and analyzing these integrated circuits because if we don't have the same order of magnitude of each, it'll produce faulty results.

Equations:

Design Equations: (for CB, CC, and CE Amplifiers):	DC Analysis Equations: (short AC sources and open circuit Capacitors):
RSeries = R1 + R2 α = β/β+1 RParallel = R1 · R2/R1+R2 Voltage_Divider = V · R1/ R1+R2 Current_Divider = I · R2/ R1+R2	- IB_NPN = VCC - VBE_on/ (1+β) · RE +RBB - IB_PNP = VEE - VBB - VBE_on/ (1+β) · RE + RBB - IC = IB · β - IE = (1+β) · IB - VC = VCC - IC · RC - VB = VBB - VE = IE · RE

AC Analysis:

AC Parameters	AC Analysis Equations (short AC sources and open circuit Capacitors):
- Gm= IC/ vT - Re= α/gm - Rπ= β/gm - Ro= VA/ IC	- RBE_EQ = RB/ (1+β) Remove β from RB - REB_EQ = (1+β) · RE Insert β from RB

Emitter Voltage:

- VE_NPN = VB_NPN - 0.7 V
- VE_PNP = VB_PNP - 0.7 V

* R load is relative to the Emitter-Base relationship. Follow current to where the load is at the emitter. The collector is not connected with the base-emitter junction. *

CE Amplifier Impact:

CE Amplifier	
- ACE_VO = - gm · RC - ACE_V = - gm · RParallel (RC ,RL) - ACE_V = - gm · RParallel(RC ,RL)/ 1+ gm - RE - RCE_IN = (β+1)) · re - RCE_IN_RE_re = RSeries(RE , re) · (β+1) - RCE_OUT = RC - RCE_IN = REB_EQ (re, β) - RCE_OUT = RC - ACE_VS = -β · RParallel (RC, RL) / RSeries(RBB , (1+β) · (re+RE))	- Large inverse gain, Small input impedance, Large output impedance - Voltage amplifier

CB Amplifier Impact:

CB Amplifier	
- ACB_VO = gm · RC - ACB_V = gm · RParallel (RC ,RL) - RCB_IN = (β+1) · re - RCB_IN = (β+1) · (RE +re) - RCB_OUT = RC - GCB = α R· Parallel(RC ,RL RL)/ RSeries(RBB , re) - RCB_IN = re - RCB_IN_RE_re = RParallel(RE , re) - RCB_OUT = RC	- Medium Gain, Small input impedance, Medium output impedance - Current amplifier

CC Amplifier Impact:

CC Amplifier	
- ACC_VO = RE/ (RE +re) - ACC_V = RL/ (RL+re) - RCC_IN = (β+1) · re - RCC_IN_LOAD = (β+1)) · (re+RL) - RCC_IN_RE_re = (β+1) · (RE +re) - RCC_OUT = re - ACC_VS = RL/ (RL+re+RBE_EQ(β R, S)) - RCC_IN = REB_EQ(β, RSeries(RL, re)) - RCC_OUT = re - RCC_OUT_RE_re = RSeries(RE , re)	- Unity gain, Large input impedance, Small output impedance - Buffer

DC Analysis Equations

Stage 1 CC: Q1 npn 2N3904	Stage 2 CE: Q2 npn 2N3904	Stage 3 CC: Q3 npn 2N3904
- Vb1 = $\frac{\frac{10}{R12+R2}}{\frac{1}{R12+R2}+\frac{1}{R13+R3}}$ - Ve1 = Vb1 - 0.7 - Ie1 = $\frac{Ve1}{R5}$ - Ic1 = Ie1 - Gm1 = 40Ic1 - Rπ1 = $\frac{\beta}{Gm1}$ - Re1 = $\frac{R\pi 1}{\beta+1}$	- Vb2 = $\frac{\frac{10}{R9}}{\frac{1}{R9}+\frac{1}{R6}}$ - Ve2 = Vb2 - 0.7 - Ie2 = $\frac{Ve2}{R8+R10}$ - Ic2 = Ie2 - Gm2 = 40Ic2 - Rπ2 = $\frac{\beta}{Gm2}$ - Re2 = $\frac{R\pi 2}{\beta+1}$	- Vb3 = $\frac{\frac{10}{R16+R4}}{\frac{1}{R16+R4}+\frac{1}{R14+R15}}$ - Ve3 = Vb3 - 0.7 - Ie3 = $\frac{Ve3}{R11}$ - Ic3 = Ie3 - Gm3 = 40Ic3 - Rπ3 = $\frac{\beta}{Gm3}$ - Re3 = $\frac{R\pi 3}{\beta+1}$

AC Analysis Equations		
- Ri1 = Rπ1 + (β + 1)R5 - Ri2 = Rπ2 + (β + 1)R8 - Ri3 = Rπ3 + (β + 1)R11	- Rin = (R13+R3) || (R12+R2) || (Ri1) - Req1 = R5 || R9 || R6 || Ri2 - Req2 = R7 || (R16 + 4) || (R14 + R15) || Ri3	- $\frac{Vb2}{Vi} = \frac{Gm1\,(Req1)}{1 + Gm1\,(Req1)}$ - $\frac{Vb3}{Vi} = \frac{Gm2\,(Req2)}{1 + Gm2\,(Req2)}$ - $\frac{V0}{Vb3} = \frac{Gm3\,(R11)}{1 + Gm3\,(R11)}$ - $\frac{V0}{Vi} = \frac{V0}{Vb3} * \frac{Vb3}{Vi} * \frac{Vb2}{Vi}$

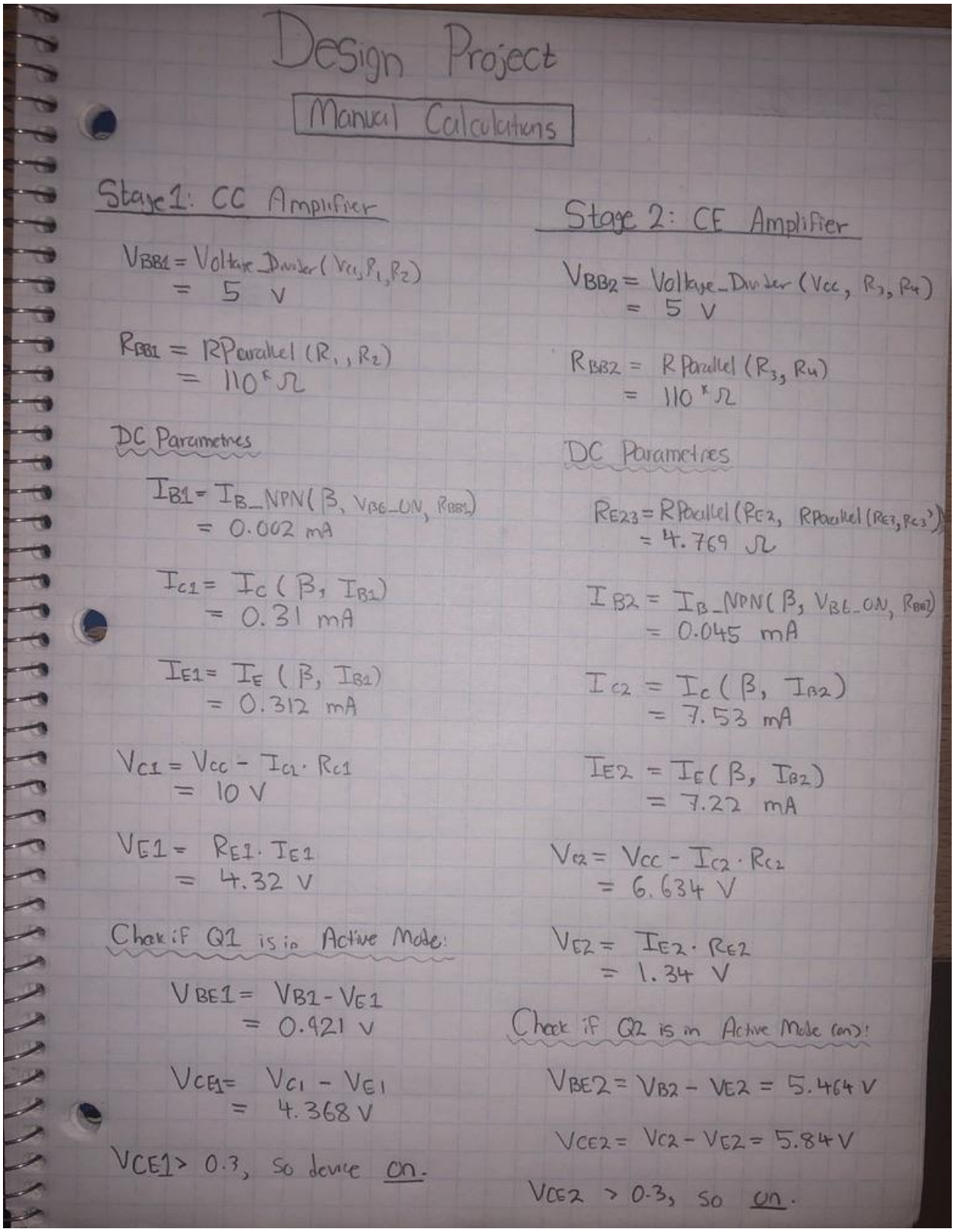
A Few Regards to Circuit Configuration:

Early Effect	Reasons for Q-Current Discrepancies
When someone is designing this circuit, they must take into consideration the early effect, implement it, as well as take Ro into consideration. Since the resistance values are usually around the same order of magnitude, if the designer fails to reproduce it, it'll cause significant discrepancies.	I chose β to be equal to 100. This affects the gain because the actual quiescent is connected to β so it will depend on it where IC= βIβ. There are many reasons why there may be discrepancies in total Q-current, such as the early effect being ignored, resistors not being ideal and the capacitors that have internal resistances. The temperature is another thing that can affect the Q-current which may lead to discrepancies. However, beyond all this, taking all these discrepancies into account, the amplifier should work.

(From Manual Calculations Below):

Percent Difference	Gain Difference
$\left\lvert\frac{y - x}{y}\right\rvert * 100\%$ - Where y = Total_Gain & - Where x = Total_Load_Gain	Gain_Difference = 8.194 - With a Gain_Difference of 8.194%, the amplifier is within range of the specification when the operating Load Resistance is RL = 1 kΩ

Manual Calculations:



Design Project

Manual Calculations

Stage 1: CC Amplifier

$V_{BB1} = Voltage\_Divider(V_{cc}, R_1, R_2)$
$= 5\ V$

$R_{BB1} = RParallel(R_1, R_2)$
$= 110^K\ \Omega$

DC Parametres

$I_{B1} = I_{B\_NPN}(\beta, V_{BE\_ON}, R_{BB1})$
$= 0.002\ mA$

$I_{C1} = I_C(\beta, I_{B1})$
$= 0.31\ mA$

$I_{E1} = I_E(\beta, I_{B1})$
$= 0.312\ mA$

$V_{C1} = V_{CC} - I_{C1} \cdot R_{C1}$
$= 10\ V$

$V_{E1} = R_{E1} \cdot I_{E1}$
$= 4.32\ V$

Check if Q1 is in Active Mode:

$V_{BE1} = V_{B1} - V_{E1}$
$= 0.921\ V$

$V_{CE1} = V_{C1} - V_{E1}$
$= 4.368\ V$

$V_{CE1} > 0.3$, so device on.

Stage 2: CE Amplifier

$V_{BB2} = Voltage\_Divider(V_{cc}, R_3, R_4)$
$= 5\ V$

$R_{BB2} = RParallel(R_3, R_4)$
$= 110^K\ \Omega$

DC Parametres

$R_{E23} = RParallel(R_{E2}, RParallel(R_{E3}, R_{C3}'))$
$= 4.769\ \Omega$

$I_{B2} = I_{B\_NPN}(\beta, V_{BE\_ON}, R_{BB2})$
$= 0.045\ mA$

$I_{C2} = I_C(\beta, I_{B2})$
$= 7.53\ mA$

$I_{E2} = I_E(\beta, I_{B2})$
$= 7.22\ mA$

$V_{C2} = V_{CC} - I_{C2} \cdot R_{C2}$
$= 6.634\ V$

$V_{E2} = I_{E2} \cdot R_{E2}$
$= 1.34\ V$

Check if Q2 is in Active Mode (on):

$V_{BE2} = V_{B2} - V_{E2} = 5.464\ V$

$V_{CE2} = V_{C2} - V_{E2} = 5.84\ V$

$V_{CE2} > 0.3$, so on.

Stage 3: CC Amplifier

$V_{BB3} = \text{Voltage\_Divider}(V_{cc}, R_5, R_6)$
$= 5\ V$

$R_{BB3} = R_{Parallel}(R_5, R_6)$
$= 110^{k}\ \Omega$

DC Parameters

$I_{BB3} = I_{B\_NPN}(\beta, V_{BC\_ON}, R_{BB3})$
$= 0.002\ mA$

$I_{C3} = I_C(\beta, I_{B3})$
$= 0.31\ mA$

$I_{E3} = I_E(\beta, I_{B3})$
$= 0.32\ mA$

$V_{C3} = V_{cc} - I_{C3} \cdot R_{C3}$
$= 10\ V$

$V_{E3} = I_{E3} \cdot R_{E4}$
$= 4.33\ V$

Gain at 2nd Stage CE:

$R_{S2} = R_{cc\_at}(re2) = 4.2\ \Omega$
$R_{L2} = R_{Parallel}(R_{BB2}, R_{EB\_2}(\beta, R_{C23}))$
$= 0.75\ \Omega$
$R_{E12} = R_{Parallel}(R_{BB2}, R_{EB\_2}(\beta, R_{Series}(re3, R_{E4})))$
$= 4.94\ \Omega$

$ACE\_Gain\_2 = ACE\_V\_RE\_re(gm2, R_{C2})$
$= 50.48\ V/V$

$Total\_Loaded\_Gain = (AV\_CC\_1) \cdot (ACE\_Gain\_2) \cdot (Acc\_3\_Gain)$
$= \underline{42.35\ V/V}$

AC Analysis of BJT Project:

Input Impedance at Q1

$R_{E1} = 75\ \Omega$

$R_{L1} = R_{BB2} \parallel (R_{EB\_2} \parallel (\beta \parallel (R_{C2} \parallel R_{C3})))$
$= 0.525^{k}\ \Omega$

$R_{in\_1} = R_{cc\_in\_load}(\beta, re1, R_{L1})$
$= 125.36^{k}\ \Omega$

Output Impedance at Q3:

$R_{out\_3} = R_{cc\_out}(re3)$
$= 64\ \Omega$

Gain Between Q1 & Q2 (CC & CE)

$Av\_CC\_1 = Acc\_VS(R_{C1}, R_{L1}, re1, \beta)$
$= 0.912\ V/V$

Gain from 3rd Stage CC

$Av\_CC\_3 = Acc\_VO(R_{E4}, re3)$
$= 0.988\ V/V$
(without Load)

$Acc\_3\_Gain = Acc\_V(R_{Series}(R_{E23}, R_{C3}), R_L)$
$= 0.931\ V/V$ (with load)

$Total\_Gain = (ACE\_Gain\_2)(AV\_CC\_1) \cdot (AV\_CC\_3)$
$= \underline{46.13\ V/V}$

Circuit Configurations (without load and with load resistance):

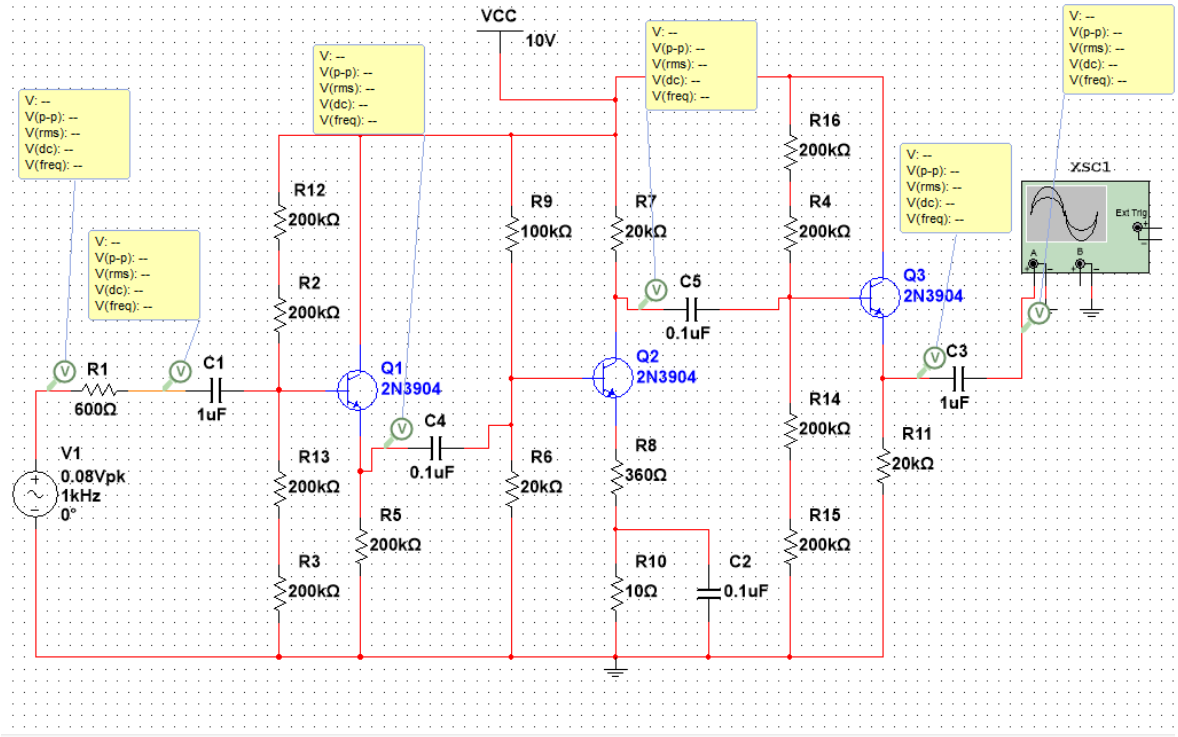


Figure 1: Circuit configuration of CC-CE-CC without any load

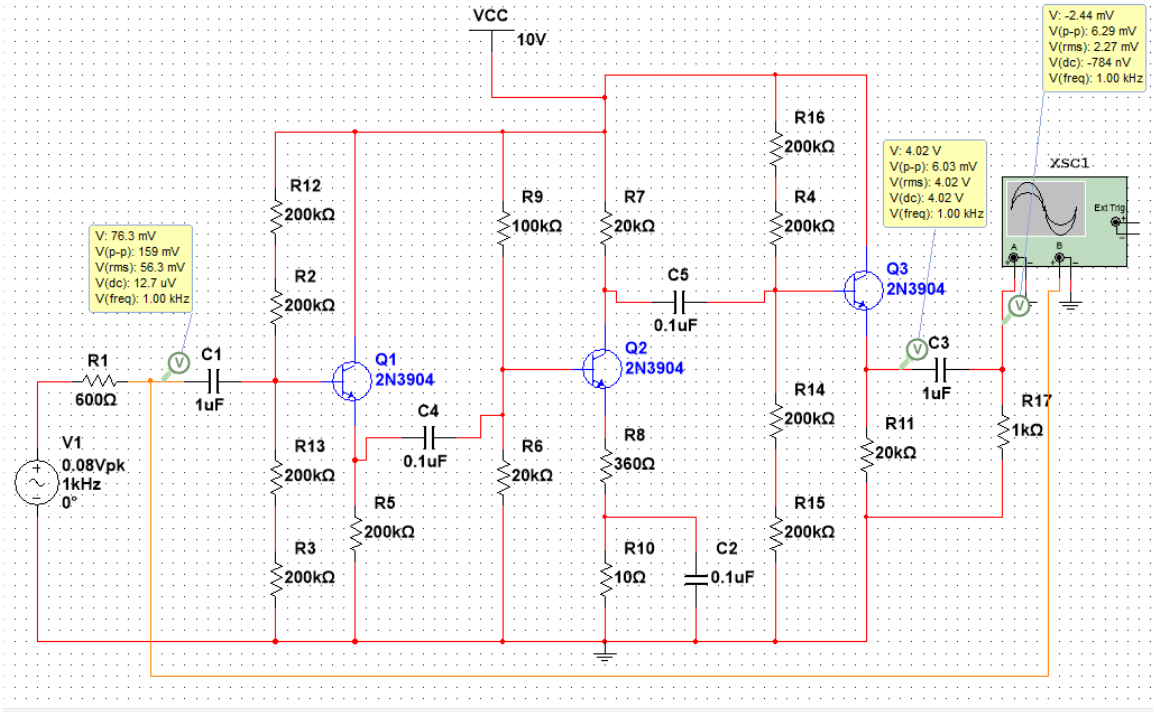


Figure 2: Circuit configuration of CC-CE-CC with load resistance R17 at 1kΩ

Circuit Descriptions:

Figure 1	Figure 2
- This schematic of three stages amplifier without a load and consists of CC then CE then CC. - I used the first stage CC amplifier to provide large Rin, and then the second stage CE amplifier provides a very large gain approximately 50V and then will keep the voltage gain around 50V and won't allow a large decrease in the voltage thereafter.	- This schematic of three stages amplifier with a 1kΩ load and consists of CC then CE then CC. - I used the same specs as Figure 1 but the only difference is that I added the 1kΩ load resistance to the voltage output.

Transistor Design:

Transistor Design		
1st Stage CC	**2nd Stage CE**	**3rd Stage CC**
I picked CC for the 1st stage because I want the voltage gain initially to be as close to 1 as possible. This, in return yields a smaller value for Rin, but it must be more than 50 kΩ and so I fixed it by putting large values for R5 in order to compensate for the smaller Rin.	I chose CE for the 2nd stage in order to obtain large values for the voltage gain and amplify it to near 50V. This is one of the properties CE gives you and in return it'll provide a large Rin.	I used CC one more time at the 3rd and last stage in order to maintain the voltage gain that was obtained by the 2nd stage CE. Since the CE provided a voltage of 50V, I wanted to ensure the values stay around here, however, the CC will try getting small values of Rin for a CC amplifier but I compensate for this by putting a large resistance value at R11.
By combining the 3 characteristics listed above, we get the circuit in figures 1 and 2 with specifications that meet the criteria outlined in the design project lab manual.		

Resistor Design:

Resistor Design		
1st Stage CC	**2nd Stage CE**	**3rd Stage CC**
I first used a voltage divider in order to decrease the voltage passing through Vb1 and I used large values for the resistors to increase Vb1, which will directly increase the Ve1, Ie1 and Ic1 which lead us to our desired specifications.	I chose the resistor that divides the Vcc to multiple streams to be quite moderate through the use of trial and error. First, I put in an extremely large resistance value, and gradually decreased it until I got optimal results at a lower resistance range.	I picked the resistance values for the 3rd stage CC for the same reasons as I chose CC for the 1st stage, mainly just to maintain the voltage gain obtained by the CE amplifier in the 2nd stage.

Waveforms / Graphs:

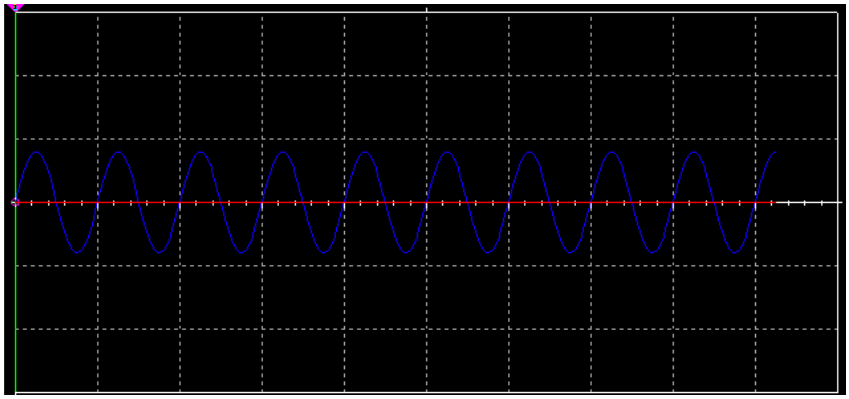


Figure 3: Waveform for Input Voltage Vin

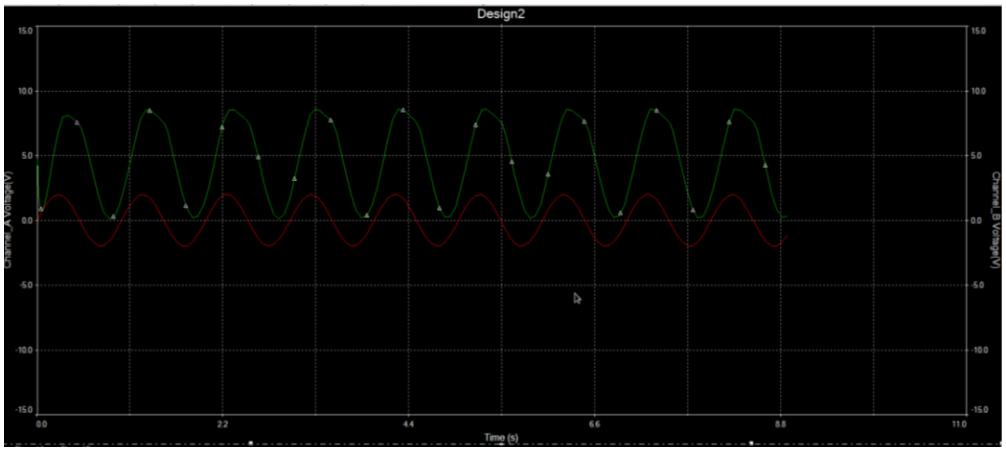


Figure 4: Waveforms for No-Load and Loaded Amplifier

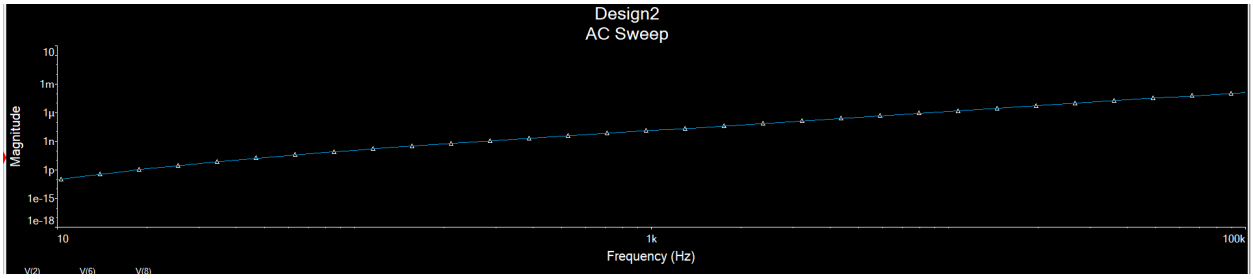


Figure 5: No-Load Magnitude Bode-Plot

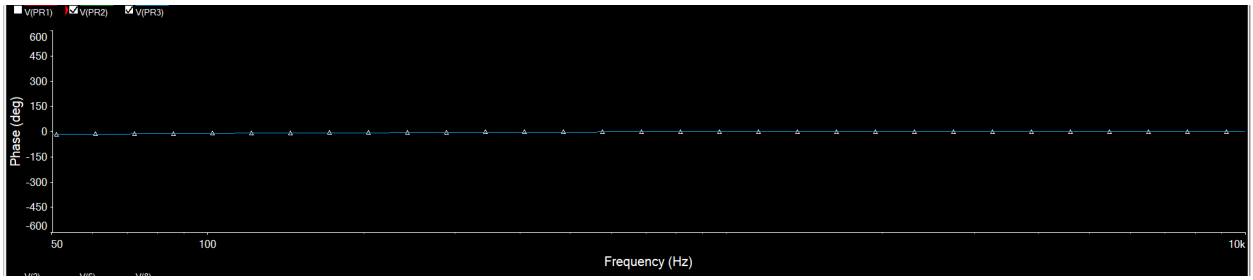


Figure 6: No-Load Phase-Degree Bode-Plot

Figure Descriptions:

Figure 3	Figure 4
Figure 3 represents the waveform for the input Voltage, aka the voltage right at the start near the triangular voltage source.	In this graph, the input signal is Green and the output signal is Red. As we can see, there is slight clipping at around 100mV peak input voltage with about 5V peak with/without load (10V for peak to peak).
Figure 5	**Figure 5**
Obtained above frequency waveform with slight error and discrepancies due to early effects which shows in AC Sweep	Similar goes for Figure 5 Bode Plot for the phase angle, however I couldn't come to a conclusion as to why my angle remained at a constant 0 and the only conclusions I came to was that my term was (jw) only which results in a constant graph.