CSCE 513: Computer Architecture
Project 3

Project #3 requirements are as follows:

1. Design a **single-cycle MIPS processor** based on the datapath from **Module 06**:

   - The developed datapath should support a subset of the MIPS ISA, which includes `LW, SW, BEQ, ADD, ADDI, SUB, J, AND, OR,` and `SLT` instructions.

2. Make sure your module- and port-names will NOT differ with those mentioned below:

```
module single_cycle_mips (
                input logic clk,          // clock signal
                input logic rst_n         //active-low reset signal used
for initialization
);
```

3. Submission is due by **November 14th at 11:59 pm** with up to **seven days late** with a penalty of **10% for each late day**, after which the submission will not be accepted and the grade for the project will be **0**.

4. **Important Note:** NO Questions about the project will be replied after **November 11th**!