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ID NO:-21EL402

Division:-04

Year:-2023-24

Subject:-Digital system Desgin (3EL42)

Branch:-Electronics

Q1 .clock divider

Verilogcode:-

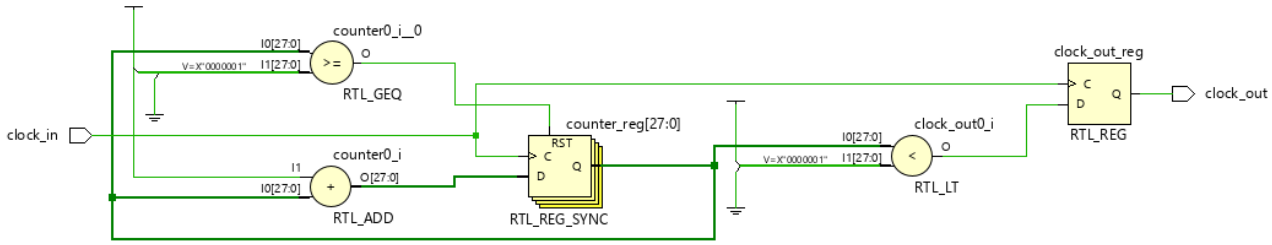
```
input clock_in;
output reg clock_out;
reg[27:0] counter=28'd0;
parameter DIVISOR = 28'd2;
always @(posedge clock_in)
begin
 counter <= counter + 28'd1;
 if(counter>=(DIVISOR-1))
  counter <= 28'd0;
 clock_out <= (counter<DIVISOR/2)?1'b1:1'b0;
end
endmodule
```

testbench:-

```
timescale 1ns / 1ps
module tb_clock_divider;
 reg clock_in;
 wire clock_out;

 Clock_divider uut (
```

```
 .clock_in(clock_in),
 .clock_out(clock_out)
);
initial begin
 clock_in = 0;

      forever #10 clock_in = ~clock_in;
end

endmodule
```

RTlsymetic:-



Synthesis report:-

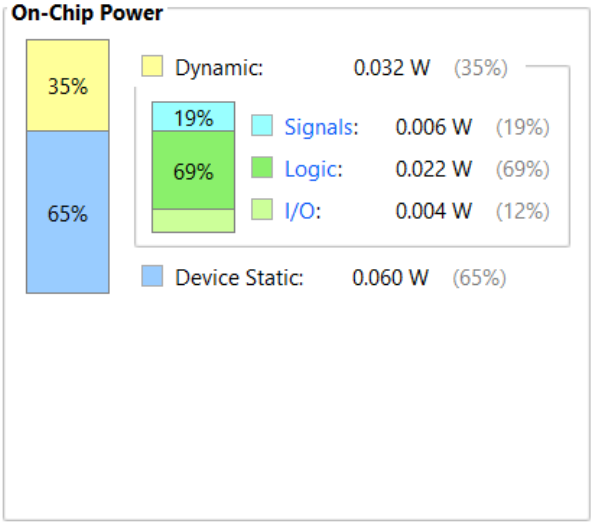
```
Start Writing Synthesis Report
--------------------------------------------------------------------------------

Report BlackBoxes:
+-+--------------+----------+
| |BlackBox name |Instances |
+-+--------------+----------+
+-+--------------+----------+

Report Cell Usage:
+------+-------+------+
|      |Cell   |Count |
+------+-------+------+
|1     |BUFG   |     1|
|2     |CARRY4 |     7|
|3     |LUT1   |     1|
|4     |LUT4   |     1|
|5     |LUT5   |     2|
|6     |LUT6   |     8|
|7     |FDRE   |    29|
|8     |IBUF   |     1|
|9     |OBUF   |     1|
+------+-------+------+
--------------------------------------------------------------------------------
Finished Writing Synthesis Report : Time (s): cpu = 00:00:31 ; elapsed = 00:00:37 . Memory (MB): peak = 1073.102 ; gain = 0.000
```

Power report:-

Power analysis from Implemented netlist. Activity derived from constraints files, simulation files or vectorless analysis.

Total On-Chip Power:	**0.092 W**
Design Power Budget:	**Not Specified**
Power Budget Margin:	**N/A**
Junction Temperature:	**25.6°C**
Thermal Margin:	74.4°C (12.0 W)
Effective ϑJA:	6.2°C/W
Power supplied to off-chip devices:	0 W
Confidence level:	Low

Launch Power Constraint Advisor to find and fix invalid switching activity



Q2. Johnson counter

Verilog code:-

```
module johnson_counter( out,reset,clk);
input clk,reset;
output [3:0] out;

reg [3:0] q;

always @(posedge clk)
begin

if(reset)
 q=4'd0;
 else
       begin
             q[3]<=q[2];
             q[2]<=q[1];
             q[1]<=q[0];
             q[0]<=(~q[3]);
       end
 end

assign out=q;
```

```
endmodule
```

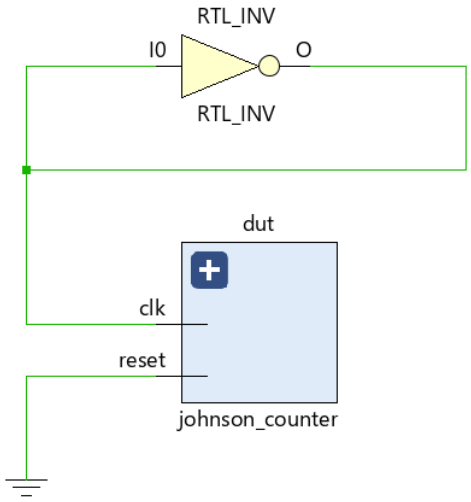
Test bench:-

```
module jc_tb;
  reg clk,reset;
  wire [3:0] out;

  johnson_counter dut (.out(out), .reset(reset), .clk(clk));

  always
    #5 clk =~clk;

  initial begin
    reset=1'b1; clk=1'b0;
   #20 reset= 1'b0;
  end

  initial
    begin
        $monitor( $time, " clk=%b, out= %b, reset=%b",
clk,out,reset);
        #105  $stop;
```

end

endmodule

RTLsymetic:-



Synthesis report:-

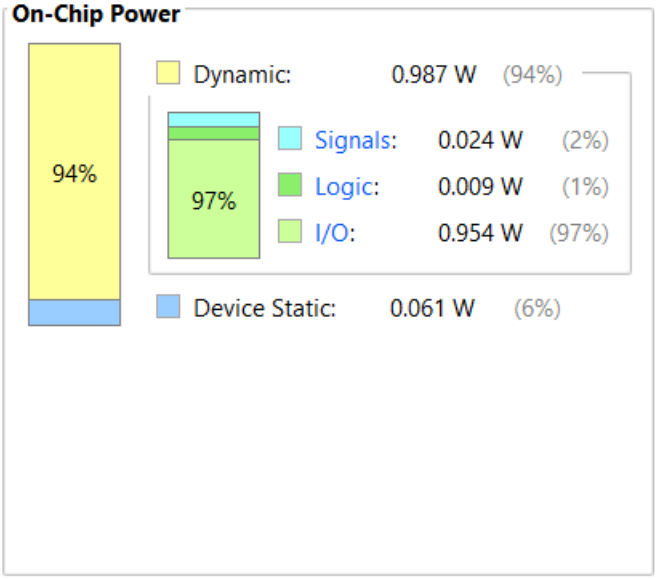
```
Start Writing Synthesis Report
--------------------------------------------------------------------------------

Report BlackBoxes:
+-+--------------+----------+
| |BlackBox name |Instances |
+-+--------------+----------+
+-+--------------+----------+

Report Cell Usage:
+-+-----+------+
| |Cell |Count |
+-+-----+------+
+-+-----+------+
--------------------------------------------------------------------------------
Finished Writing Synthesis Report : Time (s): cpu = 00:00:31 ; elapsed = 00:00:35 . Memory (MB): peak = 1019.730 ; gain = 5.355
--------------------------------------------------------------------------------
```

Powerreport:-

Power analysis from Implemented netlist. Activity derived from constraints files, simulation files or vectorless analysis.

Total On-Chip Power:	**1.048 W**
Design Power Budget:	**Not Specified**
Power Budget Margin:	**N/A**
Junction Temperature:	**30.5°C**
Thermal Margin:	69.5°C (13.1 W)
Effective ϑJA:	5.3°C/W
Power supplied to off-chip devices:	0 W
Confidence level:	Low

Launch Power Constraint Advisor to find and fix invalid switching activity



Q3 .Ring counter

Verilog code:-

```
module four_bit_ring_counter (
      input clock,
      input reset,
  output [3:0] q
    );

  reg[3:0] a;

    always @(posedge clock)
      if (reset)
        a = 4'b0001;

      else
        begin
        a <=  a<<1;
        a[0]<=a[3];
        end

    assign q = a;
```

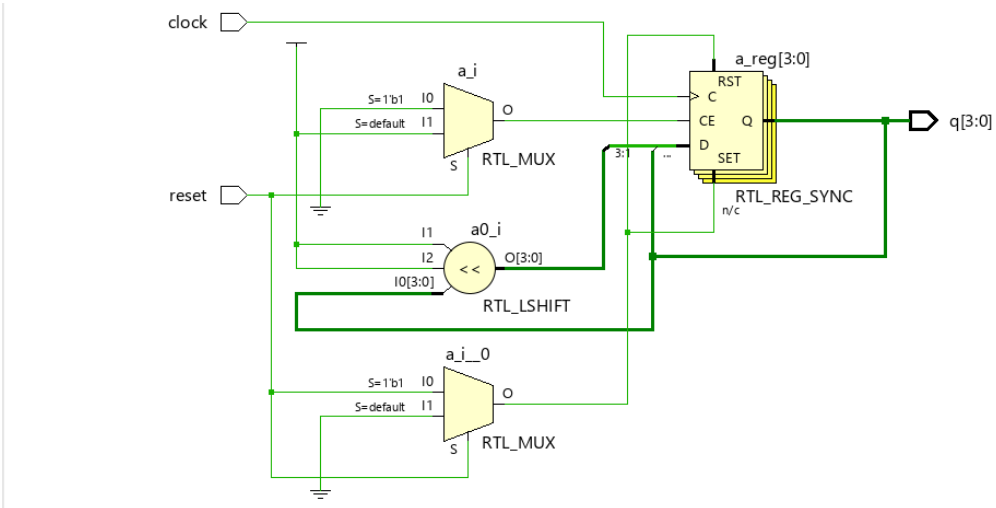
```
 endmodule
```

Test bench:-

```
timescale 1ns / 1ps
module stimulus;
        reg clock;
        reg reset;
  wire[3:0] q;

        four_bit_ring_counter r1 (
      .clock(clock),
      .reset(reset),
      .q(q)
        );

  always #10 clock = ~clock;

        initial begin

    clock = 0;
        reset = 0;
```

```
        #5 reset = 1;
        #20 reset = 0;
        #500 $finish;
    end


            initial begin
        $monitor($time, "
clock=%1b,reset=%1b,q=%4b",clock,reset,q);
            end

endmodule
```

RTlsymetic:-



Synthesis report:-

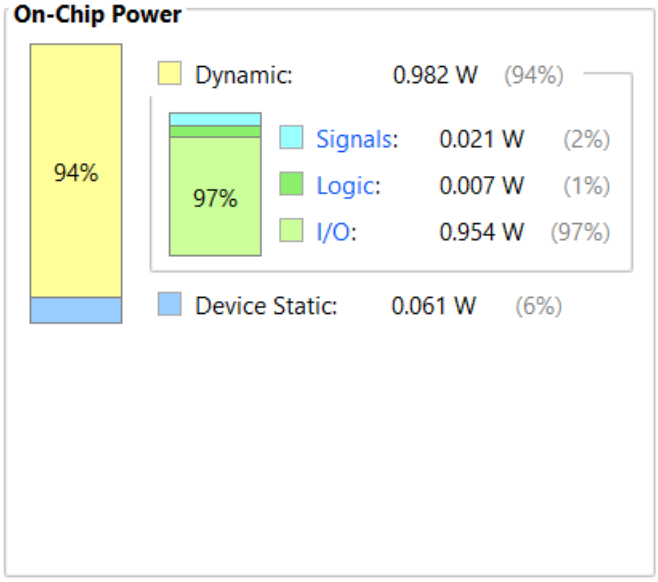
```
Start Writing Synthesis Report
-------------------------------------------------------------------------------

Report BlackBoxes:
+-+--------------+----------+
| |BlackBox name |Instances |
+-+--------------+----------+
+-+--------------+----------+

Report Cell Usage:
+------+-----+------+
|      |Cell |Count |
+------+-----+------+
|1     |BUFG |     1|
|2     |FDRE |     3|
|3     |FDSE |     1|
|4     |IBUF |     2|
|5     |OBUF |     4|
+------+-----+------+
-------------------------------------------------------------------------------
Finished Writing Synthesis Report : Time (s): cpu = 00:00:20 ; elapsed = 00:00:24 . Memory (MB): peak = 1035.621 ; gain = 31.094
-------------------------------------------------------------------------------
```

Power report:-

Power analysis from Implemented netlist. Activity derived from constraints files, simulation files or vectorless analysis.

Total On-Chip Power:	**1.043 W**
Design Power Budget:	**Not Specified**
Power Budget Margin:	**N/A**
Junction Temperature:	**31.5°C**
Thermal Margin:	68.5°C (11.0 W)
Effective ϑJA:	6.2°C/W
Power supplied to off-chip devices:	0 W
Confidence level:	Low

Launch Power Constraint Advisor to find and fix invalid switching activity



Q4 .5 Input Majority circuit

Verilog code:-

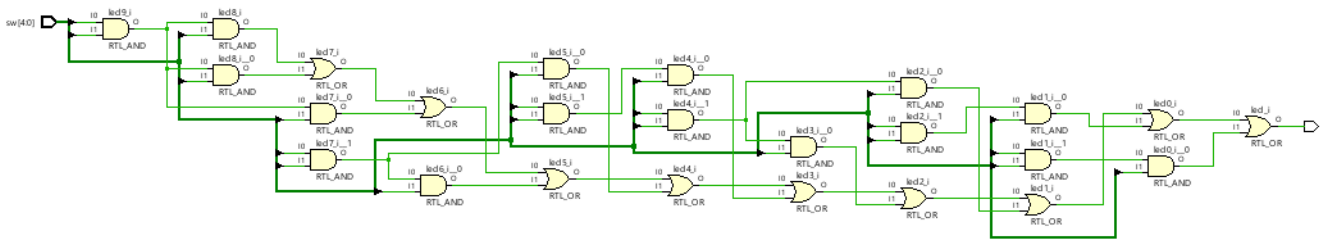
```
module majority_of_five(input [4:0] sw, output led);

assign led =     (sw[0] & sw[1] & sw[2]) |
                 (sw[0] & sw[1] & sw[3]) |
                 (sw[0] & sw[1] & sw[4]) |
                 (sw[0] & sw[2] & sw[3]) |
                 (sw[0] & sw[2] & sw[4]) |
                 (sw[0] & sw[3] & sw[4]) |
                 (sw[1] & sw[2] & sw[3]) |
                 (sw[1] & sw[2] & sw[4]) |
                 (sw[1] & sw[3] & sw[4]) |
                 (sw[2] & sw[3] & sw[4]);
Endmodule
```

Testbench :-

```
`timescale 1ns/ 1ps
module majority_of_five_tb;
reg [4:0] sw;
wire led;
majority_of_five cut (.sw(sw),.led(led));
```

```
integer k;
initial
begin
    sw = 0;
    for (k=0; k<32; k=k+1)
        #20 sw = k;
    #20      $finish;
end
endmodule
```

RTLsymetic:-



Synthesis report:-

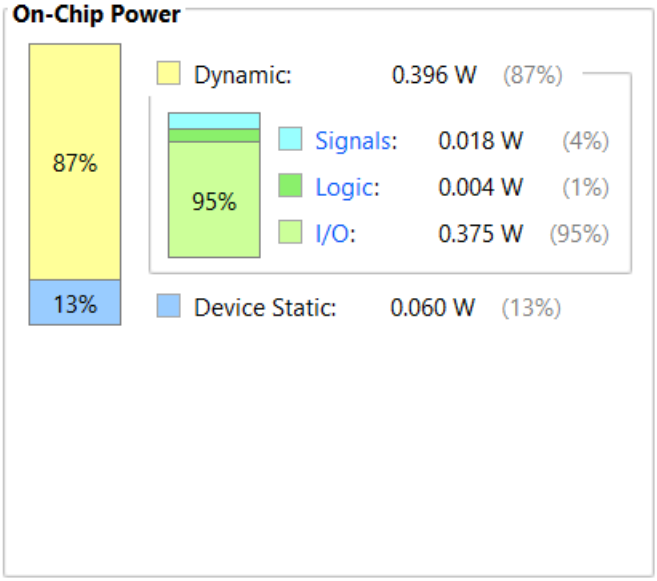
```
Start Writing Synthesis Report
--------------------------------------------------------------------------------

Report BlackBoxes:
+-+--------------+----------+
| |BlackBox name |Instances |
+-+--------------+----------+
+-+--------------+----------+

Report Cell Usage:
+------+-----+------+
|      |Cell |Count |
+------+-----+------+
|1     |LUT5 |     1|
|2     |IBUF |     5|
|3     |OBUF |     1|
+------+-----+------+
--------------------------------------------------------------------------------
Finished Writing Synthesis Report : Time (s): cpu = 00:00:20 ; elapsed = 00:00:24 . Memory (MB): peak = 1035.867 ; gain = 20.54
--------------------------------------------------------------------------------
```

Power report:-

Power analysis from Implemented netlist. Activity derived from constraints files, simulation files or vectorless analysis.

Total On-Chip Power:	**0.456 W**
Design Power Budget:	**Not Specified**
Power Budget Margin:	**N/A**
Junction Temperature:	**27.4°C**
Thermal Margin:	72.6°C (13.7 W)
Effective ϑJA:	5.3°C/W
Power supplied to off-chip devices:	0 W
Confidence level:	Low

Launch Power Constraint Advisor to find and fix invalid switching activity



Q5.Parity Generator

Verelog code:-

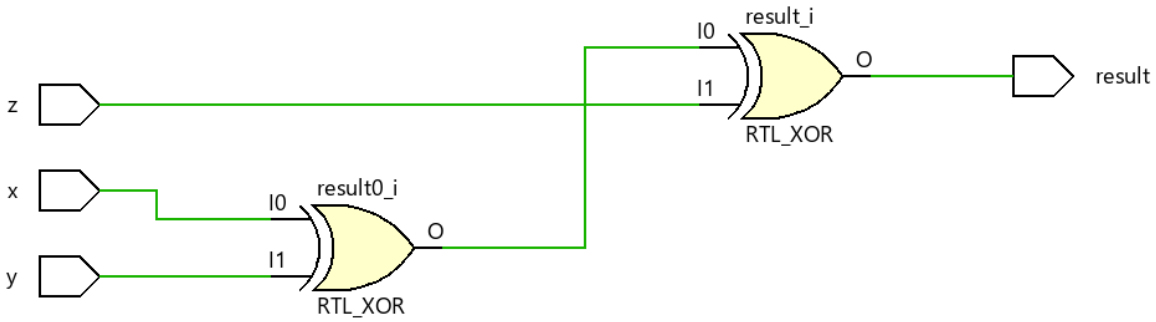
```
module parity(
input x,y,z,
output result);
xor (result,x,y,z);
endmodule
```

Testbench:-

```
initial begin
x = 0;
y = 0;
z = 0;
#100;
x = 0;
y = 0;
z = 1;
#100;
x = 0;
y = 1;
z = 0;
#100;
x = 0;
```

```
y = 1;
z = 1;
#100;
x = 1;
y = 0;
z = 0;
#100;
x = 1;
y = 0;
z = 1;
#100;
x = 1;
y = 1;
z = 0;
#100;
x = 1;
y = 1;
z = 1;
#100;
end
endmodule
```

RTL symetic:-



Synthesis report:-

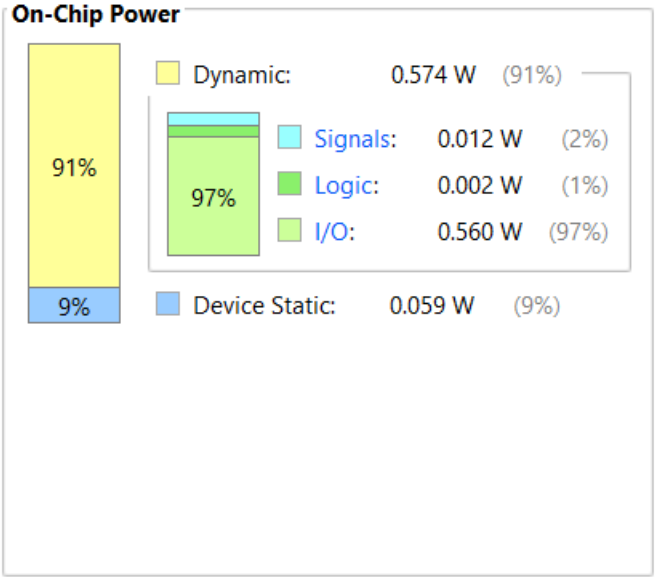
```
Start Writing Synthesis Report
------------------------------------------------------------------------------

Report BlackBoxes:
+-+--------------+----------+
| |BlackBox name |Instances |
+-+--------------+----------+
+-+--------------+----------+

Report Cell Usage:
+------+-----+------+
|      |Cell |Count |
+------+-----+------+
|1     |LUT3 |     1|
|2     |IBUF |     3|
|3     |OBUF |     1|
+------+-----+------+
------------------------------------------------------------------------------
Finished Writing Synthesis Report : Time (s): cpu = 00:00:20 ; elapsed = 00:00:23 . Memory (MB): peak = 1018.910 ; gain = 0.000
```

Power report:-

Power analysis from Implemented netlist. Activity derived from constraints files, simulation files or vectorless analysis.

Total On-Chip Power:	**0.633 W**
Design Power Budget:	**Not Specified**
Power Budget Margin:	**N/A**
Junction Temperature:	**28.3°C**
Thermal Margin:	71.7°C (13.6 W)
Effective ϑJA:	5.3°C/W
Power supplied to off-chip devices:	0 W
Confidence level:	Low

Launch Power Constraint Advisor to find and fix invalid switching activity



Q6 .one hot to binary encoding:-

Verilog code:-

```
module BinaryToOneHotEncoder (
    input [3:0] binary_input,
    output [7:0] one_hot_output
);
    always @(*) begin
        case (binary_input)
            4'b0001: one_hot_output = 8'b00000001;
            4'b0010: one_hot_output = 8'b00000010;
            4'b0100: one_hot_output = 8'b00000100;
            4'b1000: one_hot_output = 8'b00001000;
            default:   one_hot_output = 8'b00000000;
        endcase
    end
endmodule
```

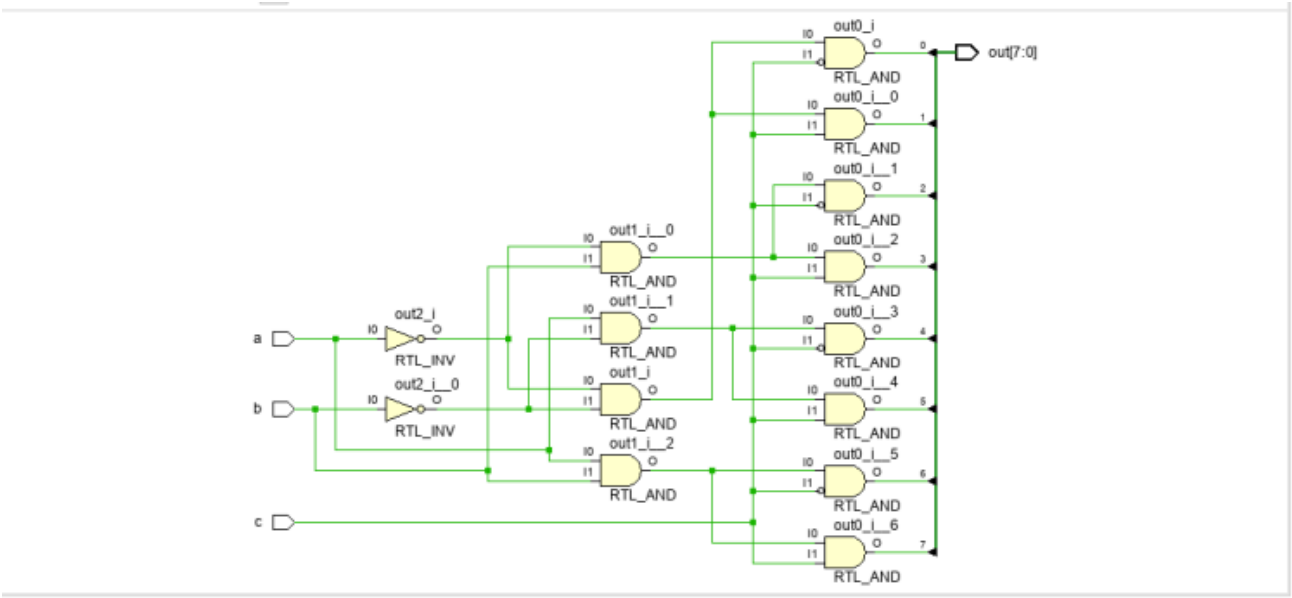
Testbench:-

```
    reg [3:0] binary_input;
    wire [7:0] one_hot_output;

    BinaryToOneHotEncoder UUT (
```

```
        .binary_input(binary_input),
        .one_hot_output(one_hot_output)
    );

    initial begin
        $display("Testing Binary to One-Hot Encoder");
        binary_input = 4'b0000;
        #10 $display("Input: %b, Output: %b", binary_input,
one_hot_output);

        binary_input = 4'b0001;
        #10 $display("Input: %b, Output: %b", binary_input,
one_hot_output);

        binary_input = 4'b0010;
        #10 $display("Input: %b, Output: %b", binary_input,
one_hot_output);

        binary_input = 4'b0100;
        #10 $display("Input: %b, Output: %b", binary_input,
one_hot_output);

        binary_input = 4'b1000;
```

```
        #10 $display("Input: %b, Output: %b", binary_input,
one_hot_output);

        binary_input = 4'b1010; // Invalid input
        #10 $display("Input: %b, Output: %b", binary_input,
one_hot_output);

        $finish;
    end
endmodule
```

RTLsynthesis:-



Synthesis report:-

```
---------------------------------------------------------------------------------
Start Writing Synthesis Report
---------------------------------------------------------------------------------

Report BlackBoxes:
+-+--------------+----------+
| |BlackBox name |Instances |
+-+--------------+----------+
+-+--------------+----------+

Report Cell Usage:
+------+-----+------+
|      |Cell |Count |
+------+-----+------+
|1     |LUT3 |     8|
|2     |IBUF |     3|
|3     |OBUF |     8|
+------+-----+------+

Report Instance Areas:
+------+---------+-------+------+
|      |Instance |Module |Cells |
+------+---------+-------+------+
|1     |top      |       |    19|
+------+---------+-------+------+
---------------------------------------------------------------------------------
Finished Writing Synthesis Report : Time (s): cpu = 00:00:17 ; elapsed = 00:00:30 . Memory (MB): peak = 1019.449 ; gain = 0.000
---------------------------------------------------------------------------------
```

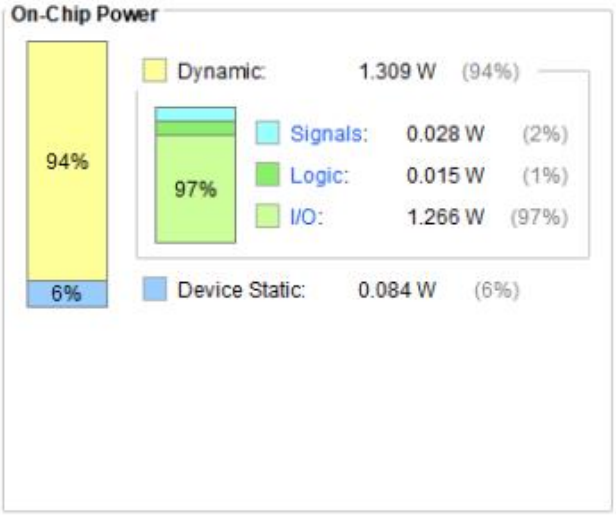
Power report:-

Summary

Power analysis from Implemented netlist. Activity derived from constraints files, simulation files or vectorless analysis.

Total On-Chip Power:	**1.393 W**
Design Power Budget:	**Not Specified**
Power Budget Margin:	**N/A**
Junction Temperature:	**27.6°C**
Thermal Margin:	57.4°C (30.3 W)
Effective ϑJA:	1.9°C/W
Power supplied to off-chip devices:	0 W
Confidence level:	Low

Launch Power Constraint Advisor to find and fix invalid switching activity



Q7 . 4-BIT BCD SYNCHRONOUS COUNTER

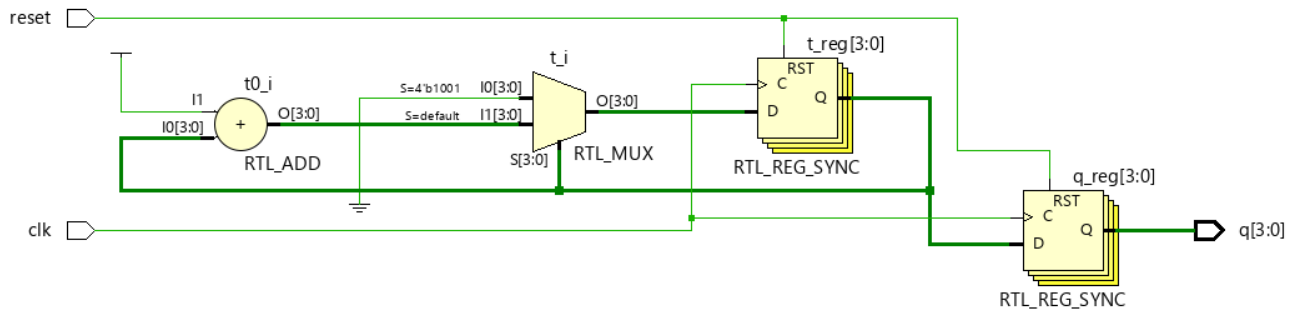
Verilog code:-

```
timescale 1ns / 1ps
module bcd_counter(input clk, reset, output reg [3:0] q);
reg [3:0] t;
always @ (posedge clk) begin
  if (reset)
  begin
    t <= 4'b0000;
    q <= 4'b0000;
  end
  else
  begin
    t <= t + 1;
    if (t == 4'b1001)
    begin
      t <= 4'b0000;
    end
    q <= t;
  end
end
endmodule
```

Testbench:-

```
module bcd_counter_tb;
reg clk;
reg reset;
wire [3:0] q;

bcd_counter DUT(.clk(clk), .reset(reset), .q(q));
initial begin
  clk = 0;
  forever #5 clk = ~clk;
end

initial begin
  reset = 1;
  #10 reset = 0;
   $monitor ("T=%0t out=%b", $time, q);
  #150 reset = 1;
 #10 reset = 0;
 #200
 $finish;
 end
endmodule
```

RTLsymetic:-



Synthesis report:-

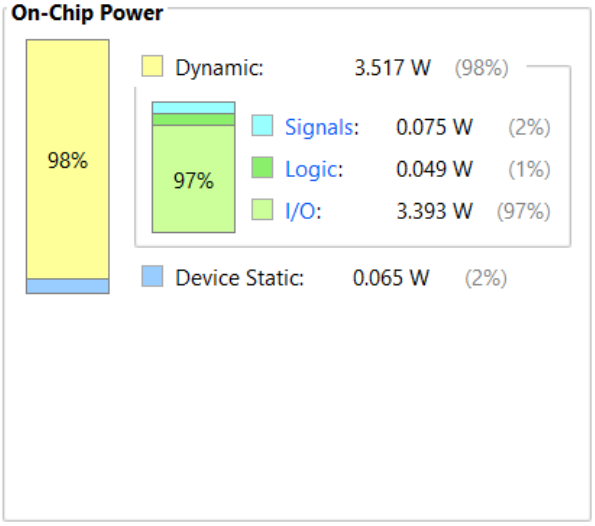
```
Start Writing Synthesis Report
--------------------------------------------------------------------------------

Report BlackBoxes:
+-+--------------+----------+
| |BlackBox name |Instances |
+-+--------------+----------+
+-+--------------+----------+

Report Cell Usage:
+------+-----+------+
|      |Cell |Count |
+------+-----+------+
|1     |BUFG |     1|
|2     |LUT1 |     1|
|3     |LUT3 |     1|
|4     |LUT4 |     2|
|5     |FDRE |     8|
|6     |IBUF |     2|
|7     |OBUF |     4|
+------+-----+------+
--------------------------------------------------------------------------------
Finished Writing Synthesis Report : Time (s): cpu = 00:00:19 ; elapsed = 00:00:25 . Memory (MB): peak = 1032.949 ; gain = 16.547
--------------------------------------------------------------------------------
```

Power report:-

Power analysis from Implemented netlist. Activity derived from constraints files, simulation files or vectorless analysis.

Total On-Chip Power:	**3.582 W**
Design Power Budget:	**Not Specified**
Power Budget Margin:	**N/A**
Junction Temperature:	**43.9°C**
Thermal Margin:	56.1°C (10.6 W)
Effective ϑJA:	5.3°C/W
Power supplied to off-chip devices:	0 W
Confidence level:	Low

Launch Power Constraint Advisor to find and fix invalid switching activity



Q8 4-BIT CARRY LOOKAHEAD ADDER

Verilog code:-

```
module CarryLookAheadAdder(
  input [3:0]A, B,
  input Cin,
  output [3:0] S,
  output Cout
);
  wire [3:0] Ci;

  assign Ci[0] = Cin;
  assign Ci[1] = (A[0] & B[0]) | ((A[0]^B[0]) & Ci[0]);

  assign Ci[2] = (A[1] & B[1]) | ((A[1]^B[1]) & ((A[0] &
B[0]) | ((A[0]^B[0]) & Ci[0])));

  assign Ci[3] = (A[2] & B[2]) | ((A[2]^B[2]) & ((A[1] &
B[1]) | ((A[1]^B[1]) & ((A[0] & B[0]) | ((A[0]^B[0]) &
Ci[0])))));
```

```
  assign Cout  = (A[3] & B[3]) | ((A[3]^B[3]) & ((A[2] & B[2]) | ((A[2]^B[2]) & ((A[1] & B[1]) | ((A[1]^B[1]) & ((A[0] & B[0]) | ((A[0]^B[0]) & Ci[0])))))));


  assign S = A^B^Ci;
```

Testbench:-

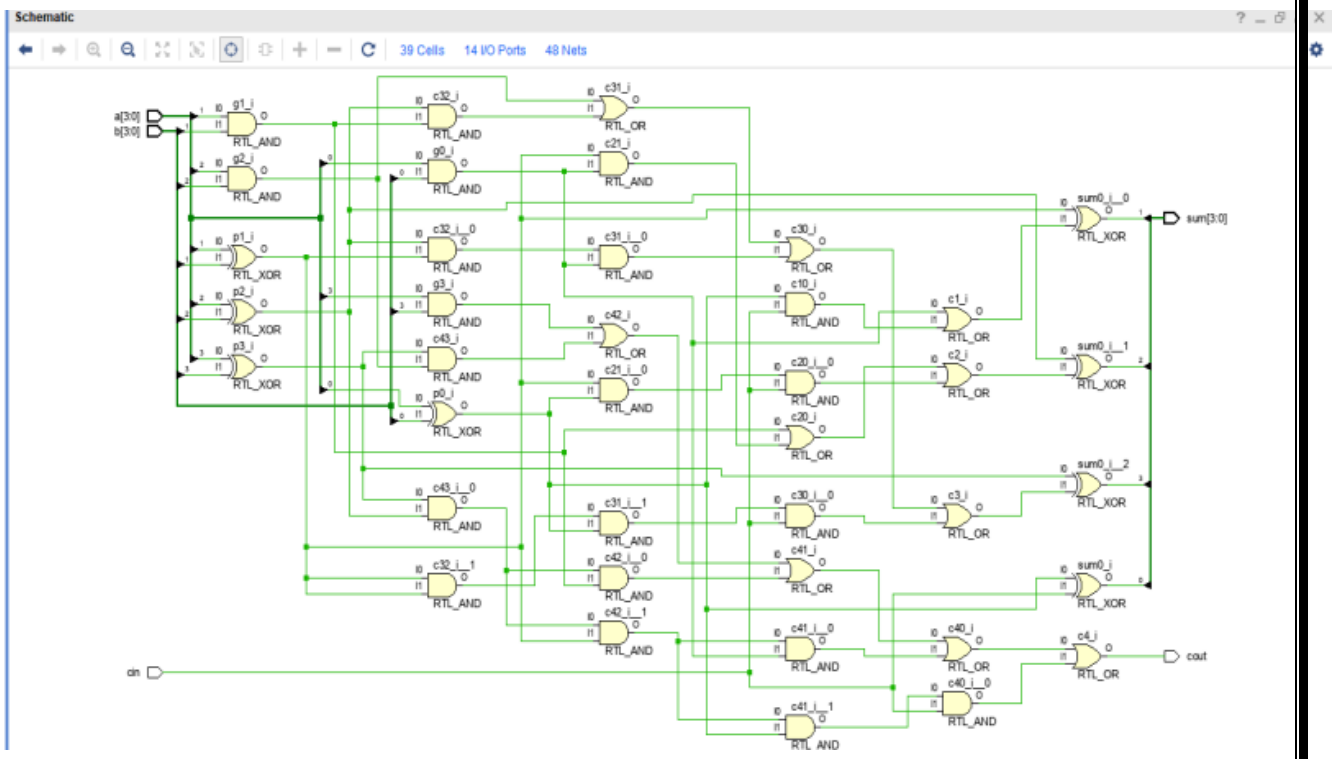
```
module TB;
  reg [3:0]A, B;
  reg Cin;
  wire [3:0] S;
  wire Cout;
  wire[4:0] add;

  CarryLookAheadAdder cla(A, B, Cin, S, Cout);

  assign add = {Cout, S};
  initial begin
    $monitor("A = %b: B = %b, Cin = %b --> S = %b, Cout = %b, Addition = %0d", A, B, Cin, S, Cout, add);
    A = 1; B = 0; Cin = 0; #3;
    A = 2; B = 4; Cin = 1; #3;
    A = 4'hb; B = 4'h6; Cin = 0; #3;
```

A = 5; B = 3; Cin = 1;

end

endmodule

RTL symetic:-



Synthesis report:-

```
Start Writing Synthesis Report
--------------------------------------------------------------------------------

Report BlackBoxes:
+-+--------------+----------+
| |BlackBox name |Instances |
+-+--------------+----------+
+-+--------------+----------+

Report Cell Usage:
+------+-----+------+
|      |Cell |Count |
+------+-----+------+
|1     |LUT2 |     1|
|2     |LUT3 |     1|
|3     |LUT4 |     1|
|4     |LUT5 |     4|
|5     |LUT6 |     2|
|6     |IBUF |     9|
|7     |OBUF |     5|
+------+-----+------+

Report Instance Areas:
+------+---------+-------+------+
|      |Instance |Module |Cells |
+------+---------+-------+------+
|1     |top      |       |    23|
+------+---------+-------+------+
--------------------------------------------------------------------------------
Finished Writing Synthesis Report : Time (s): cpu = 00:00:18 ; elapsed = 00:00:32 . Memory (MB): peak = 1015.535 ; gain = 0.000
```

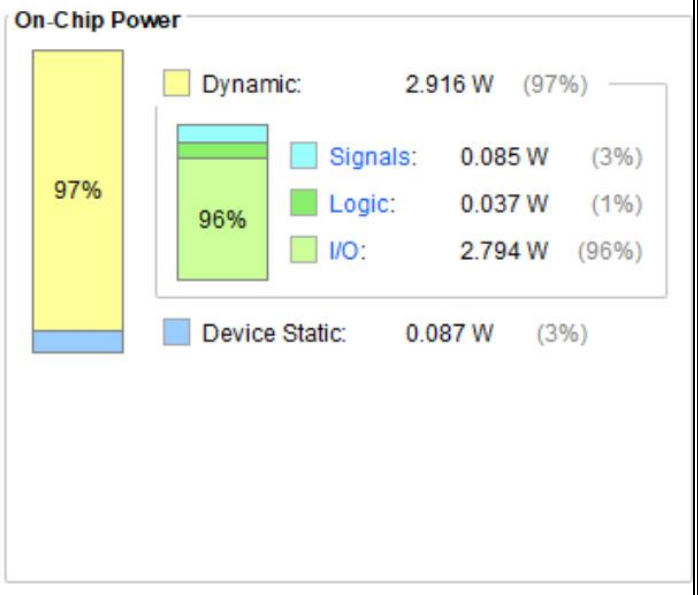
Power report:-

Summary

Power analysis from Implemented netlist. Activity derived from constraints files, simulation files or vectorless analysis.

Total On-Chip Power:	**3.003 W**
Design Power Budget:	**Not Specified**
Power Budget Margin:	**N/A**
Junction Temperature:	**30.7°C**
Thermal Margin:	54.3°C (28.7 W)
Effective ϑJA:	1.9°C/W
Power supplied to off-chip devices:	0 W
Confidence level:	Low

Launch Power Constraint Advisor to find and fix invalid switching activity



Q9 n bit comparator

Verilog code:-

```
module comparator(a,b,eq,lt,gt);
input [3:0] a,b;
output reg eq,lt,gt
always @(a,b)
begin
 if (a==b)
 begin
  eq = 1'b1;
  lt = 1'b0;
  gt = 1'b0;
 end
 else if (a>b)
 begin
  eq = 1'b0;
  lt = 1'b0;
  gt = 1'b1;
 end
 else
 begin
  eq = 1'b0;
```

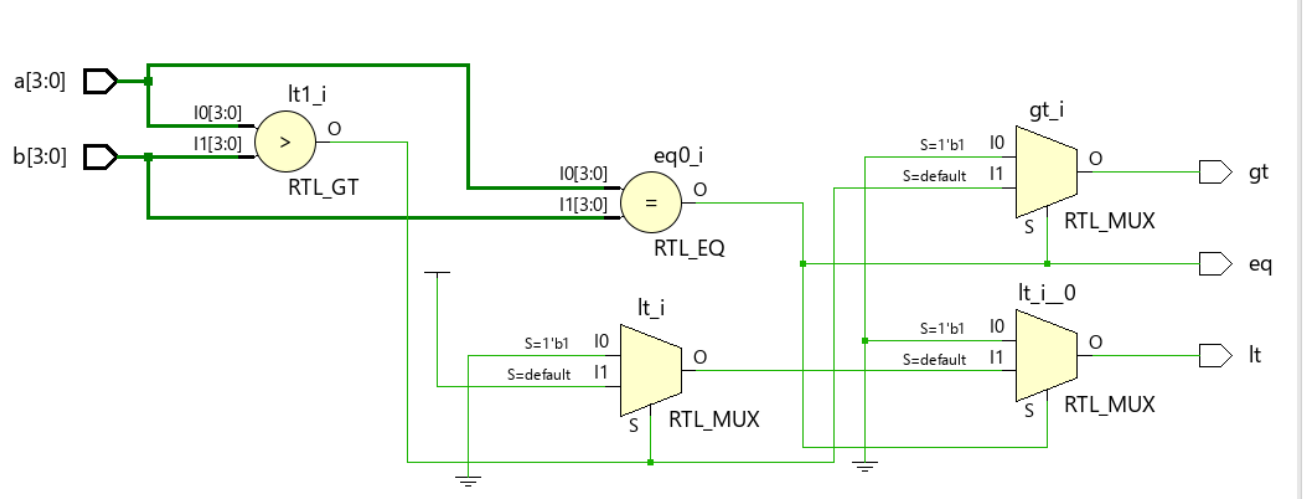
```
  lt = 1'b1;
  gt = 1'b0;
 end
end
endmodule
```

Testbench:-

```
module comparator(a,b,eq,lt,gt);
input [3:0] a,b;
output reg eq,lt,gt;
always @(a,b)
begin
 if (a==b)
 begin
  eq = 1'b1;
  lt = 1'b0;
  gt = 1'b0;
 end
 else if (a>b)
 begin
  eq = 1'b0;
  lt = 1'b0;
```

```
 gt = 1'b1;
end
else
begin
 eq = 1'b0;
 lt = 1'b1;
 gt = 1'b0;
end
end
endmodule
```

RTLsymetic:-



Synthesis report:-

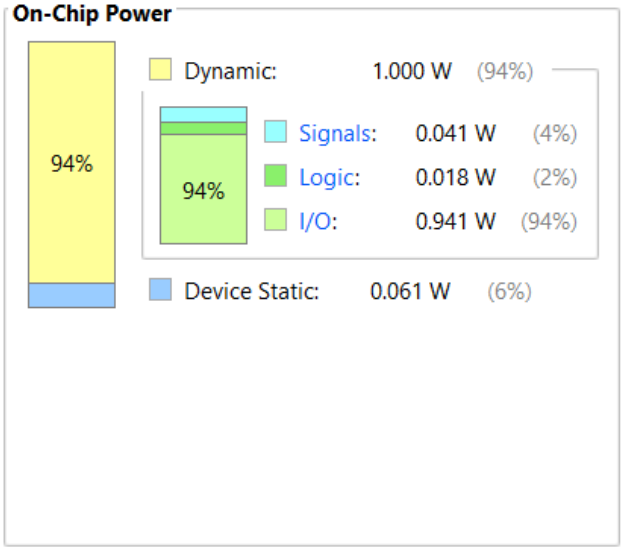
```
Start Writing Synthesis Report
--------------------------------------------------------------------------------

Report BlackBoxes:
+-+--------------+----------+
| |BlackBox name |Instances |
+-+--------------+----------+
+-+--------------+----------+

Report Cell Usage:
+------+-----+------+
|      |Cell |Count |
+------+-----+------+
|1     |LUT3 |     1|
|2     |LUT4 |     2|
|3     |LUT6 |     2|
|4     |IBUF |     8|
|5     |OBUF |     3|
+------+-----+------+
--------------------------------------------------------------------------------
Finished Writing Synthesis Report : Time (s): cpu = 00:00:31 ; elapsed = 00:00:37 . Memory  MB):
--------------------------------------------------------------------------------
```

Power report:-

Power analysis from Implemented netlist. Activity derived from constraints files, simulation files or vectorless analysis.

Total On-Chip Power:	**1.061 W**
Design Power Budget:	**Not Specified**
Power Budget Margin:	**N/A**
Junction Temperature:	**31.6°C**
Thermal Margin:	93.4°C (14.9 W)
Effective ϑJA:	6.2°C/W
Power supplied to off-chip devices:	0 W
Confidence level:	Low

Launch Power Constraint Advisor to find and fix invalid switching activity



Q10 serial register in serial register out

Verilog code:-

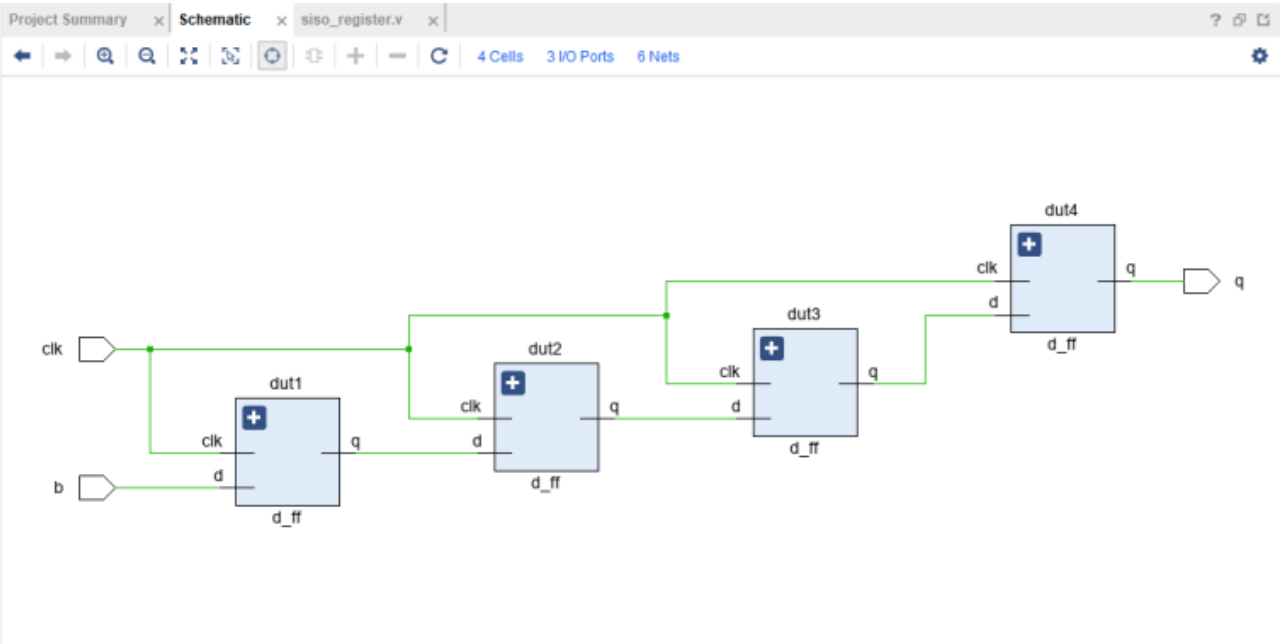
```
timescale 1ns / 1ps
module siso_design(input clk,b,output q);
wire w1,w2,w3;

d_ff dut1(.clk(clk),.d(b),.q(w1),.rst());
d_ff dut2(.clk(clk),.d(w1),.q(w2),.rst());
d_ff dut3(.clk(clk),.d(w2),.q(w3),.rst());
d_ff dut4(.clk(clk),.d(w3),.q(q),.rst());

endmodule

// d flip flop
module d_ff (
  input clk,
  input d,
  input rst,
  output reg q);

  always @(posedge clk)
  begin
    if (rst)
      q <= 1'b0;
    else
      q <= d;
  end

endmodule
```

testbench:

```
// testbench
```

```
module siso_tb();
reg clk,b;
wire q
siso_design uut(.clk(clk),.b(b),.q(q));
initial
begin
clk=1'b0;
forever #5clk=~clk;
end
initial
begin
$monitor("clk=%d,b=%d,q=%d",clk,b,q);
end
initial
begin
b=1;
#10;
b=1;
#10;
b=1;
#10;
b=0;
#50;
$finish;
End

Endmodule
```

RTLsymetic:-



Synthesis report:-

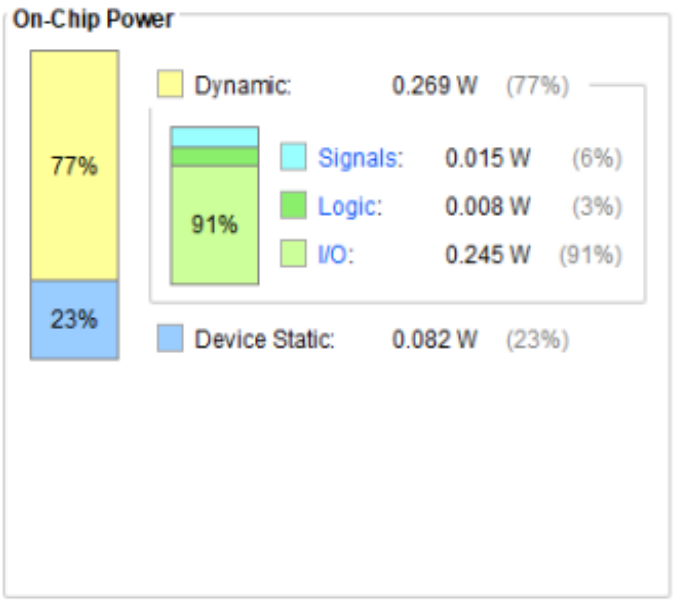
```
Start Writing Synthesis Report
------------------------------------------------------------------------------

Report BlackBoxes:
+-+--------------+----------+
| |BlackBox name |Instances |
+-+--------------+----------+
+-+--------------+----------+

Report Cell Usage:
+------+-------+------+
|      |Cell   |Count |
+------+-------+------+
|1     |BUFG   |     1|
|2     |SRL16E |     1|
|3     |FDRE   |     2|
|4     |IBUF   |     2|
|5     |OBUF   |     1|
+------+-------+------+

Report Instance Areas:
+------+---------+-------+------+
|      |Instance |Module |Cells |
+------+---------+-------+------+
|1     |top      |       |     7|
|2     |  dut1   |d_ff   |     1|
|3     |  dut3   |d_ff_0 |     1|
|4     |  dut4   |d_ff_1 |     1|
+------+---------+-------+------+
------------------------------------------------------------------------------
Finished Writing Synthesis Report : Time (s): cpu = 00:00:17 ; elapsed = 00:00:31 . Memory (MB): peak = 1018.820 ; gain = 0.000
```

Power report:-

Power analysis from Implemented netlist. Activity derived from constraints files, simulation files or vectorless analysis.

Total On-Chip Power:	**0.351 W**
Design Power Budget:	**Not Specified**
Power Budget Margin:	**N/A**
Junction Temperature:	**25.7°C**
Thermal Margin:	59.3°C (31.3 W)
Effective ϑJA:	1.9°C/W
Power supplied to off-chip devices:	0 W
Confidence level:	Low

Launch Power Constraint Advisor to find and fix invalid switching activity



Q11 Serial in parallel out shift register

Verilog code:-

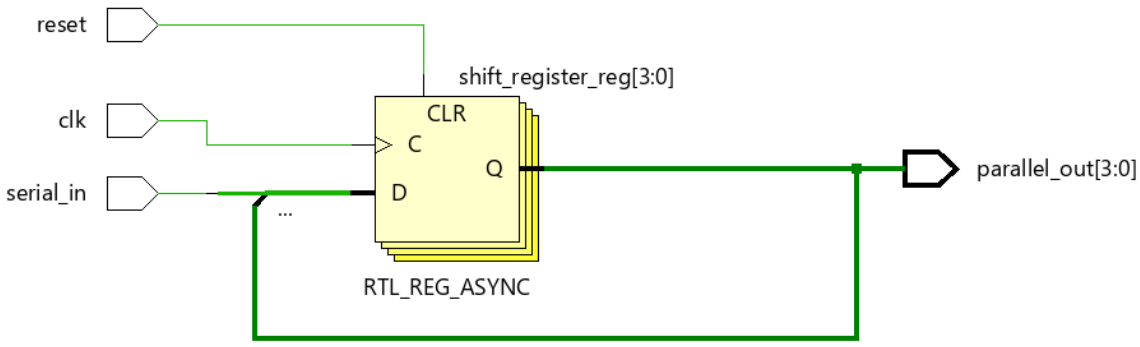
```
module sipo_shift_register #(parameter N=4) (
  input clk,
  input reset,
  input serial_in,
  output [N-1:0] parallel_out
);
  reg [N-1:0] shift_register;
  always @(posedge clk or posedge reset) begin
    if (reset)
      shift_register <= 0;
    else
      shift_register <= {shift_register[N-2:0], serial_in};
  end
  assign parallel_out = shift_register;
endmodule
```

Testbench:-

```
module testbench_sipo;
  parameter N = 4;
  parameter CLK_PERIOD = 10;
  reg clk;
  reg reset;
  reg serial_in;
  wire [N-1:0] parallel_out;
  sipo_shift_register #(N) uut (
    .clk(clk),
    .reset(reset),
    .serial_in(serial_in),
    .parallel_out(parallel_out)
  );
  always begin
    #CLK_PERIOD / 2 clk = ~clk;
  end
  initial begin
    $display("SIPO Shift Register Testbench");



    clk = 0;
```

```
    reset = 1;
    serial_in = 0;
    #CLK_PERIOD reset = 0;
    serial_in = 1;
    #CLK_PERIOD serial_in = 0;
    #CLK_PERIOD serial_in = 1;
    #CLK_PERIOD serial_in = 0;
    reset = 1;
    #CLK_PERIOD reset = 0;
    $display("Parallel Out: %b", parallel_out);
    $finish;
  end
endmodule
```

RTLsynthesis :-



Synthesis report:-

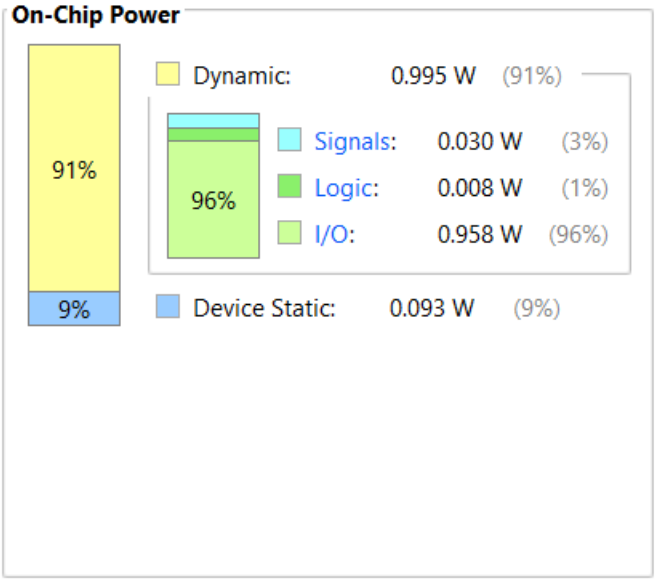
```
Start Writing Synthesis Report
--------------------------------------------------------------------------------

Report BlackBoxes:
+-+--------------+----------+
| |BlackBox name |Instances |
+-+--------------+----------+
+-+--------------+----------+

Report Cell Usage:
+------+-----+------+
|      |Cell |Count |
+------+-----+------+
|1     |BUFG |     1|
|2     |FDCE |     4|
|3     |IBUF |     3|
|4     |OBUF |     4|
+------+-----+------+
--------------------------------------------------------------------------------
Finished Writing Synthesis Report : Time (s): cpu = 00:00:32 ; elapsed = 00:00:36 . Memory  MB):
```

Power report:-

Power analysis from Implemented netlist. Activity derived from constraints files, simulation files or vectorless analysis.

Total On-Chip Power:	**1.088 W**
Design Power Budget:	**Not Specified**
Power Budget Margin:	**N/A**
Junction Temperature:	**27.8°C**
Thermal Margin:	72.2°C (27.4 W)
Effective ϑJA:	2.6°C/W
Power supplied to off-chip devices:	0 W
Confidence level:	Low

Launch Power Constraint Advisor to find and fix invalid switching activity



Q12 parallel in parallel out register

Verilog code:-

```
module pipo_shift_register #(parameter N=4) (
  input clk,
  input reset,
  input [N-1:0] parallel_in,
  output [N-1:0] parallel_out
);
  reg [N-1:0] shift_register;
  always @(posedge clk or posedge reset) begin
    if (reset)
      shift_register <= 0;
    else
      shift_register <= parallel_in;
  end
  assign parallel_out = shift_register;
endmodule
```

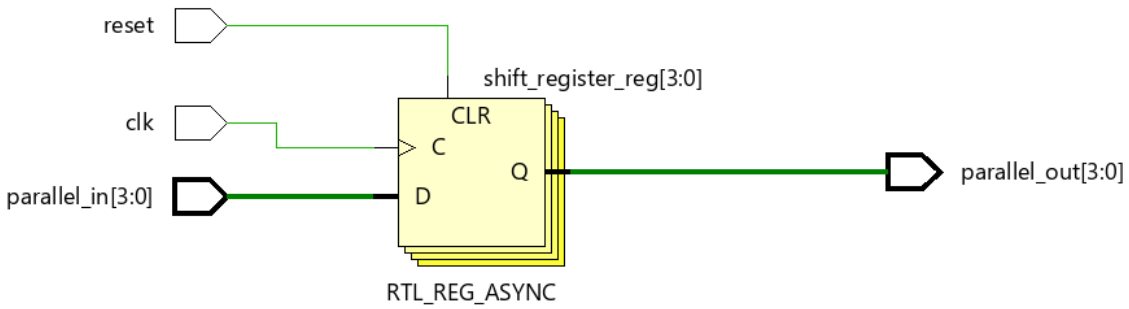
Test bench:-

```
module testbench_pipo;
  parameter N = 4;
  parameter CLK_PERIOD = 10; // Clock period in time units
  reg clk;
```

```
reg reset;
wire [N-1:0] parallel_in;
wire [N-1:0] parallel_out;
pipo_shift_register #(N) uut (
  .clk(clk),
  .reset(reset),
  .parallel_in(parallel_in),
  .parallel_out(parallel_out)
);
always begin
  #CLK_PERIOD / 2 clk = ~clk;
end
initial begin
  $display("PIPO Shift Register Testbench");
  clk = 0;
  reset = 1;
  parallel_in = 4'b0000;
  #CLK_PERIOD reset = 0;
  parallel_in = 4'b1010;
  #CLK_PERIOD parallel_in = 4'b0101;



  reset = 1;
```

```
    #CLK_PERIOD reset = 0;
    $display("Parallel Out: %b", parallel_out);
    $finish;
  end
endmodule
```

RTLsynthesis:-



Synthesis report:-

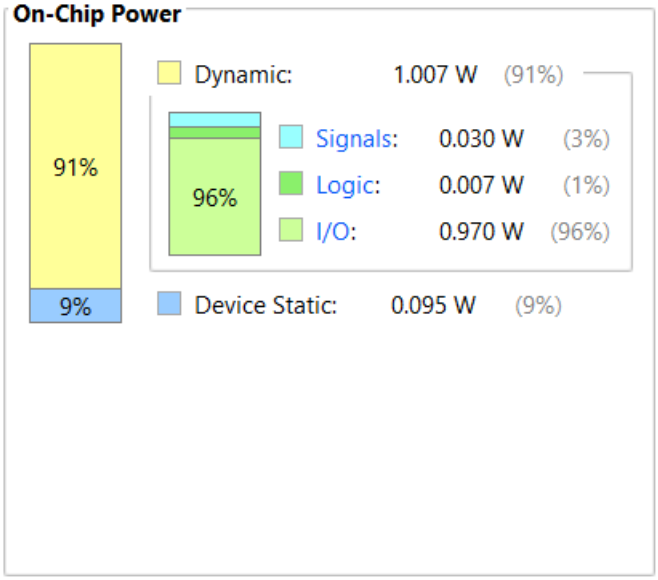
```
Start Writing Synthesis Report
--------------------------------------------------------------------------------

Report BlackBoxes:
+-+--------------+----------+
| |BlackBox name |Instances |
+-+--------------+----------+
+-+--------------+----------+

Report Cell Usage:
+------+-----+------+
|      |Cell |Count |
+------+-----+------+
|1     |BUFG |     1|
|2     |FDCE |     4|
|3     |IBUF |     6|
|4     |OBUF |     4|
+------+-----+------+
--------------------------------------------------------------------------------
Finished Writing Synthesis Report : Time (s): cpu = 00:00:32 ; elapsed = 00:00:35 . Memory (MB): peak = 1043.453 ; gain = 28.633
```

Power report:-

Power analysis from Implemented netlist. Activity derived from constraints files, simulation files or vectorless analysis.

Total On-Chip Power:	**1.102 W**
Design Power Budget:	**Not Specified**
Power Budget Margin:	**N/A**
Junction Temperature:	**30.1°C**
Thermal Margin:	54.9°C (11.8 W)
Effective ϑJA:	4.6°C/W
Power supplied to off-chip devices:	0 W
Confidence level:	Low

Launch Power Constraint Advisor to find and fix invalid switching activity



Q13 parallel in serial out register

Verilog code:-

```
module piso_shift_register #(parameter N=4) (
  input clk,
  input reset,
  input [N-1:0] parallel_in,
  output serial_out
);
  reg [N-1:0] shift_register;
  reg [N-1:0] temp;
  always @(posedge clk or posedge reset) begin
    if (reset)
      shift_register <= 0;
    else
      shift_register <= parallel_in;
  end
  always @(posedge clk or posedge reset) begin
    if (reset)
      temp <= 0;
    else
      temp <= {shift_register[N-2:0], temp[N-1]};
  end
```

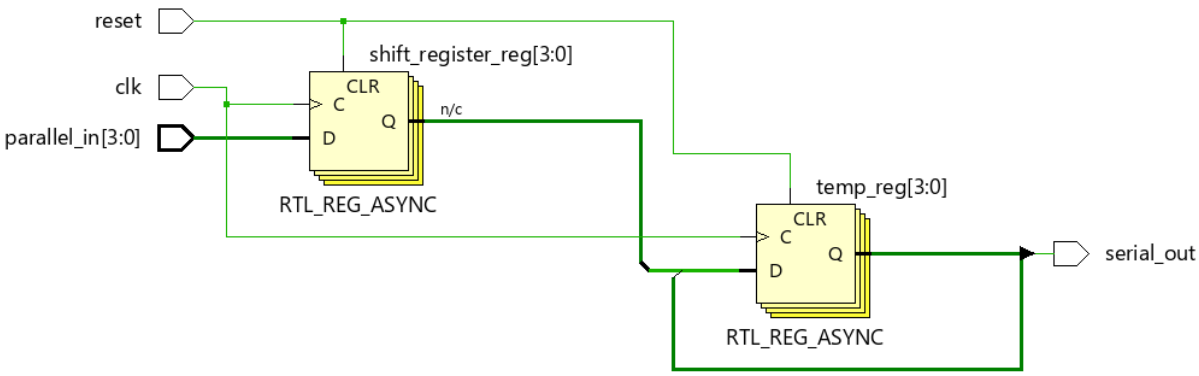
```
  assign serial_out = temp[0];
endmodule
```

Test beanch:-

```
module testbench_piso;
  parameter N = 4;
  parameter CLK_PERIOD = 10;
  reg clk;
  reg reset;
  wire [N-1:0] parallel_in;
  wire serial_out;
  piso_shift_register #(N) uut (
    .clk(clk),
    .reset(reset),
    .parallel_in(parallel_in),
    .serial_out(serial_out)
  );
  always begin
    #CLK_PERIOD / 2 clk = ~clk;
  end
  initial begin
    $display("PISO Shift Register Testbench");
```

```
    clk = 0;
    reset = 1;
    parallel_in = 4'b0000;
    #CLK_PERIOD reset = 0;
    parallel_in = 4'b1010;
    #CLK_PERIOD parallel_in = 4'b0101;
    reset = 1;
    #CLK_PERIOD reset = 0
    $display("Serial Out: %b", serial_out);
    $finish;
  end
endmodule
```

RTLsynthesis:-



Synthesis report:-

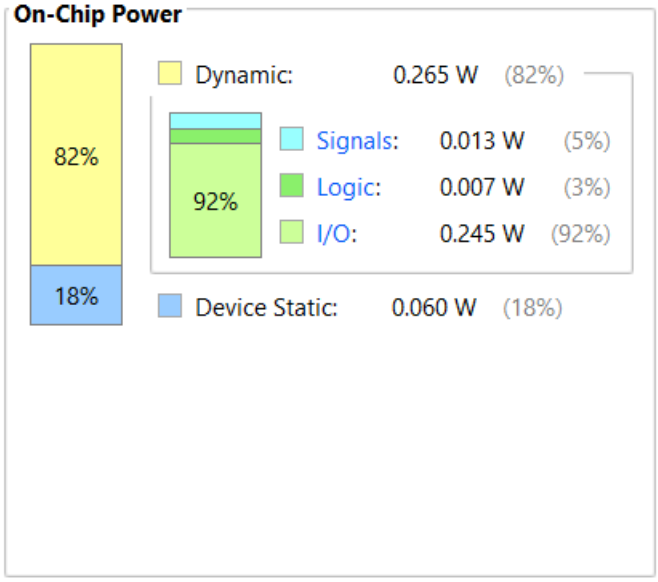
```
Start Writing Synthesis Report
--------------------------------------------------------------------------------

Report BlackBoxes:
+-+--------------+----------+
| |BlackBox name |Instances |
+-+--------------+----------+
+-+--------------+----------+

Report Cell Usage:
+------+-----+------+
|      |Cell |Count |
+------+-----+------+
|1     |BUFG |     1|
|2     |FDCE |     3|
|3     |IBUF |     3|
|4     |OBUF |     1|
+------+-----+------+
--------------------------------------------------------------------------------
Finished Writing Synthesis Report : Time (s): cpu = 00:00:21 ; elapsed = 00:00:24 . Memory (MB): peak = 1015.234 ; gain = 0.000
```

Power report:-

Power analysis from Implemented netlist. Activity derived from constraints files, simulation files or vectorless analysis.

Total On-Chip Power:	**0.325 W**
Design Power Budget:	**Not Specified**
Power Budget Margin:	**N/A**
Junction Temperature:	**26.7°C**
Thermal Margin:	73.3°C (13.9 W)
Effective ϑJA:	5.3°C/W
Power supplied to off-chip devices:	0 W
Confidence level:	Low

Launch Power Constraint Advisor to find and fix invalid switching activity



Q14 Bidirectional Shift register:-

Verilog code:-

module bidirectional_shift_register #(parameter N=8) (

```
  input clk,
  input reset,
  input shift_left,
  input shift_right,
  input [N-1:0] parallel_in,
  output [N-1:0] parallel_out
);
  reg [N-1:0] shift_register;
  reg [N-1:0] temp;
  always @(posedge clk or posedge reset) begin
    if (reset)
      shift_register <= 0;
    else if (shift_left)
      shift_register <= {shift_register[N-2:0], 1'b0};
    else if (shift_right)
      shift_register <= {1'b0, shift_register[N-1:1]};
    else
      shift_register <= parallel_in;
  end
  assign parallel_out = shift_register;
endmodule
```

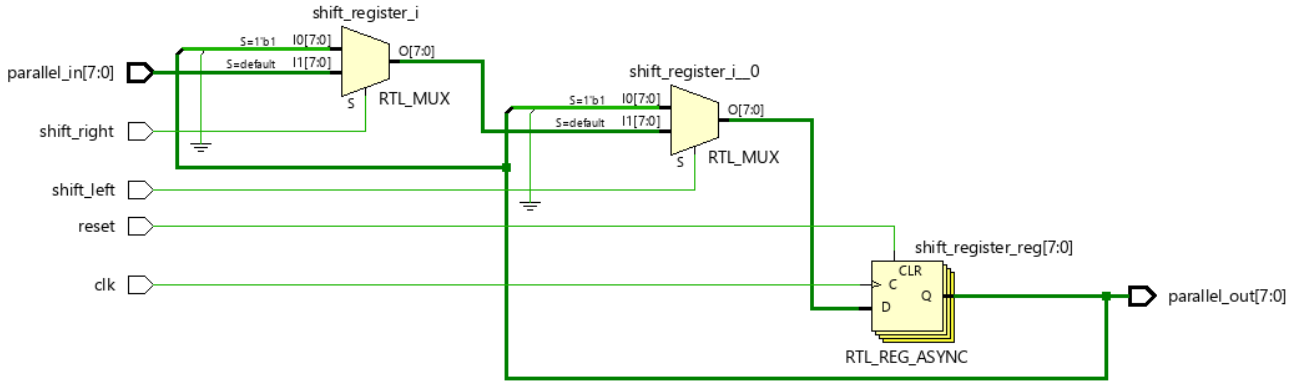
test beanch:-

```
module testbench_bidirectional_shift_register;
```

```
parameter N = 8;
parameter CLK_PERIOD = 10;
reg clk;
reg reset;
reg shift_left;
reg shift_right;
wire [N-1:0] parallel_in;
wire [N-1:0] parallel_out;
bidirectional_shift_register #(N) uut (
  .clk(clk),
  .reset(reset),
  .shift_left(shift_left),
  .shift_right(shift_right),
  .parallel_in(parallel_in),
  .parallel_out(parallel_out)
);


always begin
  #CLK_PERIOD / 2 clk = ~clk;
end
initial begin
  $display("Bidirectional Shift Register Testbench");
```

```
    clk = 0;
    reset = 1;
    shift_left = 0;
    shift_right = 0;
    parallel_in = 8'b00000000;
    #CLK_PERIOD reset = 0;
    parallel_in = 8'b10101010;
    shift_left = 1;
    #CLK_PERIOD shift_left = 0;
    shift_right = 1;
    #CLK_PERIOD shift_right = 0;

    shift_right = 1;
    #CLK_PERIOD shift_right = 0;
 parallel_in = 8'b11001100;
    shift_left = 1;
    #CLK_PERIOD shift_left = 0;
    $display("Parallel Out: %b", parallel_out);
    $finish;
  end
```

RTLsynthesis :-



Synthesis report:-

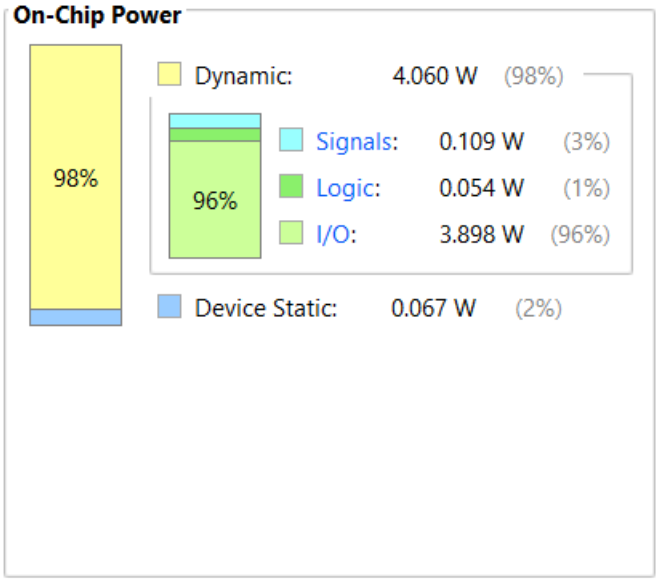
```
--------------------------------------------------------------------------------
Start Writing Synthesis Report
--------------------------------------------------------------------------------

Report BlackBoxes:
+-+--------------+----------+
| |BlackBox name |Instances |
+-+--------------+----------+
+-+--------------+----------+

Report Cell Usage:
+------+-----+------+
|      |Cell |Count |
+------+-----+------+
|1     |BUFG |     1|
|2     |LUT4 |     2|
|3     |LUT5 |     6|
|4     |FDCE |     8|
|5     |IBUF |    12|
|6     |OBUF |     8|
+------+-----+------+
--------------------------------------------------------------------------------
Finished Writing Synthesis Report : Time (s): cpu = 00:00:20 ; elapsed = 00:00:23 . Memory (MB): peak = 1030.133 ; gain = 12.38
--------------------------------------------------------------------------------
```

Power report:-

Power analysis from Implemented netlist. Activity derived from constraints files, simulation files or vectorless analysis.

Total On-Chip Power:	**4.127 W**
Design Power Budget:	**Not Specified**
Power Budget Margin:	**N/A**
Junction Temperature:	**46.7°C**
Thermal Margin:	53.3°C (10.1 W)
Effective ϑJA:	5.3°C/W
Power supplied to off-chip devices:	0 W
Confidence level:	Low

Launch Power Constraint Advisor to find and fix invalid switching activity



Q15 PRBS sequence generator

Verilog code:-

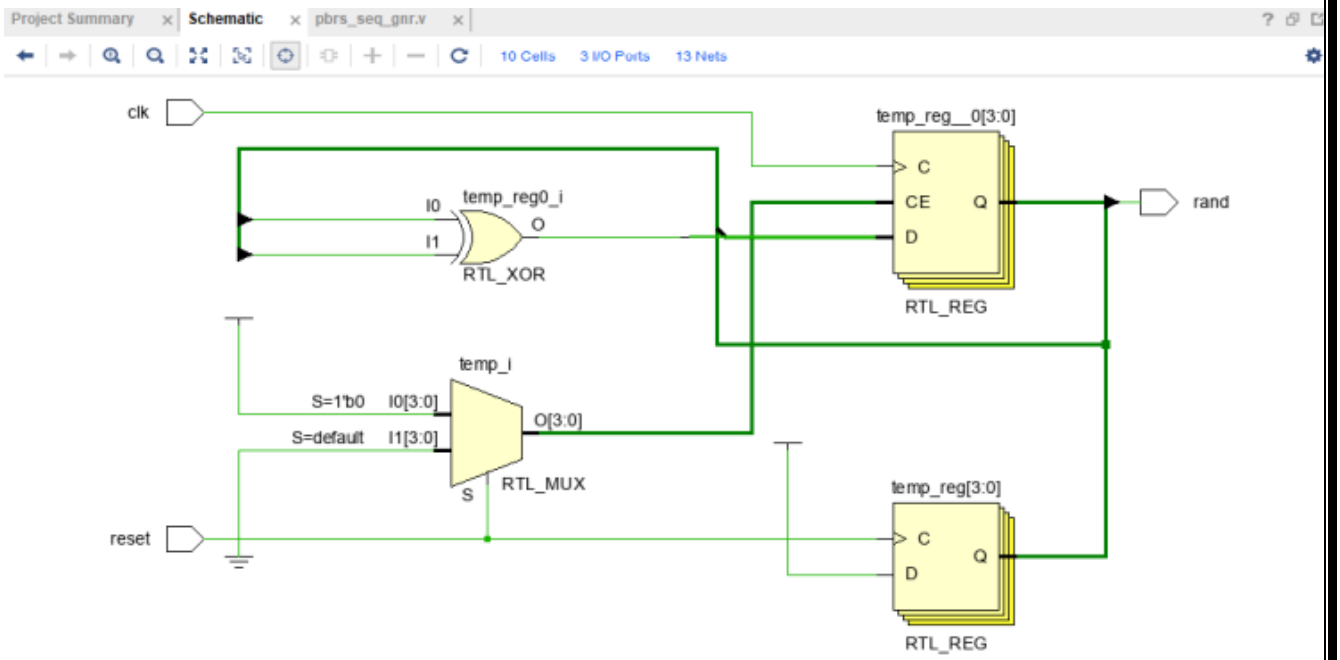
```
module prbs_generator (
  input clk,
  input reset,
  output reg [3:0] prbs_out
);

  reg [3:0] shift_register;

  always @(posedge clk or posedge reset) begin
    if (reset)
      shift_register <= 4'b0001; // Initial seed value (non-zero)
    else
      shift_register <= {shift_register[2:0], shift_register[3] ^
shift_register[0]};
  end

  assign prbs_out = shift_register;

endmodule
```

Testbench:-

```
module testbench_prbs_generator;

  // Parameters
  parameter CLK_PERIOD = 10; // Clock period in time units

  // Signals
  reg clk;
  reg reset;
  wire [3:0] prbs_out;

  // Instantiate the PRBS generator
  prbs_generator uut (
    .clk(clk),
    .reset(reset),
    .prbs_out(prbs_out)
  );

  // Clock generation
  always begin
    #CLK_PERIOD / 2 clk = ~clk;
```

```
  end
  // Testbench
  initial begin
    $display("PRBS Generator Testbench");
    // Initialize
    clk = 0;
    reset = 1;
    #CLK_PERIOD reset = 0;

    // Generate and display PRBS sequence for 16 clock cycles
    $display("PRBS Output:");
    for (int i = 0; i < 16; i = i + 1) begin
      #CLK_PERIOD;
      $display("%b", prbs_out);
    end

    $finish;
  end

endmodule
```

RTL synthesis:-



Synthesis report:-

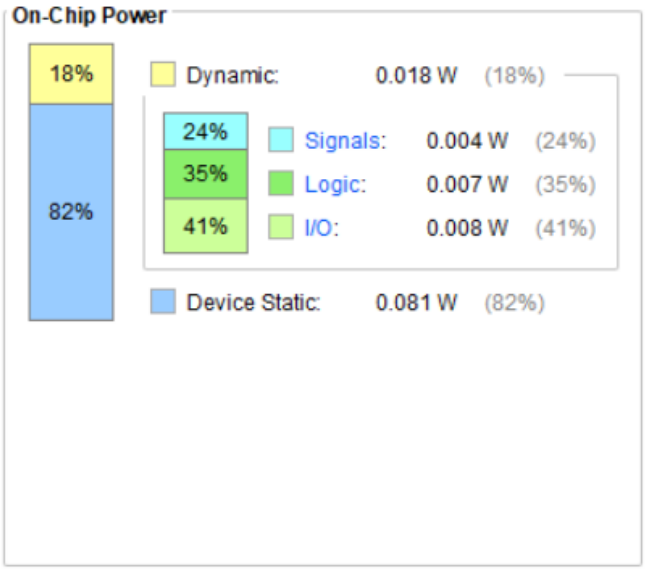
```
---------------------------------------------------------------------------------
Start Writing Synthesis Report
---------------------------------------------------------------------------------

Report BlackBoxes:
+-+--------------+----------+
| |BlackBox name |Instances |
+-+--------------+----------+
+-+--------------+----------+

Report Cell Usage:
+------+-----+------+
|      |Cell |Count |
+------+-----+------+
|1     |BUFG |     2|
|2     |LUT1 |     2|
|3     |LUT2 |     1|
|4     |FDRE |     8|
|5     |IBUF |     2|
|6     |OBUF |     1|
+------+-----+------+

Report Instance Areas:
+------+---------+-------+------+
|      |Instance |Module |Cells |
+------+---------+-------+------+
|1     |top      |       |    16|
+------+---------+-------+------+
---------------------------------------------------------------------------------
Finished Writing Synthesis Report : Time (s): cpu = 00:00:09 ; elapsed = 00:00:16 . Memory (MB): peak = 1018.242 ; gai  = 0.0
---------------------------------------------------------------------------------
```

Power report:-

Power estimation from Synthesized netlist. Activity derived from constraints files, simulation files or vectorless analysis. Note: these early estimates can change after implementation.

Total On-Chip Power:	**0.1 W**
Design Power Budget:	**Not Specified**
Power Budget Margin:	**N/A**
Junction Temperature:	**25.2°C**
Thermal Margin:	59.8°C (31.6 W)
Effective ϑJA:	1.9°C/W
Power supplied to off-chip devices:	0 W
Confidence level:	Low

Launch Power Constraint Advisor to find and fix invalid switching activity



Q16. 8-bit subtractor

Verilog code:-

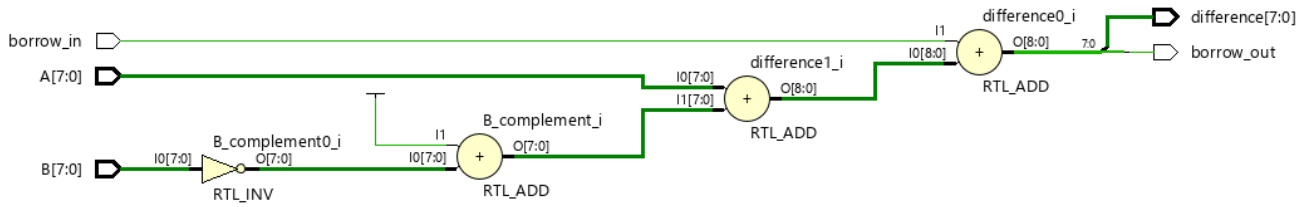
```
module eight_bit_subtractor (
  input [7:0] A,
  input [7:0] B,
  input borrow_in,
  output [7:0] difference,
  output borrow_out
);
  wire [7:0] B_complement;
  assign B_complement = (~B) + 1;
  assign {borrow_out, difference} = A + B_complement + borrow_in;
endmodule
```

Testbench:-

```
module testbench_eight_bit_subtractor;
  reg [7:0] A;
  reg [7:0] B;
  reg borrow_in;
  wire [7:0] difference;
  wire borrow_out;
  eight_bit_subtractor uut (
    .A(A),
```

```
    .B(B),
    .borrow_in(borrow_in),
    .difference(difference),
    .borrow_out(borrow_out)
  );
  initial begin
    $display("8-Bit Subtractor Testbench");
    A = 8'b00001010;
    B = 8'b00000101;
    borrow_in = 1'b0;
    #10 $display("A = %b, B = %b, Borrow In = %b,
Difference = %b, Borrow Out = %b", A, B, borrow_in,
difference, borrow_out);
    A = 8'b00000101;
    B = 8'b00001010;
    borrow_in = 1'b1;
    #10 $display("A = %b, B = %b, Borrow In = %b,
Difference = %b, Borrow Out = %b", A, B, borrow_in,
difference, borrow_out);
    $finish;
  end
endmodule
```

RTL synthesis:-



Synthesis report:-

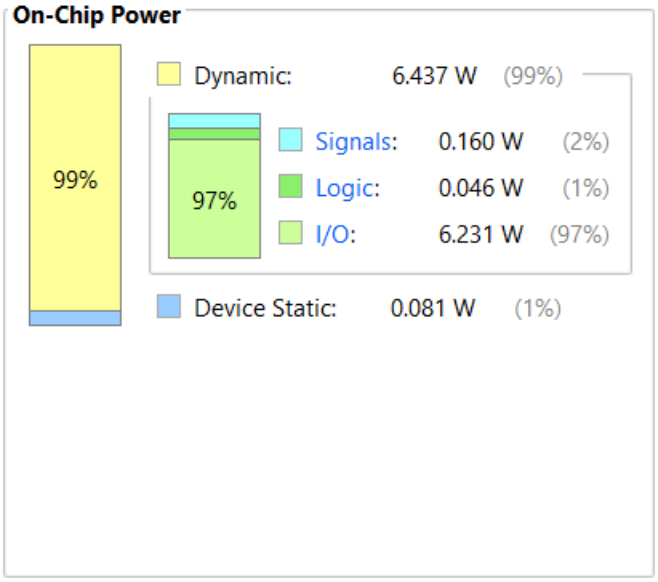
```
Start Writing Synthesis Report
--------------------------------------------------------------------------------

Report BlackBoxes:
+-+--------------+----------+
| |BlackBox name |Instances |
+-+--------------+----------+
+-+--------------+----------+

Report Cell Usage:
+------+-------+------+
|      |Cell   |Count |
+------+-------+------+
|1     |CARRY4 |     3|
|2     |LUT2   |     1|
|3     |LUT3   |     3|
|4     |LUT4   |     2|
|5     |LUT5   |     2|
|6     |LUT6   |     2|
|7     |IBUF   |    17|
|8     |OBUF   |     9|
+------+-------+------+
--------------------------------------------------------------------------------
Finished Writing Synthesis Report : Time (s): cpu = 00:00:20 ; elapsed = 00:00:23 . Memory (MB): peak = 1026.605 ; gain = 8.137
```

Power report:-

Power analysis from Implemented netlist. Activity derived from constraints files, simulation files or vectorless analysis.

Total On-Chip Power:	**6.518 W**
Design Power Budget:	**Not Specified**
Power Budget Margin:	**N/A**
Junction Temperature:	**65.3°C**
Thermal Margin:	34.7°C (5.6 W)
Effective ϑJA:	6.2°C/W
Power supplied to off-chip devices:	0 W
Confidence level:	Low

Launch Power Constraint Advisor to find and fix invalid switching activity



Q17 8-bit adder and subtractor

Verilog code:-

```
module addsub(A, B, OPER, RES);
input  OPER;
input  [7:0] A;
input  [7:0] B;
output [7:0] RES;
reg    [7:0] RES;
  always @(A or B or OPER)
  begin
    if (OPER==1'b0) RES = A + B;
    else            RES = A - B;
  end
endmodule
```

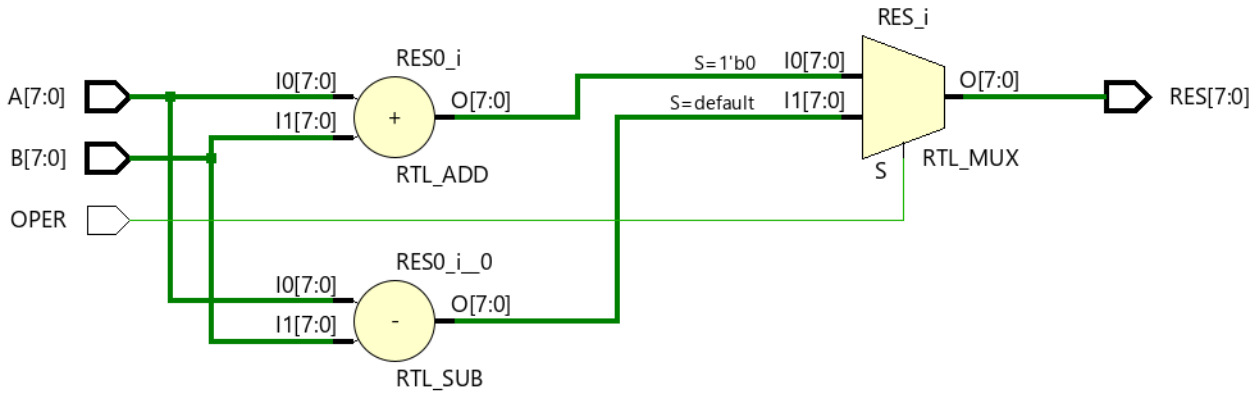
Testbench:-

```
module testbench_eight_bit_adder_subtractor;
  // Signals
  reg [7:0] A;
  reg [7:0] B;
  reg subtract;
  wire [7:0] result;
  wire overflow;
```

```
  // Instantiate the adder/subtractor
  eight_bit_adder_subtractor uut (
    .A(A),
    .B(B),
    .subtract(subtract),
    .result(result),
    .overflow(overflow)
  );
  // Testbench
  initial begin
    $display("8-Bit Adder/Subtractor Testbench");

    // Test 1: A = 10, B = 5, subtract = 0
    A = 8'b00001010;
    B = 8'b00000101;
    subtract = 1'b0;
    #10 $display("A = %b, B = %b, Subtract = %b, Result =
%b, Overflow = %b", A, B, subtract, result, overflow);

    // Test 2: A = 5, B = 10, subtract = 1
    A = 8'b00000101;
    B = 8'b00001010;
    subtract = 1'b1;
```

```
    #10 $display("A = %b, B = %b, Subtract = %b, Result =
%b, Overflow = %b", A, B, subtract, result, overflow);
    $finish;
  end
endmodule
```

RTL synthesis:-



Synthesis report:-

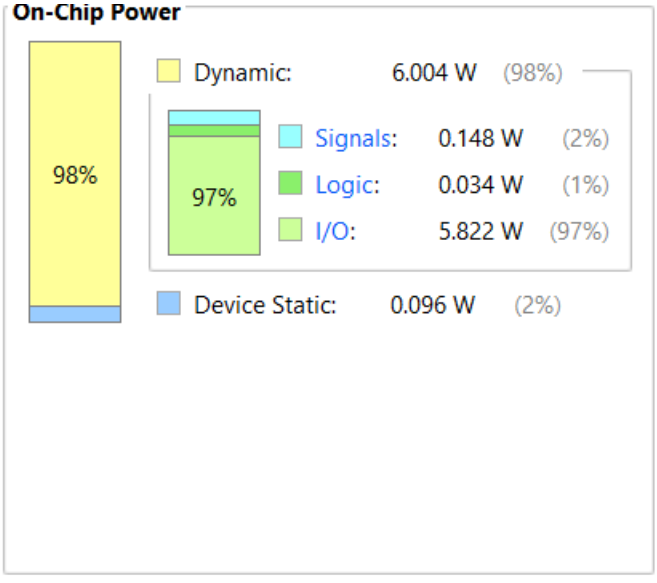
```
---------------------------------------------------------------------------------
Start Writing Synthesis Report
---------------------------------------------------------------------------------

Report BlackBoxes:
+-+--------------+----------+
| |BlackBox name |Instances |
+-+--------------+----------+
+-+--------------+----------+

Report Cell Usage:
+------+-------+------+
|      |Cell   |Count |
+------+-------+------+
|1     |CARRY4 |     2|
|2     |LUT1   |     1|
|3     |LUT3   |     7|
|4     |IBUF   |    17|
|5     |OBUF   |     8|
+------+-------+------+
---------------------------------------------------------------------------------
Finished Writing Synthesis Report : Time (s): cpu = 00:00:21 ; elapsed = 00:00:23 . Memory (MB): peak = 1045.613 ; gain = 29.246
---------------------------------------------------------------------------------
```

Power report:-

Power analysis from Implemented netlist. Activity derived from constraints files, simulation files or vectorless analysis.

Total On-Chip Power:	**6.099 W**
Design Power Budget:	**Not Specified**
Power Budget Margin:	**N/A**
Junction Temperature:	**55.5°C**
Thermal Margin:	29.5°C (5.9 W)
Effective ϑJA:	5.0°C/W
Power supplied to off-chip devices:	0 W
Confidence level:	Low

Launch Power Constraint Advisor to find and fix invalid switching activity



Q18 4 bit multiplexer

Verilog code:-

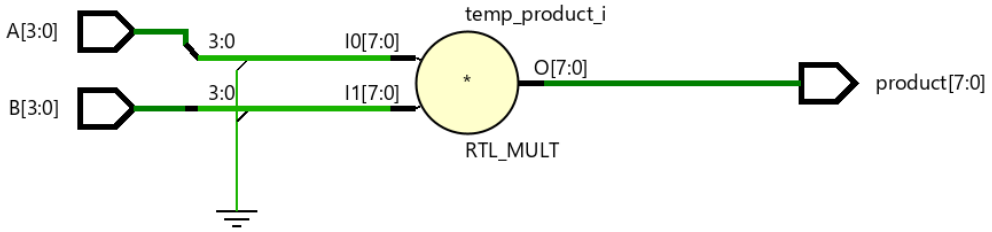
```
module four_bit_multiplier (
  input [3:0] A,
  input [3:0] B,
  output [7:0] product
);
  wire [7:0] temp_product;
  assign temp_product = {4'b0, A} * {4'b0, B};
  assign product = temp_product[7:0];
endmodule
```

Testbench:-

```
module testbench_four_bit_multiplier;
  reg [3:0] A;
  reg [3:0] B;
  wire [7:0] product;
  four_bit_multiplier uut (
    .A(A),
    .B(B),
    .product(product)
  );
```

```
  initial begin
    $display("4-Bit Multiplier Testbench");
    A = 4'b0111;
    B = 4'b0101;
    #10 $display("A = %b, B = %b, Product = %b", A, B,
product);
    A = 4'b0011;
    B = 4'b1000;
    #10 $display("A = %b, B = %b, Product = %b", A, B,
product);
    $finish;
  end
endmodule
```

RTLsynthesis:-



Synthesis report:-

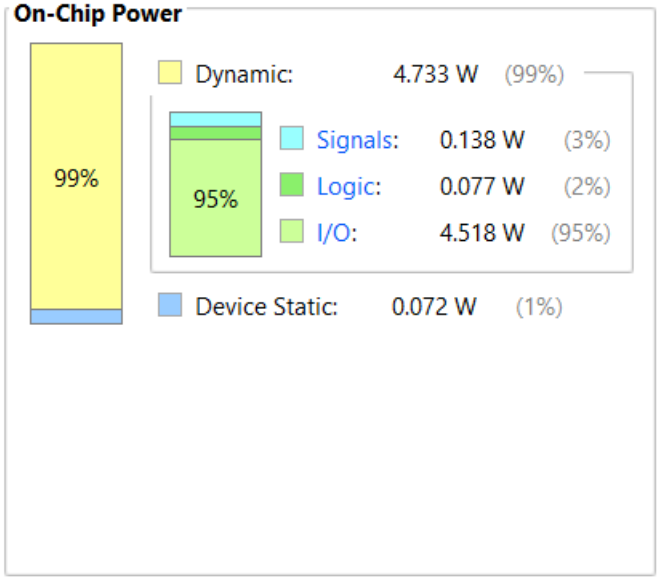
```
Start Writing Synthesis Report
------------------------------------------------------------------------------

Report BlackBoxes:
+-+--------------+----------+
| |BlackBox name |Instances |
+-+--------------+----------+
+-+--------------+----------+

Report Cell Usage:
+------+-------+------+
|      |Cell   |Count |
+------+-------+------+
|1     |CARRY4 |     2|
|2     |LUT2   |     3|
|3     |LUT3   |     1|
|4     |LUT4   |     4|
|5     |LUT5   |     1|
|6     |LUT6   |    10|
|7     |IBUF   |     8|
|8     |OBUF   |     8|
+------+-------+------+
------------------------------------------------------------------------------
Finished Writing Synthesis Report : Time (s): cpu = 00:00:19 ; elapsed = 00:00:24 . Memory (MB): peak = 1034.156 ; gain = 15.0 5
```

Power report:-

Power analysis from Implemented netlist. Activity derived from constraints files, simulation files or vectorless analysis.

Total On-Chip Power:	**4.804 W**
Design Power Budget:	**Not Specified**
Power Budget Margin:	**N/A**
Junction Temperature:	**54.7°C**
Thermal Margin:	70.3°C (11.2 W)
Effective ϑJA:	6.2°C/W
Power supplied to off-chip devices:	0 W
Confidence level:	Low

Launch Power Constraint Advisor to find and fix invalid switching activity



Q19 Fixed point division

Verilog code:-

```
module fixed_point_division (
  input [15:0] dividend, // 16-bit input with 8 fractional bits
  input [7:0] divisor,   // 8-bit input with 8 fractional bits
  output [15:0] quotient  // 16-bit output with 8 fractional bits
);

  reg [15:0] remainder;
  reg [15:0] temp_quotient;
  reg [7:0] count;

  always @(posedge clk or posedge reset) begin
    if (reset) begin
      count <= 0;
      remainder <= 0;
      temp_quotient <= 0;
    end
    else begin
      if (remainder >= divisor) begin
        remainder <= remainder - divisor;
        temp_quotient <= temp_quotient + 1;
      end
      else begin
        remainder <= remainder;
```

```
      temp_quotient <= temp_quotient;
    end

    count <= count + 1;
    if (count == 7) begin
      quotient <= temp_quotient;
      count <= 0;
    end
  end
 end

endmodule
```

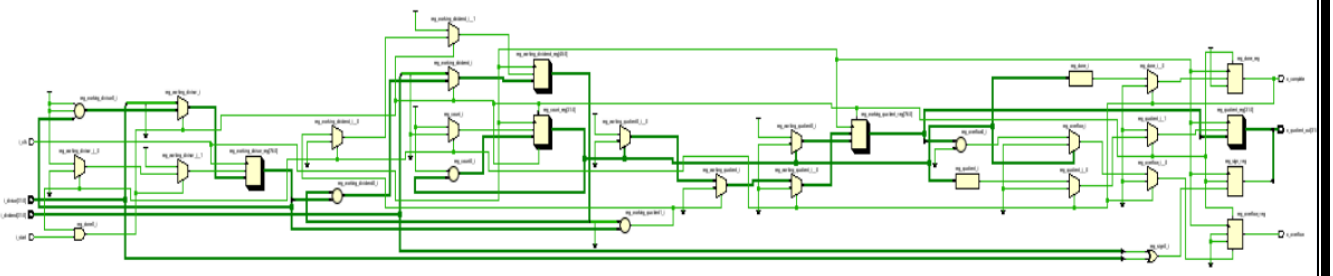
test beanch

```
module testbench_fixed_point_division;

  // Signals
  reg clk;
  reg reset;
  reg [15:0] dividend;
  reg [7:0] divisor;
  wire [15:0] quotient;
```

```
// Instantiate the fixed-point division module
fixed_point_division uut (
  .dividend(dividend),
  .divisor(divisor),
  .quotient(quotient)
);

// Clock generation
always begin
  #10 clk = ~clk;
end

// Testbench
initial begin
  $display("Fixed-Point Division Testbench");

  // Initialize
  clk = 0;
  reset = 0;
  dividend = 16'b01011000010000000; // Represents 13.25
  divisor = 8'b00000100;          // Represents 0.25
```

```
    // Apply reset
    reset = 1;
    #20 reset = 0;

    // Provide inputs
    dividend = 16'b01011000010000000; // Represents 13.25
    divisor = 8'b00000100;          // Represents 0.25
    #20;

    // Display results
    $display("Dividend: %d, Divisor: %d", dividend, divisor);
    $display("Quotient: %d.%02d", quotient[15:8],
quotient[7:0]);

    $finish;
  end

endmodule
```

RTL symetic:-



Synthesis report:-

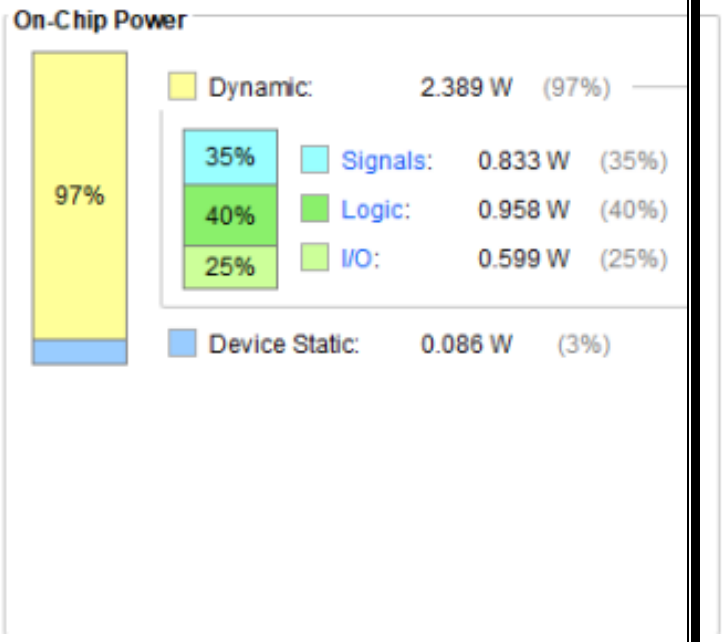
```
Start Writing Synthesis Report
--------------------------------------------------------------------------------

Report BlackBoxes:
+-+--------------+----------+
| |BlackBox name |Instances |
+-+--------------+----------+
+-+--------------+----------+

Report Cell Usage:
+------+-------+------+
|      |Cell   |Count |
+------+-------+------+
|1     |BUFG   |     1|
|2     |CARRY4 |    30|
|3     |LUT1   |    34|
|4     |LUT2   |    20|
|5     |LUT3   |   121|
|6     |LUT4   |   102|
|7     |LUT5   |    39|
|8     |LUT6   |    27|
|9     |FDRE   |   261|
|10    |FDSE   |     4|
|11    |IBUF   |    66|
|12    |OBUF   |    34|
+------+-------+------+

Report Instance Areas:
+------+---------+-------+------+
|      |Instance |Module |Cells |
+------+---------+-------+------+
|1     |top      |       |   739|
+------+---------+-------+------+
--------------------------------------------------------------------------------
Finished Writing Synthesis Report : Time (s): cpu = 00:00:17 ; elapsed = 00:00:30 . Memory (MB): peak = 1019.531 ; gain = 0.000
```

Powerreport:-

Power estimation from Synthesized netlist. Activity derived from constraints files, simulation files or vectorless analysis. Note: these early estimates can change after implementation.

Total On-Chip Power:	**2.475 W**
Design Power Budget:	**Not Specified**
Power Budget Margin:	**N/A**
Junction Temperature:	**29.7°C**
Thermal Margin:	55.3°C (29.2 W)
Effective ϑJA:	1.9°C/W
Power supplied to off-chip devices:	0 W
Confidence level:	Low

Launch Power Constraint Advisor to find and fix invalid switching activity



Q20 Master slave jk flip flop

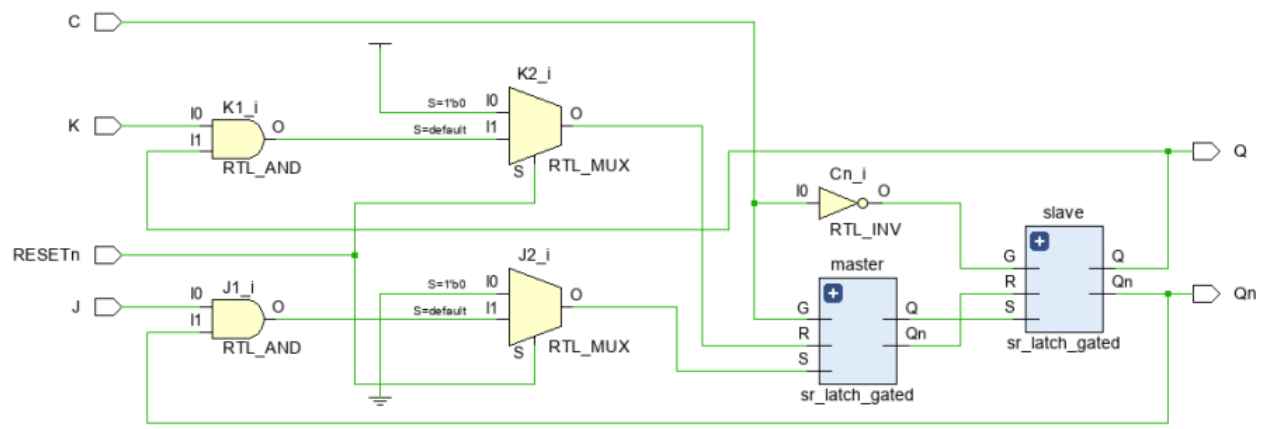
Verilogcode:-

```
module jk_flip_flop_master_slave(Q, Qn, C, J, K, RESETn);
    output Q;
    output Qn;
    input  C;
    input  J;
    input  K;
    input  RESETn;

    wire   MQ;
    wire   MQn;
    wire   Cn;
    wire   J1;
    wire   K1;
    wire   J2;
    wire   K2;
    assign J2 = !RESETn ? 0 : J1;
    assign K2 = !RESETn ? 1 : K1;

    and(J1, J, Qn);
    and(K1, K, Q);
    not(Cn, C);
    sr_latch_gated master(MQ, MQn, C, J2, K2);
    sr_latch_gated slave(Q, Qn, Cn, MQ, MQn);
endmodule


module sr_latch_gated(Q, Qn, G, S, R);
   output Q;
   output Qn;
   input  G;
   input  S;
   input  R;

   wire   S1;
   wire   R1;

   and(S1, G, S);
   and(R1, G, R);
   nor(Qn, S1, Q);
   nor(Q, R1, Qn);
endmodule
```

Test bench:-

```
module JK_ff_tb;

reg C, J, K, RESETn;

wire Q;
wire Qn;

jk_flip_flop_master_slave jkflipflop( .C(C), .RESETn(RESETn), .J(J), .K(K), .Q(Q), .Qn(Qn) );

initial begin
  $dumpfile("dump.vcd"); $dumpvars;
$monitor(C,J,K,Q,Qn,RESETn);

J = 1'b0;
K = 1'b0;
RESETn = 1;
C=1;

#10
RESETn=0;
J=1'b1;
K=1'b0;

#100
RESETn=0;
J=1'b0;
K=1'b1;

#100
RESETn=0;
J=1'b1;
K=1'b1;

#100
RESETn=0;

 #100
 RESETn=0;
 J=1'b1;
 K=1'b1;

 #100
 RESETn=0;
 J=1'b0;
 K=1'b0;

 #100
 RESETn=1;
 J=1'b1;
 K=1'b0;

 end
 always #25 C <= ~C;

 endmodule
```

RTLsymetic:-



Synthesis report:-

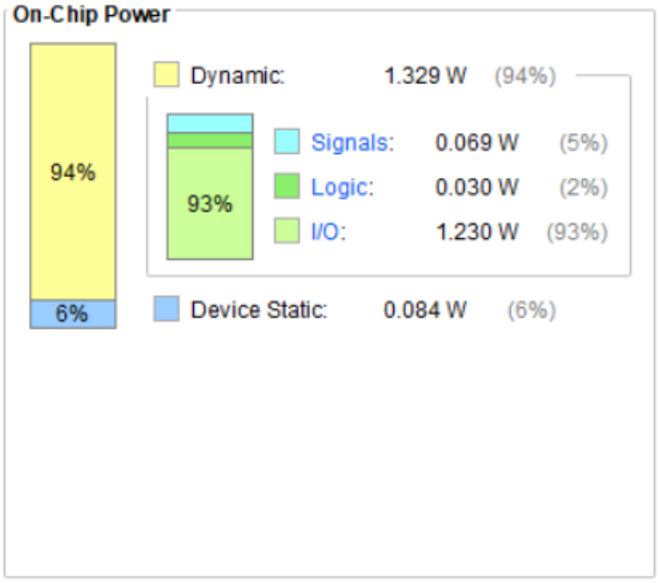
```
Start Writing Synthesis Report
--------------------------------------------------------------------------------

Report BlackBoxes:
+-+--------------+----------+
| |BlackBox name |Instances |
+-+--------------+----------+
+-+--------------+----------+

Report Cell Usage:
+------+-----+------+
|      |Cell |Count |
+------+-----+------+
|1     |LUT3 |     2|
|2     |LUT6 |     2|
|3     |IBUF |     4|
|4     |OBUF |     2|
+------+-----+------+

Report Instance Areas:
+------+---------+-------+------+
|      |Instance |Module |Cells |
+------+---------+-------+------+
|1     |top      |       |    10|
+------+---------+-------+------+
--------------------------------------------------------------------------------
Finished Writing Synthesis Report : Time (s): cpu = 00:00:15 ; elapsed = 00:00:28 . Memory (MB): peak = 1015.500 ; gai = 0.0
```

Power report:-

Power estimation from Synthesized netlist. Activity derived from constraints files, simulation files or vectorless analysis. Note: these early estimates can change after implementation.

Total On-Chip Power:	**1.413 W**
Design Power Budget:	**Not Specified**
Power Budget Margin:	**N/A**
Junction Temperature:	**27.7°C**
Thermal Margin:	57.3°C (30.2 W)
Effective ϑJA:	1.9°C/W
Power supplied to off-chip devices:	0 W
Confidence level:	Low

Launch Power Constraint Advisor to find and fix invalid switching activity



Q21 Positive edge triger

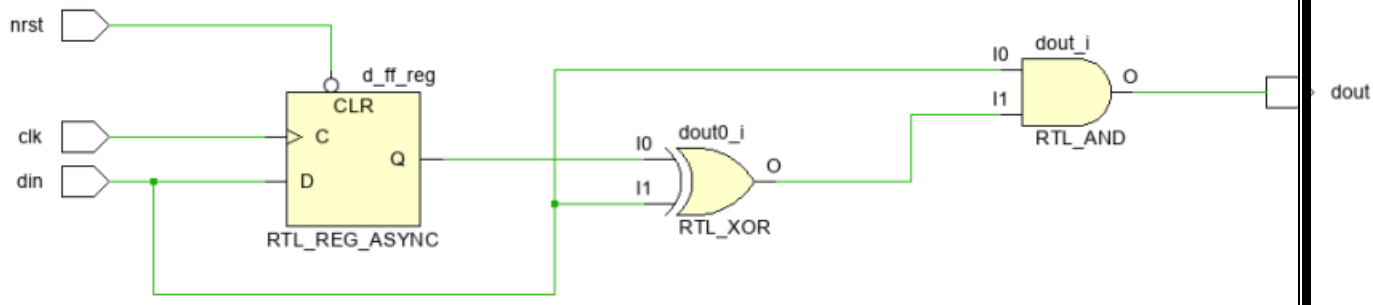
Verilog code:-

```
module pos_edge_detect(clk,nrst,din,dout);
input clk;
input nrst;
input din;
output dout;
reg d_ff;

always @(posedge clk or negedge nrst)
begin
if(!nrst)
d_ff<=1'b0;
else
d_ff<=din;
end
 assign dout=din&&(d_ff^din);
 endmodule

 module d_ff(D,C,a);
input D;
input C;
output a;
reg a;
always @(posedge C)
begin
 a <= D;
end
endmodule
```

Testbench:-

```
module tb;
    reg nrst;
    reg clk;
    reg din;
    wire dout;

    pos_edge_det ped0 (  .nrst(nrst),
                         .clk(clk),
                         .din(din),.dout(dout));



    always #5 clk = ~clk;


    initial begin
        clk <= 0;
        nrst <= 0;
        #15 nrst<= 1;
        #20 nrst<= 0;
        #15 nrst<= 1;
        #10 nrst <= 0;
        #20 $finish;
    end

    initial begin
        $dumpvars;
      $dumpfile("dump.vcd");
    end
endmodule
```

RTLsymatic:-



Synthesis report:-

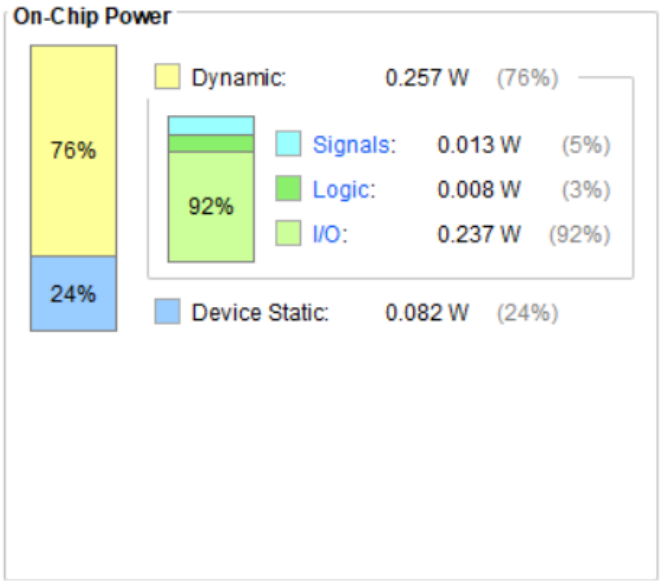
```
Start Writing Synthesis Report
-------------------------------------------------------------------------------

Report BlackBoxes:
+-+--------------+----------+
| |BlackBox name |Instances |
+-+--------------+----------+
+-+--------------+----------+

Report Cell Usage:
+------+-----+------+
|      |Cell |Count |
+------+-----+------+
|1     |BUFG |     1|
|2     |LUT1 |     1|
|3     |LUT2 |     1|
|4     |FDCE |     1|
|5     |IBUF |     3|
|6     |OBUF |     1|
+------+-----+------+

Report Instance Areas:
+------+---------+-------+------+
|      |Instance |Module |Cells |
+------+---------+-------+------+
|1     |top      |       |     8|
+------+---------+-------+------+
-------------------------------------------------------------------------------
Finished Writing Synthesis Report : Time (s): cpu = 00:00:20 ; elapsed = 00:00:41 . Memory (MB): peak = 1018.688 ; ga h = 0.
```

Power report:-

Power estimation from Synthesized netlist. Activity derived from constraints files, simulation files or vectorless analysis. Note: these early estimates can change after implementation.

Total On-Chip Power:	**0.339 W**
Design Power Budget:	**Not Specified**
Power Budget Margin:	**N/A**
Junction Temperature:	**25.6°C**
Thermal Margin:	59.4°C (31.3 W)
Effective ϑJA:	1.9°C/W
Power supplied to off-chip devices:	0 W
Confidence level:	Low

Launch Power Constraint Advisor to find and fix invalid switching activity



Q22 Bcd adder

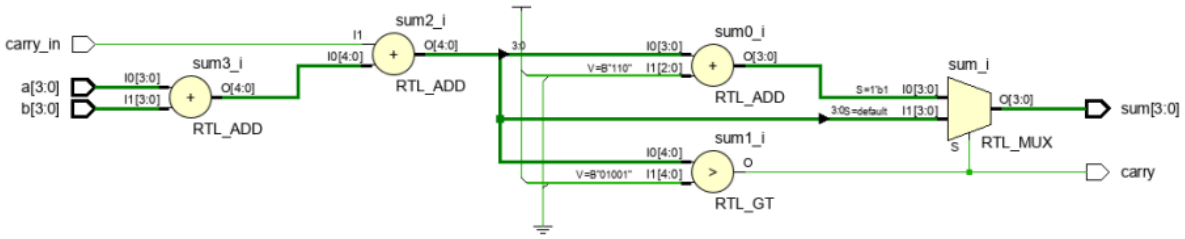
Verilog code:-

```
module bcd_adder(a,b,carry_in,sum,carry);


    input [3:0] a,b;
    input carry_in;
    output [3:0] sum;
    output carry;

    reg [4:0] sum_temp;
    reg [3:0] sum;
    reg carry;


    always @(a,b,carry_in)
    begin
        sum_temp = a+b+carry_in;
        if(sum_temp > 9)    begin
            sum_temp = sum_temp+6;
            carry = 1;
            sum = sum_temp[3:0];    end
        else    begin
            carry = 0;
            sum = sum_temp[3:0];
        end
    end

endmodule
```

Test bench:-

```
module tb_bcdadder;

    reg [3:0] a;
    reg [3:0] b;
    reg carry_in;


    wire [3:0] sum;
    wire carry;


    bcd_adder uut (
        .a(a),
        .b(b),
        .carry_in(carry_in),
        .sum(sum),
        .carry(carry)
    );

    initial begin

        a = 0;  b = 0;  carry_in = 0;   #100;
        a = 6;  b = 9;  carry_in = 0;   #100;
        a = 3;  b = 3;  carry_in = 1;   #100;
        a = 4;  b = 5;  carry_in = 0;   #100;
        a = 8;  b = 2;  carry_in = 0;   #100;
        a = 9;  b = 9;  carry_in = 1;   #100;
    end
```

RTLsymatic:-



Symatic report:-

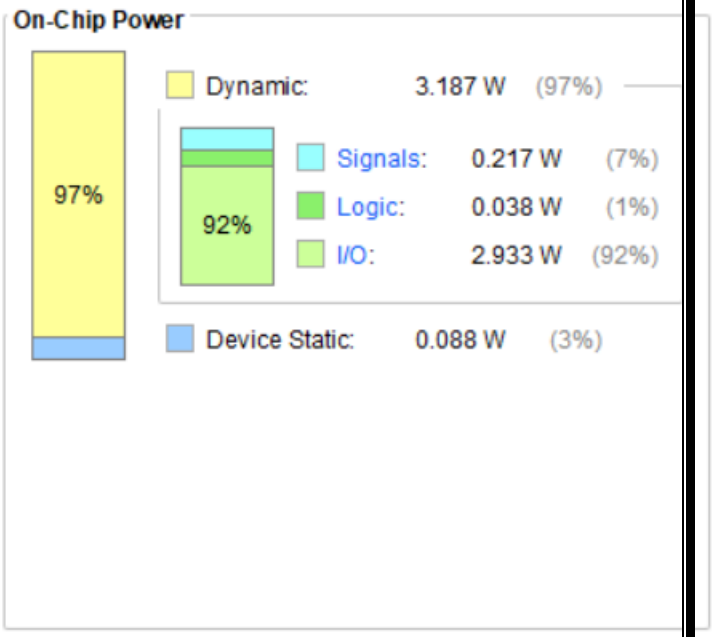
```
---------------------------------------------------------------------------------
Start Writing Synthesis Report
---------------------------------------------------------------------------------

Report BlackBoxes:
+-+--------------+----------+
| |BlackBox name |Instances |
+-+--------------+----------+
+-+--------------+----------+

Report Cell Usage:
+------+-----+------+
|      |Cell |Count |
+------+-----+------+
|1     |LUT3 |     1|
|2     |LUT5 |     2|
|3     |LUT6 |     4|
|4     |IBUF |     9|
|5     |OBUF |     5|
+------+-----+------+

Report Instance Areas:
+------+---------+-------+------+
|      |Instance |Module |Cells |
+------+---------+-------+------+
|1     |top      |       |    21|
+------+---------+-------+------+
---------------------------------------------------------------------------------
Finished Writing Synthesis Report : Time (s): cpu = 00:00:23 ; elapsed = 00:00:44 . Memory (MB): peak = 1016.285 ; ga n = 0.
---------------------------------------------------------------------------------
```

Power report:-

Power estimation from Synthesized netlist. Activity derived from constraints files, simulation files or vectorless analysis. Note: these early estimates can change after implementation.

Total On-Chip Power:	**3.275 W**
Design Power Budget:	**Not Specified**
Power Budget Margin:	**N/A**
Junction Temperature:	**31.2°C**
Thermal Margin:	53.8°C (28.4 W)
Effective ϑJA:	1.9°C/W
Power supplied to off-chip devices:	0 W
Confidence level:	Low

Launch Power Constraint Advisor to find and fix invalid switching activity



Q23 4 bit carry set

Verilog code:-

```
module carry_select_adder
        (   input [3:0] A,B,
            input cin,
            output [3:0] S,
            output cout
            );


wire [3:0] temp0,temp1,carry0,carry1;


fulladder fa00(A[0],B[0],1'b0,temp0[0],carry0[0]);
fulladder fa01(A[1],B[1],carry0[0],temp0[1],carry0[1]);
fulladder fa02(A[2],B[2],carry0[1],temp0[2],carry0[2]);
fulladder fa03(A[3],B[3],carry0[2],temp0[3],carry0[3]);


fulladder fa10(A[0],B[0],1'b1,temp1[0],carry1[0]);
fulladder fa11(A[1],B[1],carry1[0],temp1[1],carry1[1]);
fulladder fa12(A[2],B[2],carry1[1],temp1[2],carry1[2]);
fulladder fa13(A[3],B[3],carry1[2],temp1[3],carry1[3]);


multiplexer2 mux_carry(carry0[3],carry1[3],cin,cout);

multiplexer2 mux_sum0(temp0[0],temp1[0],cin,S[0]);
multiplexer2 mux_sum1(temp0[1],temp1[1],cin,S[1]);
multiplexer2 mux_sum2(temp0[2],temp1[2],cin,S[2]);
multiplexer2 mux_sum3(temp0[3],temp1[3],cin,S[3]);

endmodule
```

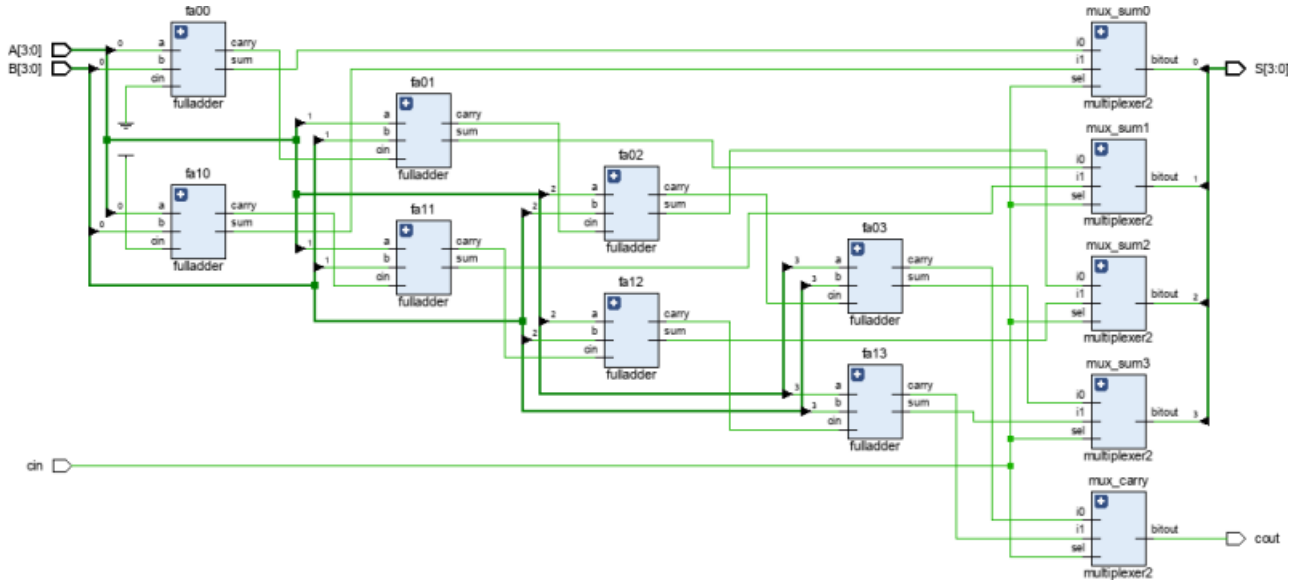
```
module fulladder
        (   input a,b,cin,
            output sum,carry
            );

assign sum = a ^ b ^ cin;
assign carry = (a & b) | (cin & b) | (a & cin);

endmodule

module multiplexer2
        (   input i0,i1,sel,
            output reg bitout
            );

always@(i0,i1,sel)
begin
if(sel == 0)
    bitout = i0;
else
    bitout = i1;
end

endmodule
```

TestBench:-

```
module tb_adder;


    reg [3:0] A;
    reg [3:0] B;
    reg cin;

    wire [3:0] S;
    wire cout;
    integer i,j,error;


    carry_select_adder uut (
        .A(A),
        .B(B),
        .cin(cin),
        .S(S),
        .cout(cout)
    );



    initial begin

        A = 0;
        B = 0;
        error = 0;

        cin = 0;
      for(i=0;i<16;i=i+1) begin
            for(j=0;j<16;j=j+1) begin
                A = i;
                B = j;
                #10;
                if({cout,S} != (i+j))
```

```
        end

        cin = 1;
        for(i=0;i<16;i=i+1) begin
              for(j=0;j<16;j=j+1) begin
                    A = i;
                    B = j;
                    #10;
                    if({cout,S} != (i+j+1))
                          error <= error + 1;
              end
        end
    end

endmodule
```

RTLsymatic:-



Synthesis report:-

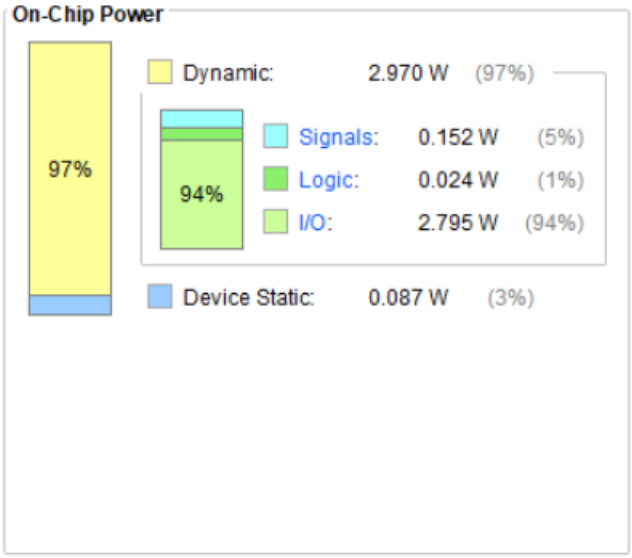
```
Start Writing Synthesis Report
--------------------------------------------------------------------------------

Report BlackBoxes:
+-+--------------+----------+
| |BlackBox name |Instances |
+-+--------------+----------+
+-+--------------+----------+

Report Cell Usage:
+------+-----+------+
|      |Cell |Count |
+------+-----+------+
|1     |LUT3 |     2|
|2     |LUT5 |     4|
|3     |IBUF |     9|
|4     |OBUF |     5|
+------+-----+------+

Report Instance Areas:
+------+---------+-------+------+
|      |Instance |Module |Cells |
+------+---------+-------+------+
|1     |top      |       |    20|
+------+---------+-------+------+
--------------------------------------------------------------------------------
Finished Writing Synthesis Report : Time (s): cpu = 00:00:22 ; elapsed = 00:00:43 . Memory (MB): peak = 1017.844 ; gain = 0.000
```

Power report:-

Power estimation from Synthesized netlist. Activity derived from constraints files, simulation files or vectorless analysis. Note: these early estimates can change after implementation.

Total On-Chip Power:	**3.058 W**
Design Power Budget:	**Not Specified**
Power Budget Margin:	**N/A**
Junction Temperature:	**30.8°C**
Thermal Margin:	54.2°C (28.6 W)
Effective ϑJA:	1.9°C/W
Power supplied to off-chip devices:	0 W
Confidence level:	Low

Launch Power Constraint Advisor to find and fix invalid switching activity



Q24 More fsm 1010 sequence detector

Verilog code:-

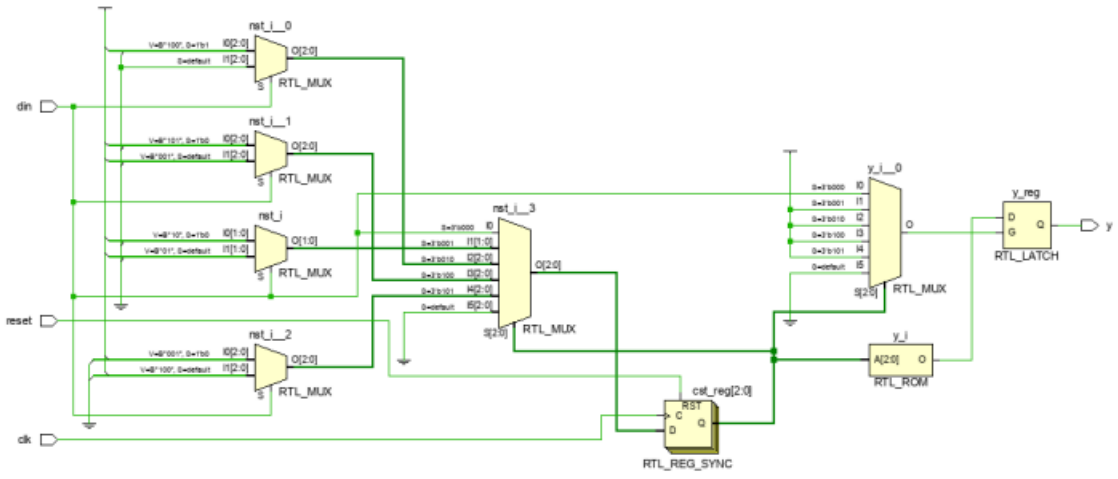
```
module morfsmolp(din, reset, clk, y);
input din;
input clk;
input reset;
output reg y;
reg [2:0] cst, nst;
parameter S0 = 3'b000,
          S1 = 3'b001,
          S2 = 3'b010,
          S3 = 3'b100,
            S4 = 3'b101;
always @(cst or din)
 begin
 case (cst)
   S0: if (din == 1'b1)
          begin
         nst = S1;
          y=1'b0;
          end
      else nst = cst;
   S1: if (din == 1'b0)
          begin
        nst = S2;
          y=1'b0;
          end
       else
          begin
          nst = cst;
          y=1'b0;
          end
   S2: if (din == 1'b1)
          begin
         nst = S3;
          y=1'b0;
          end
```

```
    S3: if (din == 1'b0)
            begin
           nst = S4;
            y=1'b0;
            end
         else
            begin
            nst = S1;
            y=1'b0;
            end
S4: if (din == 1'b0)
            begin
           nst = S1;
            y=1'b1;
            end
            else
            begin
            nst = S3;
            y=1'b1;
            end
    default: nst = S0;
  endcase
end
always@(posedge clk)
begin
            if (reset)
            cst <= S0;
            else
              cst <= nst;
end
endmodule
```

Test bench:-

```
module morfsmolp_tb;
reg din,clk,reset;
wire y;
morfsmolp m1(din, reset, clk, y);
initial
begin
reset=0       ;clk=0;din=0;
$monitor($time, , ,"c=%b",clk,,"y=%b",y,,"r=%b",reset,,"d=%b",din);
#10 din=1;
#10 din=0;
#10 din=1;
#10 din=0;
end
always
#5 clk=~clk;
initial
#100 $finish ;
endmodule
```

RTLsymatic:-



Synthesis report:-

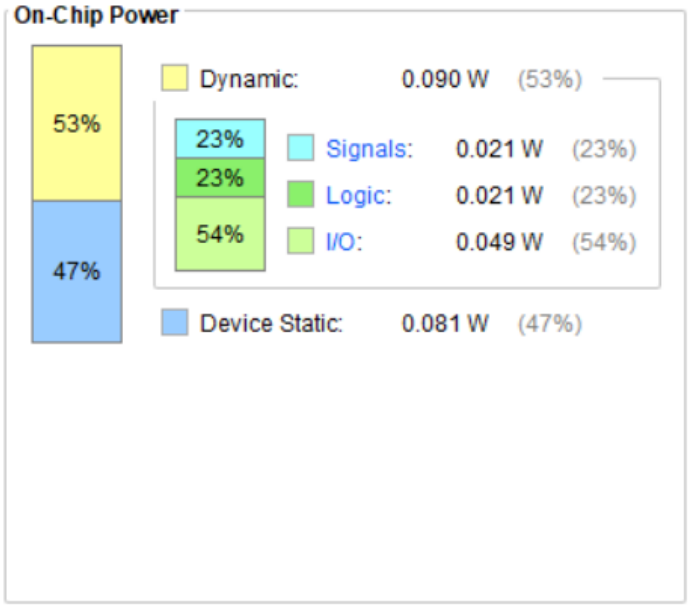
```
Start Writing Synthesis Report
-------------------------------------------------------------------------------

Report BlackBoxes:
+-+--------------+----------+
| |BlackBox name |Instances |
+-+--------------+----------+
+-+--------------+----------+

Report Cell Usage:
+------+-----+------+
|      |Cell |Count |
+------+-----+------+
|1     |BUFG |     1|
|2     |LUT2 |     2|
|3     |LUT3 |     2|
|4     |LUT5 |     1|
|5     |LUT6 |     1|
|6     |FDRE |     4|
|7     |FDSE |     1|
|8     |LD   |     1|
|9     |IBUF |     3|
|10    |OBUF |     1|
+------+-----+------+

Report Instance Areas:
+------+---------+------+------+
|      |Instance |Module |Cells |
+------+---------+------+------+
|1     |top      |       |    17|
+------+---------+------+------+
-------------------------------------------------------------------------------
Finished Writing Synthesis Report : Time (s): cpu = 00:00:10 ; elapsed = 00:00:17 . Memory (MB): peak = 1017.680 ; gain =
```

Power report:-

Power estimation from Synthesized netlist. Activity derived from constraints files, simulation files or vectorless analysis. Note: these early estimates can change after implementation.

Total On-Chip Power:	**0.172 W**
Design Power Budget:	**Not Specified**
Power Budget Margin:	**N/A**
Junction Temperature:	**25.3°C**
Thermal Margin:	59.7°C (31.5 W)
Effective ϑJA:	1.9°C/W
Power supplied to off-chip devices:	0 W
Confidence level:	Low

Launch Power Constraint Advisor to find and fix invalid switching activity



Q25 N X 1 mux

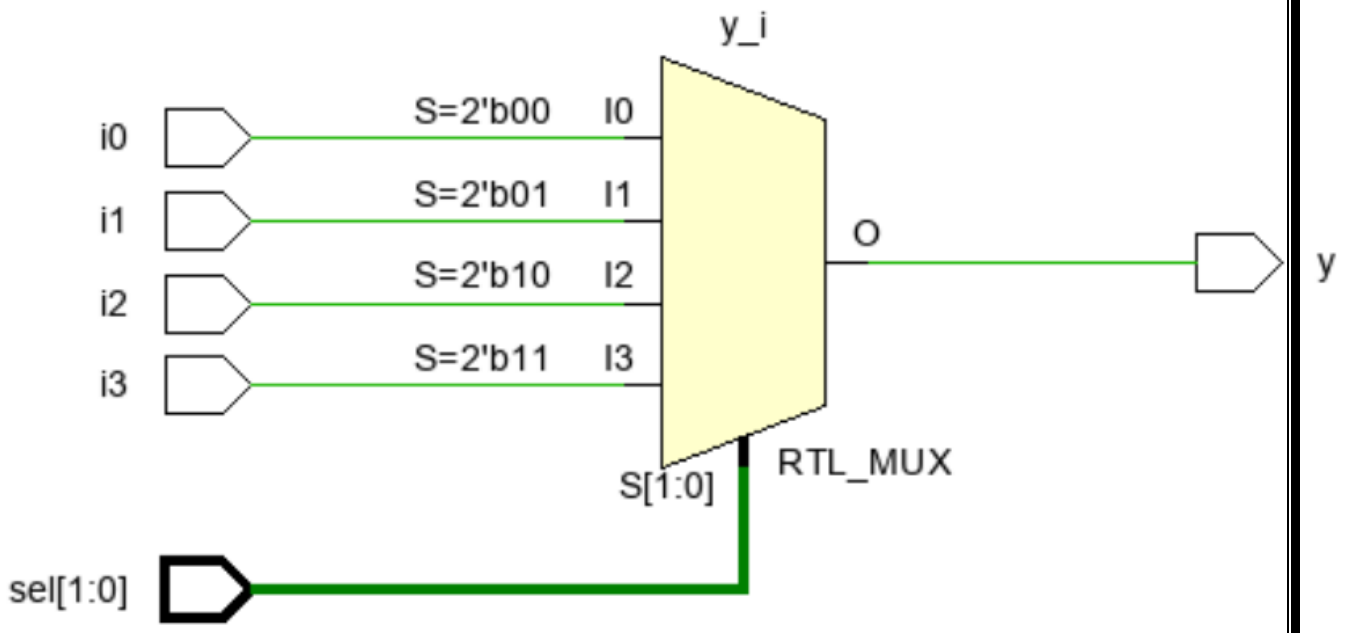
Verilog code:-

```
module mux_4_1(
  input [1:0] sel,
  input  i0,i1,i2,i3,
  output reg y);

  always @(*) begin
    case(sel)
      2'h0: y = i0;
      2'h1: y = i1;
      2'h2: y = i2;
      2'h3: y = i3;
      default: $display("Invalid sel input");
    endcase
  end
endmodule
```

Test bench:-

```
module tb;
  reg [1:0] sel;
  reg i0,i1,i2,i3;
  wire y;

  mux_example mux(sel, i0, i1, i2, i3, y);

  initial begin
    $monitor("sel = %b -> i3 = %0b, i2 = %0b ,i1 = %0b, i0 = %0b -> y = %0b", sel,i3,i2,i1,i0,
    {i3,i2,i1,i0} = 4'h5;
    repeat(6) begin
      sel = $random;
      #5;
    end
  end
endmodule
```

RTL symatic:-



Synthesis report:-

```
Start Writing Synthesis Report
--------------------------------------------------------------------------------

Report BlackBoxes:
+-+--------------+----------+
| |BlackBox name |Instances |
+-+--------------+----------+
+-+--------------+----------+

Report Cell Usage:
+------+-----+------+
|      |Cell |Count |
+------+-----+------+
|1     |LUT6 |     1|
|2     |IBUF |     6|
|3     |OBUF |     1|
+------+-----+------+

Report Instance Areas:
+------+---------+-------+------+
|      |Instance |Module |Cells |
+------+---------+-------+------+
|1     |top      |       |     8|
+------+---------+-------+------+
--------------------------------------------------------------------------------
Finished Writing Synthesis Report : Time (s): cpu = 00:00:11 ; elapsed = 00:00:20 . Memory (MB): peak = 1020.262 ; gai
```

Power report:-

Power estimation from Synthesized netlist. Activity derived from constraints files, simulation files or vectorless analysis. Note: these early estimates can change after implementation.

Total On-Chip Power:	**0.544 W**
Design Power Budget:	**Not Specified**
Power Budget Margin:	**N/A**
Junction Temperature:	**26.0°C**
Thermal Margin:	59.0°C (31.1 W)
Effective ϑJA:	1.9°C/W
Power supplied to off-chip devices:	0 W
Confidence level:	Low

Launch Power Constraint Advisor to find and fix invalid switching activity