

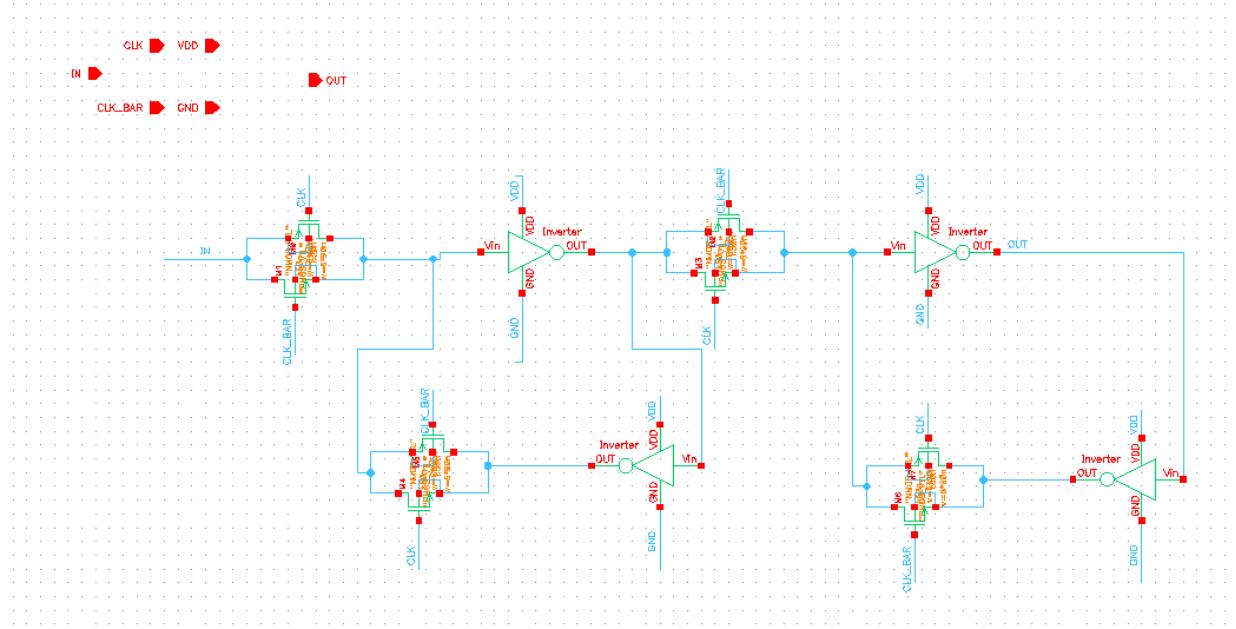
PART-II: REGISTERS AND COLUMN CIRCUITS

Group3

Name	netID	ID number
Li, Kexin	kl2646	N15468435
Qin, Yi	yq468	N18068309
Wang, Hangyu	hw1314	N17992230
Zhang, Chi	cz776	N10471367

PROBLEM 1: Address and Data Registers

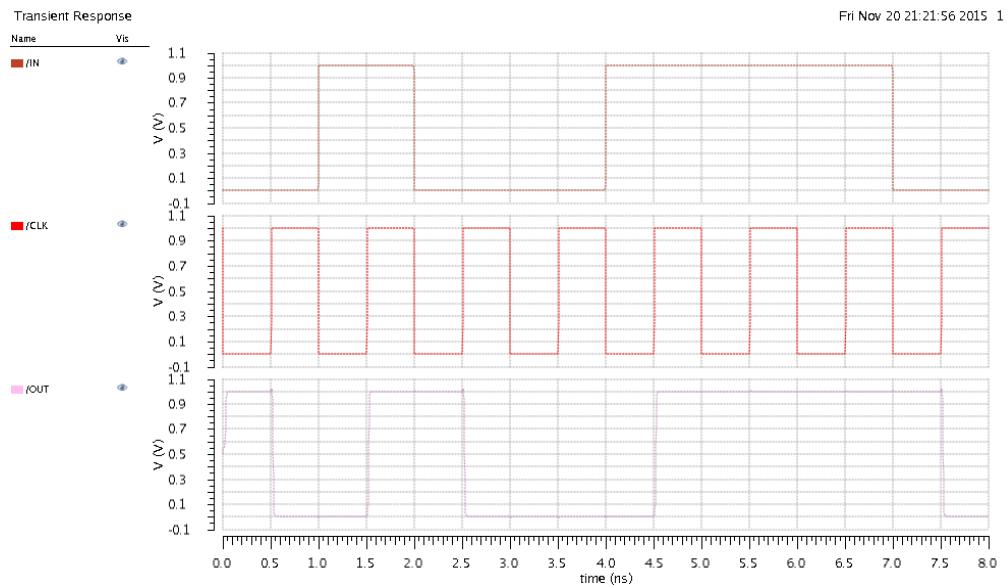
1. Schematic of single flip-flop



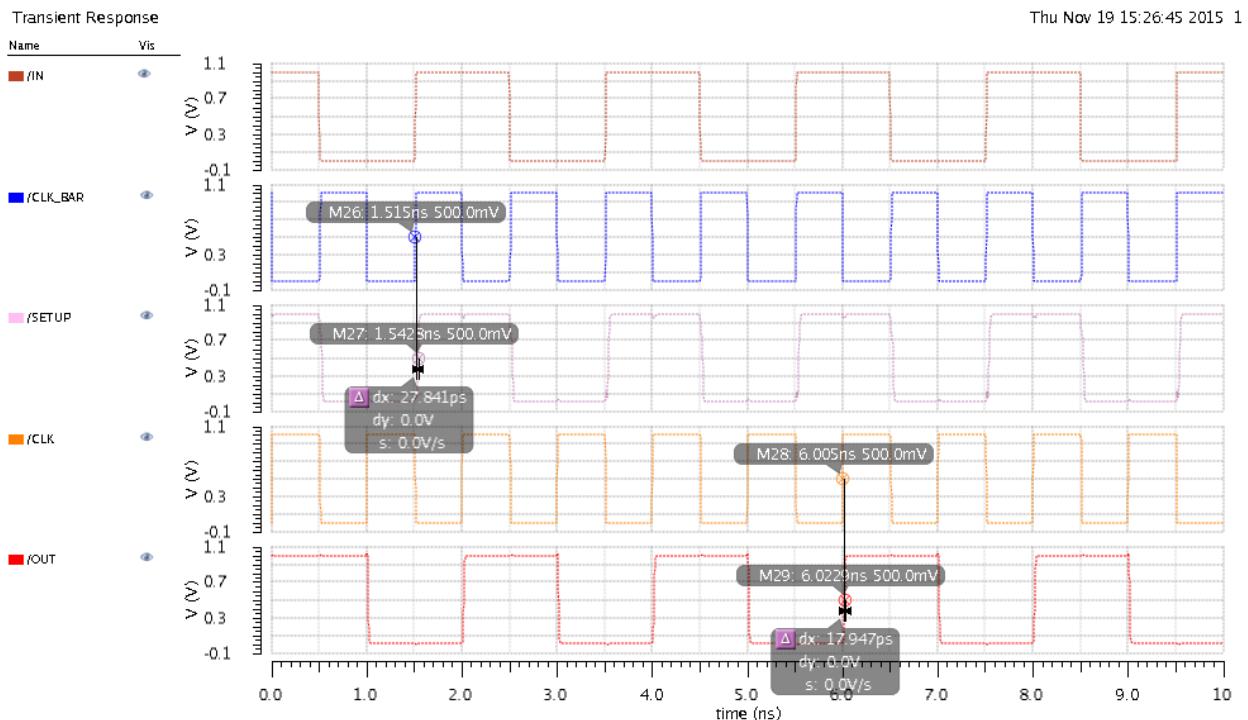
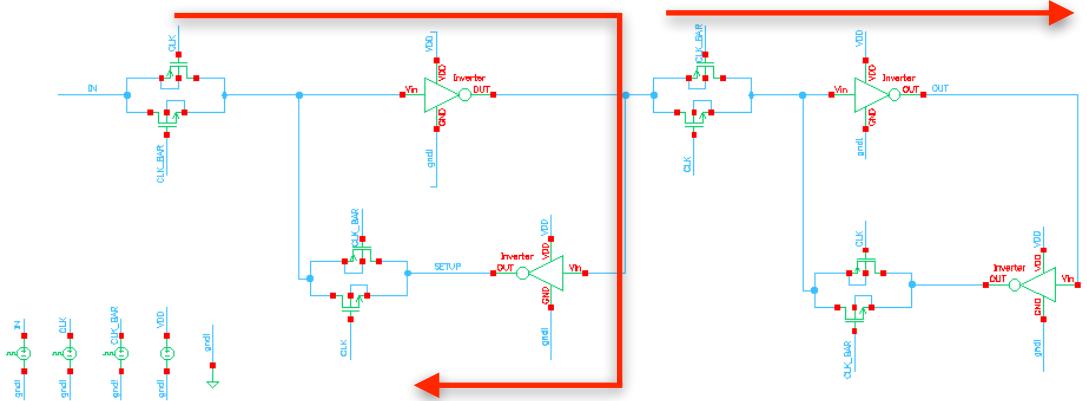
Here, we use positive edge-triggered static Master-slave flip-flop

2. Testing the function of single flip-flop

2.1 Input and Output



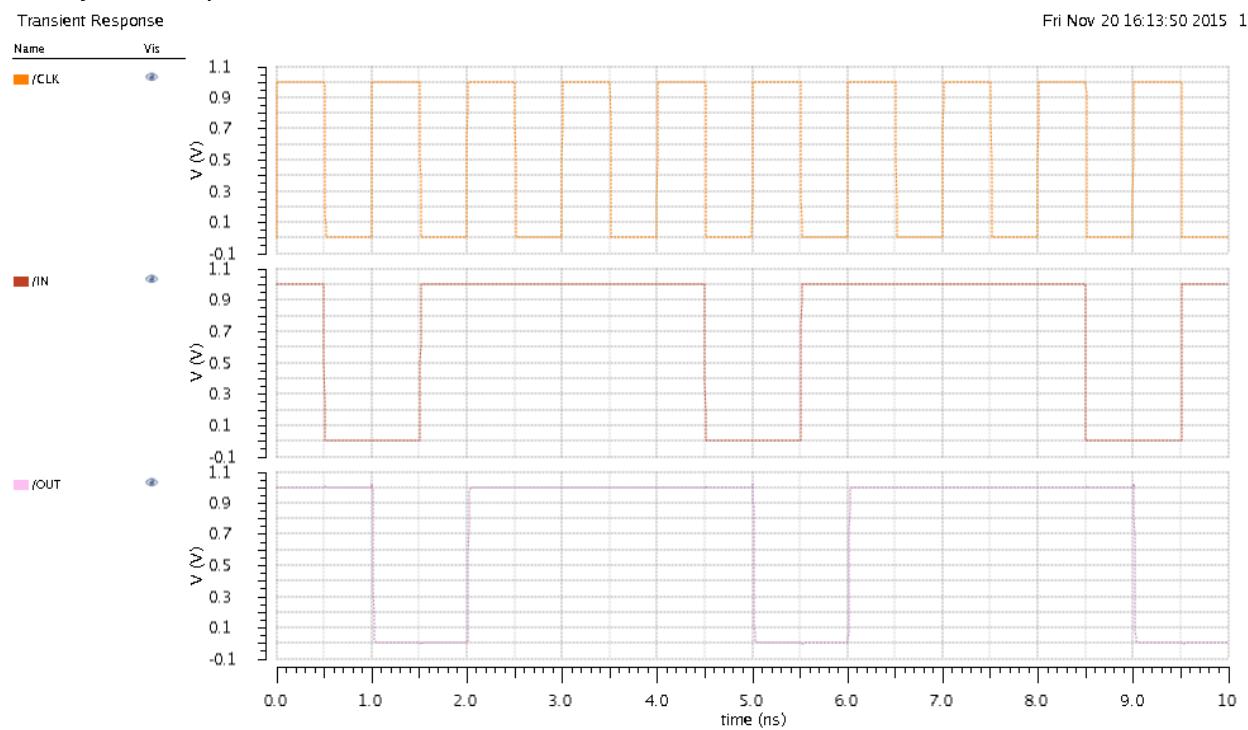
2.2 Setup time and CLK-Q delay



Setup time: the first TG on schematic will transmit signal at posedge of CLK_BAR, so the setup time is $dx = 27.841\text{ps}$ (2.78% of CLK period).

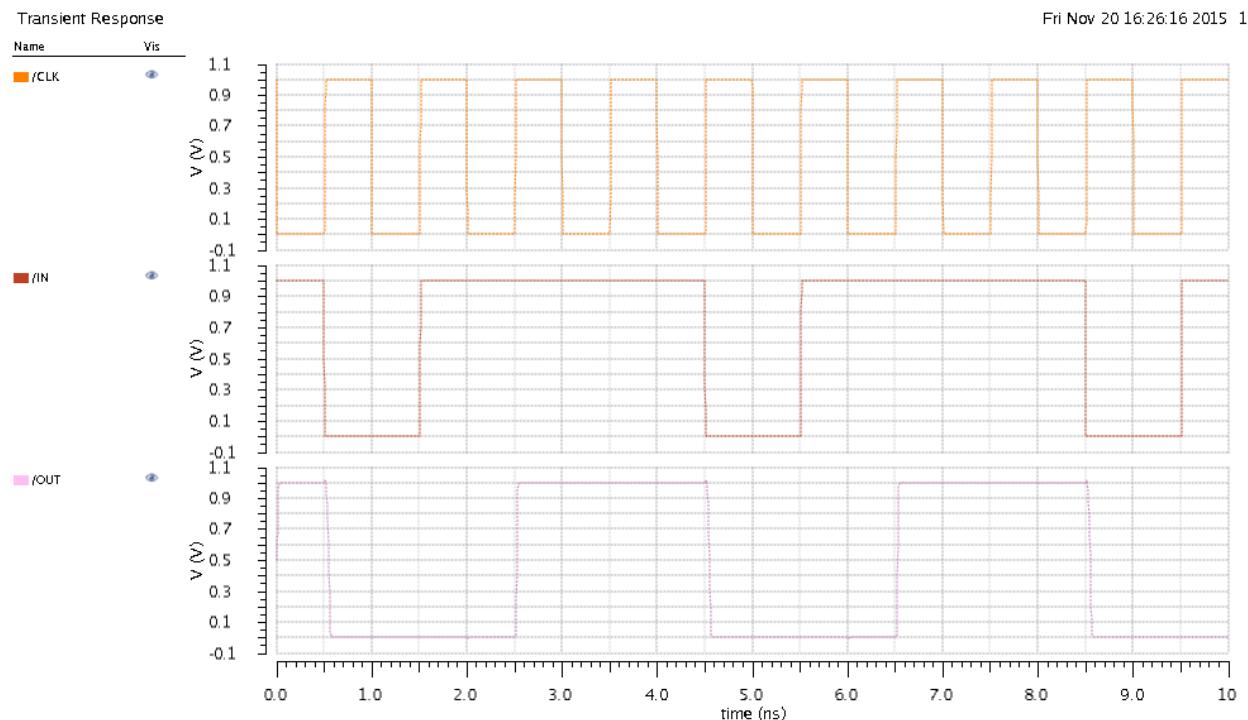
CLK-Q delay: in the slave part, the first TG will transmit signal at posedge of CLK, so the CLK-Q delay is $dx = 17.947\text{ps}$ (1.79% of CLK period).

satisfy the setup time:



Satisfy the setup time situation is above: the flip-flop will transmit signal at the posedge of CLK. From this situation, the CLK can pick up the right IN signal.

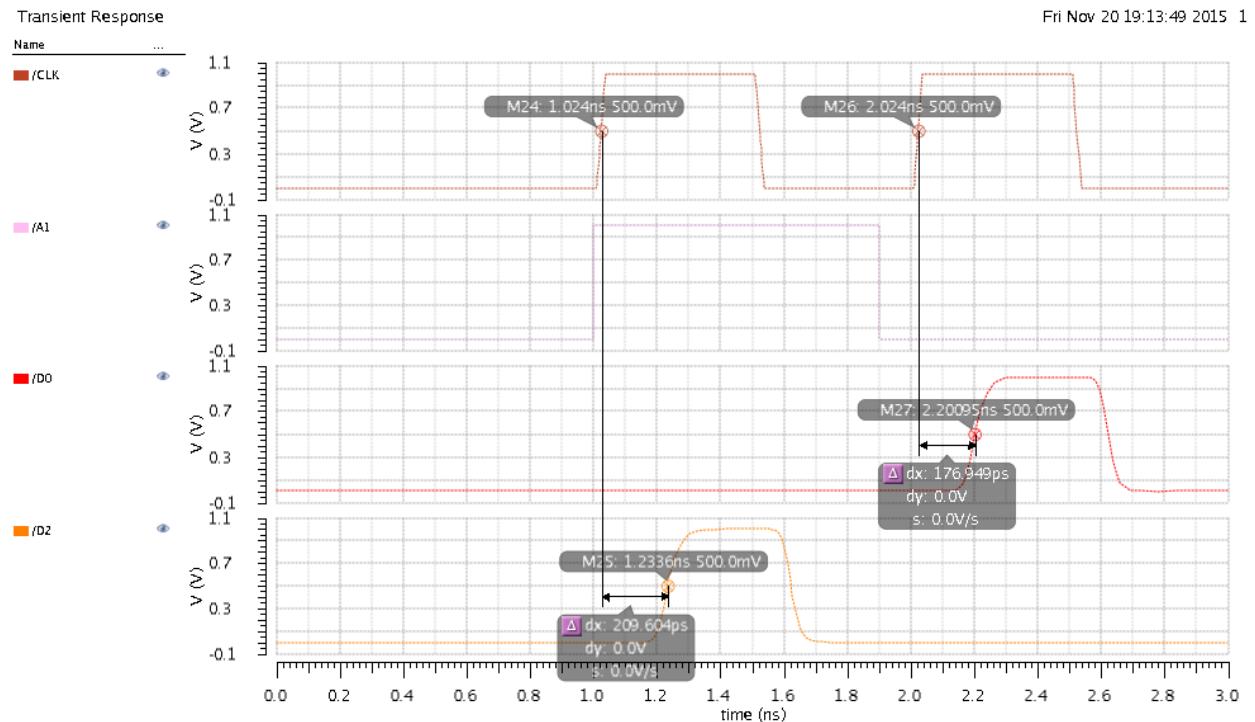
not satisfy the setup time:



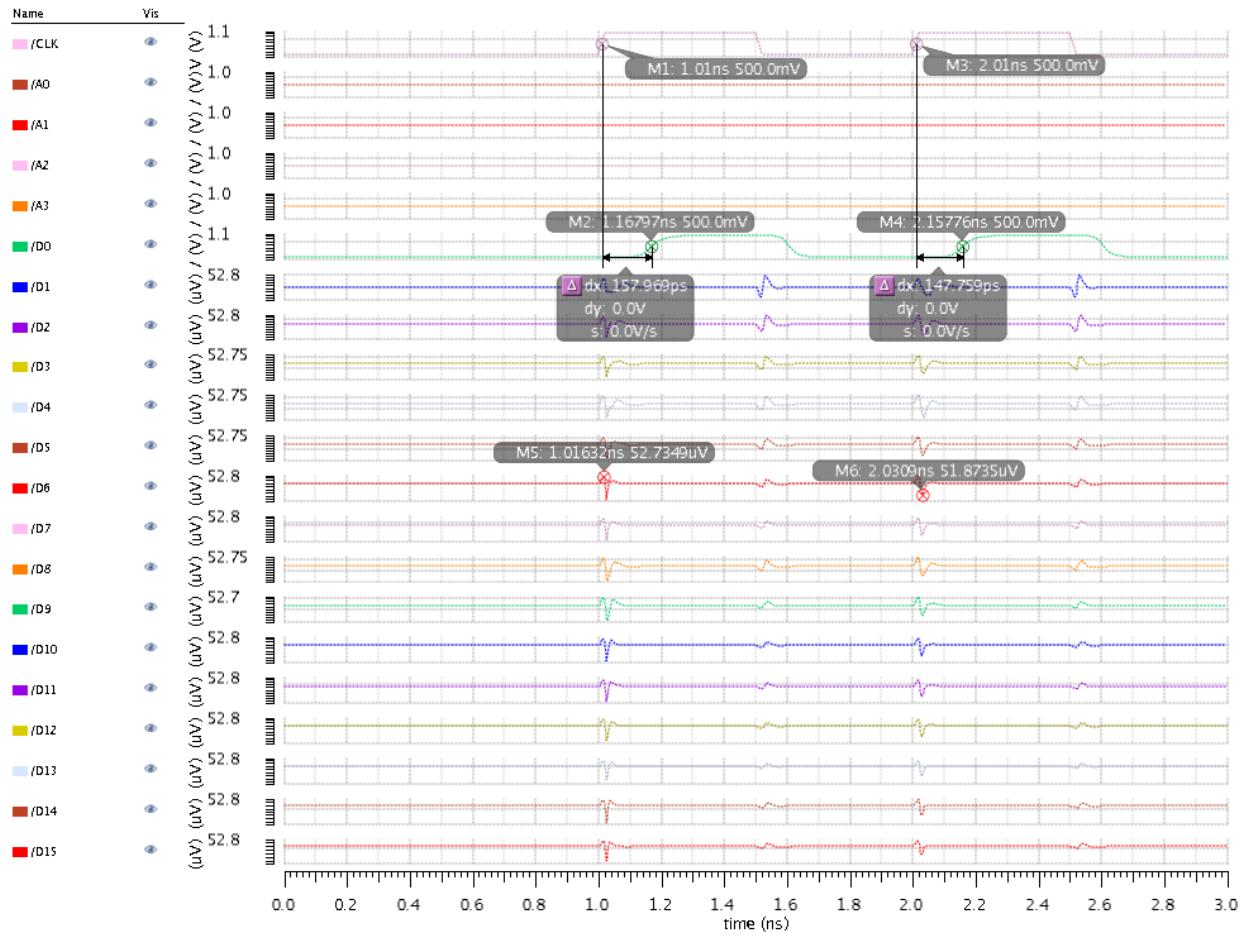
Not satisfy the setup time is above: when we give the posedge of signal exactly as the posedge of CLK coming. Here, the flip-flop is not ready, so at this situation the output signal may be wrong.

Hold time: 0

3. Row testing



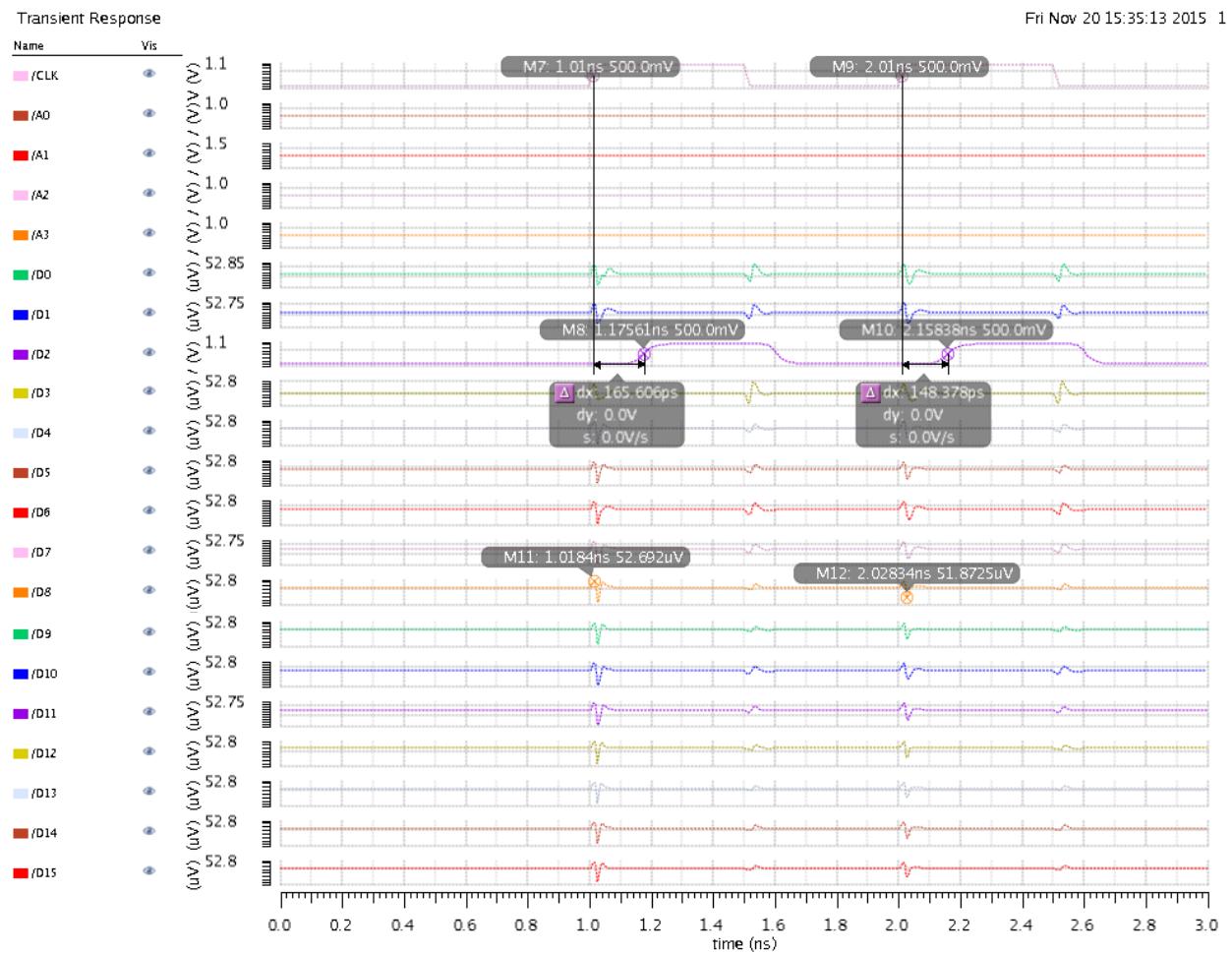
Here, the signal is set as above, and the posedge of A1 comes a little bit earlier than the posedge of CLK, so at the first posedge the input signal is $[A_0 \ A_1 \ A_2 \ A_3] = [0 \ 1 \ 0 \ 0]$. Then, D2 should be '1'. At the second posedge, the input signal is $[A_0 \ A_1 \ A_2 \ A_3] = [0 \ 0 \ 0 \ 0]$. Then, D0 should be '1'. Thus, the result is right.



When the input is $[A_0 \ A_1 \ A_2 \ A_3] = [0 \ 0 \ 0 \ 0]$, all outputs are showed above. According to the input, we can know that the result D0 is active. Since the glitch is much less than threshold voltage, it will not influence the next stage.

The delay here is $dx = 157.9\text{ps}$ and $dx = 147.7\text{ps}$.

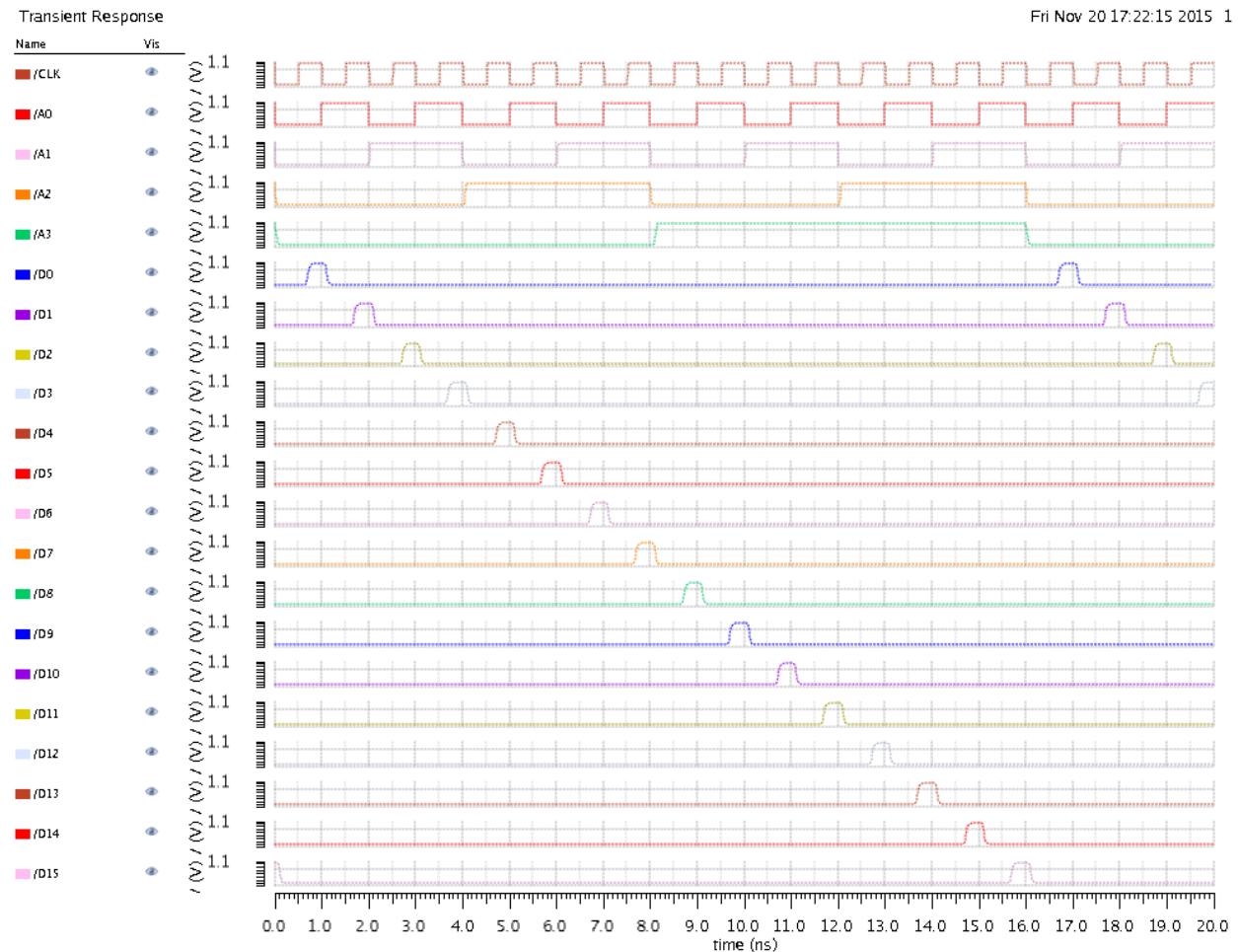
Then here is one more sample:



When the input is $[A_0 \ A_1 \ A_2 \ A_3] = [0 \ 1 \ 0 \ 0]$, all outputs are showed above. Similarly, the D2 is active here and glitch will not influence the next stage.

The delay here is $dx = 165.6\text{ps}$ and $dx = 148.3\text{ps}$.

WL changes state as the applied address changes:



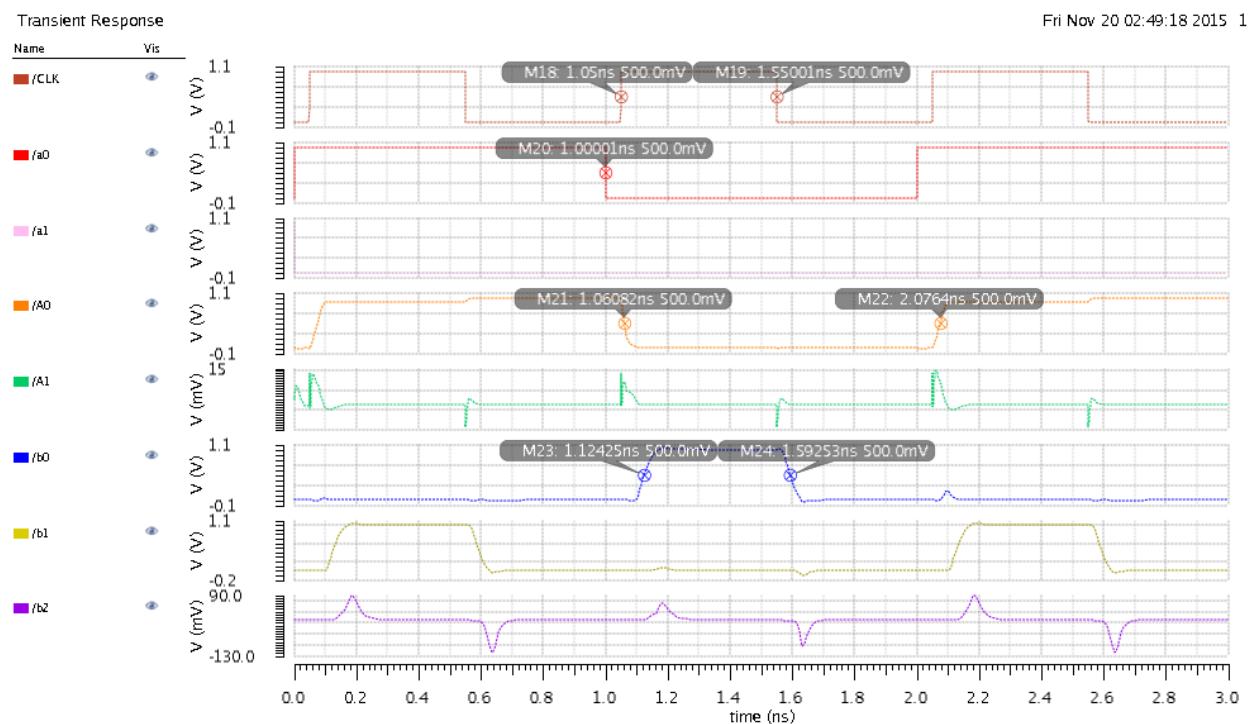
4 Column select signal with column address register:

a0 , a1 is the column address we input.

A0, A1 is the output of column_address_register

b0, b2 is the output of decoder.

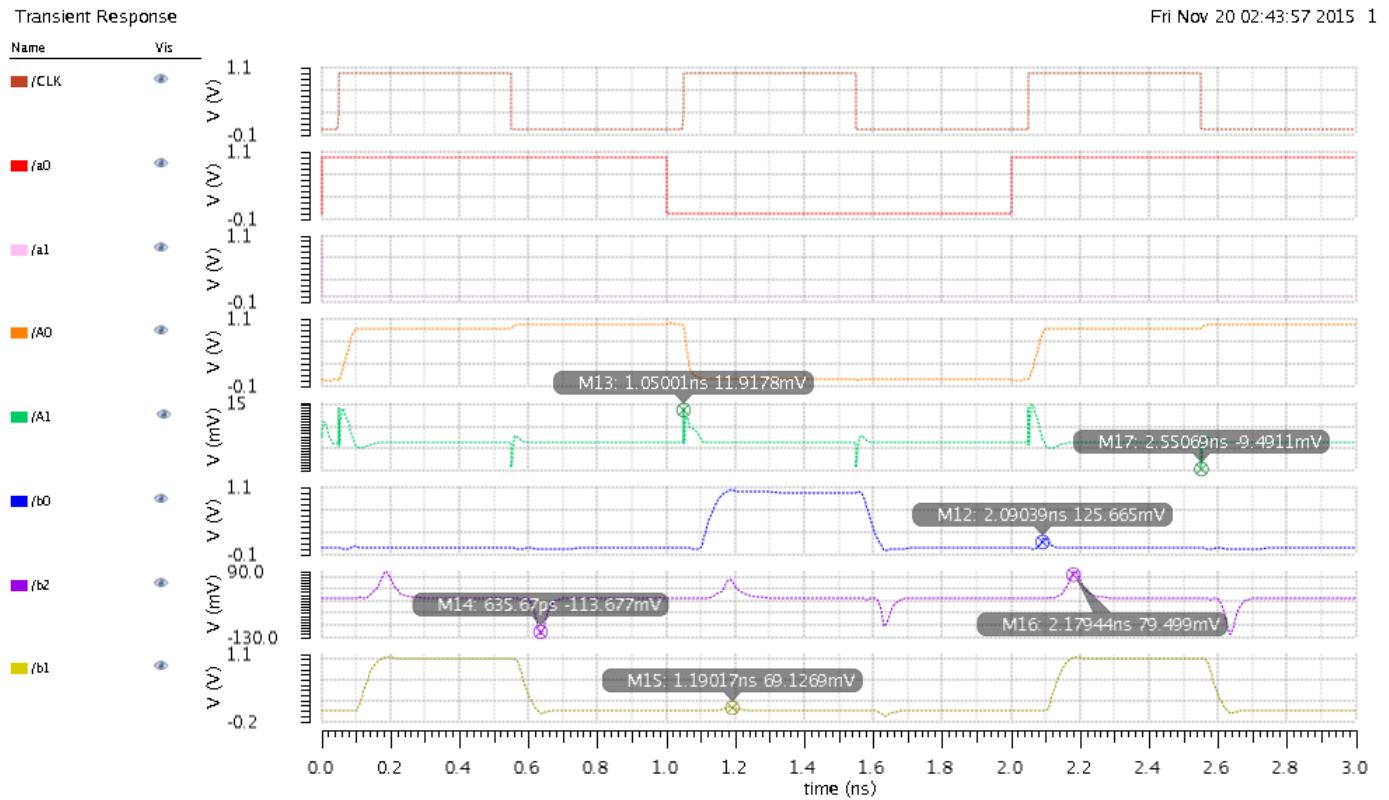
At 1.05ns, when clk is VDD, that means we want to write or read. Then the address input propagate to the register output as we can see a0 → A1. Then, it propagate to the decoder. b0 = VDD. Others are zero.



Delay from write signal to the column select signal:

$$TPLH = 1.12425 - 1.05 = 74.2 \text{ ps}$$

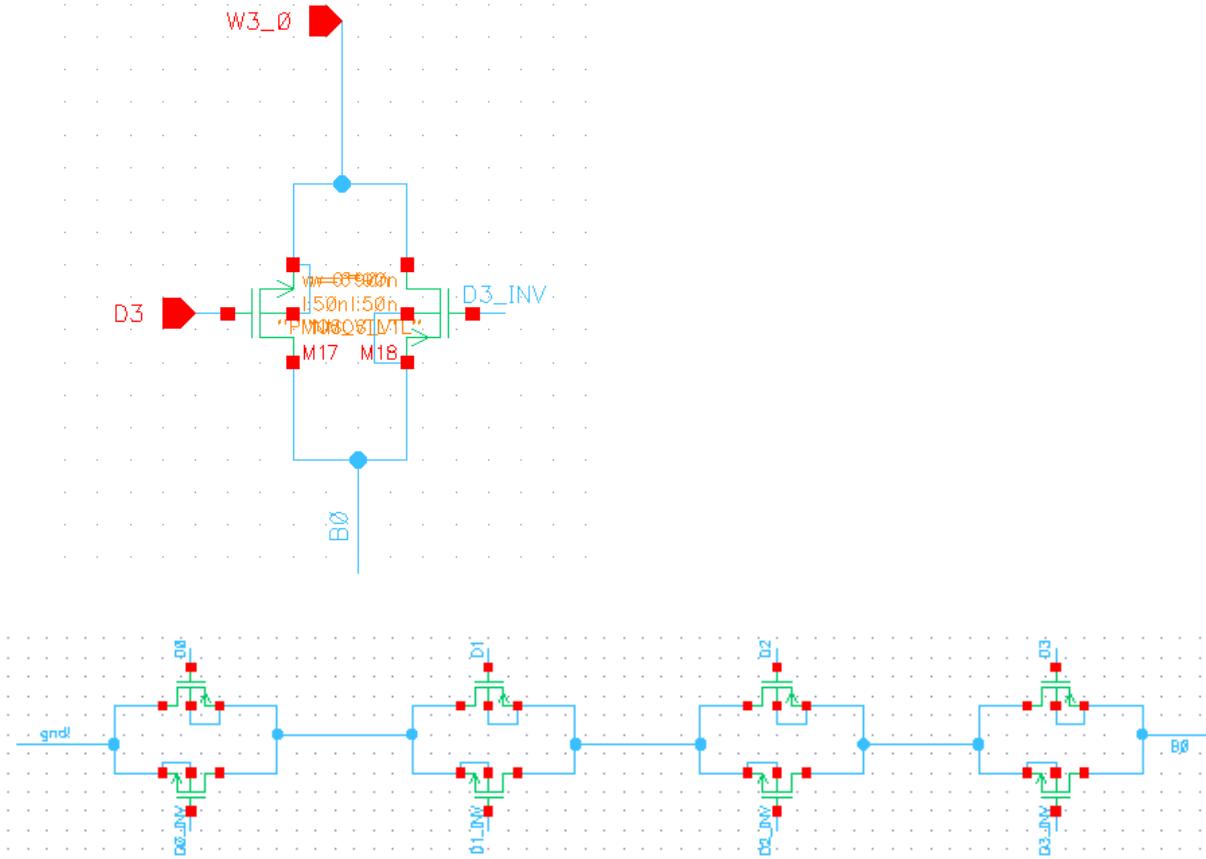
About glitch :



As we can see from picture, the delay of every stage does not exceed threshold voltage (300mV). So it is in safe region.

Problem 2: Column Multiplexer

1. Cadence schematic of the MUX



Explanation:

In the first figure, we can see we connect the output of **column select signal** to the input of MUX as a control signal by using a TG device and connect the **bit line** to the input of TG device . So, the output is what we want to read. And consider that when the column select signal does not give any signal, the output will be floating. So we connect the input of TG to GND when the input is all zero.(Second figure)

So the logic will be :

```

OUT = bit_line_column0 & ( column_select_0 )
OUT = bit_line_column1 & ( column_select_1 )
OUT = bit_line_column2 & ( column_select_2 )
OUT = bit_line_column3 & ( column_select_3 )

```

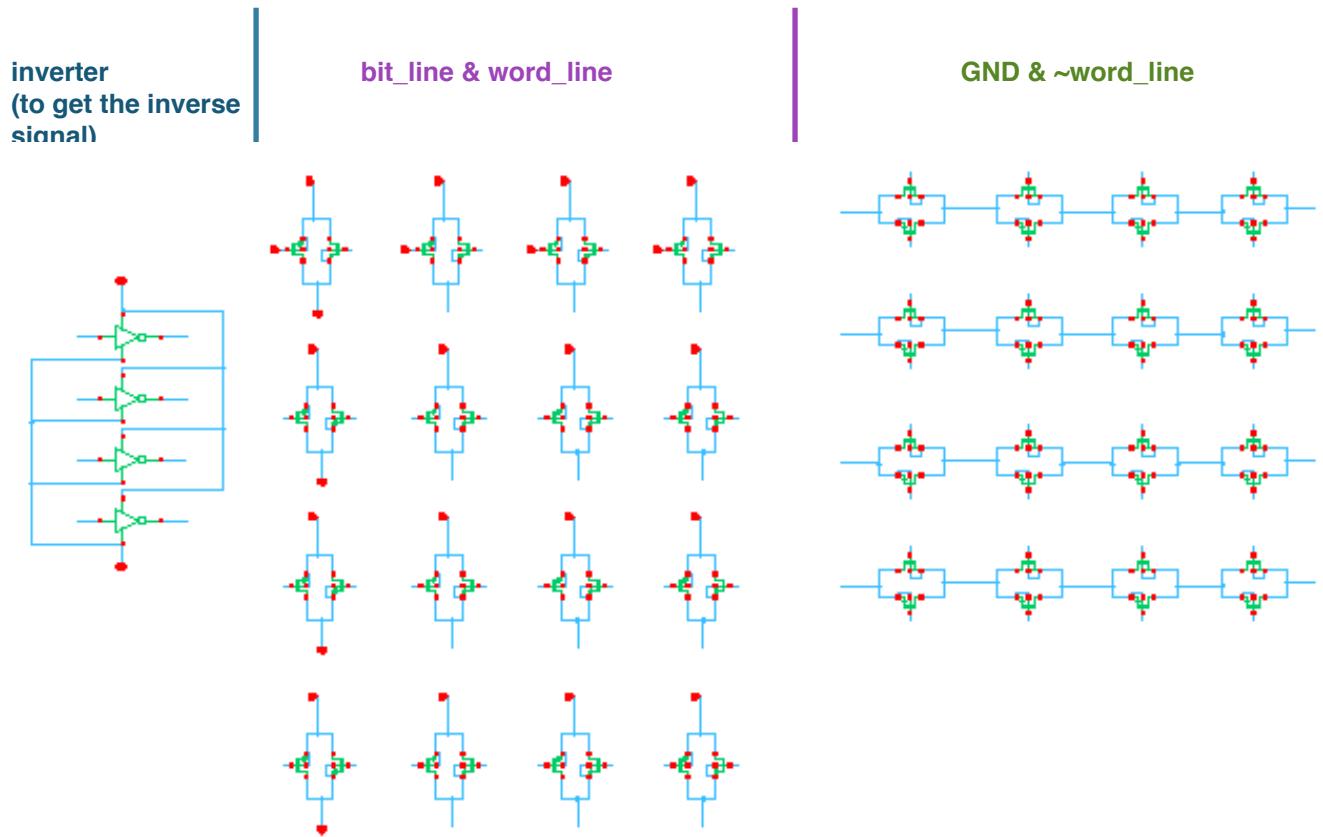
```

OUT = GND & ( ~column_select_0 & ~column_select_1 & ~column_select_2 &
~column_select_3 )

```

That means when there is no column to be selected. The output will be [0 0 0 0].

Overall schematic:



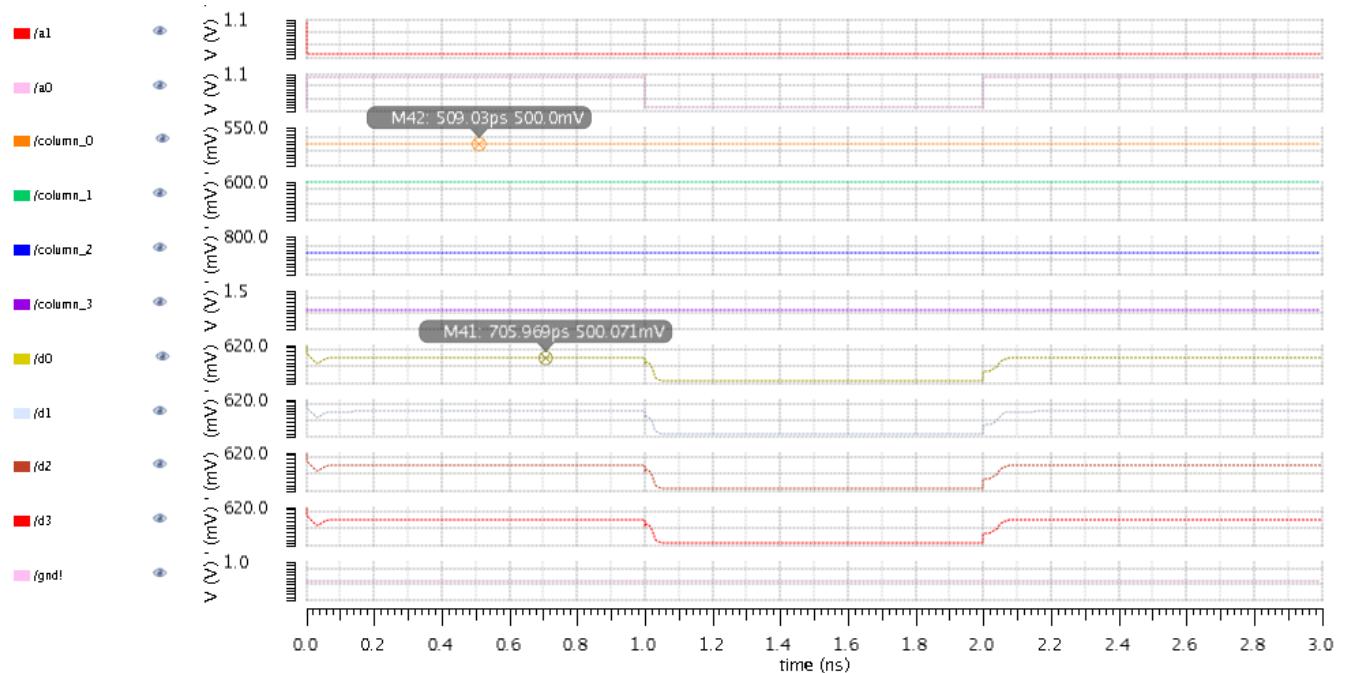
Because we have four bit input for every column, we should repeat for 4 TG. So we have 16 TG to choose and pass by the signal of bit line. In the same way, 16 TG for GND to pass by.

2. Explain how will you verify the correct operation?

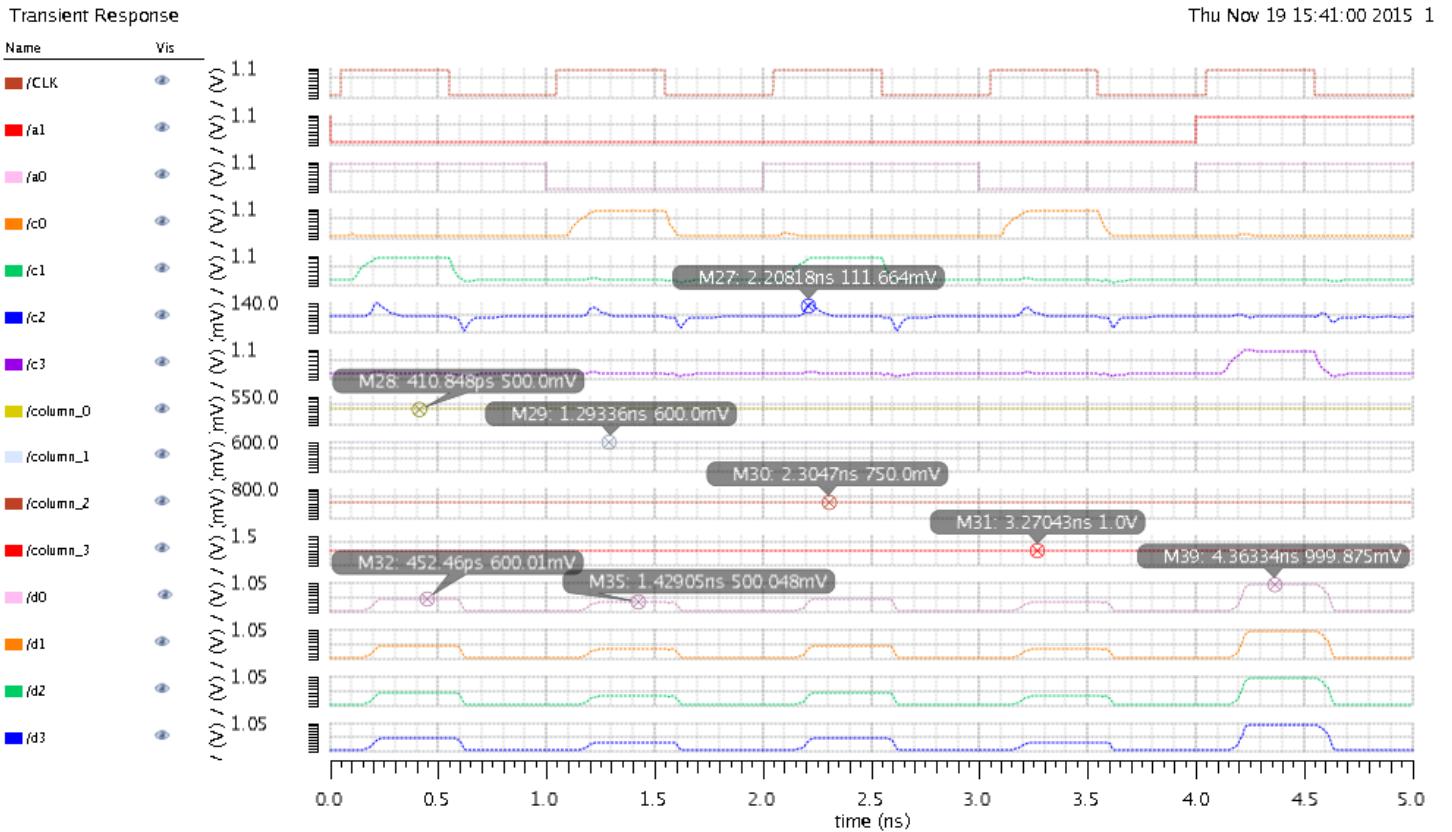
I apply a simple waveform to verify that:

From 0 to 1ns, we set input for MUX is [a3 a2 a1 a0] = 0 0 0 1 And the value of bit line of first column is 500mV , the value of bit line of second column is 600mV , the value of bit line of third column is 800mV , the value of bit line of last column is 1V

When the the a0 (the first bit line) is 1, the four bit output should equal to the value of first column. the 500mV. We can see the output is right



3. Simulation waveform showing correct operation of the MUX during READ



We set the address of column $[a_1 \ a_0] = [0 \ 1]$ during 0 - 1 ns, $[a_1 \ a_0] = [0 \ 0]$ during 1 - 2 ns, $[a_1 \ a_0] = [0 \ 1]$ during 2 - 3 ns, $[a_1 \ a_0] = [0 \ 0]$ during 3 - 4 ns, and $[a_1 \ a_0] = [1 \ 1]$ during 4 - 5 ns

The $[c_3 \ c_2 \ c_1 \ c_0]$ are the output of column select signal. We can see although there are some glitch happening, they will not influence the final output because they do not achieve the value of threshold voltage of NMOS and PMOS. We can see they operate in the right way. When $[a_1 \ a_0] = [0 \ 1]$ during 0 - 1 ns, the second column select signal (c_1) is set. When $[a_1 \ a_0] = [0 \ 0]$ during 1 - 2 ns, the first column select signal (c_0) is set. When $[a_1 \ a_0] = [1 \ 1]$ during 4 - 5 n, the last column select signal (c_3) is set.

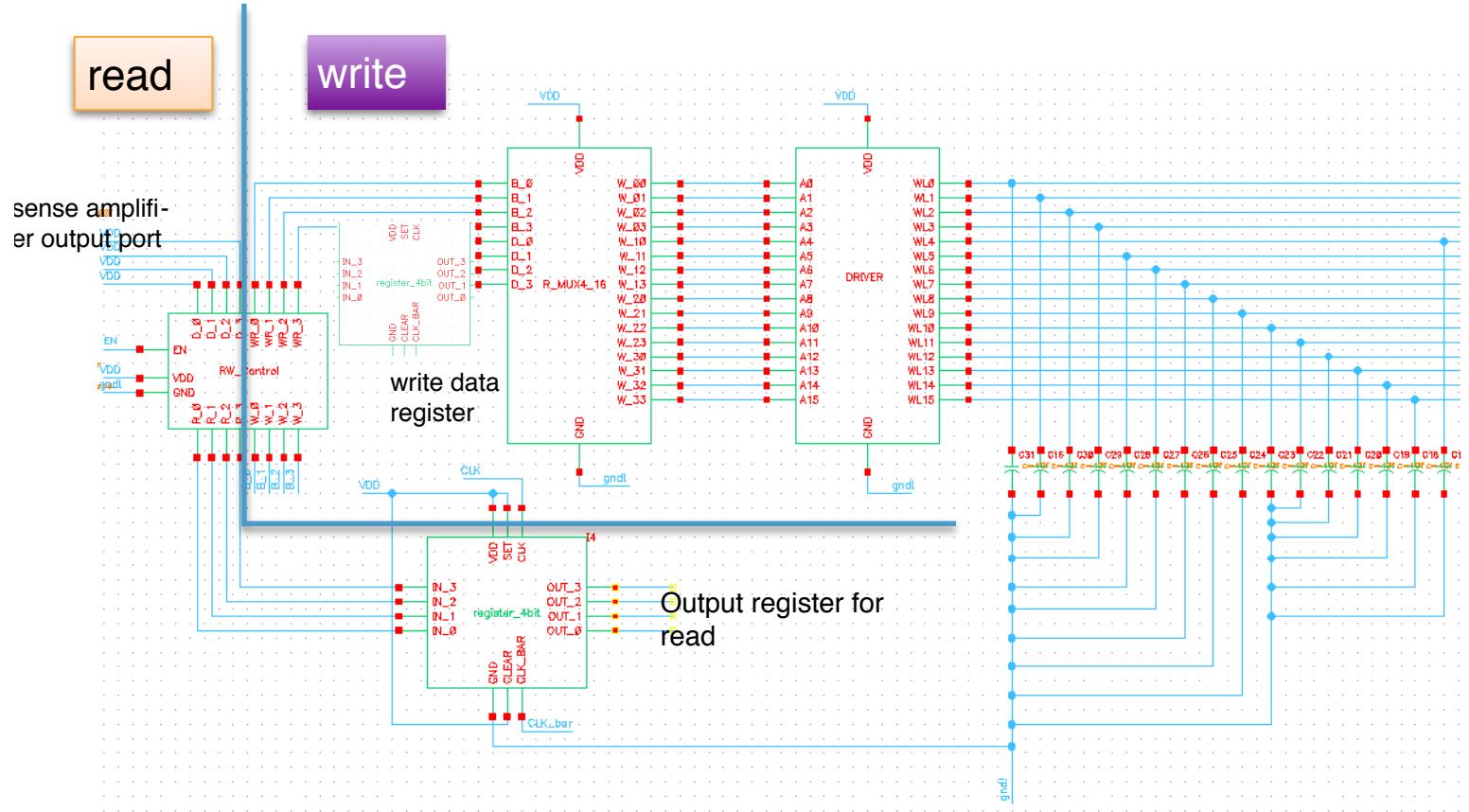
The $[d_0 \ d_1 \ d_2 \ d_3]$ are the output of MUX. The input of every column is $[\text{column_0}, \text{column_1}, \text{column_2}, \text{column_3}] = [0.5 \ 0.6 \ 0.75 \ 1] \text{ V}$

Then we can see:

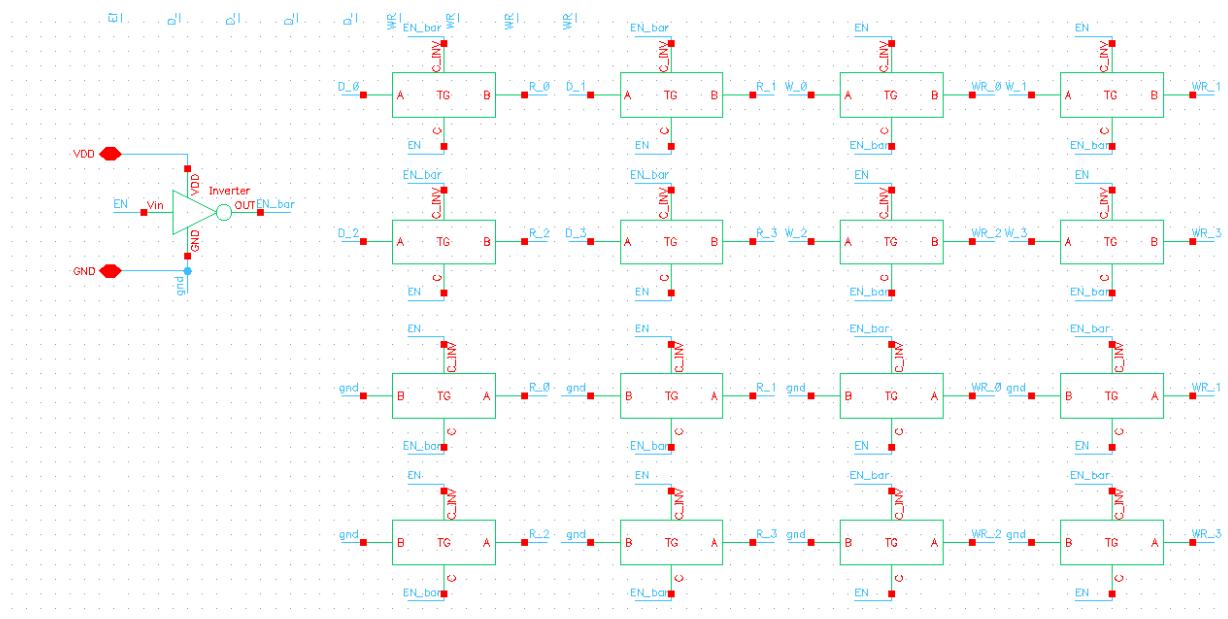
- During 0 - 1ns, the column 1 is selected. So the output should be 600mV. It is right.
- During 1 - 2ns, the column 0 is selected. So the output should be 500mV. It is right.
- During 2 - 3ns, the column 1 is selected. So the output should be 600mV. It is right.
- During 3 - 4ns, the column 0 is selected. So the output should be 500mV. It is right.
- During 4 - 5ns, the column 3 is selected. So the output should be 1V. It is right.

PROBLEM 3: WRITE CIRCUIT

1. Overall Cadence Schematic of Write circuitry



1.1 The RW_Control device (Read and write control)



For this part, we use the Transmission gate to control whether we want to read or write with a input **enable**, when enable =1, it will read. When enable = 0, it will write.

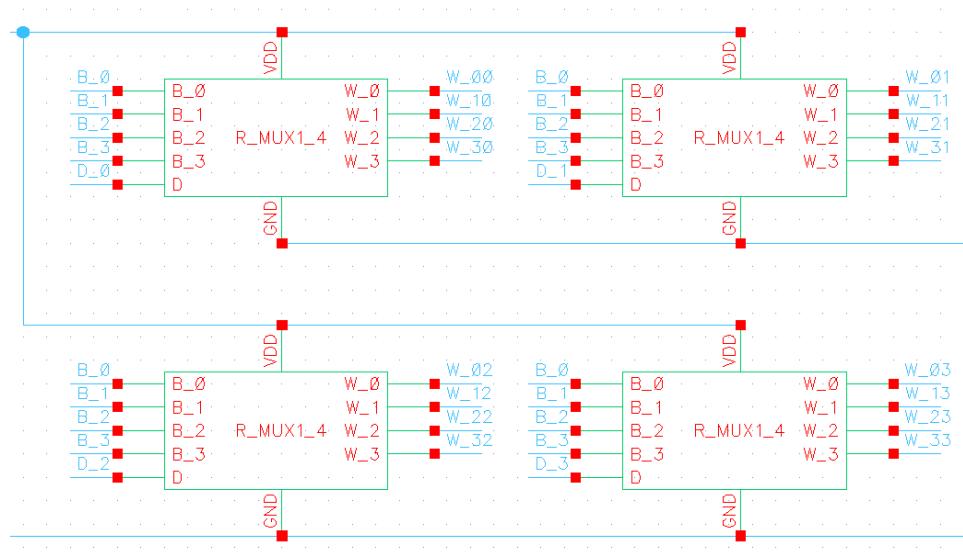
That means, when it is read state, the output of sense amplifier will connect to the output register of read. And when it is write state, the column select signal for choosing column will pass to the next level.

1.2 About reverse MUX

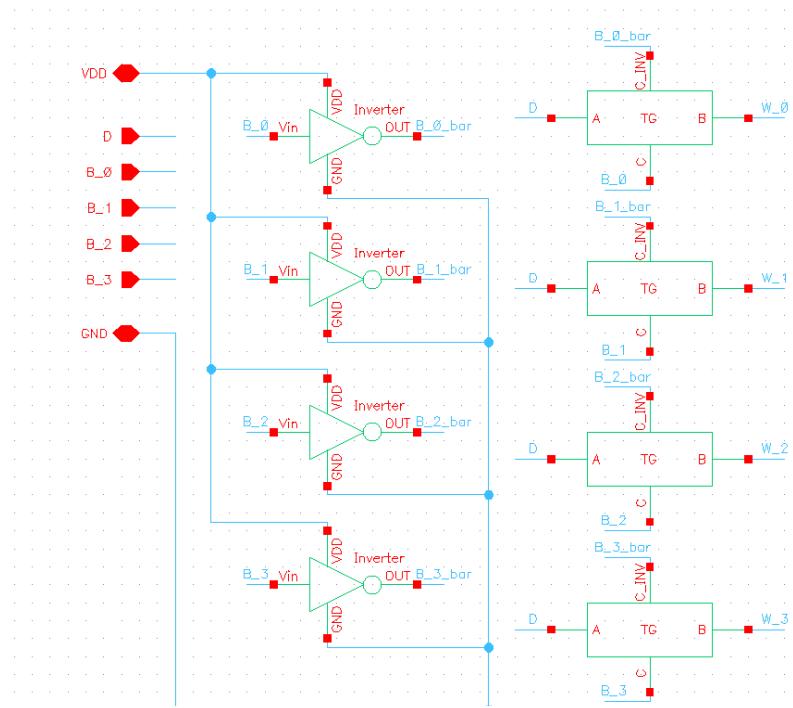
The reverse MUX is designed for the write path. It will pass the input data to bit line.

Why we do not use the same MUX device of read circuit?

Because the Transmission gate has the direction in Cadence. If the transmission gate is used for inverse direction, the output of TG can not achieve Vdd in cadence. So we use the reverse MUX to achieve that the output can achieve VDD.



Internal of R_MUX_4_16



Internal of R_MUX_1_4

We should input our write input data to all the 4_bit_MUX. And the column select signal control signal will judge which column bit line the data can pass.

In the R_MUX_1_4 , we can see that D represents the data (Input data [d3 d2 d1 d0]) and [B_3 B_2 B_1 B_0] represents the control signal (column select signal).

So the logic is that :

```

OUT_column_0 = data & ( column select signal _0 )
OUT1_column_1 = data & ( column select signal _1 )
OUT2_column_2 = data & ( column select signal _2 )
OUT3_column_3 = data & ( column select signal _3 )

```

And when the column select signal has not come, we should hold the value of bit line. So we the path should be blocked. So, can not connect to the GND.

2. Testing strategy

2.1 How can I verify my write circuit?

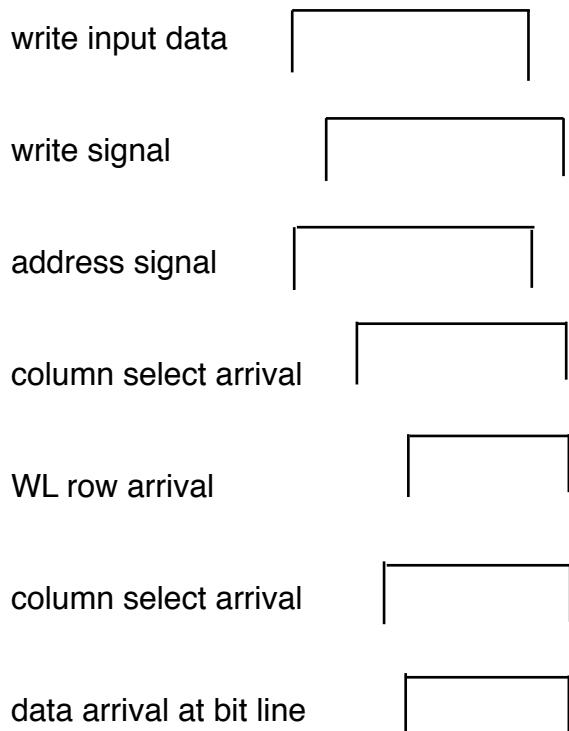
We will set the period of enable signal $T = 4 * T_{clk}$. And change the value of bit line column by column to see whether the right column of output of circuit is set when the positive clock and column select signal is set. (The output of write circuit is connected to bit line)

2.2 Which delay in write circuit is important to ensure proper write operation?

Delay from Bit line change to the negative edge of write signal.

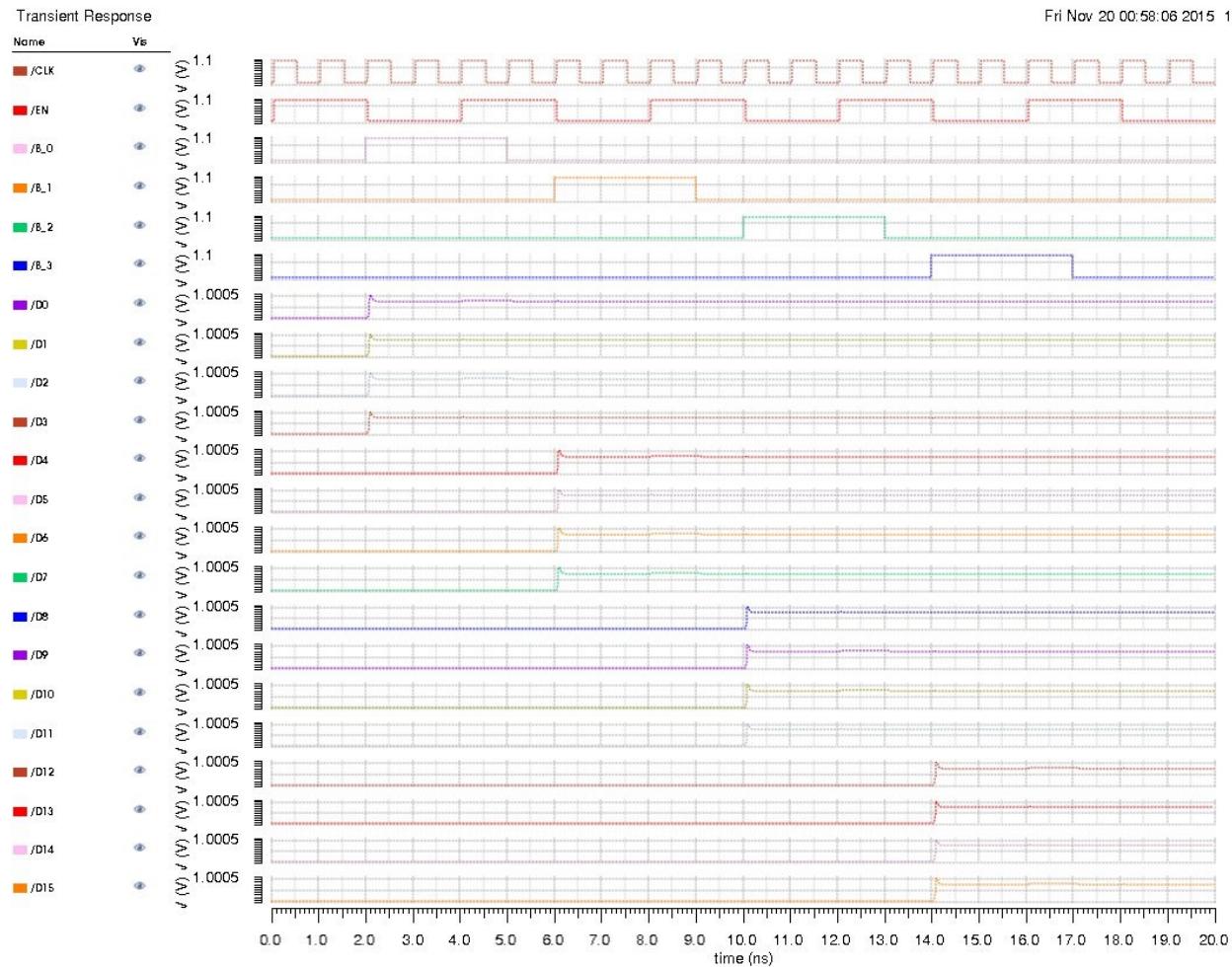
Because this period is the true period when the bit line is written to the memory cell. If this period is small. The data can not be written to the circuit.

2.3 The global timing requirement for writing circuit



So the timing requirement is that the time between the write signal to data arrival at bit line can not be very large. Also, the time between the write signal to WL row arrival can not be very large too. All these scenario may lead to the bad state that the value can not be written to the memory.

2.4 The waveform that we use to verify the operation of circuit



Analysis:

We can see that

During 2-4 ns, the enable = 0. It will write. And the column select signal _0 is set to VDD. So the column_0 will be set to VDD. Others will not change.

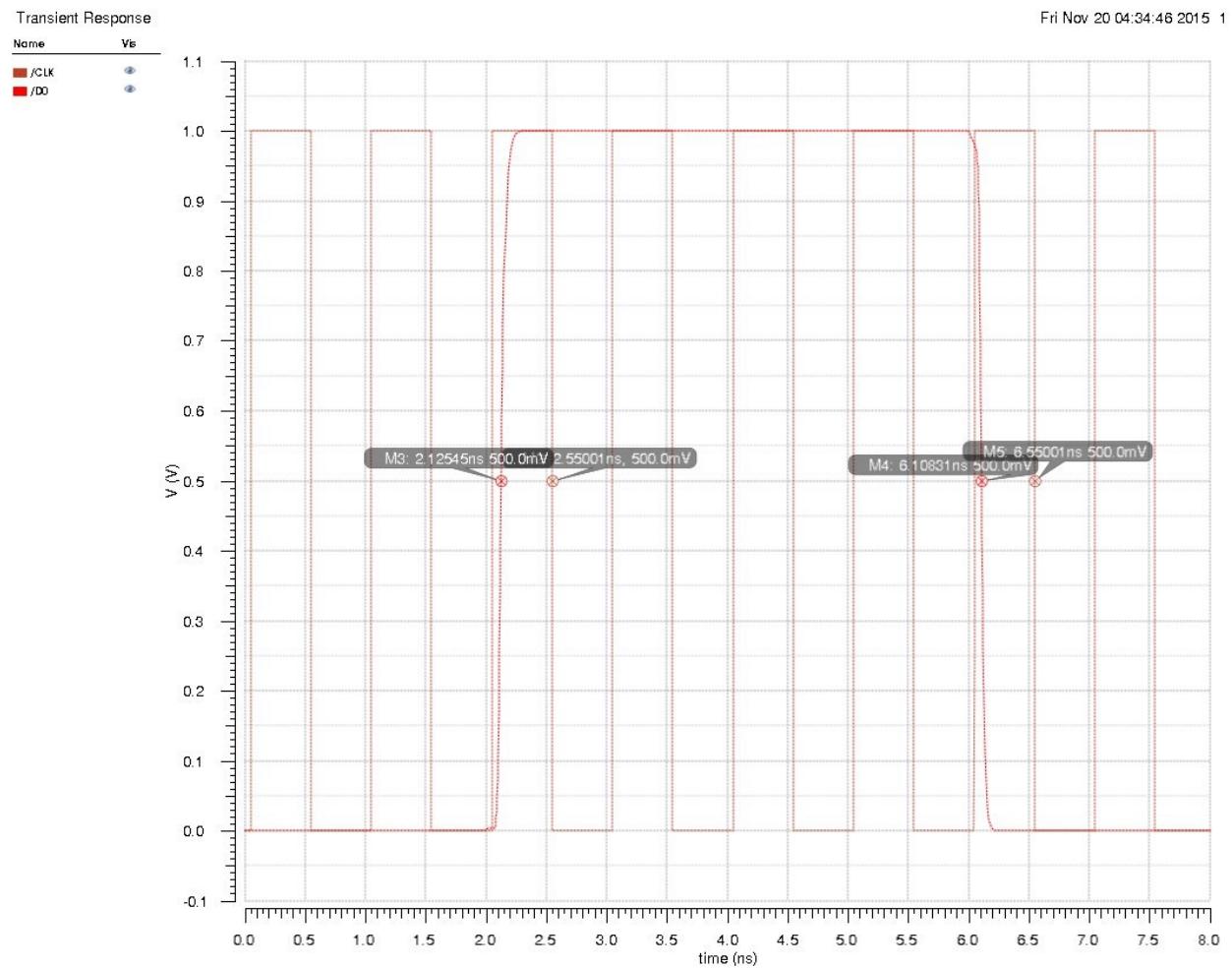
During 4-5 ns, the enable = 1. It will read, not write. Although the column select signal _0 is set to VDD. The output will not change because it is read state.

During 5-6 ns, the enable = 1. It will read. The output will not change because the column select signal _0 is not set and it is read period.

During 6-8 ns, the enable = 0. It will write. And the column select signal _1 is set to VDD. So the column_1 will be set to VDD. Others will not change.

In this way, we can see it operates right.

2.5 Report the delays that characterizes the write circuit



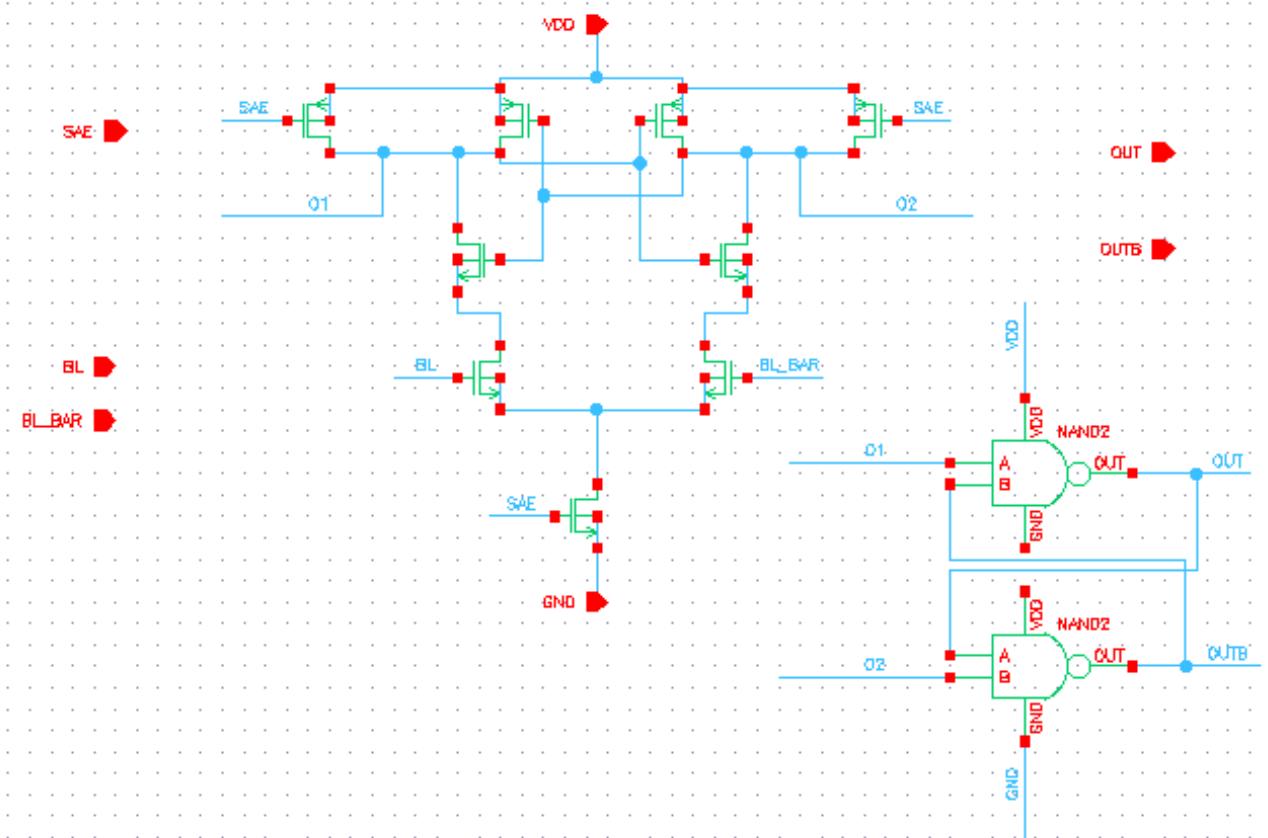
The delays that characterizes the write circuit:

$$\text{TPLH} = 2.55 - 2.1254 = 424.6 \text{ ps}$$

$$\text{TPHL} = 6.5 - 6.10831 = 391.7 \text{ ps}$$

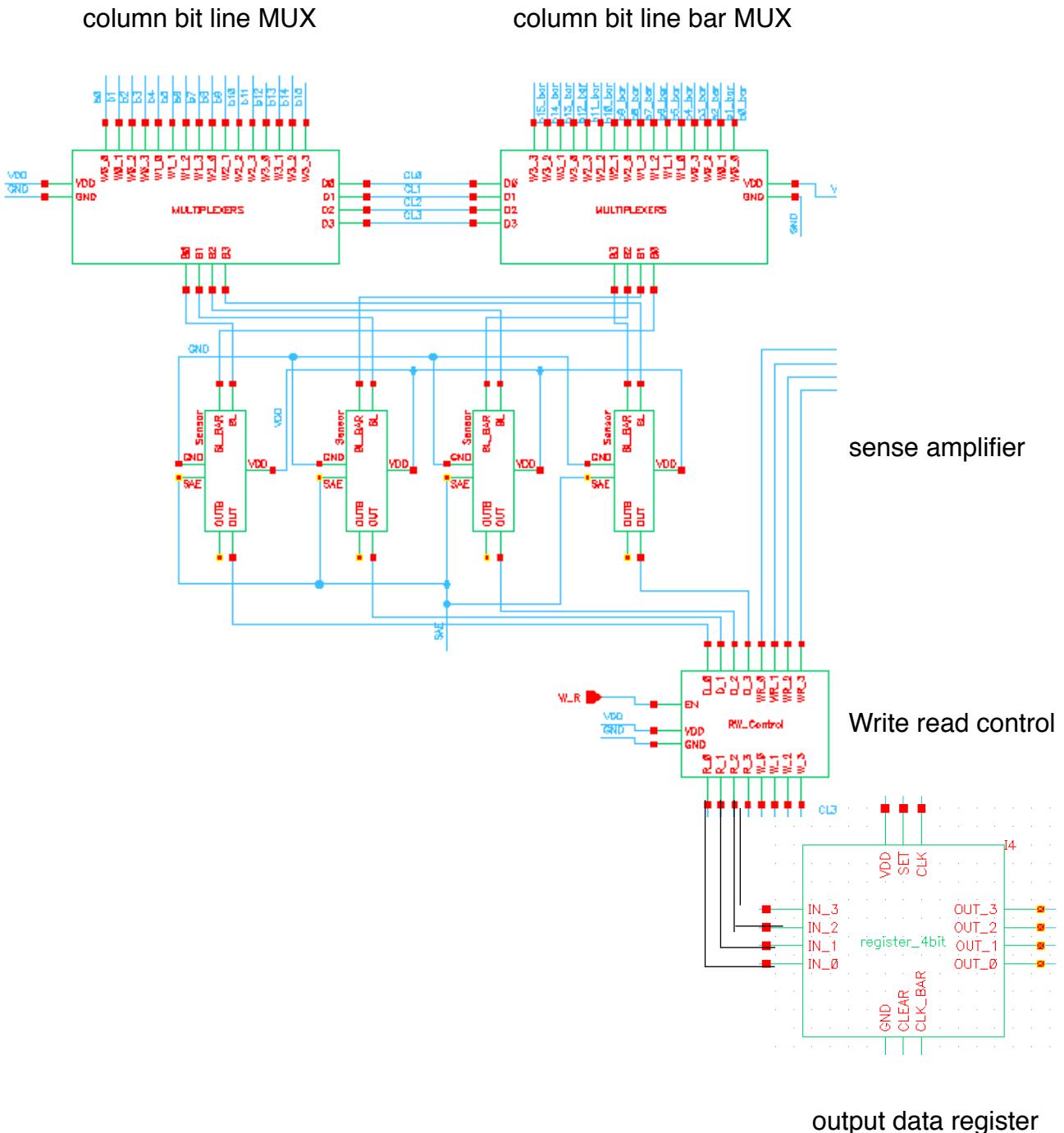
PROBLEM 4: READ CIRCUITS

1. Schematic of sense amplifier



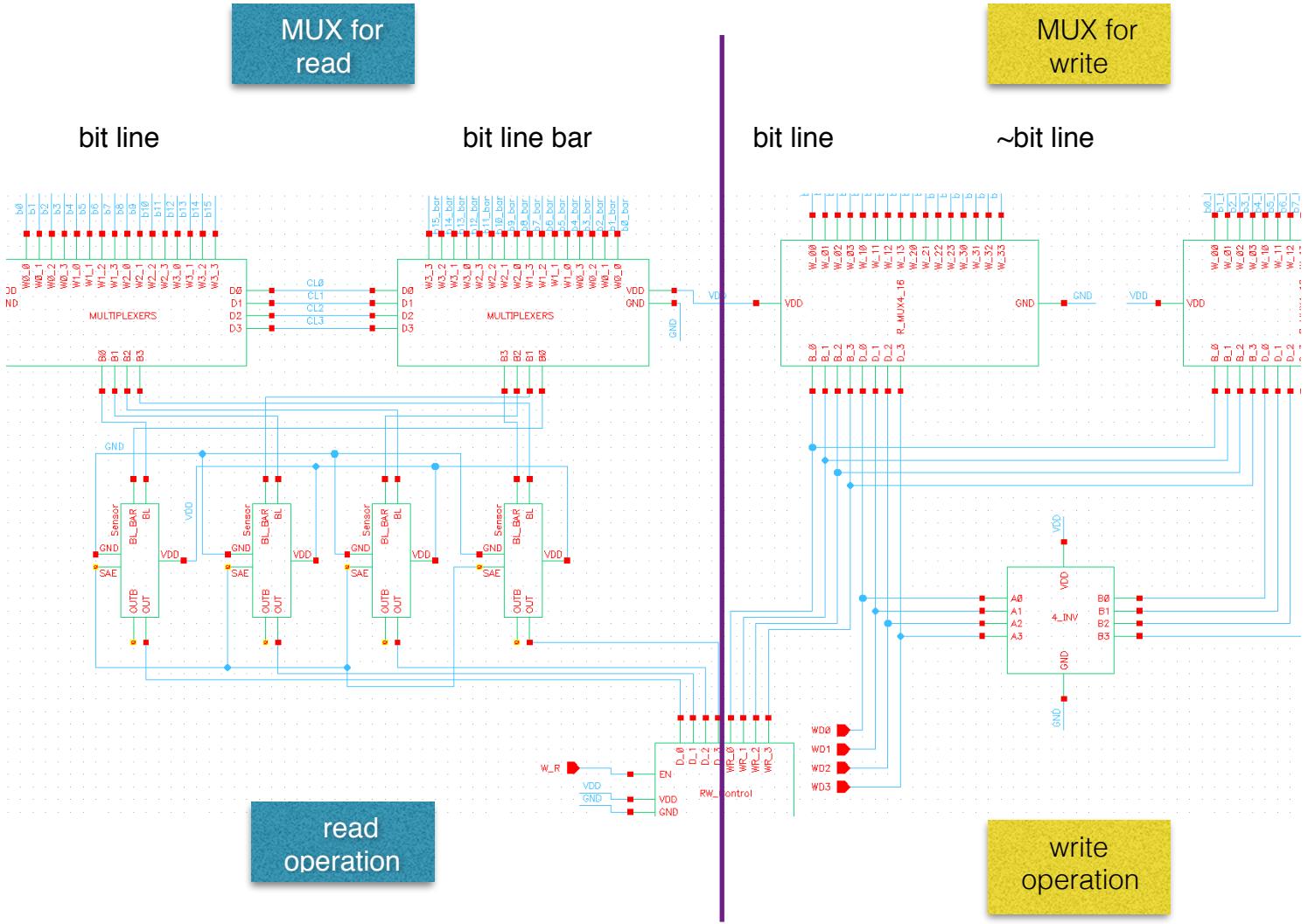
The sense amplifier is to amplify the signal and this is the schematic. The OUT will connect to the data register output. The input is Bit line and bit line bar.

2. Schematic of read circuit

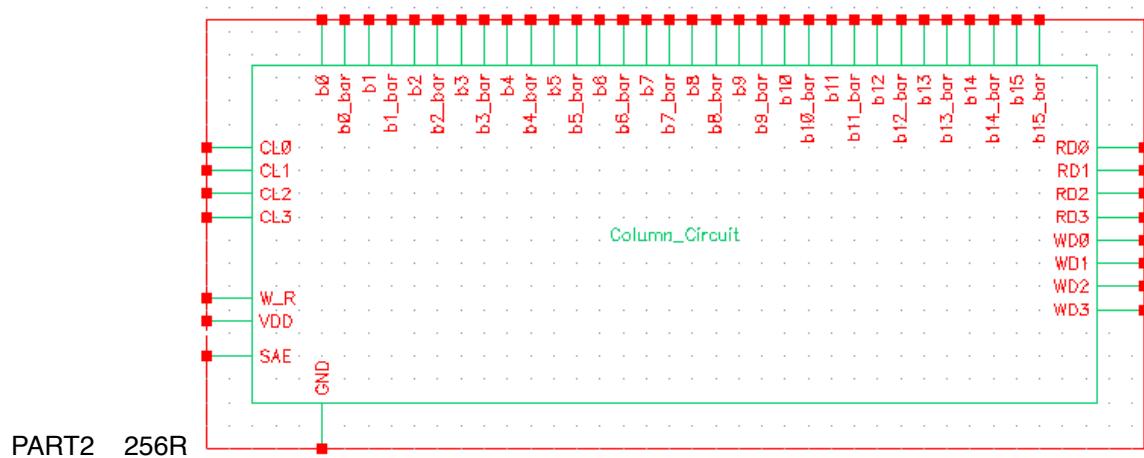


The CL0 CL1 CL2 CL3 is the column select signal (output of column decoder). And when one column select signal is chosen, the corresponding column value of bit line will pass to sense amplifier. Then, the RW_control will chose the model of read or write. If it is read model, the value can pass. Finally, pass to the data register, which will store the output value.

3. The integration of write and read circuit



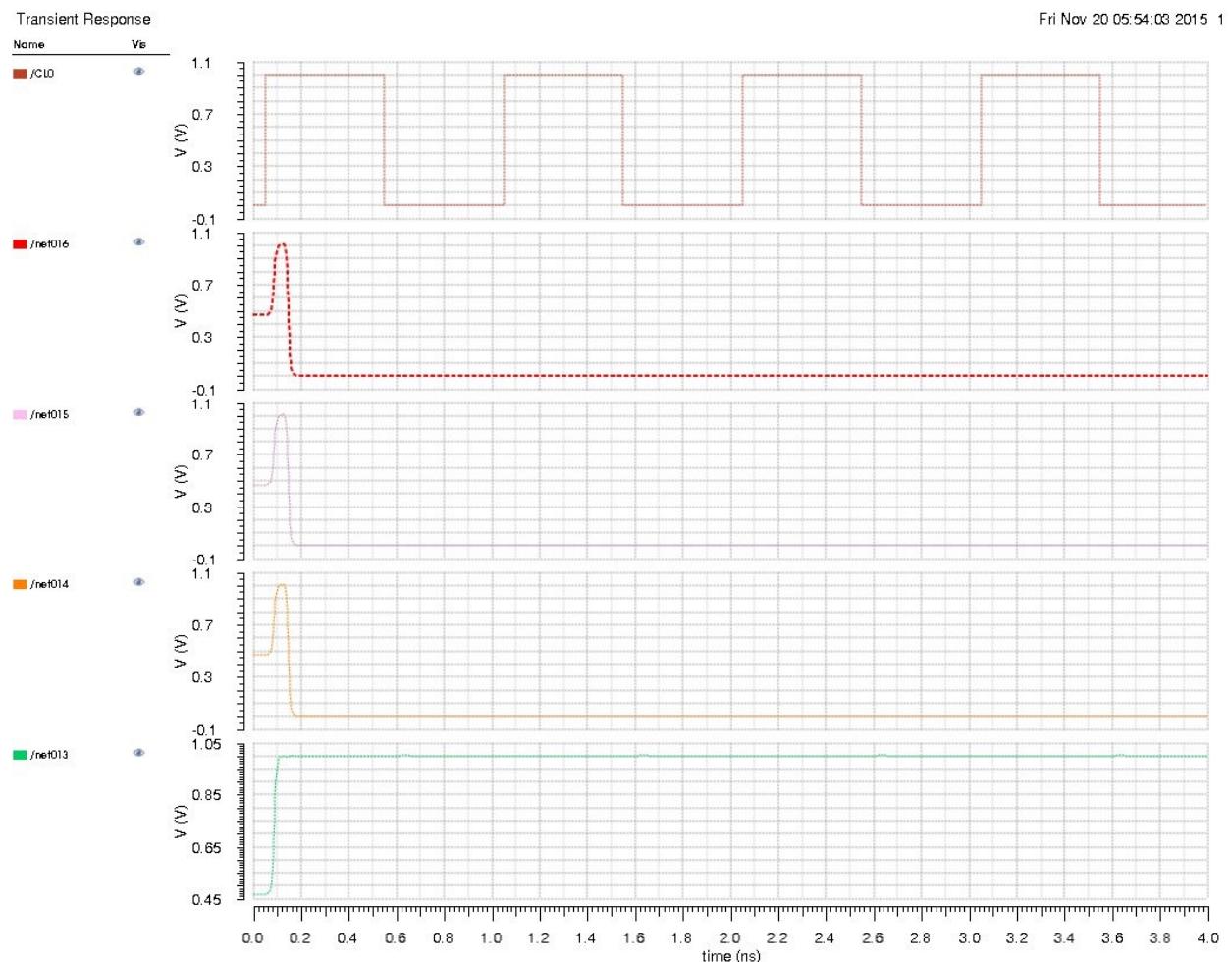
The symbol:



2. Testing the function of read circuit

2.1 Verifying the circuit and show the waveform

We apply the VDD to column select signal 0 and gnd to other. That means we choose the first column bit line.



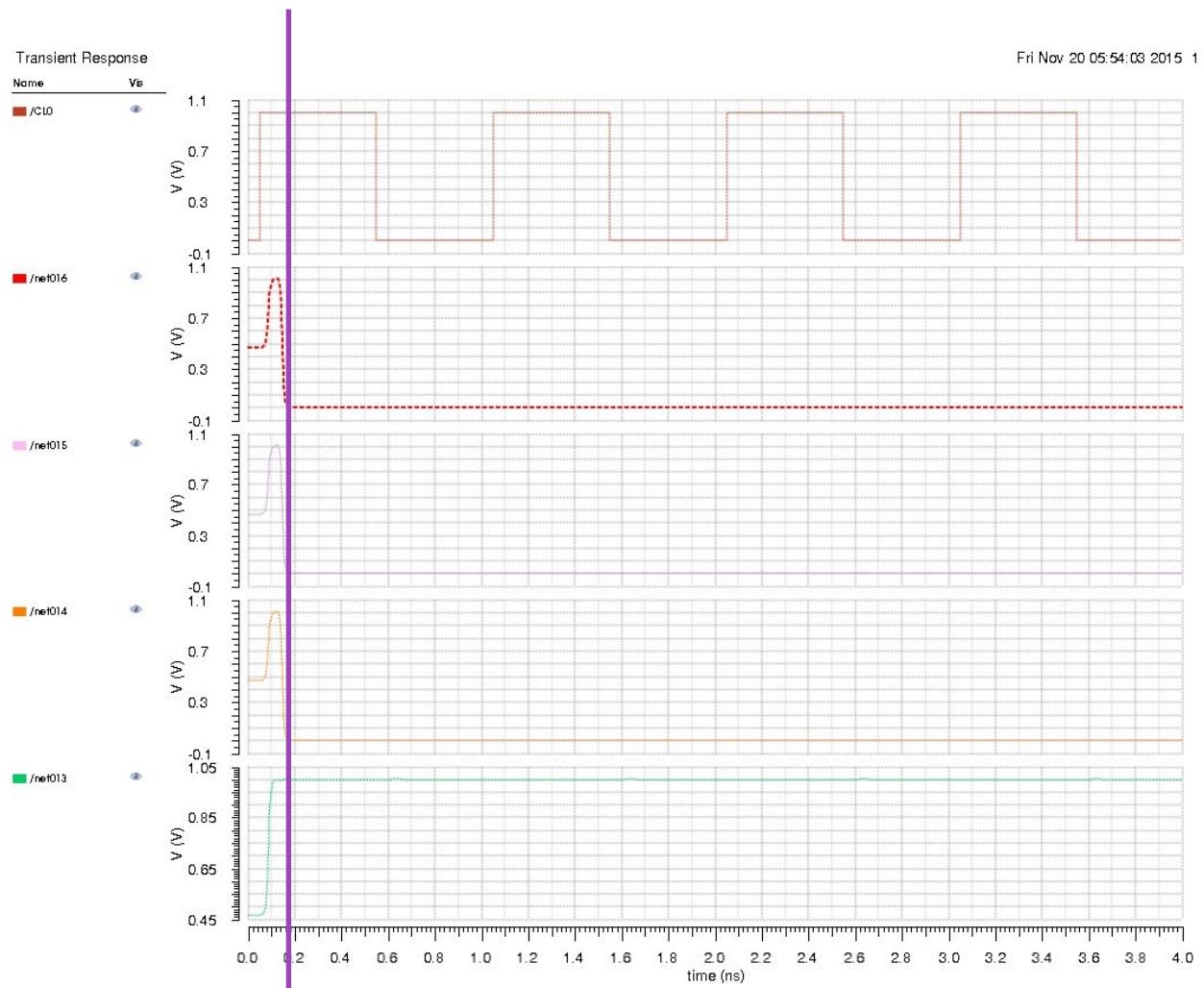
As we can see in the picture, when column select signal 0 is chosen. Only the first column is chosen. And we apply the

$[\text{bit_line_3} \text{ bit_line_2} \text{ bit_line_1} \text{ bit_line_0}] = [900\text{m} \text{ } 900\text{m} \text{ } 900\text{m} \text{ } 1] \text{ V}$
and $[\sim\text{bit_line_3} \text{ } \sim\text{bit_line_2} \text{ } \sim\text{bit_line_1} \text{ } \sim\text{bit_line_0}] = [1 \text{ } 1 \text{ } 1 \text{ } 900\text{m}] \text{ V}$

Then, we can see from picture, they are the output of sense amplifier. Only the data_0 is set to 1. Others are 0.

2.2 Characteristic delay

The most important delay is the from the change from output of amplifier to the stable state of output.

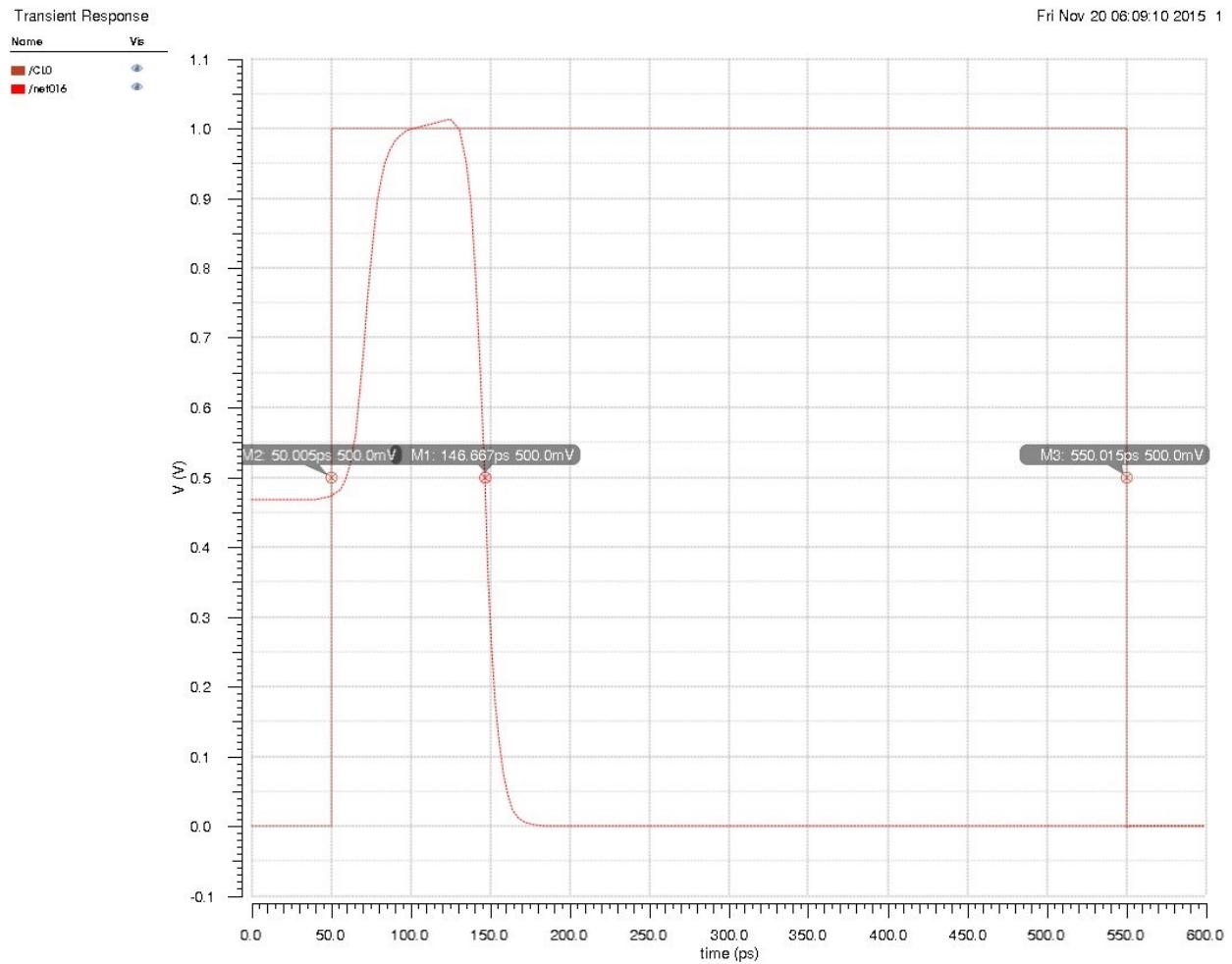


As we can see from picture, the mismatch part is the important delay because when it is a negative edge of CLK, the register will pick the output value of sense amplifier. So, if the delay is too large, the register may get a wrong value.

2.3 Time requirement

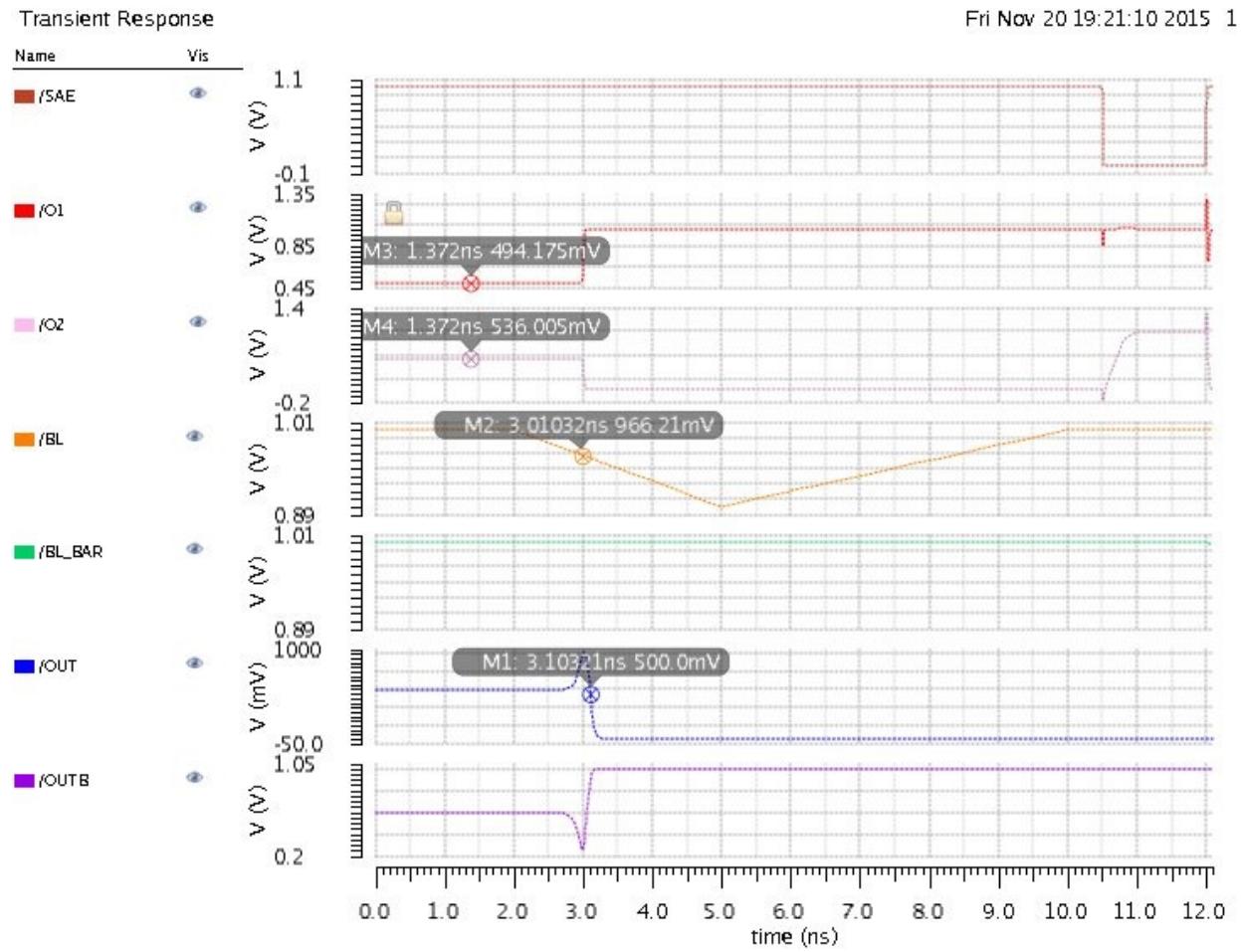
1. When the column select signal goes high, the 16 column bit line value will pass to the MUX and only pass 4 bit value. Then, they will go to the sense amplifier. SAE signal = clk & read. So, when the clk and write all come, the sense amplifier is activated. But until the column is selected and the right bit line value arrive, the sense amplifier output is what I want.

3. Testing delay that characterize the read circuit.



We can see the delay is $146.667 - 50 = 96.6670$ ps.

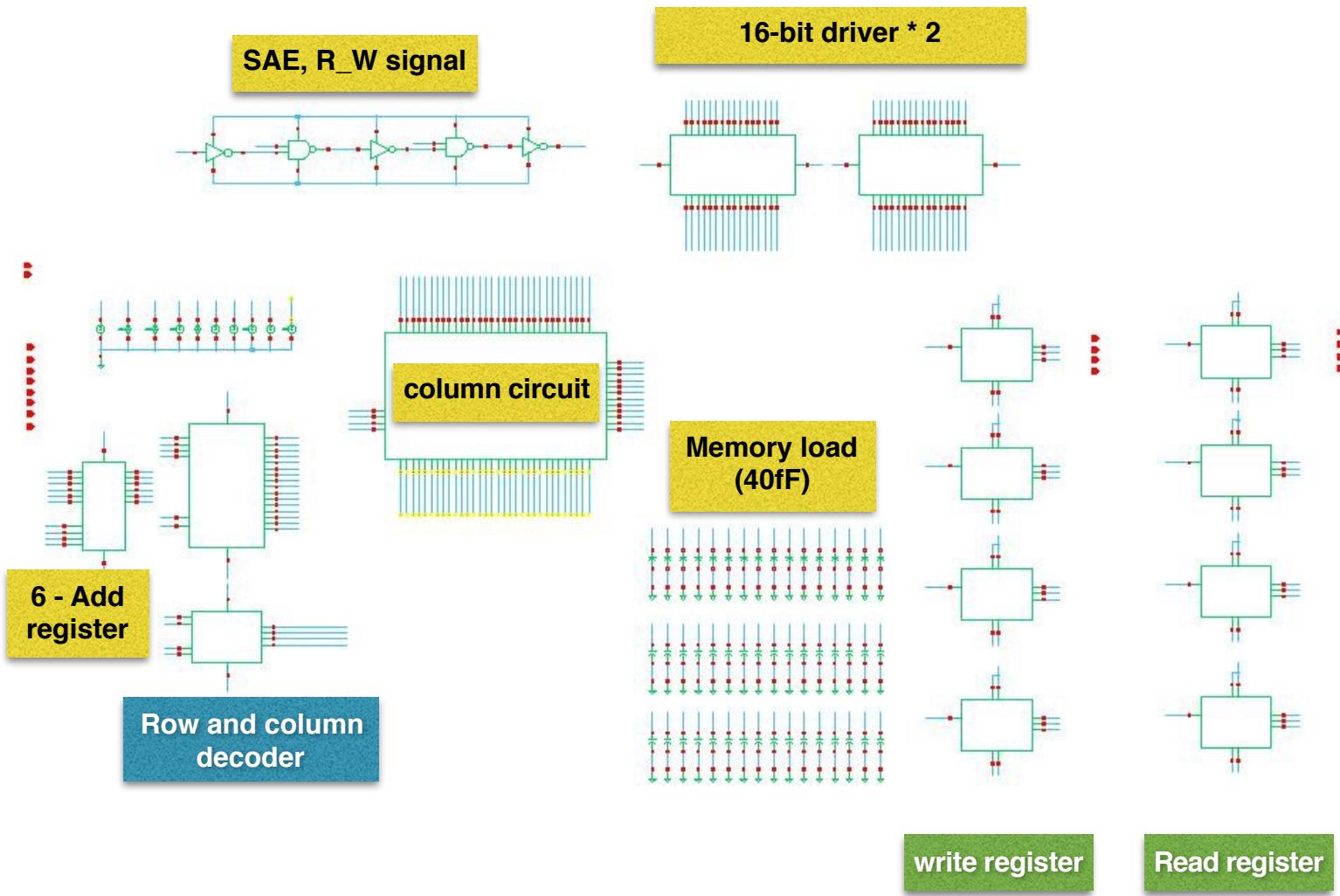
4. Testing the largest tolerance of sense amplifier



We can see that when we decrease the value of bit line, when the bit line decrease to 966.21mV, the sense amplifier can distinguish them. So the tolerance is 33.79 mV.

PROBLEM 5: Complete Peripheral

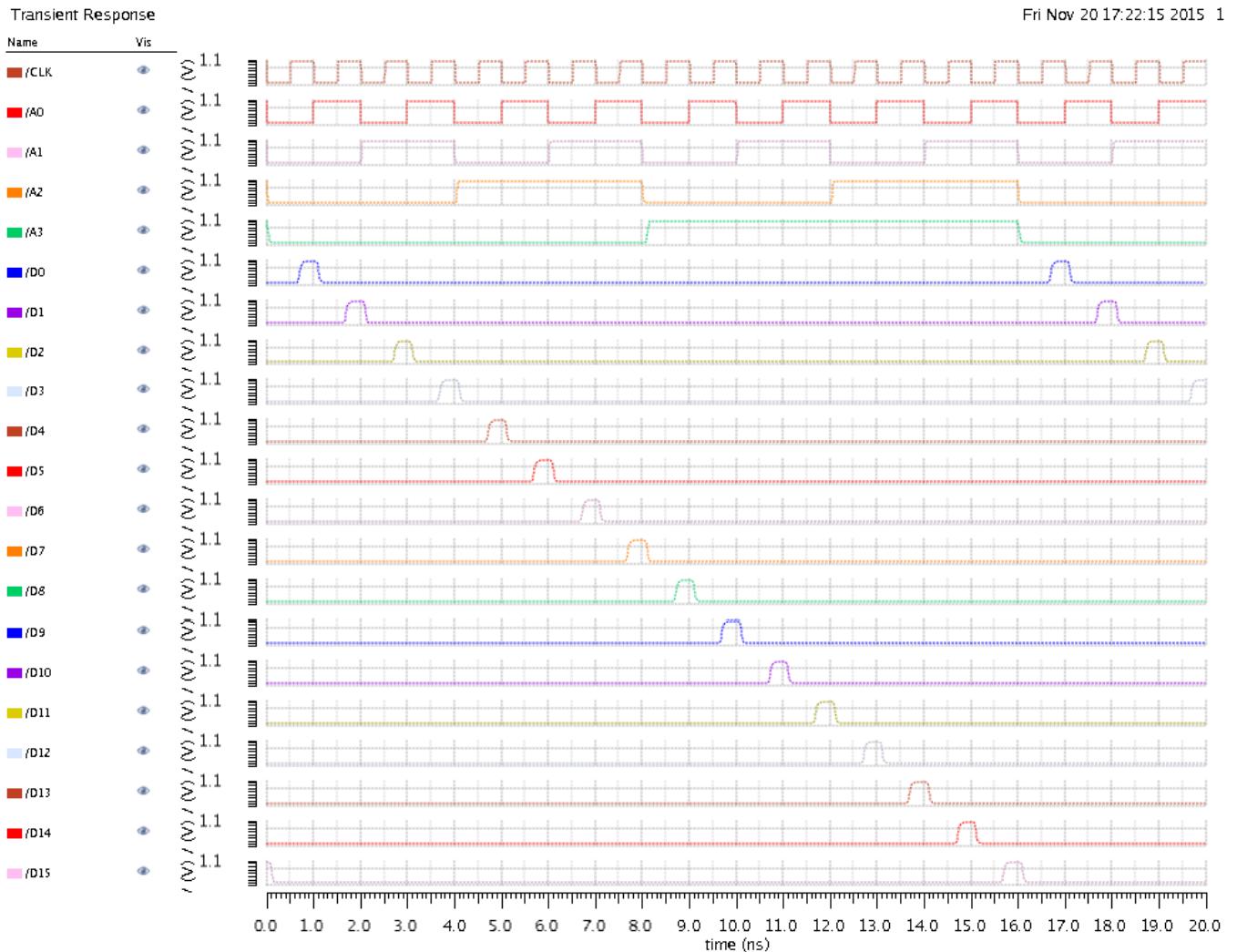
1. Overall schematic of peripheral



2. Testing path

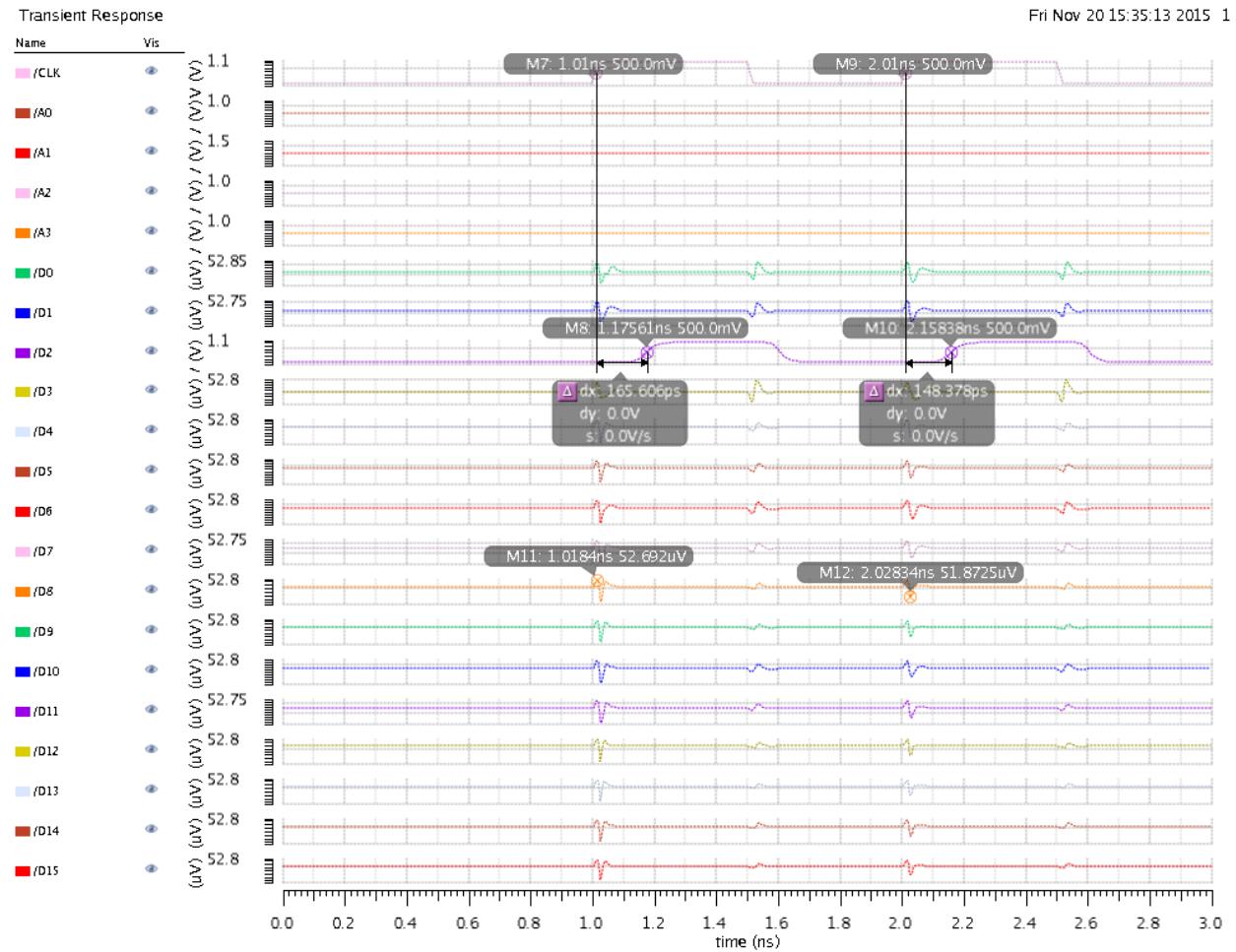
2.1 Path (1)

2.1.1 waveform to show the output of word line



As we can see the input of address propagate to the Word line.

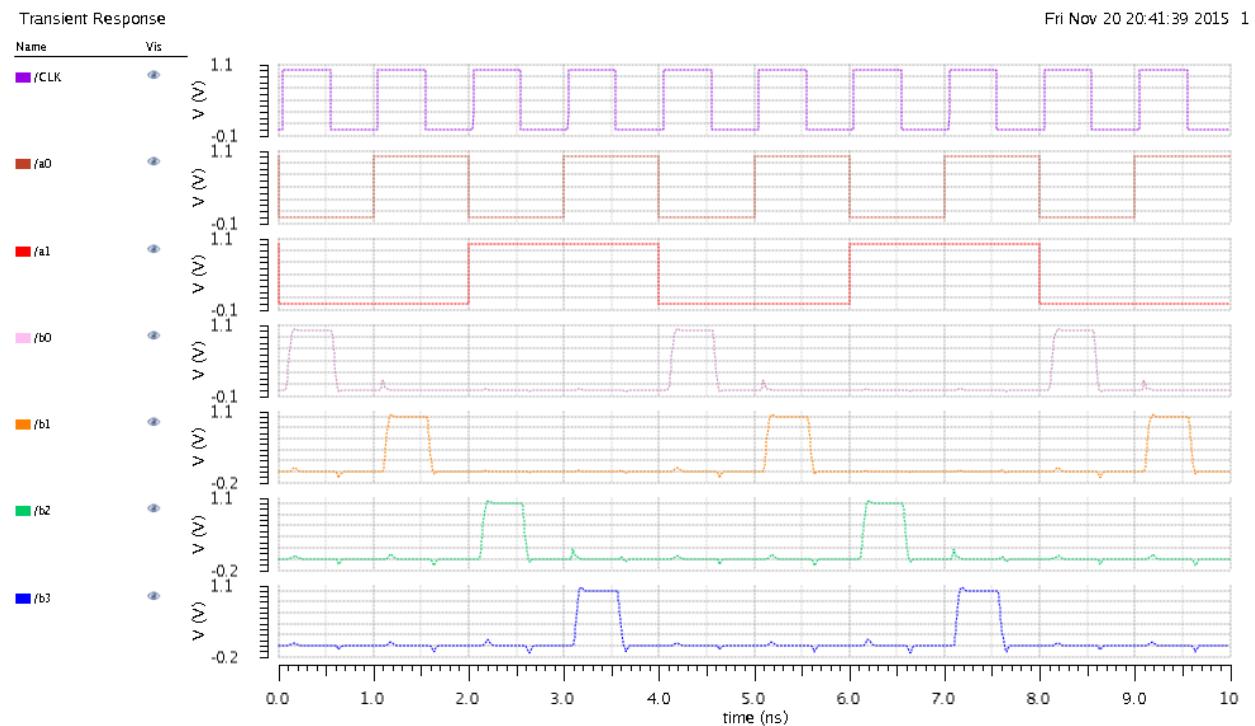
2.1.2 Testing delay from positive CLK to the word line.



The delay here is $dx = 165.6\text{ps}$ and $dx = 148.3\text{ps}$.

2.2 Path (2)

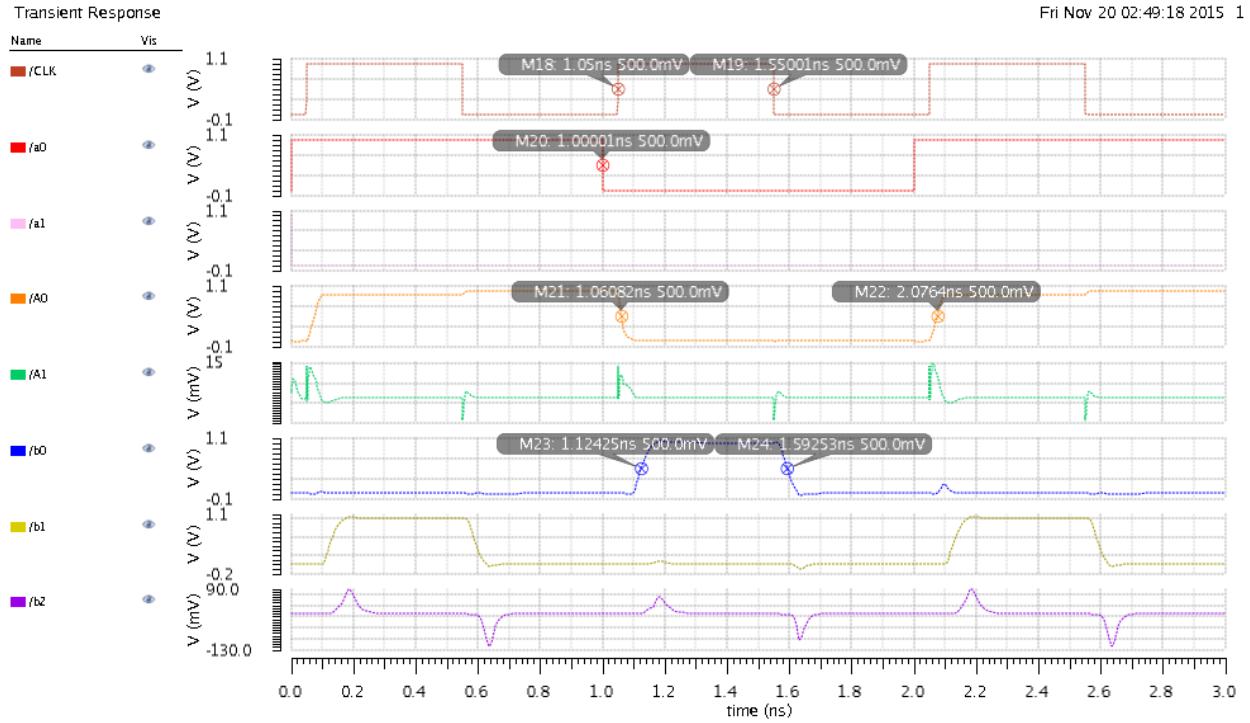
2.2.1 waveform to show the output of word line



Operation:

The address [a1 a0] propagate to the column select.

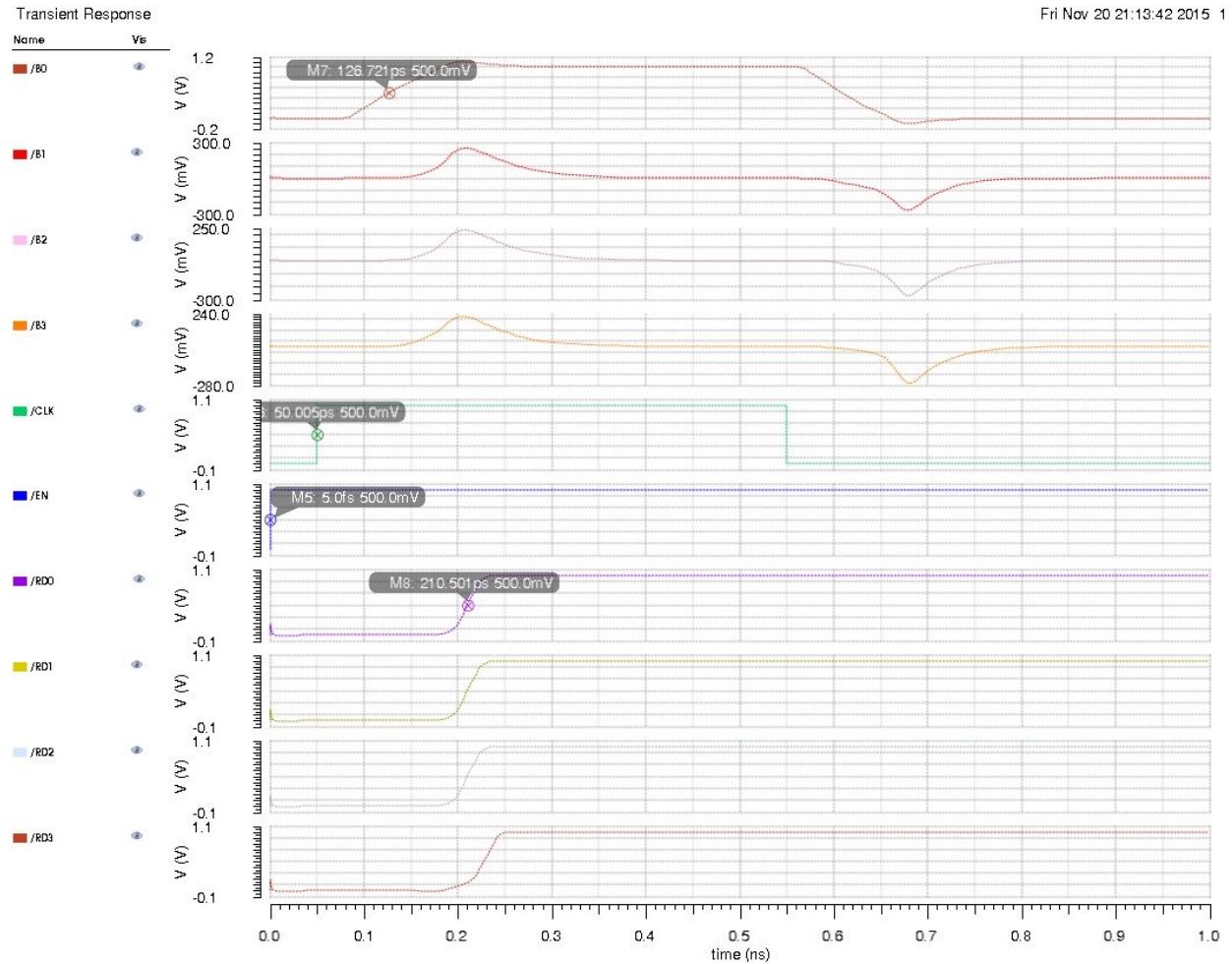
2.2.2 Testing delay from positive CLK to the column select signal.



Delay from write signal to the column select signal:

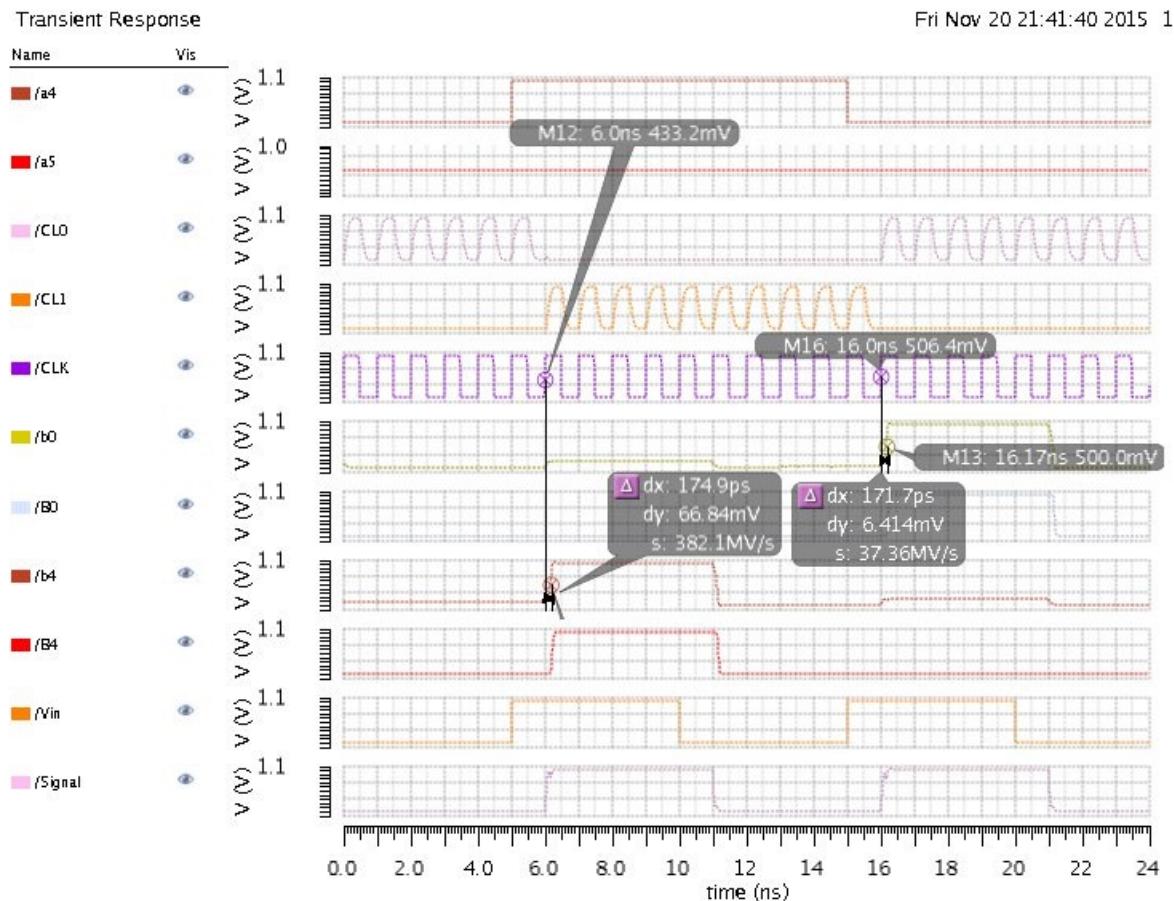
$$TPLH = 1.12425 - 1.05 = 74.2 \text{ ps}$$

2.3 Path (3) Testing whole path read delay (with column register and decoder) :



As we can see from picture, when the column select signal $[b_3 \ b_2 \ b_1 \ b_0] = [0 \ 0 \ 0 \ 1]$, which means the column 0 will be selected. And we apply the VDD to $[bit_line_3 \ bit_line_2 \ bit_line_1 \ bit_line_0] = [1 \ 1 \ 1 \ 1]$. And others to 0. We can see that the output of read register is $[1 \ 1 \ 1 \ 1]$. So, read successfully.

2.4 Path (3) Testing whole path write delay (with column register and decoder) :



Analysis:

The a4,a5 are the column address input. [CL3 CL2 CL1 CL0] are the column select signal (output of decoder). [b3 b2 b1 b0] are the output before the driver. [B3 B2 B1 B0] are the output to bit line (after driver). Vin is the input of data register for writing. Signal is the output of data register for writing.

As we can see that, during 6 - 11 ns, we write the VDD to column 1 and bit line will hold the value 1 we write if we do not write. So it will be 1 in this period. (B4)

As we can see that, during 11 - 16 ns, we write the GND to column and bit line will hold the value 0 we write if we do not write. So it will be 0 in this period. (B4)

As we can see that, during 16 - 21 ns, we write the VDD to column 0 and bit line will hold the value 1 we write if we do not write. So it will be 1 in this period. (B0)

As we can see that, during 21 - 24 ns, we write the GND to column 0 and bit line will hold the value 0 we write if we do not write. So it will be 0 in this period. (B0)

So we can see that when we write to column 1 the delay is 174.9 ps for whole writing circuit including the column select. when we write to column 0, the delay is 171.7ps.