PART-III: SRAM CELL AND ARRAY FOR 256-BIT SRAM REPORT

Group3

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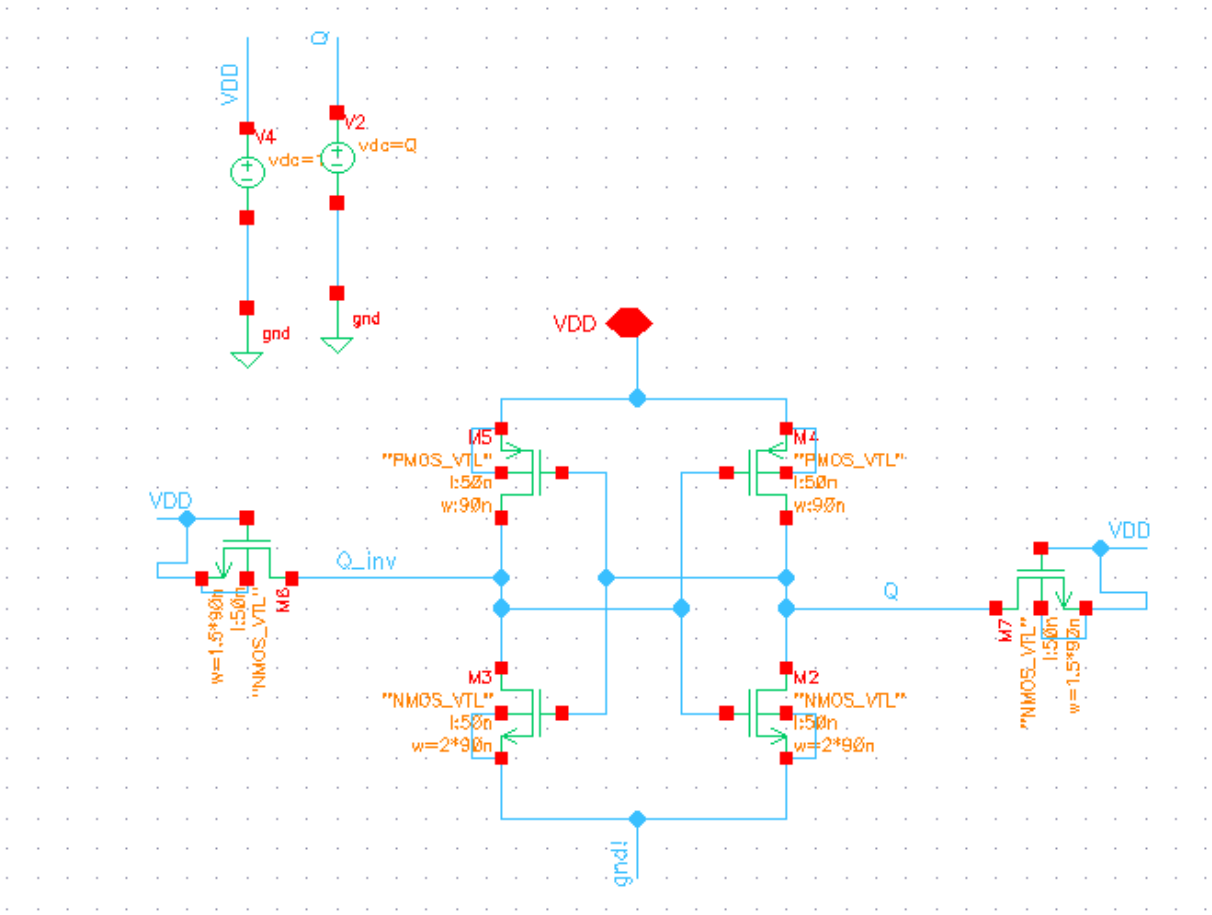
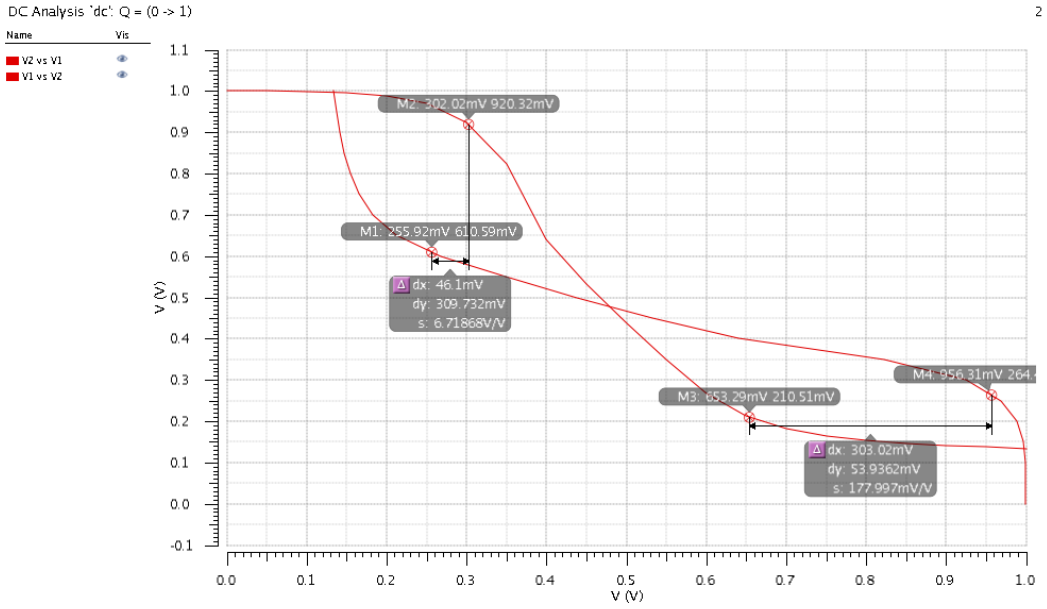
1.Cell-level results:

1.1 Read margin



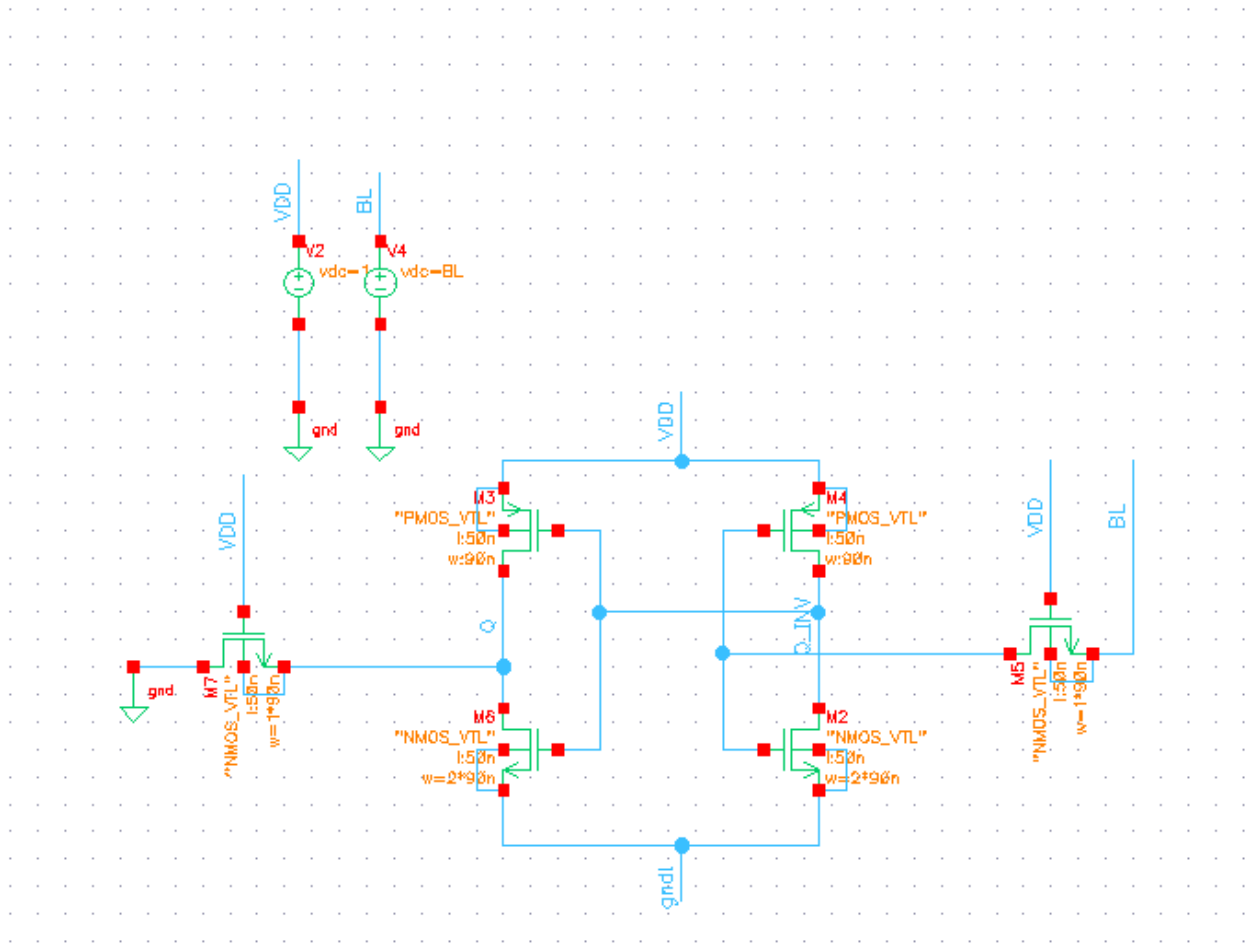
Test Schematic design for measuring Read Noise Margin



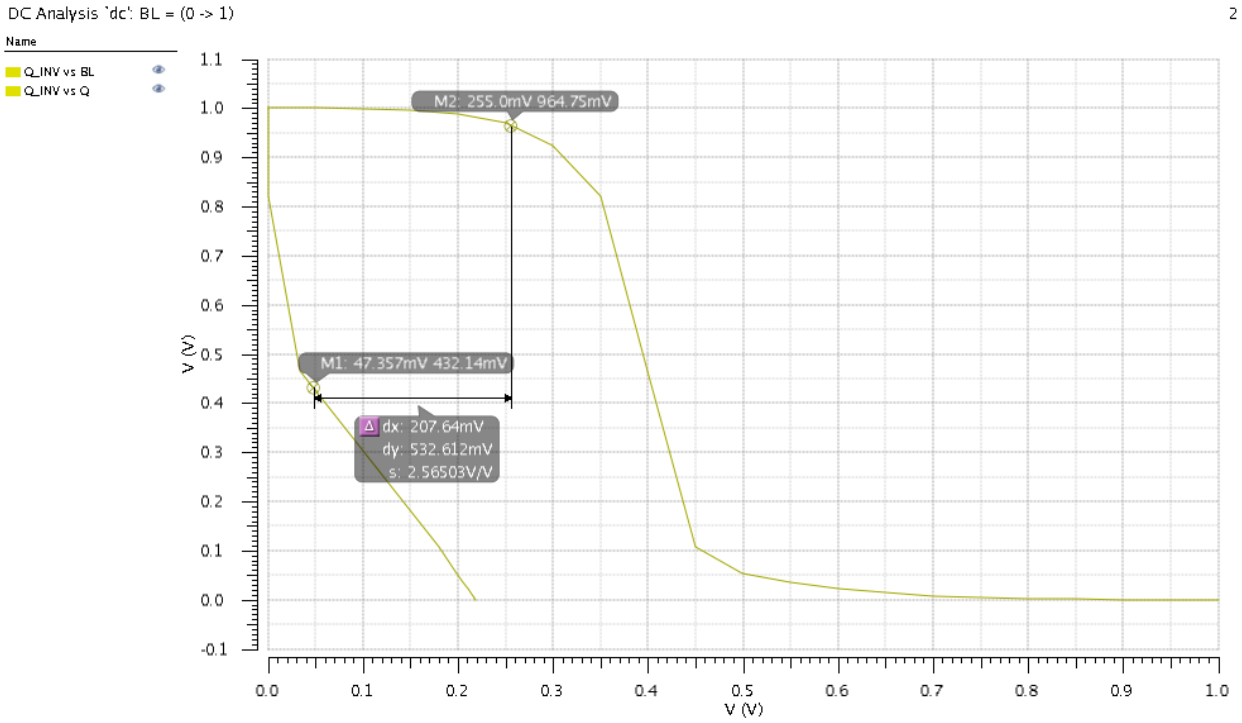
The Read Margin here is 309mV and 303mV, which are higher than 30% VDD.

1.2 Write margin

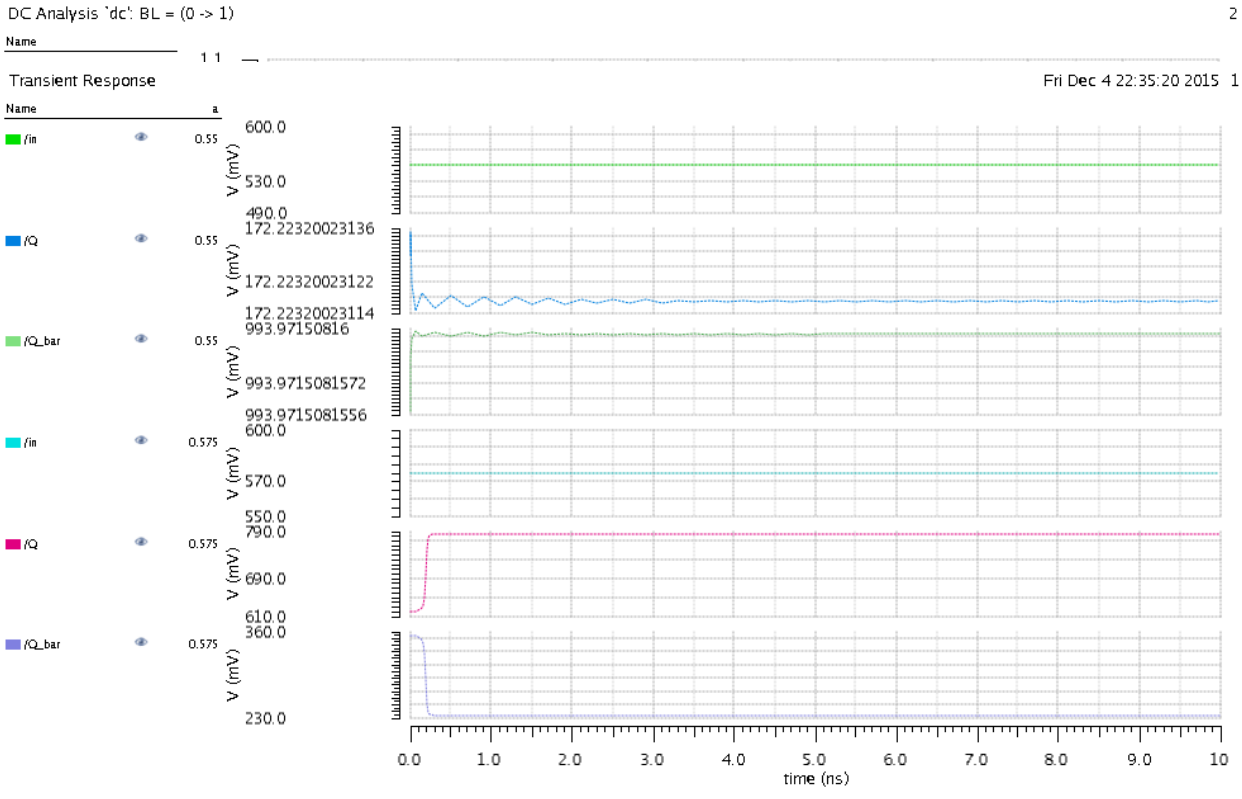
Keep W_P = 90nm; W_{access} = 90nm; W_{pd} = 180nm;



Test Schematic design for measuring Write Margin



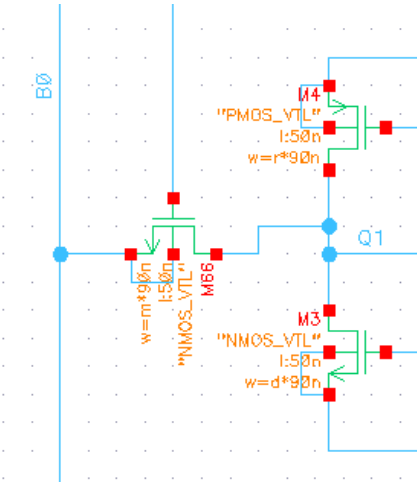
The DC analysis shows that the write margin is approximately 570mV, which is higher than 50% VDD.

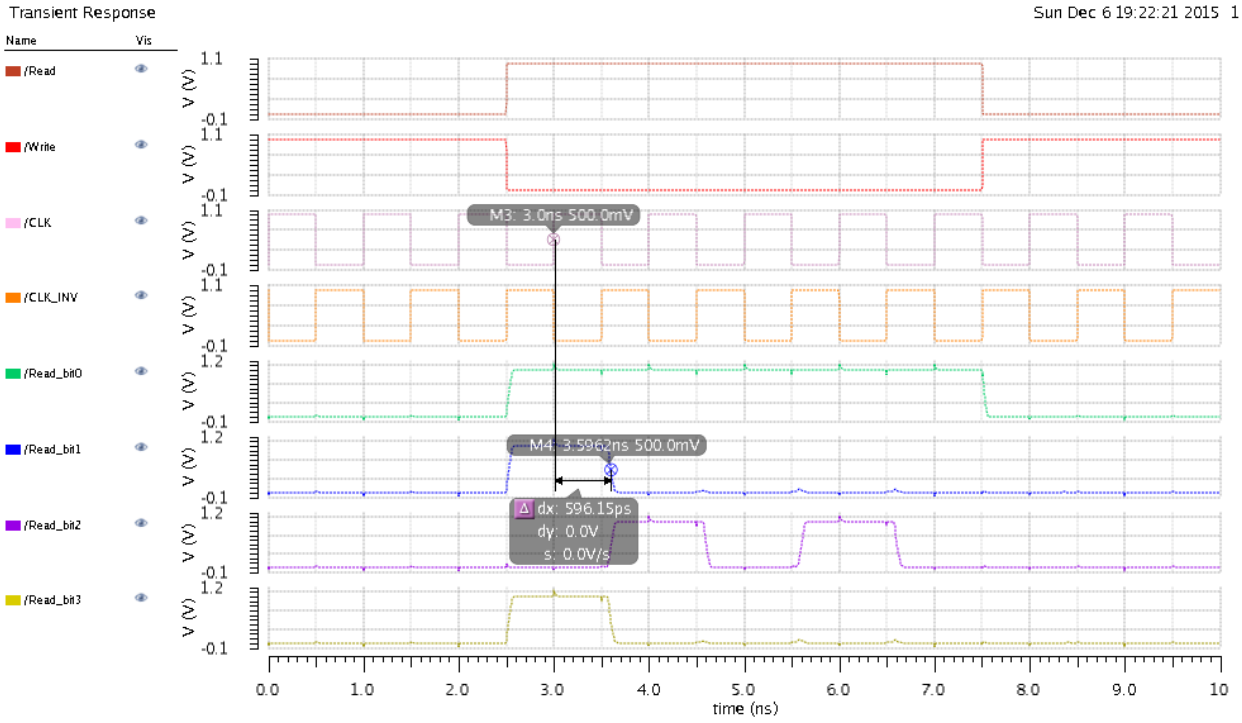


Tran Simulation for measuring Write Margin:
When we increase the input from 0 to VDD, we find that when Vin = 0.55. We can still write a 0. But when increasing it to 0.575, it can not write a 0. So our write margin is 0.55V.

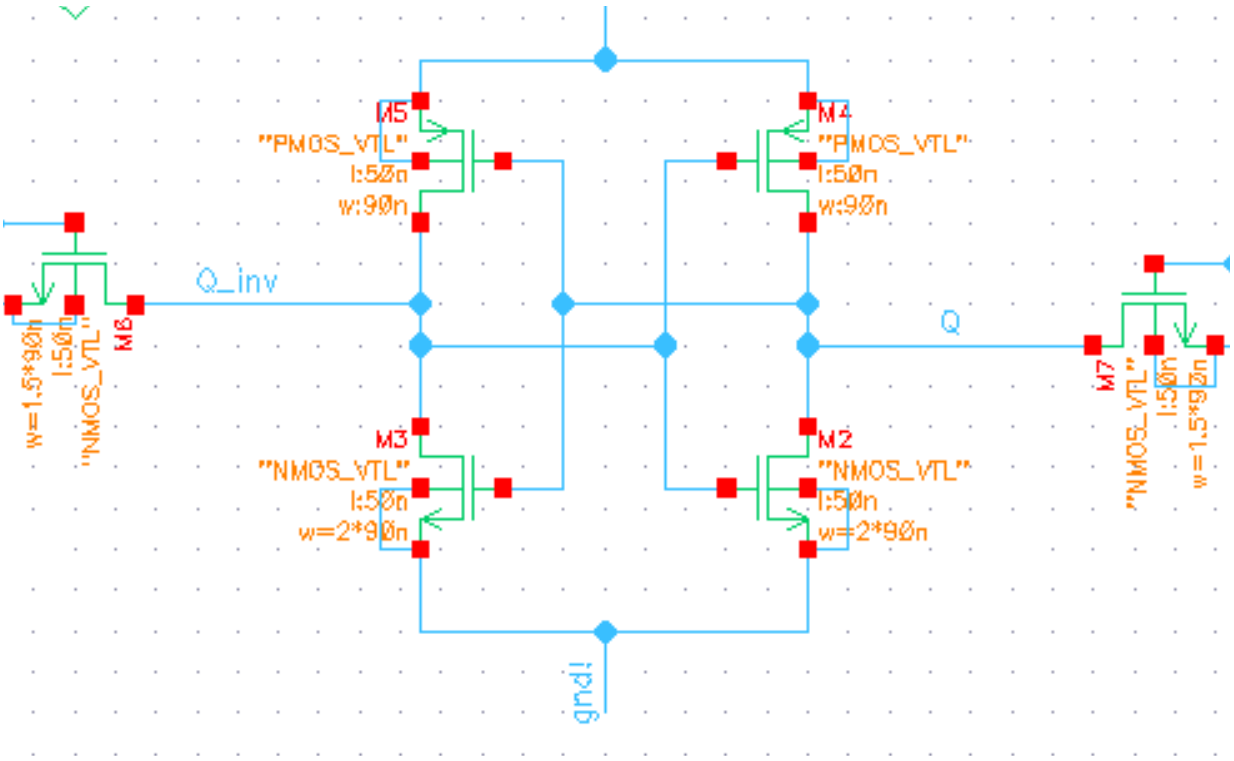
1.3. Access time measurements from Cadence simulation.

Taccess test:
Taccess = Cbit*Δbit/Iread
Here, in the test, the access time is the delay of Q1 and B0. So, we select this two point and get the result: Taccess = 596.15ps The read_bit signal is the output of sense amplifier

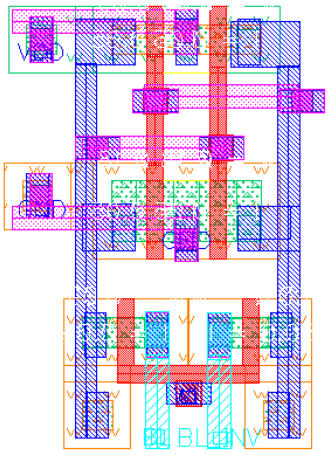




1.4. All sizes of the transistors in your 6T SRAM cell.
We set the Wpn:Waccess:Wpu= 2 : 1.5 : 1



1.5 Layout of the 6T cell with clean LVS and DRC reports.



While calculating the cell area, we did not take the subtract contact in to account, since for later SRAM design, all the PMOS (NMOS) will share this block.

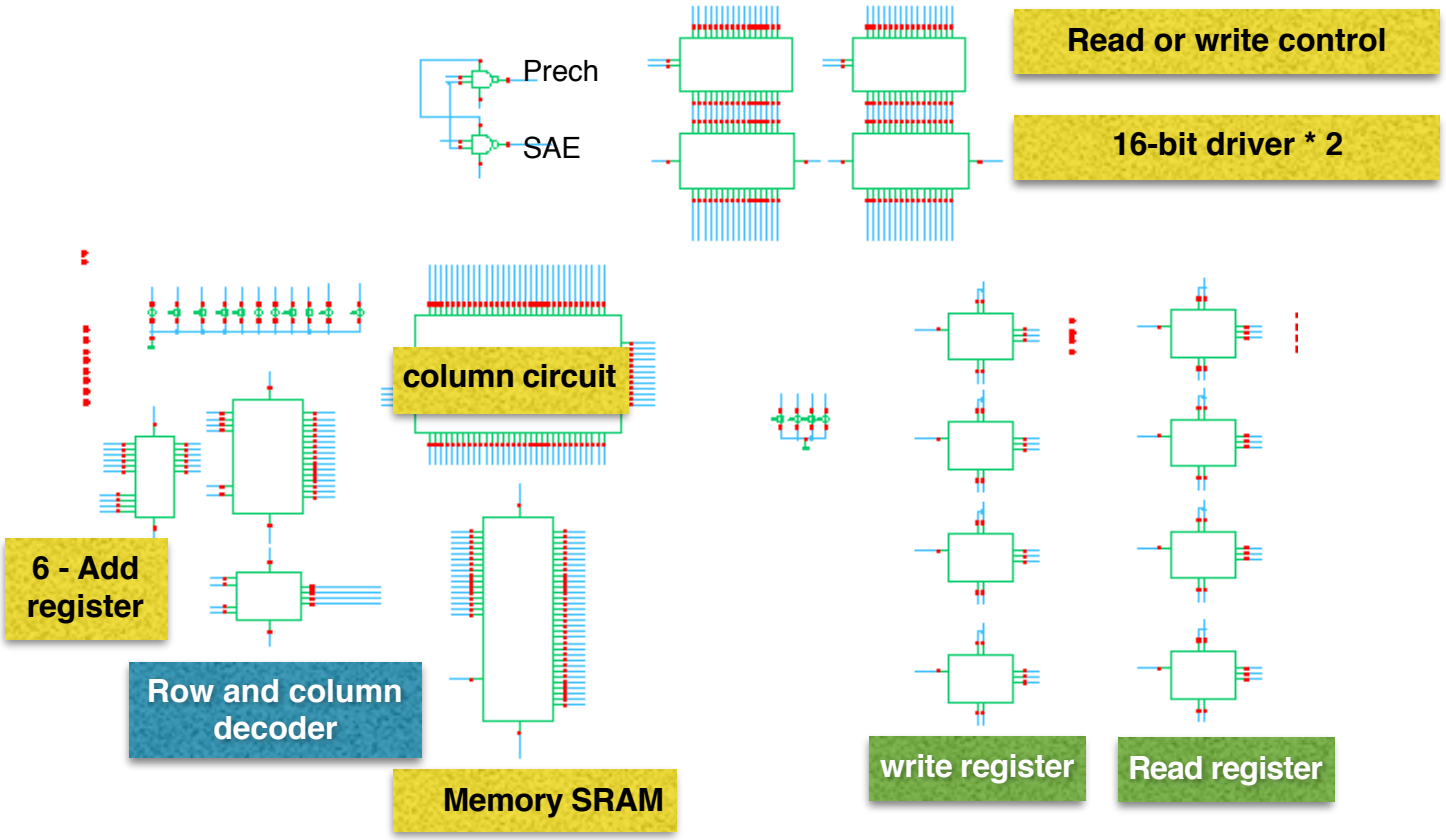
In order to minimizing the area, the PMOS transistors for the invertor, which share the source (connected to VDD), are replaced by one transistor with two fingers. The same method also applied for the NMOS transistors.

The area of this cell is 0.8381um^2
For the SRAM (256 cell): 0.8381*256 = 214.5536um^2
Taking the subtract contact and others global connection into consideration, the total area will be estimated as: 260um^2
(214.5536+1.4*0.2*(64+64))

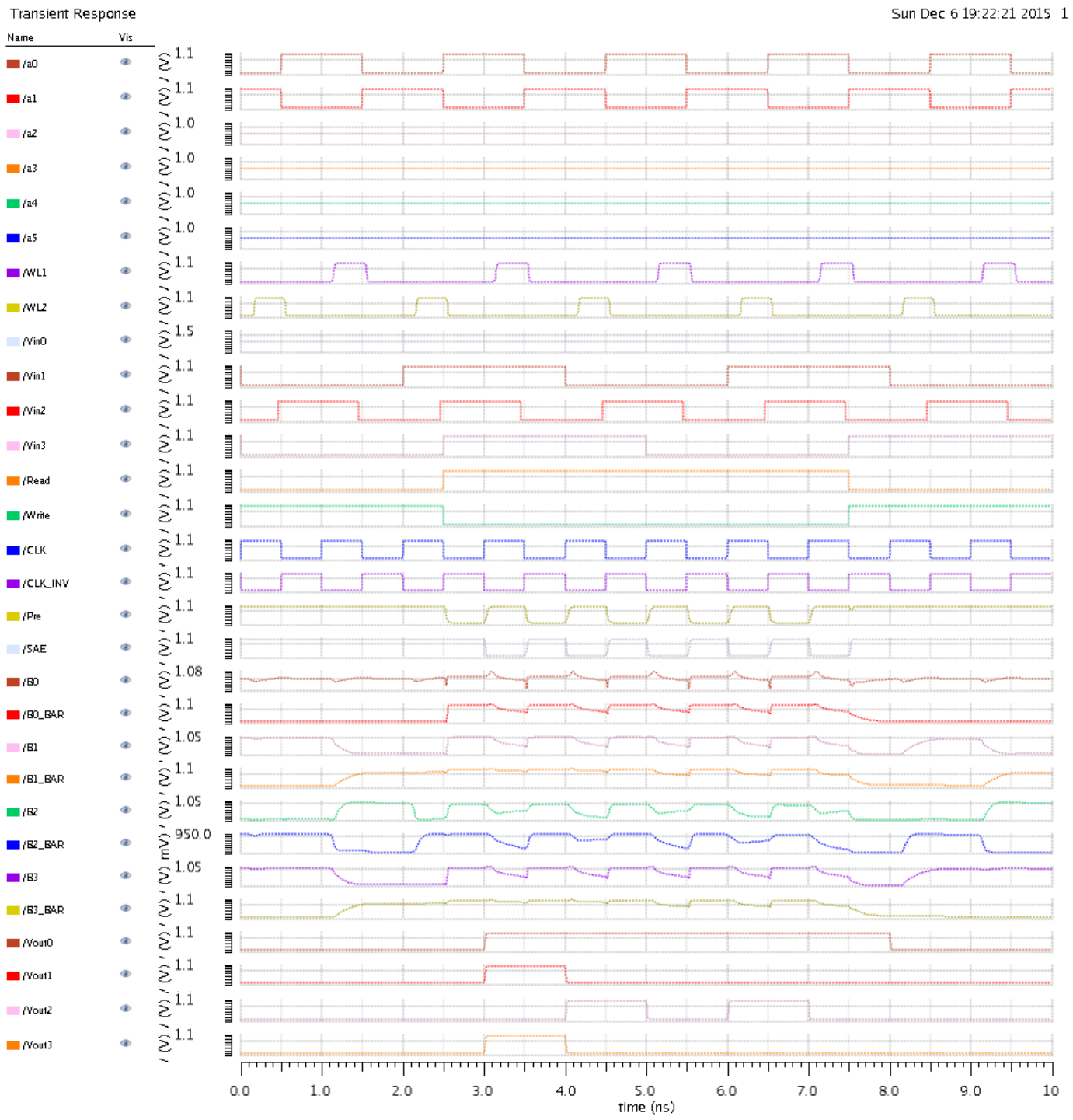
(The DRC and LVS reports are attached at the end of this document.)

2. Top-level results:

2.1 Top-level schmatic:



2.2 Schematic-level testing of the entire array:



As we can see from picture, we write to the first column, second row CELL21 and first column, third row CELL31

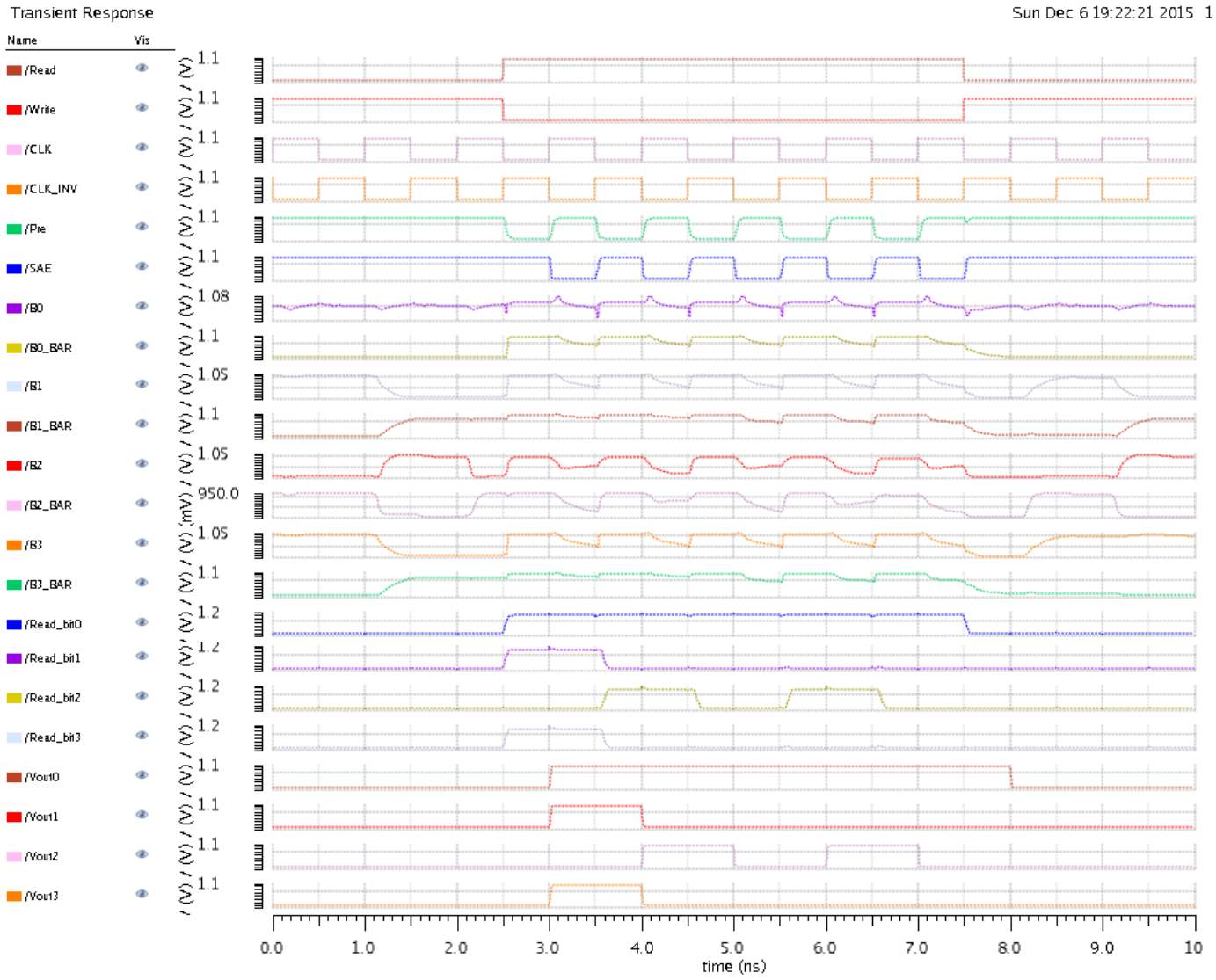
1. [a5 a4 a3 a2 a1 a0] represent address input.
2. [W1 W0] represent word line of row address.
3. Read and write signal are input signal.
4. Pre is precharge signal
5. SAE is the to activate the sense amplifier.
6. [B3 B3_bar B2 B2_bar B1 B1_bar B0 B0_bar] represent bit line of first column
7.[Vout3 Vout2 Vout1 Vout0] represent the output from read output register.
8.[Vin3 Vin3 Vin3 Vin3] is the input of write input register .

Firstly, we write to the first column, second row CELL21 and first column, third row CELL31 . The input are [Vin3 Vin2 Vin1 Vin0] shown from picture.
Then we read from these two cell and we see that the bit line change is right and the output from the read register is right.

For example, we write [1010] to CELL21 at 1 ns and [1000] to CELL31 at 2 ns, and we can see when we read from cell. When reading, the output of register is [1010] at 4 ns and [1000] at 5ns. The output is same to what we write. So, the result is right.

2.3 Output from sense amplifier

[Read_bit3 Read_bit2 Read_bit1 Read_bit0] are the output from sense amplifier or latch, we can see it amplify it successfully.



DRC report:

Cell 2000
Well.1
0 0 2 Dec 6 16:33:46 2015
Rule File Pathname: /home/FALL2015/kl2646/vlsi/project/_calibreDRC.rul_
Nwell and Pwell must not overlap
Well.2
0 0 2 Dec 6 16:33:46 2015
Rule File Pathname: /home/FALL2015/kl2646/vlsi/project/_calibreDRC.rul_
Min spacing of pwell to nwell = 0.225
Well.4
0 0 2 Dec 6 16:33:46 2015
Rule File Pathname: /home/FALL2015/kl2646/vlsi/project/_calibreDRC.rul_
Min width of well = 0.2
Poly.1
0 0 2 Dec 6 16:33:46 2015
Rule File Pathname: /home/FALL2015/kl2646/vlsi/project/_calibreDRC.rul_
Min width of poly = 0.05
Poly.2
0 0 2 Dec 6 16:33:46 2015
Rule File Pathname: /home/FALL2015/kl2646/vlsi/project/_calibreDRC.rul_
Min spacing of gate poly = 0.14
Poly.3
0 0 2 Dec 6 16:33:46 2015
Rule File Pathname: /home/FALL2015/kl2646/vlsi/project/_calibreDRC.rul_
Min extension of poly past active = 0.05
Poly.4
0 0 2 Dec 6 16:33:46 2015
Rule File Pathname: /home/FALL2015/kl2646/vlsi/project/_calibreDRC.rul_
Minimum active enclosure of gate = 0.07
Poly.5
0 0 2 Dec 6 16:33:46 2015
Rule File Pathname: /home/FALL2015/kl2646/vlsi/project/_calibreDRC.rul_
Minimum spacing of poly to active = 0.05
Poly.6
0 0 2 Dec 6 16:33:46 2015
Rule File Pathname: /home/FALL2015/kl2646/vlsi/project/_calibreDRC.rul_
Minimum spacing of field poly = 0.075
Active.1
0 0 2 Dec 6 16:33:46 2015
Rule File Pathname: /home/FALL2015/kl2646/vlsi/project/_calibreDRC.rul_
Minimum width of active = 0.09
Active.2
0 0 2 Dec 6 16:33:46 2015
Rule File Pathname: /home/FALL2015/kl2646/vlsi/project/_calibreDRC.rul_

Minimum spacing of active areas = 0.08
Active.3
0 0 2 Dec 6 16:33:46 2015
Rule File Pathname: /home/FALL2015/kl2646/vlsi/project/_calibreDRC.rul_
Minimum well enclosure of active = 0.055
Active.4
0 0 2 Dec 6 16:33:46 2015
Rule File Pathname: /home/FALL2015/kl2646/vlsi/project/_calibreDRC.rul_
Active must be inside well
Implant.1
0 0 2 Dec 6 16:33:46 2015
Rule File Pathname: /home/FALL2015/kl2646/vlsi/project/_calibreDRC.rul_
Minimum spacing of implant to gate = 0.07
Implant.2
0 0 2 Dec 6 16:33:46 2015
Rule File Pathname: /home/FALL2015/kl2646/vlsi/project/_calibreDRC.rul_
Minimum spacing of implant to contact = 0.025
Implant.3
0 0 2 Dec 6 16:33:46 2015
Rule File Pathname: /home/FALL2015/kl2646/vlsi/project/_calibreDRC.rul_
Minimum spacing of implant = 0.045
Implant.4
0 0 2 Dec 6 16:33:46 2015
Rule File Pathname: /home/FALL2015/kl2646/vlsi/project/_calibreDRC.rul_
Minimum width of implant = 0.045
Implant.6
0 0 2 Dec 6 16:33:46 2015
Rule File Pathname: /home/FALL2015/kl2646/vlsi/project/_calibreDRC.rul_
Nimplant and pimplant must not overlap
Contact.1
0 0 2 Dec 6 16:33:46 2015
Rule File Pathname: /home/FALL2015/kl2646/vlsi/project/_calibreDRC.rul_
Minimum width of contact = 0.065
Contact.2
0 0 2 Dec 6 16:33:46 2015
Rule File Pathname: /home/FALL2015/kl2646/vlsi/project/_calibreDRC.rul_
Minimum spacing of contact = 0.075
Contact.3
0 0 2 Dec 6 16:33:46 2015
Rule File Pathname: /home/FALL2015/kl2646/vlsi/project/_calibreDRC.rul_
Contact must be inside metal1 and active or poly
Contact.4
0 0 2 Dec 6 16:33:46 2015
Rule File Pathname: /home/FALL2015/kl2646/vlsi/project/_calibreDRC.rul_
Minimum active enclosure of contact = 0.005
Contact.5
0 0 2 Dec 6 16:33:46 2015
Rule File Pathname: /home/FALL2015/kl2646/vlsi/project/_calibreDRC.rul_
Minimum poly enclosure of contact = 0.005

Contact.6
0 0 2 Dec 6 16:33:46 2015
Rule File Pathname: /home/FALL2015/kl2646/vlsi/project/_calibreDRC.rul_
Minimum spacing of contact to poly = 0.035
Metal1.1
0 0 2 Dec 6 16:33:46 2015
Rule File Pathname: /home/FALL2015/kl2646/vlsi/project/_calibreDRC.rul_
Minimum width of metal1 = 0.065
Metal1.2
0 0 2 Dec 6 16:33:46 2015
Rule File Pathname: /home/FALL2015/kl2646/vlsi/project/_calibreDRC.rul_
Minimum spacing of metal1 = 0.065
Metal1.3
0 0 2 Dec 6 16:33:46 2015
Rule File Pathname: /home/FALL2015/kl2646/vlsi/project/_calibreDRC.rul_
Metal1 must extend past contact by 0.035 on two opposite sides
Metal1.4
0 0 2 Dec 6 16:33:46 2015
Rule File Pathname: /home/FALL2015/kl2646/vlsi/project/_calibreDRC.rul_
Metal1 must extend past via1 by 0.035 on two opposite sides
Via1.1
0 0 2 Dec 6 16:33:46 2015
Rule File Pathname: /home/FALL2015/kl2646/vlsi/project/_calibreDRC.rul_
Minimum width of via1 = 0.065
Via1.2
0 0 2 Dec 6 16:33:46 2015
Rule File Pathname: /home/FALL2015/kl2646/vlsi/project/_calibreDRC.rul_
Minimum spacing of via1 = 0.075
Via1.3
0 0 2 Dec 6 16:33:46 2015
Rule File Pathname: /home/FALL2015/kl2646/vlsi/project/_calibreDRC.rul_
Via1 must be inside metal1
Via1.4
0 0 2 Dec 6 16:33:46 2015
Rule File Pathname: /home/FALL2015/kl2646/vlsi/project/_calibreDRC.rul_
Via1 must be inside metal2
Metal2.1
0 0 2 Dec 6 16:33:46 2015
Rule File Pathname: /home/FALL2015/kl2646/vlsi/project/_calibreDRC.rul_
Minimum width of metal2 = 0.07
Metal2.2
0 0 2 Dec 6 16:33:46 2015
Rule File Pathname: /home/FALL2015/kl2646/vlsi/project/_calibreDRC.rul_
Minimum spacing of metal2 = 0.07
Metal2.3
0 0 2 Dec 6 16:33:46 2015
Rule File Pathname: /home/FALL2015/kl2646/vlsi/project/_calibreDRC.rul_
Metal2 must extend past via1 by 0.035 on two opposite sides
Metal2.4

0 0 2 Dec 6 16:33:46 2015
Rule File Pathname: /home/FALL2015/kl2646/vlsi/project/_calibreDRC.rul_
Metal2 must extend past via2 by 0.035 on two opposite sides
Via2.1
0 0 2 Dec 6 16:33:46 2015
Rule File Pathname: /home/FALL2015/kl2646/vlsi/project/_calibreDRC.rul_
Minimum width of via2 = 0.07
Via2.2
0 0 2 Dec 6 16:33:46 2015
Rule File Pathname: /home/FALL2015/kl2646/vlsi/project/_calibreDRC.rul_
Minimum spacing of via2 = 0.085
Via2.3
0 0 2 Dec 6 16:33:46 2015
Rule File Pathname: /home/FALL2015/kl2646/vlsi/project/_calibreDRC.rul_
Via2 must be inside metal2
Via2.4
0 0 2 Dec 6 16:33:46 2015
Rule File Pathname: /home/FALL2015/kl2646/vlsi/project/_calibreDRC.rul_
Via2 must be inside metal3
Metal3.1
0 0 2 Dec 6 16:33:46 2015
Rule File Pathname: /home/FALL2015/kl2646/vlsi/project/_calibreDRC.rul_
Minimum width of metal3 = 0.07
Metal3.2
0 0 2 Dec 6 16:33:46 2015
Rule File Pathname: /home/FALL2015/kl2646/vlsi/project/_calibreDRC.rul_
Minimum spacing of metal3 = 0.07
Metal3.3
0 0 2 Dec 6 16:33:46 2015
Rule File Pathname: /home/FALL2015/kl2646/vlsi/project/_calibreDRC.rul_
Metal3 must extend past via2 by 0.035 on two opposite sides
Metal3.4
0 0 2 Dec 6 16:33:46 2015
Rule File Pathname: /home/FALL2015/kl2646/vlsi/project/_calibreDRC.rul_
Metal3 must extend past via3 by 0.035 on two opposite sides
Via3.1
0 0 2 Dec 6 16:33:46 2015
Rule File Pathname: /home/FALL2015/kl2646/vlsi/project/_calibreDRC.rul_
Minimum width of via3 = 0.07
Via3.2
0 0 2 Dec 6 16:33:46 2015
Rule File Pathname: /home/FALL2015/kl2646/vlsi/project/_calibreDRC.rul_
Minimum spacing of via3 = 0.085
Via3.3
0 0 2 Dec 6 16:33:46 2015
Rule File Pathname: /home/FALL2015/kl2646/vlsi/project/_calibreDRC.rul_
Via3 must be inside metal3
Via3.4
0 0 2 Dec 6 16:33:46 2015

Rule File Pathname: /home/FALL2015/kl2646/vlsi/project/_calibreDRC.rul_
Via3 must be inside metal4
Metal4.1
0 0 2 Dec 6 16:33:46 2015
Rule File Pathname: /home/FALL2015/kl2646/vlsi/project/_calibreDRC.rul_
Minimum width of metal4 = 0.14
Metal4.2
0 0 2 Dec 6 16:33:46 2015
Rule File Pathname: /home/FALL2015/kl2646/vlsi/project/_calibreDRC.rul_
Minimum spacing of metal4 = 0.14
Metal4.3
0 0 2 Dec 6 16:33:46 2015
Rule File Pathname: /home/FALL2015/kl2646/vlsi/project/_calibreDRC.rul_
Minimum enclosure of metal4 around via3
Via4.1
0 0 2 Dec 6 16:33:46 2015
Rule File Pathname: /home/FALL2015/kl2646/vlsi/project/_calibreDRC.rul_
Minimum width of via4 = 0.14
Via4.2
0 0 2 Dec 6 16:33:46 2015
Rule File Pathname: /home/FALL2015/kl2646/vlsi/project/_calibreDRC.rul_
Minimum spacing of via4 = 0.16
Via4.3
0 0 2 Dec 6 16:33:46 2015
Rule File Pathname: /home/FALL2015/kl2646/vlsi/project/_calibreDRC.rul_
Via4 must be inside metal4
Via4.4
0 0 2 Dec 6 16:33:46 2015
Rule File Pathname: /home/FALL2015/kl2646/vlsi/project/_calibreDRC.rul_
Via4 must be inside metal5
Metal5.1
0 0 2 Dec 6 16:33:46 2015
Rule File Pathname: /home/FALL2015/kl2646/vlsi/project/_calibreDRC.rul_
Minimum width of metal5 = 0.14
Metal5.2
0 0 2 Dec 6 16:33:46 2015
Rule File Pathname: /home/FALL2015/kl2646/vlsi/project/_calibreDRC.rul_
Minimum spacing of metal5 = 0.14
Metal5.3
0 0 2 Dec 6 16:33:46 2015
Rule File Pathname: /home/FALL2015/kl2646/vlsi/project/_calibreDRC.rul_
Minimum enclosure of metal5 around via4
Via5.1
0 0 2 Dec 6 16:33:46 2015
Rule File Pathname: /home/FALL2015/kl2646/vlsi/project/_calibreDRC.rul_
Minimum width of via5 = 0.14
Via5.2
0 0 2 Dec 6 16:33:46 2015
Rule File Pathname: /home/FALL2015/kl2646/vlsi/project/_calibreDRC.rul_

Minimum spacing of via5 = 0.16
Via5.3
0 0 2 Dec 6 16:33:46 2015
Rule File Pathname: /home/FALL2015/kl2646/vlsi/project/_calibreDRC.rul_
Via5 must be inside metal5
Via5.4
0 0 2 Dec 6 16:33:46 2015
Rule File Pathname: /home/FALL2015/kl2646/vlsi/project/_calibreDRC.rul_
Via5 must be inside metal6
Metal6.1
0 0 2 Dec 6 16:33:46 2015
Rule File Pathname: /home/FALL2015/kl2646/vlsi/project/_calibreDRC.rul_
Minimum width of metal6 = 0.14
Metal6.2
0 0 2 Dec 6 16:33:46 2015
Rule File Pathname: /home/FALL2015/kl2646/vlsi/project/_calibreDRC.rul_
Minimum spacing of metal6 = 0.14
Metal6.3
0 0 2 Dec 6 16:33:46 2015
Rule File Pathname: /home/FALL2015/kl2646/vlsi/project/_calibreDRC.rul_
Minimum enclosure of metal6 around via5
Via6.1
0 0 2 Dec 6 16:33:46 2015
Rule File Pathname: /home/FALL2015/kl2646/vlsi/project/_calibreDRC.rul_
Minimum width of via6 = 0.14
Via6.2
0 0 2 Dec 6 16:33:46 2015
Rule File Pathname: /home/FALL2015/kl2646/vlsi/project/_calibreDRC.rul_
Minimum spacing of via6 = 0.16
Via6.3
0 0 2 Dec 6 16:33:46 2015
Rule File Pathname: /home/FALL2015/kl2646/vlsi/project/_calibreDRC.rul_
Via6 must be inside metal6
Via6.4
0 0 2 Dec 6 16:33:46 2015
Rule File Pathname: /home/FALL2015/kl2646/vlsi/project/_calibreDRC.rul_
Via6 must be inside metal7
Metal7.1
0 0 2 Dec 6 16:33:46 2015
Rule File Pathname: /home/FALL2015/kl2646/vlsi/project/_calibreDRC.rul_
Minimum width of metal7 = 0.4
Metal7.2
0 0 2 Dec 6 16:33:46 2015
Rule File Pathname: /home/FALL2015/kl2646/vlsi/project/_calibreDRC.rul_
Minimum spacing of metal7 = 0.4
Metal7.3
0 0 2 Dec 6 16:33:46 2015
Rule File Pathname: /home/FALL2015/kl2646/vlsi/project/_calibreDRC.rul_
Minimum enclosure of metal7 around via6

Via7.1
0 0 2 Dec 6 16:33:46 2015
Rule File Pathname: /home/FALL2015/kl2646/vlsi/project/_calibreDRC.rul_
Minimum width of via7 = 0.4
Via7.2
0 0 2 Dec 6 16:33:46 2015
Rule File Pathname: /home/FALL2015/kl2646/vlsi/project/_calibreDRC.rul_
Minimum spacing of via7 = 0.44
Via7.3
0 0 2 Dec 6 16:33:46 2015
Rule File Pathname: /home/FALL2015/kl2646/vlsi/project/_calibreDRC.rul_
Via7 must be inside metal7
Via7.4
0 0 2 Dec 6 16:33:46 2015
Rule File Pathname: /home/FALL2015/kl2646/vlsi/project/_calibreDRC.rul_
Via7 must be inside metal8
Metal8.1
0 0 2 Dec 6 16:33:46 2015
Rule File Pathname: /home/FALL2015/kl2646/vlsi/project/_calibreDRC.rul_
Minimum width of metal8 = 0.4
Metal8.2
0 0 2 Dec 6 16:33:46 2015
Rule File Pathname: /home/FALL2015/kl2646/vlsi/project/_calibreDRC.rul_
Minimum spacing of metal8 = 0.4
Metal8.3
0 0 2 Dec 6 16:33:46 2015
Rule File Pathname: /home/FALL2015/kl2646/vlsi/project/_calibreDRC.rul_
Minimum enclosure of metal8 around via7
Via8.1
0 0 2 Dec 6 16:33:46 2015
Rule File Pathname: /home/FALL2015/kl2646/vlsi/project/_calibreDRC.rul_
Minimum width of via8 = 0.4
Via8.2
0 0 2 Dec 6 16:33:46 2015
Rule File Pathname: /home/FALL2015/kl2646/vlsi/project/_calibreDRC.rul_
Minimum spacing of via8 = 0.44
Via8.3
0 0 2 Dec 6 16:33:46 2015
Rule File Pathname: /home/FALL2015/kl2646/vlsi/project/_calibreDRC.rul_
Via8 must be inside metal8
Via8.4
0 0 2 Dec 6 16:33:46 2015
Rule File Pathname: /home/FALL2015/kl2646/vlsi/project/_calibreDRC.rul_
Via8 must be inside metal9
Metal9.1
0 0 2 Dec 6 16:33:46 2015
Rule File Pathname: /home/FALL2015/kl2646/vlsi/project/_calibreDRC.rul_
Minimum width of metal9 = 0.8
Metal9.2

0 0 2 Dec 6 16:33:46 2015
Rule File Pathname: /home/FALL2015/kl2646/vlsi/project/_calibreDRC.rul_
Minimum spacing of metal9 = 0.8
Metal9.3
0 0 2 Dec 6 16:33:46 2015
Rule File Pathname: /home/FALL2015/kl2646/vlsi/project/_calibreDRC.rul_
Minimum enclosure of metal9 around via8
Via9.1
0 0 2 Dec 6 16:33:46 2015
Rule File Pathname: /home/FALL2015/kl2646/vlsi/project/_calibreDRC.rul_
Minimum width of via9 = 0.8
Via9.2
0 0 2 Dec 6 16:33:46 2015
Rule File Pathname: /home/FALL2015/kl2646/vlsi/project/_calibreDRC.rul_
Minimum spacing of via9 = 0.88
Via9.3
0 0 2 Dec 6 16:33:46 2015
Rule File Pathname: /home/FALL2015/kl2646/vlsi/project/_calibreDRC.rul_
Via9 must be inside metal9
Via9.4
0 0 2 Dec 6 16:33:46 2015
Rule File Pathname: /home/FALL2015/kl2646/vlsi/project/_calibreDRC.rul_
Via9 must be inside metal10
Metal10.1
0 0 2 Dec 6 16:33:46 2015
Rule File Pathname: /home/FALL2015/kl2646/vlsi/project/_calibreDRC.rul_
Minimum width of metal10 = 0.8
Metal10.2
0 0 2 Dec 6 16:33:46 2015
Rule File Pathname: /home/FALL2015/kl2646/vlsi/project/_calibreDRC.rul_
Minimum spacing of metal10 = 0.8
Metal10.3
0 0 2 Dec 6 16:33:46 2015
Rule File Pathname: /home/FALL2015/kl2646/vlsi/project/_calibreDRC.rul_
Minimum enclosure of metal10 around via9
Metal1.5
0 0 2 Dec 6 16:33:46 2015
Rule File Pathname: /home/FALL2015/kl2646/vlsi/project/_calibreDRC.rul_
Minimum spacing of metal1 wider than 0.09 & longer than 0.3 = 0.09
Metal1.6
0 0 2 Dec 6 16:33:46 2015
Rule File Pathname: /home/FALL2015/kl2646/vlsi/project/_calibreDRC.rul_
Minimum spacing of metal1 wider than 0.27 & longer than 0.9 = 0.27
Metal1.7
0 0 2 Dec 6 16:33:46 2015
Rule File Pathname: /home/FALL2015/kl2646/vlsi/project/_calibreDRC.rul_
Minimum spacing of metal1 wider than 0.5 & longer than 1.8 = 0.5
Metal1.8
0 0 2 Dec 6 16:33:46 2015

Rule File Pathname: /home/FALL2015/kl2646/vlsi/project/_calibreDRC.rul_
Minimum spacing of metal1 wider than 0.9 & longer than 2.7 = 0.9
Metal1.9
0 0 2 Dec 6 16:33:46 2015
Rule File Pathname: /home/FALL2015/kl2646/vlsi/project/_calibreDRC.rul_
Minimum spacing of metal1 wider than 1.5 & longer than 4.0 = 1.5
Metal2.5
0 0 2 Dec 6 16:33:46 2015
Rule File Pathname: /home/FALL2015/kl2646/vlsi/project/_calibreDRC.rul_
Minimum spacing of metal2 wider than 0.09 & longer than 0.3 = 0.09
Metal2.6
0 0 2 Dec 6 16:33:46 2015
Rule File Pathname: /home/FALL2015/kl2646/vlsi/project/_calibreDRC.rul_
Minimum spacing of metal2 wider than 0.27 & longer than 0.9 = 0.27
Metal2.7
0 0 2 Dec 6 16:33:46 2015
Rule File Pathname: /home/FALL2015/kl2646/vlsi/project/_calibreDRC.rul_
Minimum spacing of metal2 wider than 0.5 & longer than 1.8 = 0.5
Metal2.8
0 0 2 Dec 6 16:33:46 2015
Rule File Pathname: /home/FALL2015/kl2646/vlsi/project/_calibreDRC.rul_
Minimum spacing of metal2 wider than 0.9 & longer than 2.7 = 0.9
Metal2.9
0 0 2 Dec 6 16:33:46 2015
Rule File Pathname: /home/FALL2015/kl2646/vlsi/project/_calibreDRC.rul_
Minimum spacing of metal2 wider than 1.5 & longer than 4.0 = 1.5
Metal3.5
0 0 2 Dec 6 16:33:46 2015
Rule File Pathname: /home/FALL2015/kl2646/vlsi/project/_calibreDRC.rul_
Minimum spacing of metal3 wider than 0.09 & longer than 0.3 = 0.09
Metal3.6
0 0 2 Dec 6 16:33:46 2015
Rule File Pathname: /home/FALL2015/kl2646/vlsi/project/_calibreDRC.rul_
Minimum spacing of metal3 wider than 0.27 & longer than 0.9 = 0.27
Metal3.7
0 0 2 Dec 6 16:33:46 2015
Rule File Pathname: /home/FALL2015/kl2646/vlsi/project/_calibreDRC.rul_
Minimum spacing of metal3 wider than 0.5 & longer than 1.8 = 0.5
Metal3.8
0 0 2 Dec 6 16:33:46 2015
Rule File Pathname: /home/FALL2015/kl2646/vlsi/project/_calibreDRC.rul_
Minimum spacing of metal3 wider than 0.9 & longer than 2.7 = 0.9
Metal3.9
0 0 2 Dec 6 16:33:46 2015
Rule File Pathname: /home/FALL2015/kl2646/vlsi/project/_calibreDRC.rul_
Minimum spacing of metal3 wider than 1.5 & longer than 4.0 = 1.5
Metal4.5
0 0 2 Dec 6 16:33:46 2015
Rule File Pathname: /home/FALL2015/kl2646/vlsi/project/_calibreDRC.rul_

Minimum spacing of metal4 wider than 0.27 & longer than 0.9 = 0.27
Metal4.6
0 0 2 Dec 6 16:33:46 2015
Rule File Pathname: /home/FALL2015/kl2646/vlsi/project/_calibreDRC.rul_
Minimum spacing of metal4 wider than 0.5 & longer than 1.8 = 0.5
Metal4.7
0 0 2 Dec 6 16:33:46 2015
Rule File Pathname: /home/FALL2015/kl2646/vlsi/project/_calibreDRC.rul_
Minimum spacing of metal4 wider than 0.9 & longer than 2.7 = 0.9
Metal4.8
0 0 2 Dec 6 16:33:46 2015
Rule File Pathname: /home/FALL2015/kl2646/vlsi/project/_calibreDRC.rul_
Minimum spacing of metal4 wider than 1.5 & longer than 4.0 = 1.5
Metal5.5
0 0 2 Dec 6 16:33:46 2015
Rule File Pathname: /home/FALL2015/kl2646/vlsi/project/_calibreDRC.rul_
Minimum spacing of metal5 wider than 0.27 & longer than 0.9 = 0.27
Metal5.6
0 0 2 Dec 6 16:33:46 2015
Rule File Pathname: /home/FALL2015/kl2646/vlsi/project/_calibreDRC.rul_
Minimum spacing of metal5 wider than 0.5 & longer than 1.8 = 0.5
Metal5.7
0 0 2 Dec 6 16:33:46 2015
Rule File Pathname: /home/FALL2015/kl2646/vlsi/project/_calibreDRC.rul_
Minimum spacing of metal5 wider than 0.9 & longer than 2.7 = 0.9
Metal5.8
0 0 2 Dec 6 16:33:46 2015
Rule File Pathname: /home/FALL2015/kl2646/vlsi/project/_calibreDRC.rul_
Minimum spacing of metal5 wider than 1.5 & longer than 4.0 = 1.5
Metal6.5
0 0 2 Dec 6 16:33:46 2015
Rule File Pathname: /home/FALL2015/kl2646/vlsi/project/_calibreDRC.rul_
Minimum spacing of metal6 wider than 0.27 & longer than 0.9 = 0.27
Metal6.6
0 0 2 Dec 6 16:33:46 2015
Rule File Pathname: /home/FALL2015/kl2646/vlsi/project/_calibreDRC.rul_
Minimum spacing of metal6 wider than 0.5 & longer than 1.8 = 0.5
Metal6.7
0 0 2 Dec 6 16:33:46 2015
Rule File Pathname: /home/FALL2015/kl2646/vlsi/project/_calibreDRC.rul_
Minimum spacing of metal6 wider than 0.9 & longer than 2.7 = 0.9
Metal6.8
0 0 2 Dec 6 16:33:46 2015
Rule File Pathname: /home/FALL2015/kl2646/vlsi/project/_calibreDRC.rul_
Minimum spacing of metal6 wider than 1.5 & longer than 4.0 = 1.5
Metal7.5
0 0 2 Dec 6 16:33:46 2015
Rule File Pathname: /home/FALL2015/kl2646/vlsi/project/_calibreDRC.rul_
Minimum spacing of metal7 wider than 0.5 & longer than 1.8 = 0.5

Metal7.6
0 0 2 Dec 6 16:33:46 2015
Rule File Pathname: /home/FALL2015/kl2646/vlsi/project/_calibreDRC.rul_
Minimum spacing of metal7 wider than 0.9 & longer than 2.7 = 0.9
Metal7.7
0 0 2 Dec 6 16:33:46 2015
Rule File Pathname: /home/FALL2015/kl2646/vlsi/project/_calibreDRC.rul_
Minimum spacing of metal7 wider than 1.5 & longer than 4.0 = 1.5
Metal8.5
0 0 2 Dec 6 16:33:46 2015
Rule File Pathname: /home/FALL2015/kl2646/vlsi/project/_calibreDRC.rul_
Minimum spacing of metal8 wider than 0.5 & longer than 1.8 = 0.5
Metal8.6
0 0 2 Dec 6 16:33:46 2015
Rule File Pathname: /home/FALL2015/kl2646/vlsi/project/_calibreDRC.rul_
Minimum spacing of metal8 wider than 0.9 & longer than 2.7 = 0.9
Metal8.7
0 0 2 Dec 6 16:33:46 2015
Rule File Pathname: /home/FALL2015/kl2646/vlsi/project/_calibreDRC.rul_
Minimum spacing of metal8 wider than 1.5 & longer than 4.0 = 1.5
Metal9.5
0 0 2 Dec 6 16:33:46 2015
Rule File Pathname: /home/FALL2015/kl2646/vlsi/project/_calibreDRC.rul_
Minimum spacing of metal9 wider than 0.9 & longer than 2.7 = 0.9
Metal9.6
0 0 2 Dec 6 16:33:46 2015
Rule File Pathname: /home/FALL2015/kl2646/vlsi/project/_calibreDRC.rul_
Minimum spacing of metal9 wider than 1.5 & longer than 4.0 = 1.5
Metal10.5
0 0 2 Dec 6 16:33:46 2015
Rule File Pathname: /home/FALL2015/kl2646/vlsi/project/_calibreDRC.rul_
Minimum spacing of metal10 wider than 0.9 & longer than 2.7 = 0.9
Metal10.6
0 0 2 Dec 6 16:33:46 2015
Rule File Pathname: /home/FALL2015/kl2646/vlsi/project/_calibreDRC.rul_
Minimum spacing of metal10 wider than 1.5 & longer than 4.0 = 1.5
Grid.1
0 0 2 Dec 6 16:33:46 2015
Rule File Pathname: /home/FALL2015/kl2646/vlsi/project/_calibreDRC.rul_
All shapes must be on a 2.5 nm grid
Grid.2
0 0 2 Dec 6 16:33:46 2015
Rule File Pathname: /home/FALL2015/kl2646/vlsi/project/_calibreDRC.rul_
All shapes must be on a 2.5 nm grid
Grid.3
0 0 2 Dec 6 16:33:46 2015
Rule File Pathname: /home/FALL2015/kl2646/vlsi/project/_calibreDRC.rul_
All shapes must be on a 2.5 nm grid
Grid.4

0 0 2 Dec 6 16:33:46 2015
Rule File Pathname: /home/FALL2015/kl2646/vlsi/project/_calibreDRC.rul_
All shapes must be on a 2.5 nm grid
Grid.5
0 0 2 Dec 6 16:33:46 2015
Rule File Pathname: /home/FALL2015/kl2646/vlsi/project/_calibreDRC.rul_
All shapes must be on a 2.5 nm grid
Grid.6
0 0 2 Dec 6 16:33:46 2015
Rule File Pathname: /home/FALL2015/kl2646/vlsi/project/_calibreDRC.rul_
All shapes must be on a 2.5 nm grid
Grid.7
0 0 2 Dec 6 16:33:46 2015
Rule File Pathname: /home/FALL2015/kl2646/vlsi/project/_calibreDRC.rul_
All shapes must be on a 2.5 nm grid
Grid.8
0 0 2 Dec 6 16:33:46 2015
Rule File Pathname: /home/FALL2015/kl2646/vlsi/project/_calibreDRC.rul_
All shapes must be on a 2.5 nm grid
Grid.9
0 0 2 Dec 6 16:33:46 2015
Rule File Pathname: /home/FALL2015/kl2646/vlsi/project/_calibreDRC.rul_
All shapes must be on a 2.5 nm grid
Grid.10
0 0 2 Dec 6 16:33:46 2015
Rule File Pathname: /home/FALL2015/kl2646/vlsi/project/_calibreDRC.rul_
All shapes must be on a 2.5 nm grid
Grid.11
0 0 2 Dec 6 16:33:46 2015
Rule File Pathname: /home/FALL2015/kl2646/vlsi/project/_calibreDRC.rul_
All shapes must be on a 2.5 nm grid
Grid.12
0 0 2 Dec 6 16:33:46 2015
Rule File Pathname: /home/FALL2015/kl2646/vlsi/project/_calibreDRC.rul_
All shapes must be on a 2.5 nm grid
Grid.13
0 0 2 Dec 6 16:33:46 2015
Rule File Pathname: /home/FALL2015/kl2646/vlsi/project/_calibreDRC.rul_
All shapes must be on a 2.5 nm grid
Grid.14
0 0 2 Dec 6 16:33:46 2015
Rule File Pathname: /home/FALL2015/kl2646/vlsi/project/_calibreDRC.rul_
All shapes must be on a 2.5 nm grid
Grid.15
0 0 2 Dec 6 16:33:46 2015
Rule File Pathname: /home/FALL2015/kl2646/vlsi/project/_calibreDRC.rul_
All shapes must be on a 2.5 nm grid
Grid.16
0 0 2 Dec 6 16:33:46 2015

Rule File Pathname: /home/FALL2015/kl2646/vlsi/project/_calibreDRC.rul_
All shapes must be on a 2.5 nm grid
Grid.17
0 0 2 Dec 6 16:33:46 2015
Rule File Pathname: /home/FALL2015/kl2646/vlsi/project/_calibreDRC.rul_
All shapes must be on a 2.5 nm grid
Grid.18
0 0 2 Dec 6 16:33:46 2015
Rule File Pathname: /home/FALL2015/kl2646/vlsi/project/_calibreDRC.rul_
All shapes must be on a 2.5 nm grid
Grid.19
0 0 2 Dec 6 16:33:46 2015
Rule File Pathname: /home/FALL2015/kl2646/vlsi/project/_calibreDRC.rul_
All shapes must be on a 2.5 nm grid
Grid.20
0 0 2 Dec 6 16:33:46 2015
Rule File Pathname: /home/FALL2015/kl2646/vlsi/project/_calibreDRC.rul_
All shapes must be on a 2.5 nm grid
Grid.21
0 0 2 Dec 6 16:33:46 2015
Rule File Pathname: /home/FALL2015/kl2646/vlsi/project/_calibreDRC.rul_
All shapes must be on a 2.5 nm grid
Grid.22
0 0 2 Dec 6 16:33:46 2015
Rule File Pathname: /home/FALL2015/kl2646/vlsi/project/_calibreDRC.rul_
All shapes must be on a 2.5 nm grid
Grid.23
0 0 2 Dec 6 16:33:46 2015
Rule File Pathname: /home/FALL2015/kl2646/vlsi/project/_calibreDRC.rul_
All shapes must be on a 2.5 nm grid
Grid.24
0 0 2 Dec 6 16:33:46 2015
Rule File Pathname: /home/FALL2015/kl2646/vlsi/project/_calibreDRC.rul_
All shapes must be on a 2.5 nm grid
Grid.25
0 0 2 Dec 6 16:33:46 2015
Rule File Pathname: /home/FALL2015/kl2646/vlsi/project/_calibreDRC.rul_
All shapes must be on a 2.5 nm grid
Grid.26
0 0 2 Dec 6 16:33:46 2015
Rule File Pathname: /home/FALL2015/kl2646/vlsi/project/_calibreDRC.rul_
All shapes must be on a 2.5 nm grid
Antenna.poly
0 0 2 Dec 6 16:33:46 2015
Rule File Pathname: /home/FALL2015/kl2646/vlsi/project/_calibreDRC.rul_
Maximum allowed field poly area to antenna area is 100:1. Connect diode to relax constraint.
Antenna.metal1
0 0 2 Dec 6 16:33:46 2015
Rule File Pathname: /home/FALL2015/kl2646/vlsi/project/_calibreDRC.rul_

Maximum allowed (poly + metal 1) antenna area to gate area is 300:1. Connect diode to relax constraint.
Antenna.metal2
0 0 2 Dec 6 16:33:46 2015
Rule File Pathname: /home/FALL2015/kl2646/vlsi/project/_calibreDRC.rul_
[Area(poly)+Area(Metal 1)]:Area(Gate) should be < 300:1 to prevent plasma induced damage.
Antenna.metal3
0 0 2 Dec 6 16:33:46 2015
Rule File Pathname: /home/FALL2015/kl2646/vlsi/project/_calibreDRC.rul_
[Area(poly)+Area(Metal 1)+Area(Metal 2)]:Area(Gate) should be < 300:1 to prevent plasma induced gate oxide damage.
Antenna.metal4
0 0 2 Dec 6 16:33:46 2015
Rule File Pathname: /home/FALL2015/kl2646/vlsi/project/_calibreDRC.rul_
[Area(poly)+Area(Metal 1)+Area(Metal 2)+Area(Metal 3)]:Area(Gate) should be < 300:1 to prevent plasma induced gate oxide damage
Antenna.metal5
0 0 2 Dec 6 16:33:46 2015
Rule File Pathname: /home/FALL2015/kl2646/vlsi/project/_calibreDRC.rul_
[Area(poly+M1+M2+M3+M4):Area(Gate) should be < 300:1 to prevent plasma induced gate oxide damage
Antenna.metal6
0 0 2 Dec 6 16:33:46 2015
Rule File Pathname: /home/FALL2015/kl2646/vlsi/project/_calibreDRC.rul_
[Area(poly+M1+M2+M3+M4+M5)]:Area(Gate) should be < 300:1 to prevent plasma induced gate oxide damage
Antenna.metal7
0 0 2 Dec 6 16:33:46 2015
Rule File Pathname: /home/FALL2015/kl2646/vlsi/project/_calibreDRC.rul_
[Area(poly+M1+M2+M3+M4+M5+M6)]:Area(Gate) should be < 300:1 to prevent plasma induced gate oxide damage
Antenna.metal8
0 0 2 Dec 6 16:33:46 2015
Rule File Pathname: /home/FALL2015/kl2646/vlsi/project/_calibreDRC.rul_
[Area(poly+M1+M2+M3+M4+M5+M6+M7)]:Area(Gate) should be < 300:1 to prevent plasma induced gate oxide damage
Antenna.metal9
0 0 2 Dec 6 16:33:46 2015
Rule File Pathname: /home/FALL2015/kl2646/vlsi/project/_calibreDRC.rul_
[Area(poly+M1+M2+M3+M4+M5+M6+M7+M8)]:Area(Gate) should be < 300:1 to prevent plasma induced gate oxide damage
Antenna.metal10
0 0 2 Dec 6 16:33:46 2015
Rule File Pathname: /home/FALL2015/kl2646/vlsi/project/_calibreDRC.rul_
[Area(poly+M1+M2+M3+M4+M5+M6+M7+M8+M9)]:Area(Gate) should be < 300:1 to prevent plasma induced gate oxide damage

LVS report:

```
################################################
##                                            ##
##      C A L I B R E   S Y S T E M       ##
##                                            ##
##         L V S   R E P O R T          ##
##                                            ##
################################################
```

REPORT FILE NAME: Cell.lvs.report
LAYOUT NAME: /home/FALL2015/kl2646/vlsi/project/Cell.sp ('Cell')
SOURCE NAME: /home/FALL2015/kl2646/vlsi/project/Cell.src.net ('Cell')
RULE FILE: /home/FALL2015/kl2646/vlsi/project/_calibreLVS.rul_
RULE FILE TITLE: LVS Rule File for FreePDK45
CREATION TIME: Sun Dec 6 16:34:07 2015
CURRENT DIRECTORY: /home/FALL2015/kl2646/vlsi/project
USER NAME: kl2646
CALIBRE VERSION: v2013.1_14.11 Thu Feb 7 13:01:09 PST 2013

OVERALL COMPARISON RESULTS

```
   #    ###################     _  _
  #     #          #     *  *
 #  #    #    CORRECT    #      |
  # #    #          #     \___/
   #     ###################
```

****
*
CELL SUMMARY
****
*

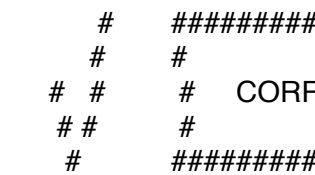
Result	Layout	Source
GROUP3 256RAM PART3		

```
  -----------    -----------                 --------------
  CORRECT        Cell                        Cell


*********************************************************************************************************************
*
                                LVS PARAMETERS
*********************************************************************************************************************
*


o LVS Setup:

   LVS COMPONENT TYPE PROPERTY           element
   LVS COMPONENT SUBTYPE PROPERTY        model
   // LVS PIN NAME PROPERTY
   LVS POWER NAME                        "VDD"
   LVS GROUND NAME                       "VSS" "GROUND"
   LVS CELL SUPPLY                       NO
   LVS RECOGNIZE GATES                   ALL
   LVS IGNORE PORTS                      NO
   LVS CHECK PORT NAMES                  NO
   LVS IGNORE TRIVIAL NAMED PORTS        NO
   LVS BUILTIN DEVICE PIN SWAP           YES
   LVS ALL CAPACITOR PINS SWAPPABLE      NO
   LVS DISCARD PINS BY DEVICE            NO
   LVS SOFT SUBSTRATE PINS               NO
   LVS INJECT LOGIC                      YES
   LVS EXPAND UNBALANCED CELLS           YES
   LVS FLATTEN INSIDE CELL               NO
   LVS EXPAND SEED PROMOTIONS            NO
   LVS PRESERVE PARAMETERIZED CELLS      NO
   LVS GLOBALS ARE PORTS                 YES
   LVS REVERSE WL                        NO
   LVS SPICE PREFER PINS                 NO
   LVS SPICE SLASH IS SPACE              YES
   LVS SPICE ALLOW FLOATING PINS         YES
   // LVS SPICE ALLOW INLINE PARAMETERS
   LVS SPICE ALLOW UNQUOTED STRINGS      NO
   LVS SPICE CONDITIONAL LDD             NO
   LVS SPICE CULL PRIMITIVE SUBCIRCUITS  NO
   LVS SPICE IMPLIED MOS AREA            NO
   // LVS SPICE MULTIPLIER NAME
   LVS SPICE OVERRIDE GLOBALS            NO
   LVS SPICE REDEFINE PARAM              NO
   LVS SPICE REPLICATE DEVICES           NO
   LVS SPICE SCALE X PARAMETERS          NO
   LVS SPICE STRICT WL                   NO
```

```
// LVS SPICE OPTION
LVS STRICT SUBTYPES                NO
LVS EXACT SUBTYPES                 NO
LAYOUT CASE                      NO
SOURCE CASE                       NO
LVS COMPARE CASE                    NO
LVS DOWNCASE DEVICE                  NO
LVS REPORT MAXIMUM                  50
LVS PROPERTY RESOLUTION MAXIMUM       32
// LVS SIGNATURE MAXIMUM
// LVS FILTER UNUSED OPTION
// LVS REPORT OPTION
LVS REPORT UNITS                   YES
// LVS NON USER NAME PORT
// LVS NON USER NAME NET
// LVS NON USER NAME INSTANCE

// Reduction

LVS REDUCE SERIES MOS               YES
LVS REDUCE PARALLEL MOS              YES
LVS REDUCE SEMI SERIES MOS            YES
LVS REDUCE SPLIT GATES              YES
LVS REDUCE PARALLEL BIPOLAR           YES
LVS REDUCE SERIES CAPACITORS          YES
LVS REDUCE PARALLEL CAPACITORS         YES
LVS REDUCE SERIES RESISTORS           YES
LVS REDUCE PARALLEL RESISTORS         YES
LVS REDUCE PARALLEL DIODES           YES
LVS REDUCTION PRIORITY              PARALLEL

LVS SHORT EQUIVALENT NODES            NO

// Trace Property

TRACE PROPERTY  mn(nmos_vtl)  l l 4e-09 ABSOLUTE
TRACE PROPERTY  mn(nmos_vtl)  w w 4e-09 ABSOLUTE
TRACE PROPERTY  mp(pmos_vtl)  l l 4e-09 ABSOLUTE
TRACE PROPERTY  mp(pmos_vtl)  w w 4e-09 ABSOLUTE
TRACE PROPERTY  mn(nmos_vth)  l l 4e-09 ABSOLUTE
TRACE PROPERTY  mn(nmos_vth)  w w 4e-09 ABSOLUTE
TRACE PROPERTY  mp(pmos_vth)  l l 4e-09 ABSOLUTE
TRACE PROPERTY  mp(pmos_vth)  w w 4e-09 ABSOLUTE
TRACE PROPERTY  mn(nmos_vtg)  l l 4e-09 ABSOLUTE
TRACE PROPERTY  mn(nmos_vtg)  w w 4e-09 ABSOLUTE
TRACE PROPERTY  mp(pmos_vtg)  l l 4e-09 ABSOLUTE
TRACE PROPERTY  mp(pmos_vtg)  w w 4e-09 ABSOLUTE
TRACE PROPERTY  mn(nmos_thkox)  l l 4e-09 ABSOLUTE
TRACE PROPERTY  mn(nmos_thkox)  w w 4e-09 ABSOLUTE
```

TRACE PROPERTY mp(pmos_thkox) l l 4e-09 ABSOLUTE
TRACE PROPERTY mp(pmos_thkox) w w 4e-09 ABSOLUTE

CELL COMPARISON RESULTS (TOP LEVEL)



LAYOUT CELL NAME: Cell
SOURCE CELL NAME: Cell

INITIAL NUMBERS OF OBJECTS

	Layout	Source	Component Type
Ports:	5	5	
Nets:	7	7	
Instances:	4	4	MN (4 pins)
	2	2	MP (4 pins)
Total Inst:	6	6	

NUMBERS OF OBJECTS AFTER TRANSFORMATION

	Layout	Source	Component Type
Ports:	5	5	
Nets:	7	7	
Instances:	2	2	MN (4 pins)
	1	1	_bitcorev (4 pins)

Total Inst: 3 3

****
*
INFORMATION AND WARNINGS
****
*

	Matched Layout	Matched Source	Unmatched Layout	Unmatched Source	Component Type
Ports:	5	5	0	0	
Nets:	7	7	0	0	
Instances:	2	2	0	0	MN(NMOS_VTL)
	1	1	0	0	_bitcorev
Total Inst:	3	3	0	0	

o Initial Correspondence Points:

Ports: VDD GND BL BL_INV WL

****
*
SUMMARY
****
*

Total CPU Time: 0 sec
Total Elapsed Time: 0 sec