

ECE 6473
Introduction to VLSI Design
Fall 2015

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Electrical and Computer Engineering
New York University

Course Focus

- An advanced treatment of analysis and design of VLSI circuits and systems
- We will learn:
 - a. How to design components of a VLSI system?
 - b. How to design a complex VLSI system using these components

Course Outline

- Introduction
- MOSFET Digital Logic (*I-V characteristics, inverter, complex logic, timing and power ...*)
- Advanced Digital Logic (*dynamic, domino, pass transistor logic ...*)
- Sequential Elements
- Arithmetic blocks (*adders, multipliers...*)
- Interconnects

Course Outline

- Memories (*SRAM, DRAM, peripherals and array...*)
- Physical Design
- VLSI System Design (*general system components, clocking, power, input/output ...*)
- Future (*spintronics ...*)

Pre-requisites

- Basic/elementary knowledge of:
 - Semiconductor devices
 - Digital logic
 - CMOS circuits
 - Linux environment for simulation and design

M. Morris R. Mano, Charles R. Kime, and Tom Martin,
“Logic and Computer Design Fundamentals,” 5th ed.
Prentice Hall.

Grading Policy- Tentative

- Two exams (**50% of overall grade**)
 - *Midterm (20%)*
 - *Final (30%)*
- Homework + Project (**50% of overall grade**)
- Homework will include both design and theoretical problems
- Project will include a short presentation/project demo and report.

Homework

- VLSI system design includes the design of individual components (eg. gates, adders ...) and design of the system by interconnecting the components properly.
- Theoretical and design homework problems:
 - emphasis on individual components
 - collaboration and discussion policies will be declared with each homework

Project

- Project will focus on designing a system using the components in the homework.
- Project will be conducted in groups of FOUR. Total number of project groups = 25.
- Plan your project group after the first class.
- Each group member needs to contribute equally. Project report must list the contribution of each person.

Text Books

Introduction to VLSI Circuits and Systems, Uyemura, John Wiley, 2002.

Digital Integrated Circuits: A Design Perspective (2nd Edition), J. M. Rabaey, A. Chandrakasan, B. Nikolic, Prentice Hall, 2002.

Class notes will be posted on the course website.

Journal and conference published articles will be shared as and when necessary.

Website, Office Hours, etc...

Website: newclasses.nyu.edu

Office Hours:

Instructor: Shaloo Rakheja (shaloo.rakheja@nyu.edu)

Tuesday: 12:00 – 2:00 PM

2 MetroTech

10th Floor, Rm 10.068

Course Assistants:

Akash Jumrani (akash.jumrani@nyu.edu)

Jinesh Doshi (jjd465@nyu.edu)

Narsimh Nayak (narsimh.nayak@nyu.edu)

Office hours: Tuesday: 2:00 – 4:00 PM & Friday: 12:00 – 2:00 PM

Academic Misconduct

Students caught engaging in an academically dishonest practice will receive a failing grade for the course.

University policy on academic dishonesty will be followed strictly.

Under no circumstances will the grade be adjusted or a re-exam allowed if caught !

Lecture: 09/14/2015

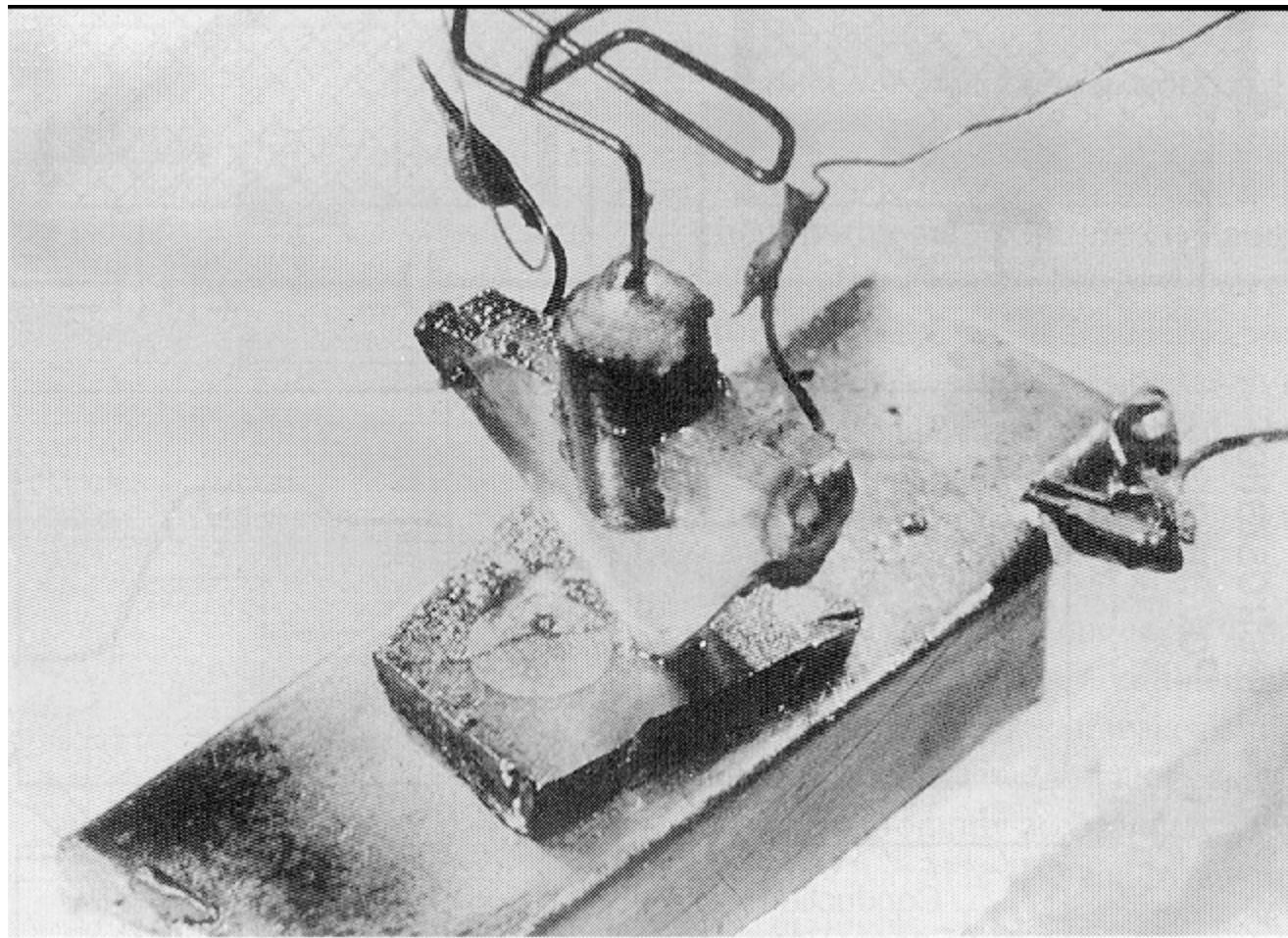
- Overview of VLSI Design
 - Historical perspectives
 - Challenges
 - Overall methodology
- Logic Design with MOSFETs
 - Basic gates
 - Transistor characteristics
- Introduction to Linux and Cadence (Jinesh Doshi)

Introduction

- Overview of VLSI Design
 - Historical perspectives
 - Challenges
 - Overall methodology

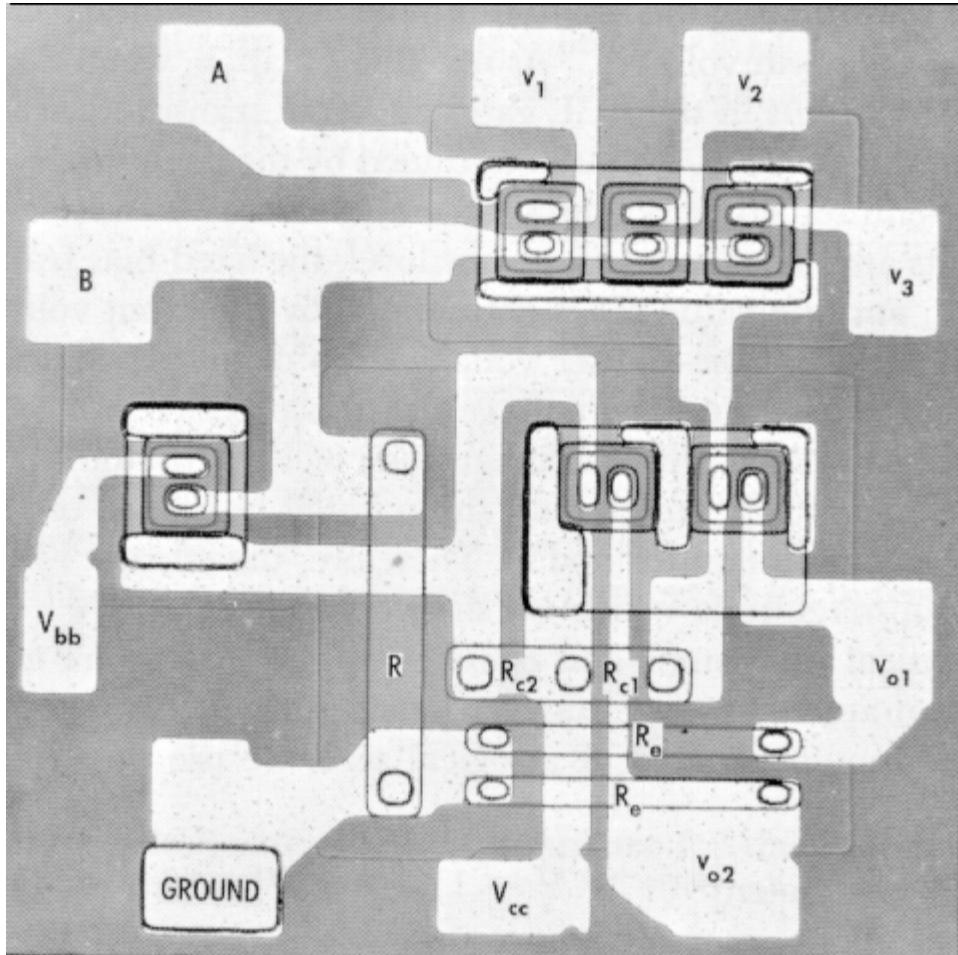
Slides borrowed from
Prof. Saibal Mukhopadhyay
ECE, Georgia Tech (2010)

The Transistor Revolution



First transistor
Bell Labs, 1948

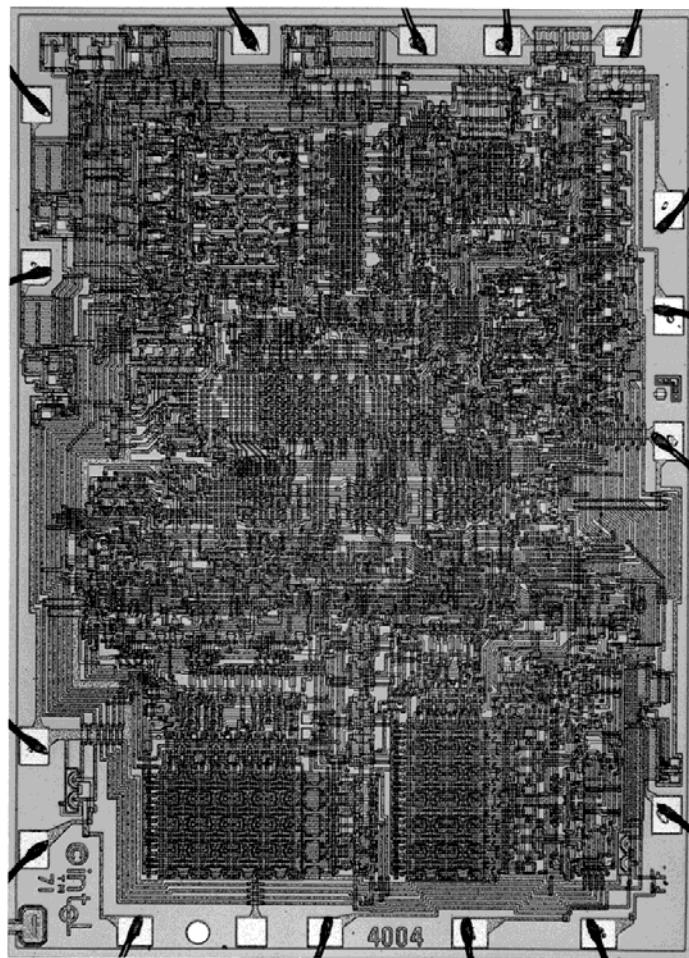
Early Integrated Circuits



*Bipolar logic
1960's*

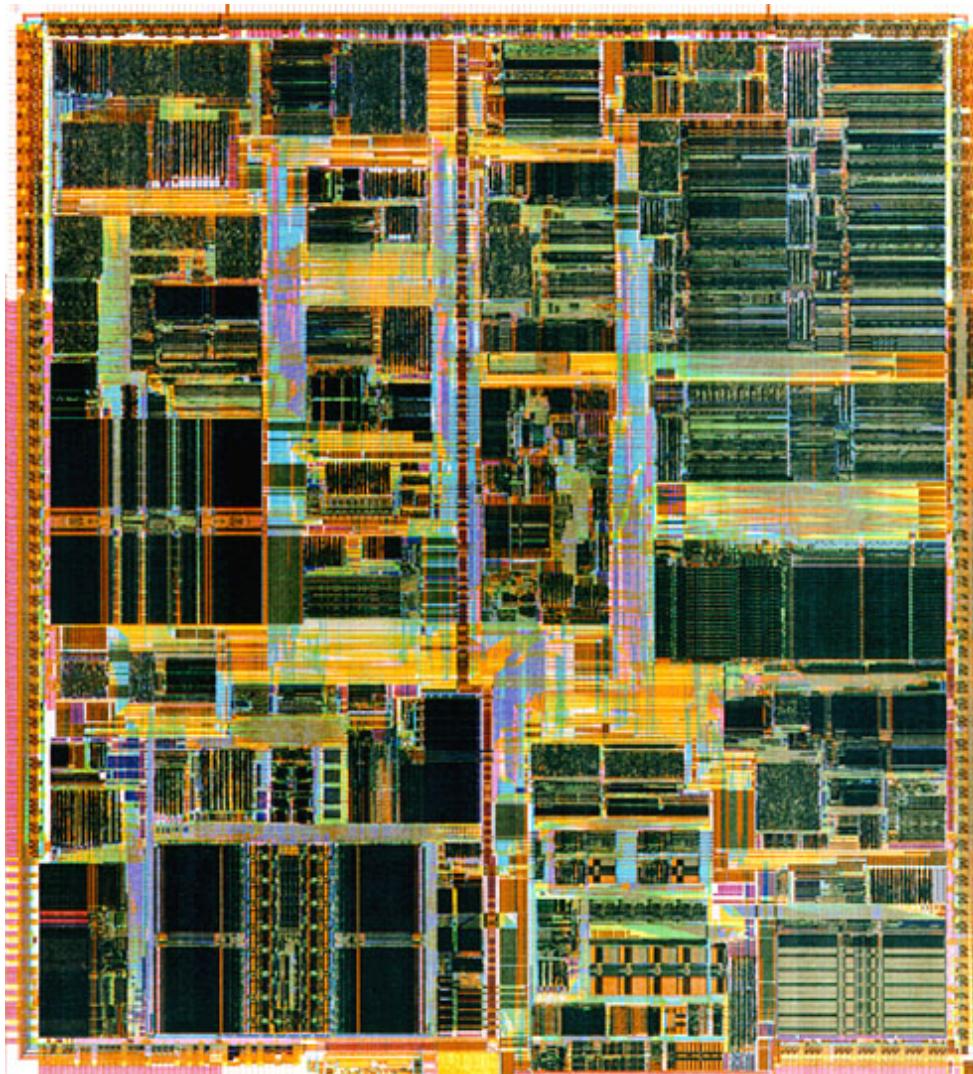
ECL 3-input Gate
Motorola 1966

Intel 4004 Micro-Processor



1971
1000 transistors
1 MHz operation

Intel Pentium (IV) microprocessor



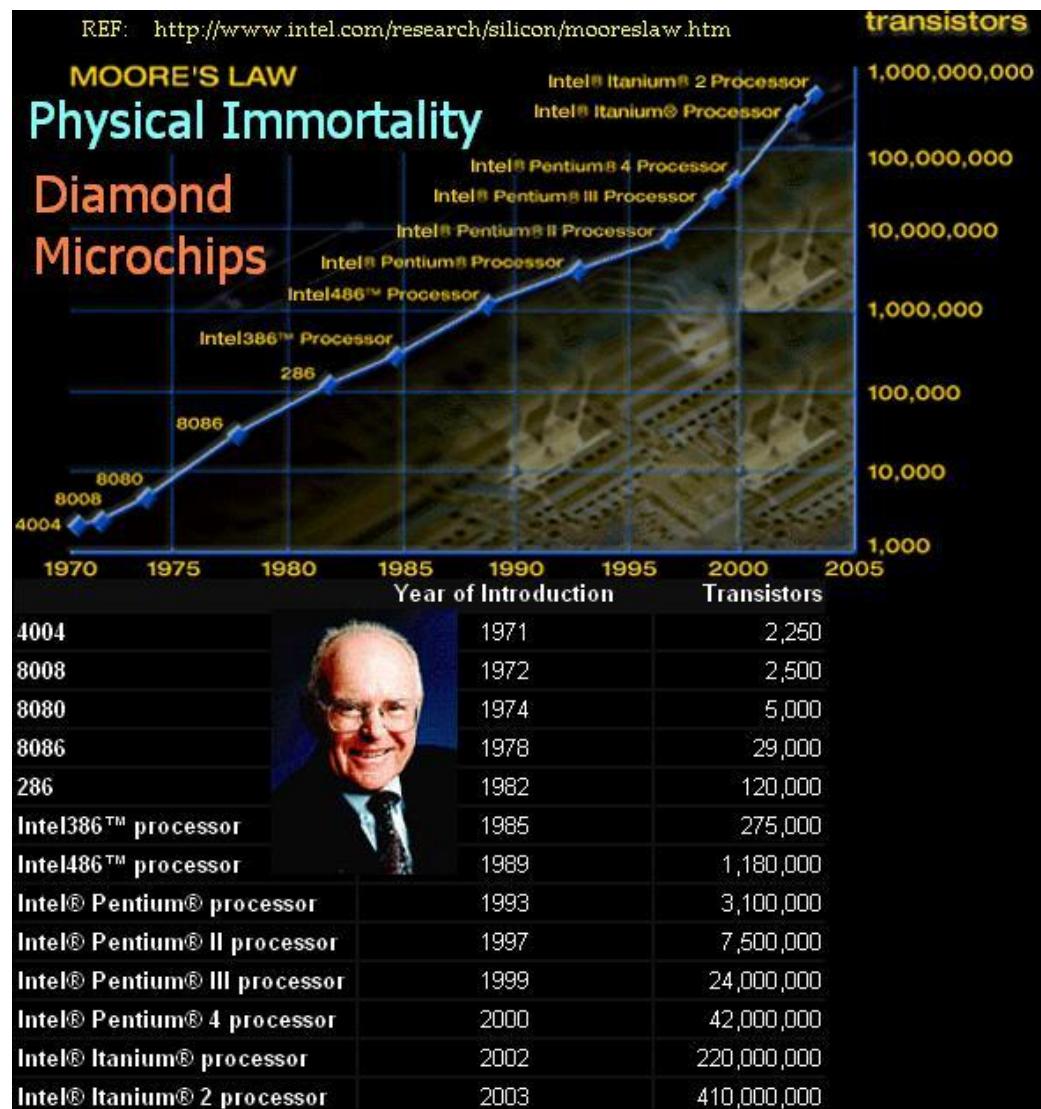
Moore's Law

- In 1965, Gordon Moore noted that the number of transistors on a chip doubled every 18 to 24 months.
- He made a prediction that semiconductor technology will double its effectiveness every 18 months

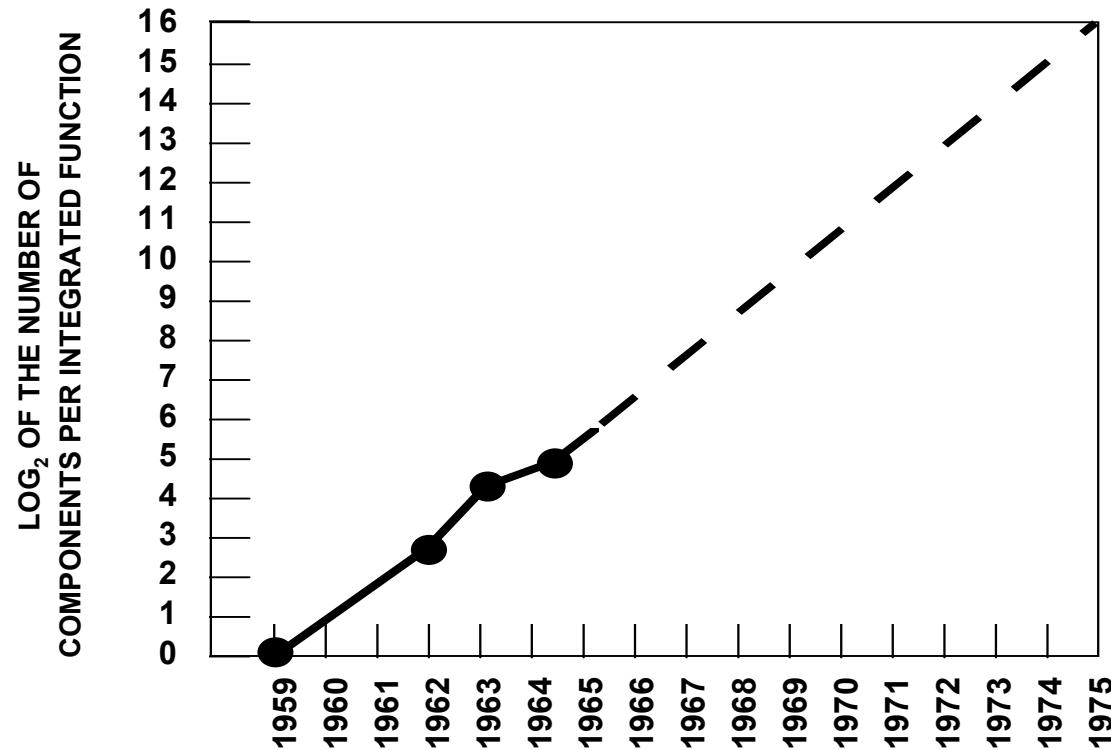
Moore's Law

“The complexity for minimum component costs has increased at a rate of roughly a factor of two per year ... Certainly over the short term this rate can be expected to continue, if not to increase. Over the longer term, the rate of increase is a bit more uncertain, although there is no reason to believe it will not remain nearly constant for at least 10 years. ”

**Electronics Magazine, 19 April
1965**

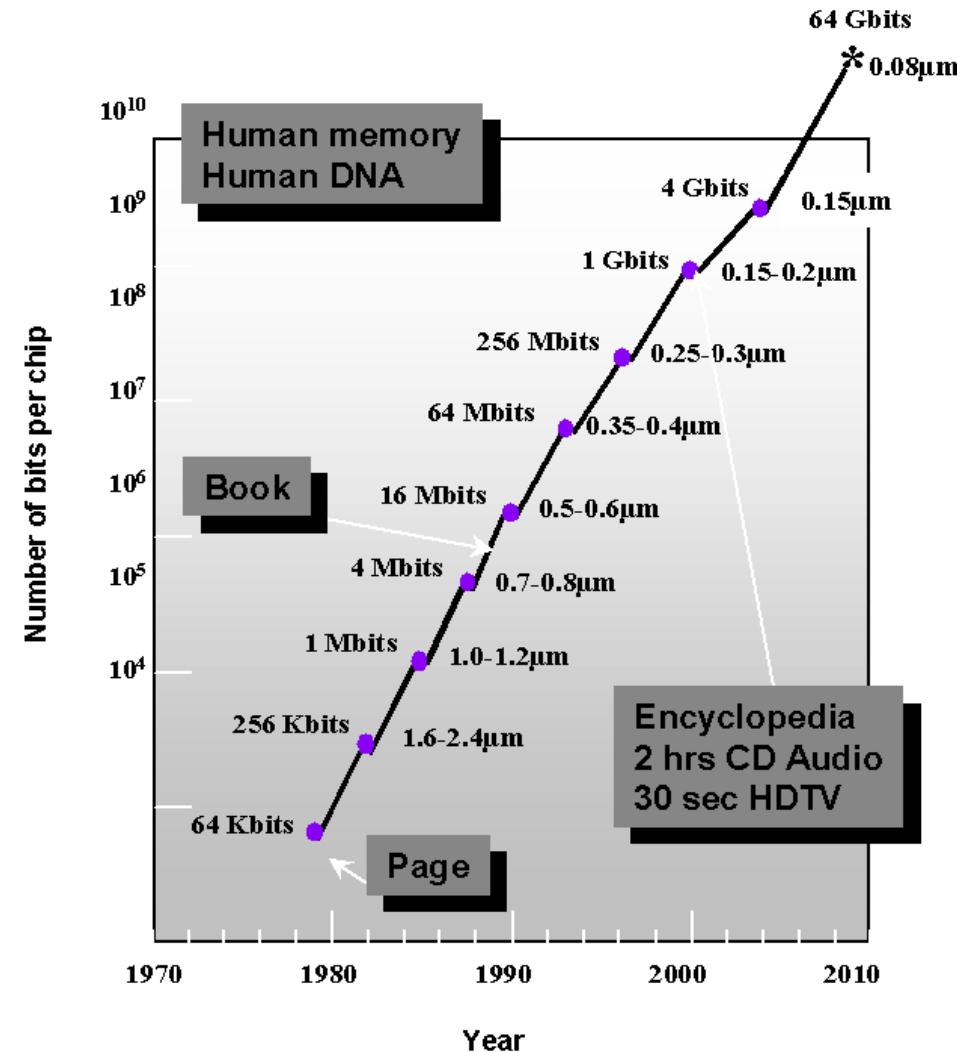


Moore's Law

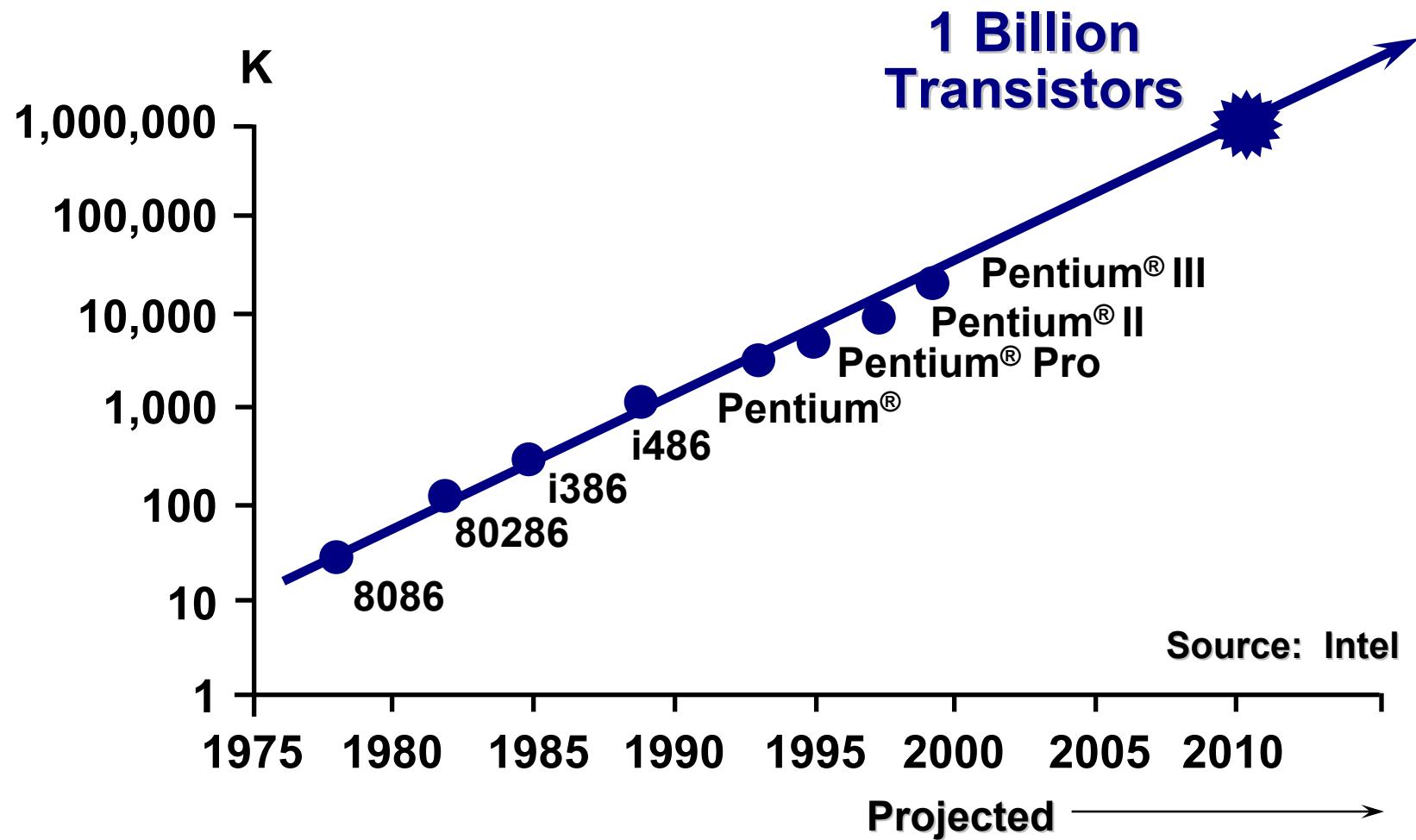


Electronics, April 19, 1965.

Evolution in Complexity

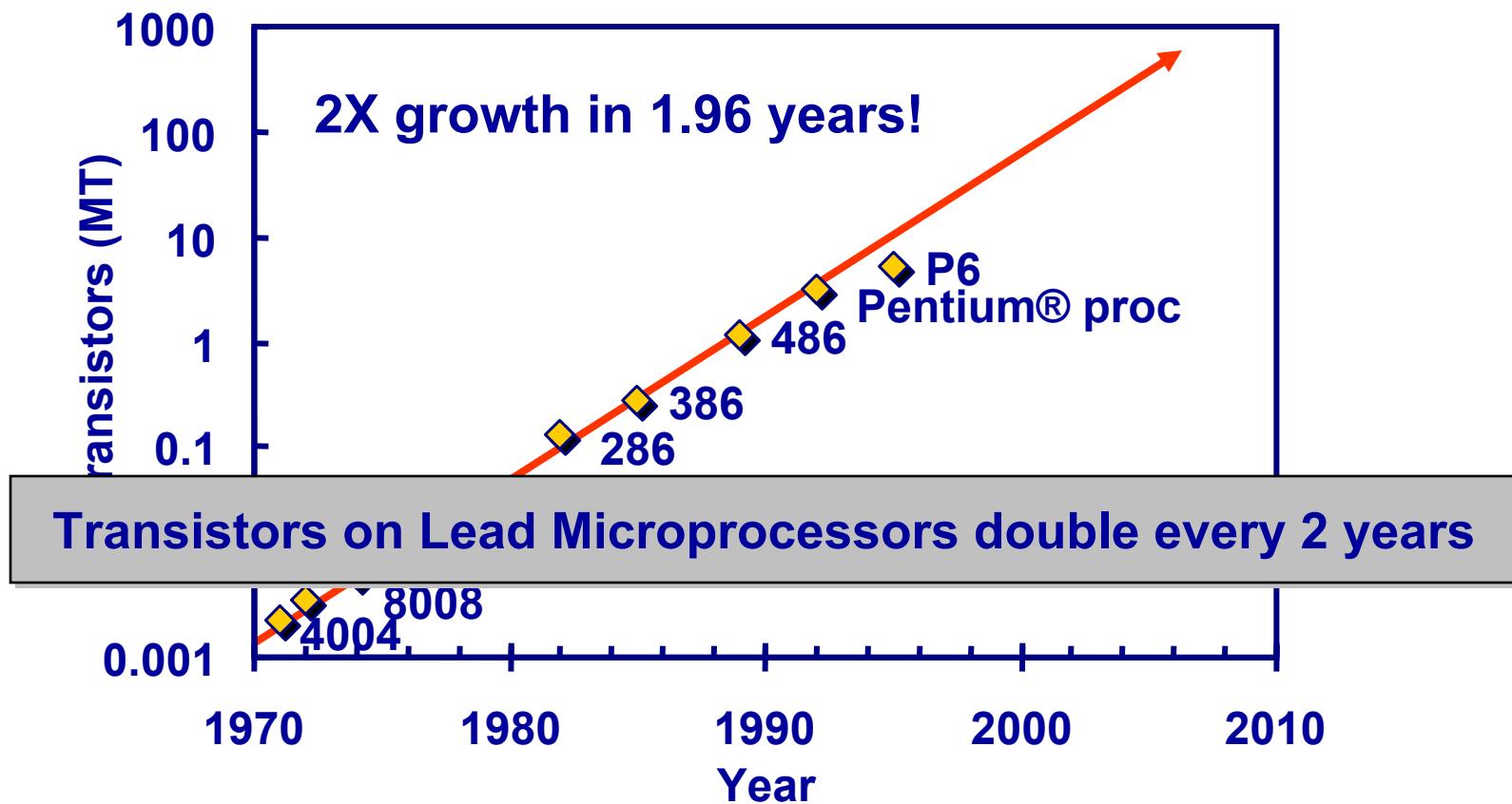


Transistor Counts



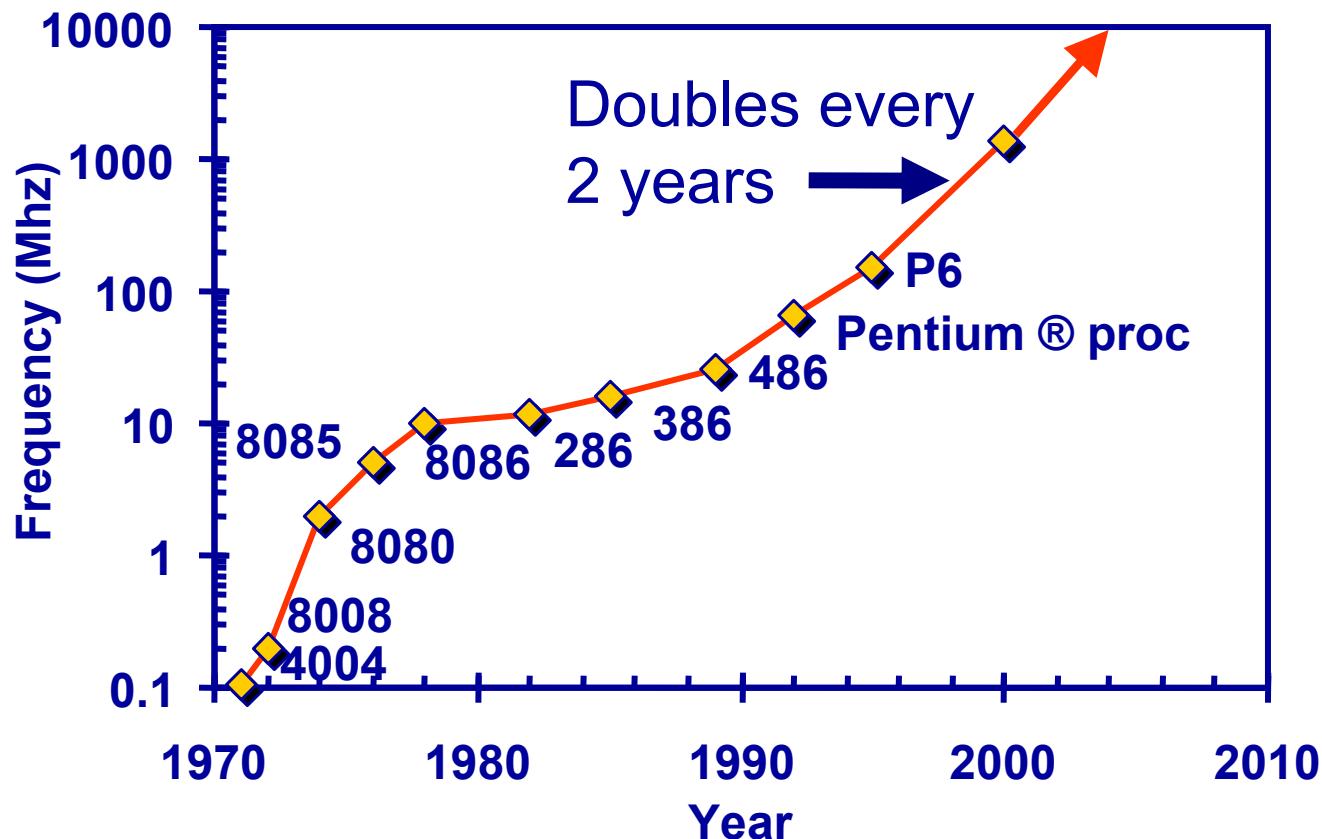
Courtesy, Intel

Moore's law in Microprocessors



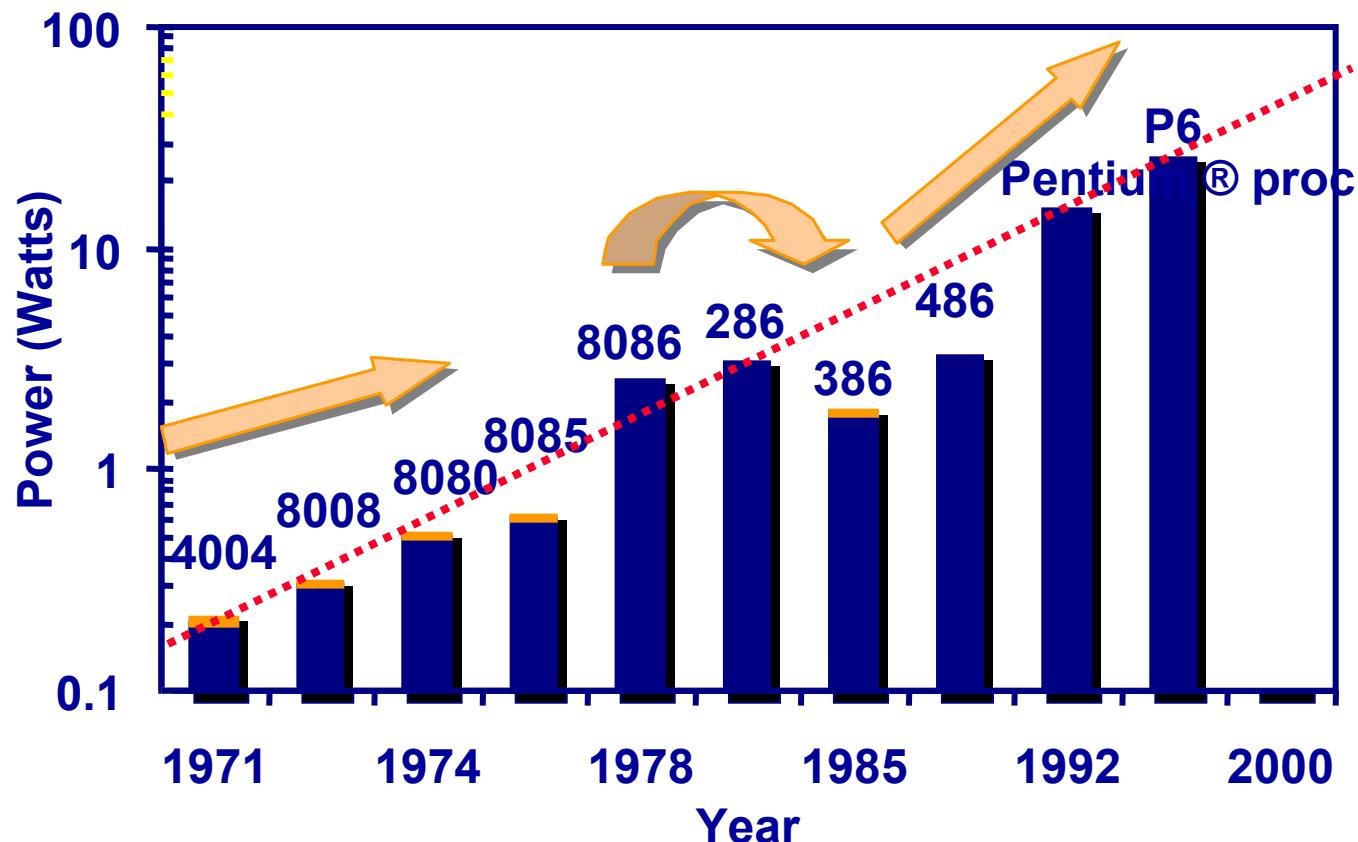
Courtesy, Intel

Frequency



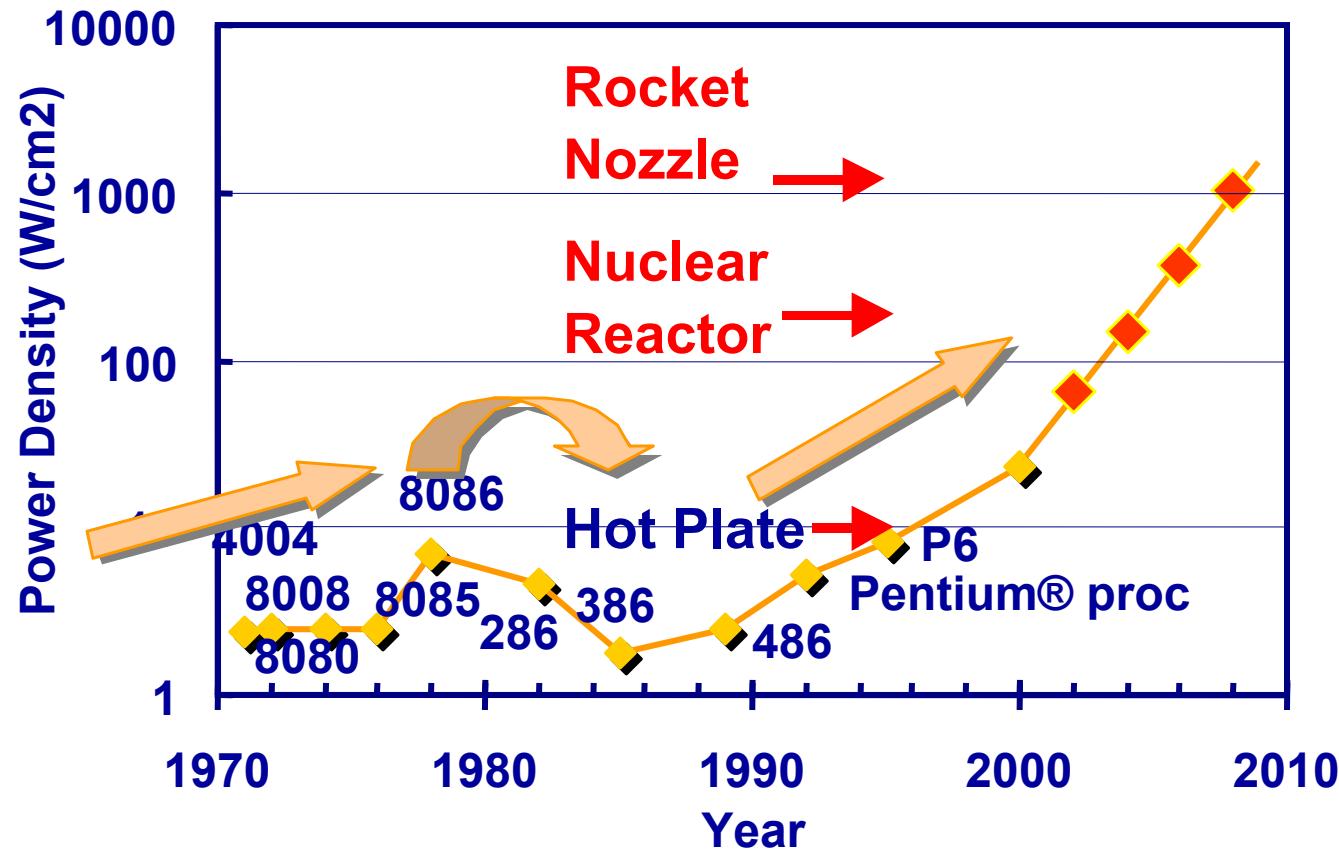
Lead Microprocessors frequency doubles every 2 years

Power Dissipation



Lead Microprocessors power continues to increase

Power density



Power density too high to keep junctions at low temp

Courtesy, Intel

Not Only Microprocessors

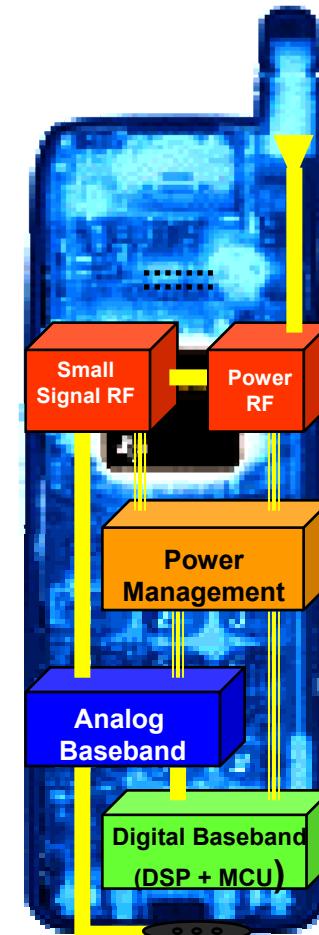
Cell
Phone



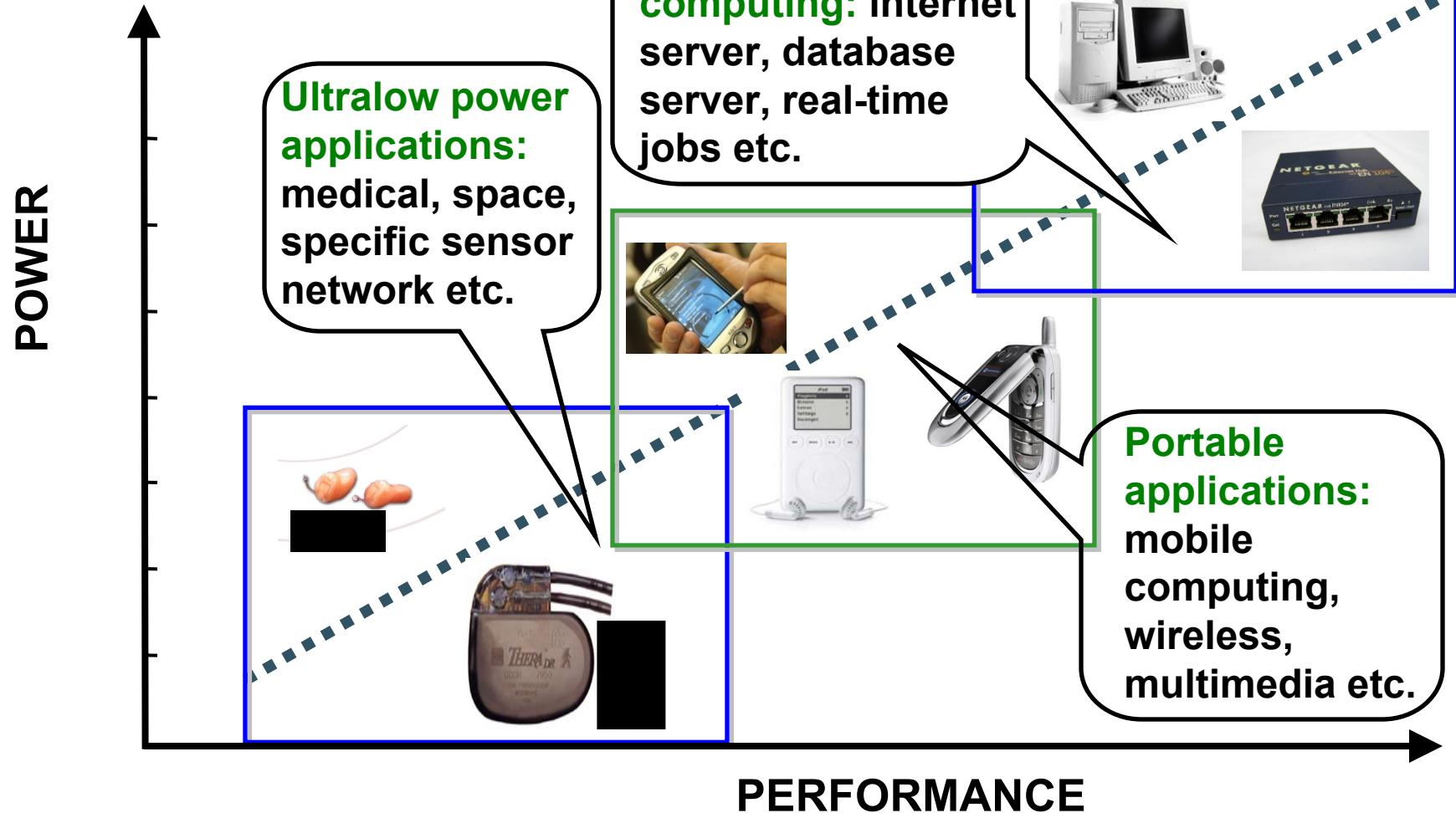
Digital Cellular Market
(Phones Shipped)

	1996	1997	1998	1999	2000
Units	48M	86M	162M	260M	435M

(data from Texas Instruments)

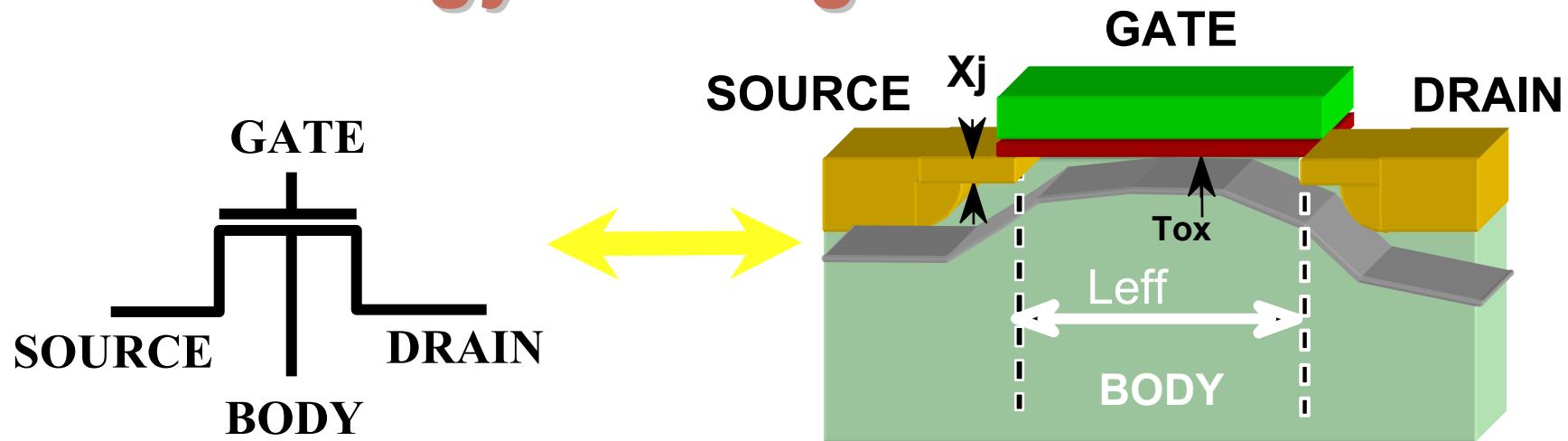


VLSI Applications



- Different applications have different power-performance demands

Technology Scaling



Dimensions scale down by 30%	Doubles transistor density
Oxide thickness scales down	Faster transistor, higher performance
Vdd & Vt scaling	Lower active power

Technology Scaling

Technology scaling improves:

- Transistor performance
- Transistor density
- Energy consumed per switching transition

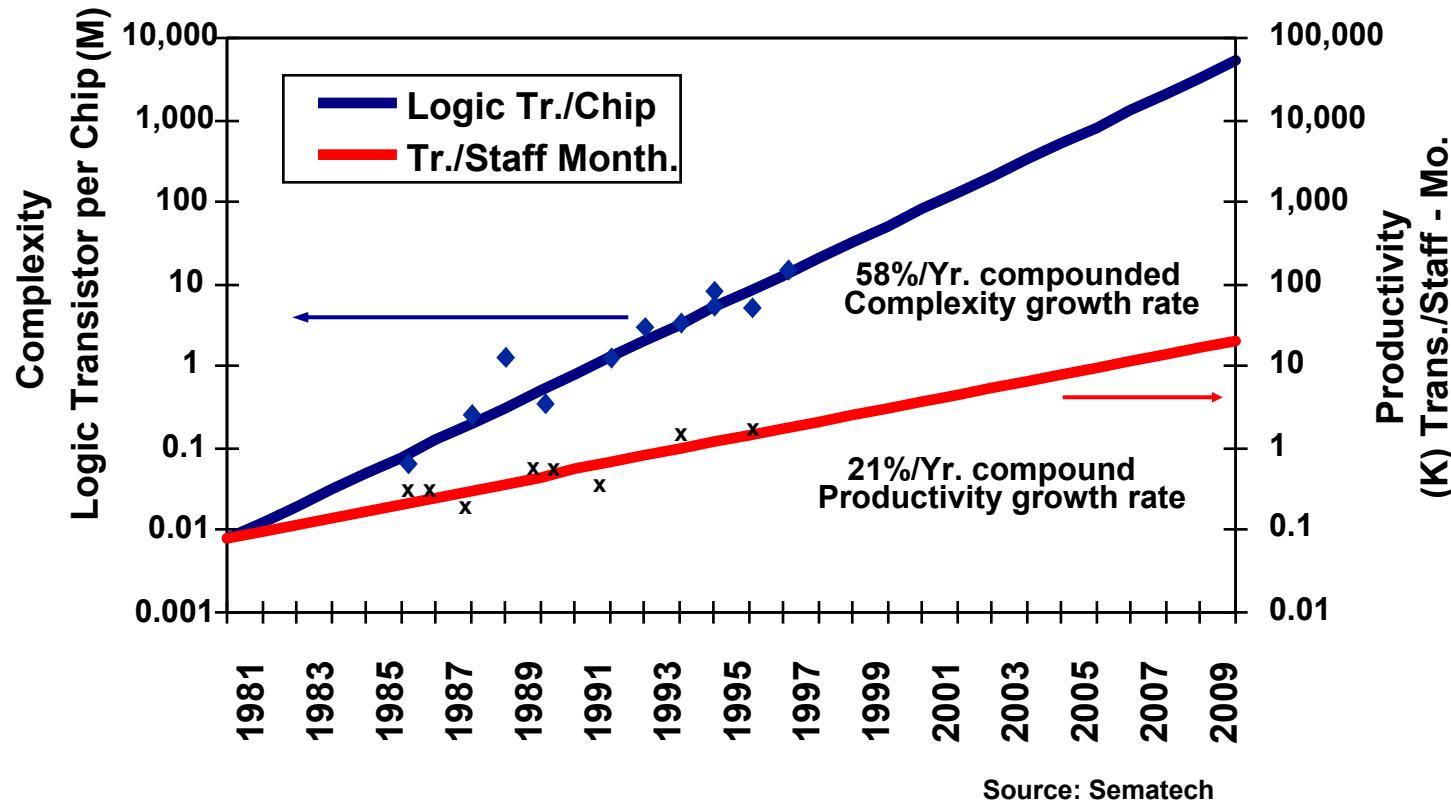
0.7X scaling factor (30% scaling) results in:

- 30% gate delay reduction (43% freq. ↑)
- 2X transistor density increase (49% area ↓)
- Energy per transition reduction

Why Scaling?

- Technology shrinks by 0.7/generation
- With every generation can integrate 2x more functions per chip; chip cost does not increase significantly
- Cost of a function decreases by 2x
- But
 - How to design chips with more and more functions?
 - Design engineering population does not double every two years
- Hence, a need for more efficient design methods
 - Exploit different levels of abstraction

Productivity Trends



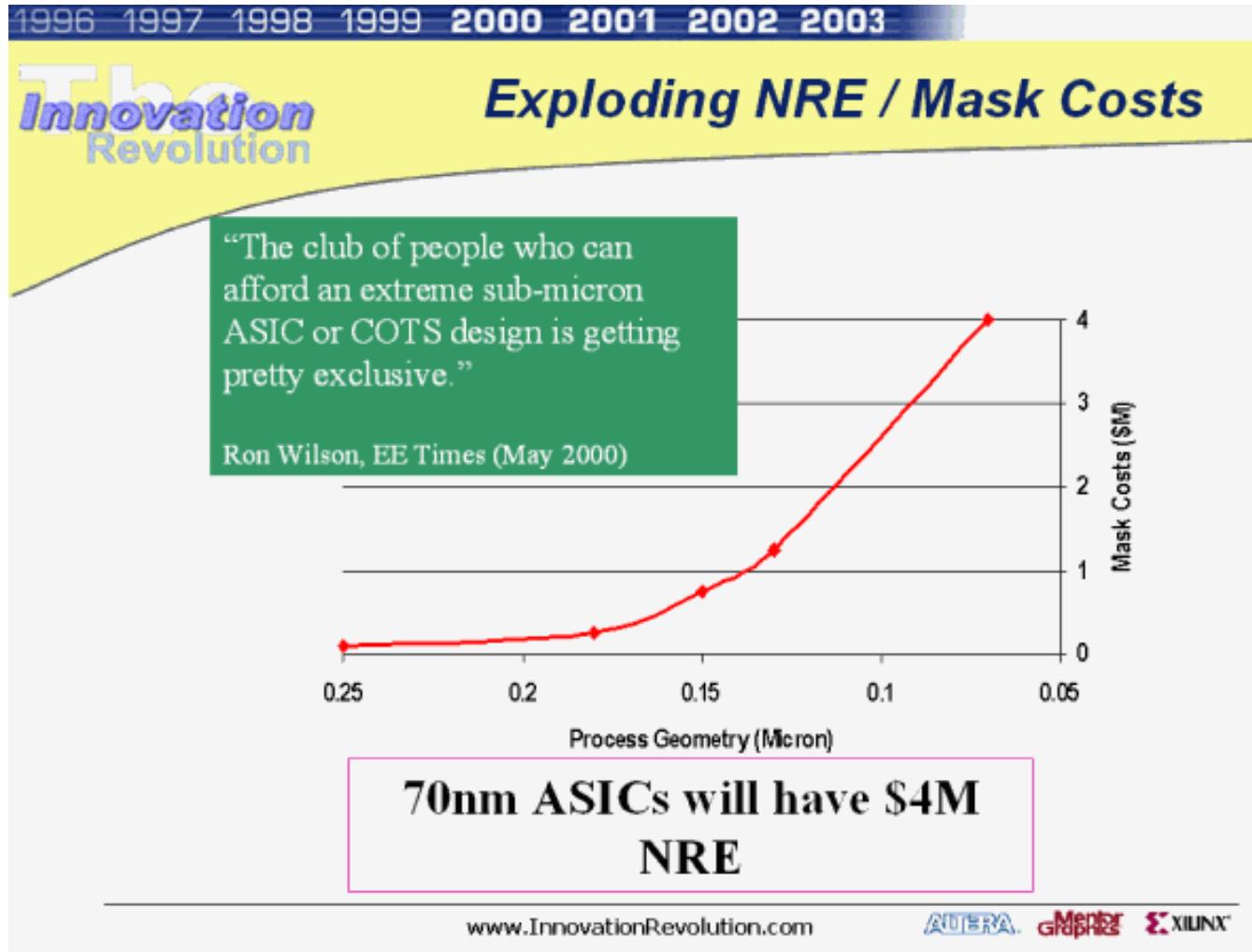
Complexity outpaces design productivity

Courtesy, ITRS Roadmap

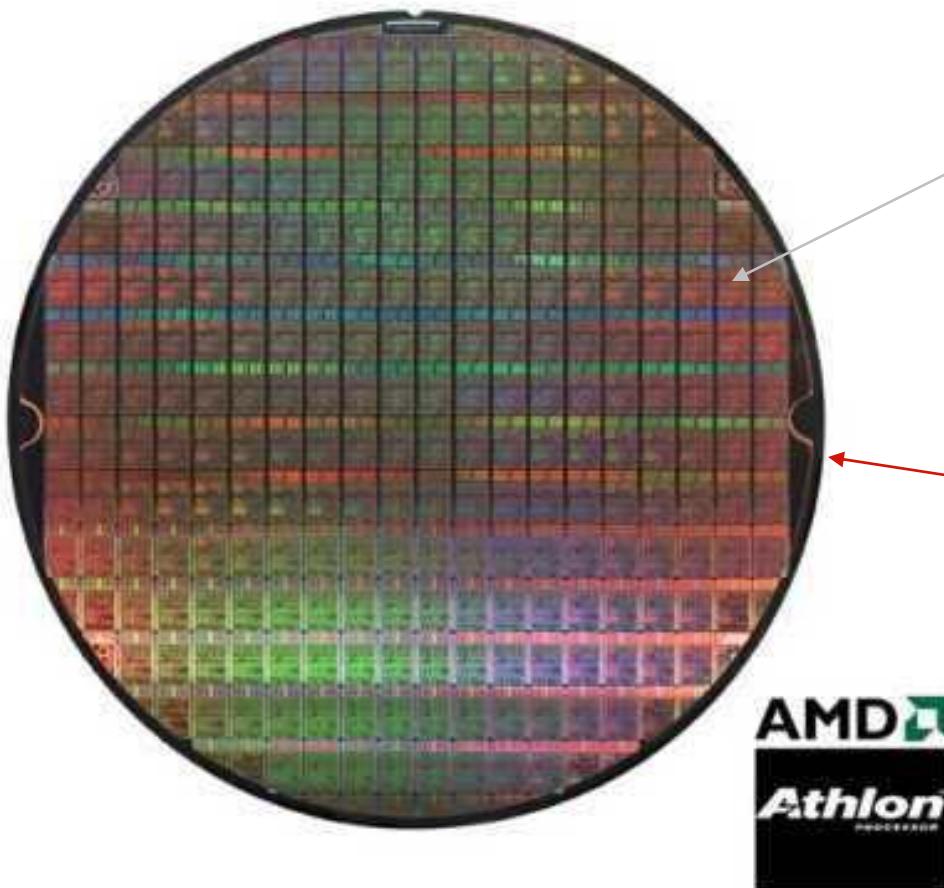
Cost of Integrated Circuits

- NRE (non-recurrent engineering) costs
 - design time and effort, mask generation
 - one-time cost factor
- Recurrent costs
 - silicon processing, packaging, test
 - proportional to volume
 - proportional to chip area

NRE Cost is Increasing



Die Cost

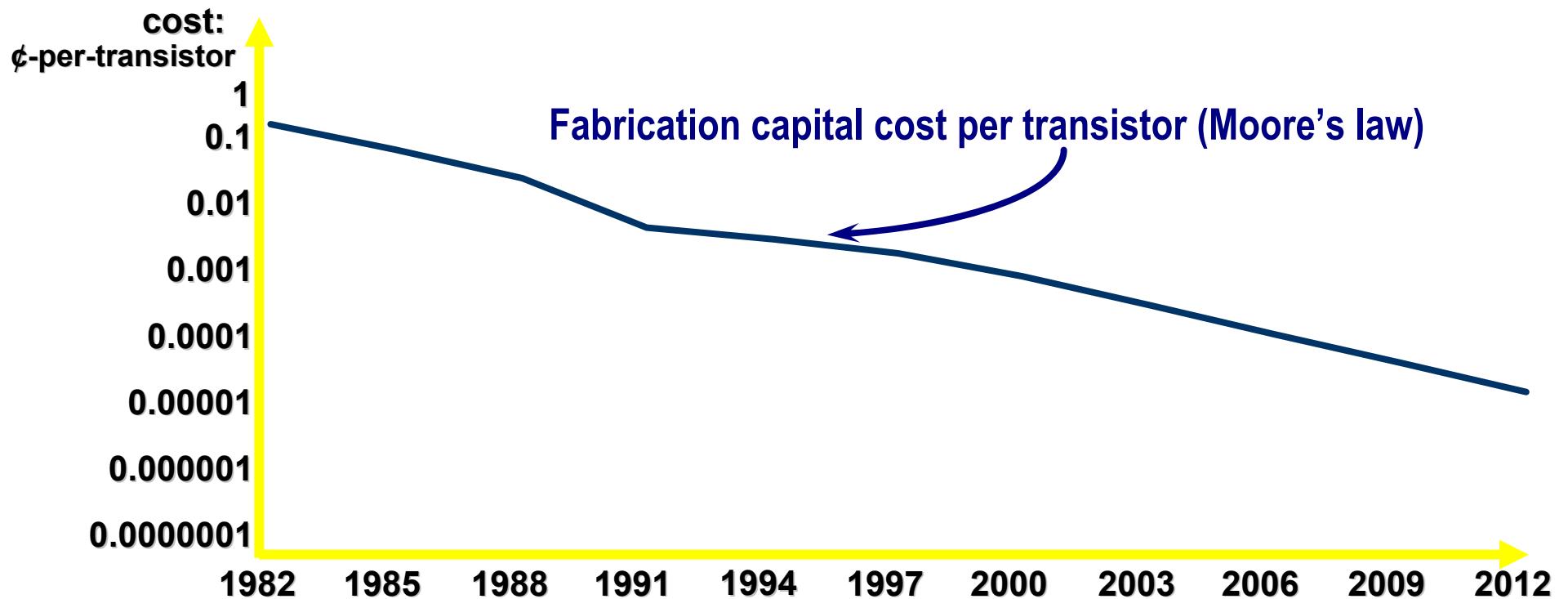


Single die

Wafer

Going up to 12" (30cm)

Cost per Transistor

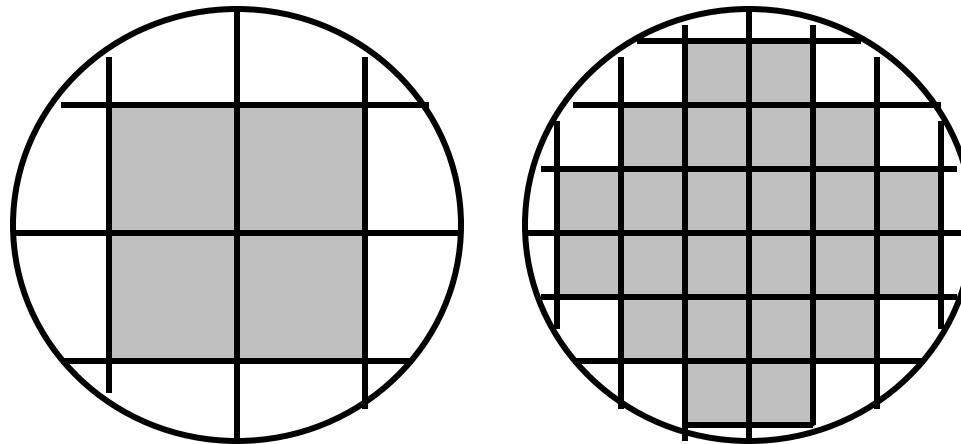


Yield

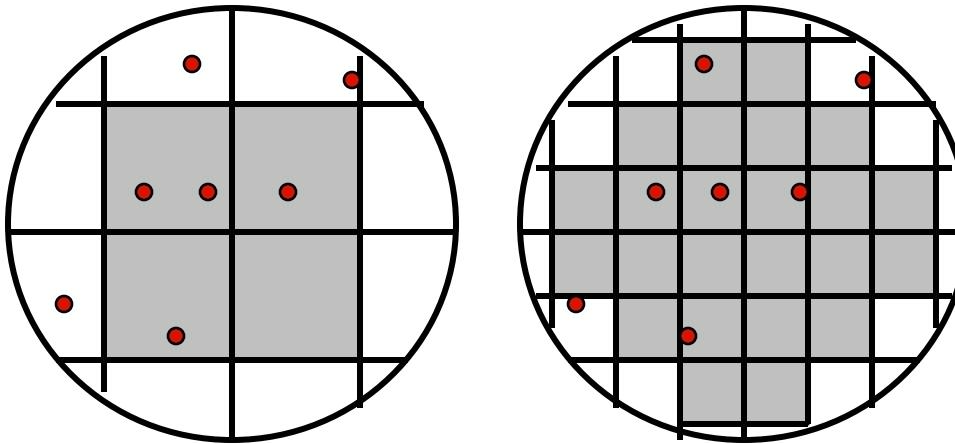
$$Y = \frac{\text{No. of good chips per wafer}}{\text{Total number of chips per wafer}} \times 100\%$$

$$\text{Die cost} = \frac{\text{Wafer cost}}{\text{Dies per wafer} \times \text{Die yield}}$$

$$\text{Dies per wafer} = \frac{\pi \times (\text{wafer diameter}/2)^2}{\text{die area}} - \frac{\pi \times \text{wafer diameter}}{\sqrt{2} \times \text{die area}}$$



Defects

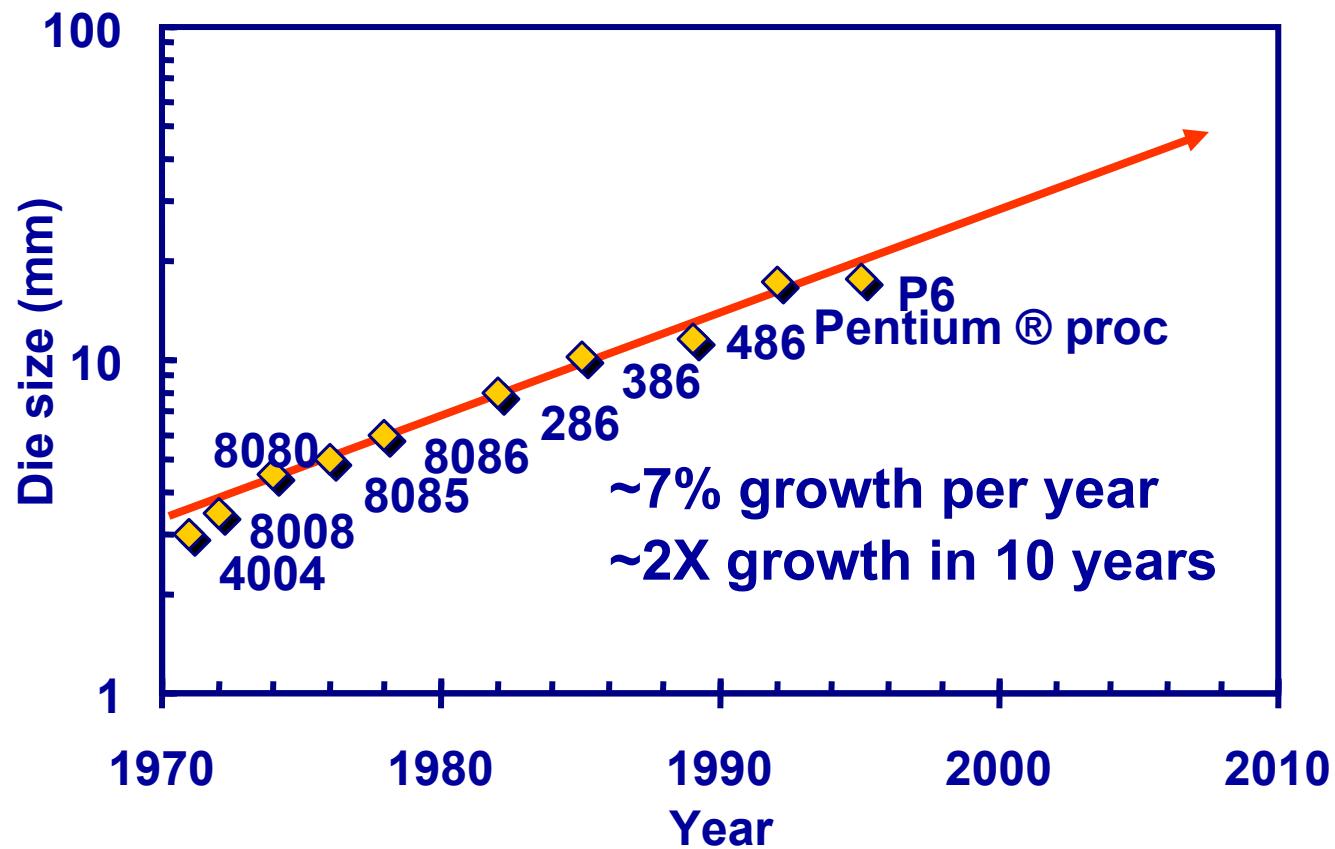


$$\text{die yield} = \left(1 + \frac{\text{defects per unit area} \times \text{die area}}{\alpha} \right)^{-\alpha}$$

α is approximately 3

$$\text{die cost} = f(\text{die area})^4$$

Die Size Growth



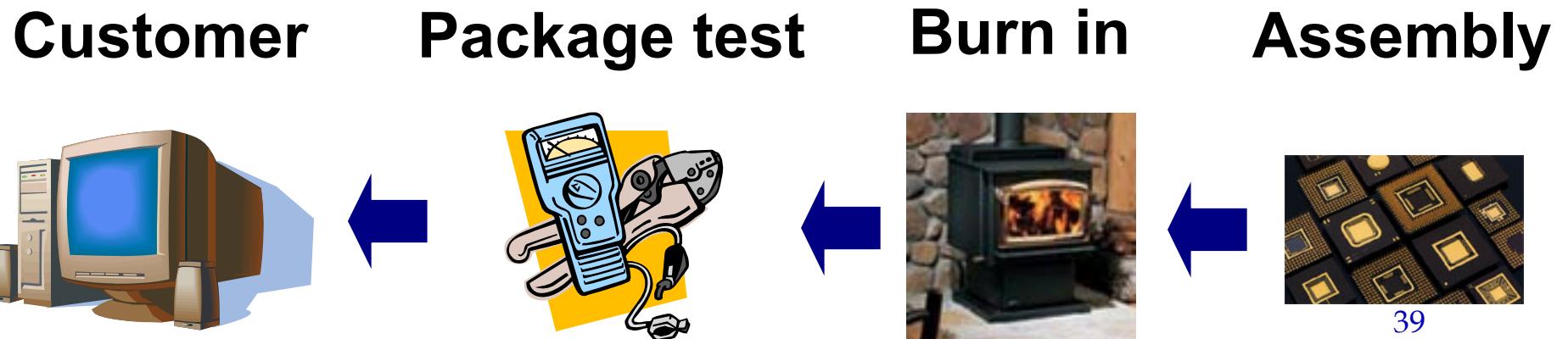
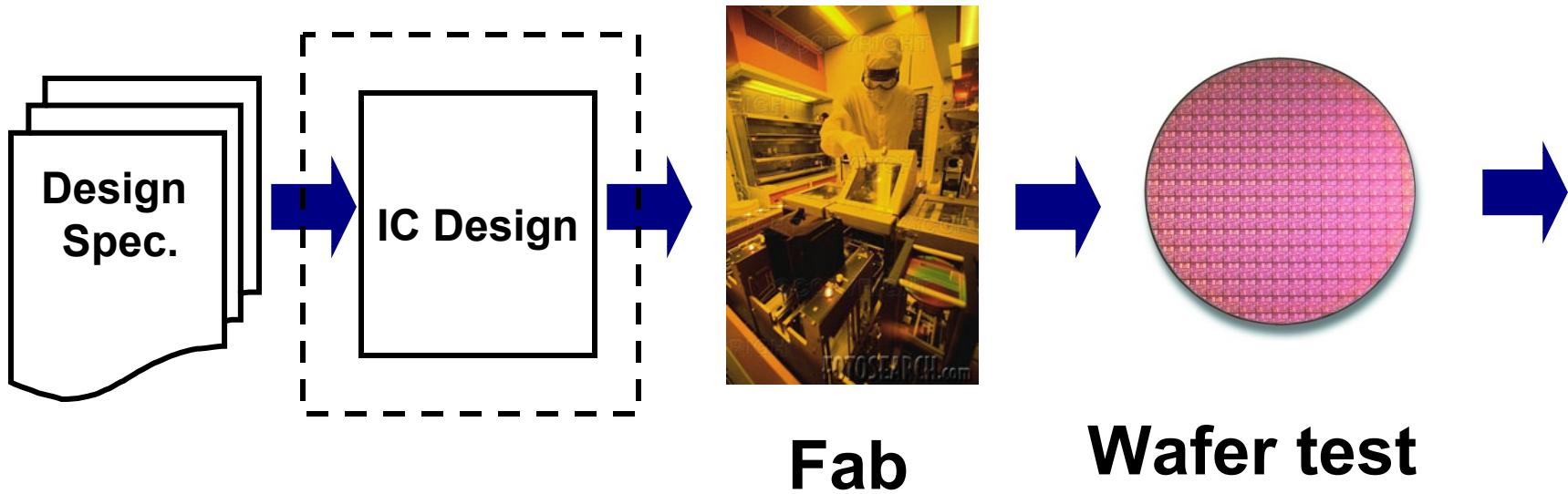
Die size grows by 14% to satisfy Moore's Law

Courtesy, Intel

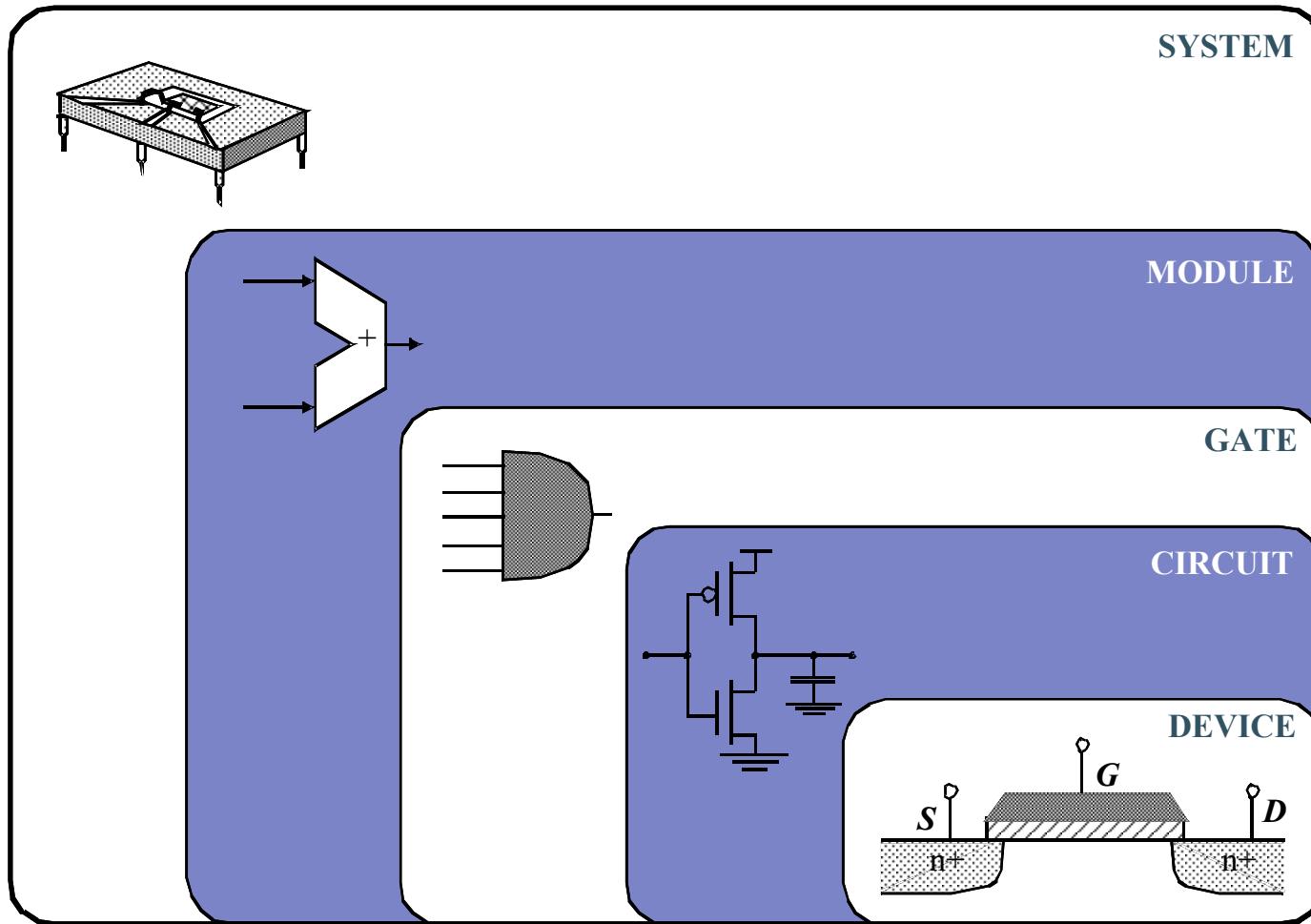
Design Metrics

- How to evaluate performance of a digital circuit (gate, block,)?
 - Cost
 - Reliability
 - Scalability
 - Speed (delay, operating frequency)
 - Power dissipation
 - Energy to perform a function

IC Design and Test Flow

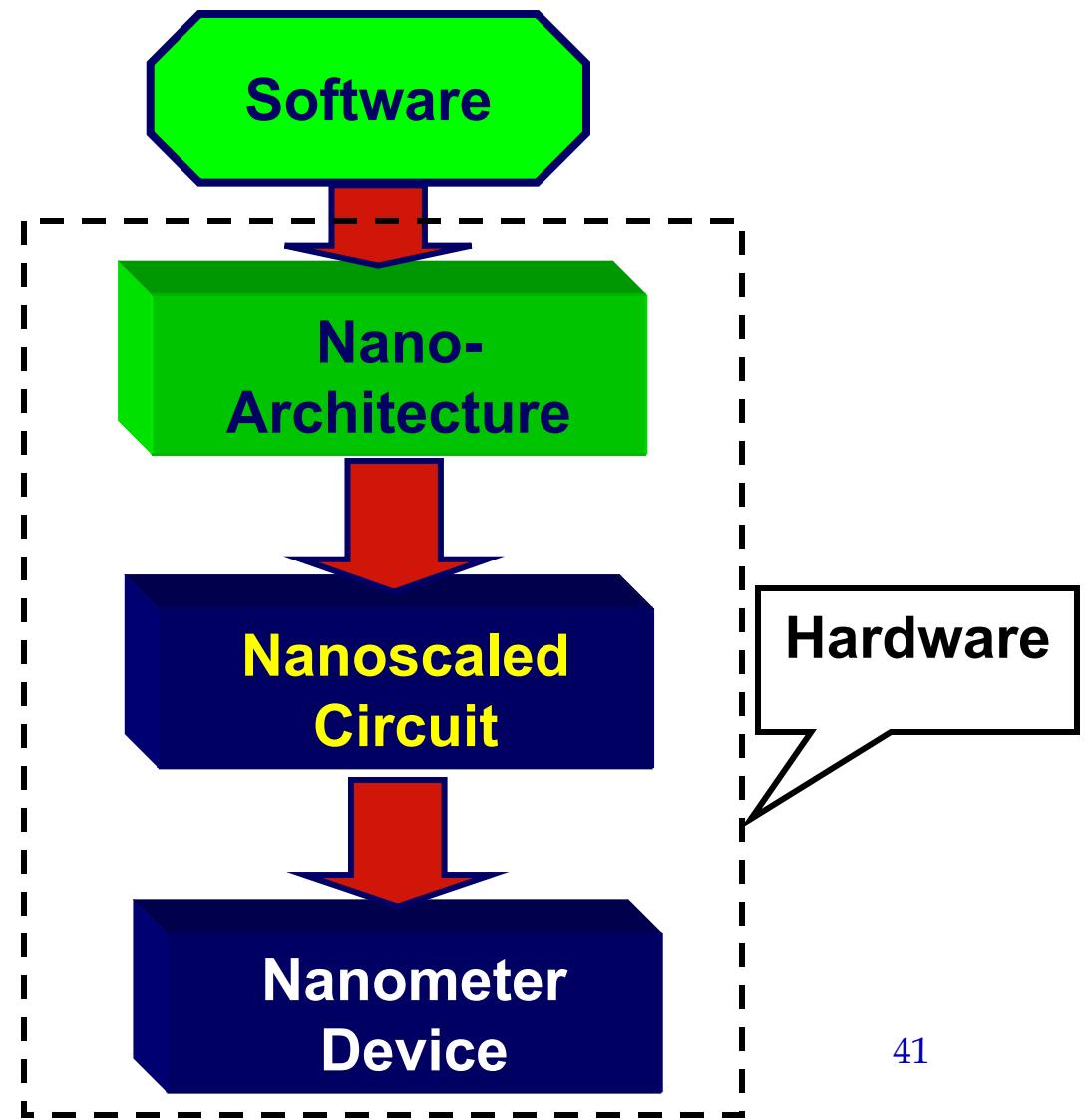


Design Abstraction Levels

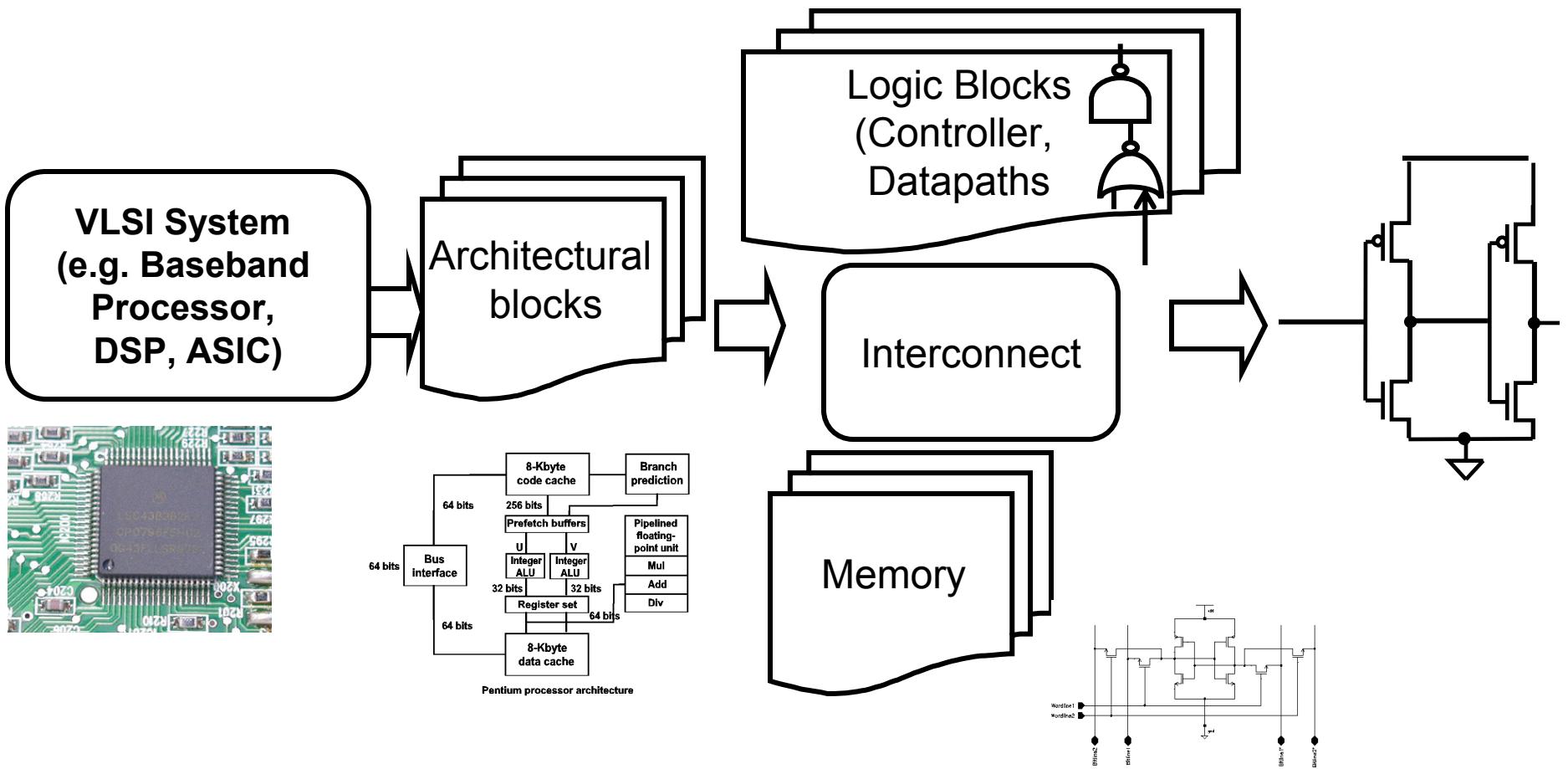


VLSI System Design

- Different levels of abstraction
- An optimal system design requires hardware/software co-design



VLSI Systems



System -> Architecture -> Logic -> Transistor

General Overview of the Design Hierarchy.

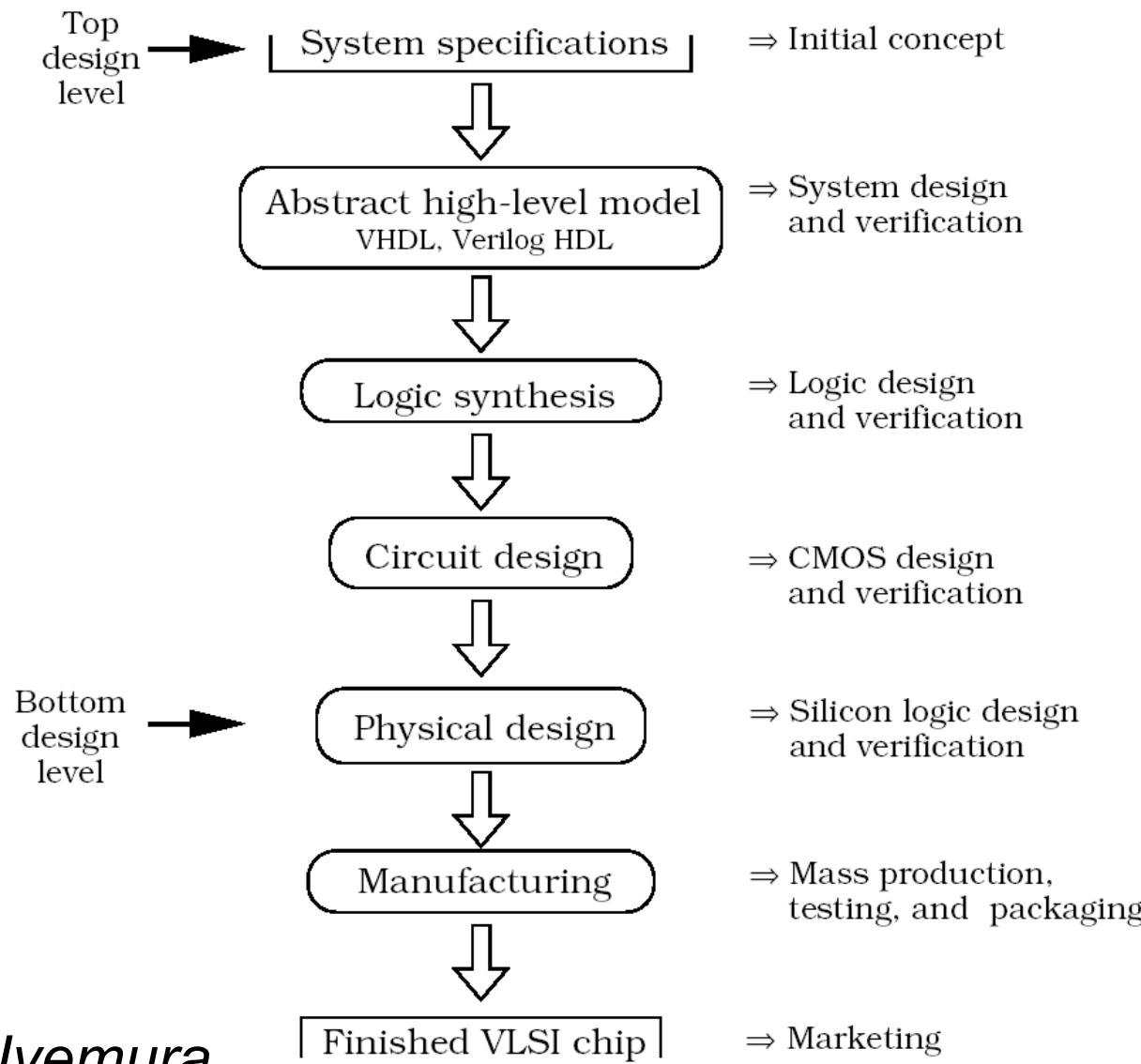


Fig. 1.2, Uyemura

A Simple Design Flow for a Microprocessor

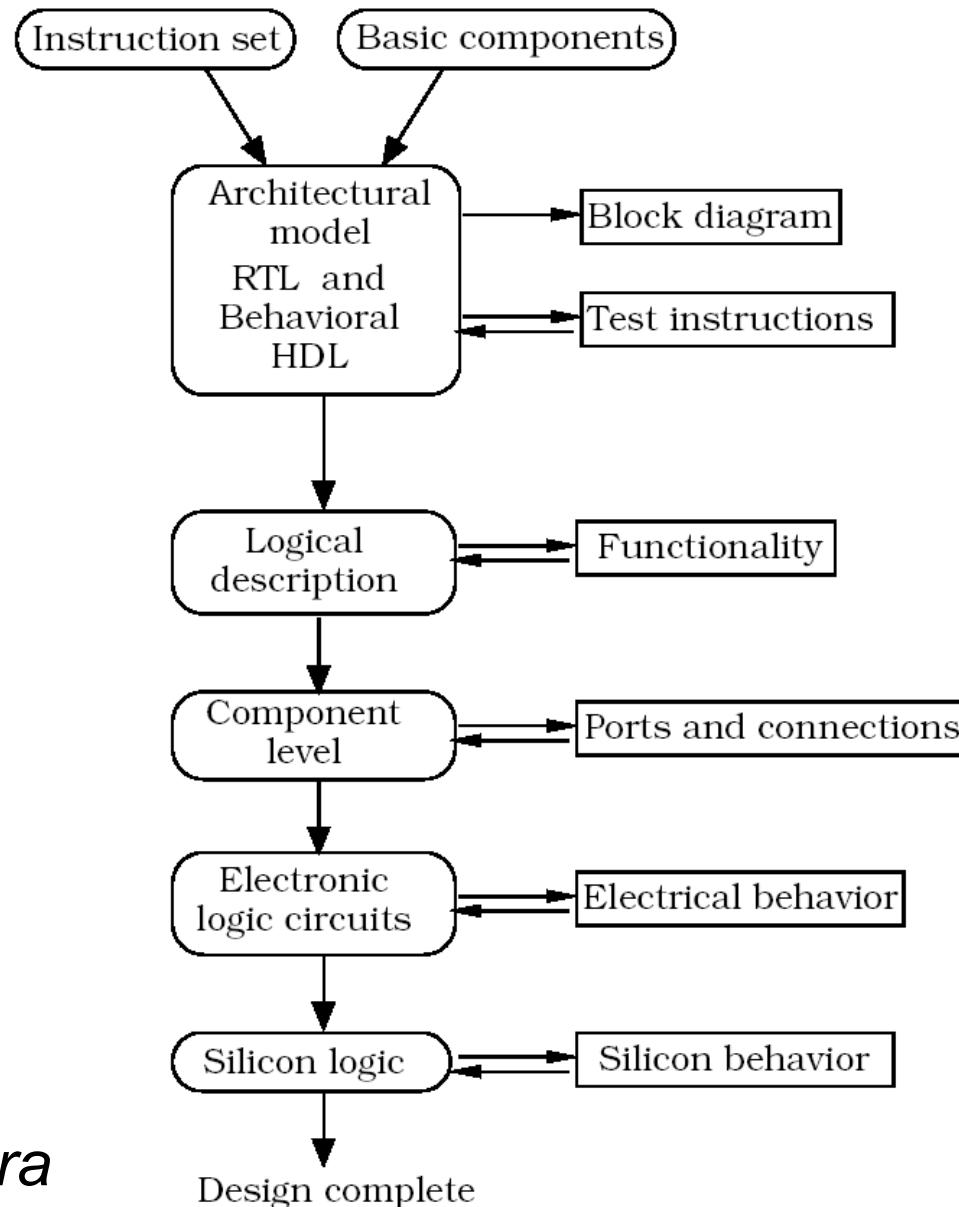


Fig. 1.3, Uyemura

Challenges in Digital Design

“Microscopic Problems”

- Ultra-high speed design
- Interconnect
- Noise, Crosstalk
- Reliability, Manufacturability
- Power Dissipation
- Clock distribution.

Everything Looks a Little Different



“Macroscopic Issues”

- Time-to-Market
- Millions of Gates
- High-Level Abstractions
- Reuse & IP: Portability
- Predictability
- etc.

and There's a Lot of Them!

Summary

- Digital integrated circuits have come a long way and still have quite some potential left for the coming decades
- Understanding the design metrics that govern digital design is crucial
 - Cost, reliability, speed, power and energy dissipation
- Understanding of the design hierarchy is essential
 - Each level of design abstraction is important in meeting the design spec.
- Some interesting challenges ahead
 - At the end of the course we aim to have a clear perspective of these challenges.

Logic design

In digital electronics, data is represented using only two logic states.

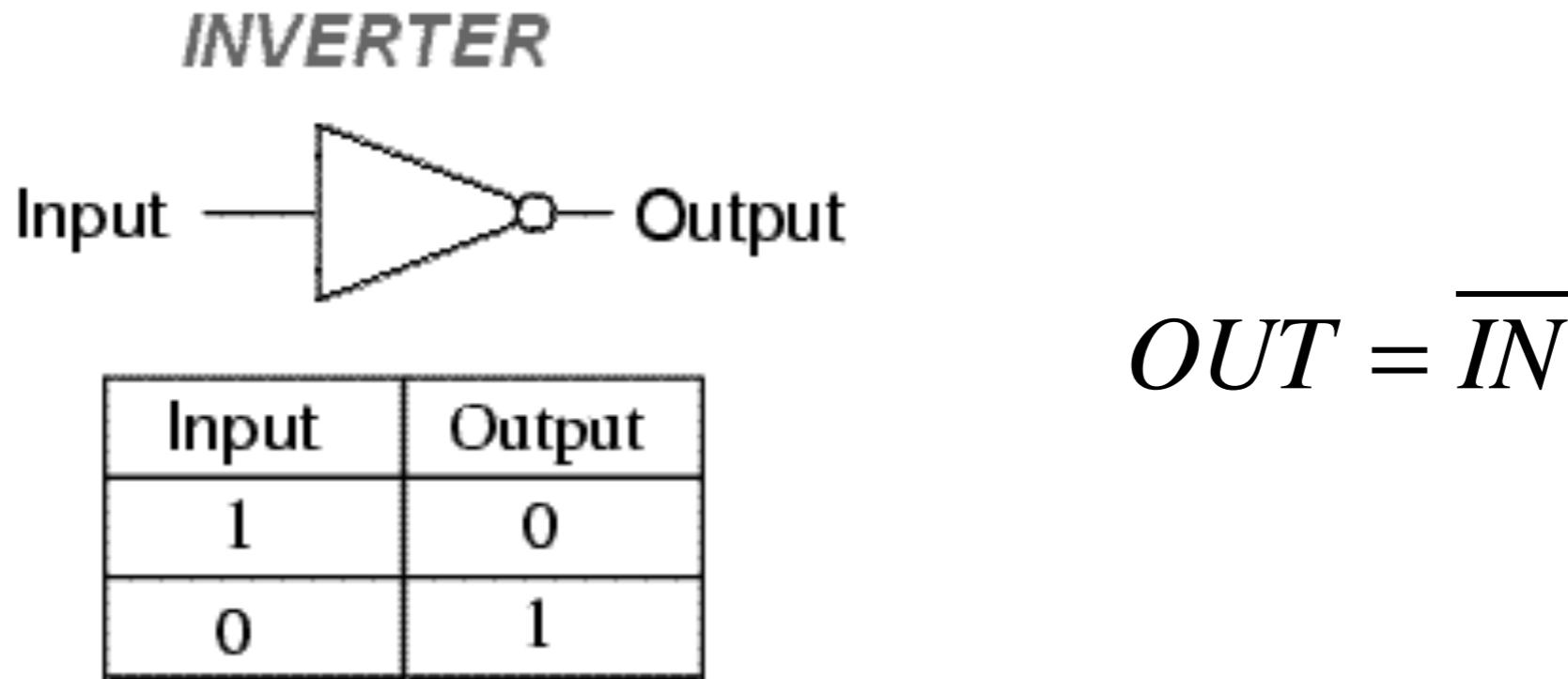
Logic “1” → HIGH (H)

Logic “0” → LOW (L)

A digital logic circuit consists of gates to implement Boolean logic.

Basic building blocks of digital logic: *Inverter, NAND, NOR gates.*

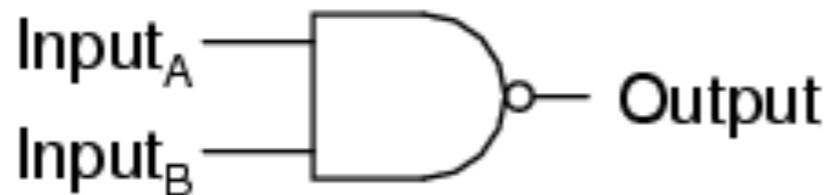
Inverter



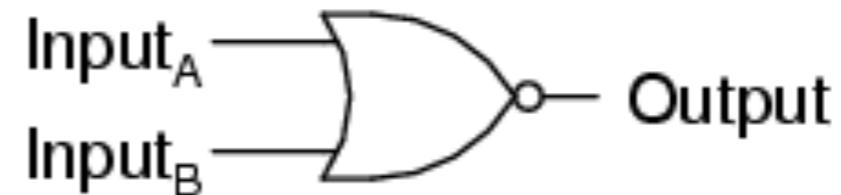
- Single input, single output gate.
- The gate inverts the input signal.
- At the physical level, digital “1” and “0” are simply voltages.

NAND and NOR

NAND gate



NOR gate



A	B	Output
0	0	1
0	1	1
1	0	1
1	1	0

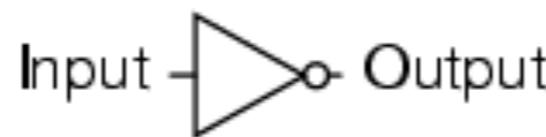
$$OUT = \overline{A \cdot B}$$

A	B	Output
0	0	1
0	1	0
1	0	0
1	1	0

$$OUT = \overline{\overline{A} + \overline{B}}$$

Inverter with NAND and NOR ?

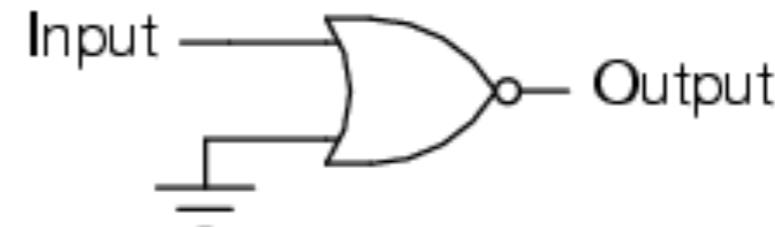
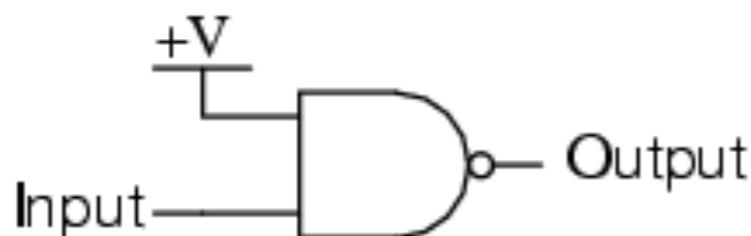
Inverter with *NAND* and *NOR* ?



Input	Output
0	1
1	0



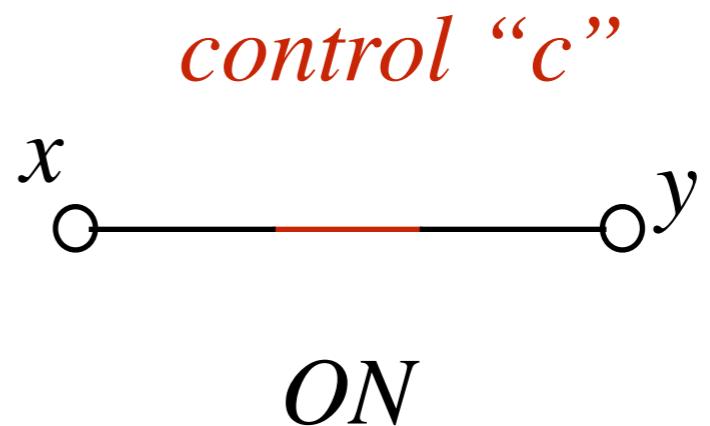
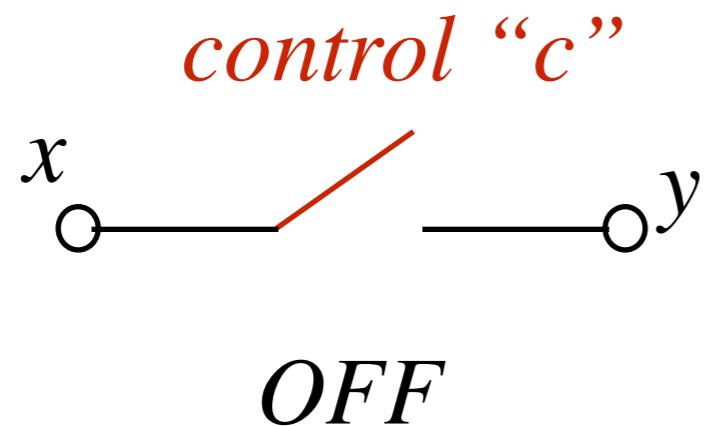
... or ...



Components of logic gates

Digital logic gates are composed of **transistors**.

Transistor is a voltage-controlled switch.



Components of logic gates

Digital logic gates are composed of **transistors**.

Transistor is a voltage-controlled switch.

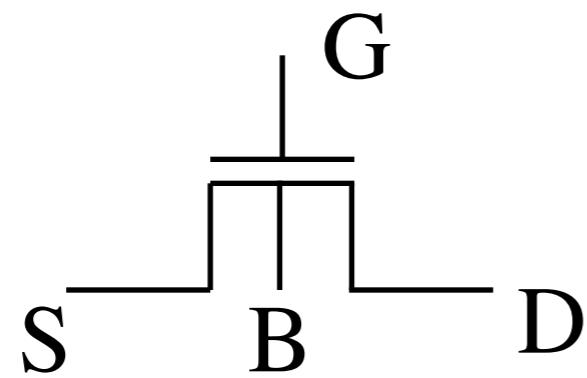


OFF

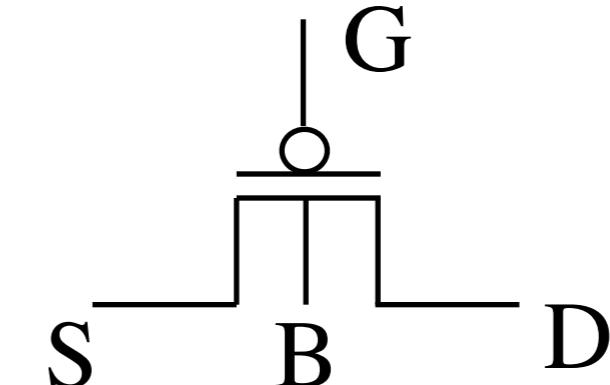


ON

MOSFET: metal oxide semiconductor field effect transistor

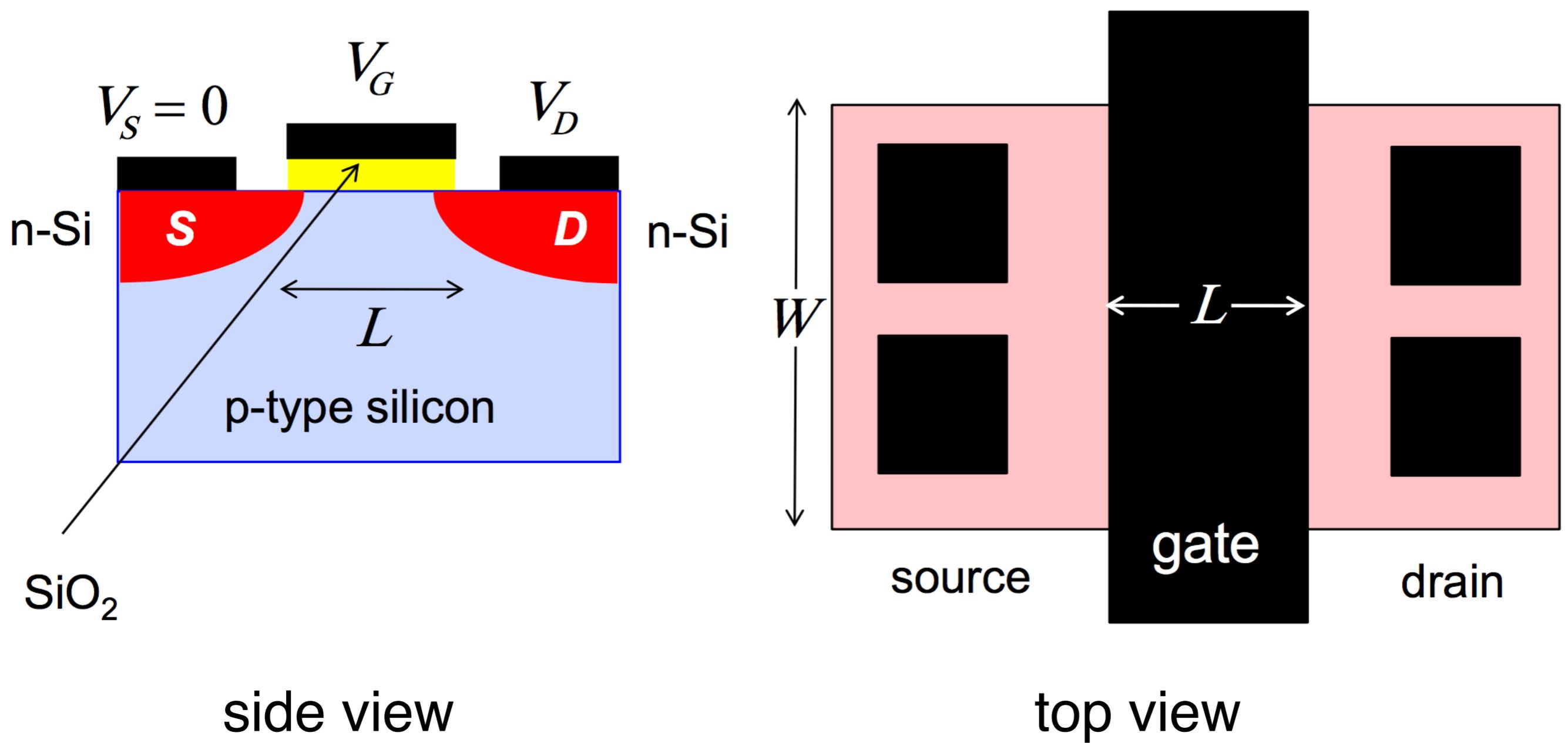


n-type MOSFET



p-type MOSFET

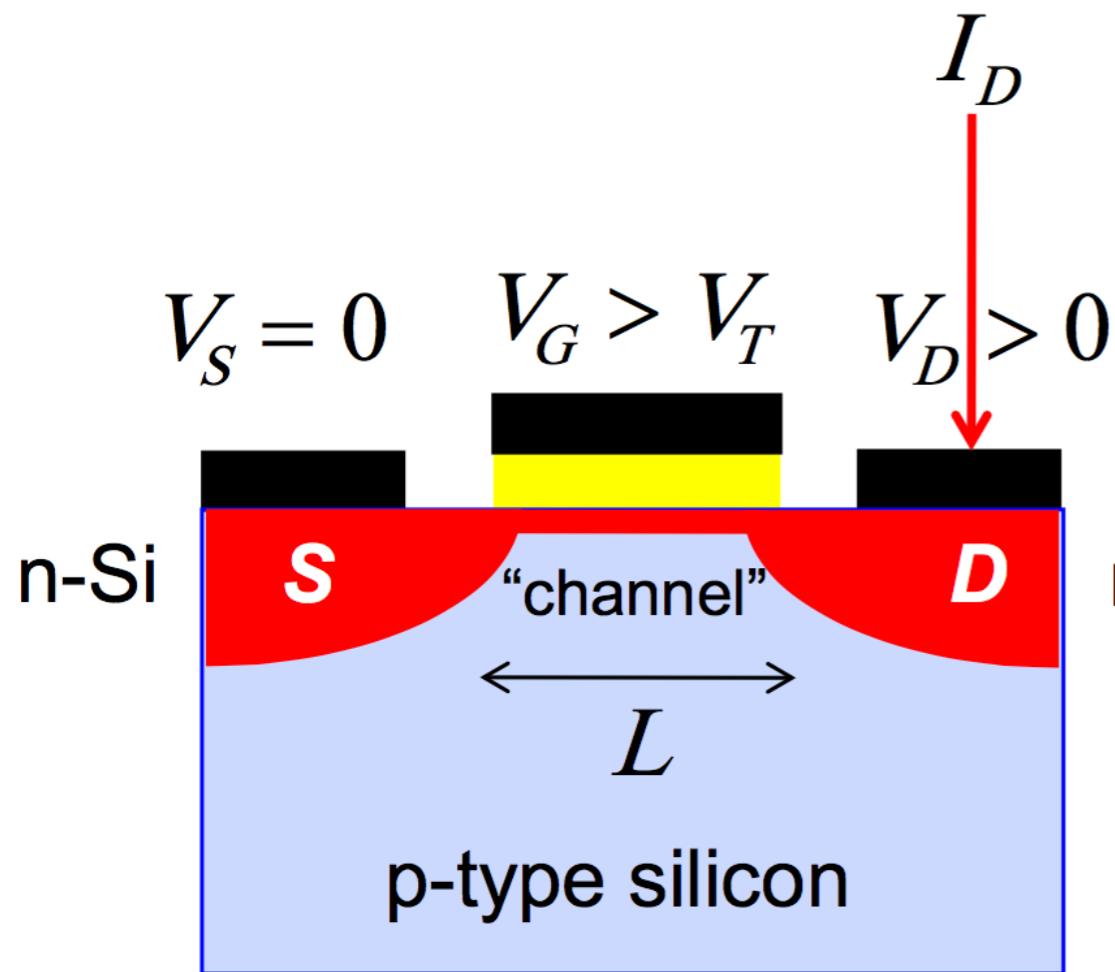
MOSFET



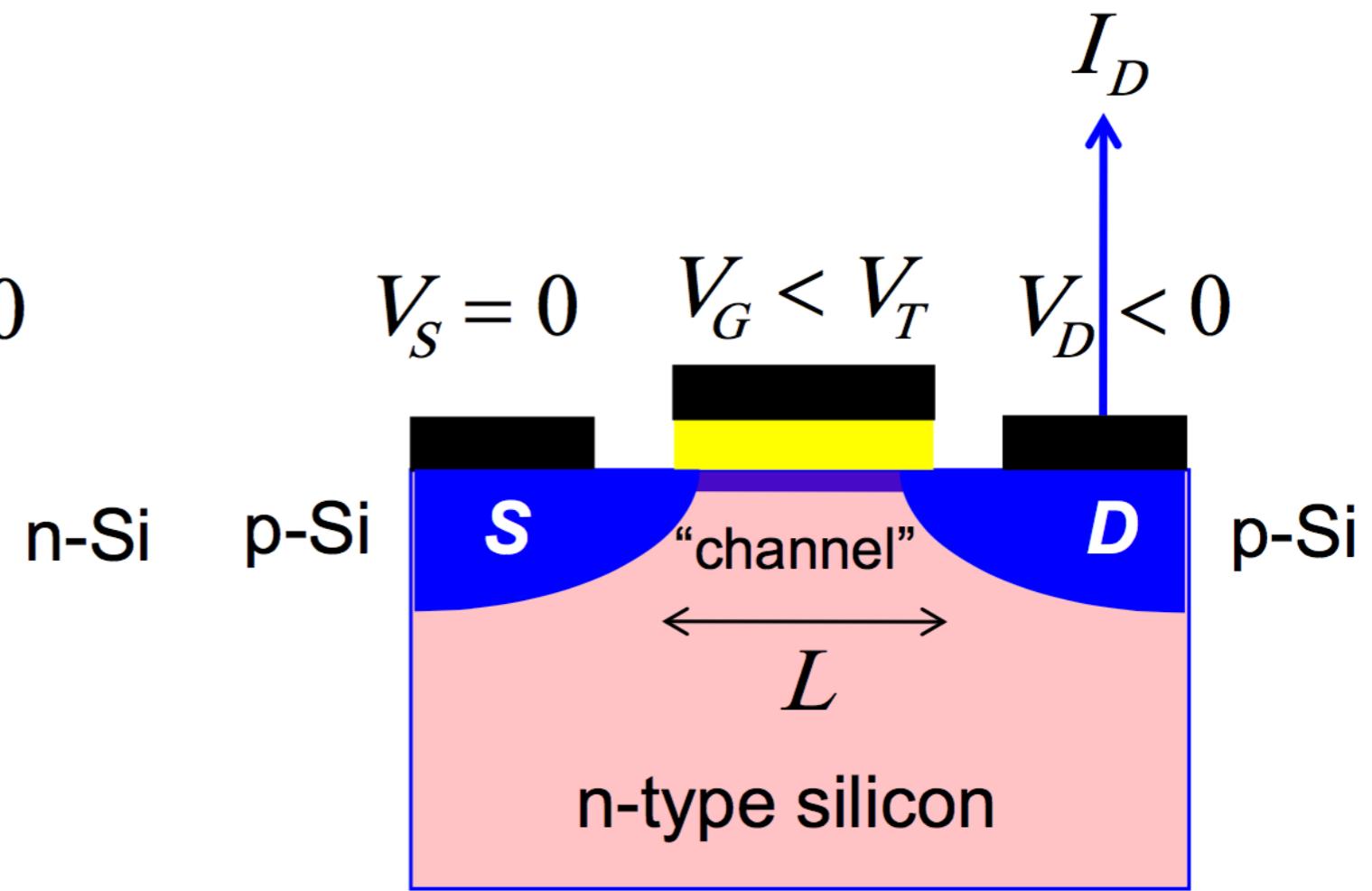
Slide courtesy: Prof. Mark Lundstrom, Purdue University

n-type and p-type FET

n-MOSFET



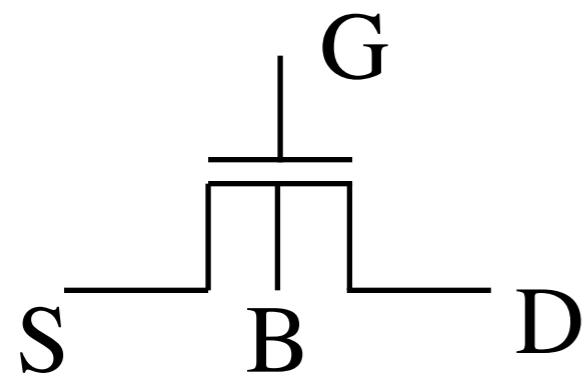
p-MOSFET



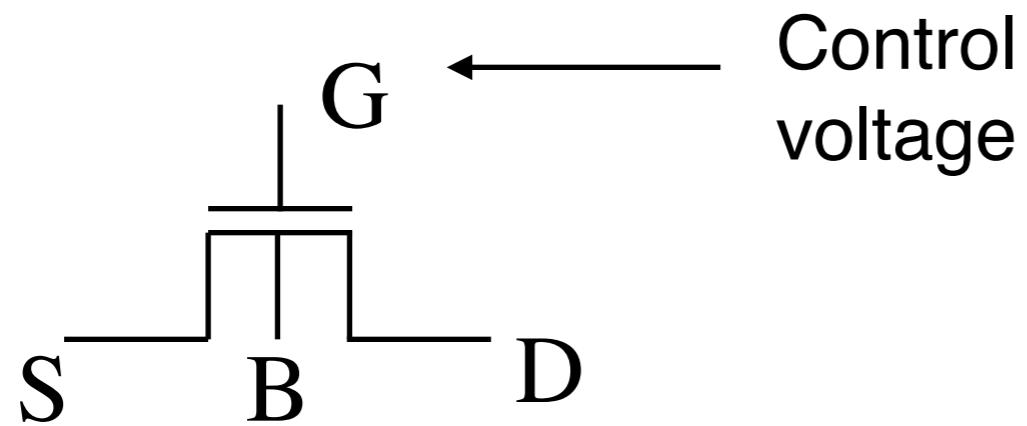
side view

side view

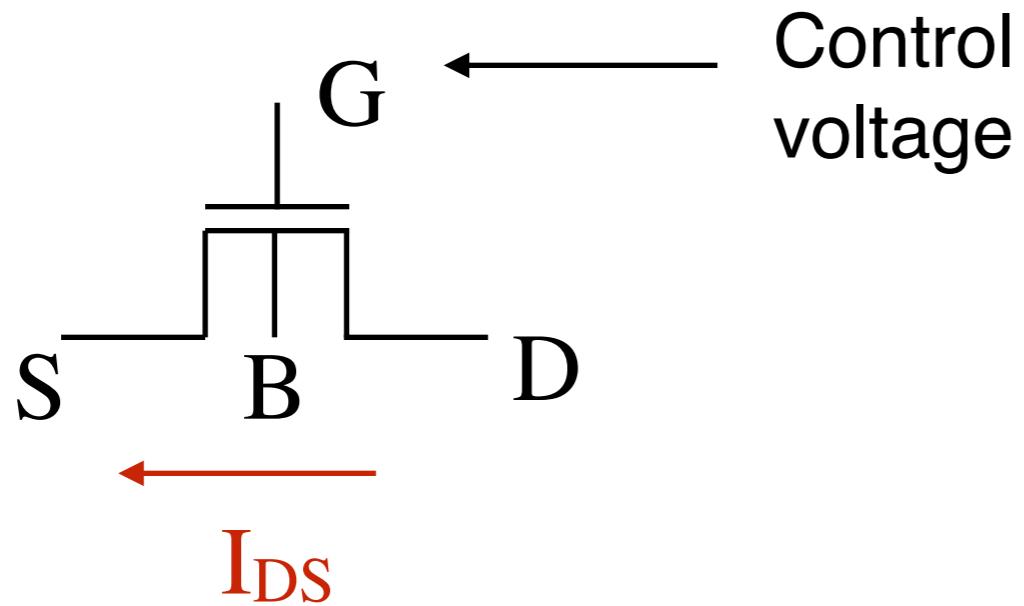
n-FET output curves



n-FET output curves



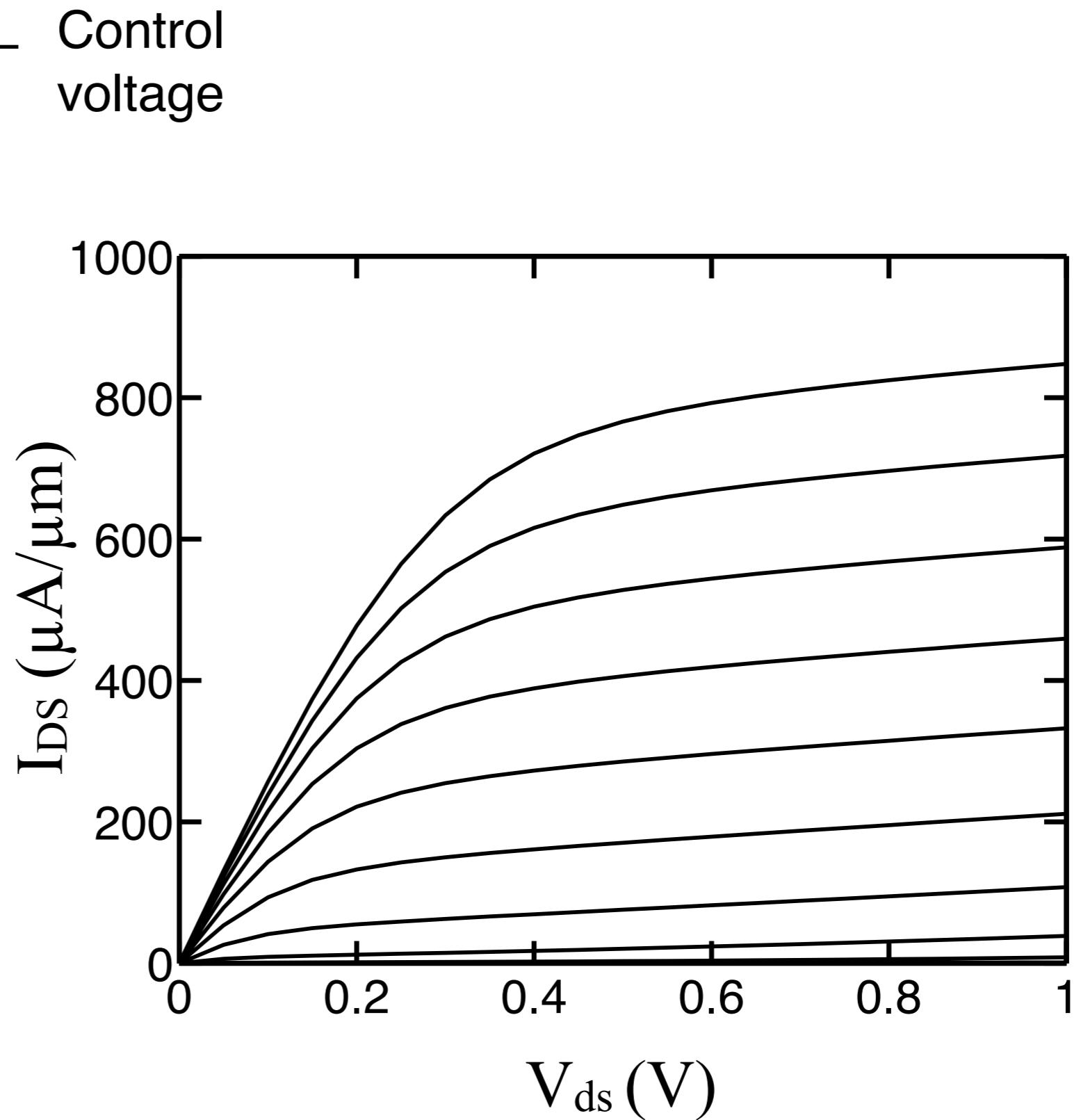
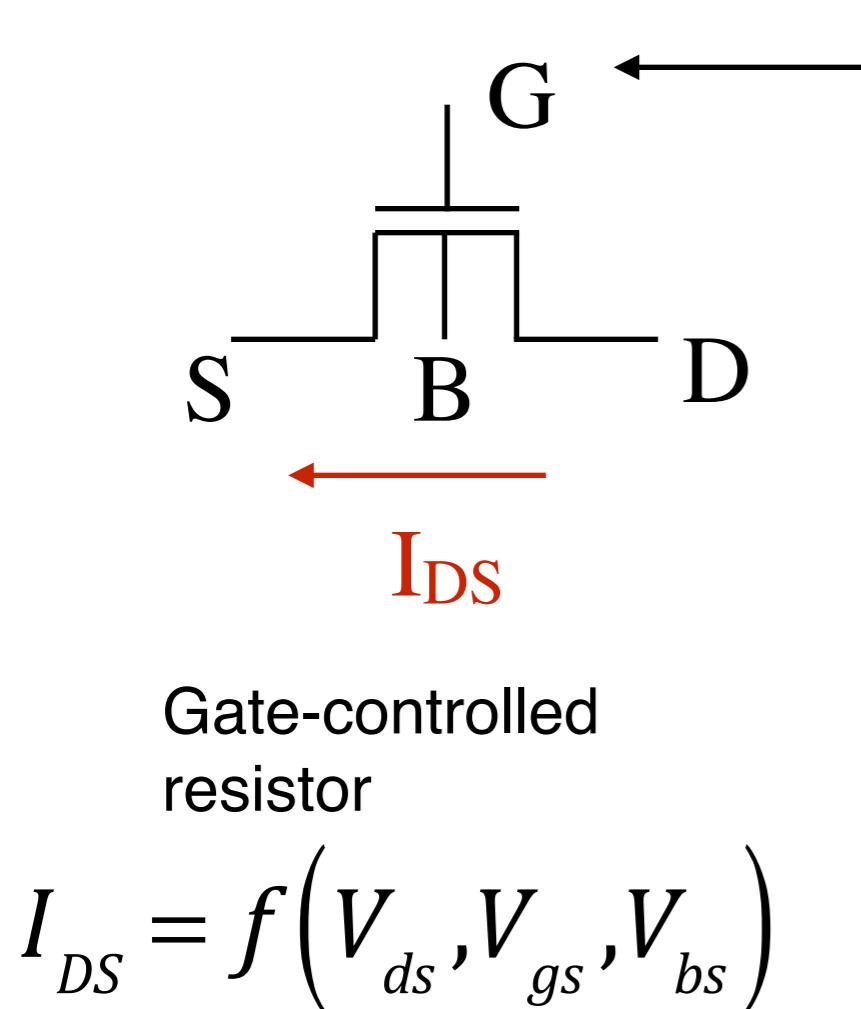
n-FET output curves



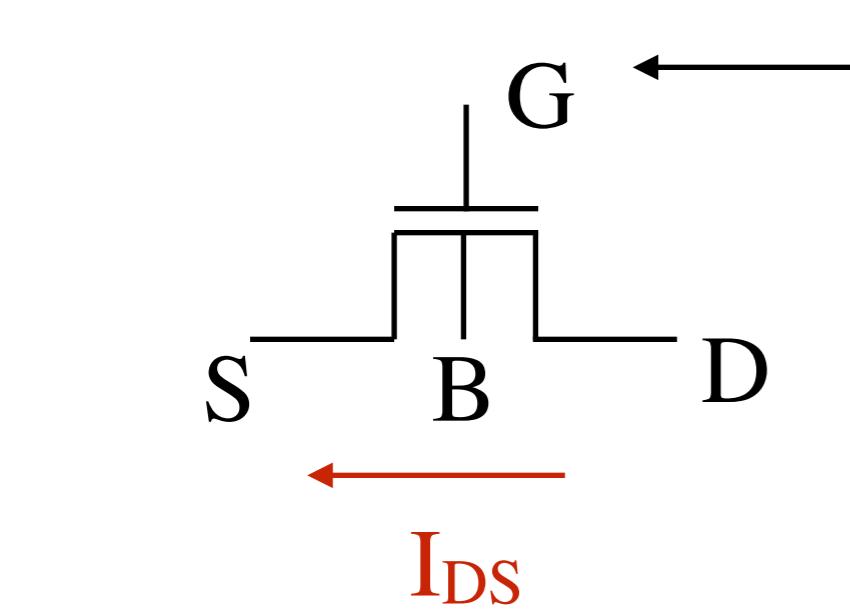
Gate-controlled
resistor

$$I_{DS} = f(V_{ds}, V_{gs}, V_{bs})$$

n-FET output curves



n-FET output curves

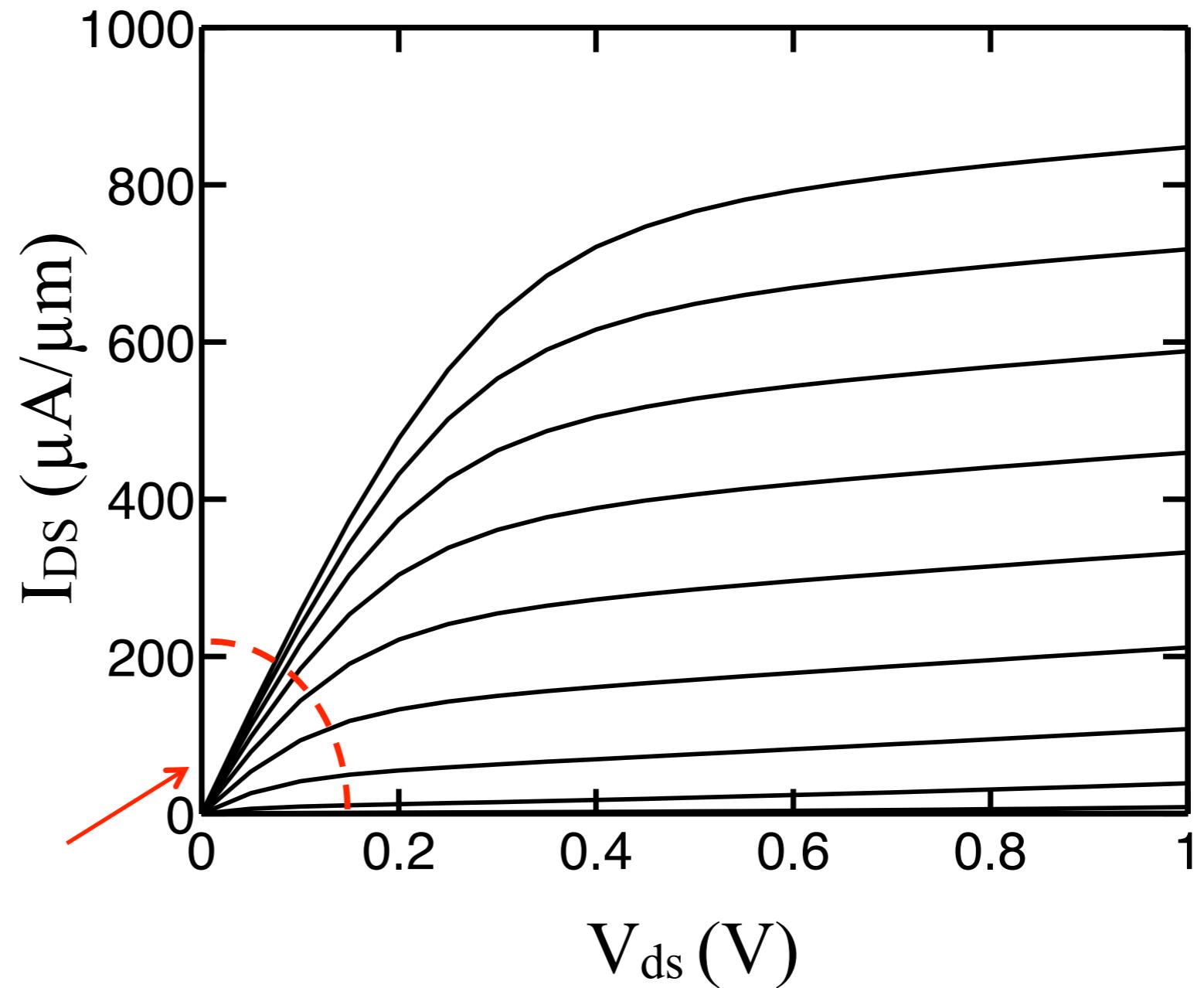


Gate-controlled resistor

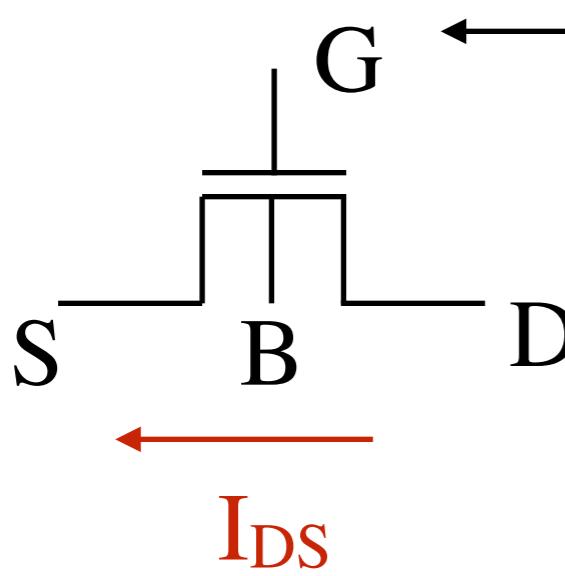
$$I_{DS} = f(V_{ds}, V_{gs}, V_{bs})$$

gate-voltage controlled
Resistor

a.k.a. linear region



n-FET output curves



Gate-controlled resistor

$$I_{DS} = f(V_{ds}, V_{gs}, V_{bs})$$

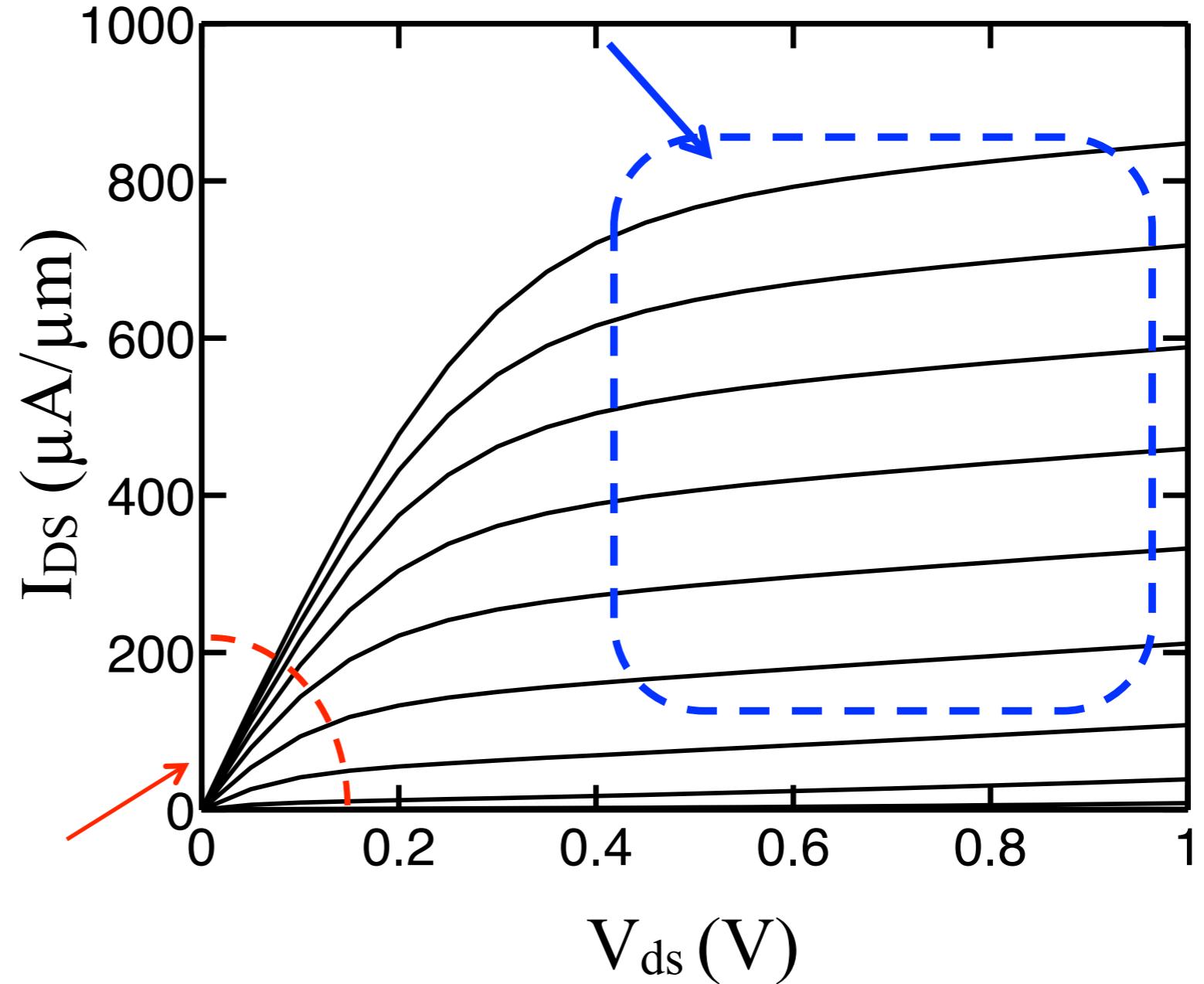
gate-voltage controlled Resistor

a.k.a. linear region

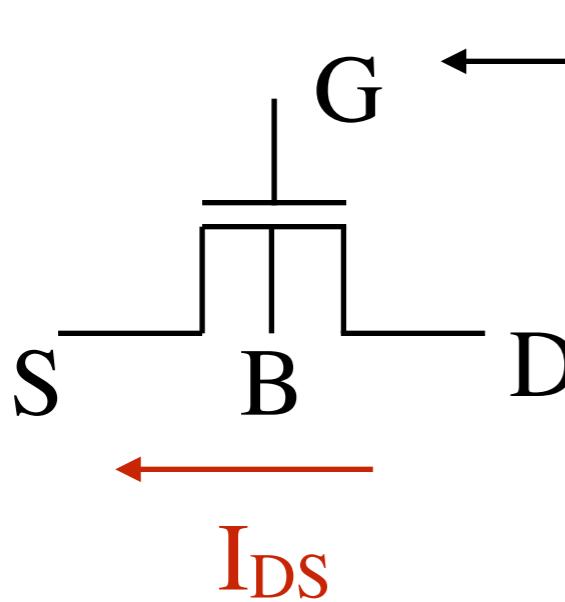
Control voltage

gate-voltage controlled current source

a.k.a. saturation

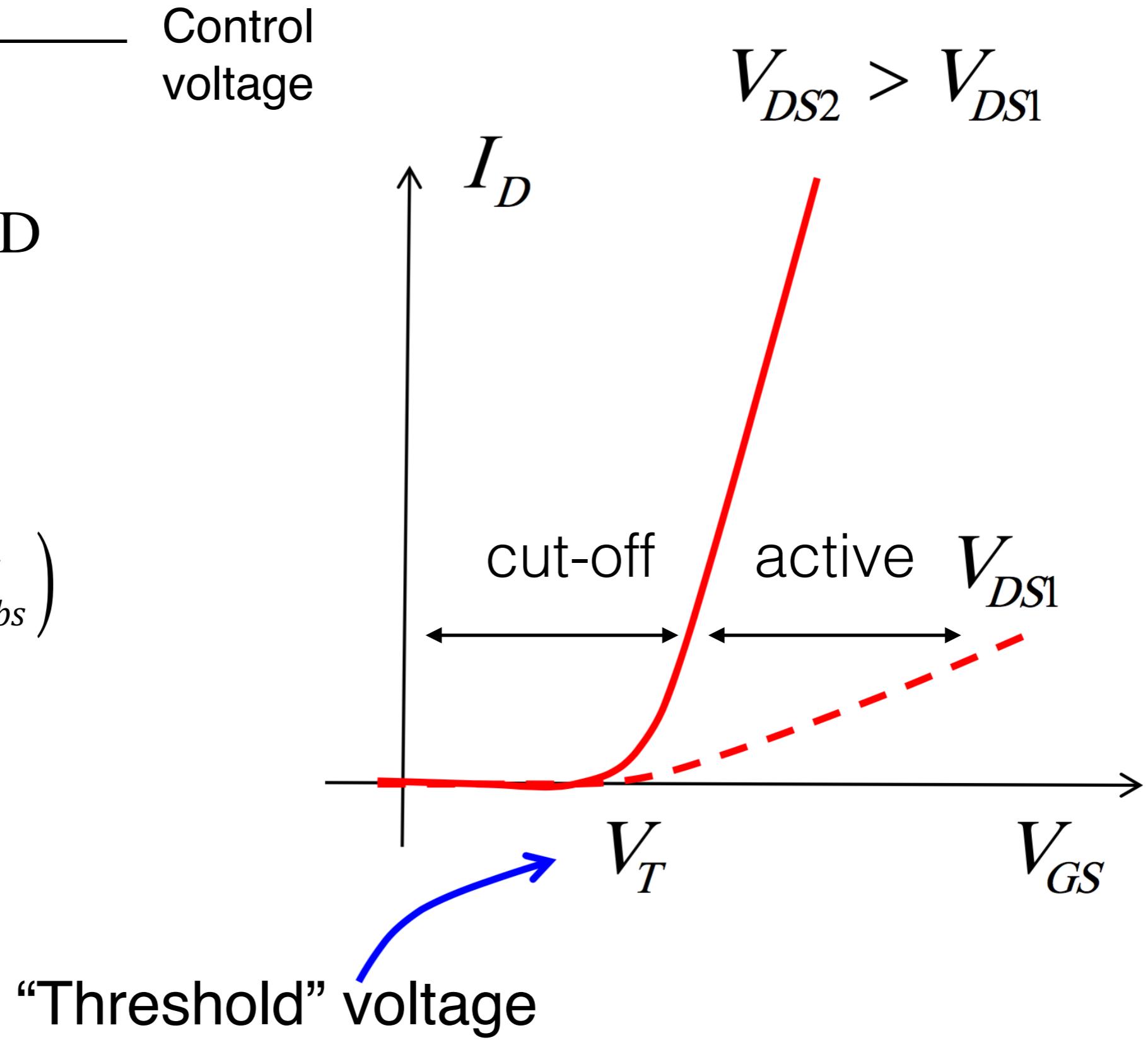


n-FET transfer curves

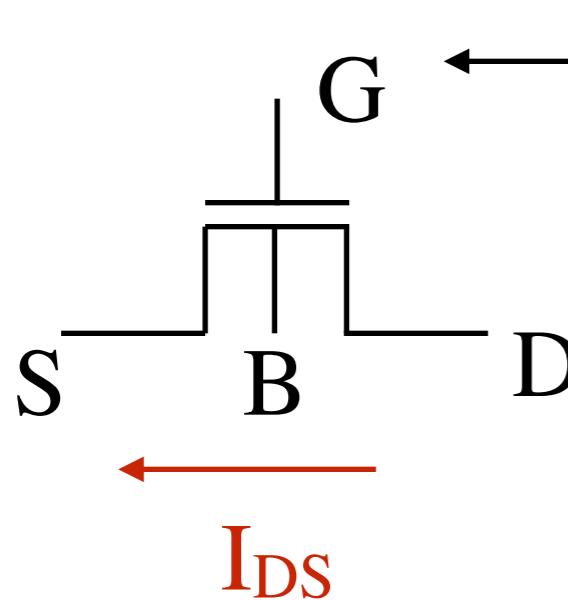


Gate-controlled resistor

$$I_{DS} = f(V_{ds}, V_{gs}, V_{bs})$$



n-FET transfer curves

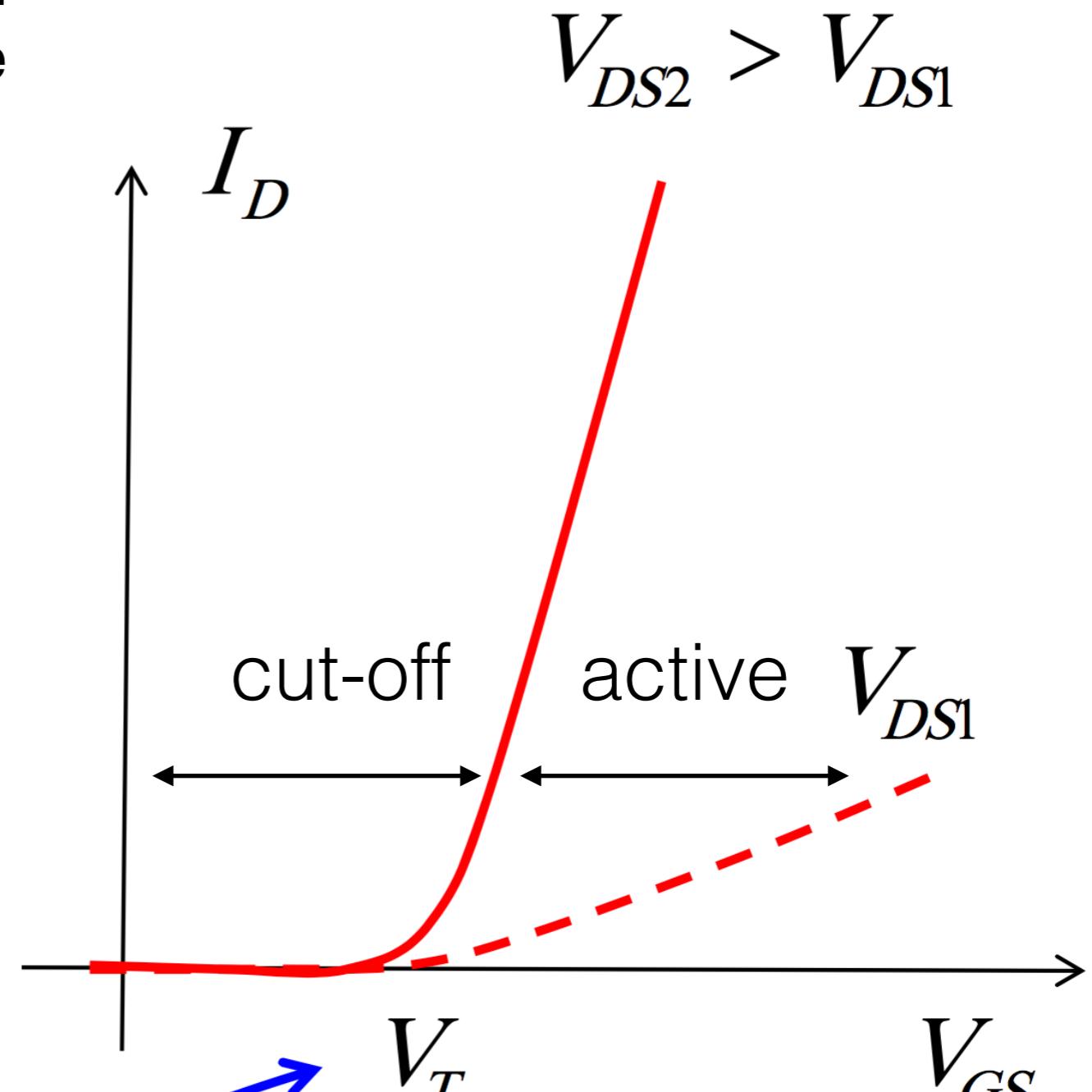


Gate-controlled resistor

$$I_{DS} = f(V_{ds}, V_{gs}, V_{bs})$$

$V_{gs} > V_T$ “ON”
 $V_{gs} \leq V_T$ “OFF”

“Threshold” voltage



Summary

- What is a MOSFET?

Ans: Its a current-controlled switch.

- What is the control voltage?

Ans: Primarily, gate-source voltage, V_{gs} .

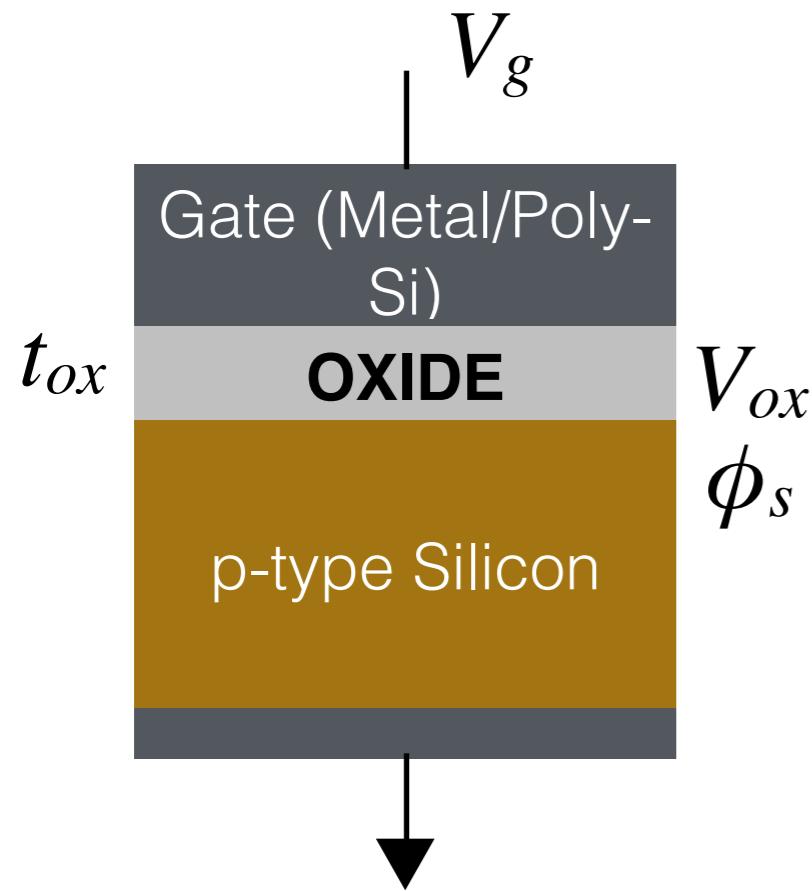
- How much control voltage is needed to turn the switch on?

Ans: Threshold voltage (V_T)

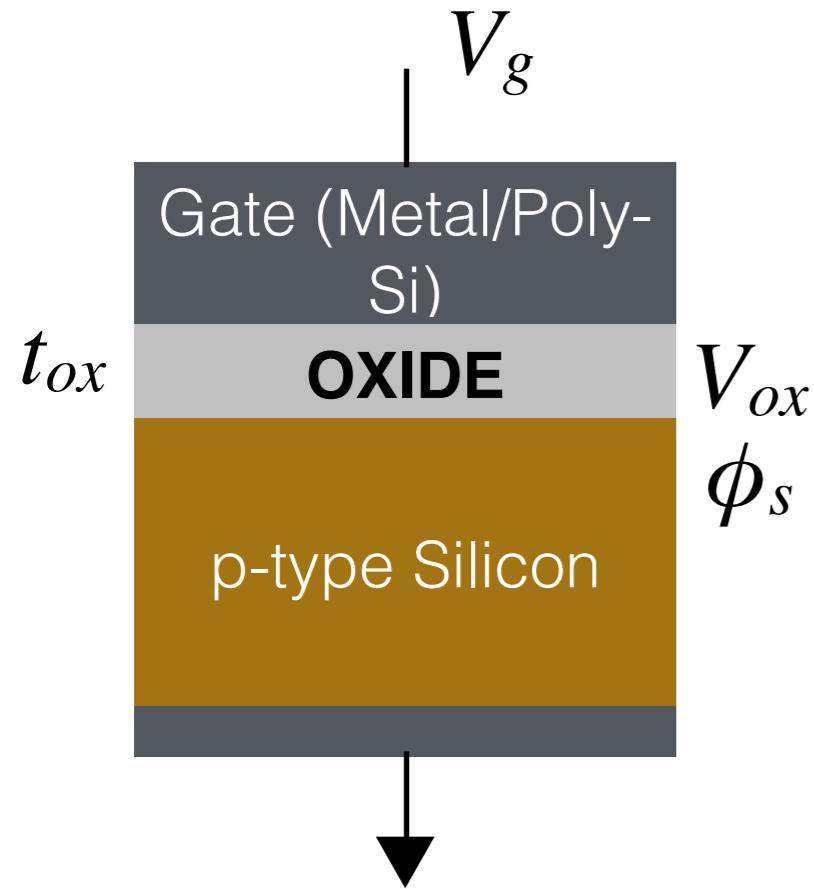
- How much current flows through the device?

Ans: The drain-source current (I_{DS}). Its value depends on all of the terminal voltages (V_{gs} , V_{ds} , V_{bs}).

Concept of threshold voltage



Concept of threshold voltage



From KVL, gate voltage must balance out V_{ox} and ϕ_s

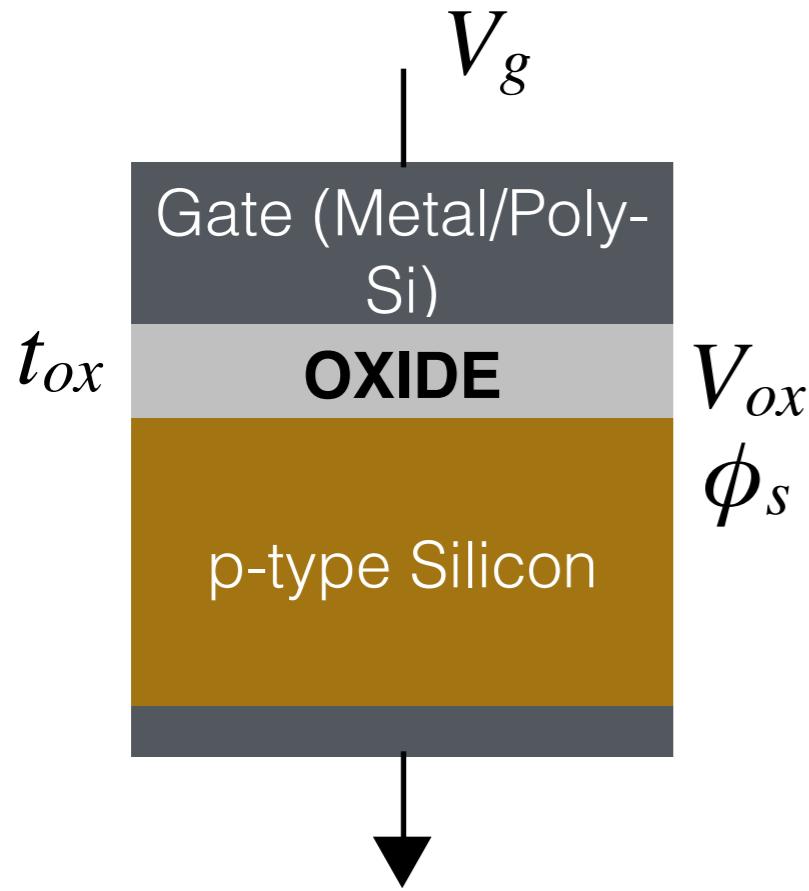
$$V_T = V_{ox} + \phi_s + \left(\phi_{ms} + \frac{Q_{ox}}{C_{ox}} \right)$$

Flat-band
fabrication; material

$$V_{ox} = \frac{Q_B}{C_{ox}}$$

Threshold voltage is defined as the gate voltage for which an inversion layer is created in the p-type silicon. This occurs when $\phi_s = 2\phi_f$. (Bulk potential)

Concept of threshold voltage



From KVL, gate voltage must balance out V_{ox} and ϕ_s

$$V_T = V_{ox} + \phi_s + \left(\phi_{ms} + \frac{Q_{ox}}{C_{ox}} \right)$$

Flat-band
fabrication; material

$$V_{ox} = \frac{Q_B}{C_{ox}}$$

$$\phi_f = \frac{k_B T}{q} \ln \left(\frac{N_A}{n_i} \right)$$

$$Q_B = \sqrt{2qN_A \epsilon_{si}(2\phi_f)}$$

Threshold voltage is defined as the gate voltage for which an inversion layer is created in the p-type silicon. This occurs when $\phi_s = 2\phi_f$. (Bulk potential)

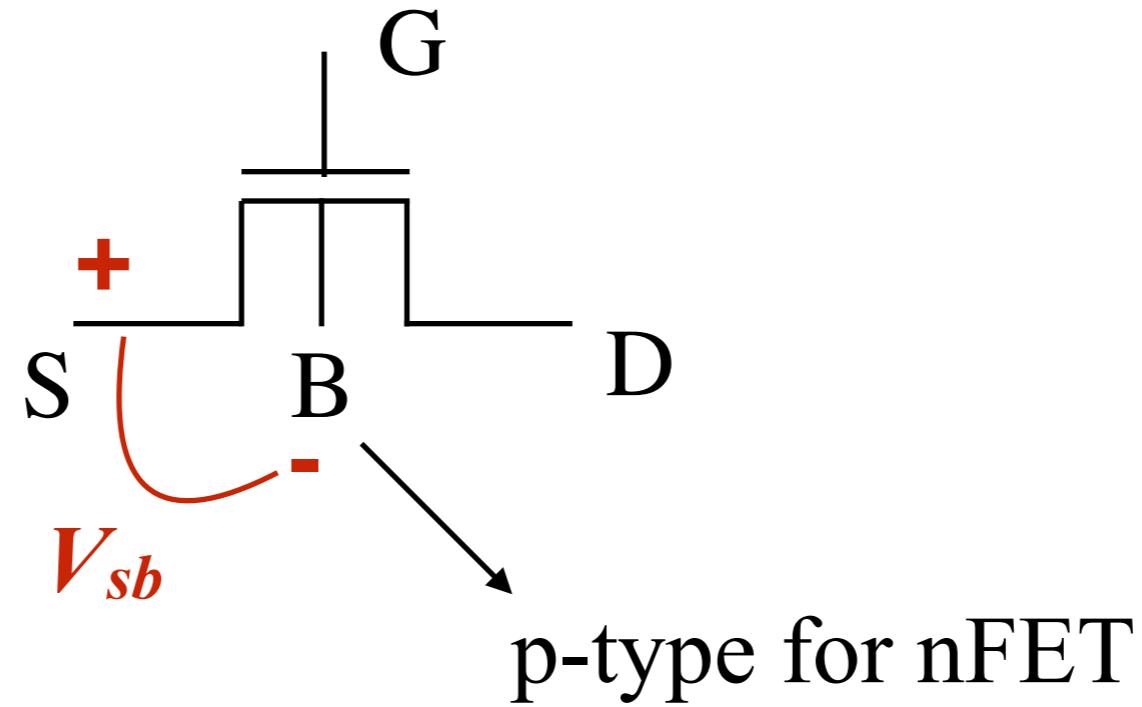
k_B : Boltzmann constant

T: Temperature in Kelvin

N_A : doping density (m^{-3})

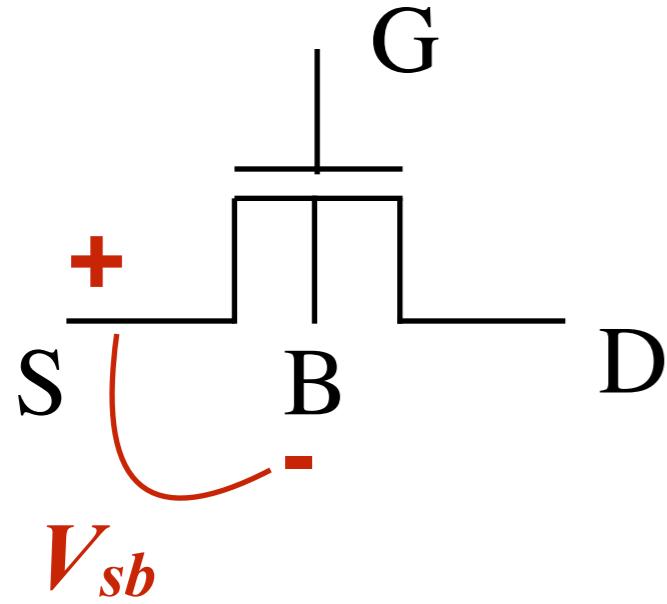
n_i : intrinsic carrier concentration $\sim 10^{10} (\text{cm}^{-3})$

Effect of substrate bias on V_T



- Negative body with respect to gate makes the body source junction reverse biased.
- This increases the depletion width.
- Hence, more gate voltage is needed to compensate for this effect —> Increase in V_T with negative V_{bs} .

Effect of substrate bias on V_T



$$V_T = V_{fb} + 2|\phi_f| + \frac{\sqrt{2q\epsilon_{si}N_A(2|\phi_f|-V_{bs})}}{C_{ox}}$$

$$V_T = V_{T0} + \gamma \left(\sqrt{(2|\phi_f|-V_{bs})} - \sqrt{2|\phi_f|} \right)$$

$$V_{T0} = V_{fb} + 2|\phi_f| + \frac{Q_{B0}}{C_{ox}}$$

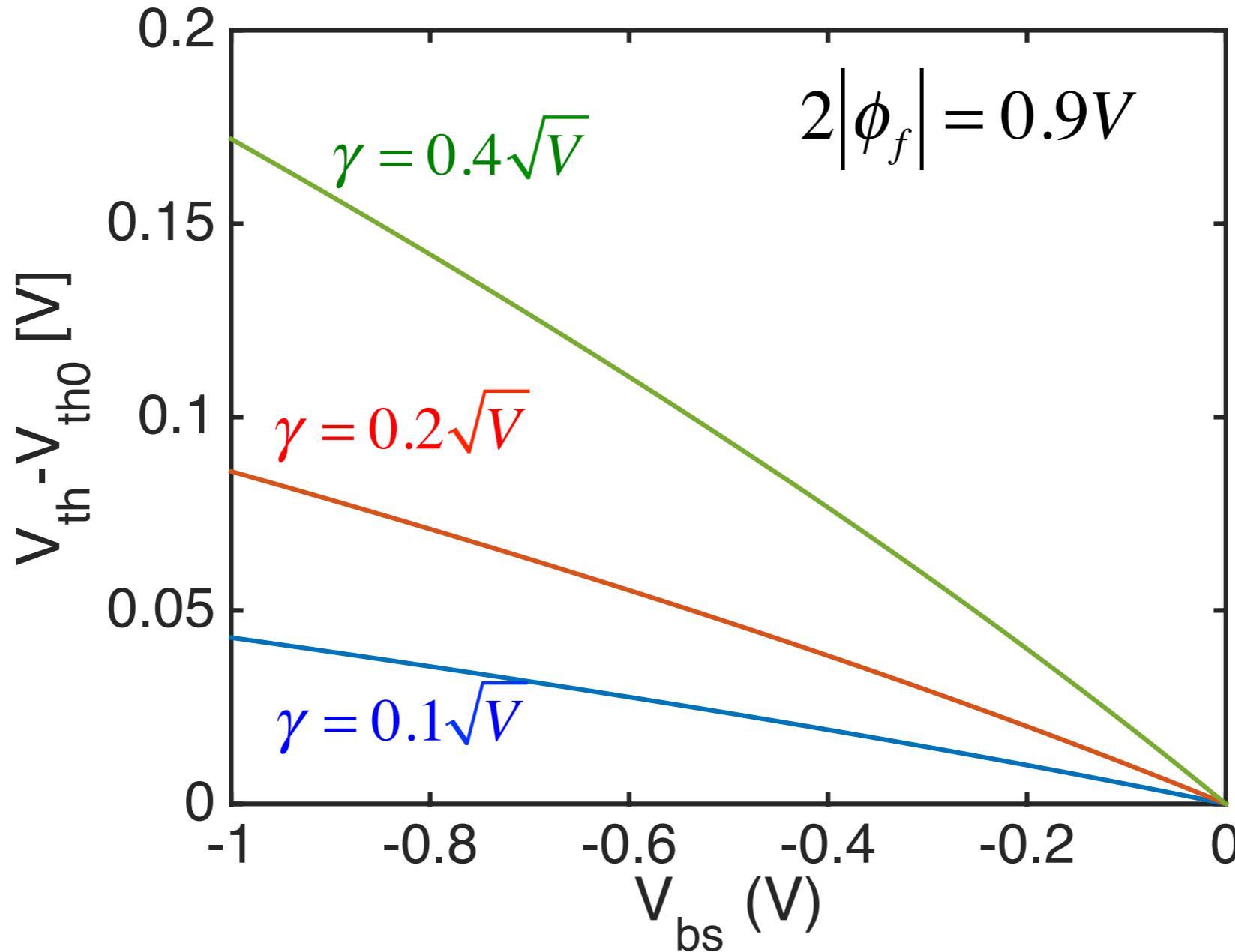
$$\gamma = \frac{\sqrt{2q\epsilon_{si}N_A}}{C_{ox}}$$

V_{fb} : Flat-band voltage (depends on work function difference and oxide charge)

Q_{B0} : depletion charge at $V_{bs} = 0$

γ : Body-effect coefficient {unit: sqrt(V)}

Effect of substrate bias on V_T



Derivation of transistor I-V characteristics
On board

Summary of transistor I-V equations

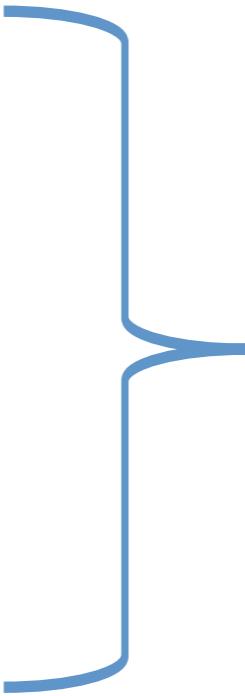
Linear: $V_{ds} < V_{dsat}$

$$I_{DS} = \mu_n C_{ox} \left(\frac{W}{L} \right) \left[(V_{gs} - V_T) V_{ds} - \frac{V_{ds}^2}{2} \right]$$

Saturation: $V_{ds} \geq V_{dsat}$

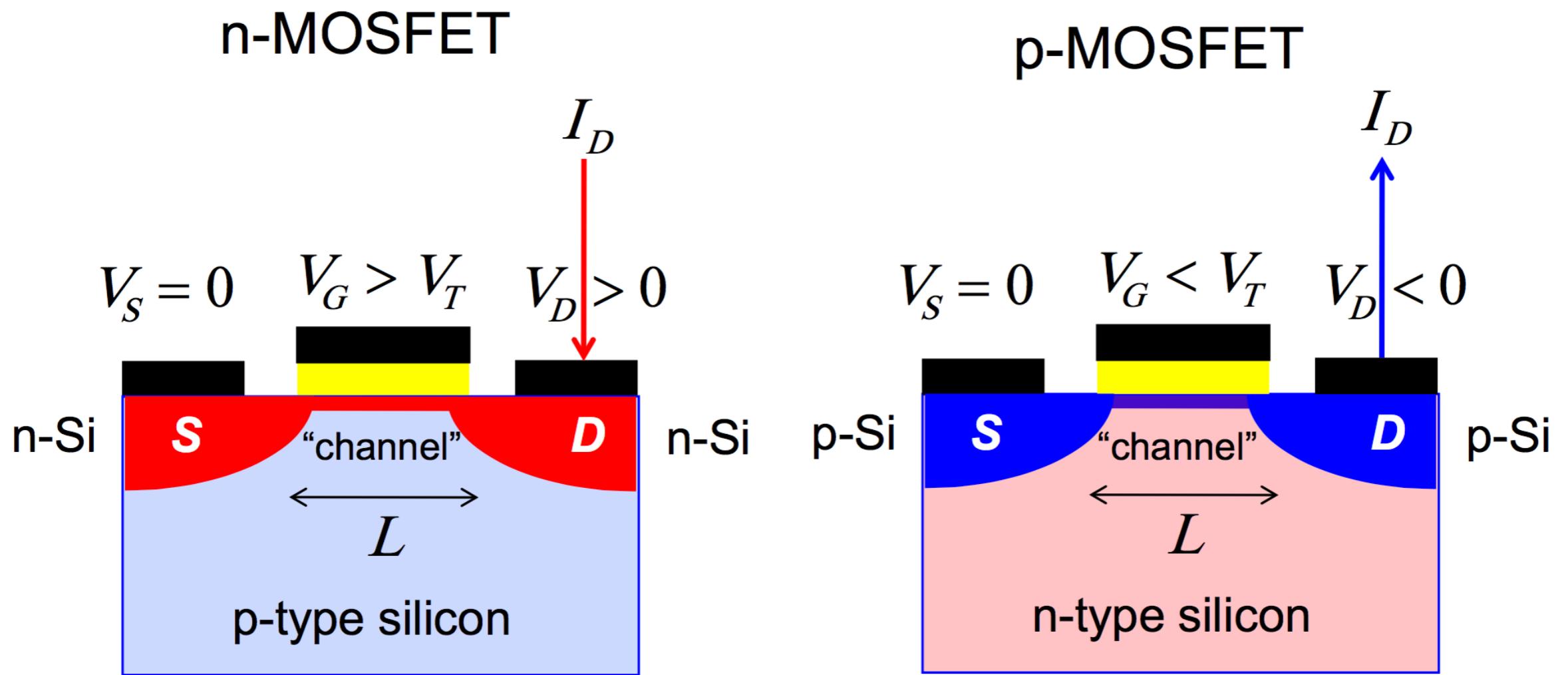
$$I_{DS} = \frac{1}{2} \mu_n C_{ox} \left(\frac{W}{L} \right) (V_{gs} - V_T)^2 (1 + \lambda V_{ds})$$

Saturation voltage: $V_{dsat} = (V_{gs} - V_T)$

- 
- $V_{gs} > V_T$ (Device is ON)
 - No velocity saturation.
 - In saturation, current increases as $(V_{gs} - V_t)^2$
 - Transistor is not a perfect current source in saturation due to CLM.

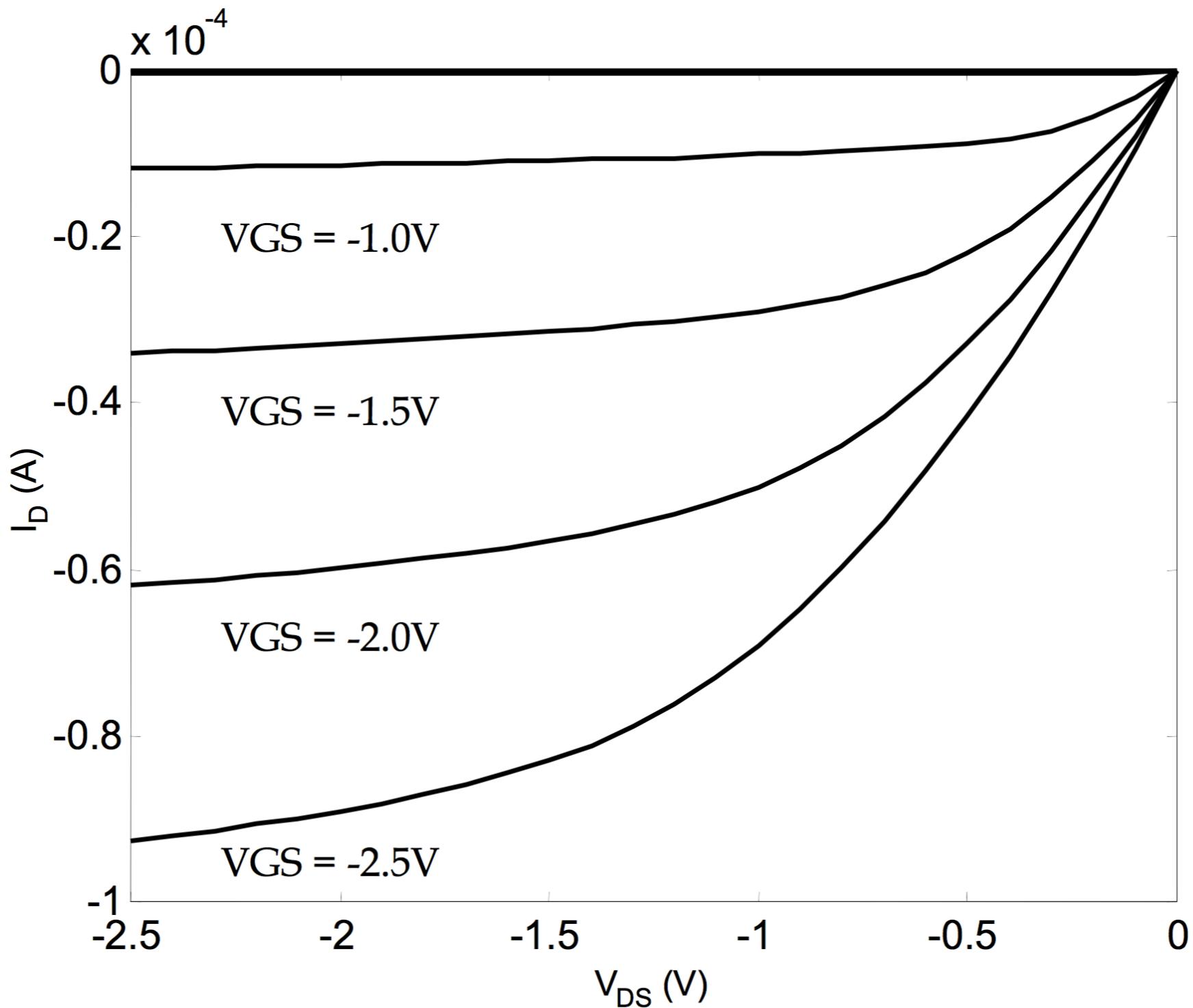
Homework problem: Calculate output conductance of the transistor in linear and saturation regimes of transport

n-FET to p-FET



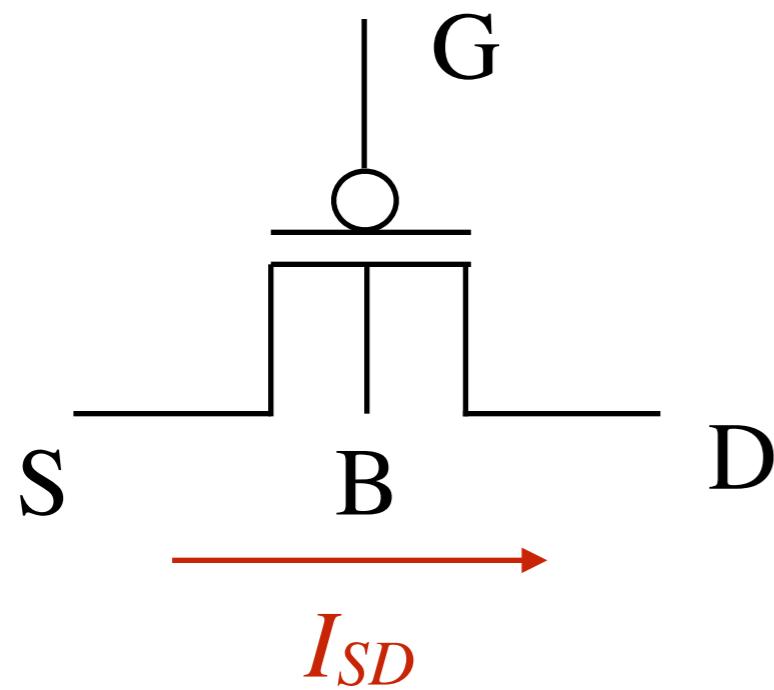
- Substrate is n-type (i.e. n-well) and source/drain are p-type.
- Current is carried by holes.

How to analyze a p-FET



One possibility: Assume all variables negative!

p-FET current



- Source is at higher potential than drain.
- Current flows from source to drain.
- Body is normally connected to V_{dd} .
- Voltages: V_{sg} , V_{sd} ...

Linear ($V_{sd} < V_{sdat}$):

$$I_{SD} = \mu_h C_{ox} \frac{W}{L} \left[(V_{sg} + V_{TP}) V_{sd} - \frac{V_{sd}^2}{2} \right]$$

Above cut-off

Saturation ($V_{sd} \geq V_{sdsat}$) :

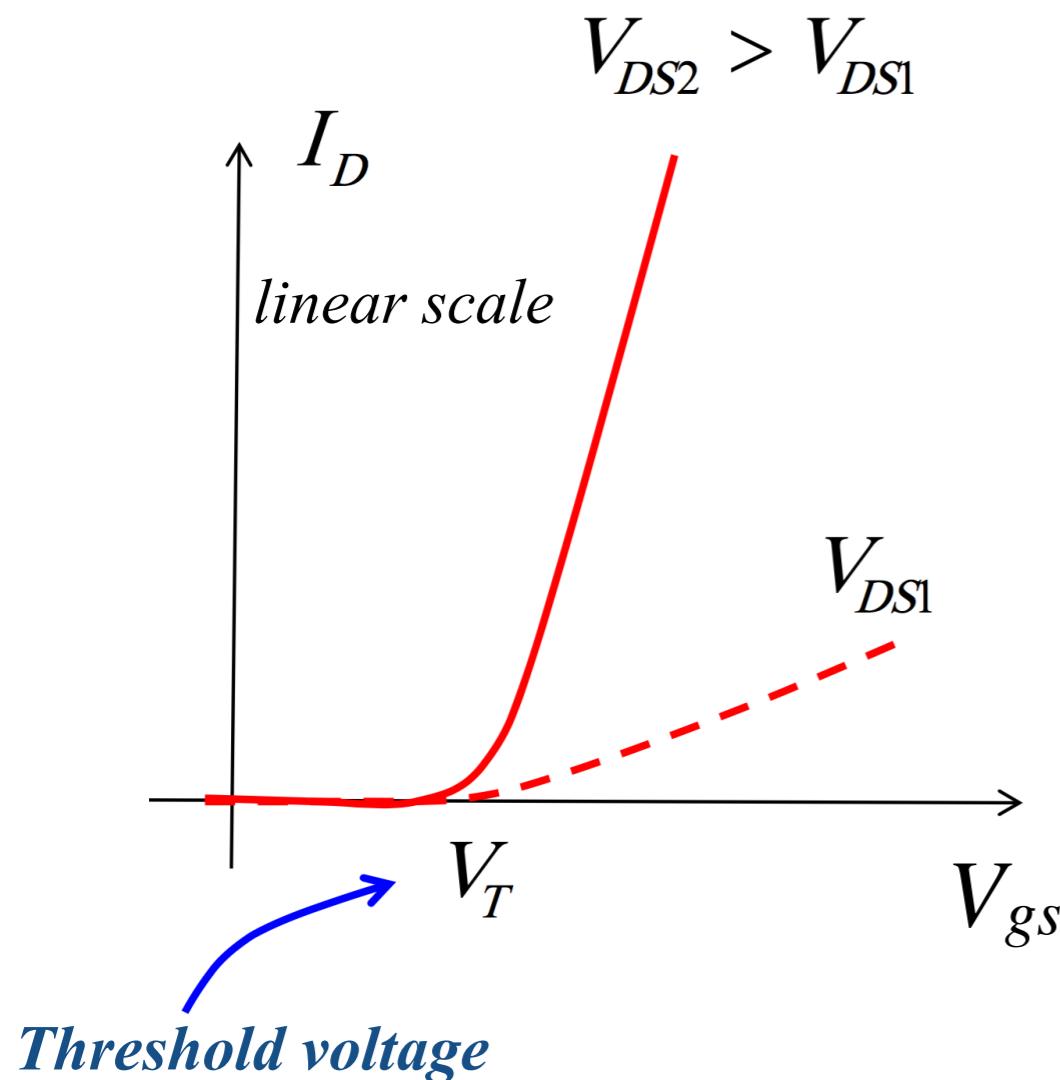
$$I_{SD} = \frac{1}{2} \mu_h C_{ox} \frac{W}{L} (V_{sg} + V_{TP})^2 (1 + \lambda V_{sd})$$

$$V_{sdat} = (V_{sg} + V_{TP})$$

V_{TP} is negative for enhancement mode p-FET

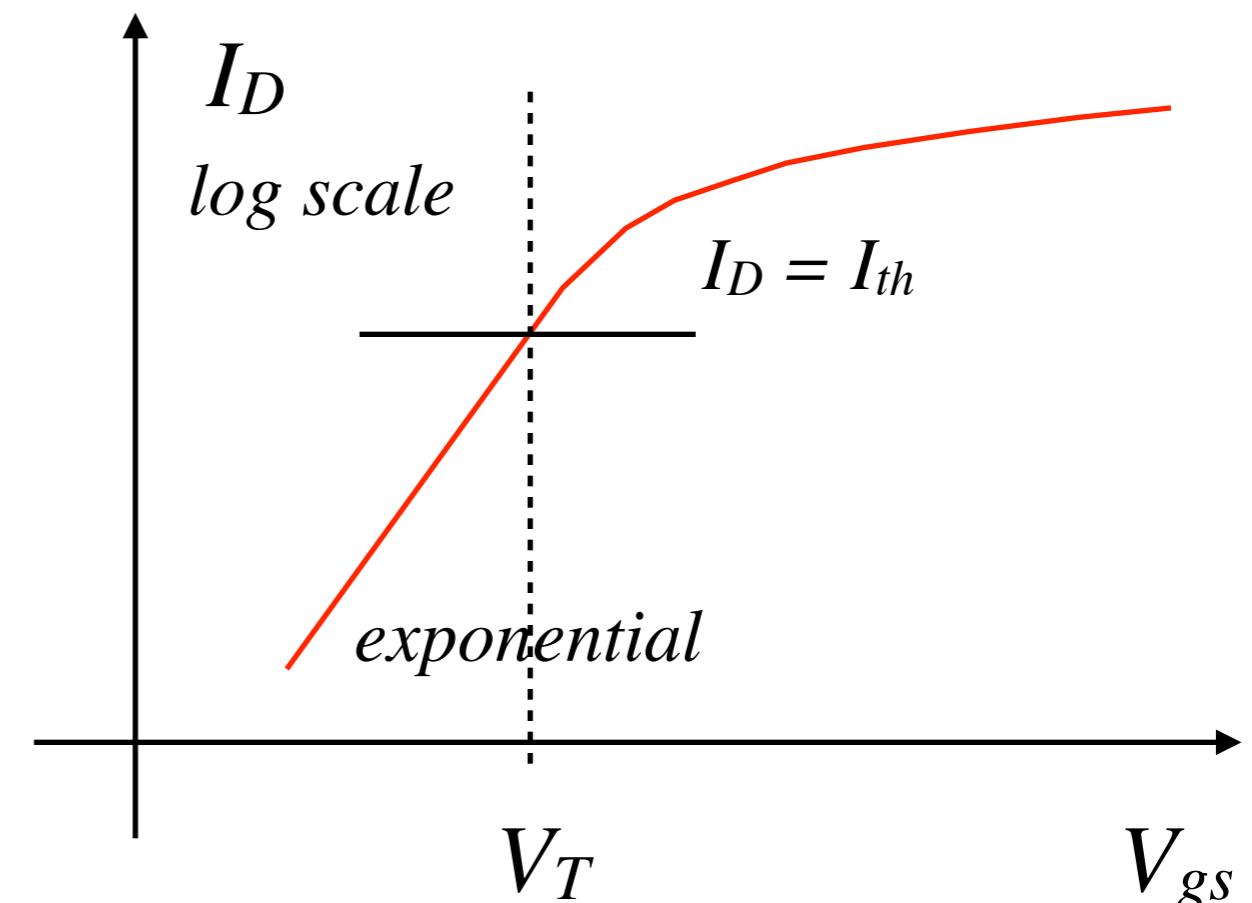
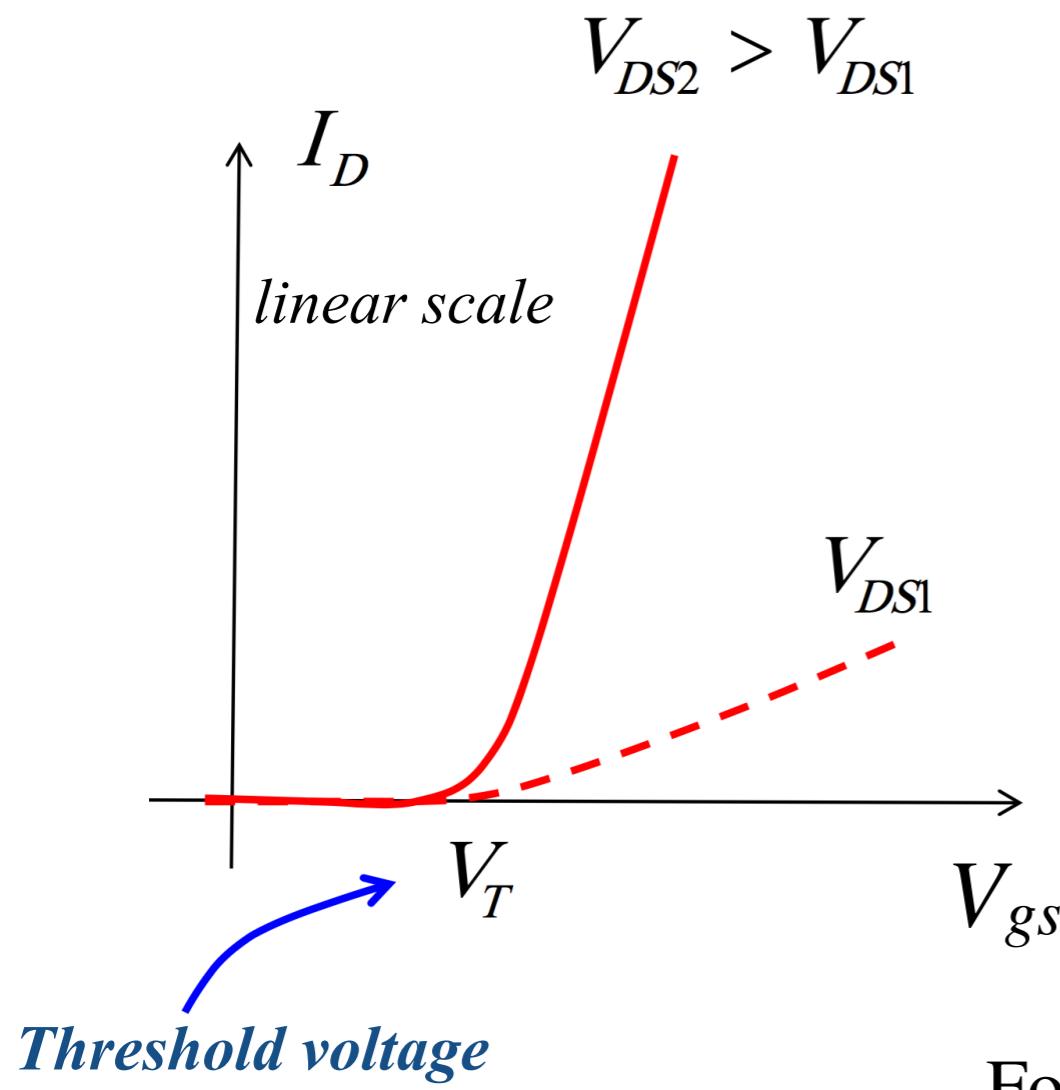
Sub-threshold conduction

- When $V_{gs} < V_T$, a small amount of drain-source current flows.
- Known as *sub-threshold conduction*.



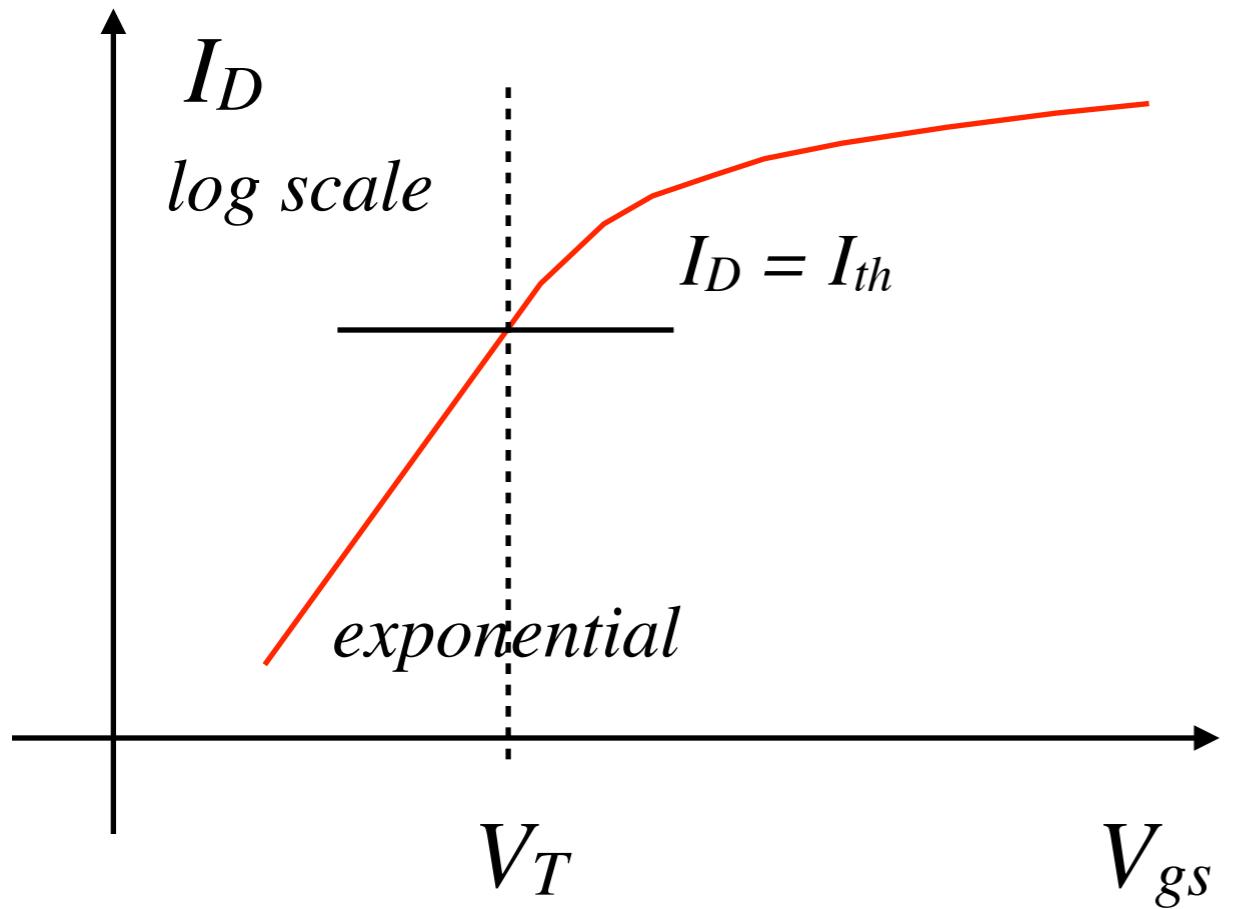
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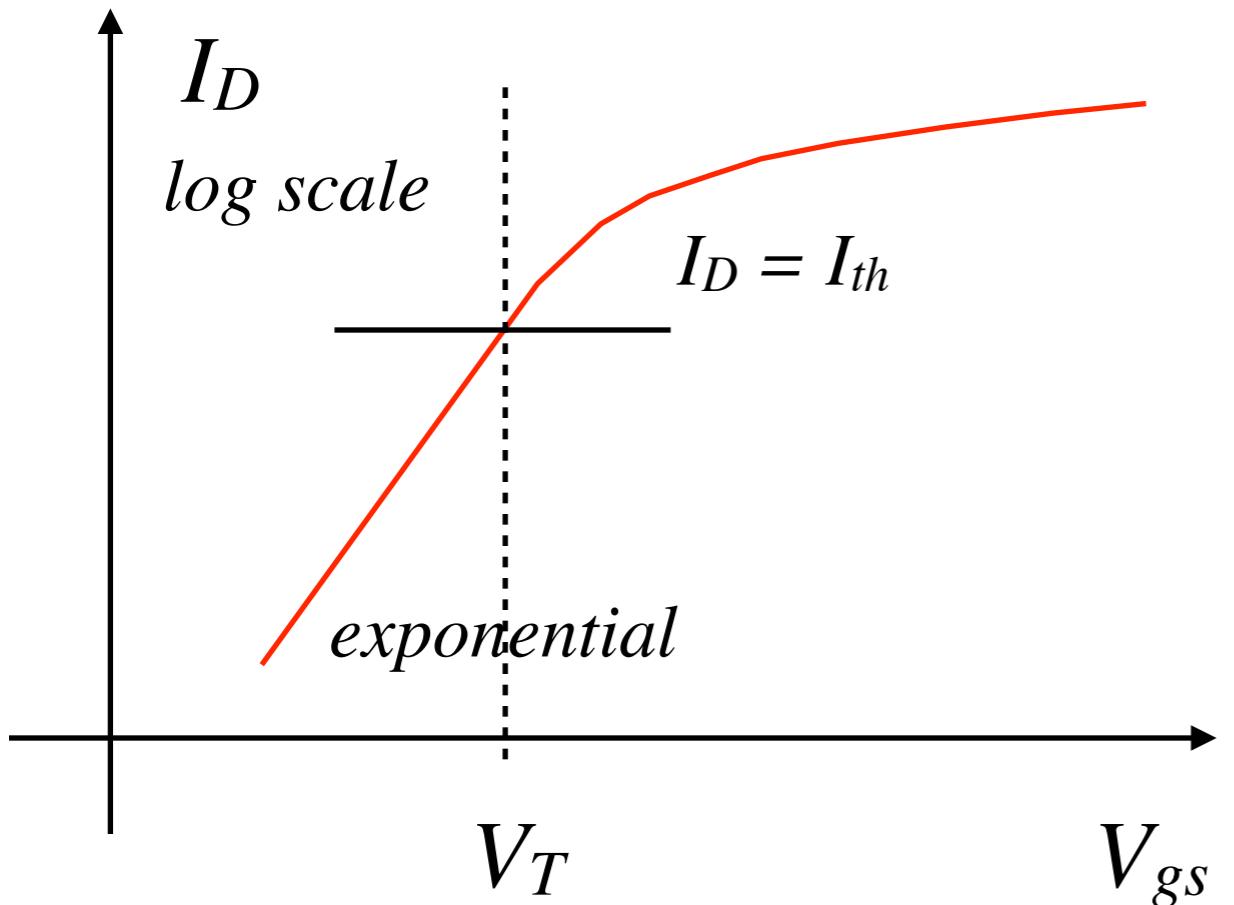
For $V_{gs} < V_T$, current varies exponentially with V_{gs} .

Sub-threshold conduction



- For $V_{gs} < V_T$, current varies exponentially with V_{gs} .
- A practical definition of V_T : V_{gs} needed to obtain a pre-defined value of threshold current, I_{th} .
- Usually, $I_{th} = 300 \text{ nA} * (\text{W/L})$

Sub-threshold conduction



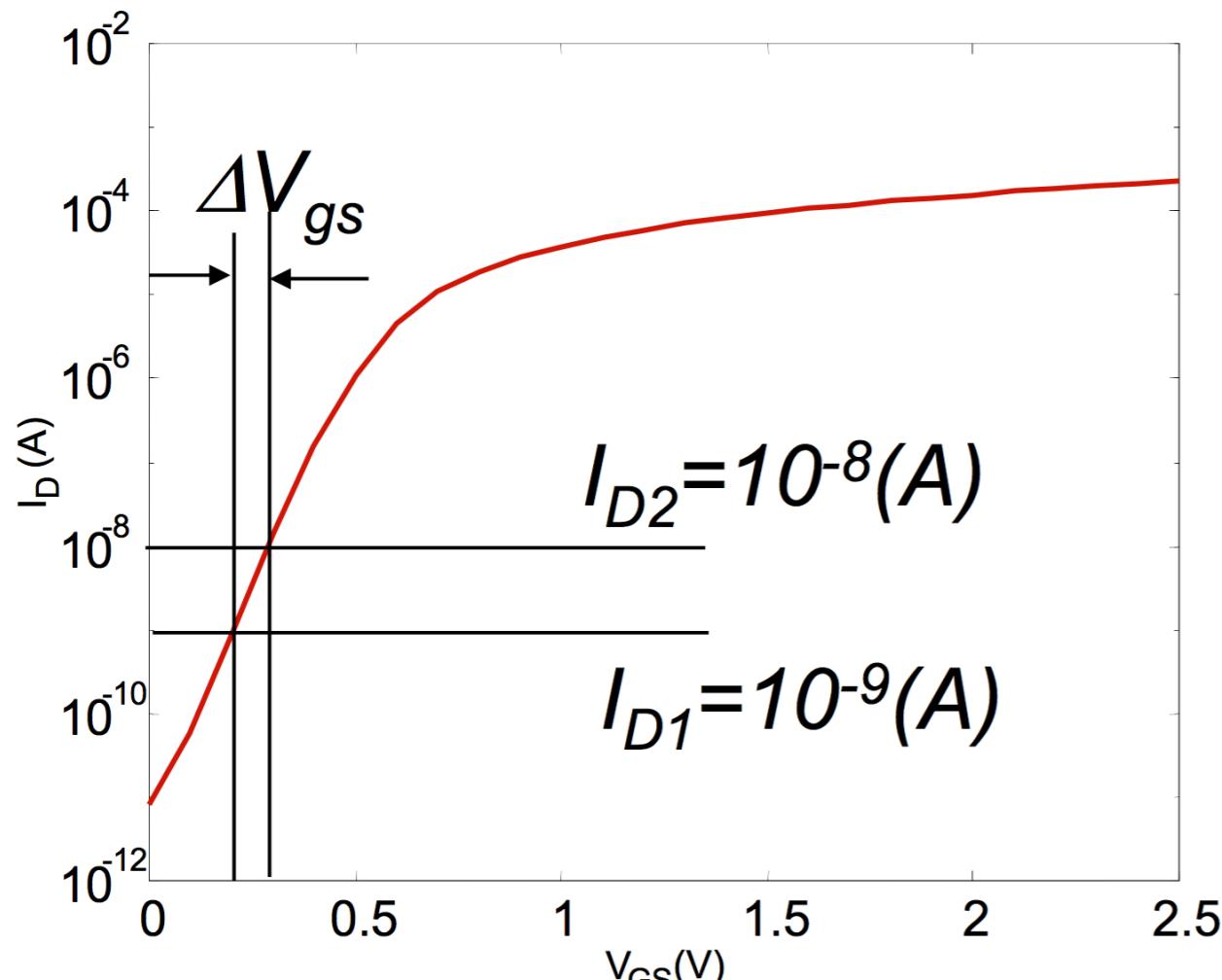
$$I_{DS} = I_0 \exp\left(\frac{q(V_{gs} - V_T)}{nk_B T}\right) \left(1 - \exp\left(-\frac{qV_{ds}}{k_B T}\right)\right)$$

$n = (1 + C_{dep}/C_{ox})$ non-ideality factor
Typically between 1.0-1.5

Note: @ $V_{gs} = V_T$, $I_{DS} = I_0$ for $V_{ds} \gg k_B T/q$ ($V_{ds} > 100$ mV)

- For $V_{gs} < V_T$, current varies exponentially with V_{gs} .
- A practical definition of V_T : V_{gs} needed to obtain a pre-defined value of threshold current, I_{th} .
- Usually, $I_{th} = 300$ nA*(W/L)

Sub-threshold slope



Subthreshold Slope (S) is defined as the ΔV_{gs} required for 1 decade change in I_D

$$\Rightarrow \Delta V_{gs} \text{ for } I_{D2}/I_{D1} = 10$$

$$\Rightarrow \frac{I_{D2}}{I_{D1}} = e^{\frac{q(V_{gs2}-V_{gs1})}{nkT}} = e^{\frac{q(\Delta V_{gs})}{nkT}}$$

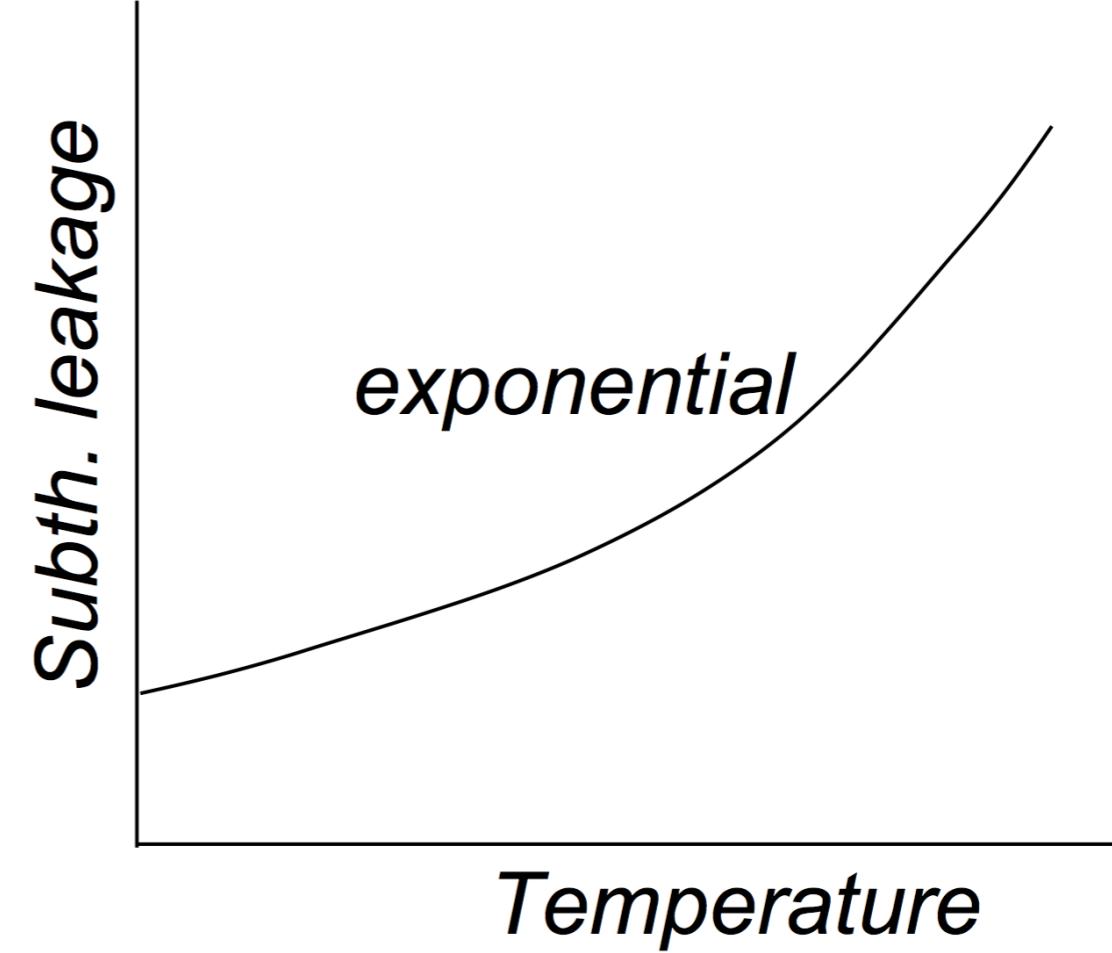
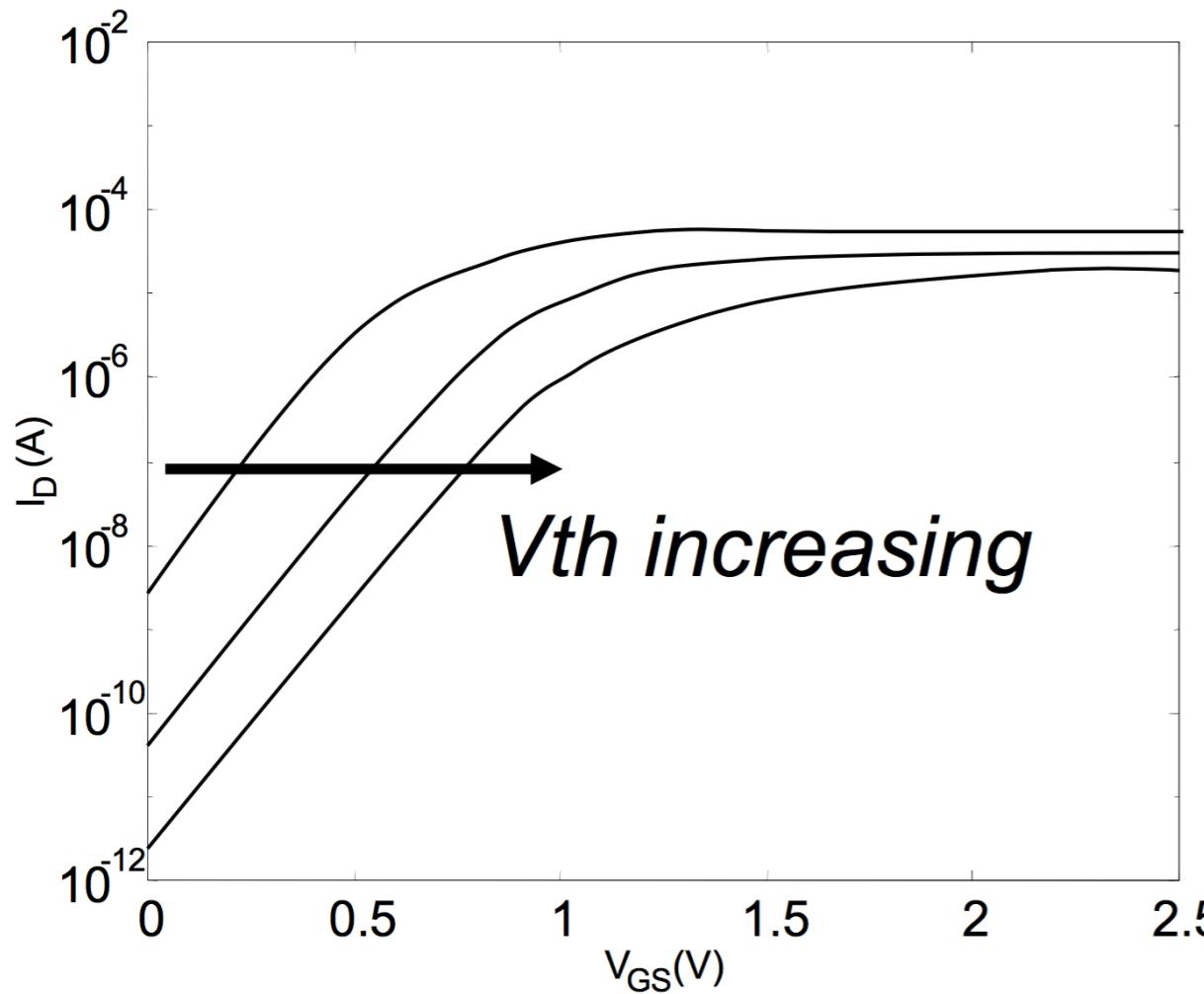
$$\Rightarrow \Delta V_{gs} = \frac{nkT}{q} \ln\left(\frac{I_{D2}}{I_{D1}}\right)$$

$$\Rightarrow S = \frac{nkT}{q} \ln(10) = \frac{kT}{q} \ln(10) \left(1 + \frac{C_D}{C_{ox}}\right)$$

$$\text{Min. } S = \frac{kT}{q} \ln(10) \sim 60 \text{ mV / decade (for } n=1) \text{ at room temp (} T = 300 \text{ K)}$$

Typical values 60 - 100 mV / decade

Sub-threshold current



- Lower V_{th} exponentially increases the current but does not impact subth. Slope (a parallel shift of I_d - V_{gs} curve in the subth. region)
- Higher temperature exponentially increases the current and linearly increases the subth. slope

Next lecture (09/21)

- Recap of transistor I-V characteristics
 - Linear versus saturation + velocity saturation
 - Sub-threshold conduction
 - n-FET versus p-FET
- Short-channel effects
 - Drain-induced barrier lowering (DIBL)
 - V_T roll-off
- Device capacitances
- Device performance
 - Delay
 - Energy dissipation
- Inverter design