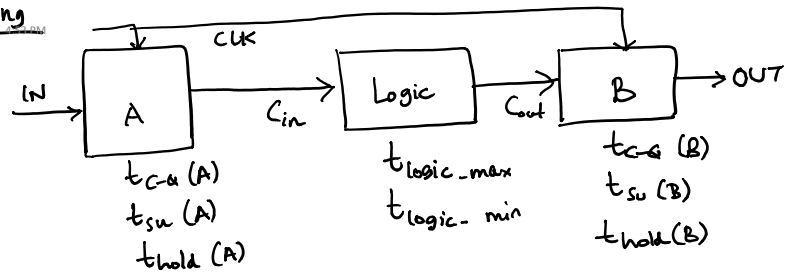
Clocking

Sunday, November 22, 2015 12:24 PM



Typically, the clock edges arrive together for Reg. A & B.
That is, $t_{CLK,A} = t_{CLK,B}$

Clock Frequency :-

$$t_{clk} = \underbrace{t_{c-q}(A)}_{\text{For "A"}} + t_{logic-max} + \underbrace{t_{su}(B)}_{\text{For "B"}}$$

The data arriving at Reg. A will be available after $t_{c-q}(A)$ at the logic block. The logic block will produce a delay of $t_{logic-max}$. And this data must be available $t_{su}(B)$ before the clock arrives at Reg. B.

Hold time :-

The hold time req. for Reg. B indicates that the input to Reg. B should NOT change for at least $t_h(B)$ time units after the clock edge. The soonest the data can arrive at the input of Reg. B is $t_{c-q}(A)\_min + t_{logic-min}$.

$$t_{hold}(B) \leq t_{c-q}(A)\_min + t_{logic-min}$$

Unfortunately, there are uncertainties in the clock arrival times. We categorize these into :- SKEW → spatial, JITTER → temporal

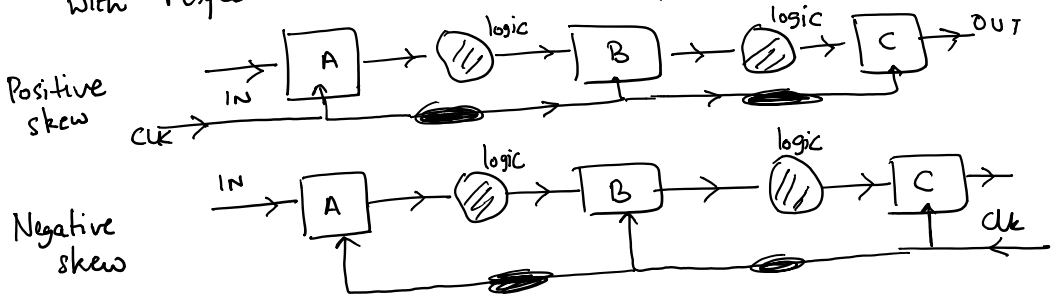
Clock skew is the spatial variation in temporally-equivalent clock edges. Clock skew depends on the routing direction. It is caused by static mismatches in the clock paths and differences in the clock load.

Clock skew → Positive
Clock skew → Negative

Positive clock skew :- Receiving edge arrives later than the launching edge

Negative clock skew :- Receiving edge arrives earlier than the launching edge.

The definitions of receiving & launching clock edge are with respect to the direction of data flow.



Positive skew analysis :

$$T_{clk} + \delta \geq t_{c-q} + t_{setup} + t_{logic-max}$$

(δ ↑ skew)

$$T_{clk} \geq t_{c-q} + t_{setup} + t_{logic-max} - \delta$$

Possibility to operate the circuit faster

However because of positive skew, there is a likelihood of hold violation!

$$\delta + t_h \leq t_{c-q(min)} + t_{logic-min}$$

$$t_h \leq t_{c-q(min)} + t_{logic-min} - \delta$$

→ stringent constraint on hold.

Worst case for race condition is when the receiving edge of the clock arrives late.

Negative skew analysis :

$$T_{clk} - \delta \geq t_{c-q} + t_{logic} + t_{su}$$

$$T_{clk} \geq t_{c-q} + t_{logic} + t_{su} + \delta$$

Clock frequency reduces with Negative skew.

In this case no race condition is ever possible.

Summary of clock skew :-

+ive :- improves performance + degrades reliability

-ive :- degrades performance + improves reliability.

Remember :- Worst case performance when receiving clock edge arrives early. ⇒ due to skew.

Worst case race condition when receiving clock

arrives early.

Worst case race condition when receiving clock edge arrives late.

⇒ due to skew.

Clock Jitter :

Jitter is the temporal variation in the arrival of clock edge at a given location on the chip. This leads to a change in the clock period.

Worst case performance due to both skew & jitter will be given as :-

$$T_{clk} \geq t_{c-q} + t_{logic} + t_{su} + \delta + 2t_{jitter}$$

Receiving edge arrives early & launching edge arrives late

Worst case for race condition due to skew & jitter :-

$$t_{hold} \leq t_{c-q\,min} + t_{logic\,min} - \delta - 2t_{jitter}$$

Launching edge arrives early & receiving edge arrives late

Performance worst case :-

Receiving edge early & launching edge late

Reliability or race condition worst case :-

Receiving edge late & launching edge early

⇒ Both jitter & Skew