ECE 6473

Sample Final Exam

Total time: 150 minutes

Maximum score: 100 points + 10 bonus points

Important notes and comments about the test:

- This question paper has **8 pages**.
- There are a total of **FIVE problems + ONE bonus problem worth 10 points.**
- Please ensure you have all the pages with all the problems.
- Use of calculator is allowed during the test. No laptop computer and cell phone.
- You are allowed ONE page (both sides) cheat sheet for the test.
- You have to return the question sheet back with your answer book. Do not take it home. You will lose all your credit if you take it home.
- Attach your cheat sheet with the answer book. You will receive only partial credit if your cheat sheet is missing.
- It is recommended that for numerical answers, you box your final answer so I can clearly read it.

Clearly mark your final answer so I can see it easily. If I am unable to read your handwriting, you will not get credit for the answer. Please write clearly.

Distribution of points per problem

Problem	Points
1. DRAM cell	20
2. Timing in synchronous circuits	30
3. Two-transistor memory cell	15
4. Transistor sizing	15
5. Short questions	20

1. DRAM cell (20 points)

Consider a DRAM cell storing logic "1".
The storage capacitance of the DRAM cell is $C_s = 50\,fF$ and the bit-line (BL) capacitance is $C_{BL} = 450\,fF$. The supply voltage $V_{DD} = 3.0$V and the threshold voltage of the access device $V_T = 0.5$ V. The word-line (WL) is NOT boosted. The constant leakage through the capacitor is 250 pA.
At time t = 0, the WL is brought to low (cell is storing "1").

A read operation is initiated at time t = 100 µs, by elevating the WL to V_{DD}. Assume for the read operation, the BL is pre-charged to $V_{pre} = V_{DD}/2$.
Answer the following:

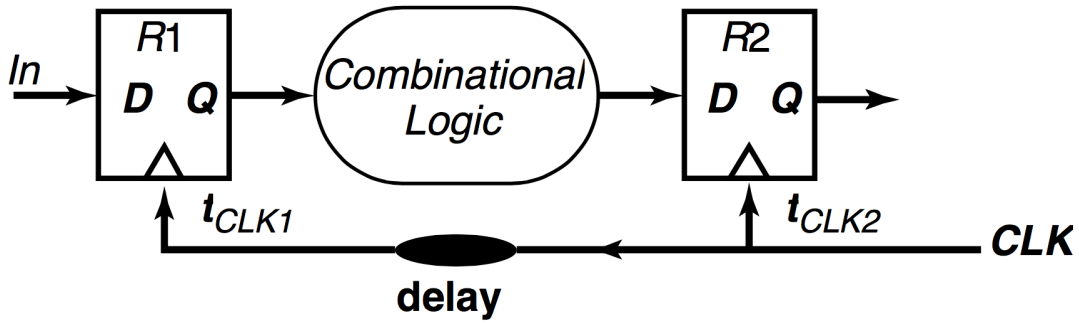
a) What is the maximum voltage (V_{max}) and the charge stored in the cell capacitor (C_s) at $t = 0$? **(2 points)**
b) What is the voltage stored in the capacitor at the time of the read operation at t = 100 µs? **(3 points)**
c) What is the BL voltage and the voltage stored in the cell capacitor after the read operation is over? **(5 points)**

Next consider, the read operation started at t = 10 ms.

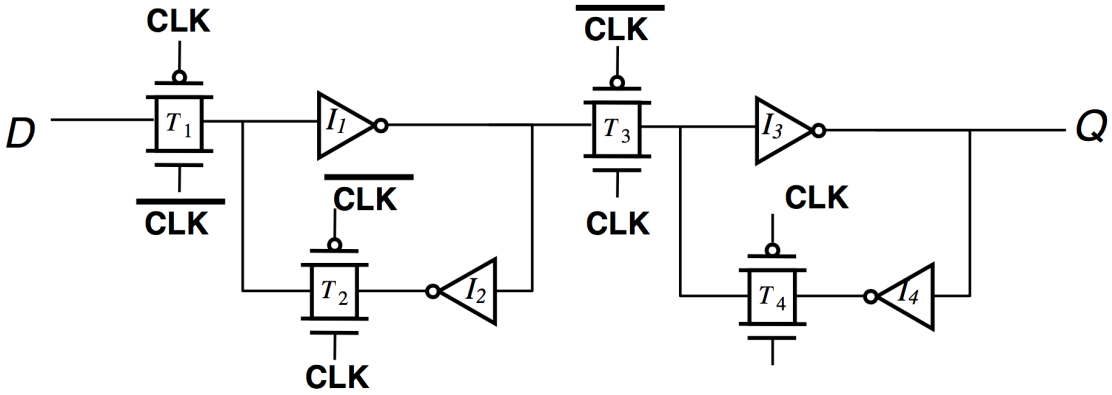
d) What is the value stored in the cell capacitor at the start of the read operation at t = 10 ms? **(4 points)**
e) What is the voltage stored in the cell capacitor after the read operation is over? **(3 points)**
f) Is the read operation correct (i.e. what logic value has been read)? **(3 points)**

2. Timing in synchronous circuits (30 points)

Consider the following circuit:



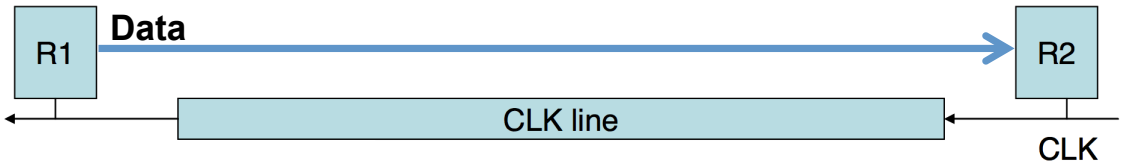
The flip-flops are designed using the following master-slave configuration and the delay characteristics:



Delay of transmission gate = 50 ps
Delay of inverter = 50 ps

The logic circuit has the following delay characteristics:
Maximum delay = 500 ps
Minimum delay = 100 ps

The clock between R1 and R2 goes through the following signal line as shown.



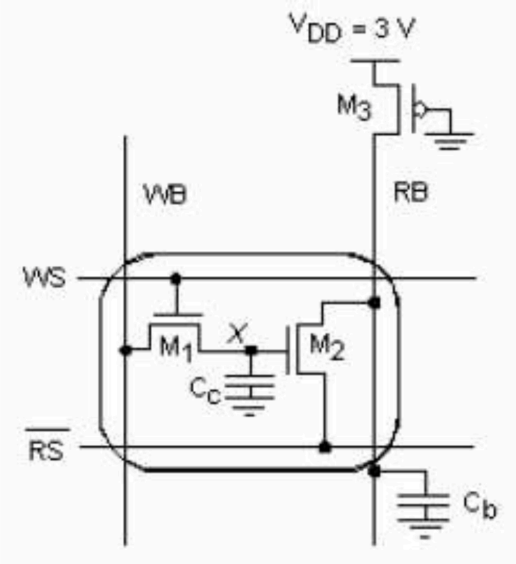
The resistance and the capacitance characteristic of the interconnect are as follows:
Resistance per unit length (r) = 0.1 Ω/µm
Capacitance per unit length (c) = 0.2 fF/µm
Length of the clock line = 2 mm

Answer the following questions:

a) What is the set-up time, clock-to-Q delay, and hold time of the master-slave flip-flop? **(5 points)**
b) Draw the equivalent circuit model of the interconnect (consider the distributed π model). What is the clock skew between R1 and R2? Is the skew positive or negative? **(6 points)**
c) What is the worst-case clock frequency the circuit can operate at? **(3 points)**
d) Can there be a hold violation? **(3 points)**
e) If you had considered lumped interconnect model in part (b), would the worst-case clock frequency of the circuit computed in part (c) increase or decrease? Explain your answer. **(3 points).**
f) To minimize the delay of CLK signal from R2 to R1, I decide to add inverters into the CLK line. However, I decide to add inverters that are bigger than the minimum size, say by a factor of '$s = 2$'. Assuming the delay of a minimum-sized inverter in the technology is 10 ps, find (i) optimal number of inverters to minimize the delay and (ii) the optimal delay of the CLK after inverters. What is the percentage improvement in delay after adding repeaters? **(10 points)**

Problem 3: Two-transistor memory cell (15 points)

Consider the 2-T memory cell shown below. The data is stored on the capacitor denoted as C_c on node X.



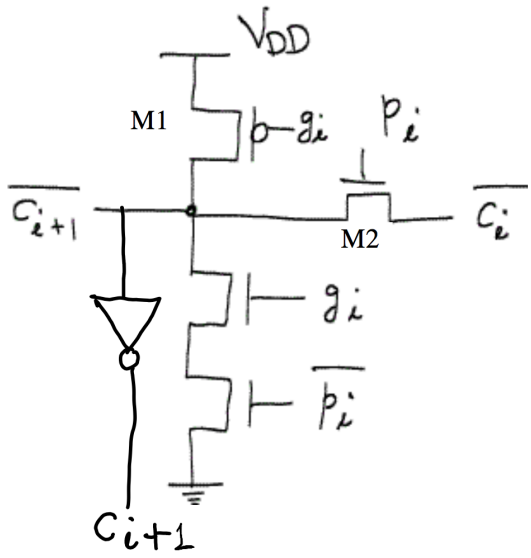
a) Describe the read and write operation of the memory. Explain what should be the logical values of different signals to perform the read and write operations. Mention the voltage levels for logic "0" and logic "1" of the cell. Do you have a destructive read operation? **(8 points)**

b) Determine the maximum current through M2 during a read operation. Make appropriate assumptions about the operating region of M2. Assume, μ_n = 200 cm^2/Vs, $\varepsilon_{ox} = 3.9 \times 8.85 \times 10^{-12}$ F/m, $(W/L)_{M2} = 1$, T_{ox} = 5 nm, V_{DD} = 2.5V, V_t = 0.5V. Ignore channel length modulation and body effects in the analysis. **(3 point)**

c) Compute the time it takes to achieve a 0.5V voltage drop on the bit-line during a read operation. Assume C_c = 50 fF, C_b = 2pF. Neglect the PMOS (M3) current for your computation (as if PMOS is connected to a pre-charge signal). Ignore channel-length modulation and body effects in the analysis. **(4 points)**

Problem 4: Transistor sizing (15 points)

Consider the following circuit. This circuit is actually one stage of the Manchester-carry circuit.

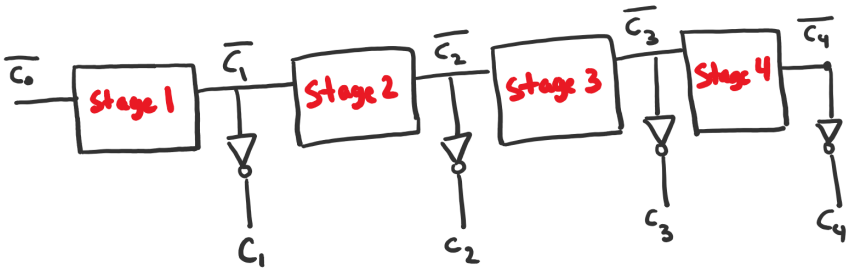


The input conditions for carry C_i to propagate to C_{i+1} stage is $p_i = 1$ and $g_i = 0$.

Answer the following questions:

a) What should be the ratio of the widths of M1 and M2 to ensure that while carry propagation ($p_i = 1$ and $g_i = 0$), a logic "0" is 0.1 V? **(5 points)**

b) If the above stage is used to construct a 4-stage Manchester carry chain, what will be the physical voltage levels at the end of 4th stage if the carry propagates to all the stages. Assume that the voltage drop across each NMOS is small so that 2nd order terms can be neglected. To answer this question, see the following circuit. **(10 points)**

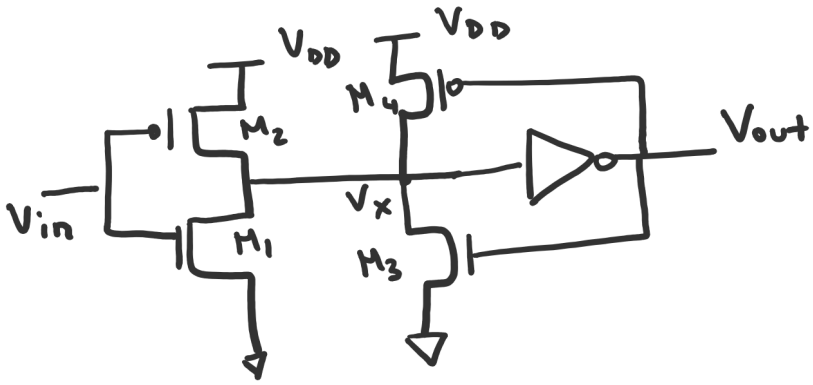


Problem 5: Short questions—comprehensive understanding (20 points)
No points without proper justification

a. Consider a 4-stage logic path where each stage has effort of 12, 9, 6, and 6 time units, respectively? Can this design be improved for delay? What changes will you recommend? Justify your answer quantitatively. **(5 points)**
b. How should the ratio of V_t/V_{DD} be changed to reduce the total power dissipation in the circuit? That is, should V_t/V_{DD} be increased or decreased? Here, V_t is threshold voltage and V_{DD} is supply voltage. **(4 points)**
c. If I came up with a new device technology where $\kappa_n = \kappa_p$, how much area would I save to implement a minimum sized inverter when compared with a technology where $\kappa_n/\kappa_p = 2.5$? Ignore area in contacts and only consider area consumed by transistors. **(4 points)**
d. If the worst-case delay of a minimum-sized 2-input NAND gate in a technology is 50 ps, what would be the delay of a 4-input NAND gate that is sized 5×? Consider no external fan-out. **(3 points)**
e. If the delay of a wire with width = 100 nm is 100 ps, what would be the delay of the wire with width = 50 nm, if all other physical properties of the wire were the same? Ignore fringing capacitance of the wire. **(4 points)**

Bonus problem: Complex circuit functionality (10 points)

Consider the circuit shown below. Assume that the inverter is ideal with $V_m = V_{DD}/2$, where V_m is the switching threshold of the inverter.



Draw the voltage-transfer characteristics (i.e. V_{out} versus V_{in}) of the circuit. Explain your answer.