

HW-3

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Problem 1

a

$$Y = \overline{(B + A) \cdot C \cdot D} \quad (1)$$

b

As from the figure, suppose β_N denotes β for NMOS used in this design, β_n denotes β for NMOS in equivalent generic design. And β_P and β_p respectively. Thus we have $\beta_P = 2\beta_p$ and $\beta_N = 3\beta_n$. Thus for MOSFET really used in this design

$$\begin{aligned} \frac{W}{L}_{NMOS} &= 3 \\ \frac{W}{L}_{PMOS} &= 4 \end{aligned} \quad (2)$$

c

Suppose internal capacitance for each NMOS is C_n , and C_p for PMOS respectively.

Initial State	Final State	Delay
$A_1B_0C_1D_0$	$A_1B_0C_1D_1$	$t_{pHL} \propto 3R_NC_N + R_NC_Y$
$A_0B_1C_1D_0$	$A_0B_1C_1D_1$	
$A_0B_1C_1D_1$	$A_0B_0C_1D_1$	$t_{pLH} \propto R_PC_P + R_PC_Y$

Problem 2

a

$$\begin{aligned} E_{total} &= E_r + uE_r + \dots + u^N E_r \\ &= E_r \frac{u^{\frac{\ln \frac{C_L}{C_1}}{\ln u} + 1} - 1}{u - 1} \end{aligned} \quad (3)$$

b

For each inverter, there is $t_{pj} = u\tau_r$. Thus for each step, Energy-Delay Product is $EDP_j = ju^j E_r u \tau_r = ju^{j+1} E_r \tau_r = ju^{j+1} EDP_{ref}$. Thus,

$$\begin{aligned} EDP_{chain} &= EDP_{ref} + u^2 EDP_{ref} + 2u^3 EDP_{ref} + \dots + Nu^{N+1} EDP_{ref} \\ &= EDP_{ref} \left(1 + \frac{u^2 \left[\left(\frac{\ln C_L / C_1}{\ln u} (u-1) - 1 \right) u^{\frac{\ln C_L / C_1}{\ln u}} + 1 \right]}{(u-1)^2} \right) \end{aligned} \quad (4)$$

Thus, normalized Energy-Delay Product is,

$$\frac{EDP_{chain}}{EDP_{ref}} = 1 + \frac{u^2 \left[\left(\frac{\ln C_L / C_1}{\ln u} (u-1) - 1 \right) u^{\frac{\ln C_L / C_1}{\ln u}} + 1 \right]}{(u-1)^2} \quad (5)$$

For optimal 'u' of minimum normalized EDP,

$$\begin{aligned} 0 &= \frac{u^2 \left[u^{\frac{\ln C_L / C_1}{\ln u}} \left(\frac{\ln C_L / C_1}{\ln u} - \frac{(u-1) \ln C_L / C_1}{u \ln^2 u} \right) + \left(\frac{u^{\frac{\ln C_L / C_1}{\ln u} - 1} \ln C_L / C_1 - \frac{u^{\frac{\ln C_L / C_1}{\ln u}} \ln C_L / C_1}{u \ln u} \right) \left(\frac{(u-1) \ln C_L / C_1}{\ln u} - 1 \right) \right]}{(u-1)^2} \\ &\quad + \frac{2u \left[u^{\frac{\ln C_L / C_1}{\ln u}} \left(\frac{(u-1) \ln C_L / C_1}{\ln u} - 1 \right) \right]}{(u-1)^2} \\ &\quad + \frac{2u^2 \left[u^{\frac{\ln C_L / C_1}{\ln u}} \left(\frac{(u-1) \ln C_L / C_1}{\ln u} - 1 \right) \right]}{(u-1)^3} \end{aligned} \quad (6)$$

c

For condition of (b), $u \approx 3.996934$. For optimal 'u' for minimum delay, $u = e \approx 2.718282$.

Problem 3