PART-I: DECODER LOGIC AND WORD- LINE GENERATION FOR 256-BIT SRAM REPORT

Group3

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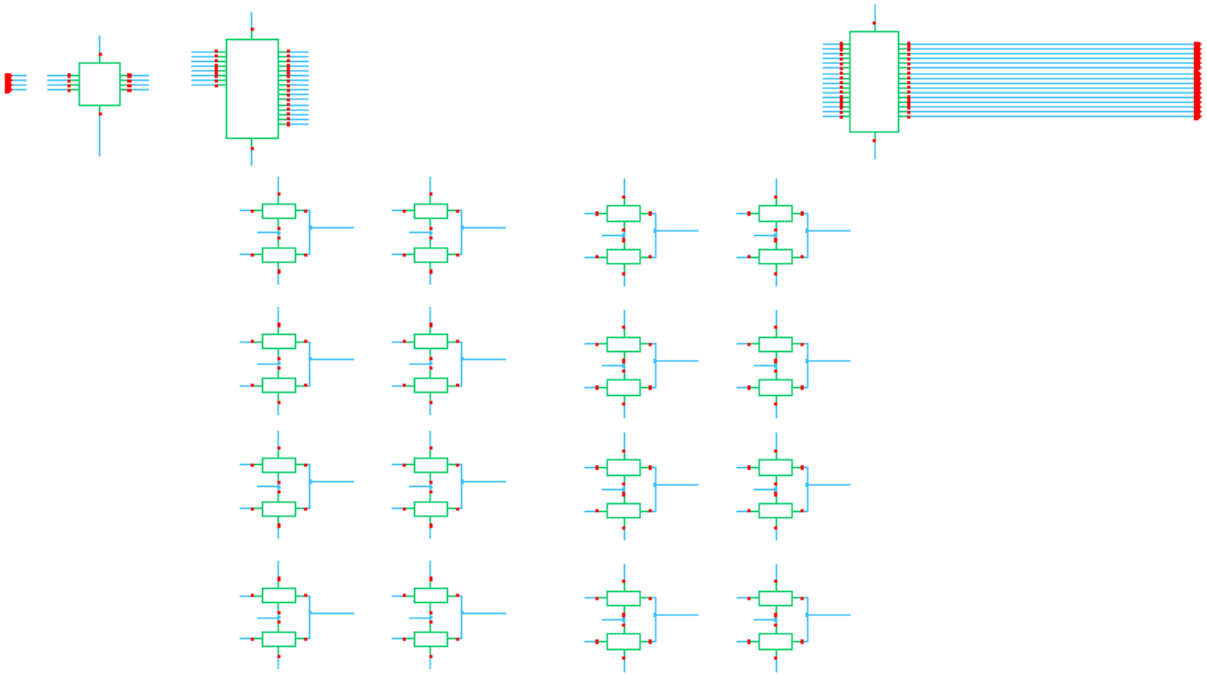
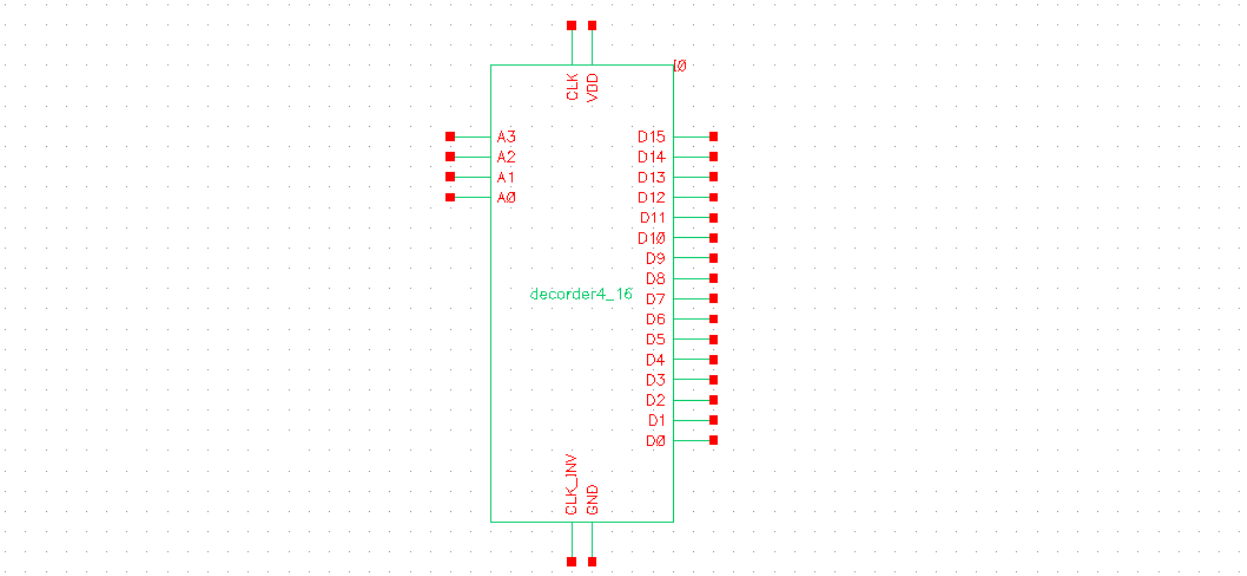
Overall schematic:

Overall schematic and top-level schematic of 4-16 decoder:

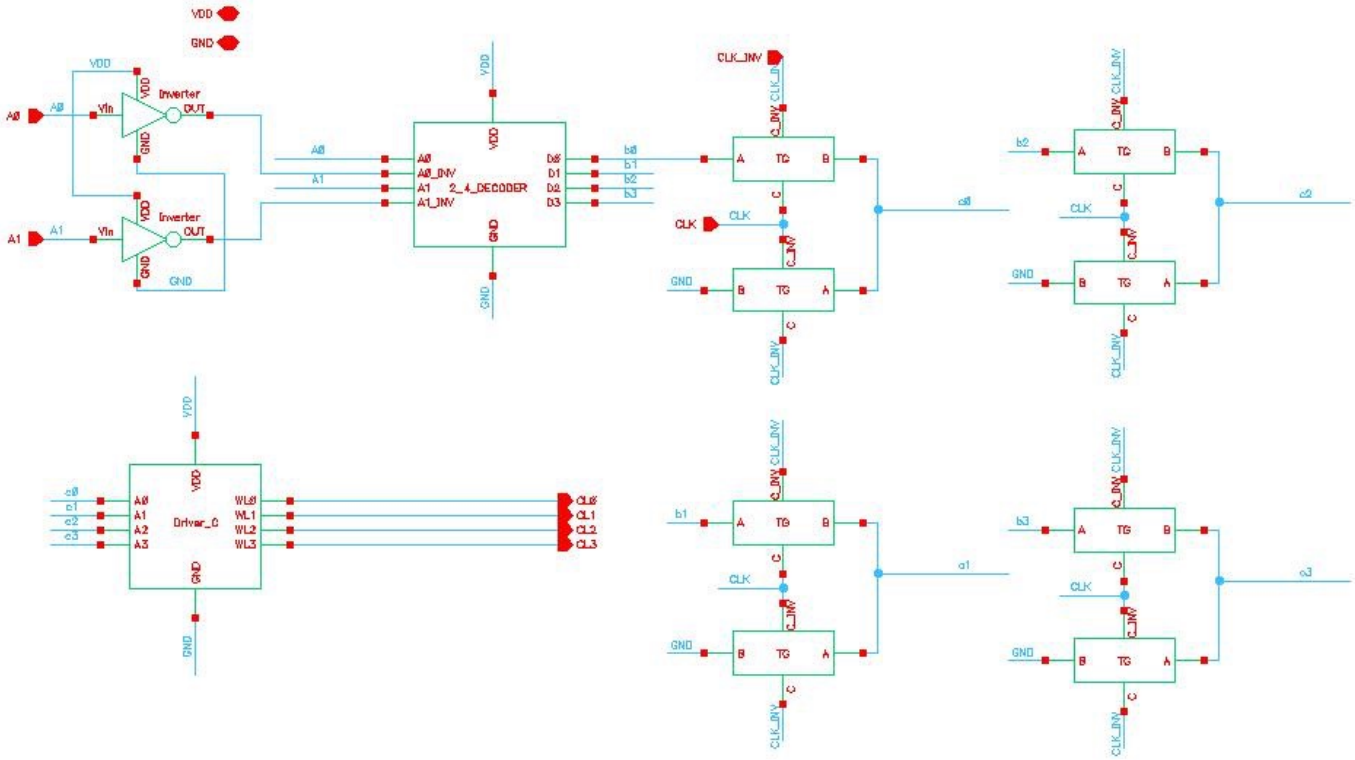
Inverter —> 4-16decoder —> WL generation —> drive —> output



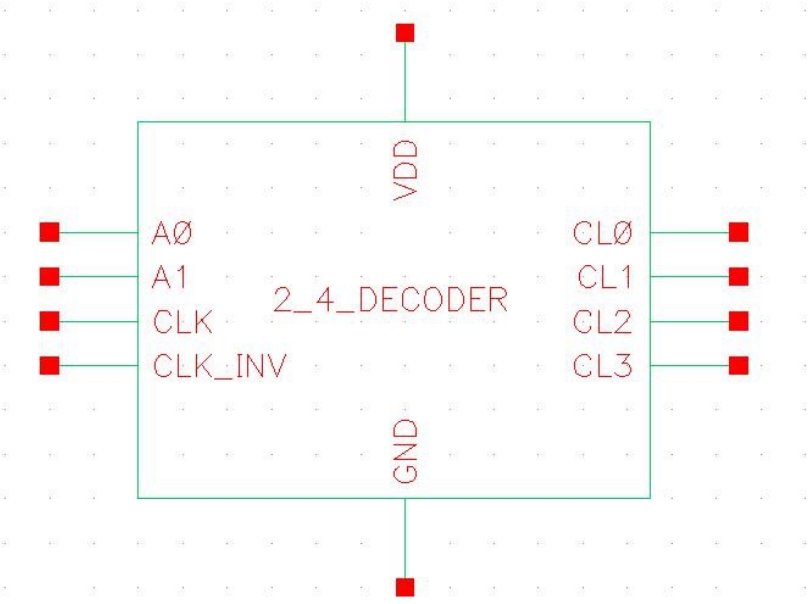
Symbol:



Overall schematic and top-level schematic of 2-4 decoder:



Symbol:



1. Circuit Design

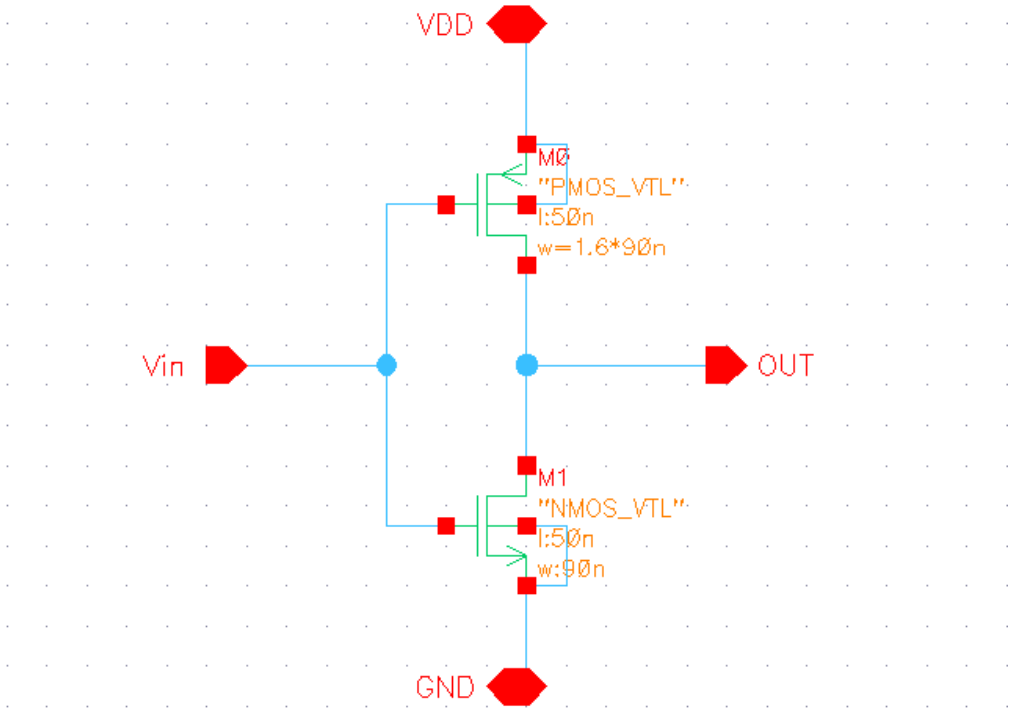
This partial report is the first partial report for course project of course Intro to VLSI Design.
And this report covers:

(1) Address Decoder as well as mention to Column Decoder of complete design of the 256-bit SRAM;
(2) WL generation circuit.
(3) Driver circuit.

1.1 The basic component

1.1.1 Inverter

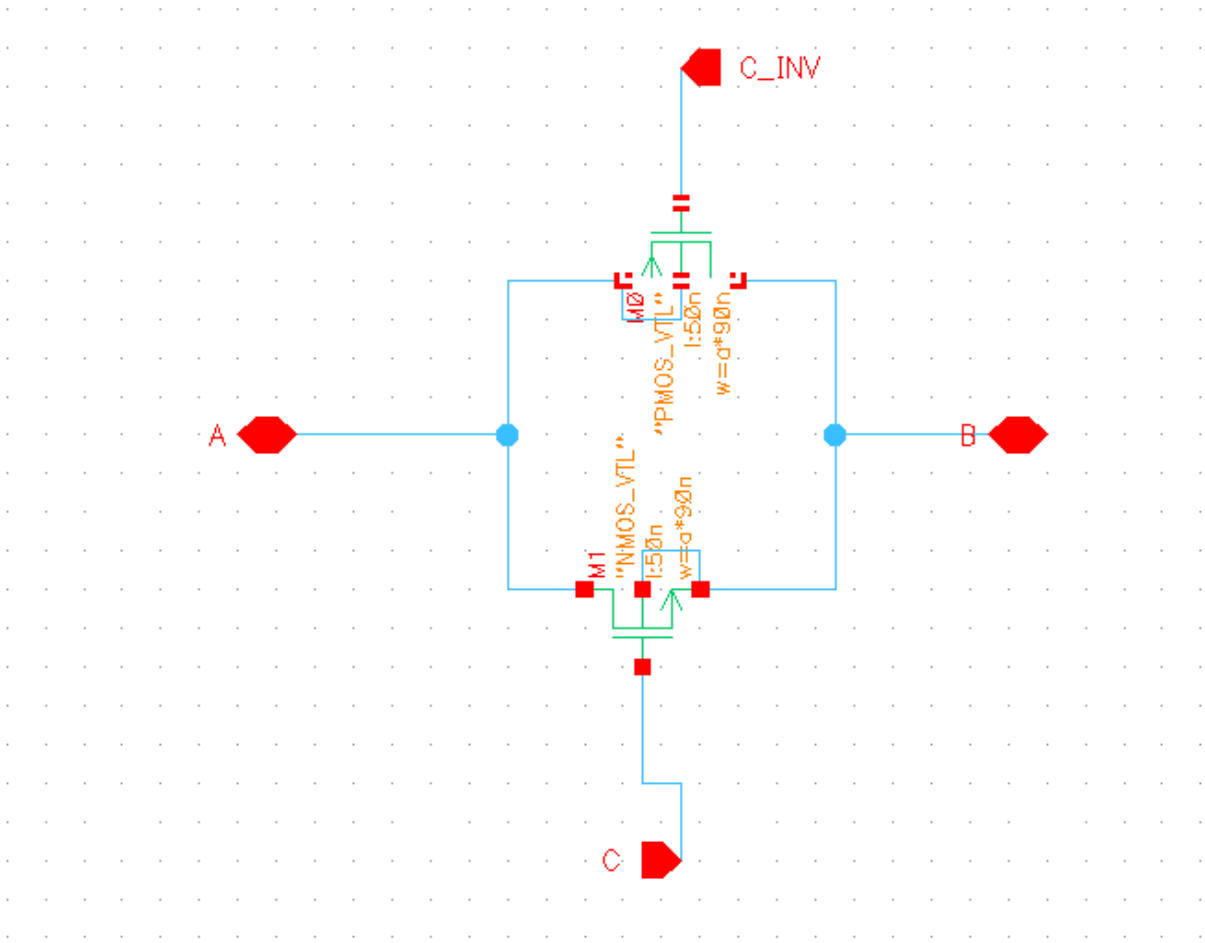
The overall big component is composed by the inverter and transmission gate. So, we list these two things first.
Here is the structure of inverter:



[Figure inverter]

The ratio of width for PMOS is r=1.6. We will discuss this value later.

1.1.2 Transmission gate
For the structure of transmission gate:



The width of PMOS and NMOS will be set later based on the minimal value of delay theory. And it is just set as a variable here.

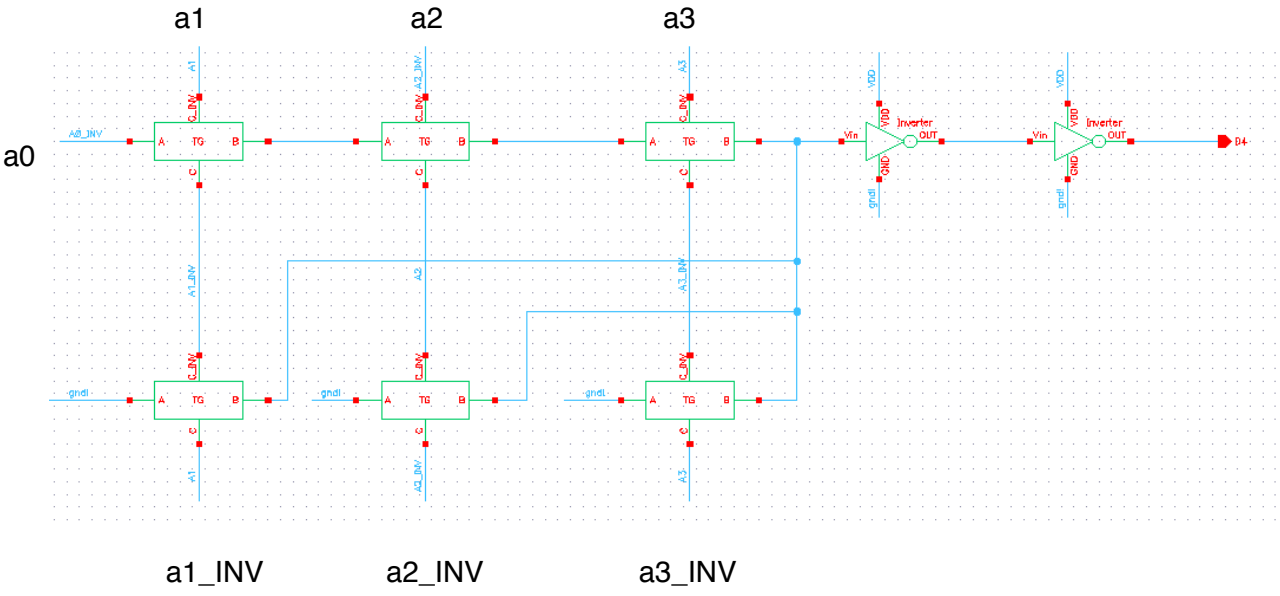
1.2 Address Decoder:

1.2.1 4-16 Row Address Decoder:

The address is represented by a3 a2 a1 a0

Output	Expression	Output	Expression	Output	Expression	Output	Expression
D0	0000	D4	0100	D8	1000	D12	1100
D1	0001	D5	0101	D9	1001	D13	1101
D2	0010	D6	0110	D10	1010	D14	1110
D3	0011	D7	0111	D11	1011	D15	1111

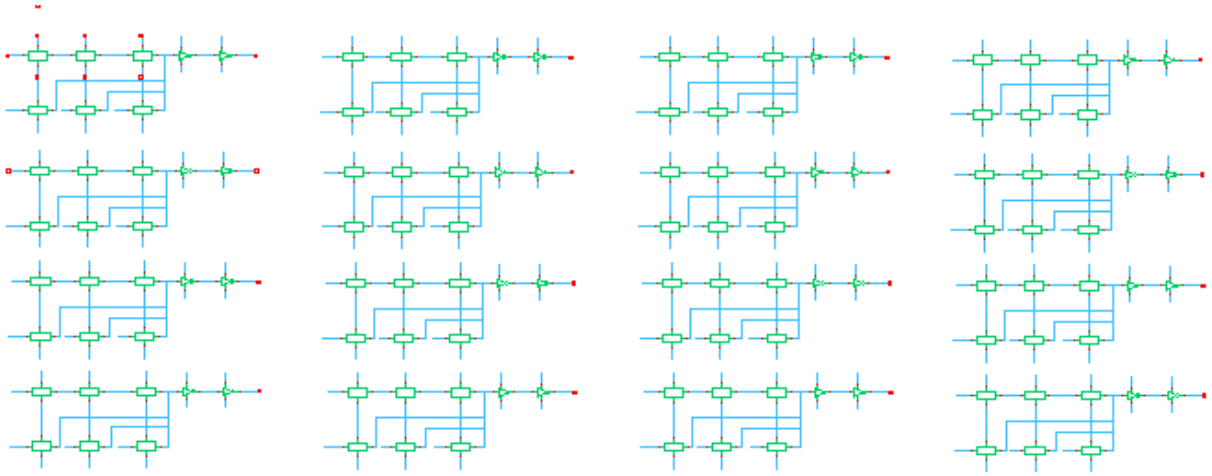
The logic of Decoder is implemented using transmission gate, taking the circuit design



[Figure: Schematic Design of a Cell of 4-16 decoder]

The logic of output is S= a0 * a1 * a2 *a3

The design of the 4_16 Decoder is simply repeating this cell for D0 D2…D15, with different inputs signal.

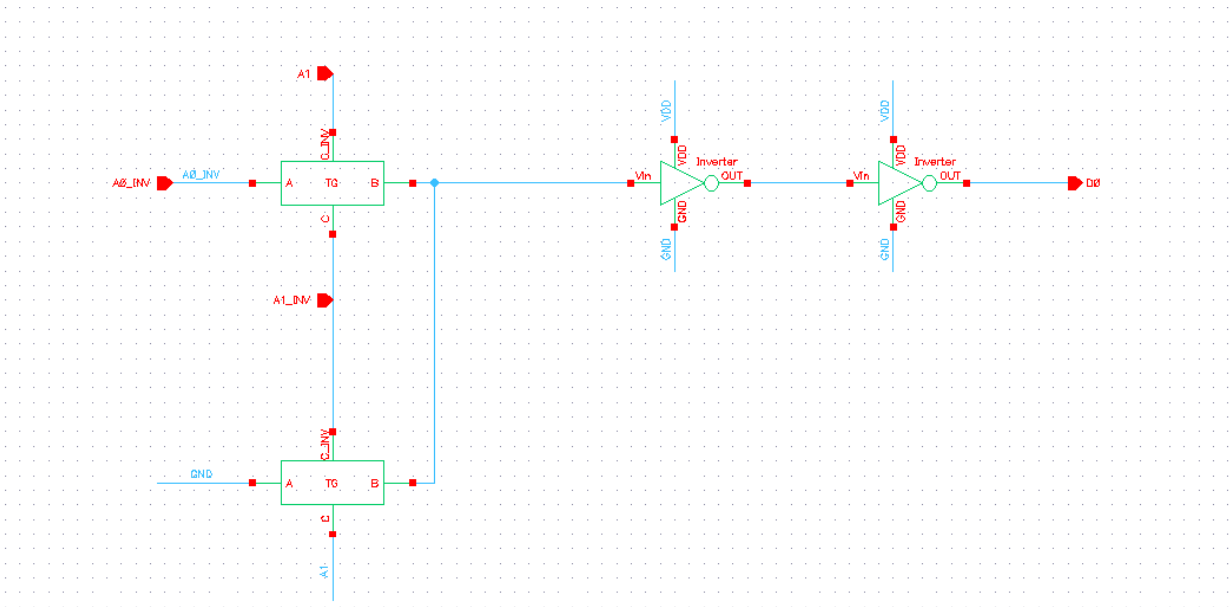


[Figure: Schematic Design of 4-16 decoder]

1.2.2 2-4 Column Address Decoder:

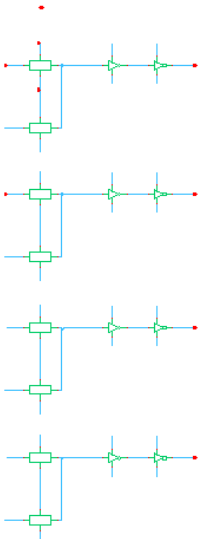
The address is represented by a6 a5

Output	Expression
D0	00
D1	01
D2	10
D3	11



[Figure: Schematic Design of a Cell of 2-4 Decoder]

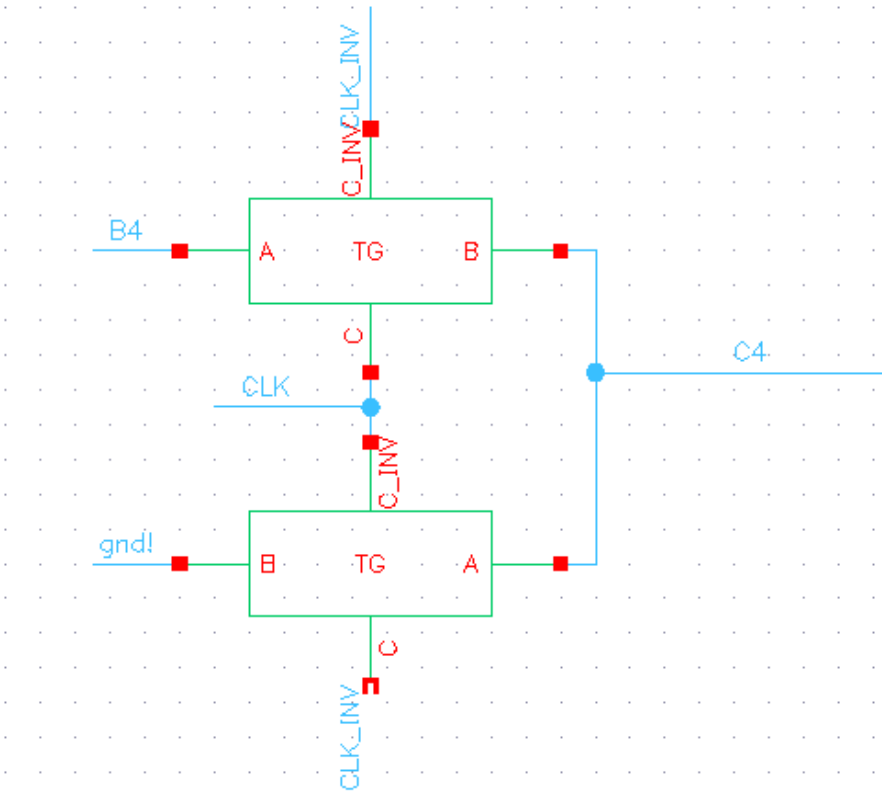
The design of the 2_4 Decoder is simply repeating this cell for D0 D2…D3, with different inputs signal.



[Figure: Schematic Design of 2-4 Decoder]

1.3 WL generation circuit.

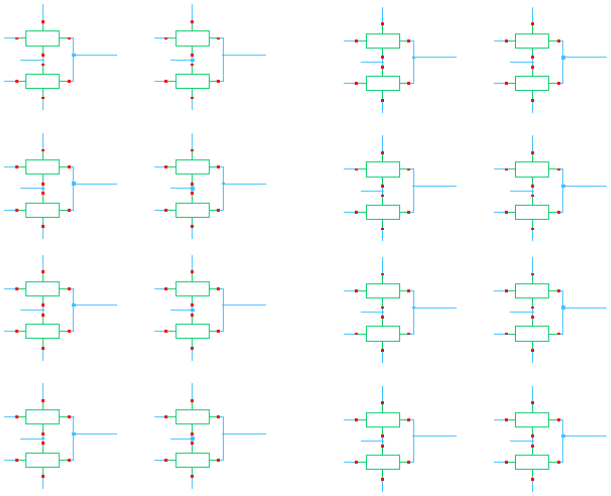
D_X is the output of the Decoder.



[Figure : Schematic Design of a Cell of WL generation]

This can be termed as a 2-1Mux. The write or read signal will be added to CLK and CLK_INV. We use the write or read signal to choose whether WL will be charged to 1. And the terminal of B4 is the output of decoder. The terminal B of second TG will connected to GND.

The whole WL generation circuit consists 16 Cells as shown below for each WL signal.

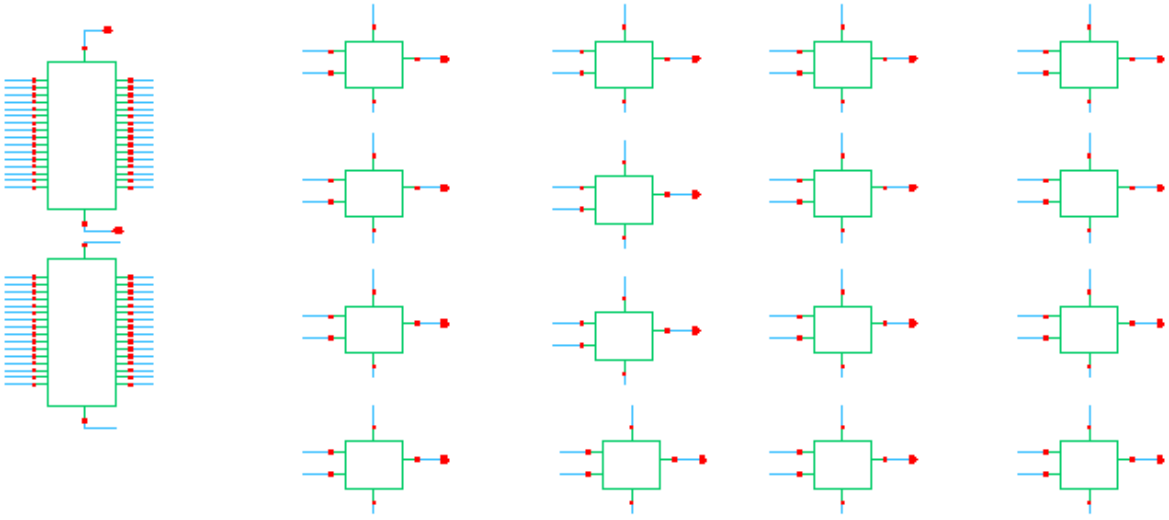


[Figure: Schematic Design of WL generation circuit]

1.4 Driver

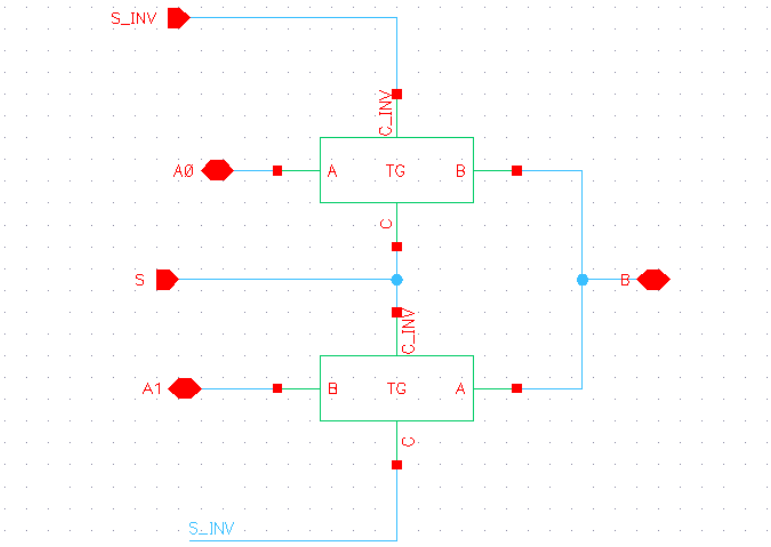
Instead of driving the Load capacitance using the signal generated by the WL generation circuit, a driver is added for the 40fF load. Drive is also used to maintain the output to reach VDD (1V).

The main components of the driver is 2-1 Mux. The outputs of the WL generation circuit are applied as ‘Select signal’ for the gate of the transistors. The Drain of the transmission gates are either connected to global ground or Vdd.



[Figure: Schematic design of driver]

The driver is composed of one 16-bit TG, one 16-bit inverter and 16 2-1 mux. The 16-bit inverter is to get the compliment signal of the output of last level and the 16- bit -TG is used to achieve the parallel to avoid glitch. So, the a0 and a0_inv will have approximately same delay. So, it will input to 2-1 mux approximately at same time.



[Figure: Schematic design of a driver cell for drive]

The main components of the driver is 2-1 Mux. The outputs of the WL generation circuit are applied as ‘Select signal’ for the gate of the transistors. The Drain of the transmission gates are either connected to global ground or Vdd.

Same driver cell is applied for each output of the WL generation circuit.

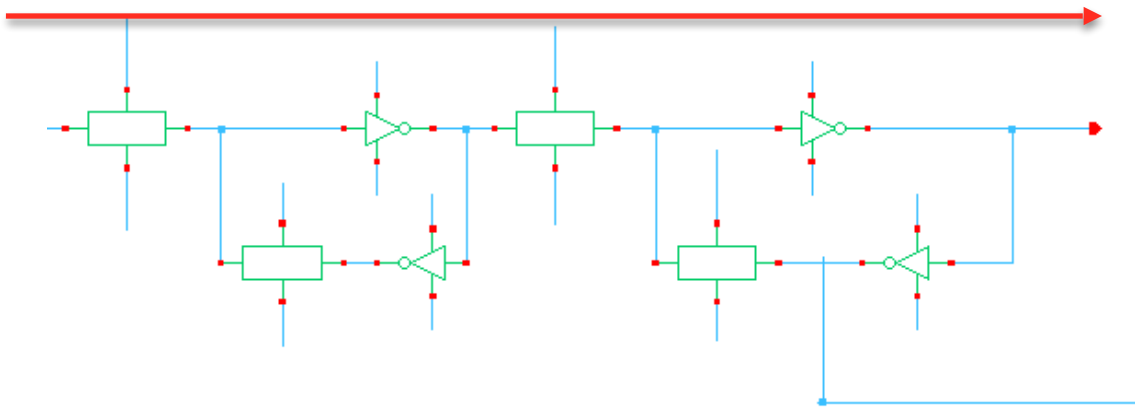
2. Analysis and Sizing.

--Theoretically sizing every devices based on the minimal delay (The reference Cref is to minimal inverter)

2.1 Find the Critical Path:

Altrough we do not add the register in this stage, we should add this for further stage, so when we sizing the critical path. We should add this in our critical path to get more exact and correct calculation result.

1.Address register



1.1 Analysis of critical path in this device:

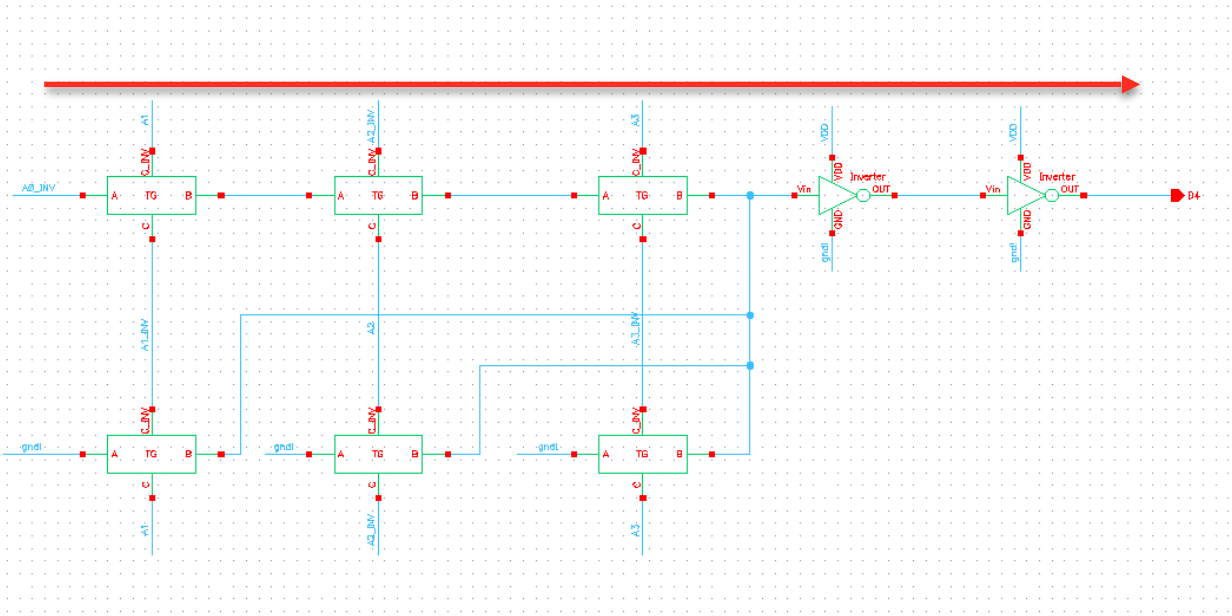
As shown in the picture, the first stage in schematic is a register. So in the register, the first stage is a Transmission gate. Then, the second stage is an inverter. The third stage is a Transmission gate. Also, the last stage is an inverter. In this scenario, the input capacitance of inverter is 1+r and the input capacitance of transmission gate is 2. And in this project, the optimal value of r is 1.55 to get same Tplh and Tphl with VDD=1V. So, the input capacitance of inverter is near 2.55 and input capacitance of transmission gate is near 2. So, theoretically and after testing by ourselves. The delay of inverter is more than transmission gate a little. In this way, the inverter should be termed as critical path. And the transmission gate should be termed as branching path. So the critical path is : **TG—> inverter —> TG—> inverter**

1.2 Analysis of logic effort, branching effort

In this register, the logic effort, branching effort for every stage are shown below:

Stage	Device name	Logic effort (g)	Branching effort (b)
1	TG	2/(1+r)	(3+r) / (1+r)
2	inverter	1	(3+r) / 2
3	TG	2/(1+r)	(3+r) / (1+r)
4	inverter	1	(3+r)/2

For the stage 4:
Because the branching effort of stage 4 should consider the input of next device, it will be analyzed in next device.



2. 4 to 16 Decoder

2.1 Analysis of critical path in this device:

As shown in picture, the critical path in this device is one transmission gate and one inverter. The reason that I choose first TG as critical path is that the input of A_inv signal

is from the register of last stage. Regardless of its branching effort, the GH value is same to TG. So, we only need add one in our critical path.
So the critical path is : **TG —> TG —> TG —> inverter —> inverter**

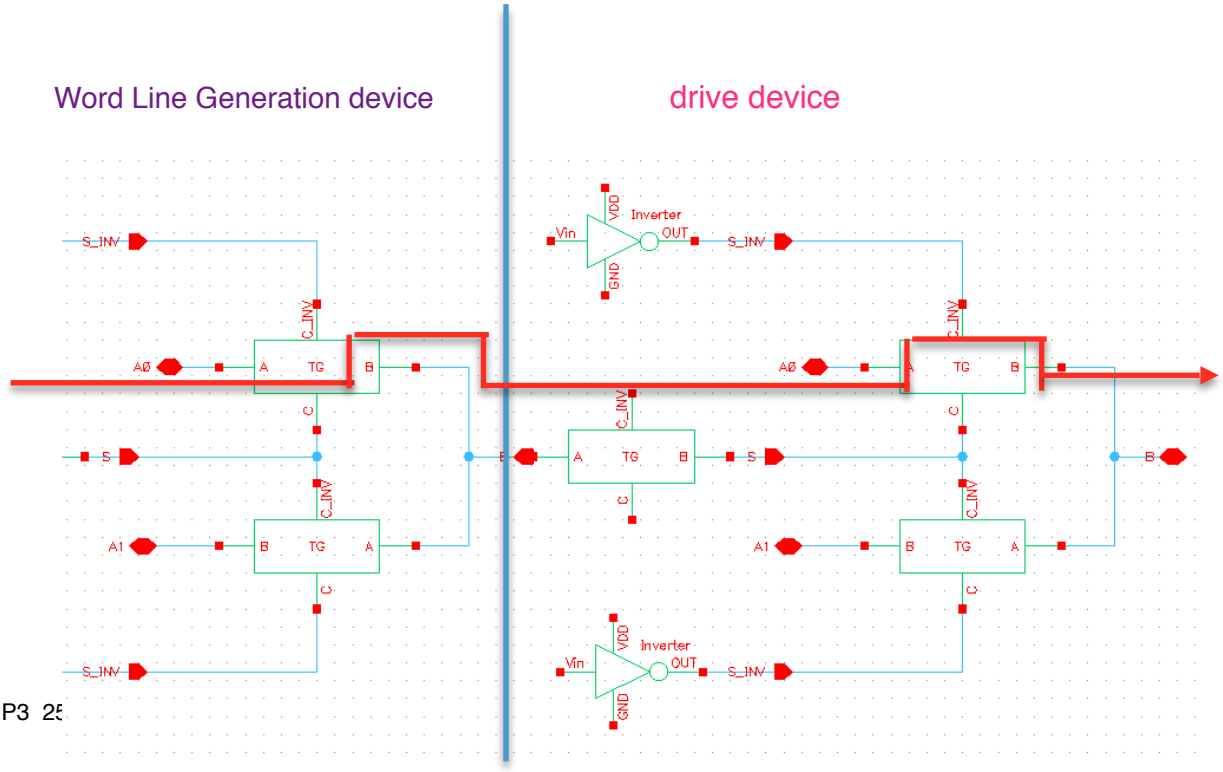
2.2 Analysis of logic effort, branching effort

In this register, the logic effort, branching effort for every stage are shown below:

Stage	Device name	Logic effort (g)	Branching effort (b)
5	TG	2/(1+r)	1
6	TG	2/(1+r)	1
7	TG	2/(1+r)	(7+r)/(1+r)
8	inverter	1	1
9	inverter	1	(3+r)/2

For the branching effort of stage 4:
The branching effort of stage 4 should consider the input of this device. As shown in picture, the output of stage 4 includes one transmission gate and one inverter in register. So, the branching effort should be calculated for these two devices.

3. The Word Line Generation device and drive device



3.1 Analysis of critical path in this device:
In this device, the critical path is unusual. Because the inverter is not termed as in critical path but the transmission gate. The reason is that the output of transmission gate has branching but inverter not. Both considering the branching effort and logical effort we find that the transmission path has more effort for the transmission gate g*h=2*2 but inverter g*h = 2.55*1. So we should choose the transmission gate as critical path.
So the critical path is : **TG —> TG —> TG**

3.2 Analysis of logic effort, branching effort
In this driver, the logic effort, branching effort for every stage are shown below:

Stage	Device name	Logic effort (g)	Branching effort (b)
10	TG	1 / (1+r)	(3+r) / 2
11	TG	2 / (1+r)	2
12	TG	1 / (1+r)	1

Size every device based on the theoretical value of every stage:

H = 59.9161

GB =32.1146

F = G * H * B = 1924.2

f = (F) ^ (1/N) = 1.7891

Stage	Device name	Logic effort (g)	Branching effort (b)	Electrical effort (h)	Ratio to Cref (Real setting)
1	TG	0.7716	1.7716	1.3721	1.3721
2	inverter	1	2.2960	0.8169	1.1209
3	TG	0.7716	1.7716	1.3721	1.5380
4	inverter	1	2.2960	0.8169	1.2565
5	TG	0.7716	1	2.4309	3.0543
6	TG	0.7716	1	2.4309	7.4244
7	TG	0.7716	3.3148	0.7333	5.4446
8	inverter	1	1	1.8757	10.2121
9	inverter	1	2	0.9378	9.5772
10	TG	0.7716	2.2960	1.0587	10.1397
11	TG	0.7716	2	1.2154	12.3241
12	TG	0.3858	1	4.8617	59.9161

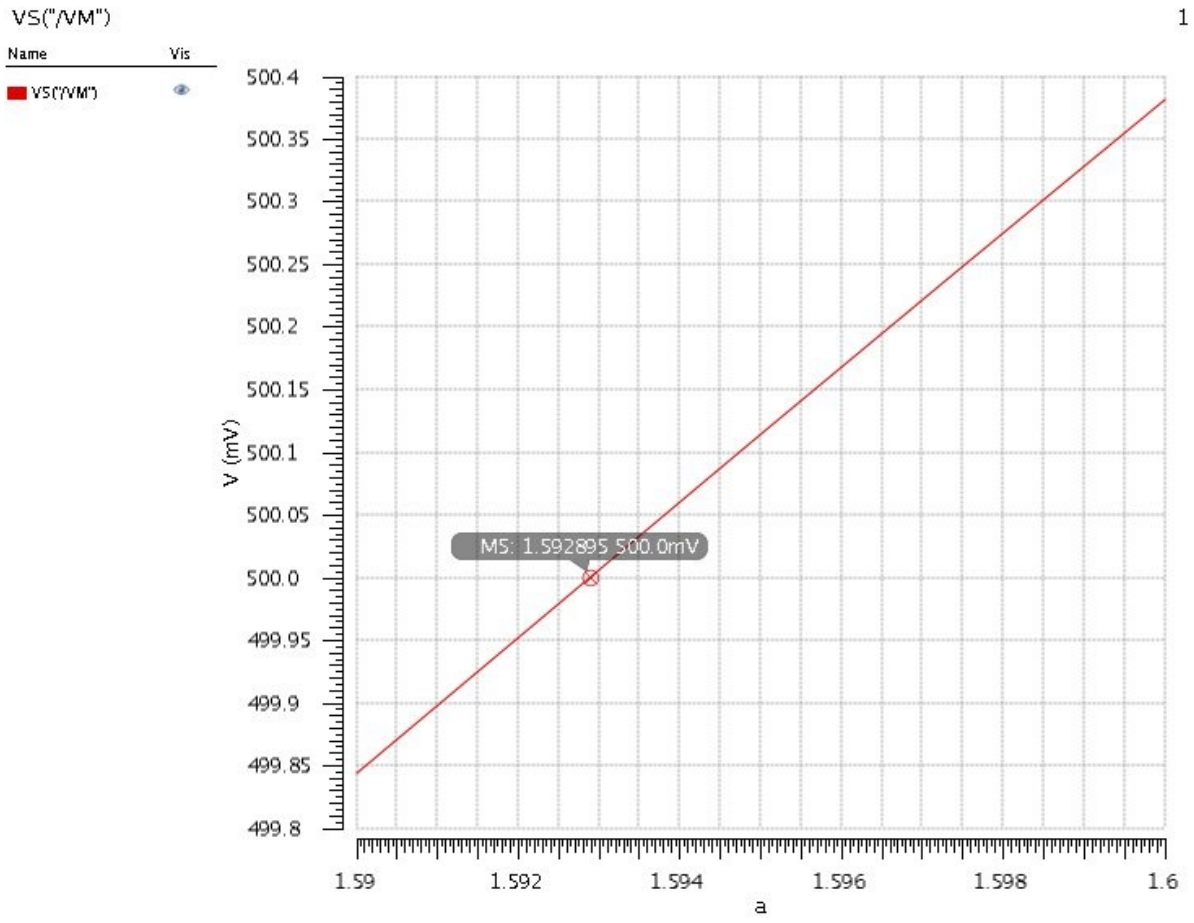
[Table: The calculation of effort]

The value of Ratio to Cref is the real value we want to set. And for the stage 6-11. We can see the range is from 3-12. So we take the 6 for average value of ratio we set for both NMOS and PMOS. But for the last level, we can see it is very high. So the influence of last level is obviously most. So we should pay more attention to this part. We exactly get the optimal value of last level through cadence (parameter analysis tool), which will be explained at next part.

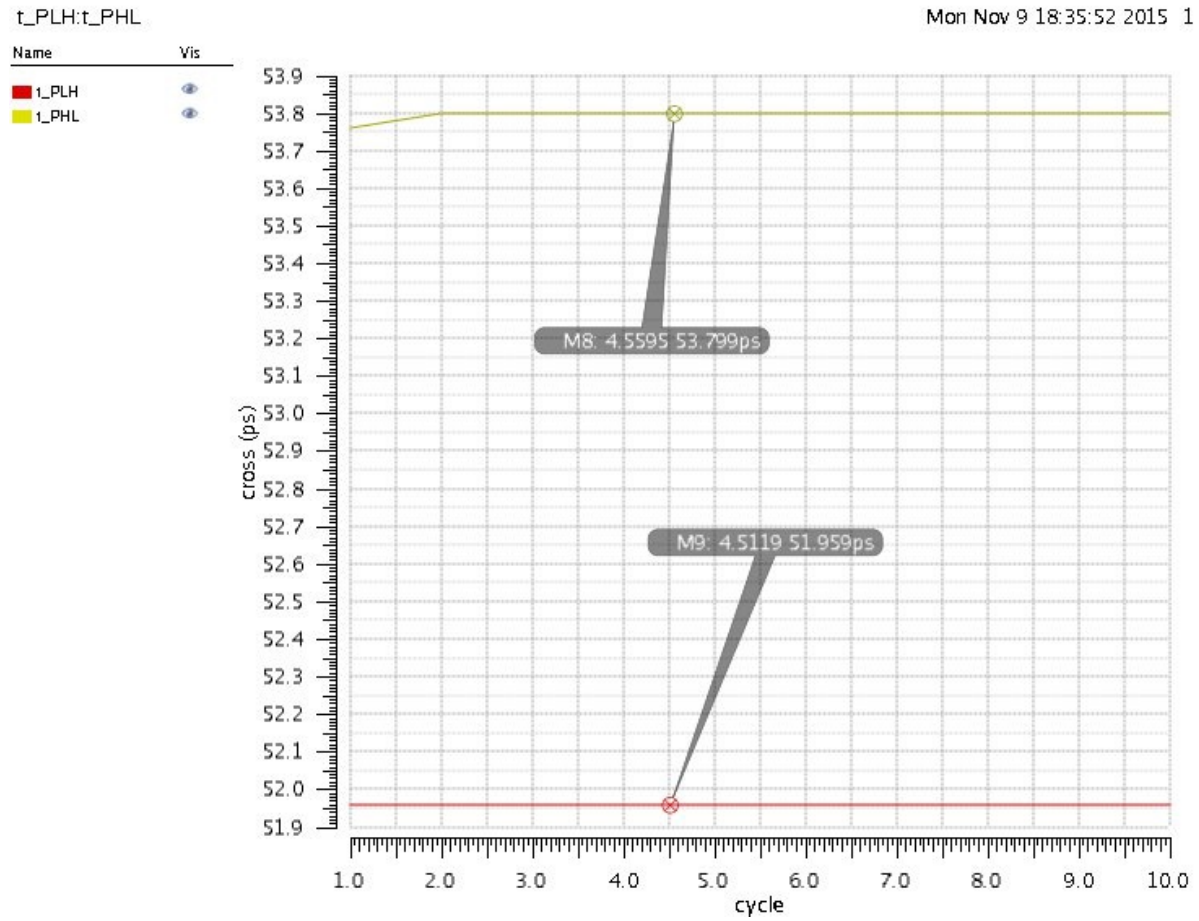
1.3 Some consideration in real design:

Component:

1.3.1 Inverter

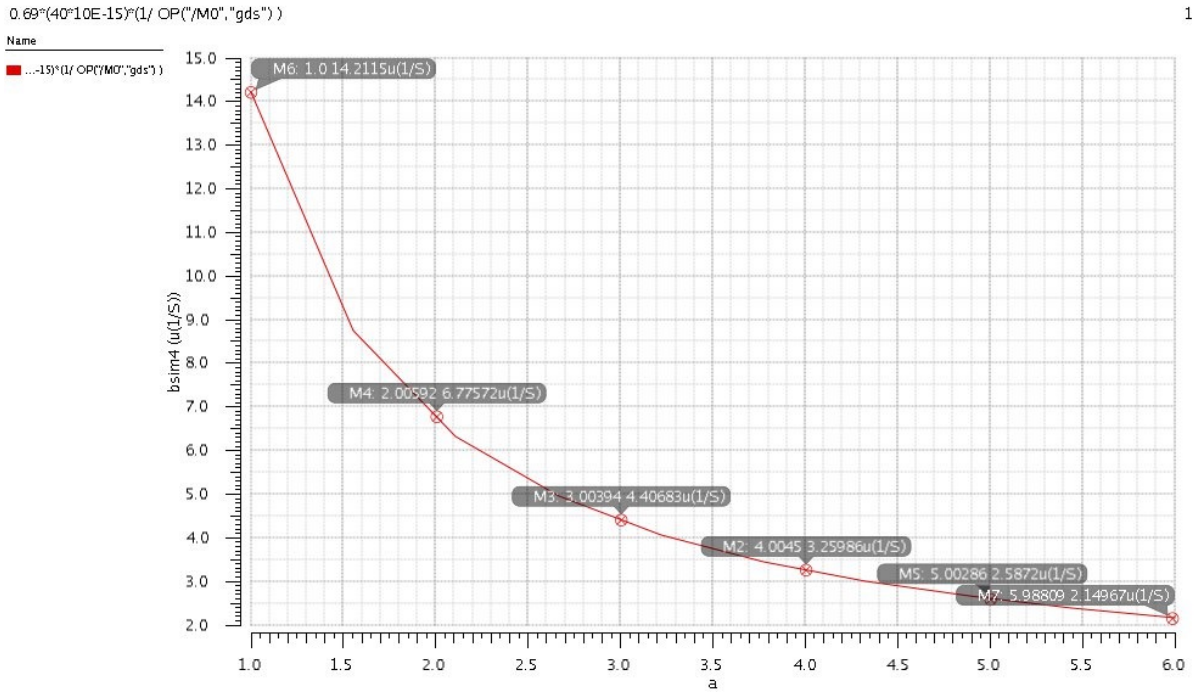


Analysis:
Sizing the width of PMOS = 1.592 * width of NMOS;
At this ratio, the switching threshold voltage will equals to 0.5Vdd, which will help having better use of limited driving voltage.



Analysis:
Low to high delay = 51.6149ps, high to low delay = 53.798ps, which is very close to each other and could be considered as similar as it is 0.4% of half wave length will be used in testing.

1.3.2 Best sizing for TG



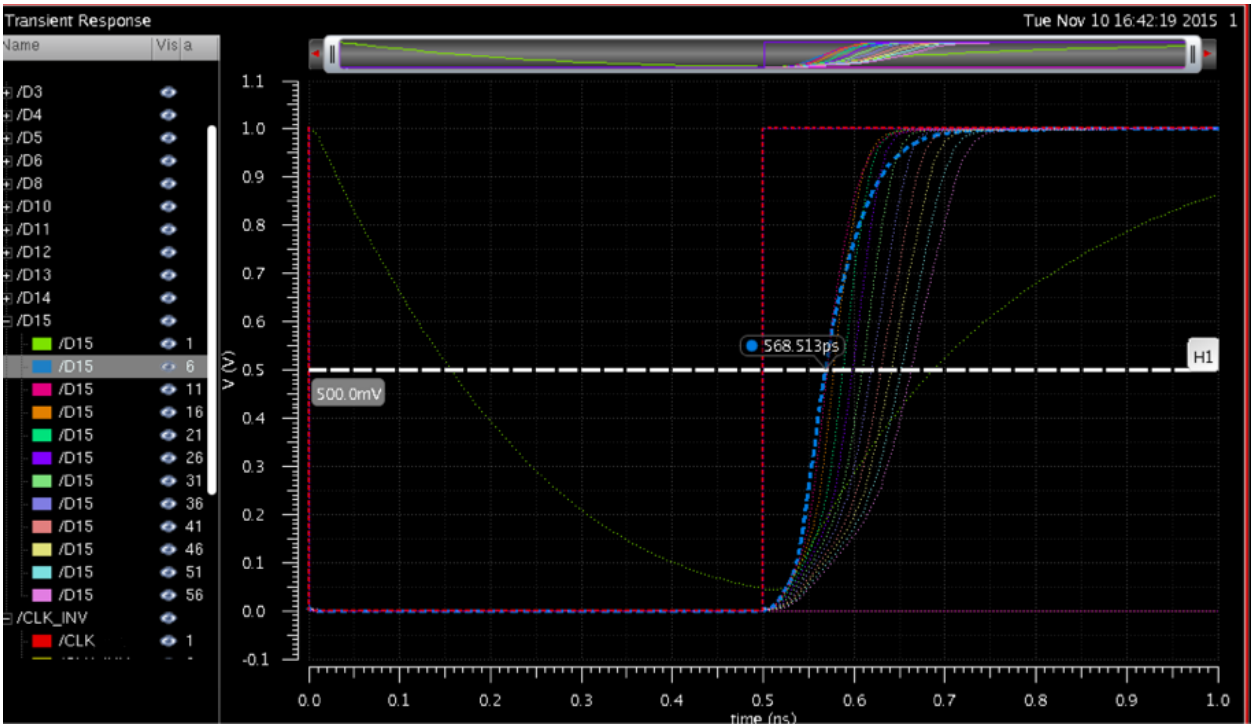
Based on above mentioned analysis, using transmission gate based devices will help improve performance with concern of time delay. Thus as transmission gates are used for implementing most of devices used in this part of the project, sizing of transmission gate is of vital importance. With calculation, the following plot in Figure was generated. As shown in the plot, using a = 6 as ration toward minimum size will ensure best performance. Some adjustment was made in design to cope with design complexity.

1.3.3. The test of u (ratio to reference) of last stage

As we can see from the effort calculation table, the value of capacitance of last stage is obviously largest. So, we need size the last one more exactly. So, we test the total delay varying with the last stage capacitance value. We set the capacitance to a variable a and using the parameter analysis tool to get the best value of a, which produces the minimal value of total delay.

1.3.3.1 The testing of rough range of best value a (width ratio to Cref)

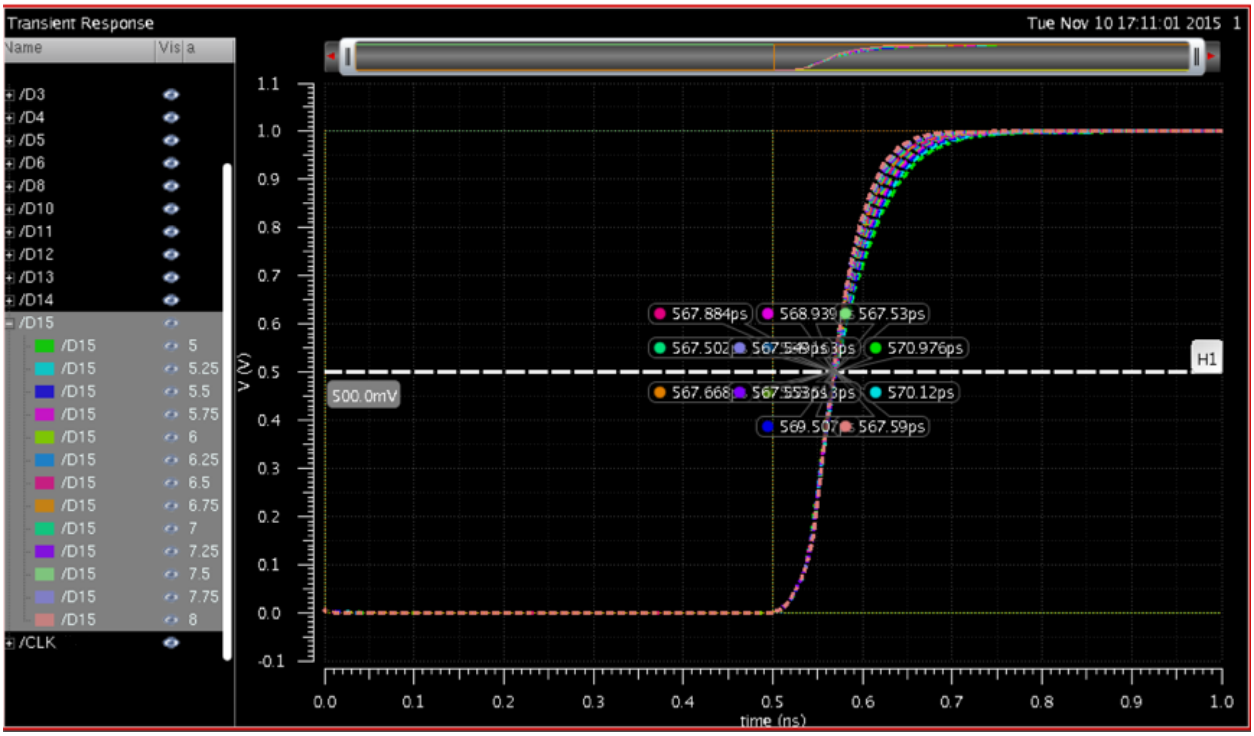
We set a from 1 to 60 based on the theoretical calculation.



Analysis:
As we can see from picture, the minimal value of delay we get is when a is near 6. But this is a rough range, so we set the range from 5 to 8 to get optimal value of a (width ratio to Cref).

1.3.3.2 The testing of exact value of optimal a (width ratio to Cref)

We set a from 5 to 8. Step is 0.25.

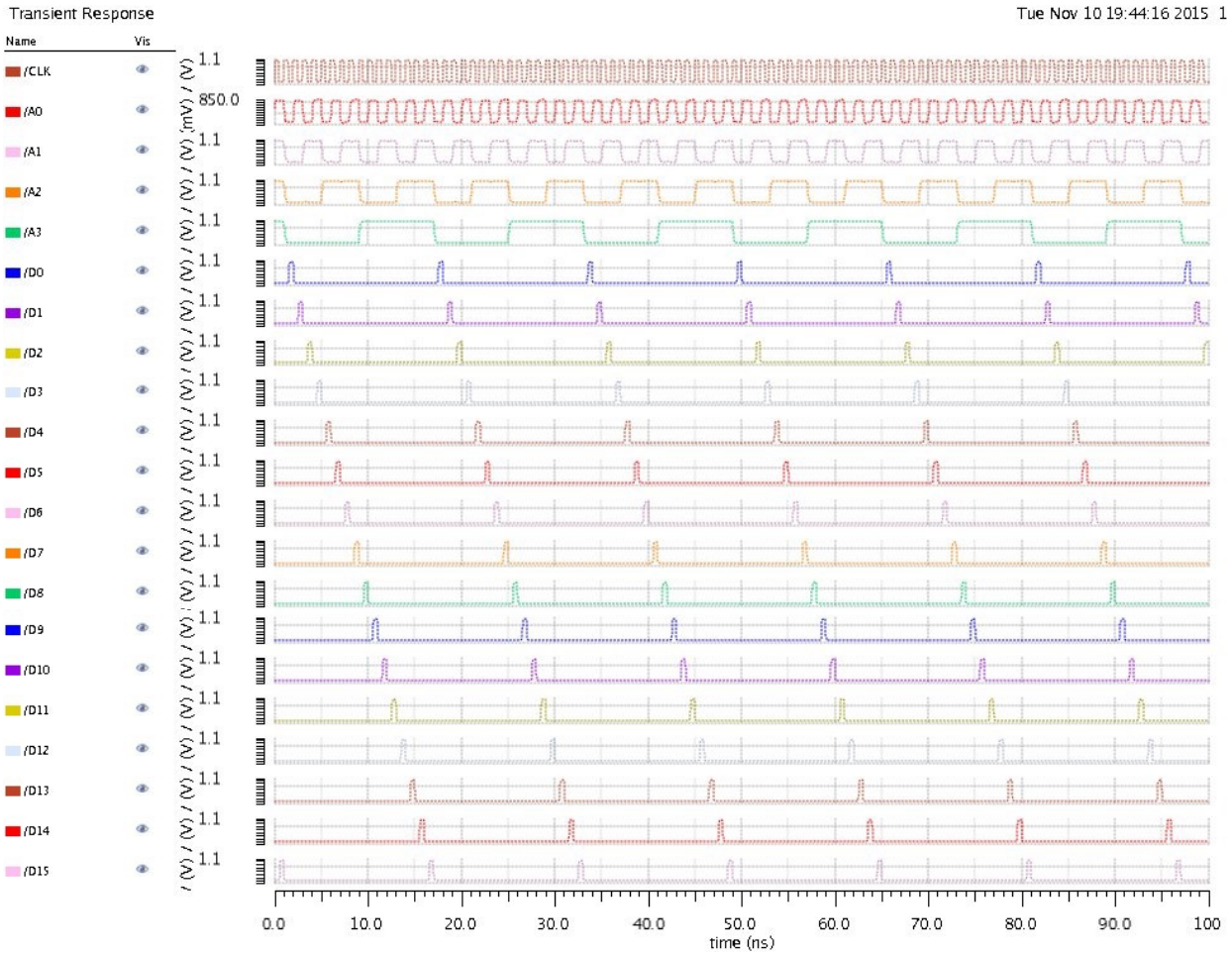


Analysis:
As we can see from picture, the minimal value of delay we get is when a is near 7.25. When a = 7.25. The minimal total delay is 67.549ps.

4. Simulation and Analysis:

4.1 Simulation of decoder

First, a functionality test was performed to ensure, again, that logic device logic is correct.
The address is represented by a3 a2 a1 a0.



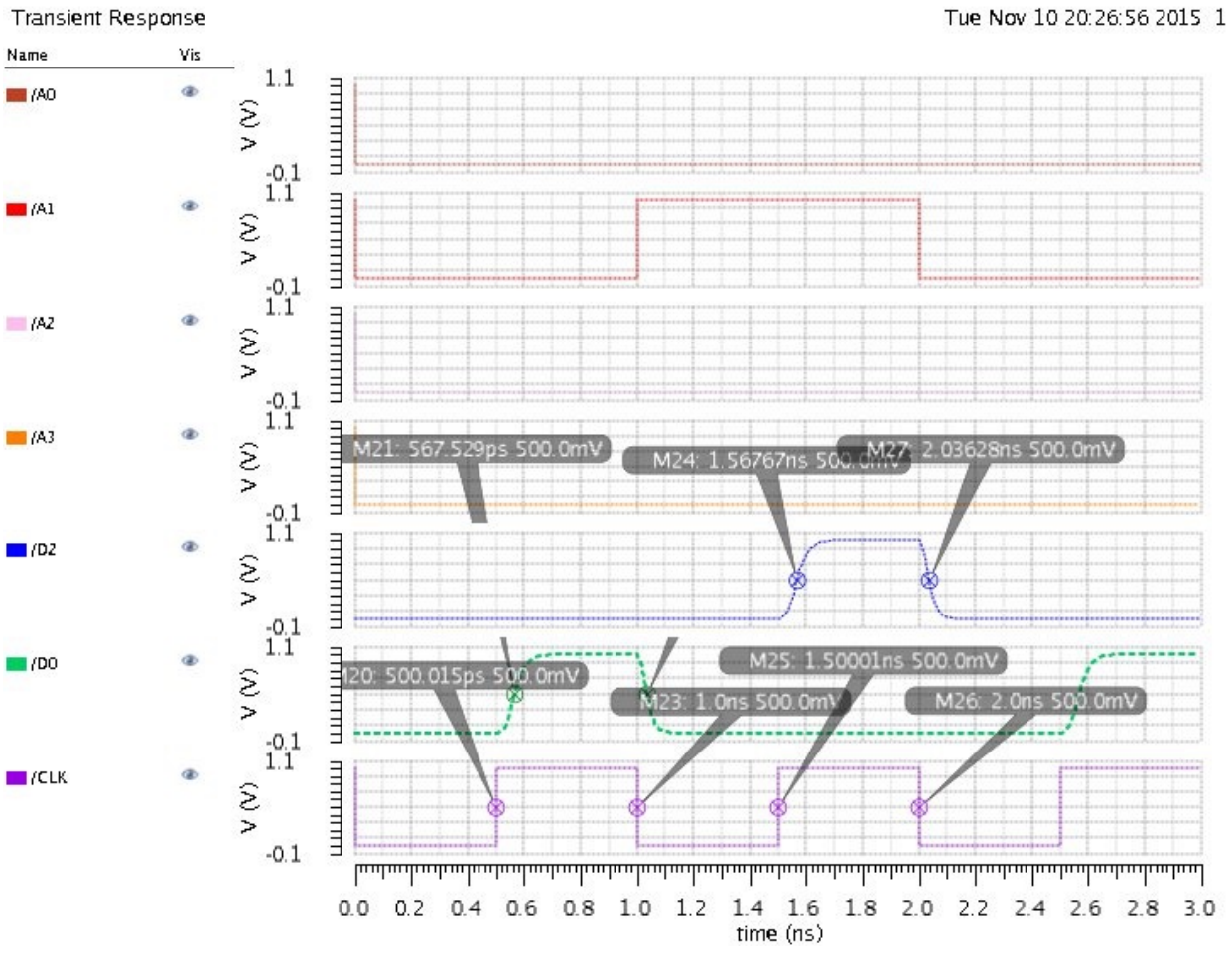
Output	Expression	Output	Expression	Output	Expression	Output	Expression
D0	0000	D4	0100	D8	1000	D12	1100
D1	0001	D5	0101	D9	1001	D13	1101
D2	0010	D6	0110	D10	1010	D14	1110
D3	0011	D7	0111	D11	1011	D15	1111

As we can see from picture, the output is correct of D0 to D15. So the logic is right.

4.2 Waveform of operation

4.2.1 Test case 1

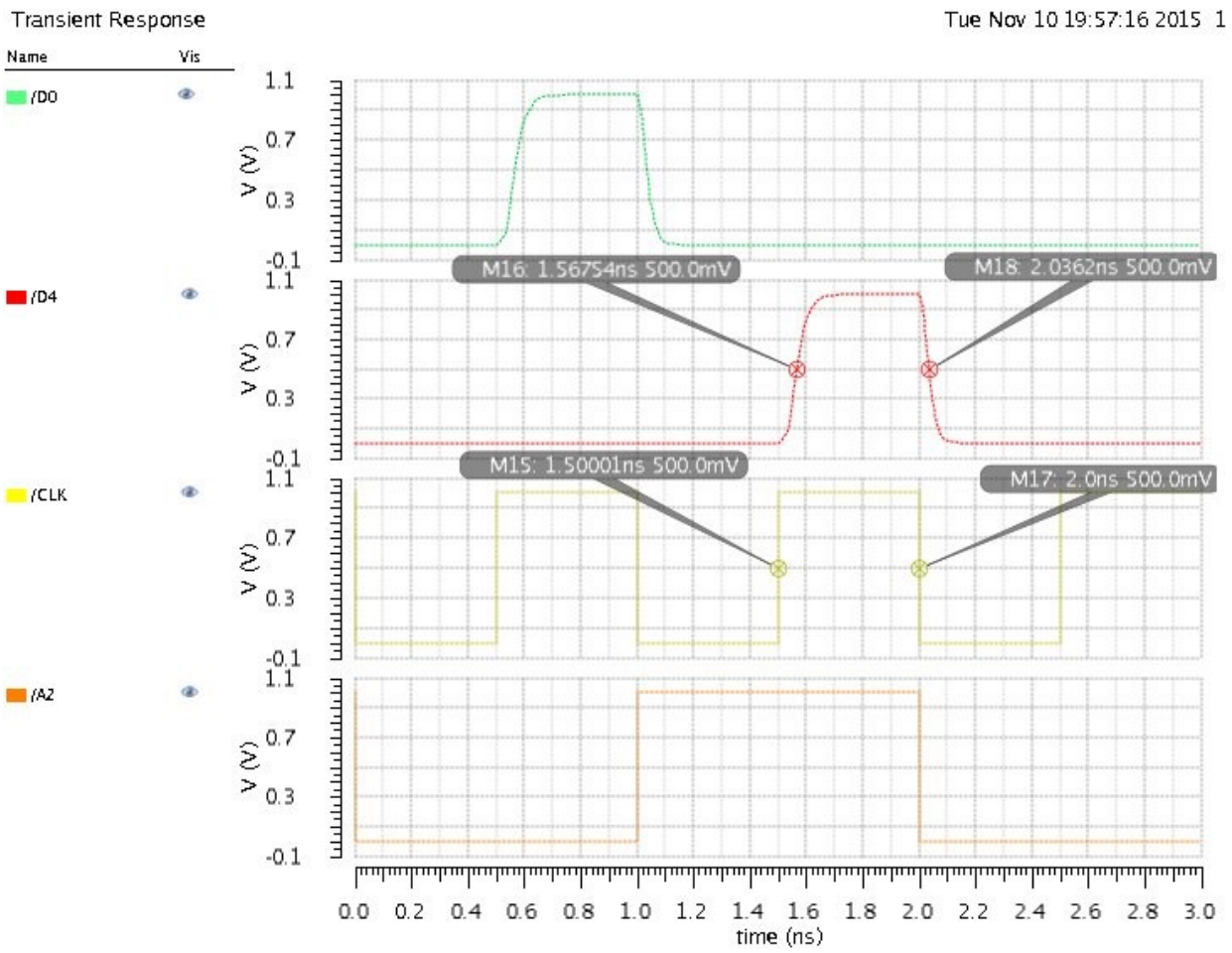
We set address from A0, A1, A2, A3 = 0 for 0 – 1ns and make A2 = 1 at 1ns and turn it back to 0 at 1.9ns



As we can see from picture:
The **delay of at rising edge** is 1.5675 - 1.5 = 67.5ps
The **delay of at falling edge** is 2.03628 - 2 = 36.28ps

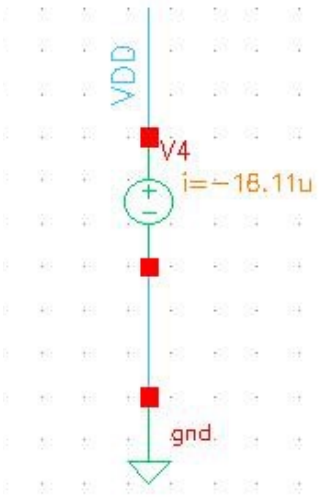
4.2.2 Test case 2

Then, We test the output from the address = A0 A1 A2 A3 = [0 0 0 0] to address = A0 A1 A2 A3 = [0 1 0 0]



As we can see from picture:
The **delay of at rising edge** is 1.5675 - 1.5 = 67.5ps
The **delay of at falling edge** is 2.0362 - 2 = 36.2ps

4.2 Average Power Consumption

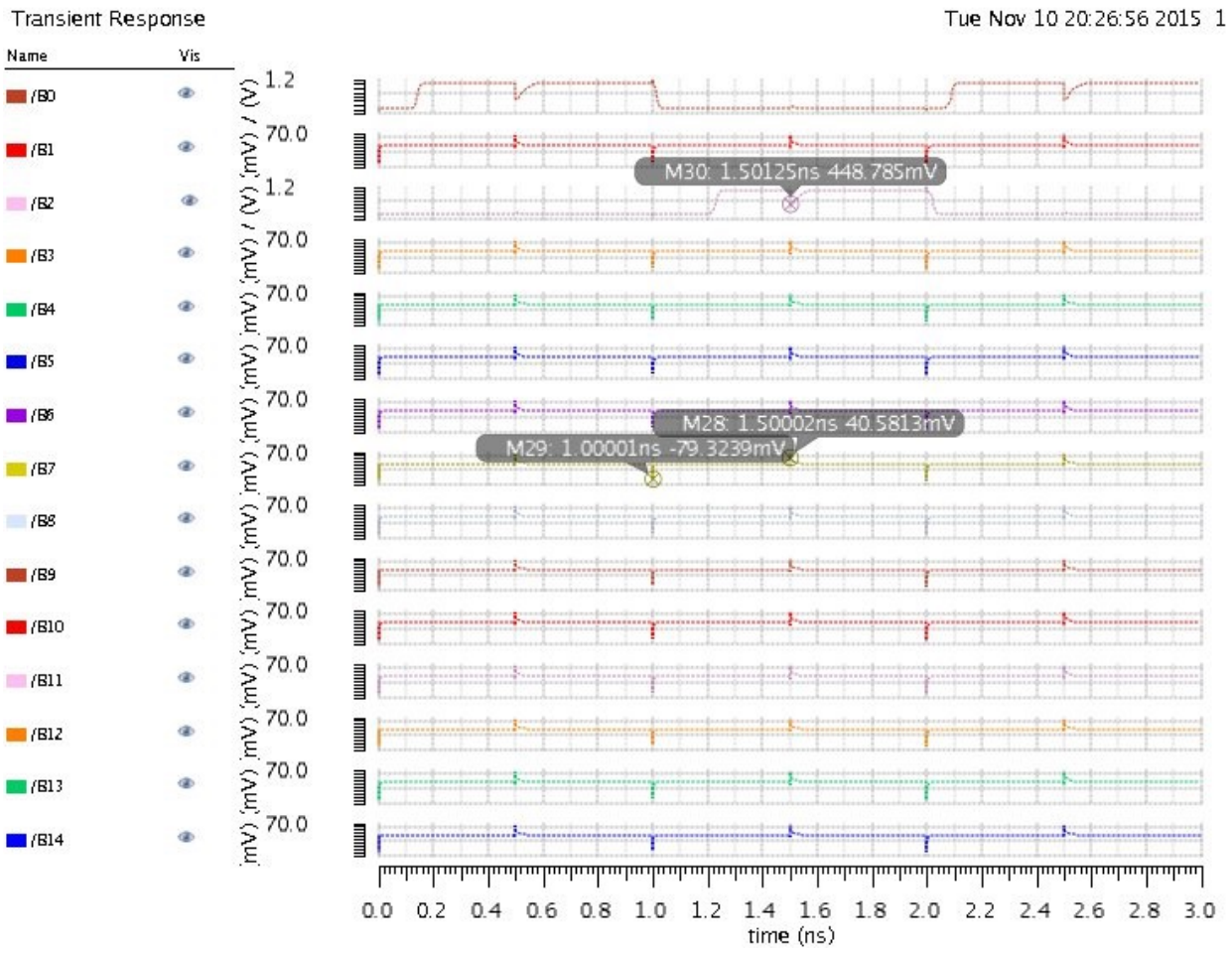


We use the calculator tool in cadence and get the average value of current. And because the current is already the average value, the power can be calculated through the formula.

$$Power = Vdd \cdot I_{average} = 1 \cdot 18.11 \cdot 10^{-6} = 1.811 \cdot 10^{-5}\ Watt$$

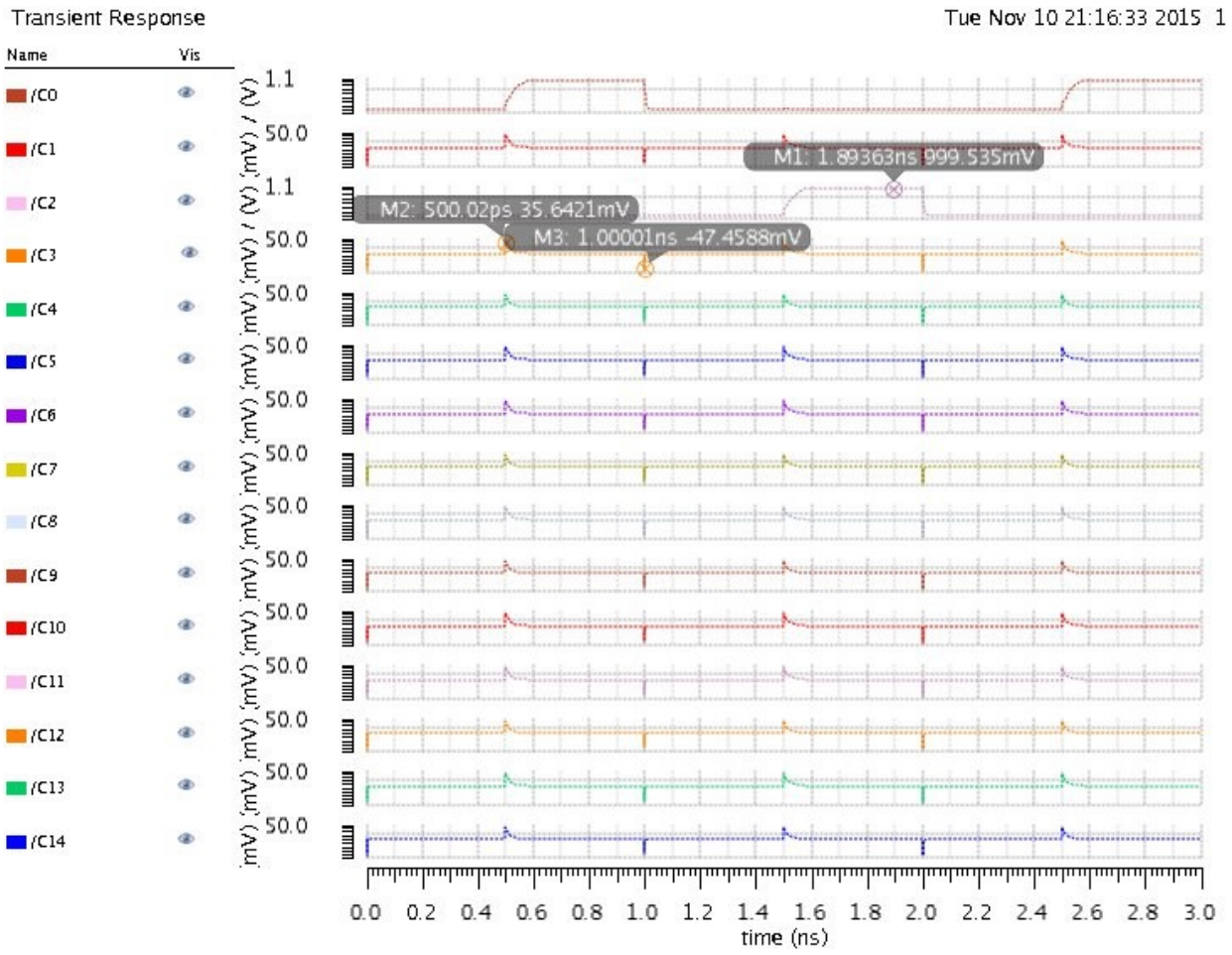
4.3 Testing glitch at every level

4.3.1 Testing glitch of first level — 4-16 decoder



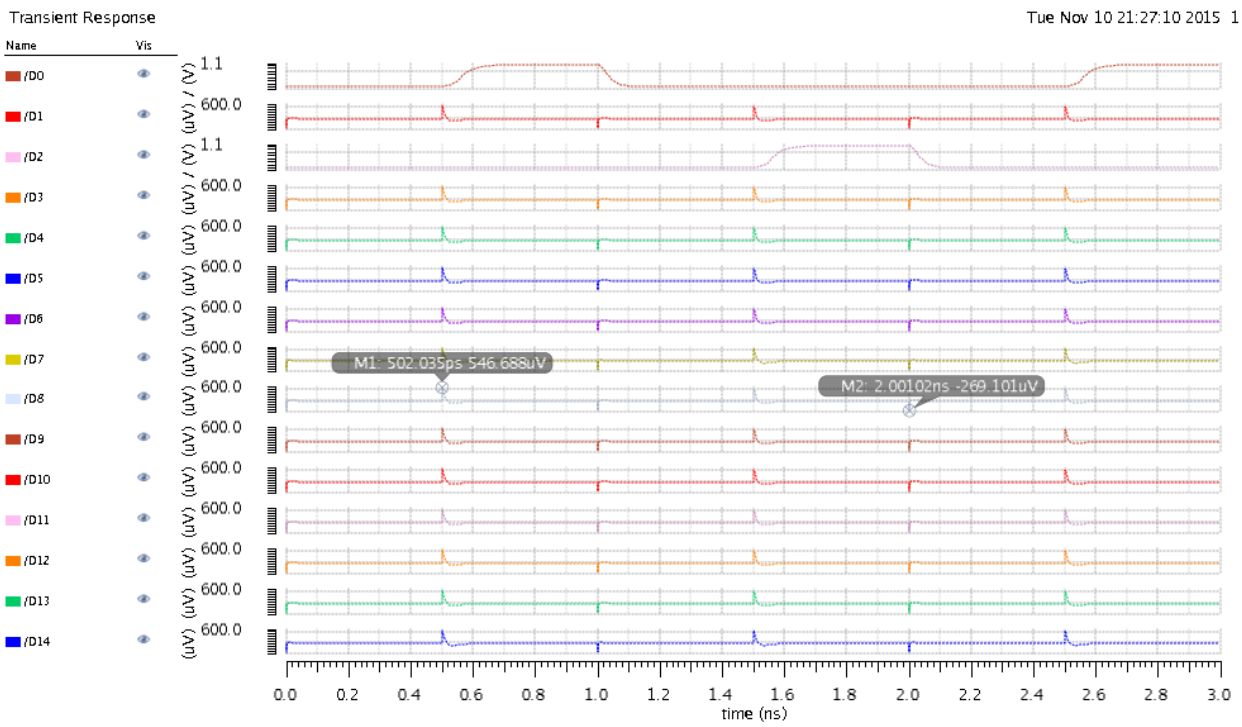
As we can see from picture, the value of positive glitch is 40.5813uV. The value of negative glitch is -79.3239uV.

4.3.2 Testing glitch of second level — Word Line Generation



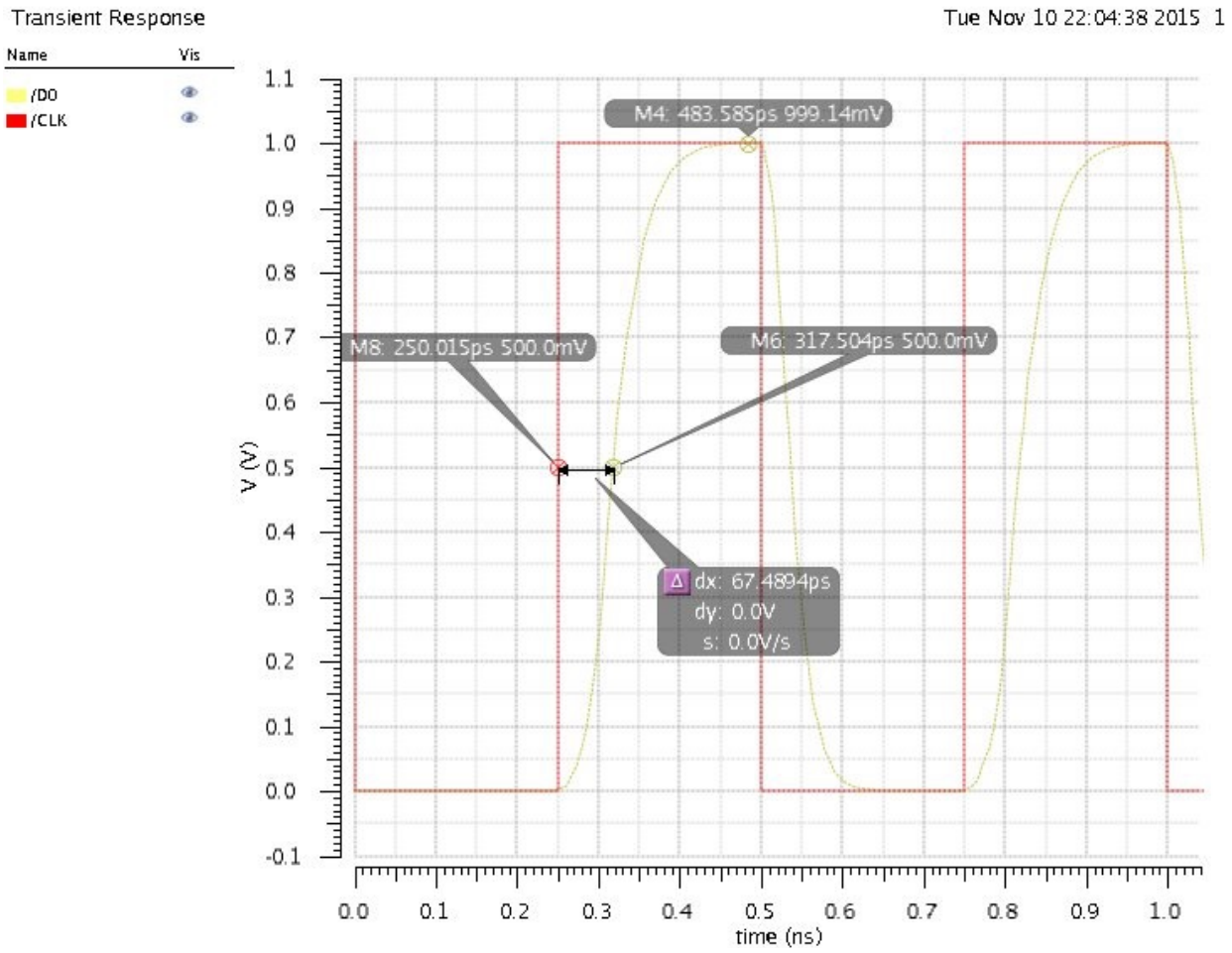
As we can see from picture, the value of positive glitch is 35.6421mV. The value of negative glitch is -47.4588mV.

4.3.4 Testing glitch of last level — Drive



As we can see from picture, the value of positive glitch is 546.688uV. The value of negative glitch is -269.101uV.

4.4 Testing highest frequency



The highest frequency is when Tclk=500ns. So the highest frequency is Freq = 1/Tclk= 2G Hz. And when we increase the frequency for further step, the value of output can not achieve Vdd (1V). So our highest frequency is 2G Hz. And the corresponding delay is 67.4894ps.