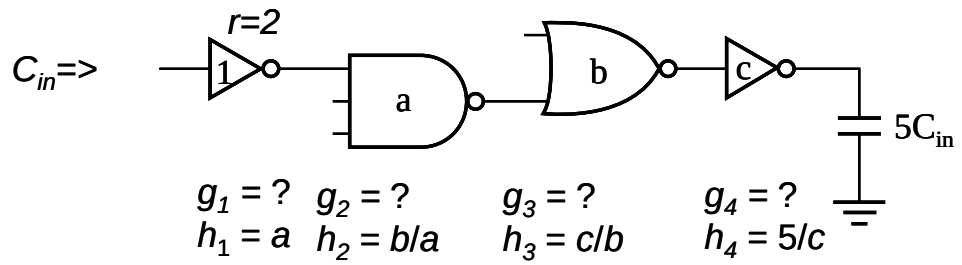
Logical Effort Calculations: Clarifications



In the above problem the factor 'a' (and similarly b, and c) refers to:

$$a = \frac{C_{input\_NAND3}}{C_{input\_1st\_stage}} = \frac{C_{input\_NAND3}}{C_{in}}$$

$$b = \frac{C_{input\_NOR2}}{C_{input\_1st\_stage}} = \frac{C_{input\_NOR2}}{C_{in}}$$

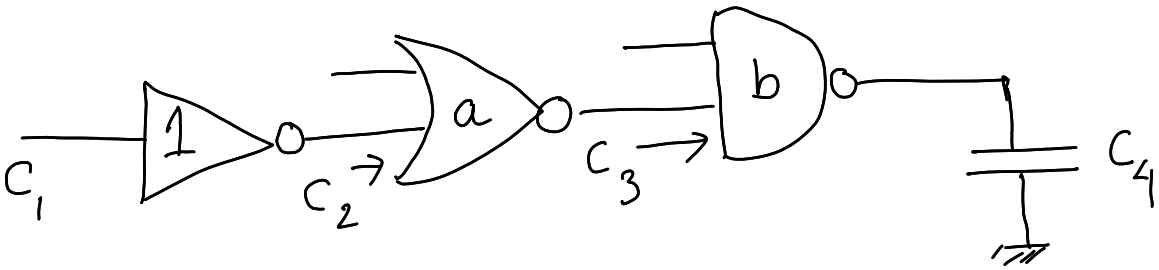
$$c = \frac{C_{input\_NOT}}{C_{input\_1st\_stage}} = \frac{C_{input\_NOT}}{C_{in}}$$

Therefore, by definition the same factor for the 1st stage is:

$$\frac{C_{input\_1st\_stage}}{C_{input\_1st\_stage}} = 1$$

Therefore, the factors 'a', 'b', and 'c' are scaling factors for the input capacitances of the different stages with respect to the input capacitance of the 1st stage.

In relation to the example 8.4 in the Uyemura's book, this refers to:



$$a = \frac{C_{input\_NOR2}}{C_{input\_1st\_stage}} = \frac{C_2}{C_1} \text{ and } b = \frac{C_{input\_NAND2}}{C_{input\_1st\_stage}} = \frac{C_3}{C_1}$$

THESE FACTORS DO NOT REFER TO THE SIZE OF THE DEVICES IN THESE GATES.

Let us revisit the Example 8.4 in the book.

The book first computes the 'raw' input capacitance values for the input capacitance of the each stage (i.e. C_1, C_2, and C_3).

The next step book performs is the computation of the sizes of the different devices of these three gates.

The way I look at this problem is as follows:

At first stage we have an inverter. As soon as C_1 (and 'r') is given the sizes of the NMOS and PMOS for that inverter is determined.

$C_1 = (1 + r)\, Cn$, where. Cn is the capacitance of the NMOS device of the inverter.

$\Rightarrow Cn = C1/(1+r)$
$\Rightarrow Wn = (1/C_{ox}L)Cn$

- ⇨ This determines the NMOS and hence PMOS size of the inverter. You can determine this also as the scaling factor with reference to the minimum size NMOS device. $S_1 = Wn/W_{min}$

Next, we want to determine the sizes of the NMOS and PMOS devices of 2nd stage. First, let us determine the absolute sizes.

$C_2 = (1 + 2r)\, C_{n\_NOR}$, where, C_{n_NOR} is the input cap. of the NMOS device of the NOR2,

The factor '2r' determines for a NOR2 gate the width of the PMOS has to be 2r times larger than the width of the NMOS device.

$C_{n\_NOR} = C_2 / (1+2r)$
$\Rightarrow W_{n\_NOR} = (1/C_{ox}L)C_{n\_NOR}$

This determines the NMOS and PMOS sizes of the NOR-2 gates. You can of-course determine the width as a scaling factor of the minimum size NMOS, or NMOS for the inverter etc.

Let us now understand how book approached the problem:

Let us consider the equation (8.157)

Eq. 8.157 expresses the capacitance C_2 as a scaling factor S_2 with respect to the NMOS capacitance of the inverter at the first stage (C_{Gn})

If we assume the size of the NMOS in the NOR gate is S_2 times the size of the NMOS device of the inverter, then the input capacitance of the NOR-2 gate becomes:

$C_2 = C_{n\_NOR} + C_{p\_NOR} = C_{n\_NOR} + 2r(C_{n\_NOR}) = C_{n\_NOR}(1+2r) = S_2C_{Gn}(1+2r)$

$S_2 = C2/[(1+2r)C_{Gn}]$ => eq. 8.157

You can use this equation, compute C_{Gn} from 8.160, and use it to find out S_2.

This will give the scaling factor for the NMOS capacitance of the NOR-2 gate with reference to the NMOS capacitance of the inverter. This ratio will be same as the width scaling factor of the NMOS for NOR-2 gate with respect to the NMOS width of the first stage.

Next, book refers that (after eq. 8.158) that it wants to compute the scaling factor with reference to the input capacitance of the NOT gate $C_1 = (1 + r) C_{Gn}$

Lets assume that the input capacitance of the NMOS of the NOR-2 gates is $C_{n\_NOR} = S_2C_1$. This leads to eq. 8.159.

$C_2 = C_{n\_NOR}(1+2r) = S_2C_1(1+2r) = S_2C_1(1+2r) = S_2\ (1+2r)\ (1 + r)\ C_{Gn}$

$\Rightarrow S_2 = \dfrac{C_2}{(1+2r)(1\ +\ r)C_{Gn}}$, where C_{Gn} can be computed from 8.160

Note, this S_2 (i.e. S_2 in eq. 8.159, lets call it $S_2^{(1)}$) is different from the S_2 in eq. 8.157.

So, let us now summarize the different scaling factors we have seen (in context of the Example 8.4 in the book):

(1) 'a' => capacitance scaling factor of NOR-2 gate with reference to the input capacitance of the 1st stage
$a = C_2/C_1$

(2) S_2 (eq. 8.157) => capacitance (and width) scaling factor for the NMOS of NOR-2 gate with reference to the NMOS of the first stage inverter.

(3) $S_2^{(1)}$ (eq. 8.159) => capacitance scaling factor for the NMOS of NOR-2 gate with reference to the input capacitance of the first stage inverter.

The Key:

For ‘logical effort’ based design problems the two scaling factors are important:

(a) The input capacitance scaling factor => This is normally with reference to the input capacitance of the 1st stage i.e. input capacitance of the path.

(b) The device size scaling factor => This is normally with respect to the width of the NMOS’s in the first stage or a minimum size NMOS devices.

We can also have a third one which gives the device capacitance as a scaling factor of the input capacitance of the first stage. However, (a) and (b) are sufficient to design the logic path.

A Final Comment:

The factors h1, h2, h3 in the homework-2 solution refers to the capacitance scaling factor.