ECE 6473
Lecture 2
Date: 09/21/2015

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Reading

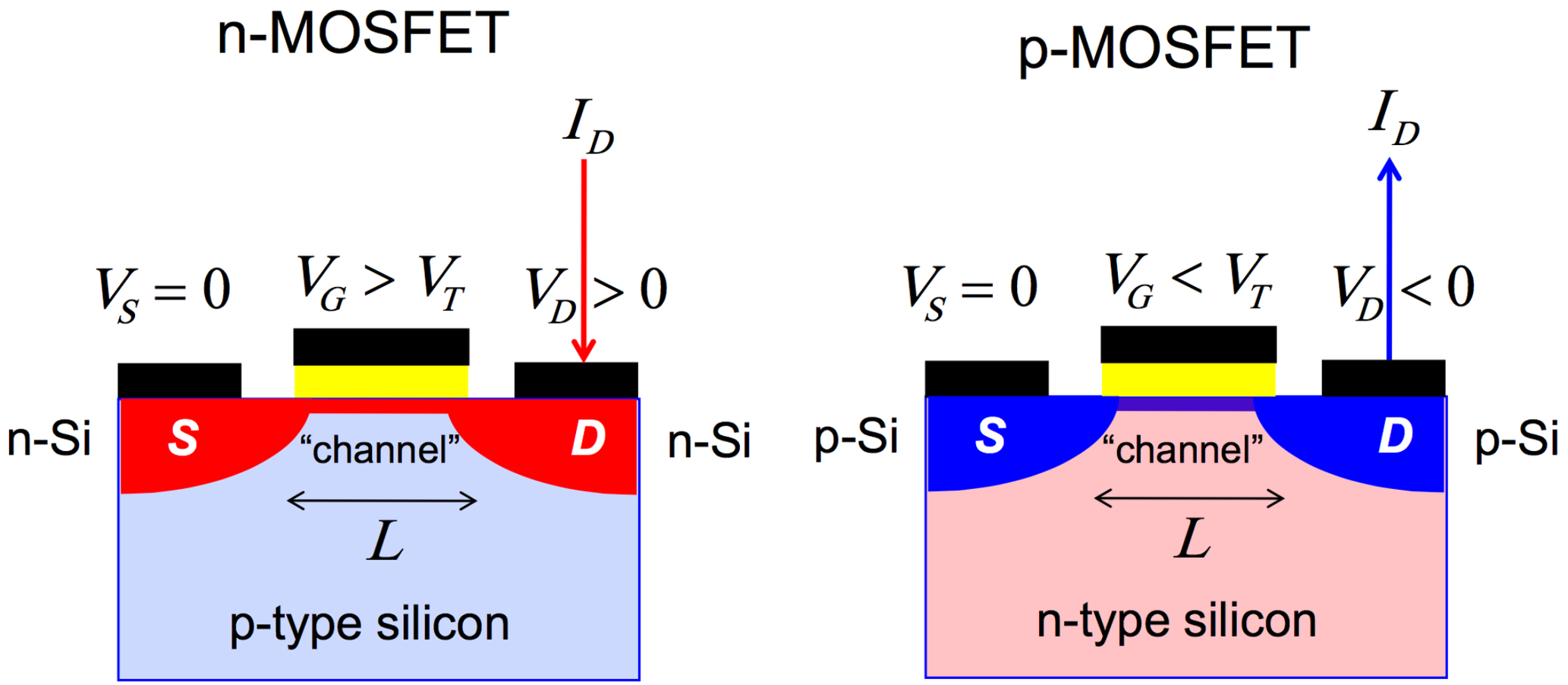
- Power point and hand-written lecture notes posted on newclasses.nyu.edu

- Sections 3.3.1–3.3.2, 5.1—5.4 from Digital Integrated Circuits by Jan M. Rabaey et al.

MOSFET analysis

- Recap from 09/14/2015
    - MOSFET I-V characteristics
    - Transistor Resistance
    - *Sub-threshold Conduction (read from posted lecture notes and discuss in office hours)*
- MOSFET capacitance
- Introduction to Inverter functionality

MOSFET



CMOS process has two types of transistors: NFET and PFET

MOSFET

	NFET	PFET
Body or substrate	p-doped	n-doped
Source/Drain contacts	n+ doped	p+ doped
Current	Flows from drain to source (I_{DS})	Flows from source to drain (I_{SD})
Current carriers	Electrons	Holes
Threshold voltage	Positive	Negative
Relevant terminal voltages	V_{gs}, V_{ds}, V_{bs}	V_{sg}, V_{sd}, V_{sb}

- In MOSFETs, threshold voltage is the control voltage. It tells whether or not the transistor is conducting.

- Threshold voltage is fixed by the fabrication process.

NFET I-V characteristics

Modes of operation

$V_{gs} < V_{Tn}$

Cut-off or "OFF"

Ideally in cut-off, the transistor must not conduct any current.

$V_{gs} \geq V_{Tn}$

Active or "ON"

Linear

$V_{ds} < V_{gs} - V_{Tn}$

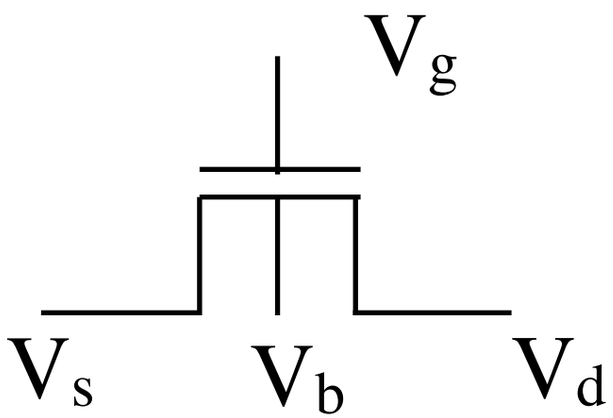
Saturation

$V_{ds} \geq V_{gs} - V_{Tn}$

(V_{gs}-V_{Tn}) is the SATURATION voltage

NFET I-V model for hand calculation

Active region: $V_{gs} \geq V_{Tn}$



Linear ($V_{ds} < V_{gs}-V_{Tn}$): $$I_{DS} = (\mu_n C_{ox})\left(\frac{W}{L}\right)\left[(V_{gs} - V_{Tn})V_{ds} - \frac{V_{ds}^2}{2}\right]$$

Saturation ($V_{ds} \geq V_{gs}-V_{Tn}$): $$I_{DS} = \frac{1}{2}(\mu_n C_{ox})\left(\frac{W}{L}\right)(V_{gs} - V_{Tn})^2(1+\lambda V_{ds})$$

$\kappa_n = (\mu_n C_{ox})$: Process parameter —> decided by the foundry. Designers CANNOT tweak it.

$\beta_n = \kappa_n \times (W/L)$ —> Designers can tweak W/L ratio. Hence, β_n is a design parameter.

λ: Channel-length modulation. Also considered fixed by foundry.

Threshold voltage, V_{Tn}

$$V_{Tn} = V_{T0} + \gamma\left(\sqrt{\left(2\left|\phi_f\right| - V_{bs}\right)} - \sqrt{2\left|\phi_f\right|}\right)$$

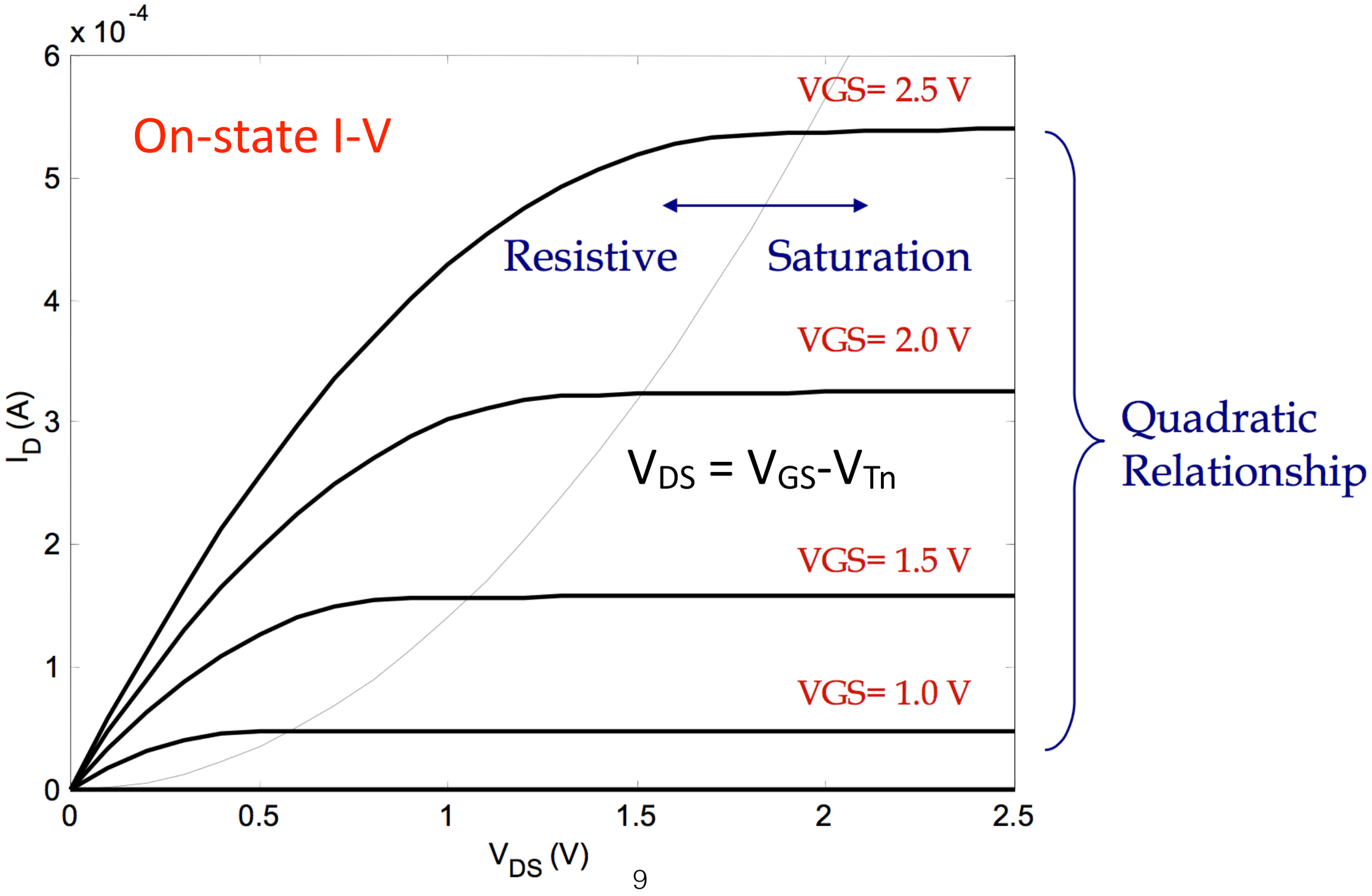
V_{T0}: Process parameter. Fixed by the foundry.

γ: Body-effect coefficient. Fixed by the foundry.

ϕ_f: Bulk Fermi potential. Fixed by the foundry

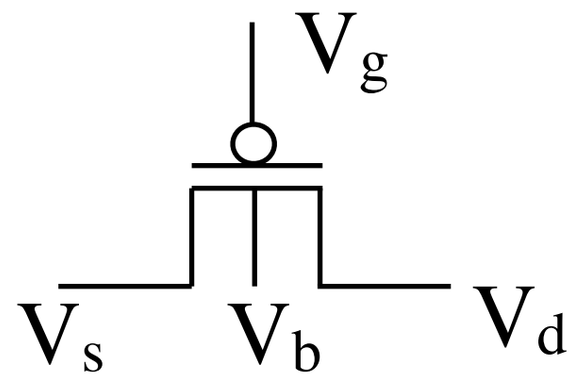
- **V_{Tn} is fixed by the foundry.**
- **Designers can control V_{bs} voltage through circuit design.**
- **When V_{bs} = 0V, V_{Tn} cannot be tweaked.**

NFET I-V characteristics



PFET I-V model for hand calculation

Active region: $V_{sg} \geq \left| V_{Tp} \right|$



Linear ($V_{sd} < V_{sg}+V_{Tp}$): $$I_{SD} = \left(\mu_h C_{ox}\right)\left(\frac{W}{L}\right)\left[\left(V_{sg} + V_{TP}\right)V_{sd} - \frac{V_{sd}^2}{2}\right]$$

Saturation ($V_{sd} \geq V_{sg} + V_{Tp}$): $$I_{SD} = \frac{1}{2}\left(\mu_h C_{ox}\right)\left(\frac{W}{L}\right)\left(V_{sg} + V_{TP}\right)^2\left(1 + \lambda V_{sd}\right)$$

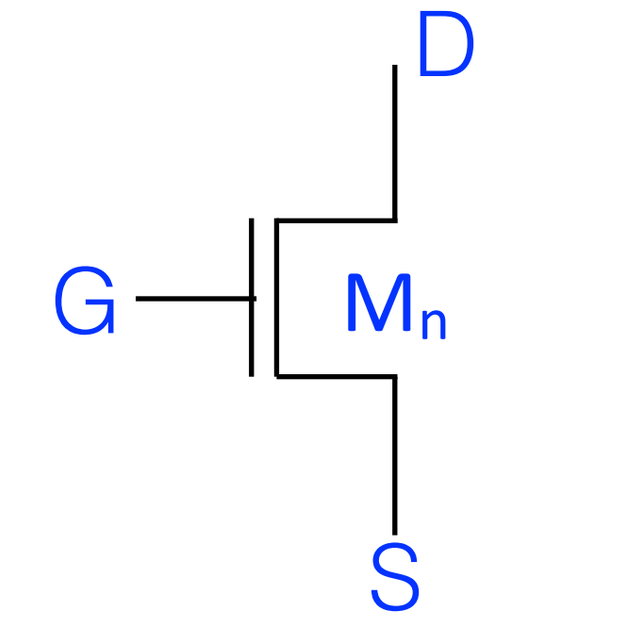
$\kappa_p = (\mu_h C_{ox})$: Process parameter —> decided by the foundry. Designers CANNOT tweak it.

$\beta_p = \kappa_p \times (W/L)$ —> Designers can tweak W/L ratio. Hence, β_p is a design parameter.

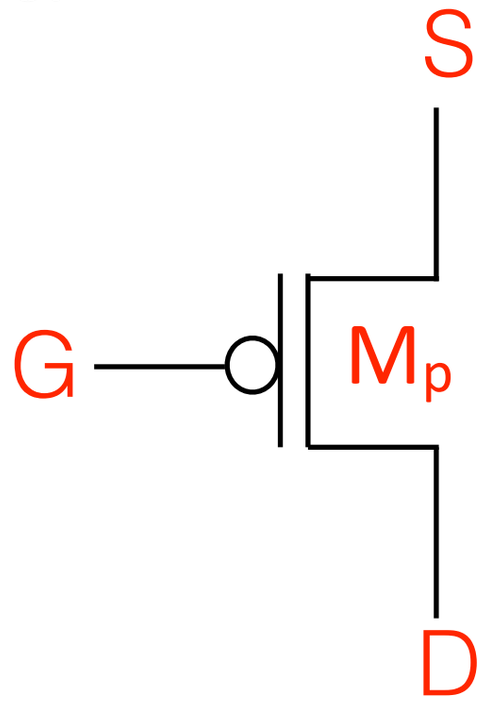
λ: Channel-length modulation. Also considered fixed by foundry.

NFET versus PFET

In CMOS digital design, we will use both NFETs and PFETs for complementary logic.



$\beta_n = \kappa_n \times (W/L)_n$



$\beta_p = \kappa_p \times (W/L)_p$

Very important point: For the same C_{ox}, $\kappa_n > \kappa_p$

Differential resistance of the transistor

Differential resistance of the transistor is a useful concept for analog design. It is also called small signal resistance.

$$r = \left(\frac{\partial I_{DS}}{\partial V_{ds}} \right)^{-1}$$

Linear region

$$r = \frac{1}{\mu_n C_{ox} \left(\frac{W}{L} \right) \left[\left(V_{gs} - V_{Tn} \right) - V_{ds} \right]}$$

Saturation region

$$r = \frac{2}{\mu_n C_{ox} \left(\frac{W}{L} \right) \left(V_{gs} - V_{Tn} \right)^2 \lambda}$$

If ƛ = 0, then r = ∞ (ideal current source).

Very useful for designing current mirror circuits in analog space.

Large signal resistance of the transistor

Large signal resistance of the transistor is a useful concept for digital design.

$$R = \left(\frac{\Delta I_{DS}}{\Delta V_{ds}} \right)^{-1}$$

Say $V_{gs} = V_{dd}$

V_{ds} changes from 0 to V_{dd}

What is R?

When V_{ds} = 0V, I_{DS} = 0.
When $V_{ds} = V_{dd}$, I_{DS} = Saturation current

Large signal resistance of the transistor

Large signal resistance of the transistor is a useful concept for digital design.

$$R = \left(\frac{\Delta I_{DS}}{\Delta V_{ds}} \right)^{-1}$$

Say $V_{gs} = V_{dd}$

V_{ds} changes from 0 to V_{dd}

What is R?

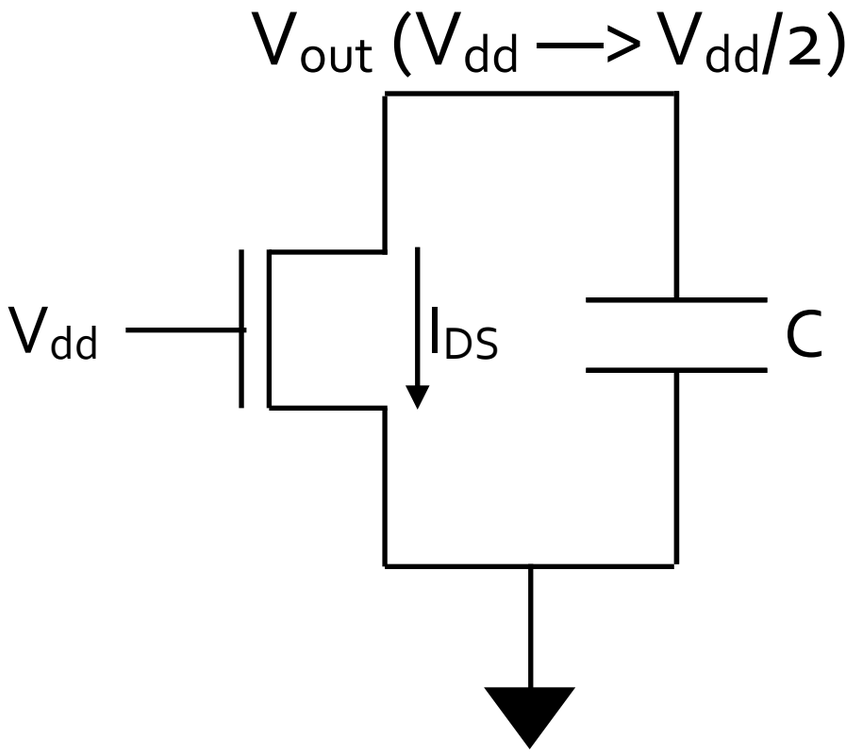
When V_{ds} = 0V, I_{DS} = 0.
When $V_{ds} = V_{dd}$, I_{DS} = Saturation current

$$R = \left(\frac{I_{DS,sat}}{V_{dd}} \right)^{-1}$$

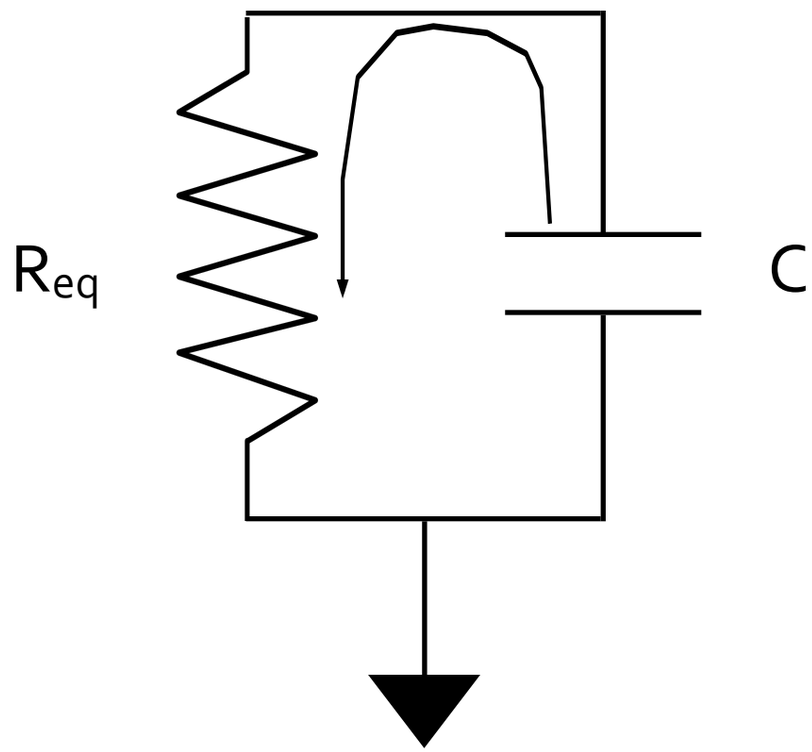
Substitute $I_{DS,sat}$ in this equation

$$\frac{2V_{dd}}{(\mu_n C_{ox})\left(\frac{W}{L}\right)(V_{dd} - V_{Tn})^2(1 + \lambda V_{dd})}$$

Problem:
Discharging time of a capacitor through a NFET



Question:
Obtain the time constant for discharging of the capacitor through the NFET.



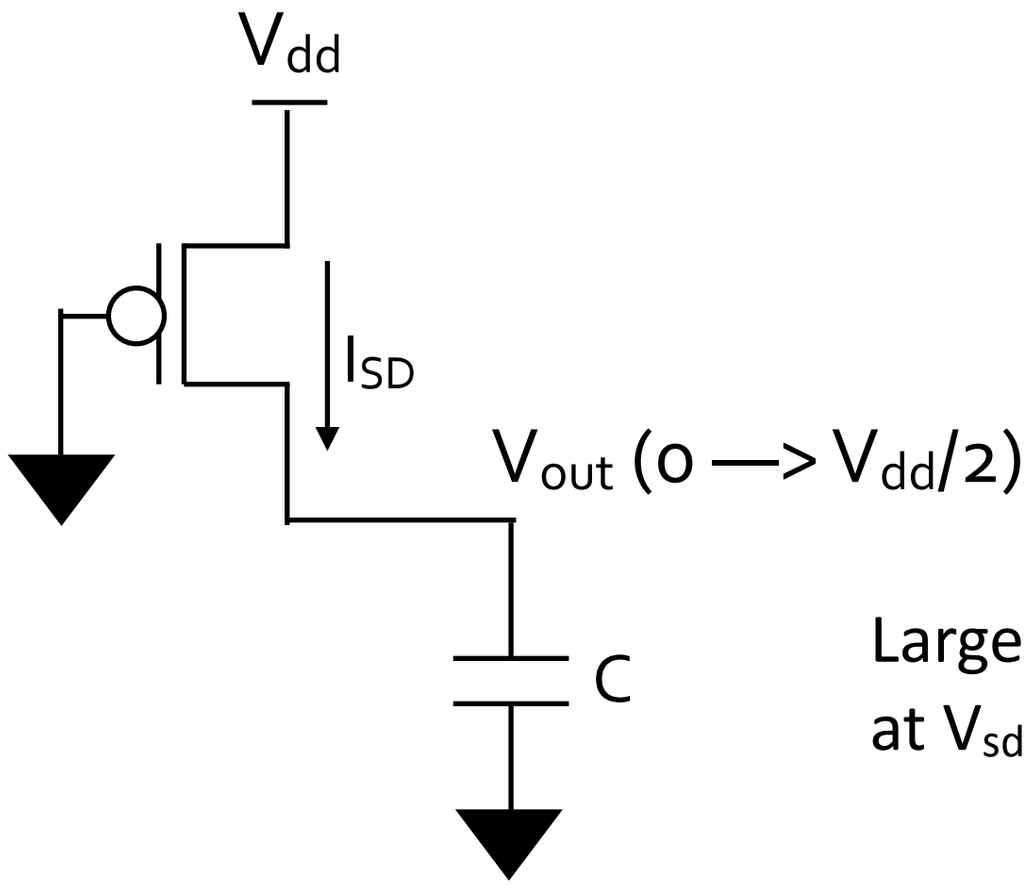
$$\tau = 0.69 R_{eq} C$$

$$R_{eq} = \frac{1}{2}\left(R_1 + R_2\right)$$

Large signal resistance at $V_{ds} = V_{dd}$

Large signal resistance at $V_{ds} = V_{dd}/2$

Problem:
Charging time of a capacitor through a PFET



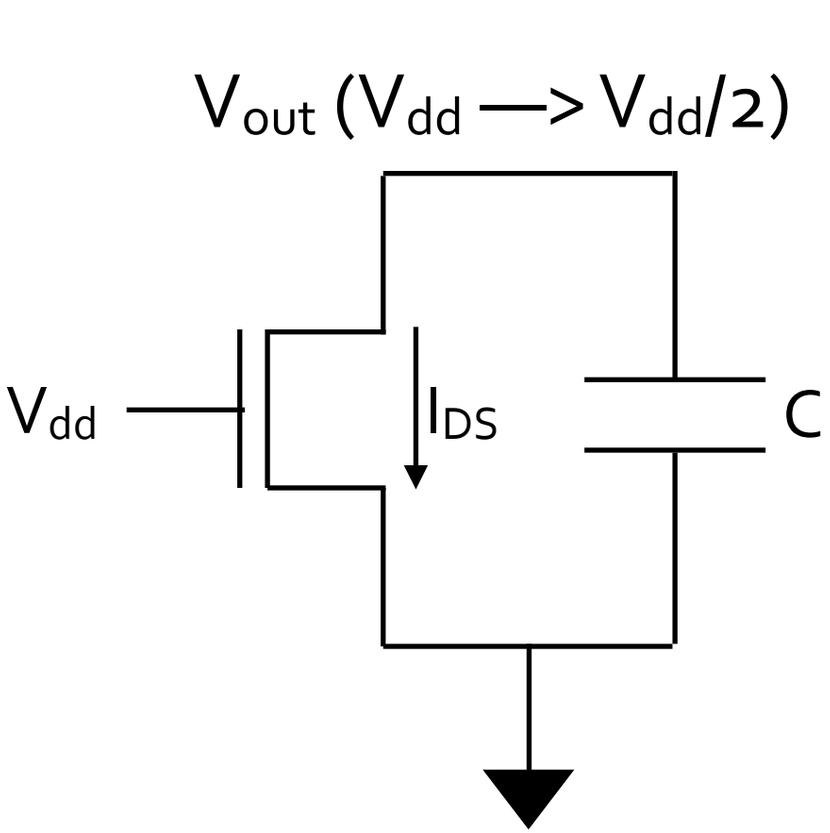
$$\tau = 0.69 R_{eq} C$$

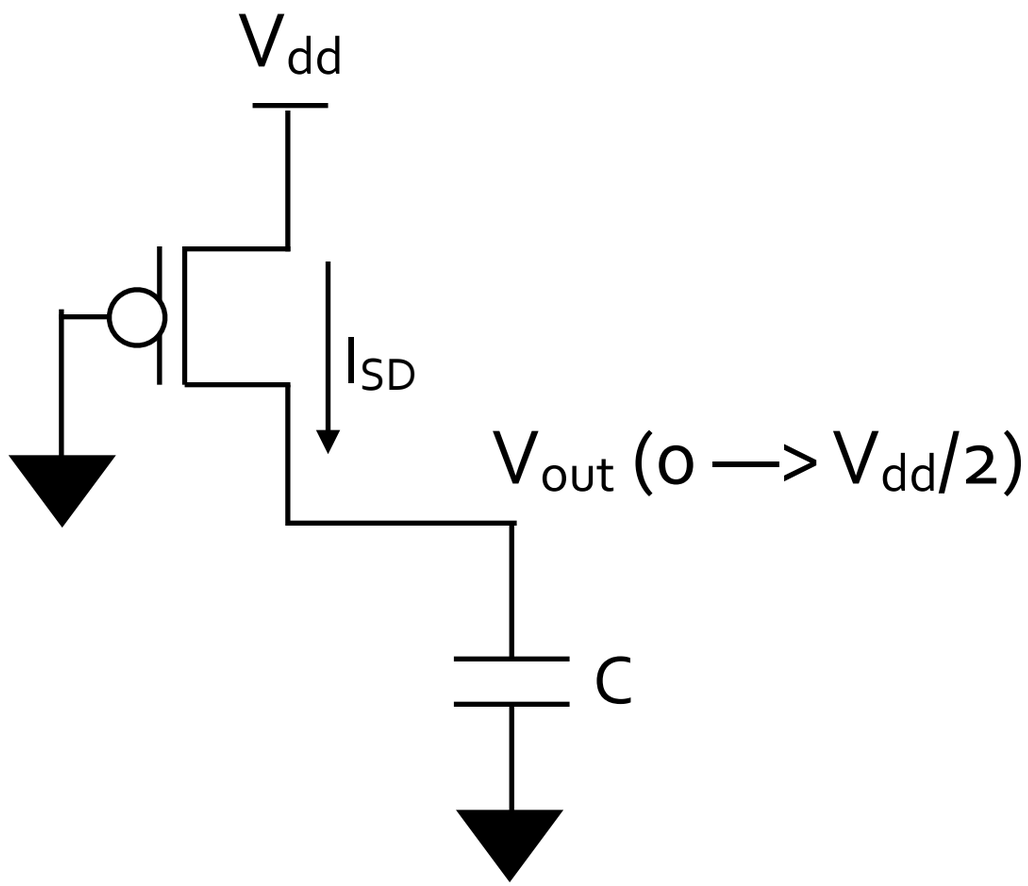
$$R_{eq} = \frac{1}{2}\left(R_1 + R_2\right)$$

Large signal resistance
at $V_{sd} = V_{dd}$

Large signal resistance
at $V_{sd} = V_{dd}/2$

Calculating equivalent resistance, R_{eq}





$$R_{eq} = \frac{3V_{dd}}{4I_{DSAT}}\left(1 - \frac{5}{6}\lambda V_{dd}\right)$$

$$I_{DSAT} = \frac{1}{2}(\mu C_{ox})\left(\frac{W}{L}\right)\left[(V_{dd} - V_T)^2\right]$$

Use the values of μ, C_{ox}, V_T, (W/L) corresponding to either NFET or PFET depending on analysis.

Equivalent resistance

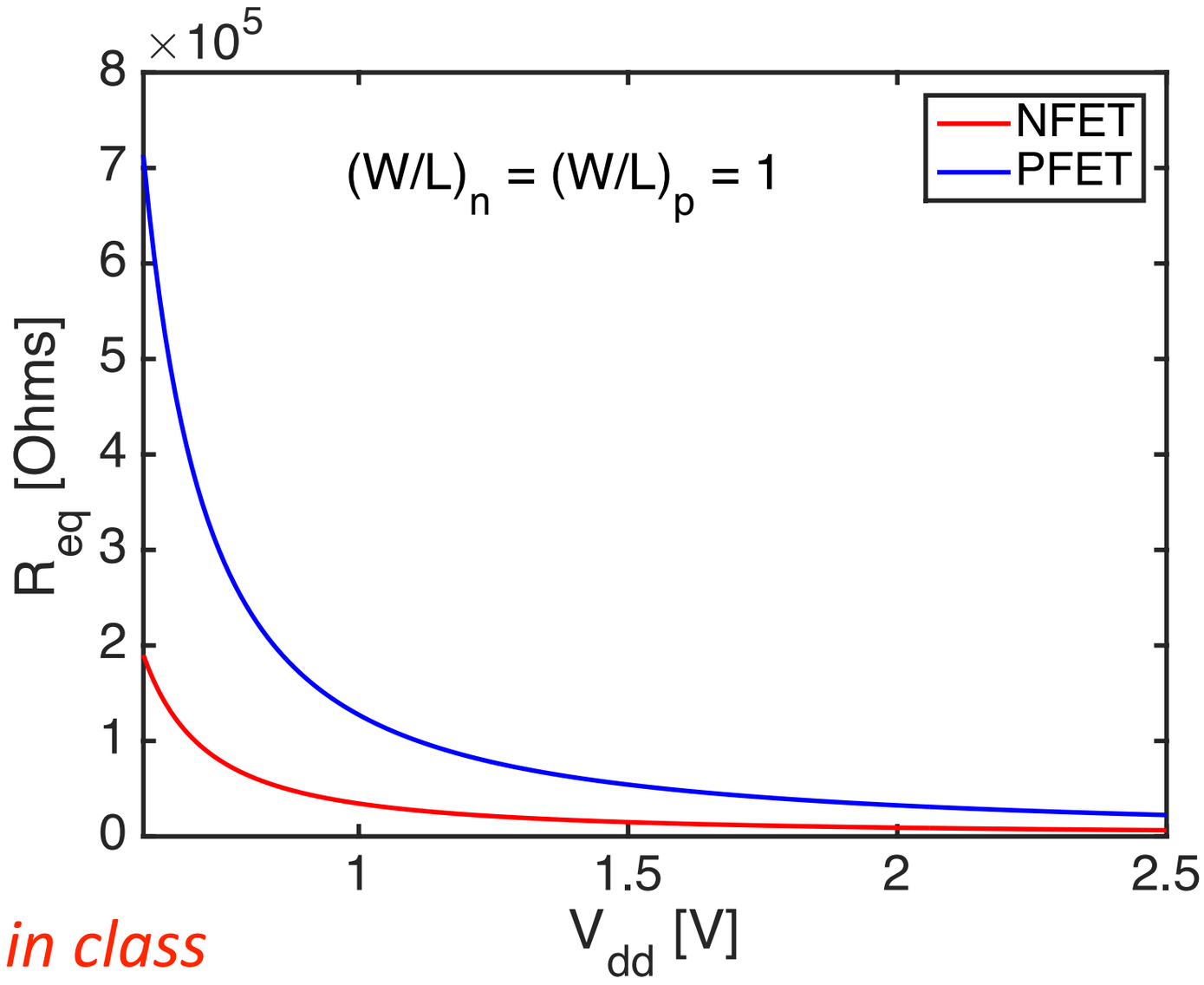
$$R_{eq} = \frac{3V_{dd}}{2(\mu C_{ox})\left(\frac{W}{L}\right)(V_{dd} - V_T)^2}\left(1 - \frac{5}{6}\lambda V_{dd}\right)$$

Observations:

(W/L)⬆, Req⬇

(μC_{ox})⬆, Req⬇

Vdd⬇, Req⬆



Try the MATLAB file given in class

Equivalent resistance in Jan. M. Rabaey's book

The analysis we have presented in class is based on averaging the resistances to find R_{eq}.

A more accurate analysis is given in Eq. (3.41) and (3.42) in Chapter 3 of Jan M. Rabaey's book.

Using the approach in the book, the value of R_{eq} is given as

$$R_{eq} = \frac{3V_{dd}}{4I_{DSAT}}\left(1 - \frac{7}{9}\lambda V_{dd}\right)$$

$$I_{DSAT} = \frac{1}{2}(\mu C_{ox})\left(\frac{W}{L}\right)\left[(V_{dd} - V_T)^2\right]$$

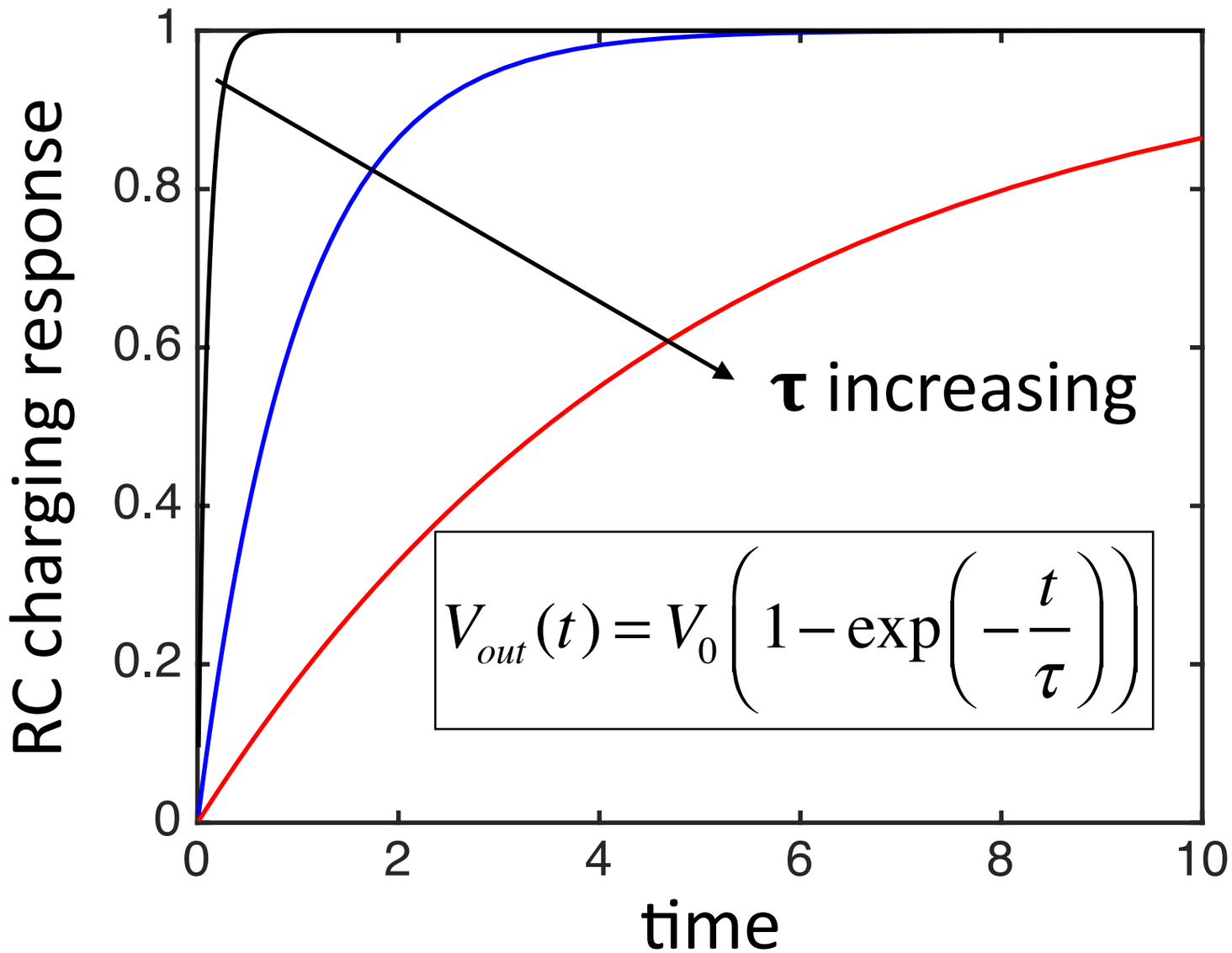
This factor changes. Not a big deal, since mostly $\lambda V_{dd} << 1$.

Summary: charging and discharging of capacitors through NFET and PFET

- Time constant of charging and discharging of capacitance is always given as $\boxed{\tau = 0.69 R_{eq} C}$
- R_{eq}: Equivalent resistance of the transistor.
- To compute R_{eq}, we must take average of initial resistance of transistor (R_1) and value at half way through the transition (R_2).
- That is, $\boxed{R_{eq} = \frac{1}{2}\left(R_1 + R_2\right)}$
- C is the total capacitance that is being charged or discharged.

Summary: charging and discharging of capacitors through NFET and PFET

Time constant of charging and discharging of capacitance is always given as $\tau = 0.69 R_{eq} C$



Summary: charging and discharging of capacitors through NFET and PFET

- If NFET is used to discharge the capacitor, the final voltage across the capacitor will be 0.

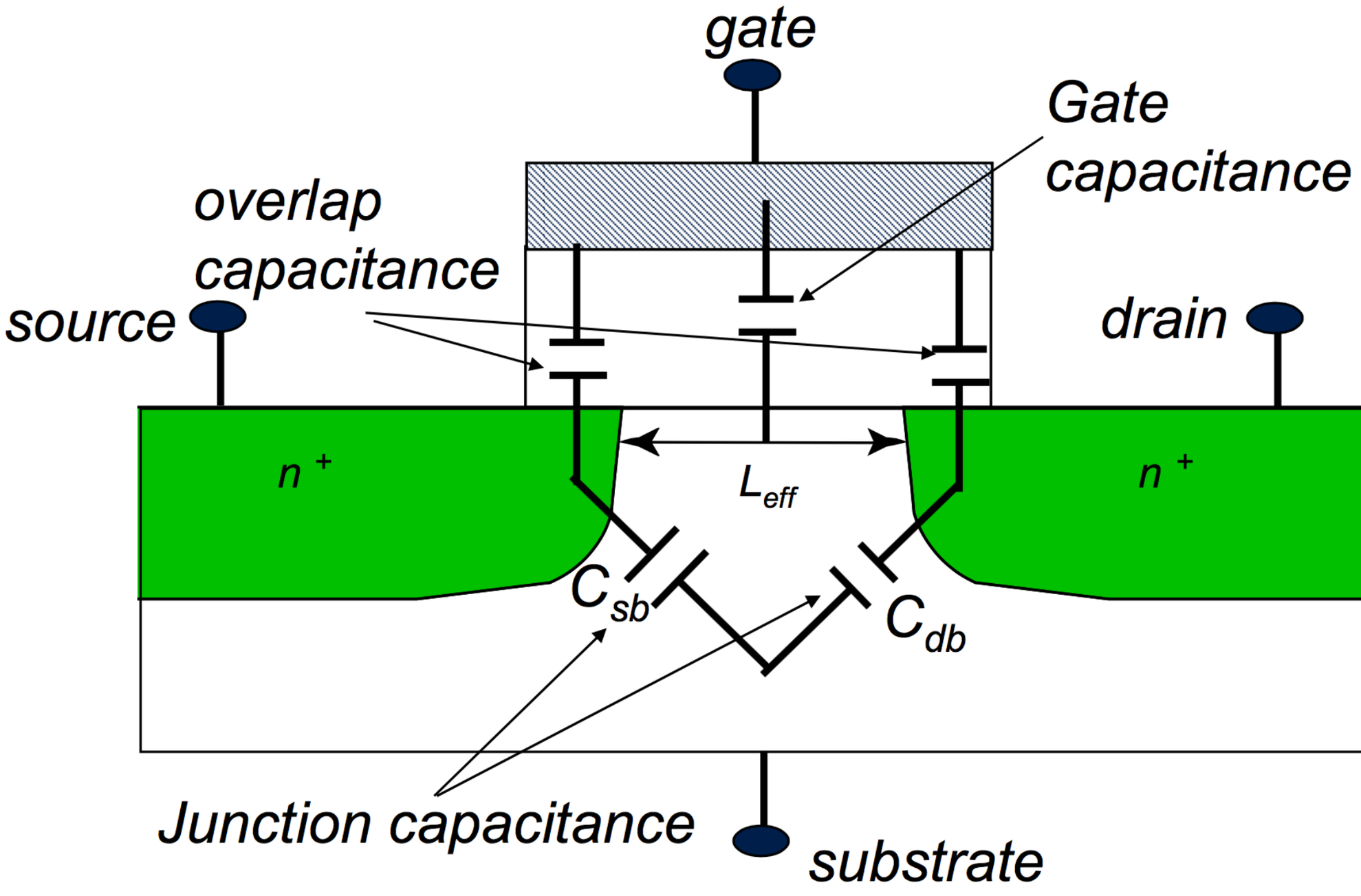
- If PFET is used to charge the capacitor, the final voltage across the capacitor will be V_{dd}.

In CMOS logic:

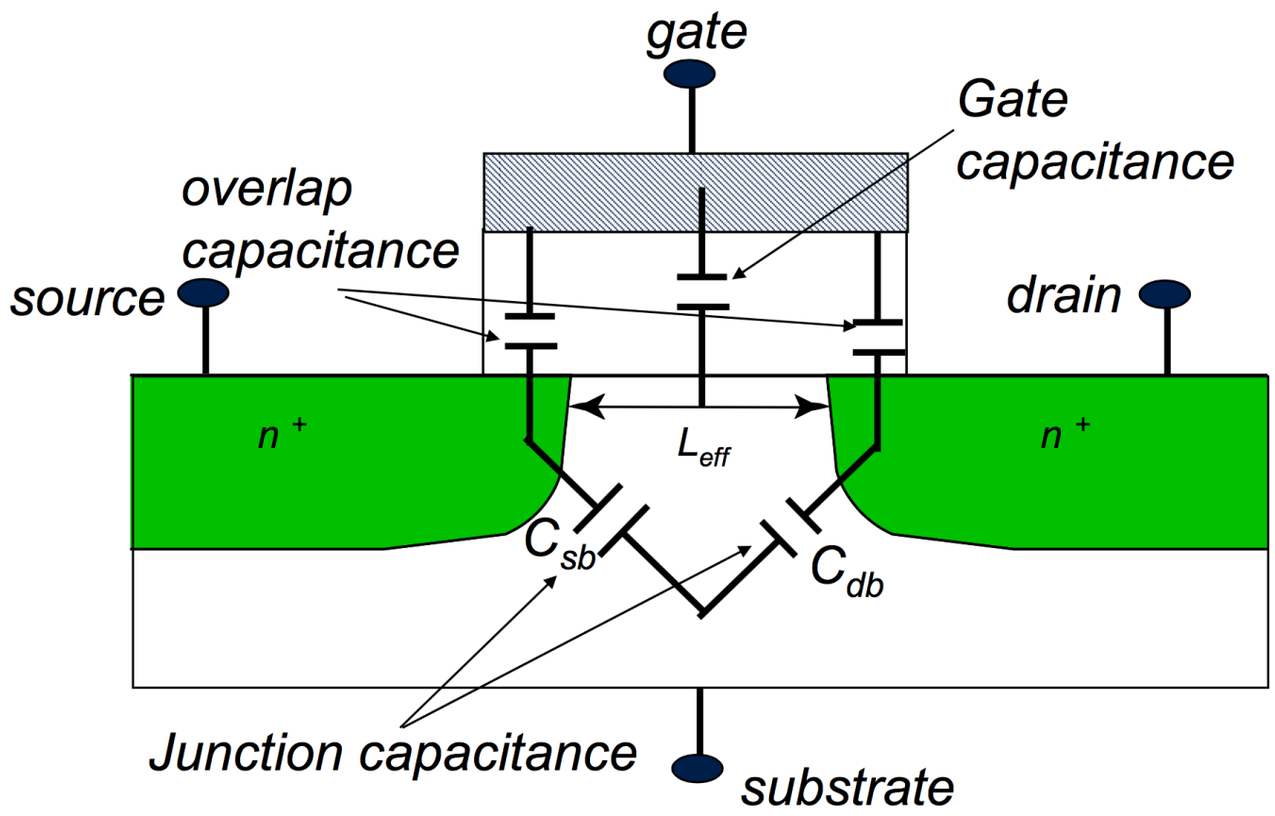
- when a circuit "node" needs to be discharged to ground, we must use NFET to discharge. NFETs form the pull-down network (PDN) in CMOS logic.

- When a circuit "node" needs to be charged to Vdd, we must use PFET to charge. PFETs form the pull-up network (PUN) in CMOS logic.

The MOSFET capacitance



The MOSFET capacitance



a. Gate capacitance
b. Source overlap capacitance
c. Drain overlap capacitance
d. Source-body junction capacitance
e. Drain-body junction capacitance

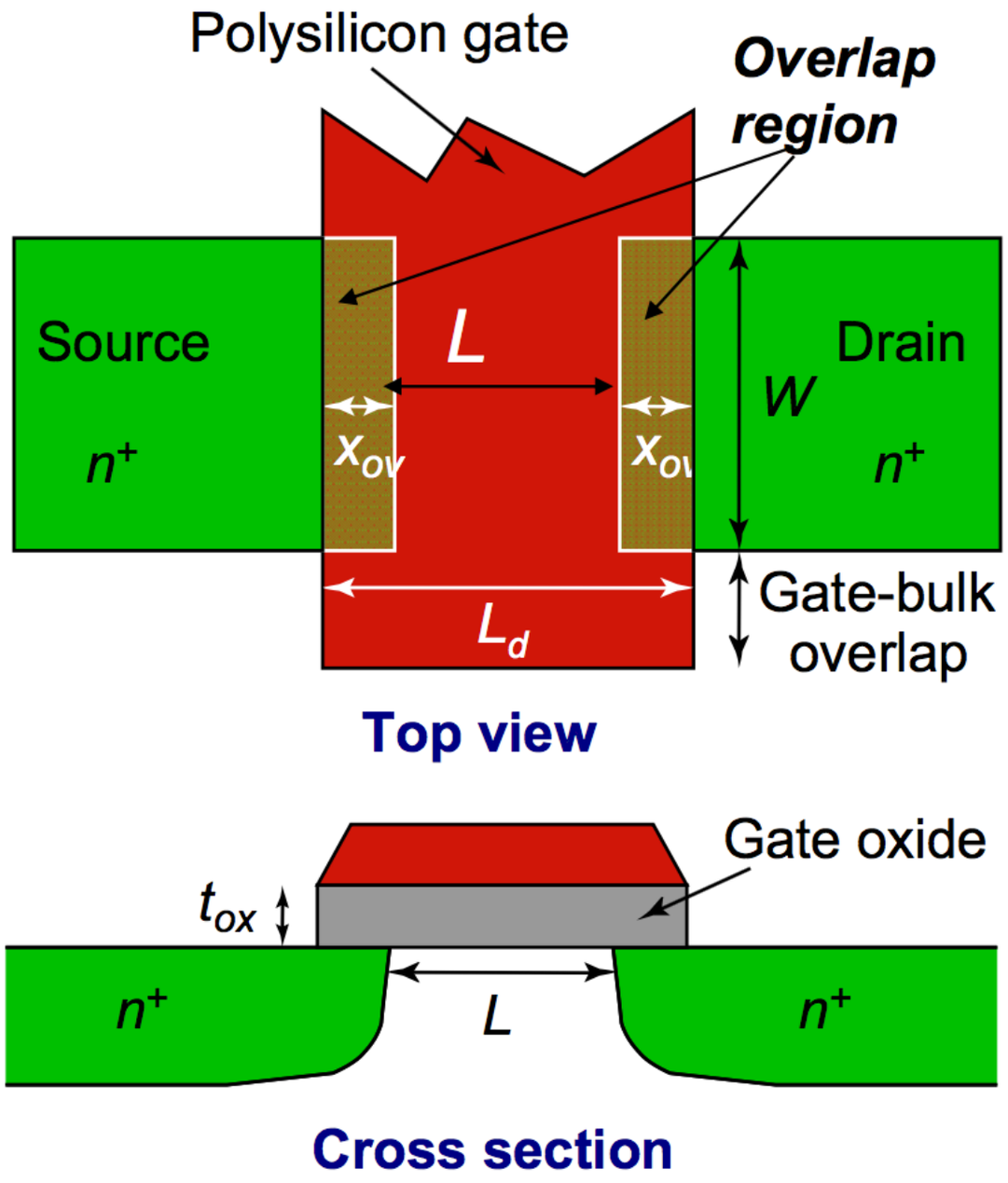
all capacitances depend on width and length of the device.

Except for gate capacitance, other capacitances are parasitic capacitances.

The MOSFET capacitance

- The gate capacitance is the gate voltage dependent capacitance of the Metal-Oxide-Semiconductor structure and depends on the oxide material and the oxide thickness.
- The overlap caps are between gate and source/drain terminals. They are parasitic caps. and does not contribute to the charge. The importance of the overlap cap will be introduced later in “Miller effect” discussion.
- The junction capacitances are due to p-n junction between the n+ source/drain and p-type body (for NFET). They are also parasitic capacitances and depends on the junction doping and drain-to-body and source-to-body biases.
- All capacitances depends on the length and/or width of the devices.

The gate and overlap capacitance



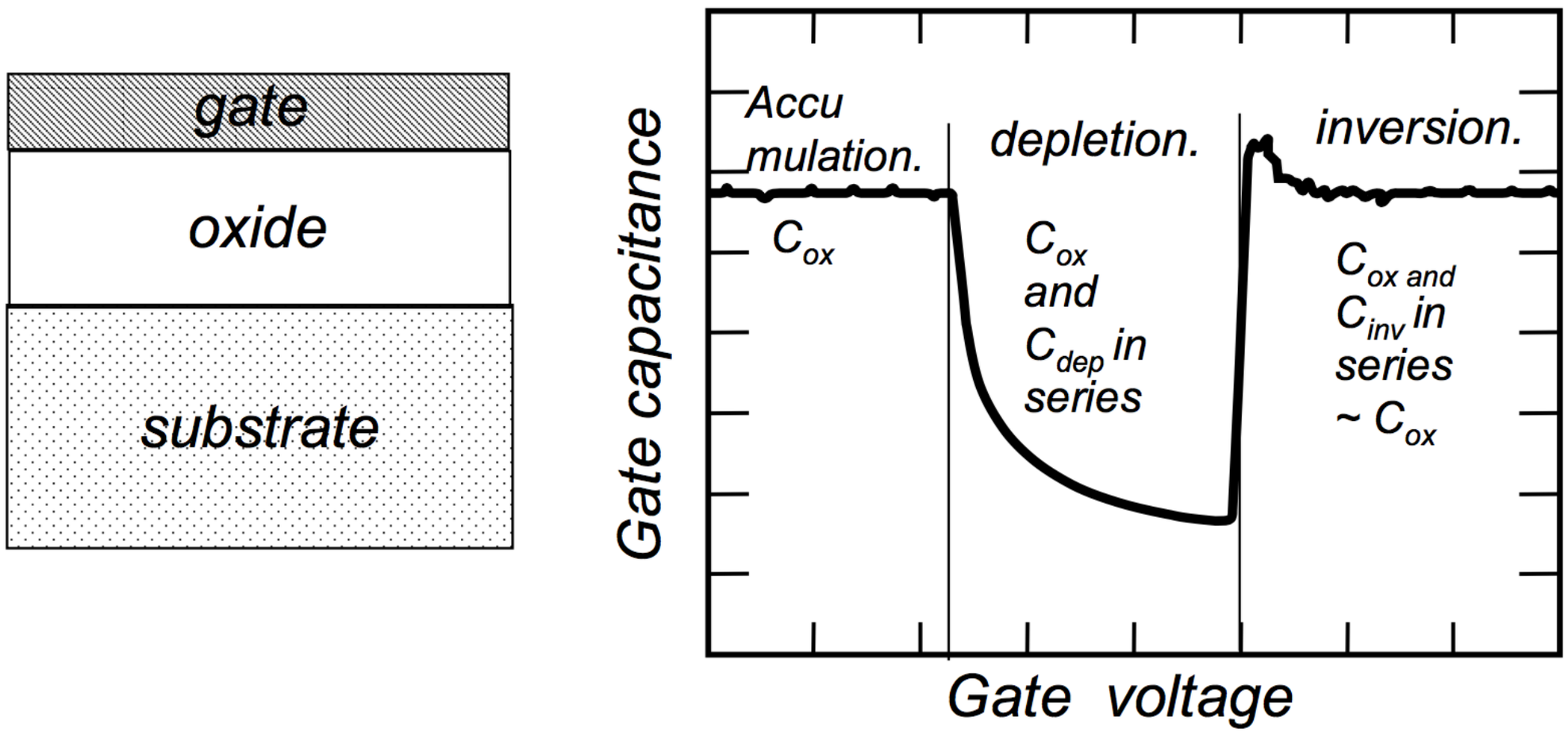
gate capacitance:

$$C_{gate} = C_{ox}WL = \frac{\varepsilon}{t_{ox}}WL$$

overlap capacitance:

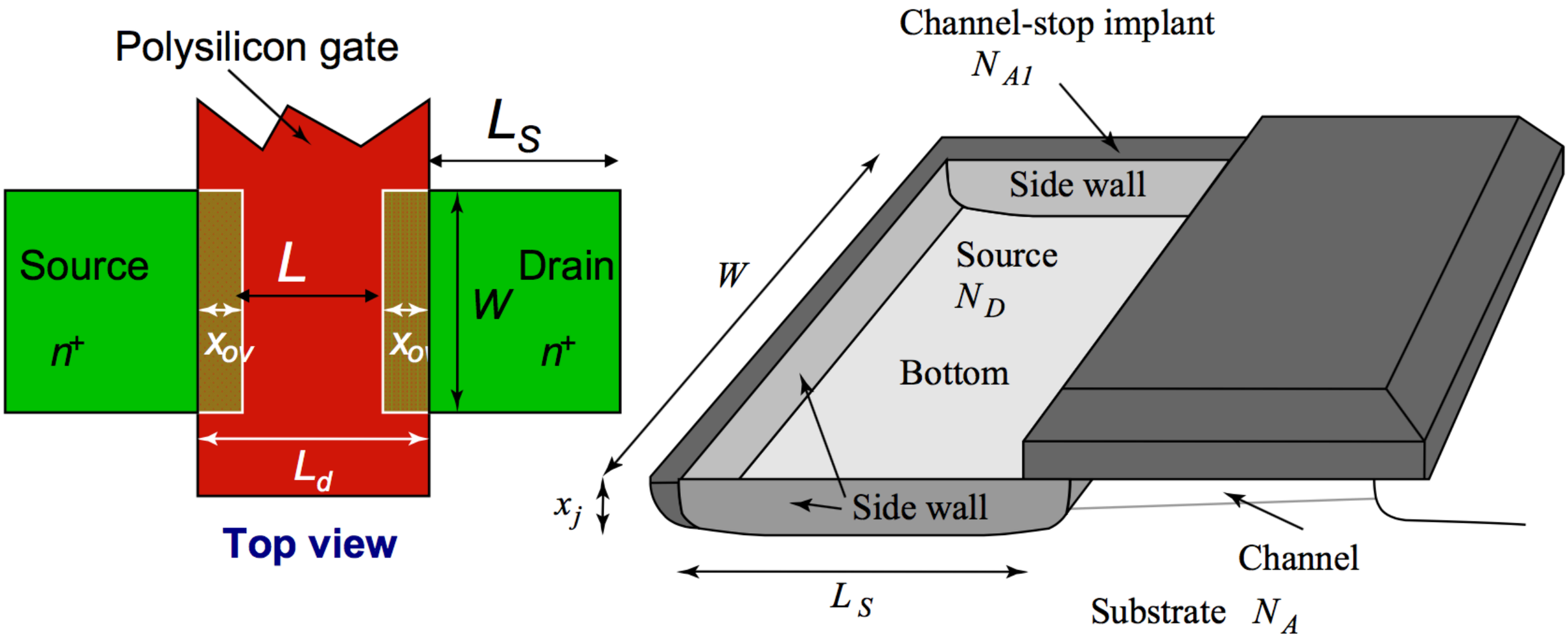
$$C_{ov} = C_{ox}WX_{ov} = \frac{\varepsilon}{t_{ox}}WX_{ov}$$

The gate capacitance



For digital logic we are most interested in "on" (i.e. inversion) and "off" (i.e. in accumulation or weak depletion) devices.

Junction or Diffusion capacitance

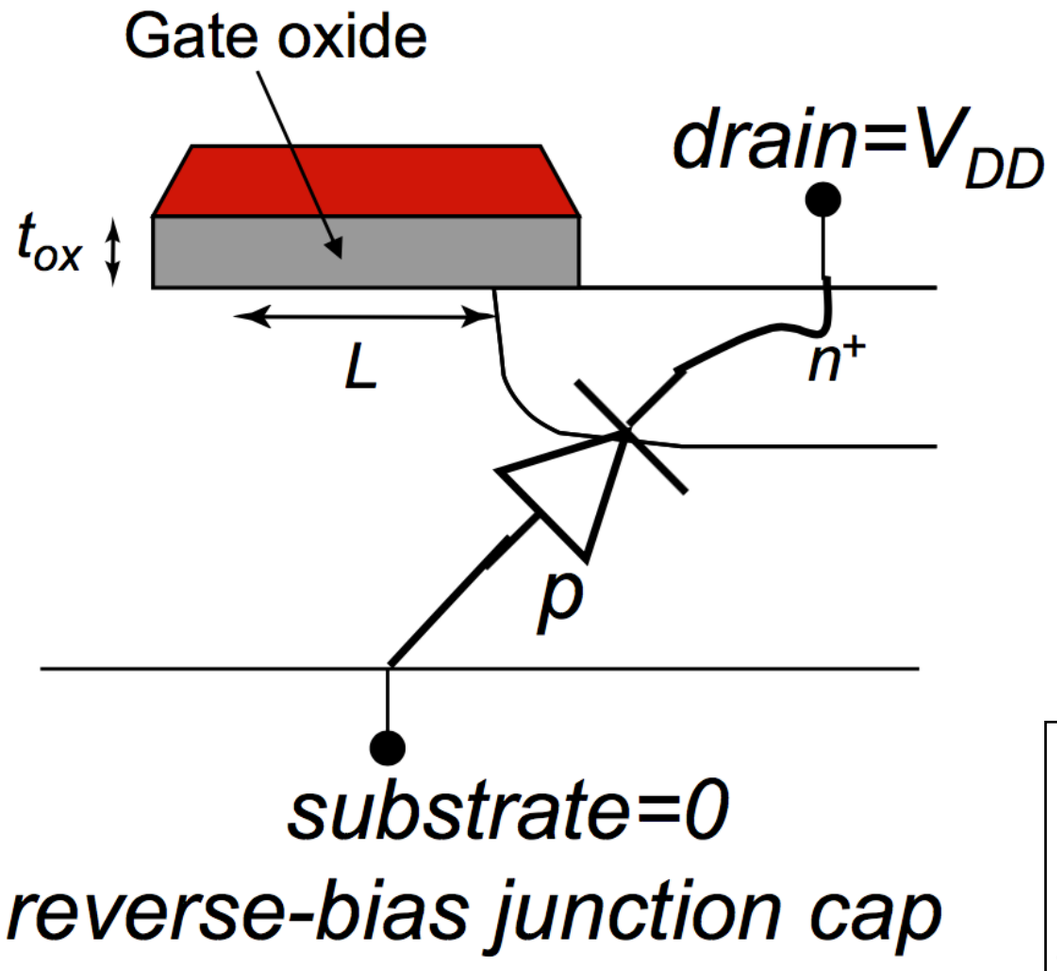


$$C_{Junction} = C_{bottom} + C_{sidewall} = C_j \times AREA + C_{jsw} \times PERIMETER$$

$$= C_j W L_S + C_{jsw}\left(W + 2L_S\right)$$

C_j & C_{jsw} *are technology and voltage dependent parameter*

Junction or Diffusion capacitance



Highly non-linear (voltage-dependent)

$$C_j = \frac{C_{j0}}{\left(1 - \frac{V_{jun}}{\phi_0}\right)^m}$$

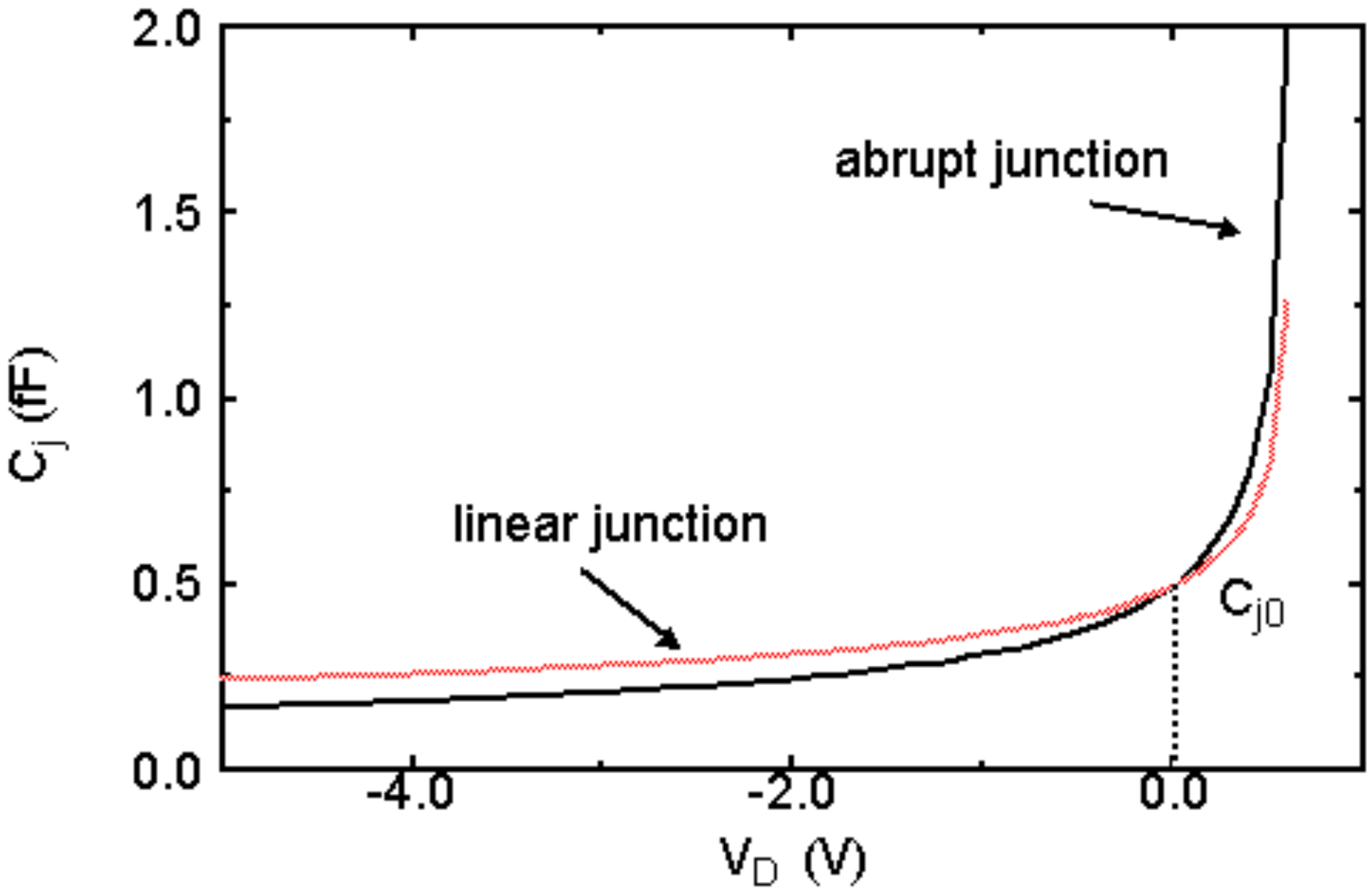
C_{j0}: junction capacitance under zero bias

V_{jun}: junction voltage (negative for reverse biased junctions)

ϕ_0: built-in junction bias

m: grading coefficient (1/3 (linear junction) or 1/2 (abrupt jn.))

Junction or Diffusion capacitance



$$C_j = \frac{C_{j0}}{(1 - V_D/\phi_0)^m}$$

m = 0.5: abrupt junction
m = 0.33: linear junction

Linearizing junction capacitance

An easy way to linearize the junction capacitance is given as

$$C_j = k_{eq} C_{j0}$$

$$k_{eq} = \frac{-\phi_0^m}{\left(V_{high} - V_{low}\right)(1-m)}\left[\left(\phi_0 - V_{high}\right)^{1-m} - \left(\phi_0 - V_{low}\right)^{1-m}\right]$$

- The factor k_{eq} is the linearizing factor.

- C_{j0} is the junction capacitance per unit area under zero bias conditions.

Model for manual analysis

gate capacitance:

$$C_{gate} = \frac{\varepsilon}{t_{ox}} WL$$

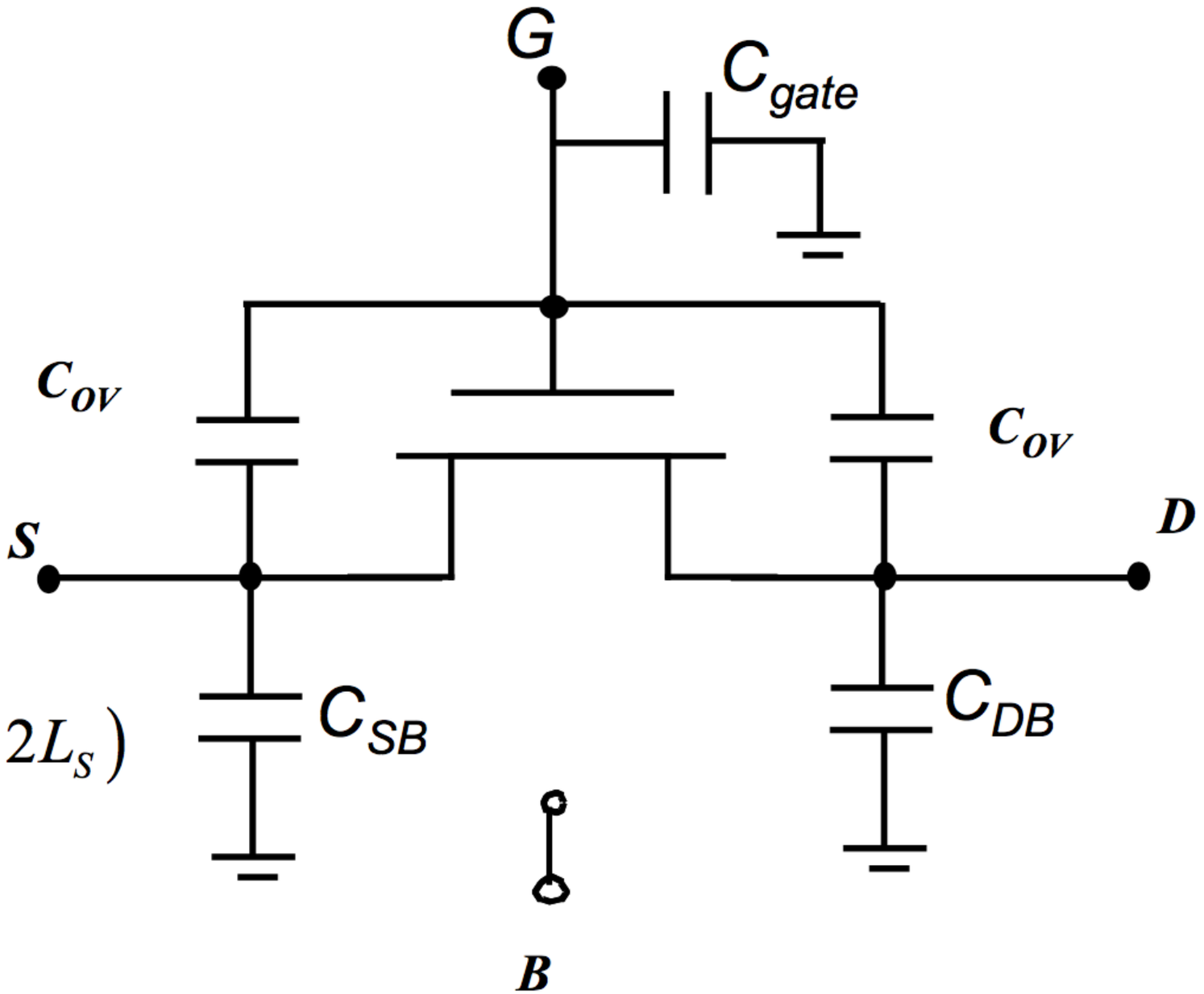
overlap capacitance:

$$C_{ov} = \frac{\varepsilon}{t_{ox}} WX_{ov}$$

Junction capacitance:

$$C_{Junction} = C_j WL_S + C_{jsw}\left(W + 2L_S\right)$$

C_j & C_{jsw} are tech. param.



CMOS inverter analysis

a. Steady state or DC operation

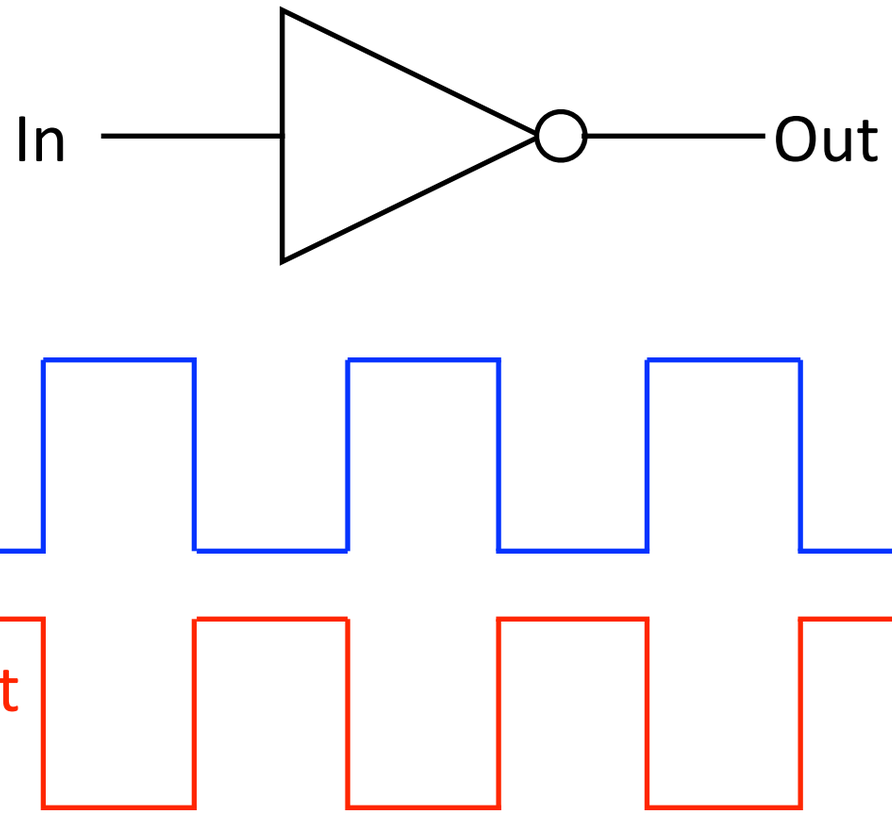
b. Switching characteristics

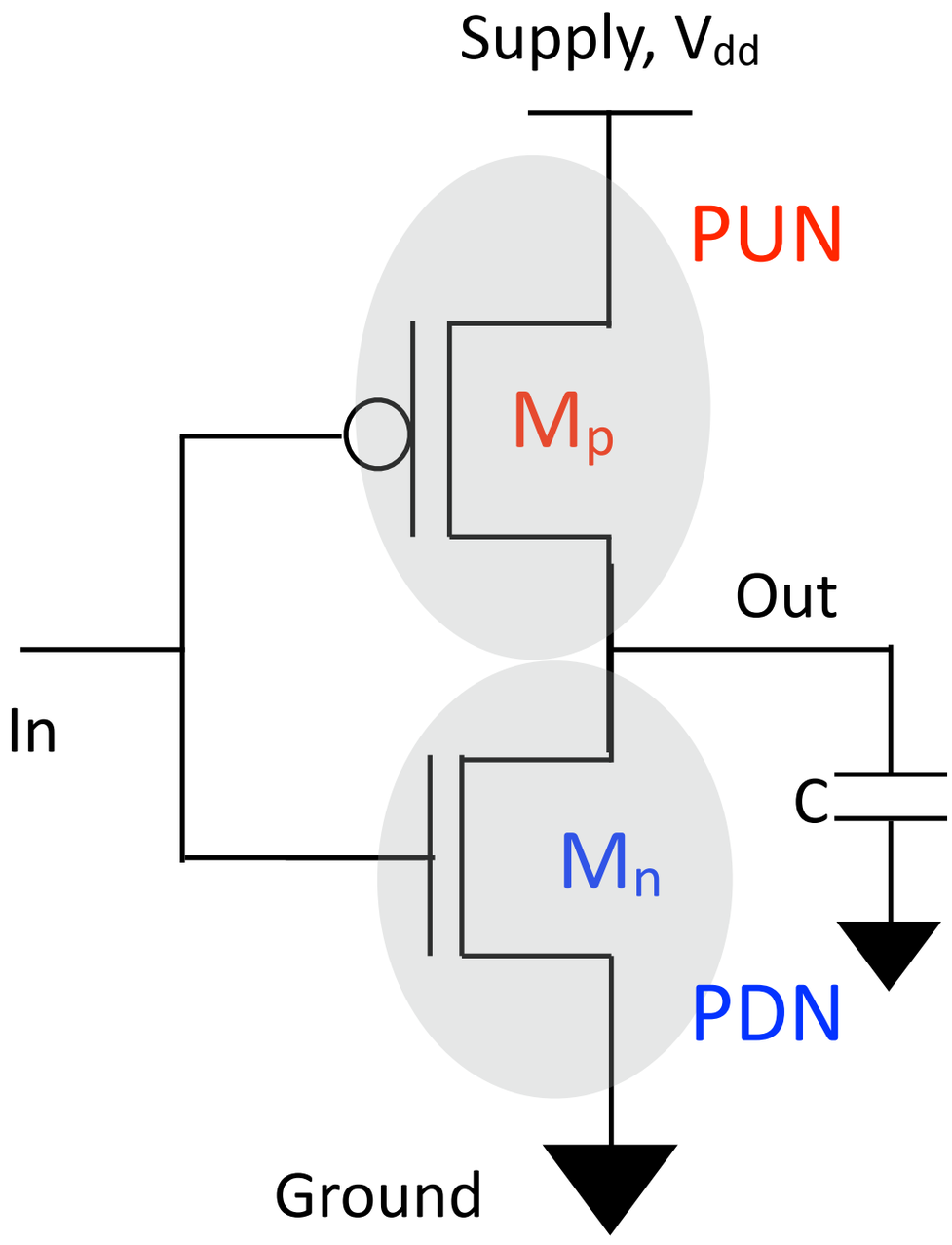
c. Power dissipation

CMOS inverter

- Rail-to-rail voltage swing
- Logic levels are independent of device sizes – ratioless logic
- Low-impedance path to V_{dd} or ground
- Infinite input impedance – infinite drivability
- No direct path between V_{dd} and ground in steady state

CMOS inverter

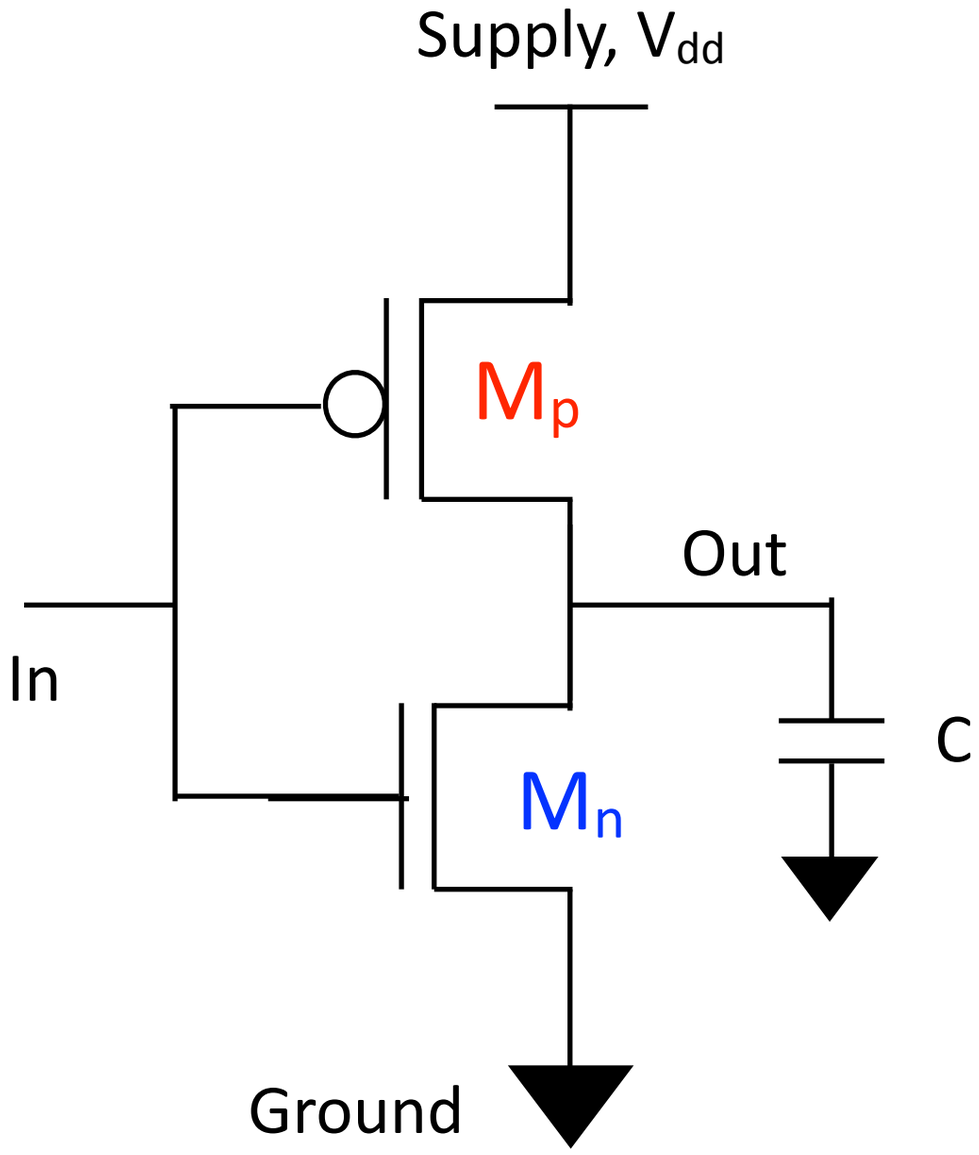




- The PFET (Mp) is good at pulling up "C" to Vdd.

- The NFET (Mn) is good at pulling down "C" to ground.

Inverter functionality



$\beta_p = \kappa_p \times (W/L)_p$

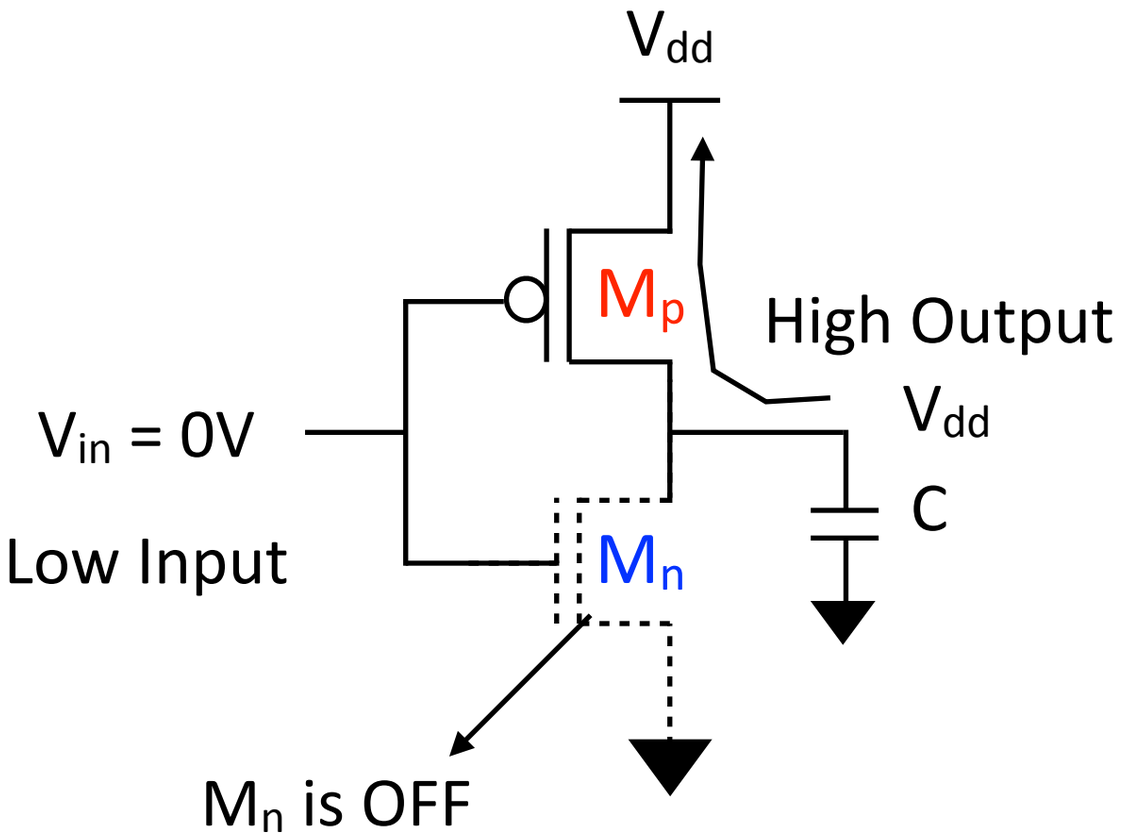
$\beta_n = \kappa_n \times (W/L)_n$

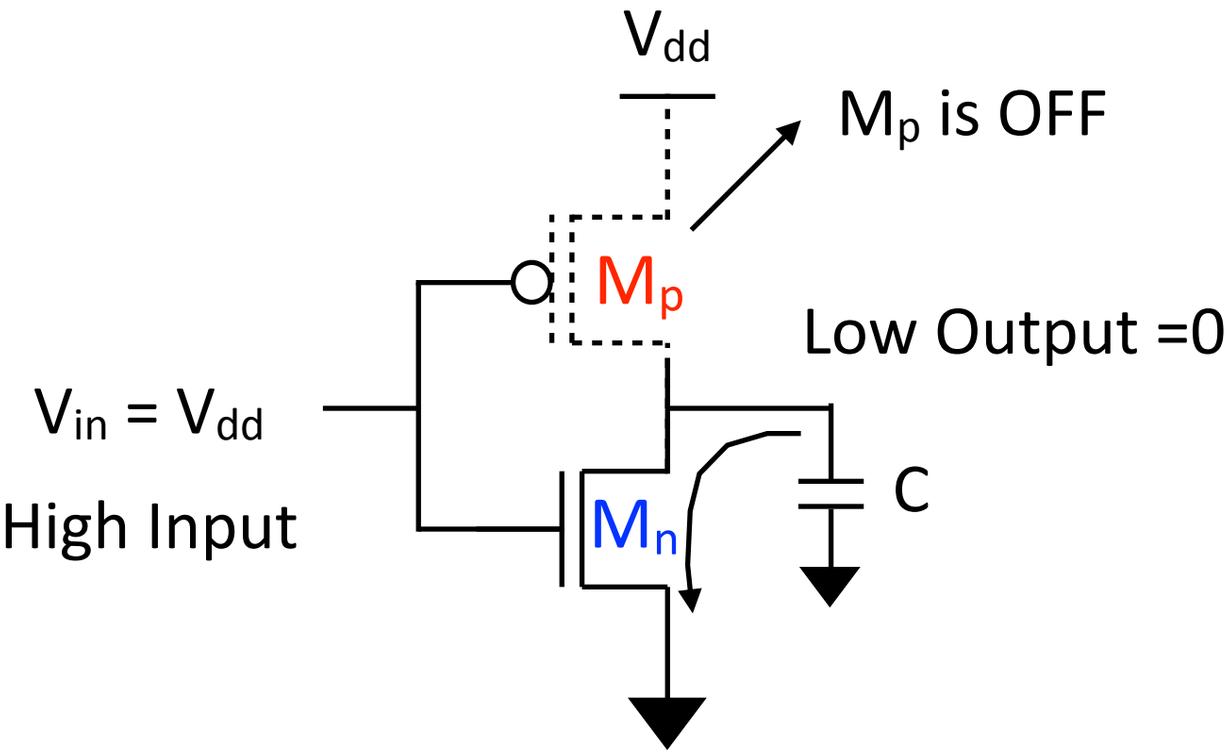
Typically: $\kappa_n > \kappa_p$

Why:

Because $\mu_n > \mu_h$

Inverter functionality

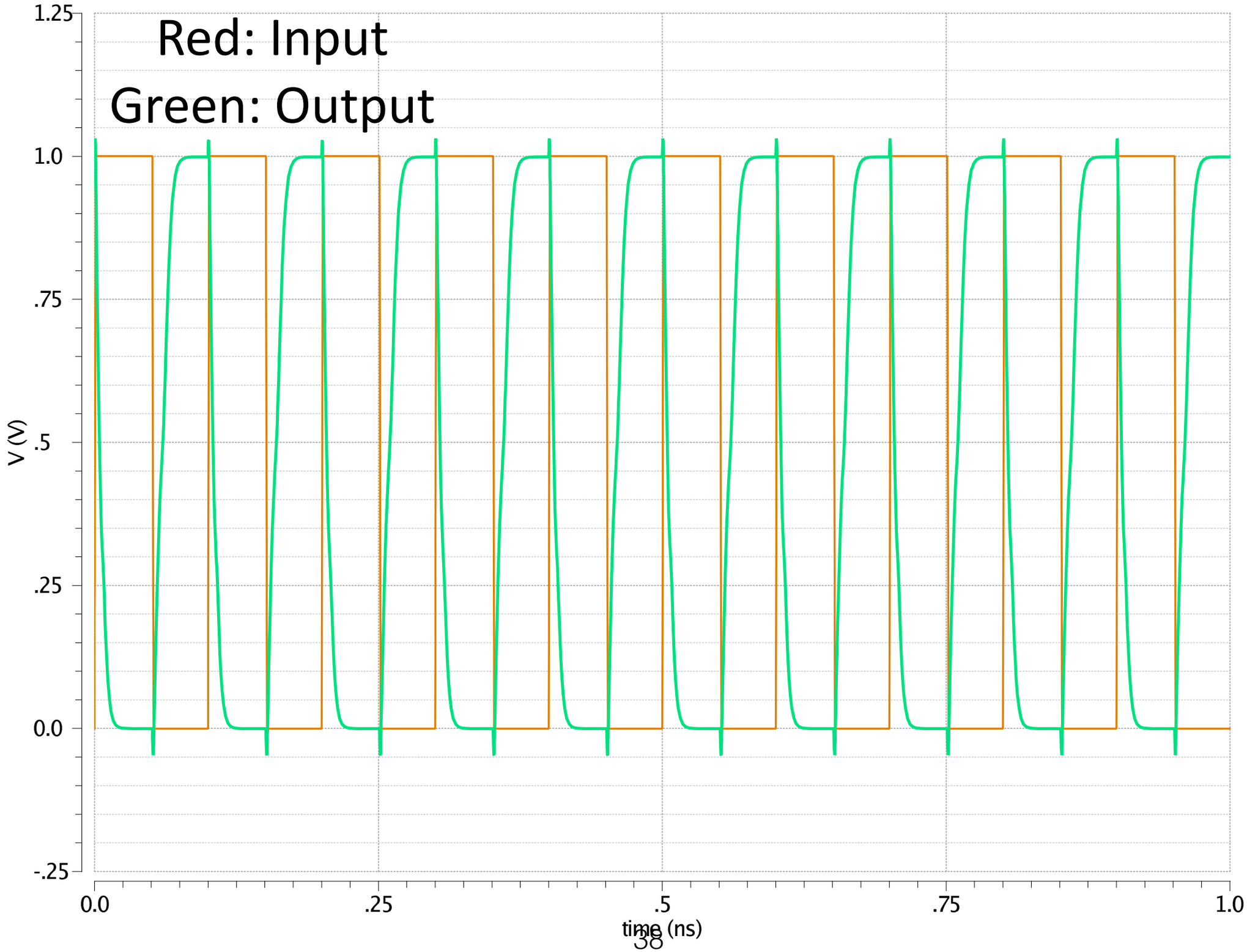




Low output level = 0

High output level = V_{dd}

Inverter transient response (HSPICE sim.)

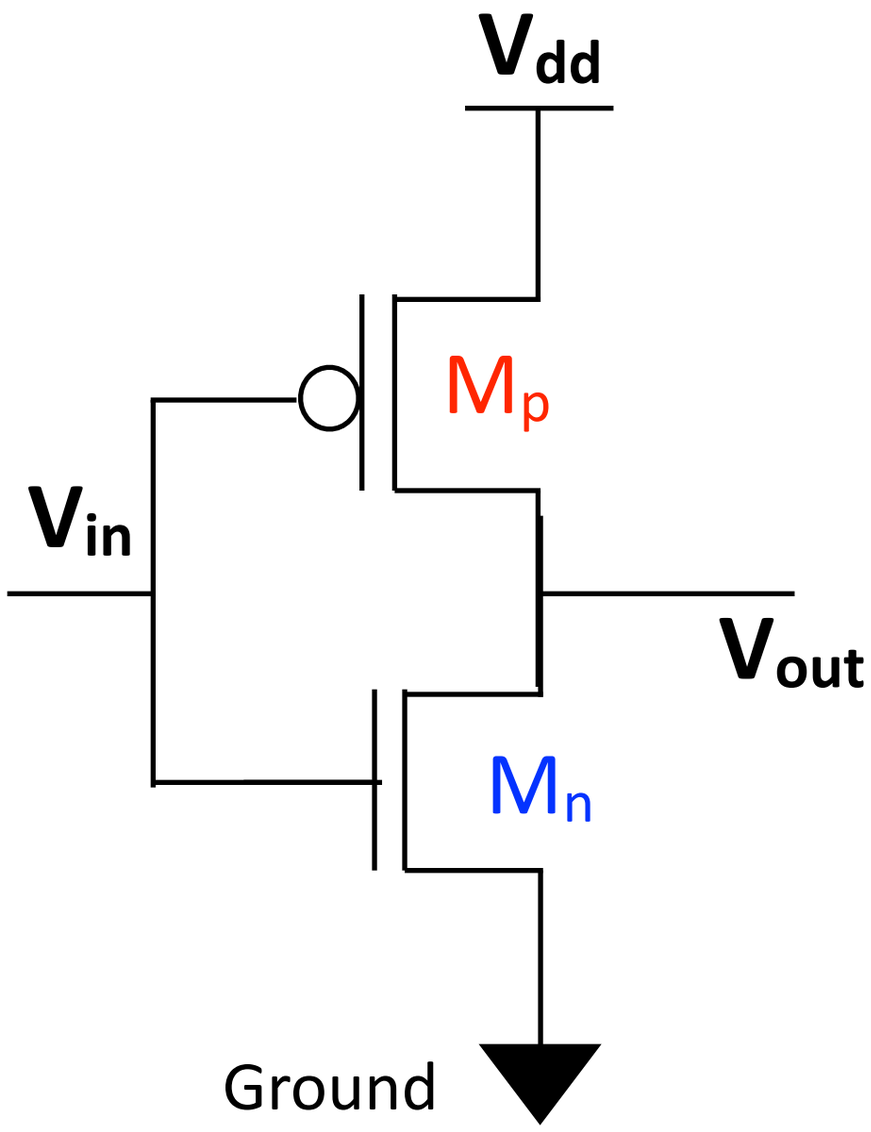


CMOS inverter analysis

Steady state or DC characteristics

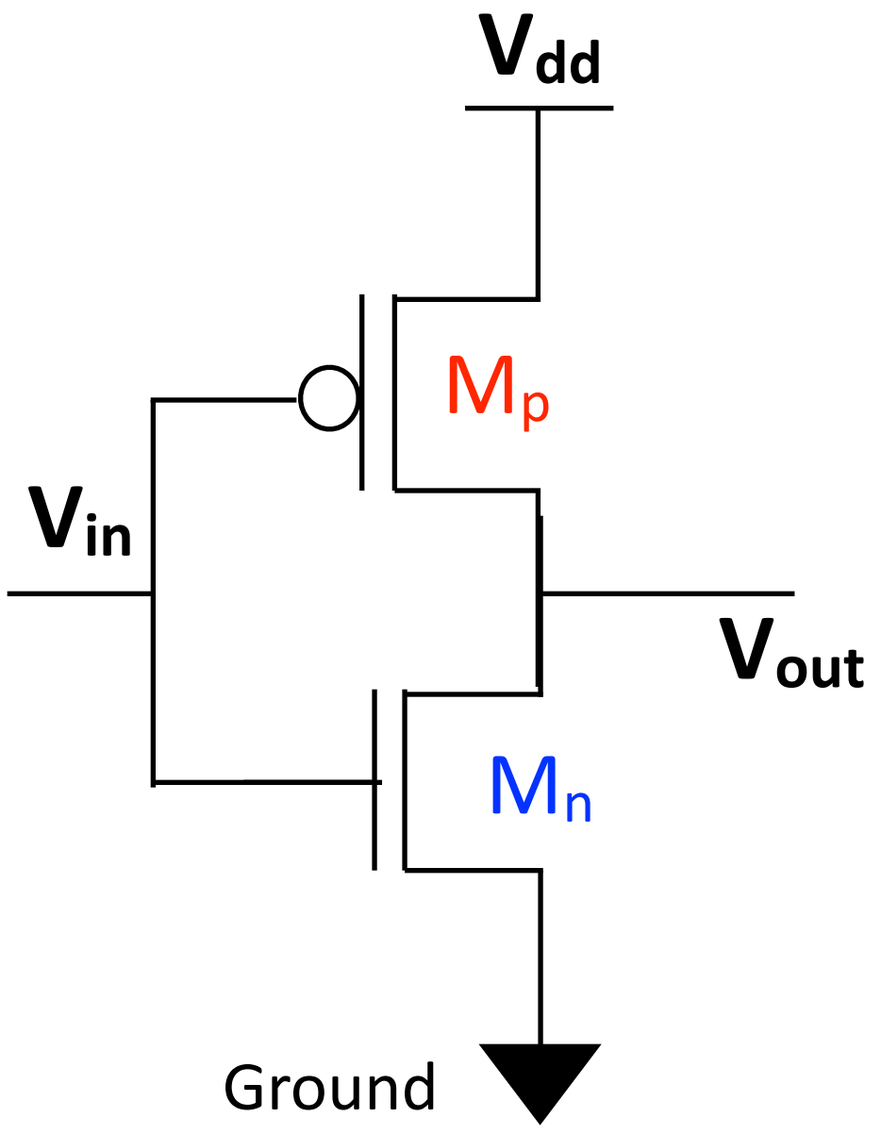
Robustness and noise tolerance

Voltage transfer characteristics (VTC)



VTC tells us V_{out} versus V_{in} for the inverter.

Voltage transfer characteristics (VTC)



VTC tells us V_{out} versus V_{in} for the inverter.

Voltage conditions:

NFET: $V_{gsn} = V_{in},\ V_{dsn} = V_{out}$

PFET: $V_{sgp} = V_{dd}\text{-}V_{in},\ V_{sdp} = V_{dd}\text{-}V_{out}$

DC characteristics:

$$I_{NFET}(V_{gsn},\ V_{dsn},\ V_{thn}) = I_{PFET}(V_{sgp},\ V_{sdp},\ V_{thp})$$

Key: Need to determine the operating region of NFET and PFET for different input and output voltage

Voltage transfer characteristics (VTC)

DC characteristics:

$$I_{NFET}(V_{gsn},\ V_{dsn},\ V_{thn}) = I_{PFET}(V_{sgp},\ V_{sdp},\ V_{thp})$$

NFET Regions

$$cut-off: V_{in} < V_{thn}, V_{out} \sim V_{DD}:$$

$$saturation: V_{in} > V_{thn}, V_{out} > V_{in} - V_{thn}$$

$$linear: V_{in} > V_{thn}, V_{out} < V_{in} - V_{thn}$$

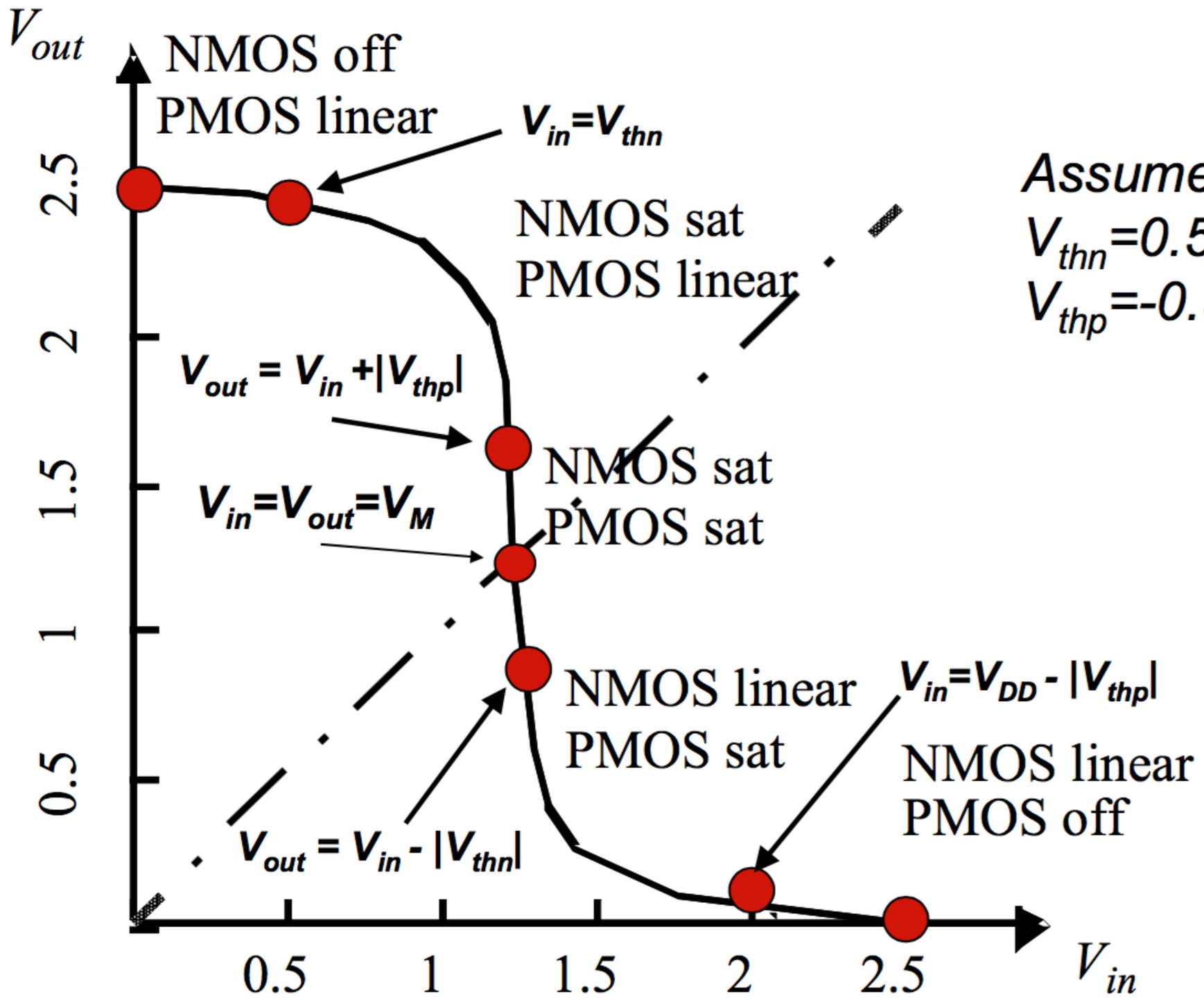
PFET Regions

$$linear: V_{in} < V_{DD} - \left|V_{thp}\right|, V_{DD} - V_{out} < V_{DD} - V_{in} - \left|V_{thp}\right|$$

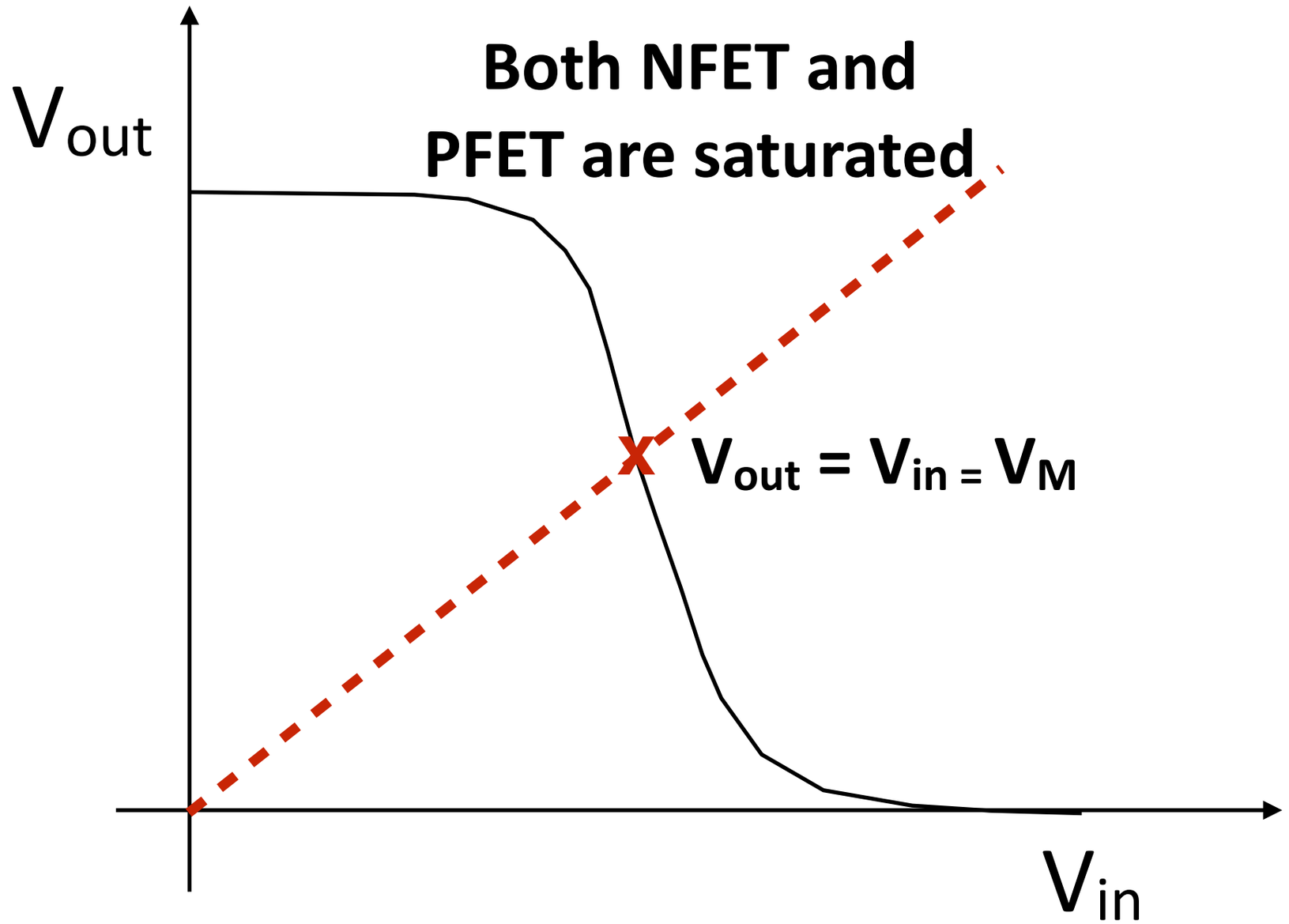
$$saturation: V_{in} < V_{DD} - \left|V_{thp}\right|, V_{DD} - V_{out} > V_{DD} - V_{in} - \left|V_{thp}\right|$$

$$cut-off: V_{in} > V_{DD} - \left|V_{thp}\right|, V_{out} \sim 0$$

Voltage transfer characteristics (VTC) graphically explained

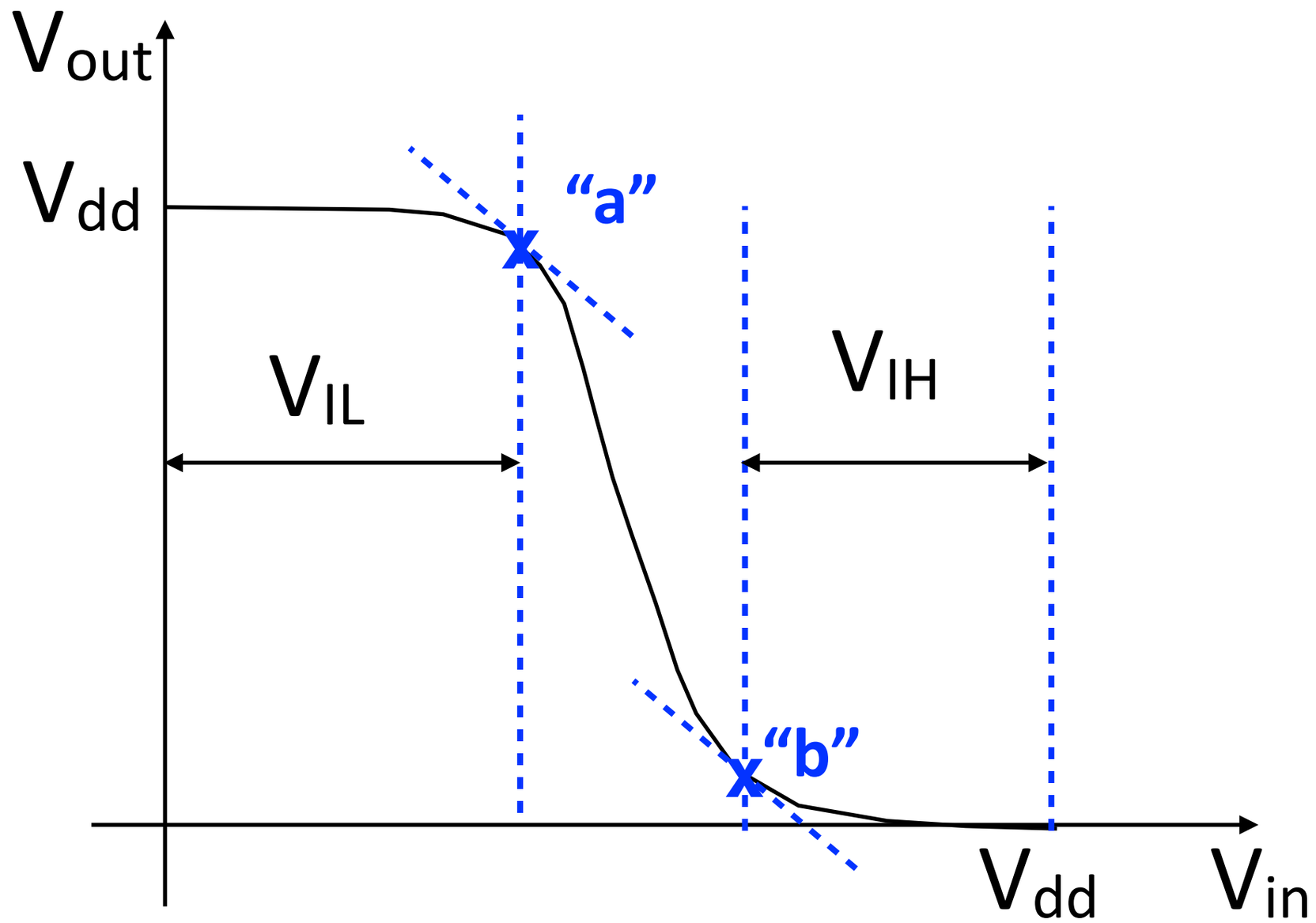


Switching threshold voltage



$V_M = V_{out} = V_{in}$ —> known as switching threshold or the trip point.

Noise margins

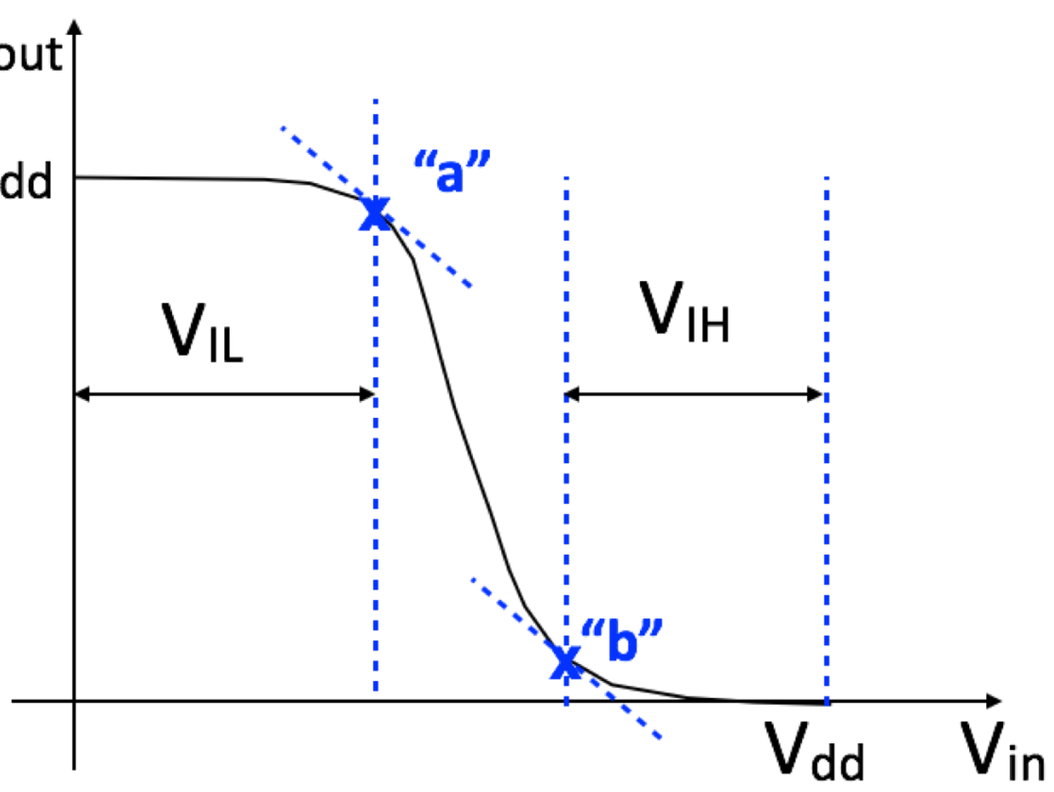


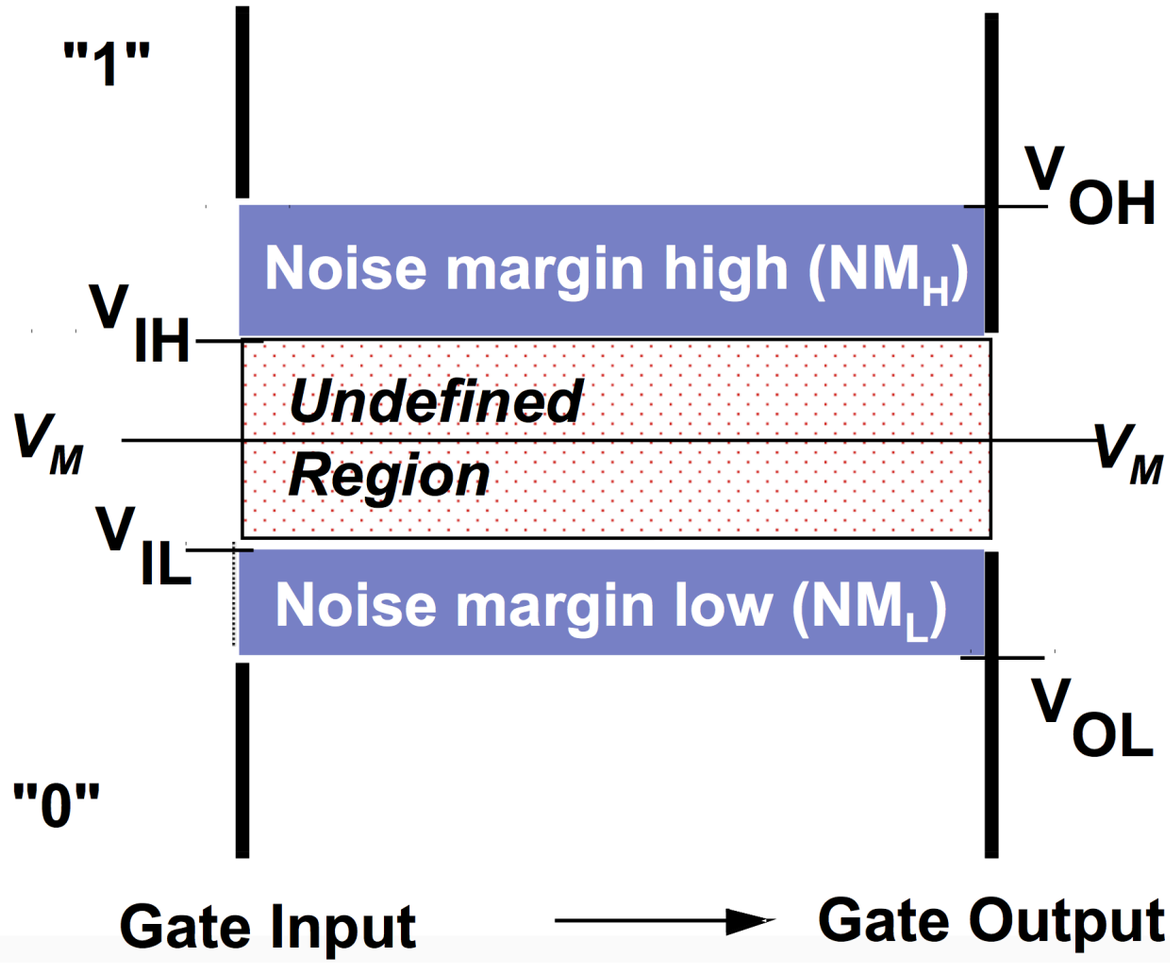
"a" and "b" are points with gain = 1

V_{IL}: low noise margin

V_{IH}: high noise margin

What do noise margins signify physically?





- Noise margins signify robustness to noise.
- An input signal within (0, V_{IL}) voltage levels will always be considered as logic "0" or LOW.
- An input signal within (V_{IH}, V_{DD}) levels will always be considered as logic "1" or HIGH.

Switching threshold (V_M) computation

At $V_{in} = V_{out} = V_M$, both NFET and PFET are saturated.

$$V_M = \frac{V_{dd} - |V_{Tp}| + \sqrt{\frac{\beta_n}{\beta_p}} V_{Tn}}{1 + \sqrt{\frac{\beta_n}{\beta_p}}}$$

Recall:

$\beta_n = (\mu_n Cox)(W/L)_n$

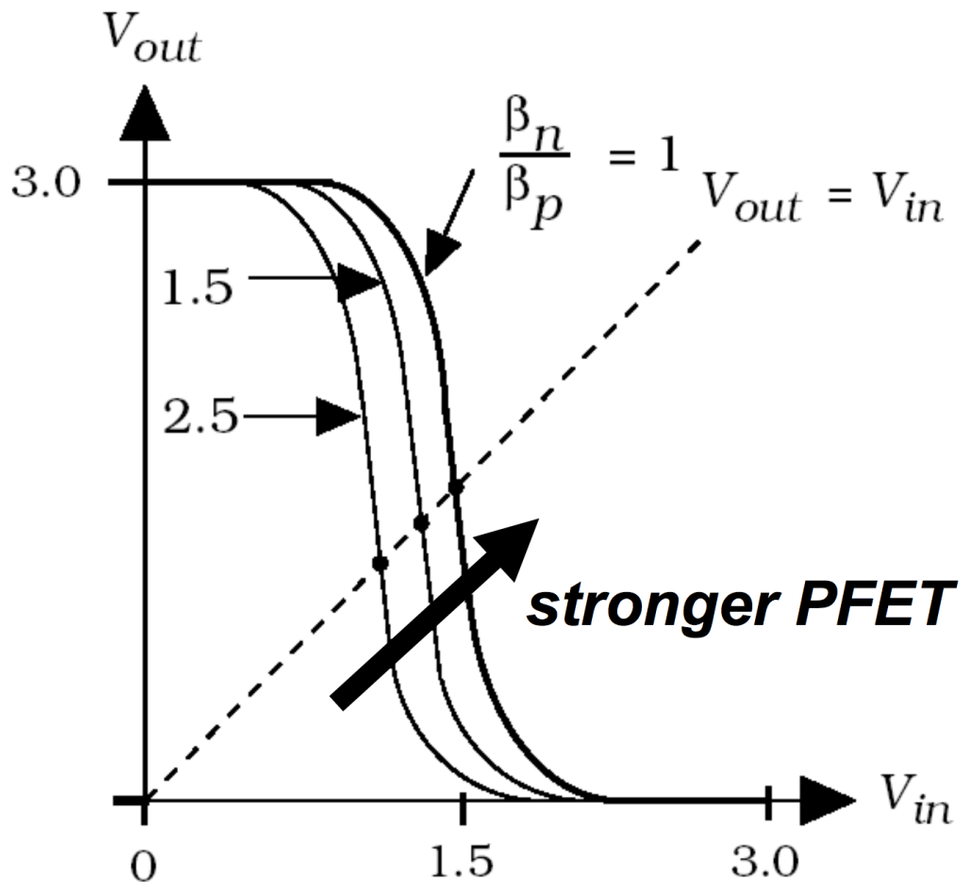
$\beta_p = (\mu_h Cox)(W/L)_p$

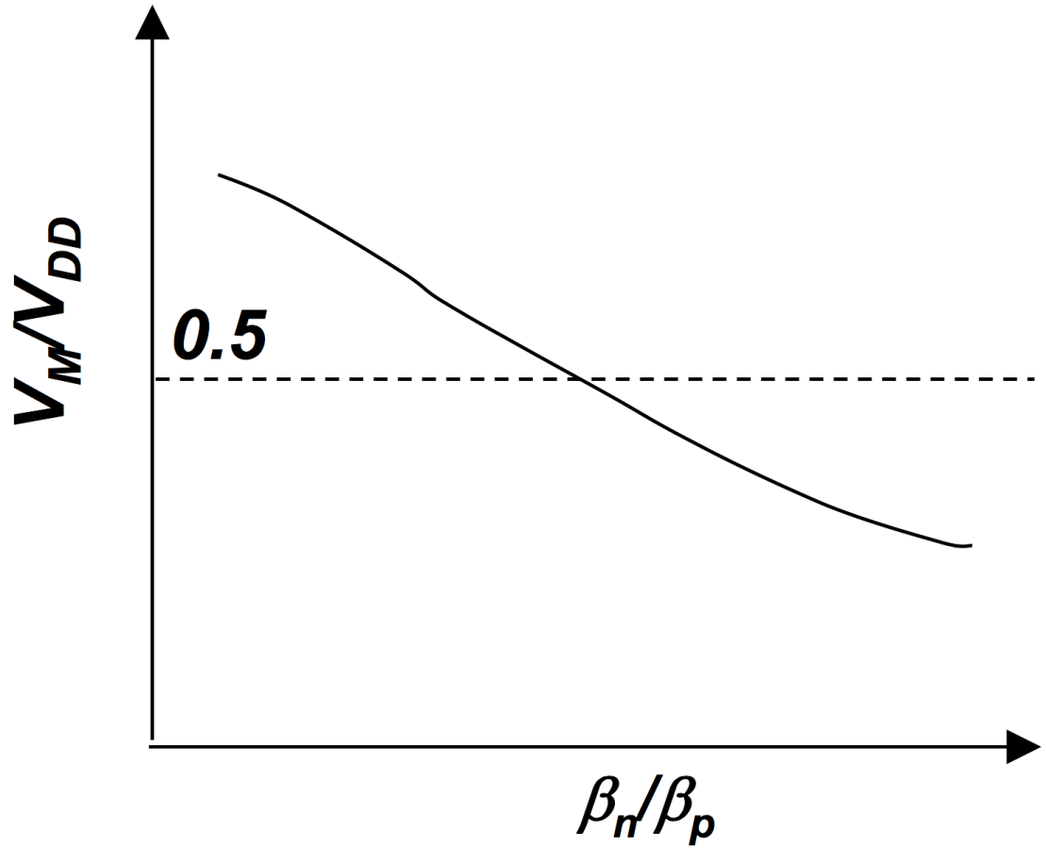
$$For\ V_M = rV_{DD} \Rightarrow \sqrt{\frac{\beta_n}{\beta_p}} = \frac{(1-r)V_{DD} - |V_{thp}|}{(rV_{DD} - V_{thn})}$$

$$To\ achieve\ V_M = 0.5V_{DD}\ with\ |V_{thp}| = V_{thn} \Rightarrow \beta_n/\beta_p = 1$$

$$Normally,\ \mu_n/\mu_p = 2,\ W_p/L_p = 2(W_n/L_n)\ (assuming, C_{oxp} = C_{oxn})$$

Design of switching threshold





Stronger PFET —> difficult high-to-low transition —> higher switching threshold (V_M)

Stronger NFET —> difficult low-to-high transition —> low switching threshold (V_M)

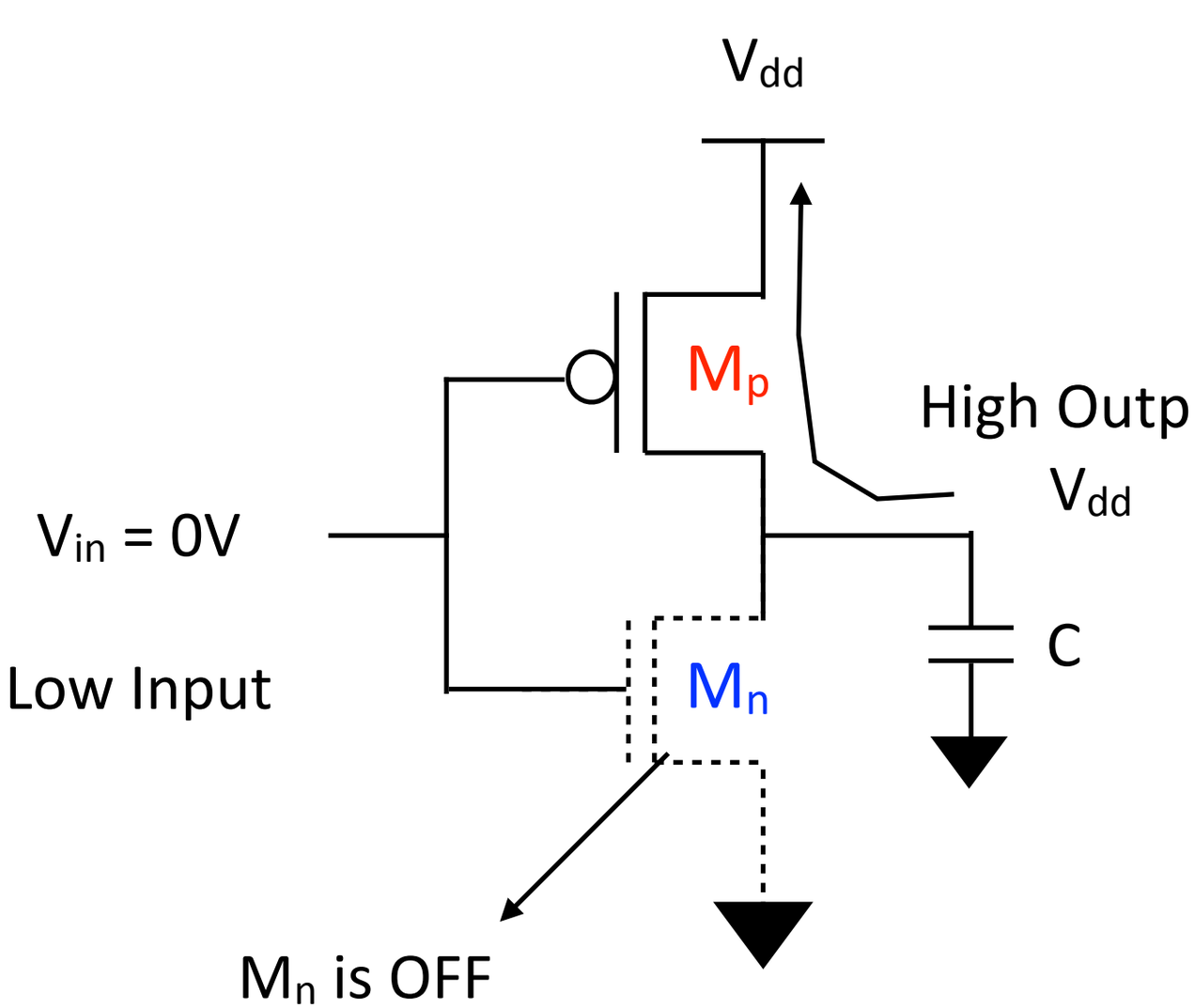
Proper choice of (β_n/β_p)is necessary to achieve a desired switching threshold (V_M)

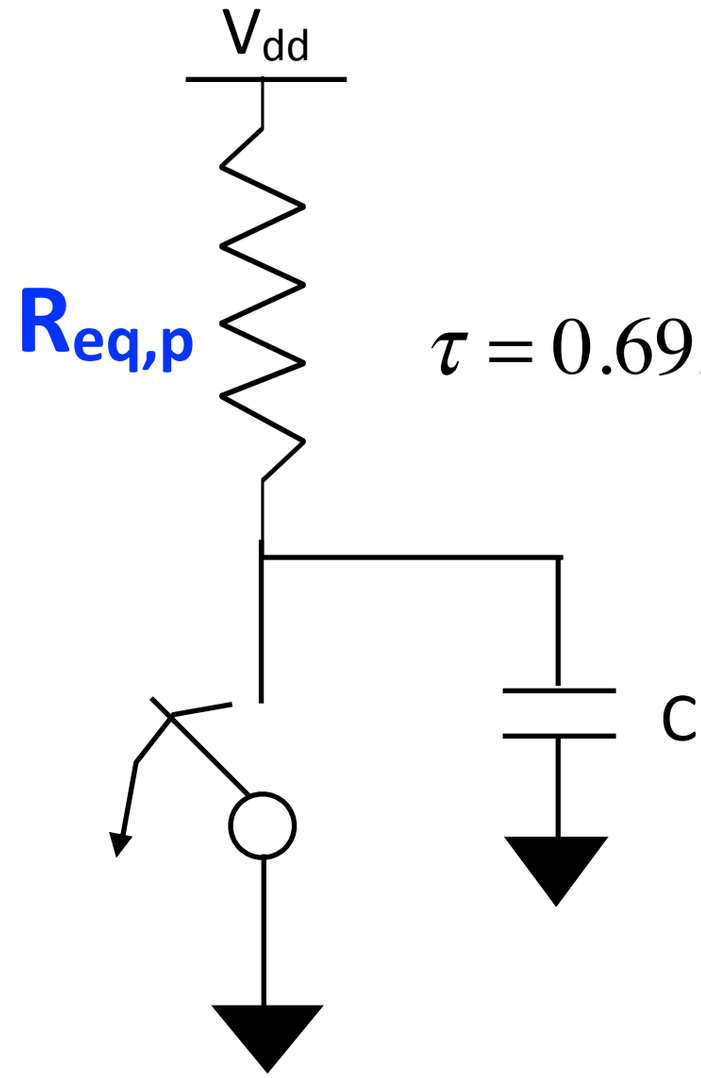
CMOS inverter analysis

Switching characteristics

Performance (speed)

Low to high transition time in inverter





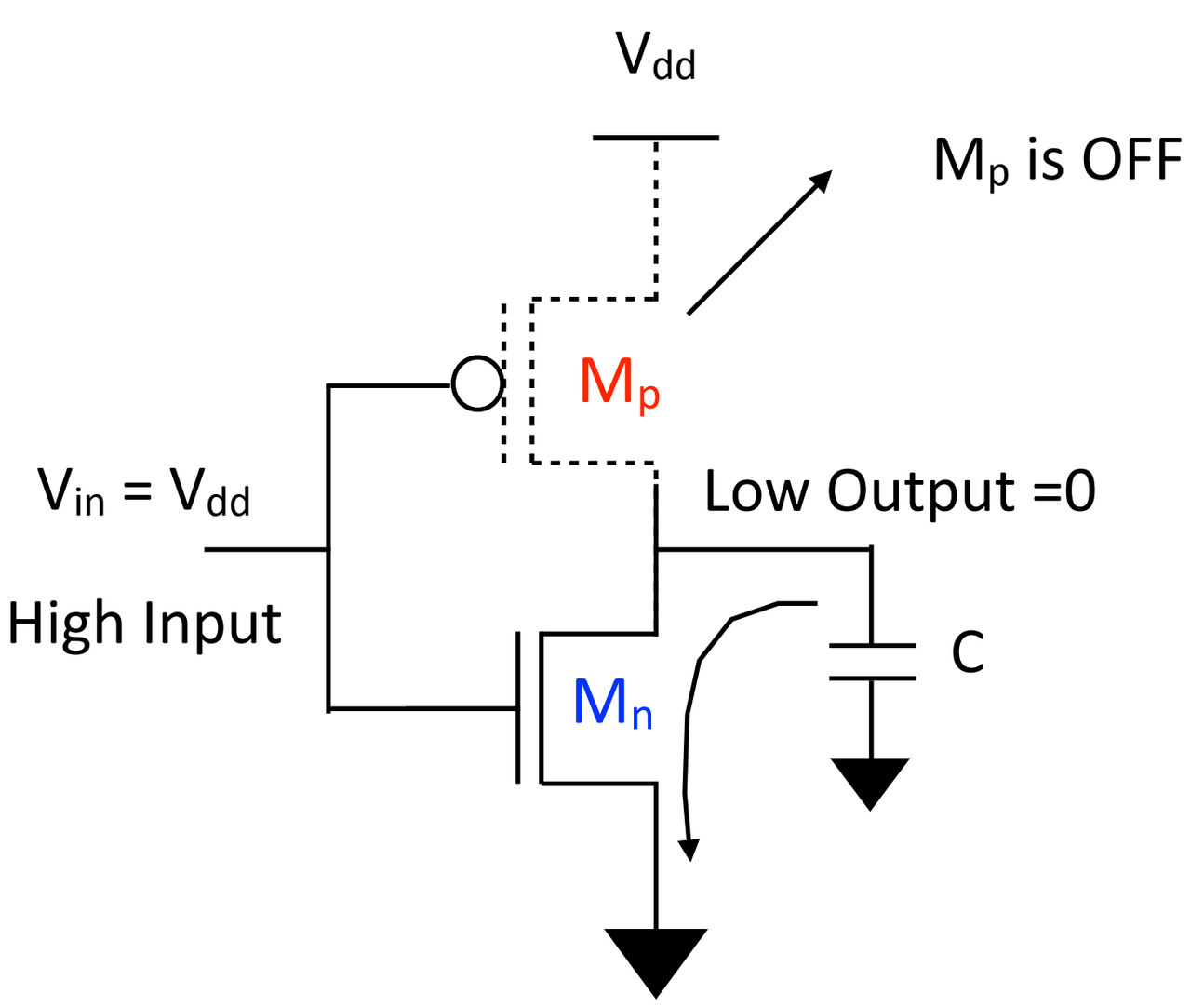
$$\tau = 0.69 R_{eq,p} C$$

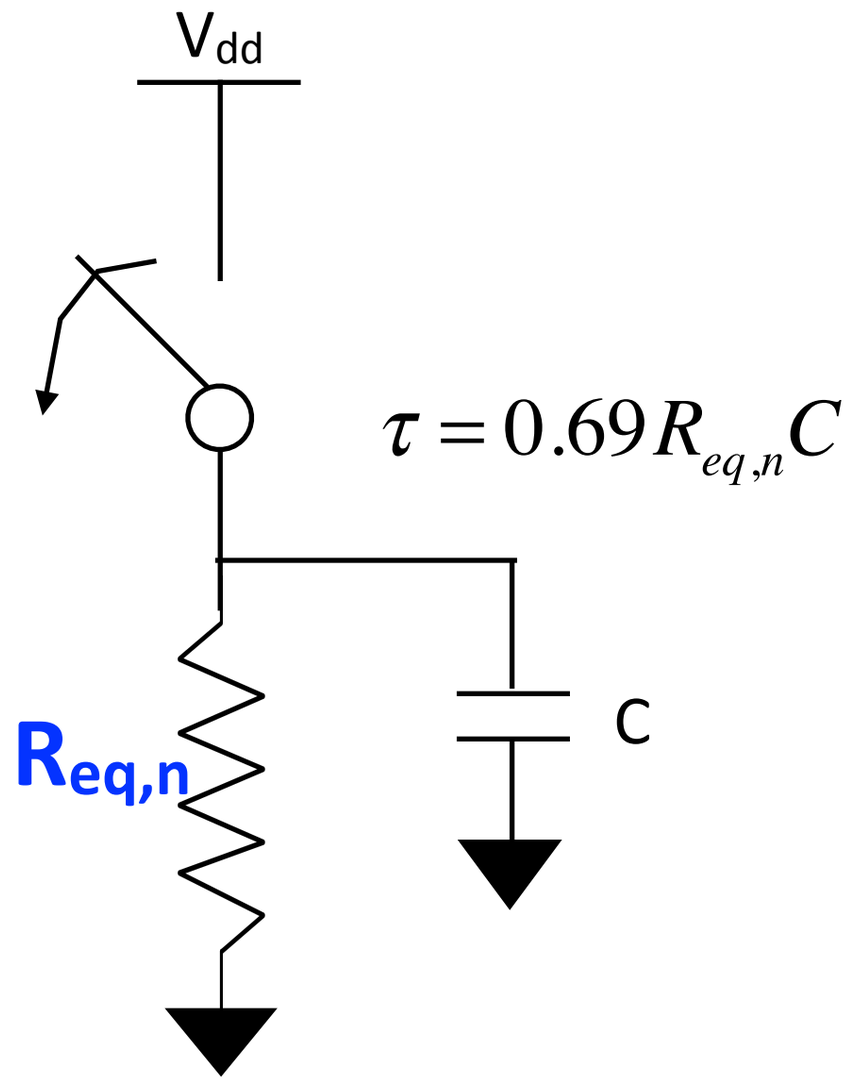
Input: High —> Low

Output: Low —> High

$$t_{pLH} = 0.69 R_{eq,p} C$$

High to low transition time in inverter



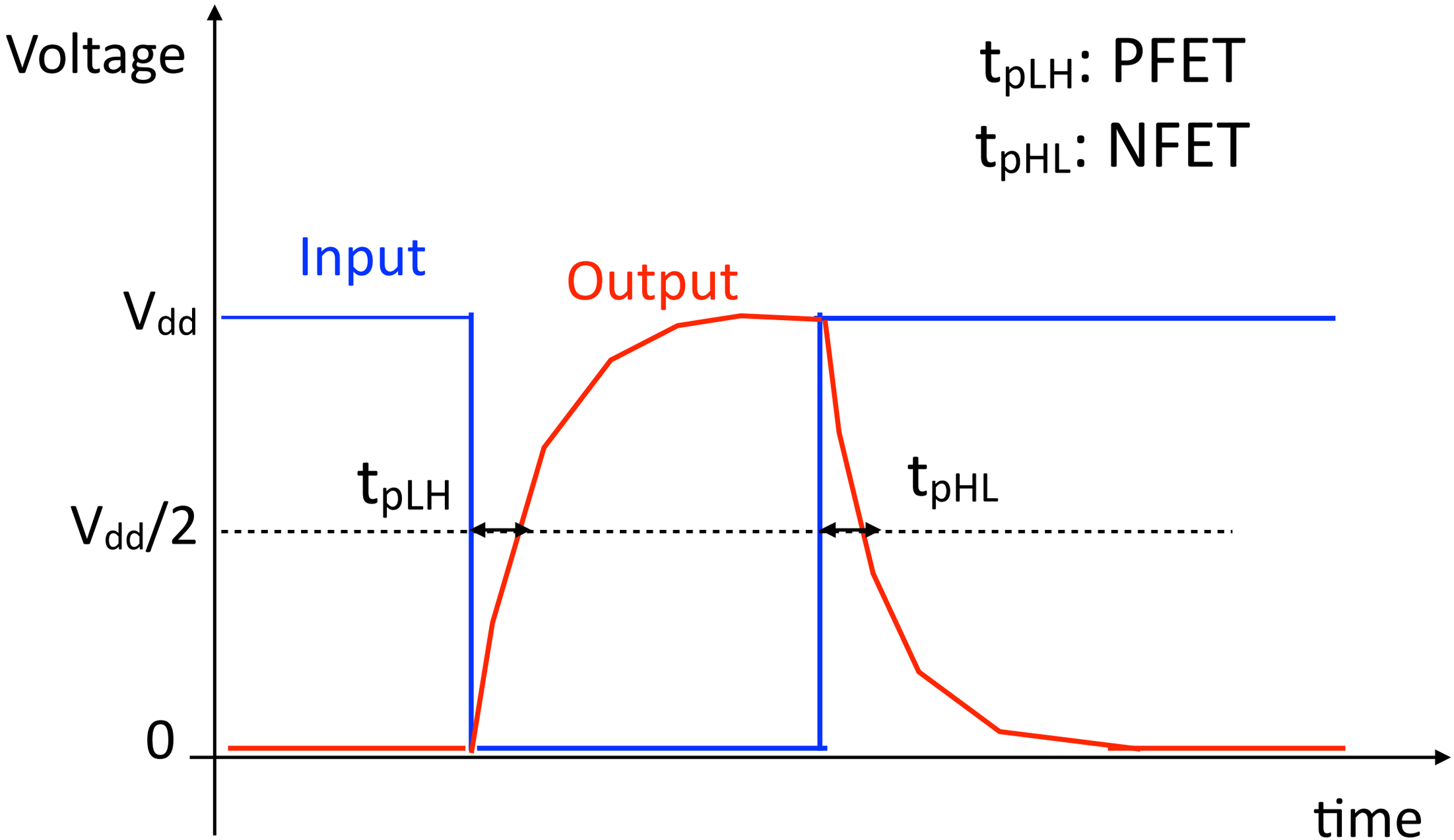


Input: Low —> High

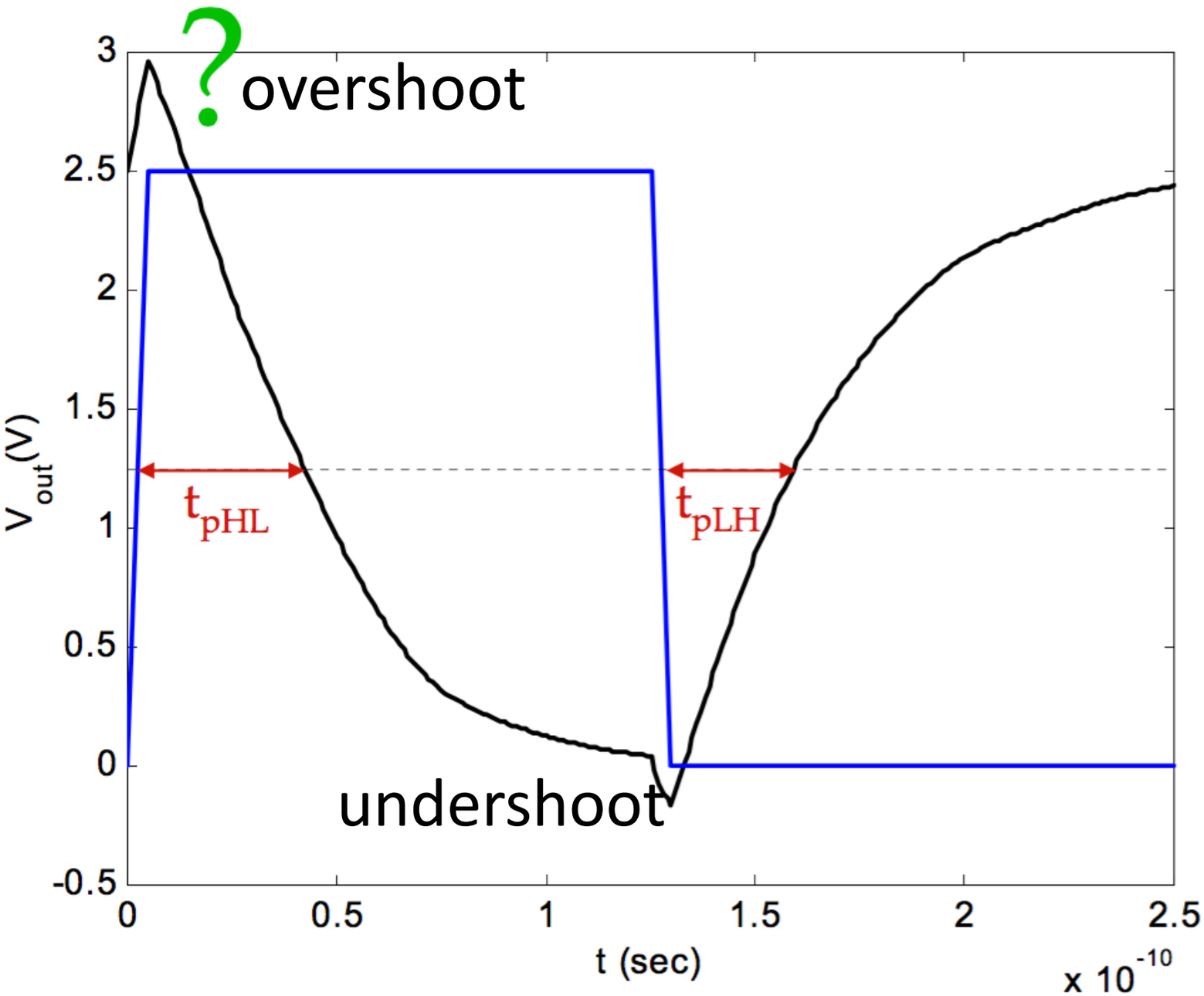
Output: High —> Low

$$t_{pHL} = 0.69 R_{eq,n} C$$

Inverter transient response



Inverter transient response from HSPICE



Propagation delay

$$t_p = 0.5\left(t_{pLH} + t_{pHL}\right)$$

$$= 0.69C_L \frac{\left(R_{eq,n} + R_{eq,p}\right)}{2}$$

Rise time:

10% to 90% of V_{dd}

$$t_r = ln(9)R_{eq,p}C_L$$

Fall time:

90% to 10% of V_{dd}

$$t_f = ln(9)R_{eq,n}C_L$$

Inverter transient response from HSPICE

Propagation delay

$$t_p = 0.5\left(t_{pLH} + t_{pHL}\right)$$

$$= 0.69 C_L \frac{\left(R_{eq,n} + R_{eq,p}\right)}{2}$$

Rise time:

10% to 90% of V_{dd}

$t_r = ln(9) R_{eq,p} C_L$

Fall time:

90% to 10% of V_{dd}

$t_f = ln(9) R_{eq,n} C_L$

Next class we will study more details of inverter sizing based on desired fall time, rise time …

Next class on 09/28/2015

- Recap from 09/21/2015
    - MOSFET capacitances
    - Inverter DC characteristics
        - Definitions of rise time, fall time, propagation delay
- Calculation of inverter delay and sizing
- Power dissipation of inverter