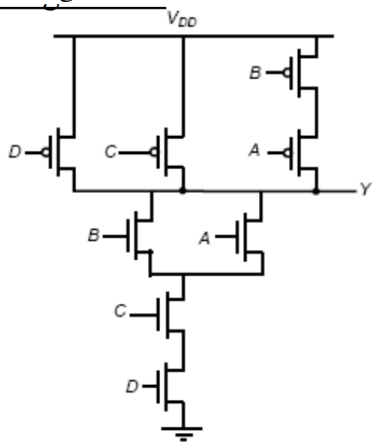
ECE 6473
Homework # 3
Date Assigned: October 9th, 2015
Due Date: October 19th, 2015 @ 11.59 PM

Grading:
Problem 1: 30 points
Problem 2: 40 points
Problem 3: 30 points

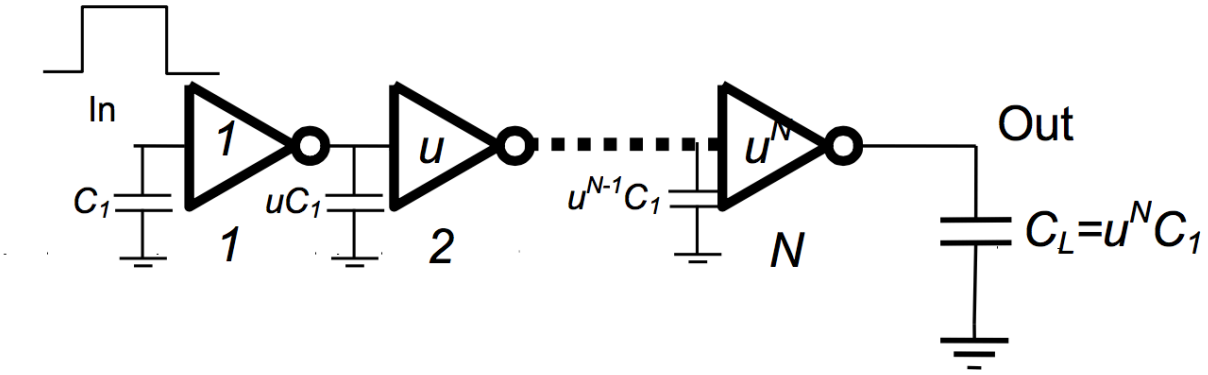
Problem 1: Consider the following circuit



a. What is the logic function implemented by the CMOS transistor network?
b. Size the NMOS and PMOS devices so that the output resistance is the same as that of an inverter with an NMOS $W/L = 1$ and PMOS $W/L = 2$.
c. Consider a step input and only **one input is allowed to make a transition** at one time. What are the input patterns that give the worst case t_{pHL} and t_{pLH}. State clearly what are the initial input patterns and what are the final patters (mention which input has to make a transition) in order to achieve this maximum propagation delay. Consider the effect of the capacitances at the internal nodes.

Problem 2: Sizing Optimization for Delay, Energy, and Energy-Delay product

Consider the following inverter chain.



Assume, the reference delay as: $\tau_r = 0.69R_1C_1$ and reference energy as: $E_r = C_1V_{DD}^2$ where, R_1 is the resistance of the first stage (the ratio α is chosen such that PMOS and NMOS have same resistance). The reference energy delay product is $EDP_{ref} = E_r\tau_r$. Neglect C_{FET} in the entire analysis.

(a) Derive an expression for the total energy dissipated in the chain for one complete swing of the input (i.e. low-to-high + high-to-low) (assume u> 1) in terms of 'u', E_r, C_L, and C_1.

(b) Derive the expression for normalized Energy-Delay Product (EDP_{chain}/EDP_{ref}) of the chain in terms of 'u', E_r, C_L, and C1. Find out the relation that provides the optimal 'u' for minimum normalized EDP.

(c) Now consider $C_L = 256C_1$. First, find out the optimal 'u' that provides minimum normalized EDP. You can vary 'u' from 2 to 10 in very fine steps (< 0.001) and find out when the optimal relation obtained from (b) is satisfied. How does it differ from the optimal 'u' for minimum delay for same C_L?

Problem 3: Find C_1/C and C_2/C that results in optimal delay.

The logic chain in the following figure is constructed with r = 2.5. Determine the optimum input capacitance (with respect to C) for each stage to achieve a minimum delay through the 'red' colored path using the Logical Effort method. Assume the NAND3 gate in the branch point is a unit-size NAND3 gate i.e. its pull-up and pull-down resistances are same as that of a reference inverter.