

ECE 6473  
Lecture 3  
Date: 09/28/2015

Shaloo Rakheja  
Assistant Professor  
Electrical and Computer Engineering, NYU

# Reading

- Power point and hand-written lecture notes posted on [newclasses.nyu.edu](http://newclasses.nyu.edu)
- Chapter 5 and sections 6.1, 6.2.1 from Digital Integrated Circuits by Jan M. Rabaey et al.

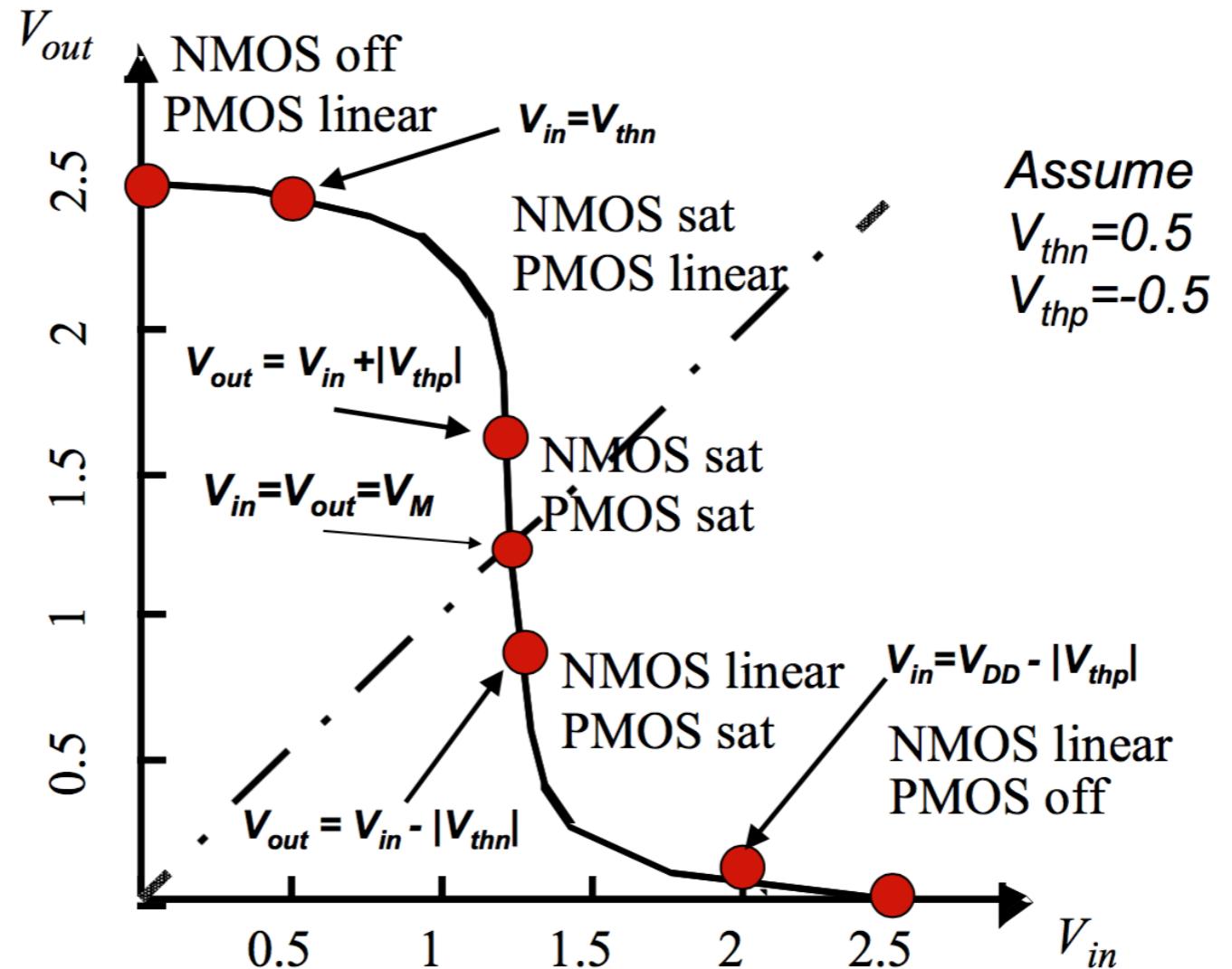
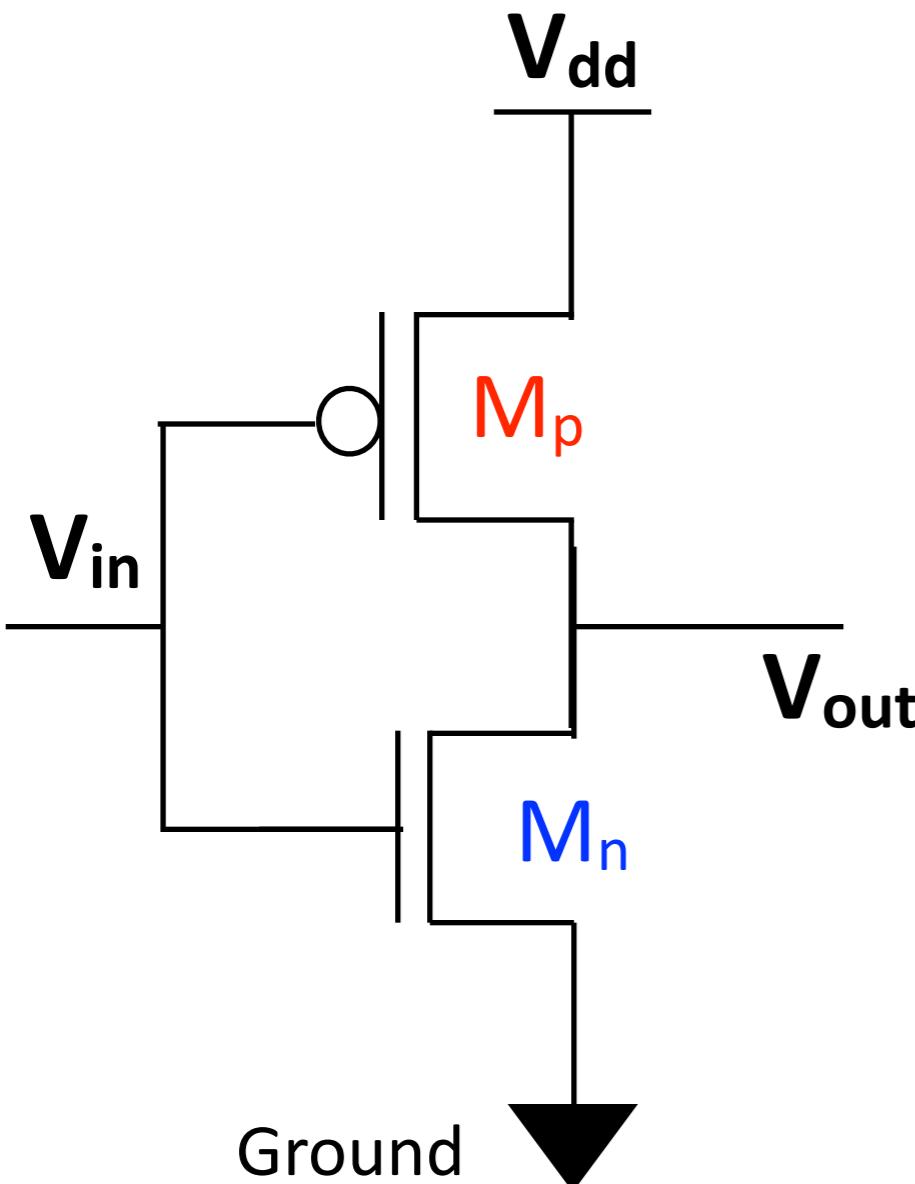
# Homework

- Due on Oct. 5th.
- Work on setting up Cadence. We will use FreePDK45 for the class assignments and the project :)

# Inverter analysis

- Recap from 09/21/2015
  - Voltage transfer characteristics
  - Switching characteristics
- Inverter capacitances and self loading
- Inverter sizing for driving a chain of inverters
- Power dissipation
- Introduction to CMOS logic gates

# Inverter Voltage Characteristics



**VTC tells us  $V_{out}$  versus  $V_{in}$**

# Switching threshold ( $V_M$ ) computation

**At  $V_{in} = V_{out} = V_M$ , both NFET and PFET are saturated.**

$$V_M = \frac{V_{dd} - |V_{Tp}| + \sqrt{\frac{\beta_n}{\beta_p}} V_{Tn}}{1 + \sqrt{\frac{\beta_n}{\beta_p}}} \quad \left. \right\}$$

Recall:

$$\beta_n = (\mu_n C_{ox})(W/L)_n$$

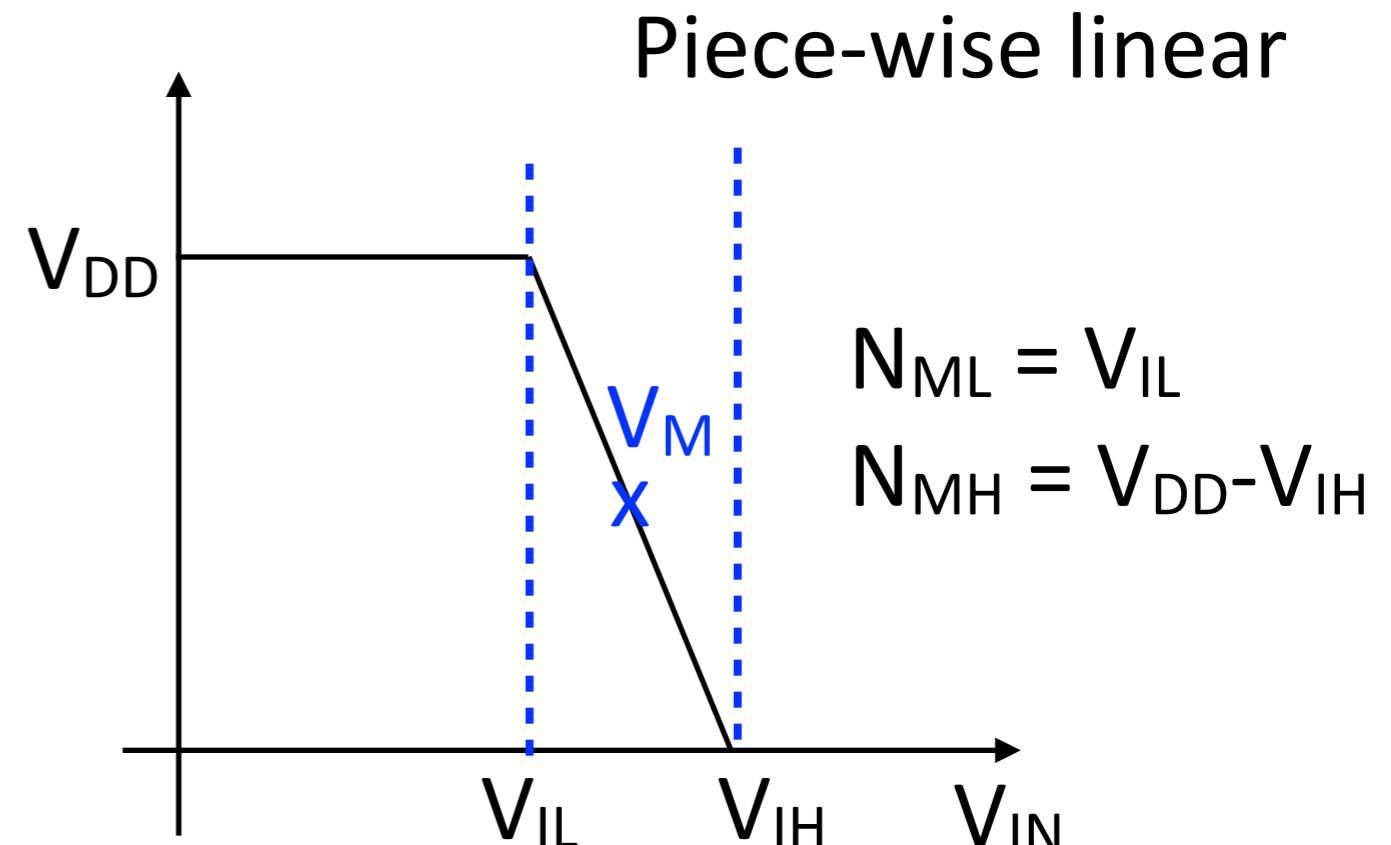
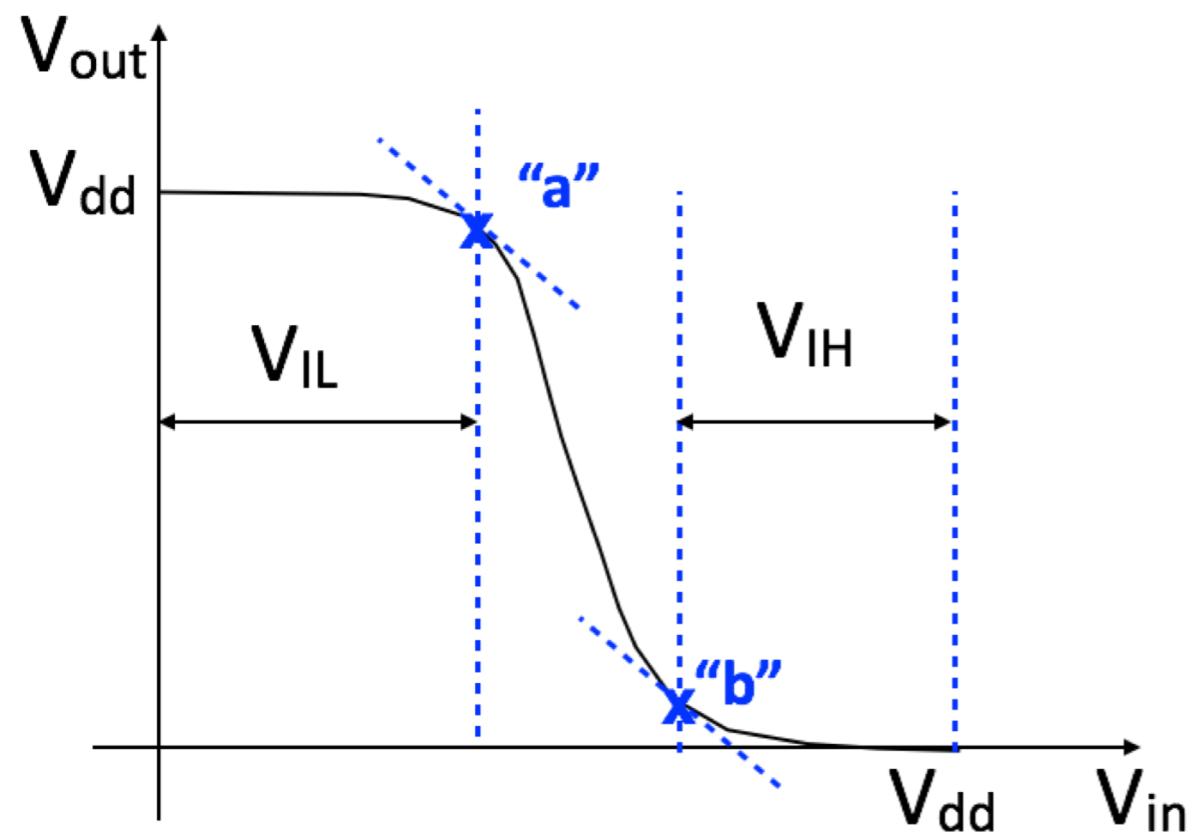
$$\beta_p = (\mu_h C_{ox})(W/L)_p$$

$$For \ V_M = rV_{DD} \Rightarrow \sqrt{\frac{\beta_n}{\beta_p}} = \frac{(1-r)V_{DD} - |V_{thp}|}{(rV_{DD} - V_{thn})}$$

To achieve  $V_M = 0.5V_{DD}$  with  $|V_{thp}| = V_{thn} \Rightarrow \beta_n / \beta_p = 1$

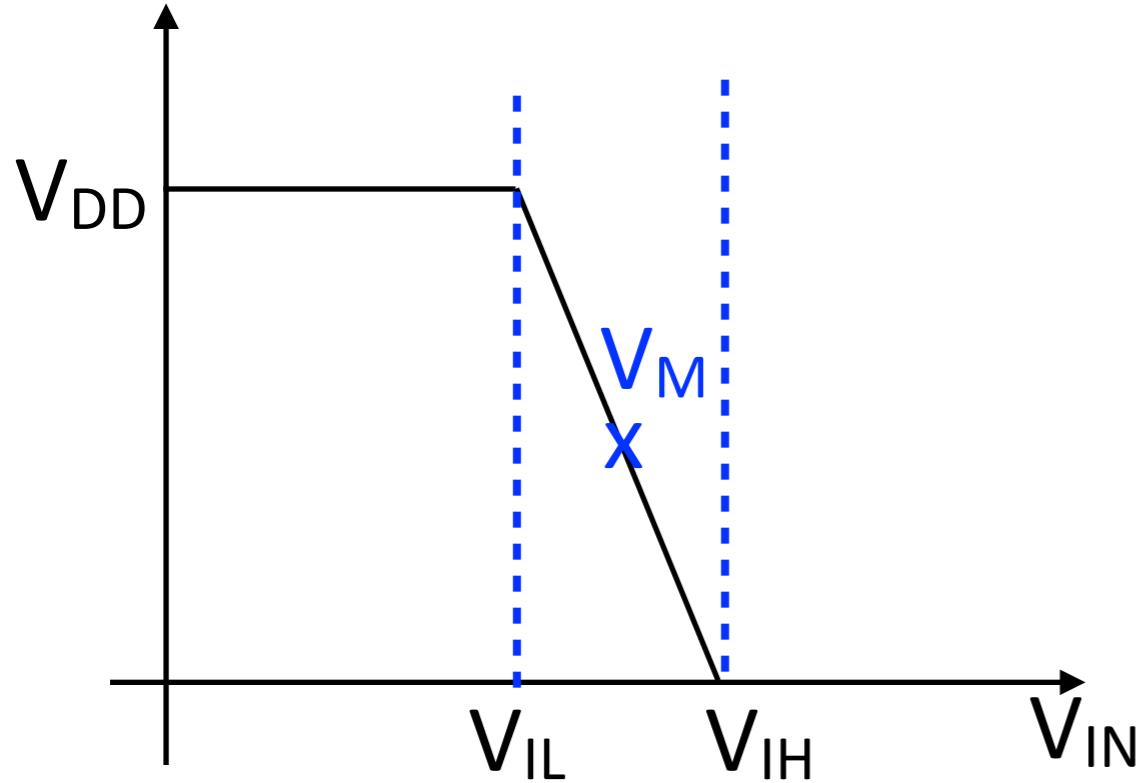
Normally,  $\mu_n / \mu_p = 2$ ,  $W_p / L_p = 2(W_n / L_n)$  (assuming,  $C_{oxp} = C_{oxn}$ )

# Noise margin



- Noise margins signify robustness to noise.
- An input signal within  $(0, V_{IL})$  voltage levels will always be considered as logic “0” or LOW.
- An input signal within  $(V_{IH}, V_{DD})$  levels will always be considered as logic “1” or HIGH.

# Noise margin



$$N_{ML} = V_{IL}$$

$$N_{MH} = V_{DD} - V_{IH}$$

- In the region around  $V_M$ , both NFET and PFET are in saturation.
- Note: for this analysis you cannot neglect channel-length modulation.

$$V_{IH} - V_{IL} = -\left(\frac{V_{OH} - V_{OL}}{g}\right) = -\frac{V_{DD}}{g}$$

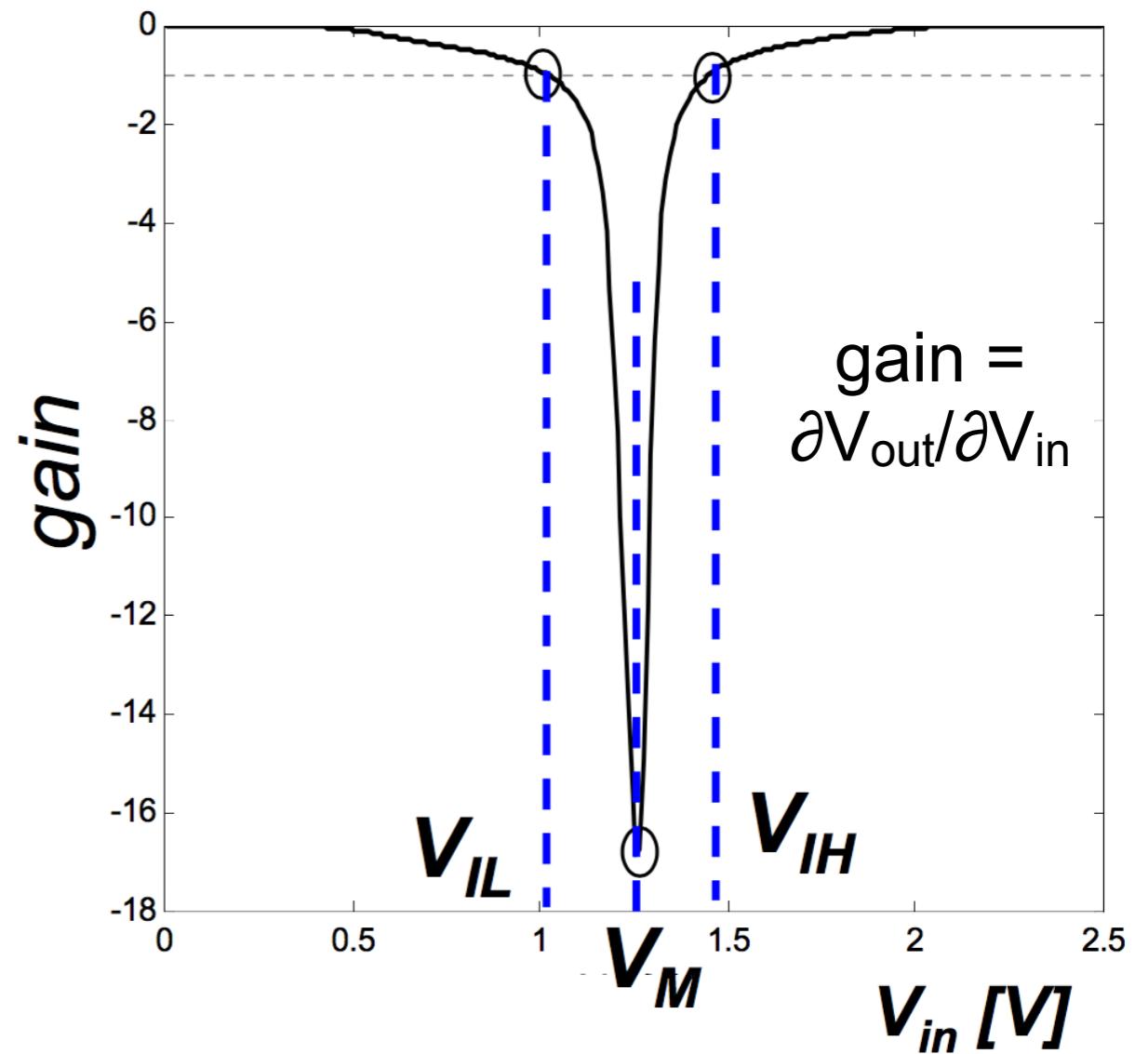
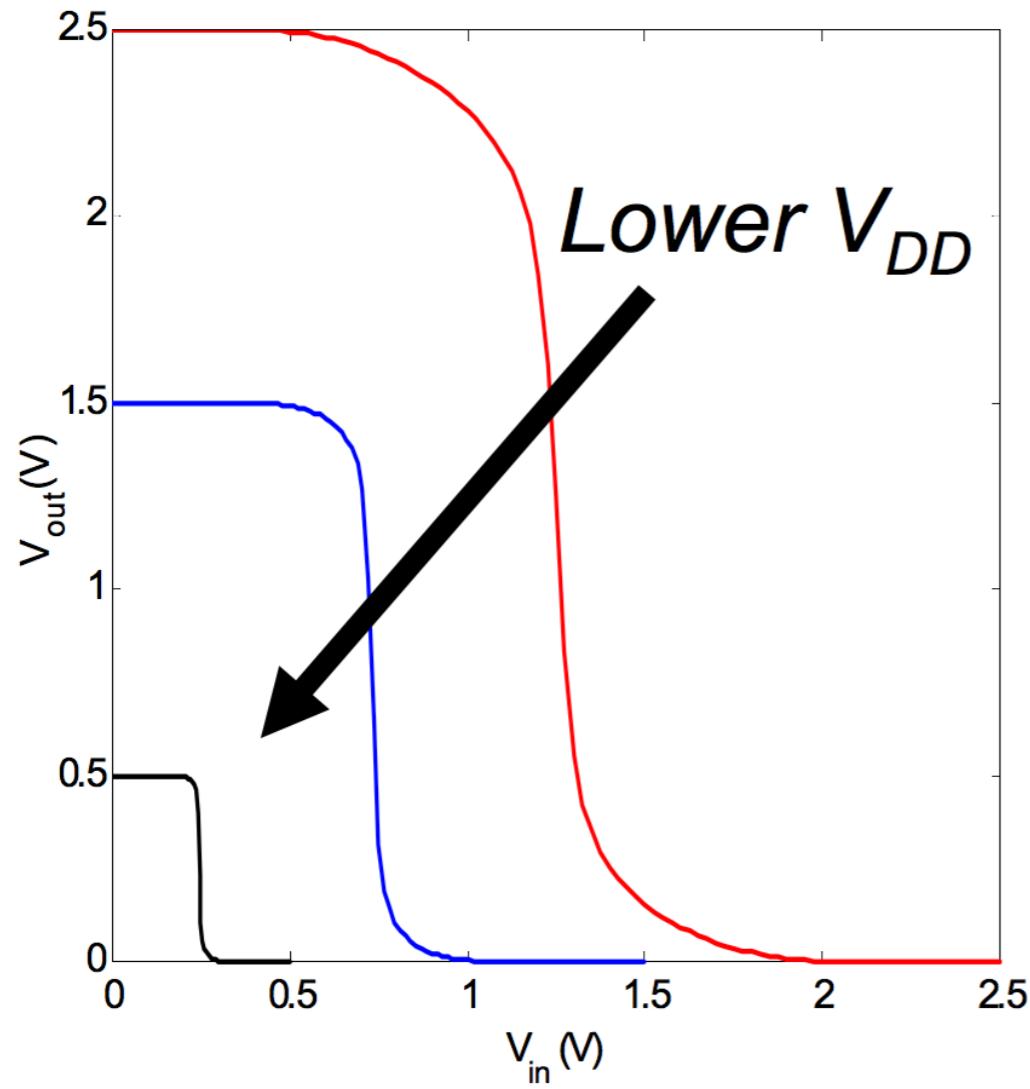
$$V_{IH} = V_M - \frac{V_M}{g}$$

$$V_{IL} = V_M + \frac{V_{DD} - V_M}{g}$$

$$g = \frac{dV_{out}}{dV_{in}} = -\frac{2(1 + \sqrt{\beta_p / \beta_n})}{(V_M - V_{Tn})(|\lambda_n| - |\lambda_p|)}$$

$g$ : inverter gain in the transition between  $V_{IL}$  and  $V_{IH}$ .

# Effect of Supply voltage on VTC



- Key is to bring  $V_{IL}$  and  $V_{IH}$  as close to  $V_M$
- Increase  $N_{ML}$  and  $N_{MH}$ .

# Can an inverter work when supply is below threshold voltage ?

For :  $V_{DD} < V_{th}$

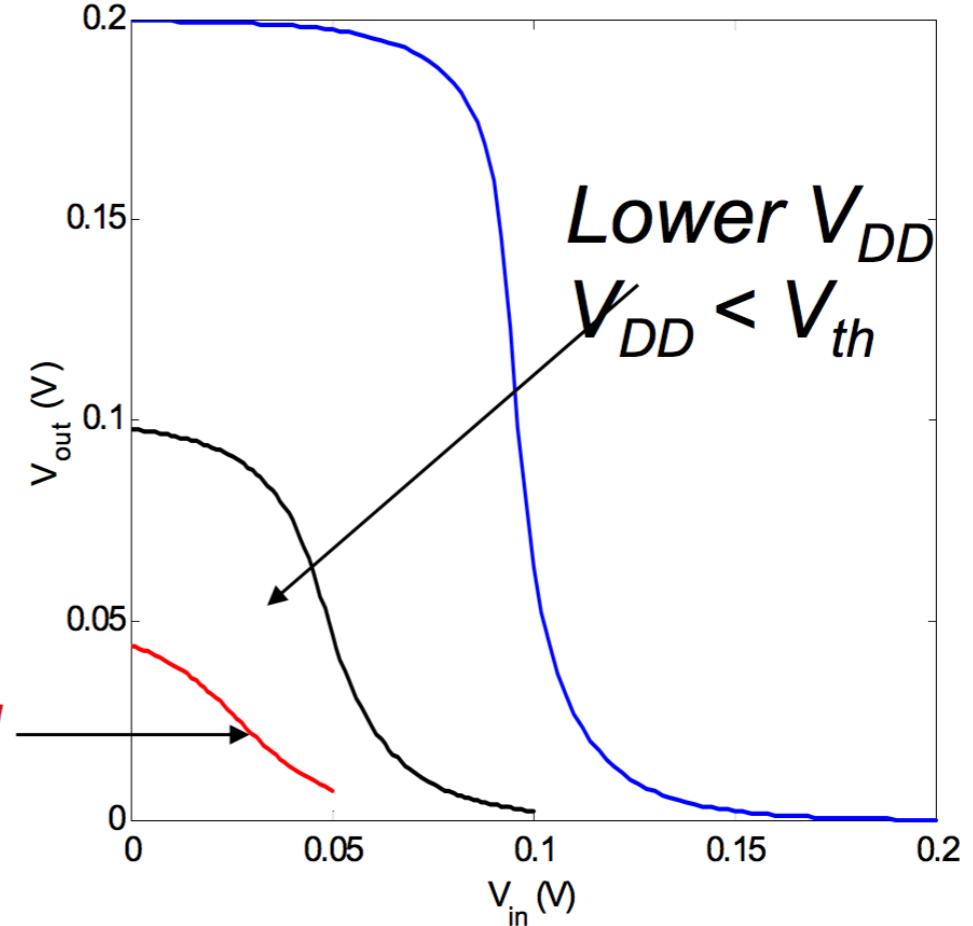
VTC is obtained from :

$$I_{subthP} = I_{subthN}$$

$$\Rightarrow I_{0P} e^{\frac{V_{DD}-V_{in}-|V_{thp}|}{n_p kT/q}} \left( 1 - e^{\frac{q(V_{DD}-V_{out})}{kT}} \right)$$

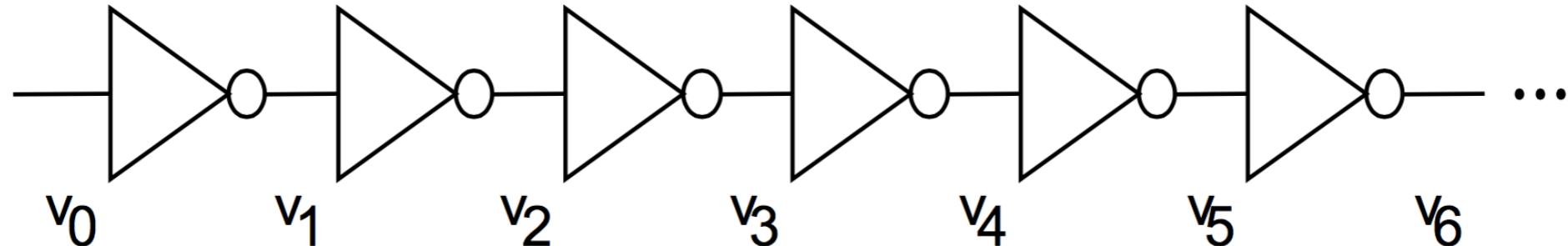
$$= I_{0N} e^{\frac{V_{in}-V_{thn}}{n_n kT/q}} \left( 1 - e^{\frac{qV_{out}}{kT}} \right) \quad \text{gain} = -1$$

“subthreshold inverter”



**Minimum possible  $V_{DD}$  for inverter operation:**  
 **$V_{DD}$  for maximum gain in VTC (@switching th.) = -1**

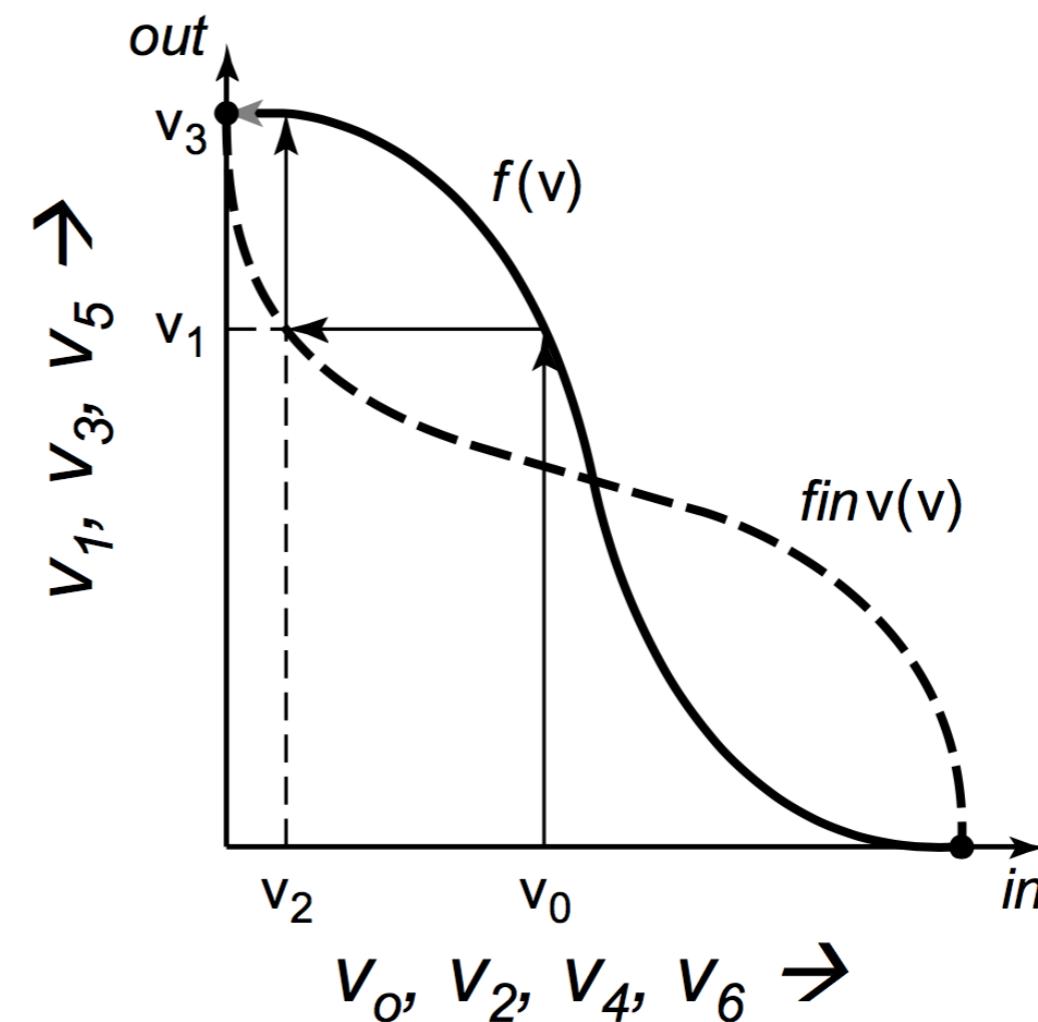
# Regenerative property of inverter



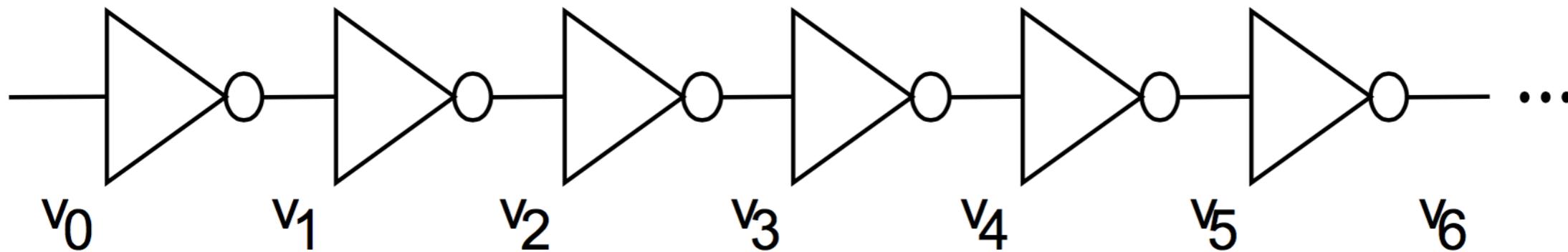
A chain of inverters

Assume  $V_M = V_{DD}/2$

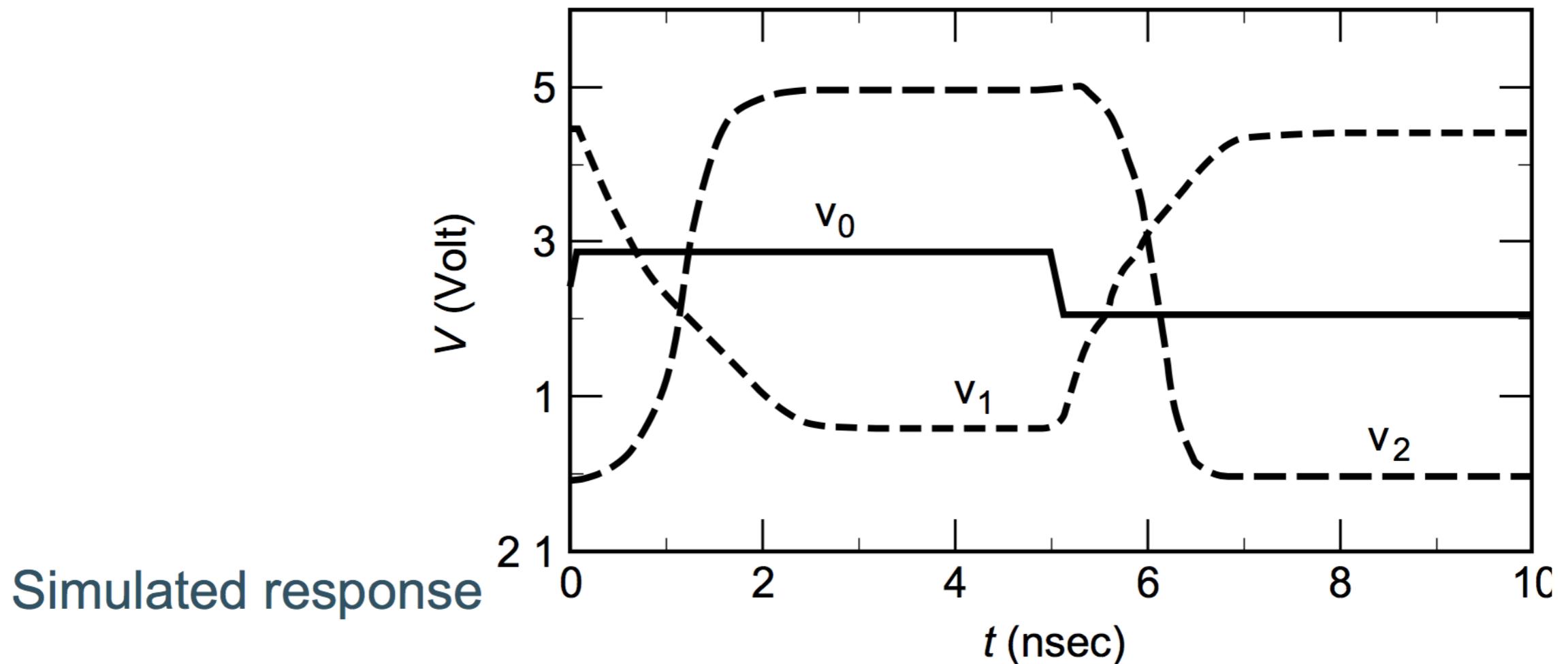
$v_0$	$v_6$
$V_{DD}/2 - \epsilon$	$V_{OL}$
$V_{DD}/2 + \epsilon$	$V_{OH}$



# Regenerative property of inverter



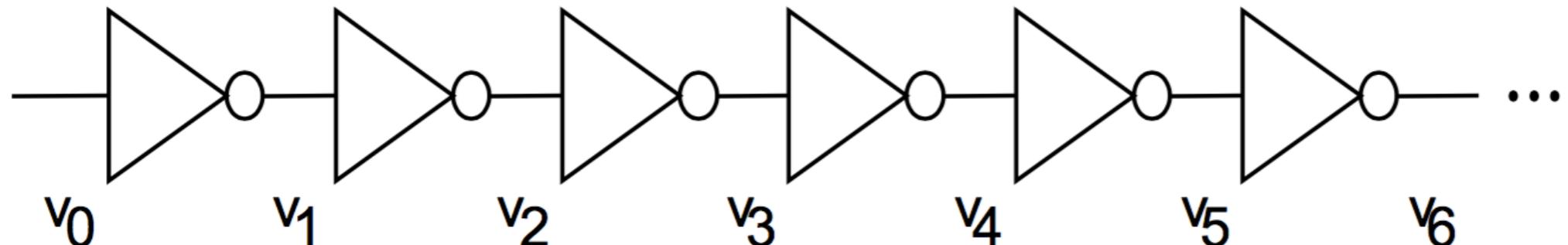
A chain of inverters



# Non-regenerative ?

When will the inverter chain be non-regenerative?

# Non-regenerative ?

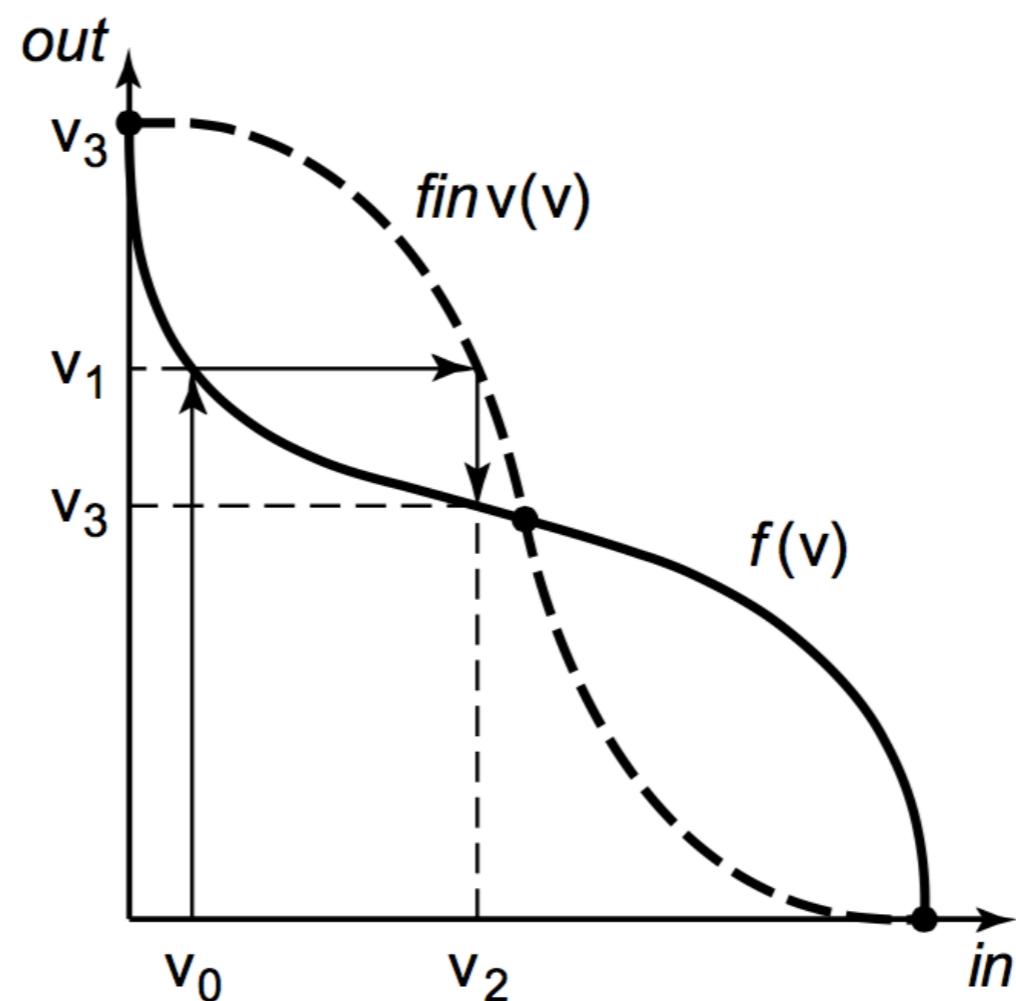


A chain of inverters

Assume  $V_M = V_{DD}/2$

For a small noise in  $v_0$ ,  
 $v_6$  approaches an  
intermediate level

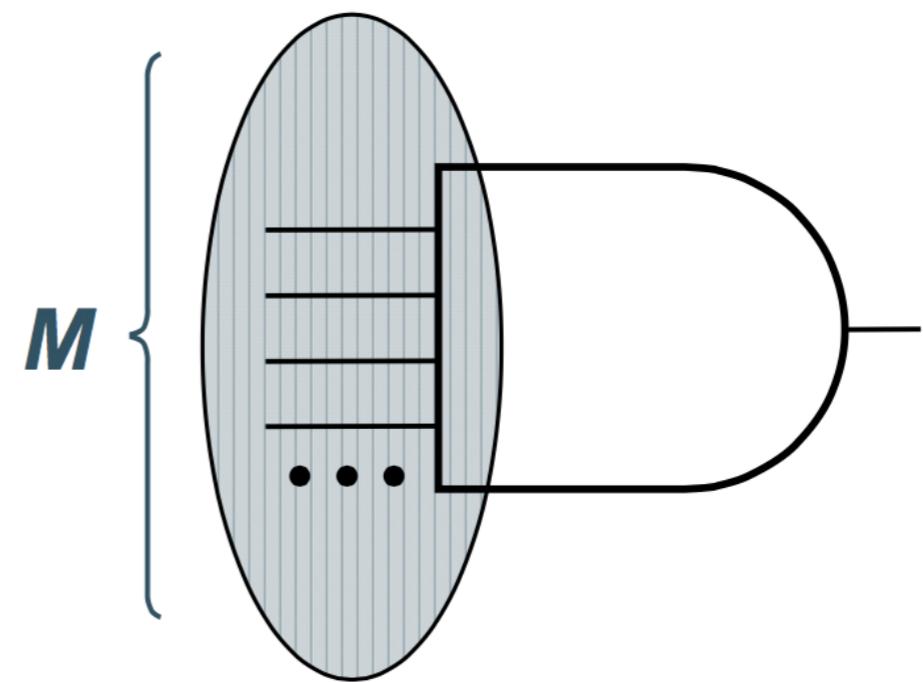
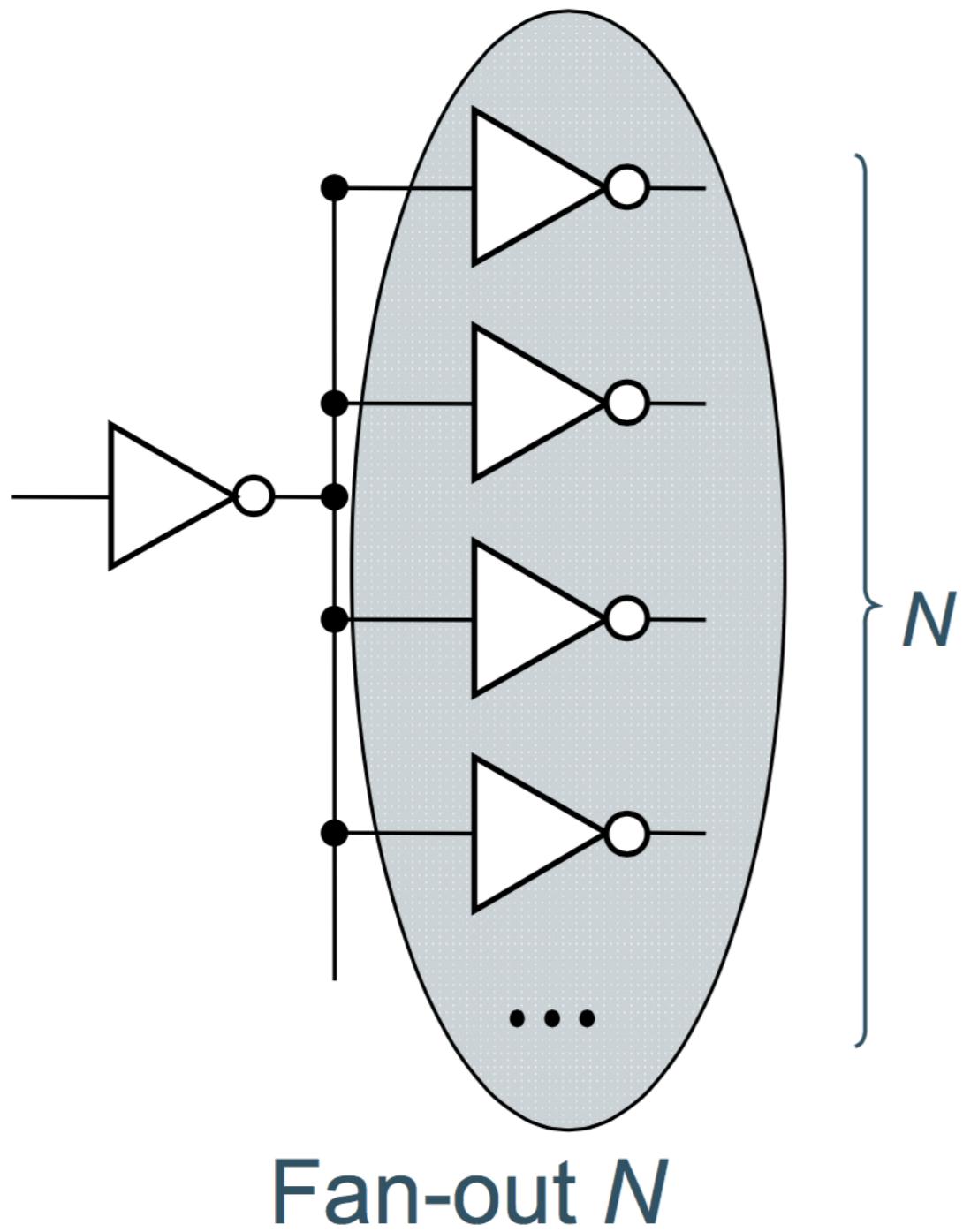
Convince yourself  
Non-regenerative !



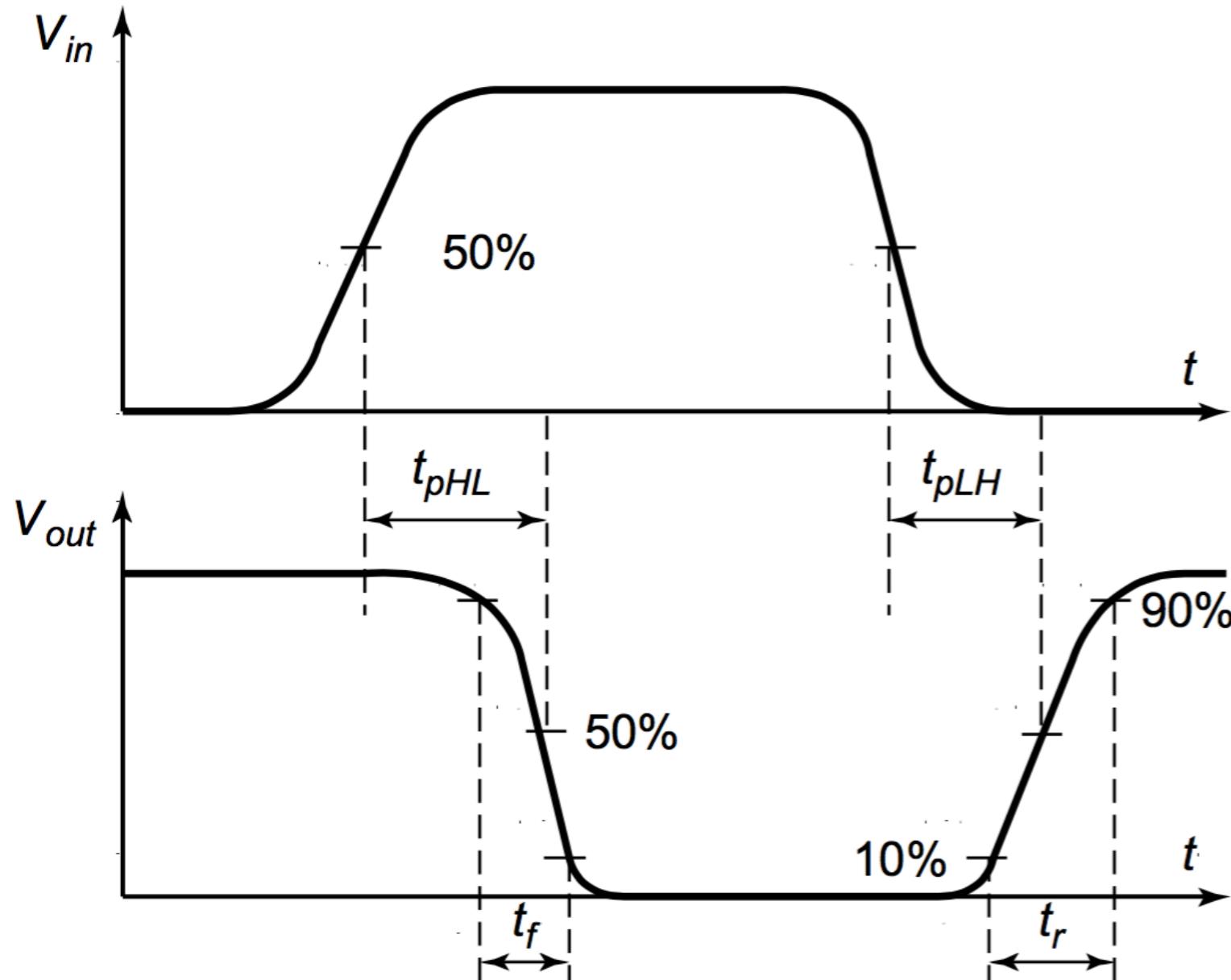
# CMOS inverter

## Switching characteristics

# Fan-in and Fan-out



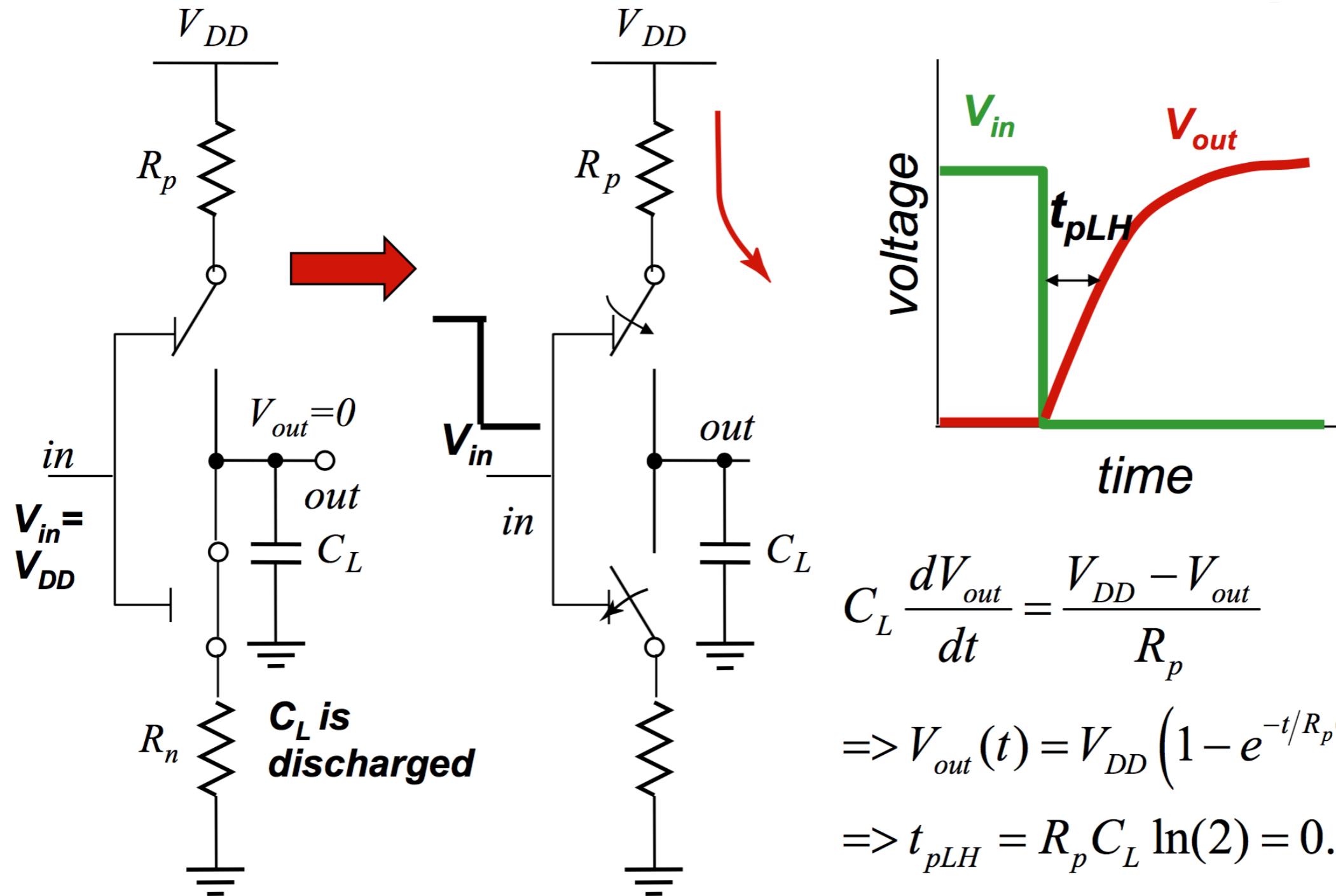
# Delay definitions



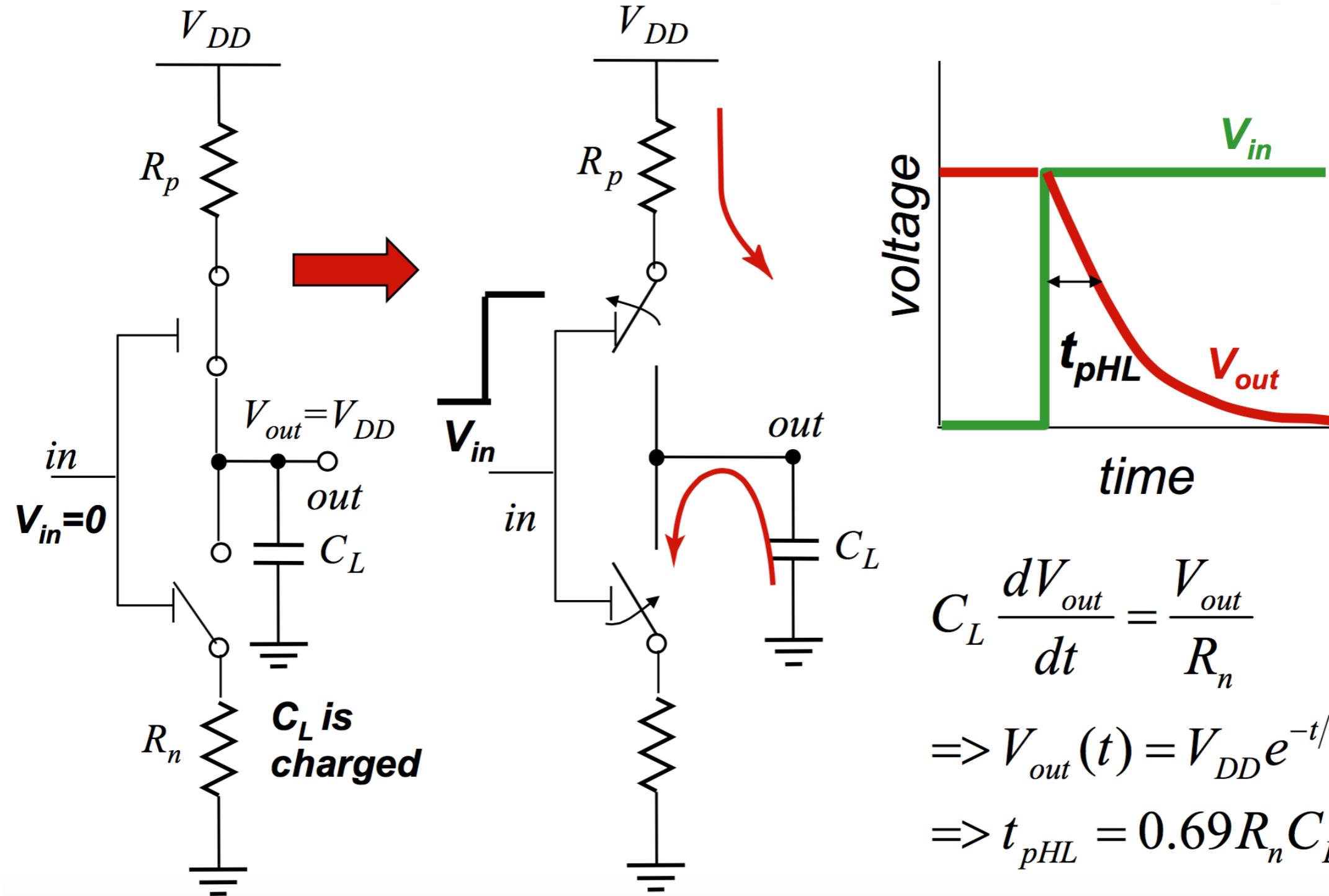
## Definitions:

- $t_{pHL}$ : high-to-low delay
- $t_{pLH}$ : low-to-high delay
- $t_r$ : 10%-90% rise time
- $t_f$ : 90% to 10% fall time

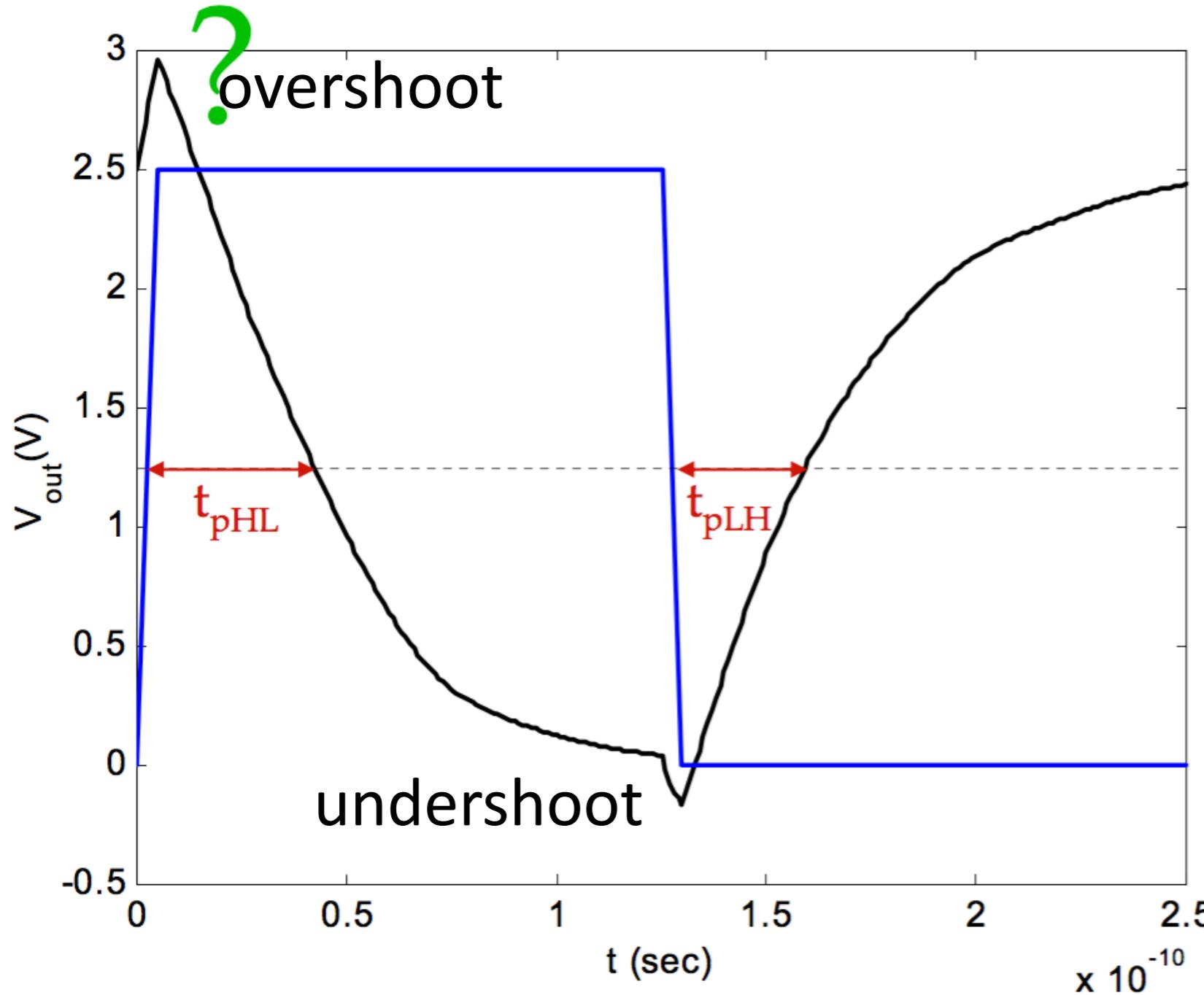
# First order transient response: Low to High



# First order transient response: High to Low



# Inverter transient response from HSPICE



Propagation delay

$$t_p = 0.5(t_{pLH} + t_{pHL})$$
$$= 0.69C_L \frac{(R_n + R_p)}{2}$$

**Rise time:**

10% to 90% of  $V_{dd}$

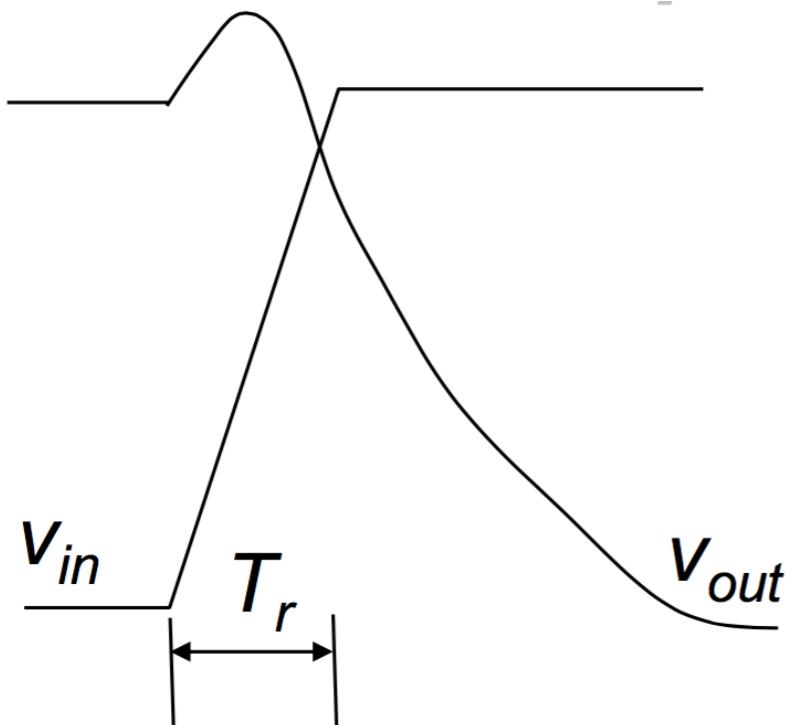
$$t_r = \ln(9)R_pC_L$$

**Fall time:**

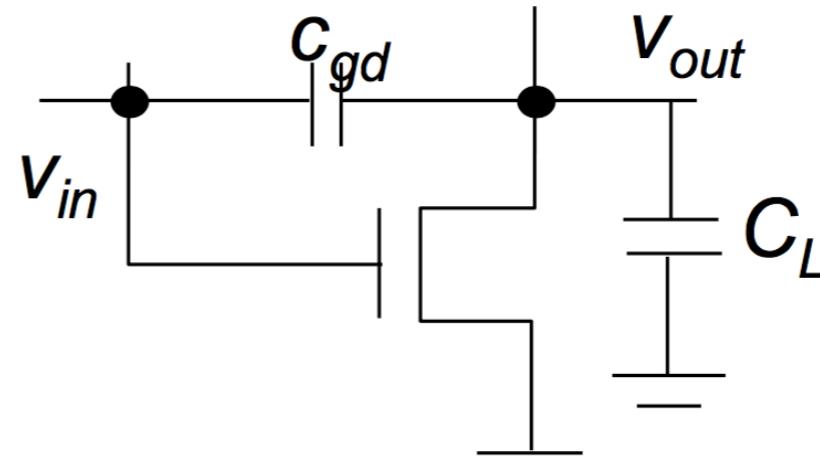
90% to 10% of  $V_{dd}$

$$t_f = \ln(9)R_nC_L$$

# Overshoot and undershoot



**Direct coupling of the input transition to the output through overlap capacitances**



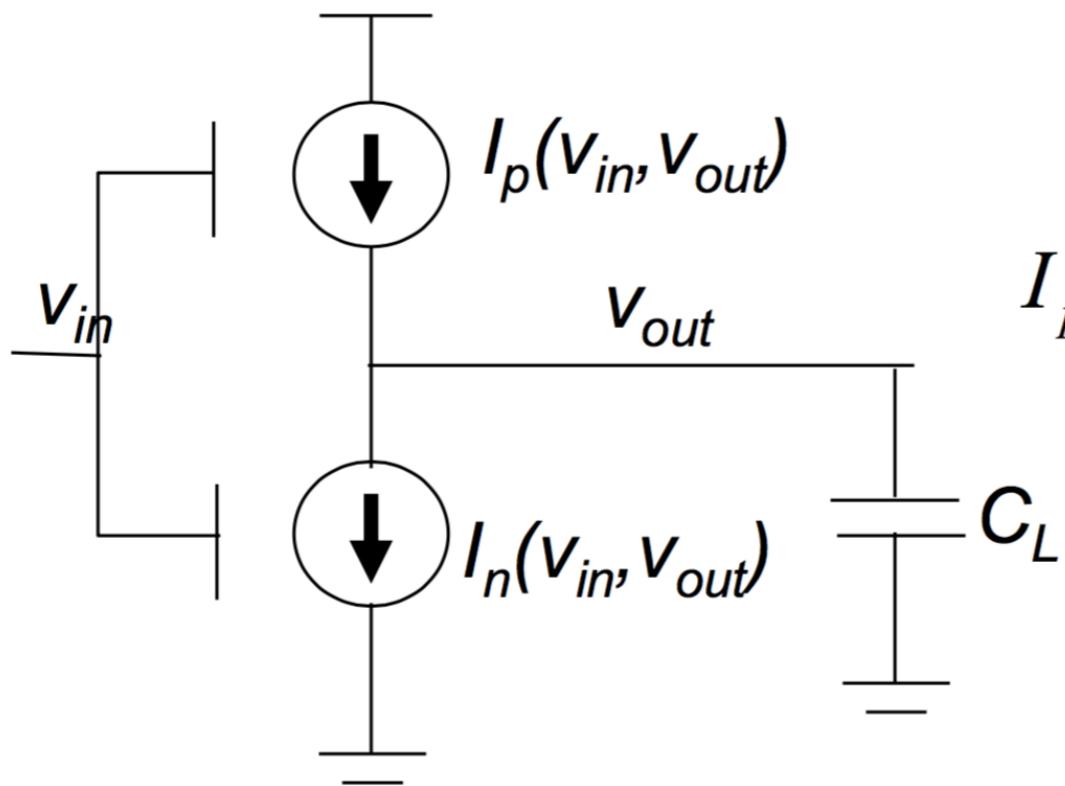
$$C_{gd} \frac{d(v_{out} - v_{in})}{dt} + C_L \frac{d(v_{out})}{dt} = 0$$

$$\Rightarrow \frac{dv_{out}}{dt} = \frac{C_{gd}}{C_{gd} + C_L} \frac{dv_{in}}{dt} = \frac{C_{gd}}{C_{gd} + C_L} \frac{V_{DD}}{T_r}$$

$$\Rightarrow \underbrace{v_{out}(t) - V_{DD}}_{\text{overshoot}} = \left( \frac{C_{gd}}{C_{gd} + C_L} \frac{V_{DD}}{T_r} \right) t$$

**Larger overlap capacitances and faster input transition increases the overshoot/undershoot**

# Generalized delay calculation



$$I_p(v_{in}, v_{out}) - I_n(v_{in}, v_{out}) = \frac{d(C_L v_{out})}{dt}$$

*Given:*

- (1)  $v_{in}$ : Input waveform, (e.g. step function, or with a finite rise/fall time)
- (2) Capacitance (constant or voltage dependence)
- (3) MOSFET parameters (e.g,  $\beta$ ,  $V_{DD}$ ,  $V_{th}$ , etc.)

*Find out: Low-to-high, High-to-low and propagation delay, rise time and fall time etc.*

# A simple case for manual analysis

- (1)  **$V_{in}$  a step function: only NFET (for H-L) or PFET (L-H) is active, the other one is zero.**
- (2) **Devices are in satn. (neglect ch. len. mod.) for region of interest**
  - **$v_{out} = V_{DD}$  to  $V_{DD}/2$  for H-L – NFET**
  - **$v_{out} = 0$  to  $V_{DD}/2$  for L-H - PFET**

$$High-to-Low: I_{satn} = -C_L \frac{dv_{out}}{dt} \Rightarrow -\frac{C_L}{I_{satn}} \int_{V_{DD}}^{0.5V_{DD}} dv_{out} = \int_0^{t_{pHL}} dt$$

$$Low-to-High: I_{satp} = C_L \frac{dv_{out}}{dt} \Rightarrow \frac{C_L}{I_{satp}} \int_0^{0.5V_{DD}} dv_{out} = \int_0^{t_{pLH}} dt$$

# A simple case for manual analysis

High-to-low delay  
(NFET resistance)

$$t_{pHL} = 0.69 R_n C_L$$

$$R_n = \frac{3V_{DD}}{4I_{DSATn}} = \frac{3}{2\beta_n (V_{DD} - V_{Tn})^2}$$

$$t_{pHL} = \frac{C_L V_{DD}}{\beta_n (V_{DD} - V_{Tn})^2}$$

Low-to-high delay  
(PFET resistance)

$$t_{pLH} = 0.69 R_p C_L$$

$$R_p = \frac{3V_{DD}}{4I_{DSATp}} = \frac{3}{2\beta_p (V_{DD} - |V_{Tp}|)^2}$$

$$t_{pLH} = \frac{C_L V_{DD}}{\beta_p (V_{DD} - |V_{Tp}|)^2}$$

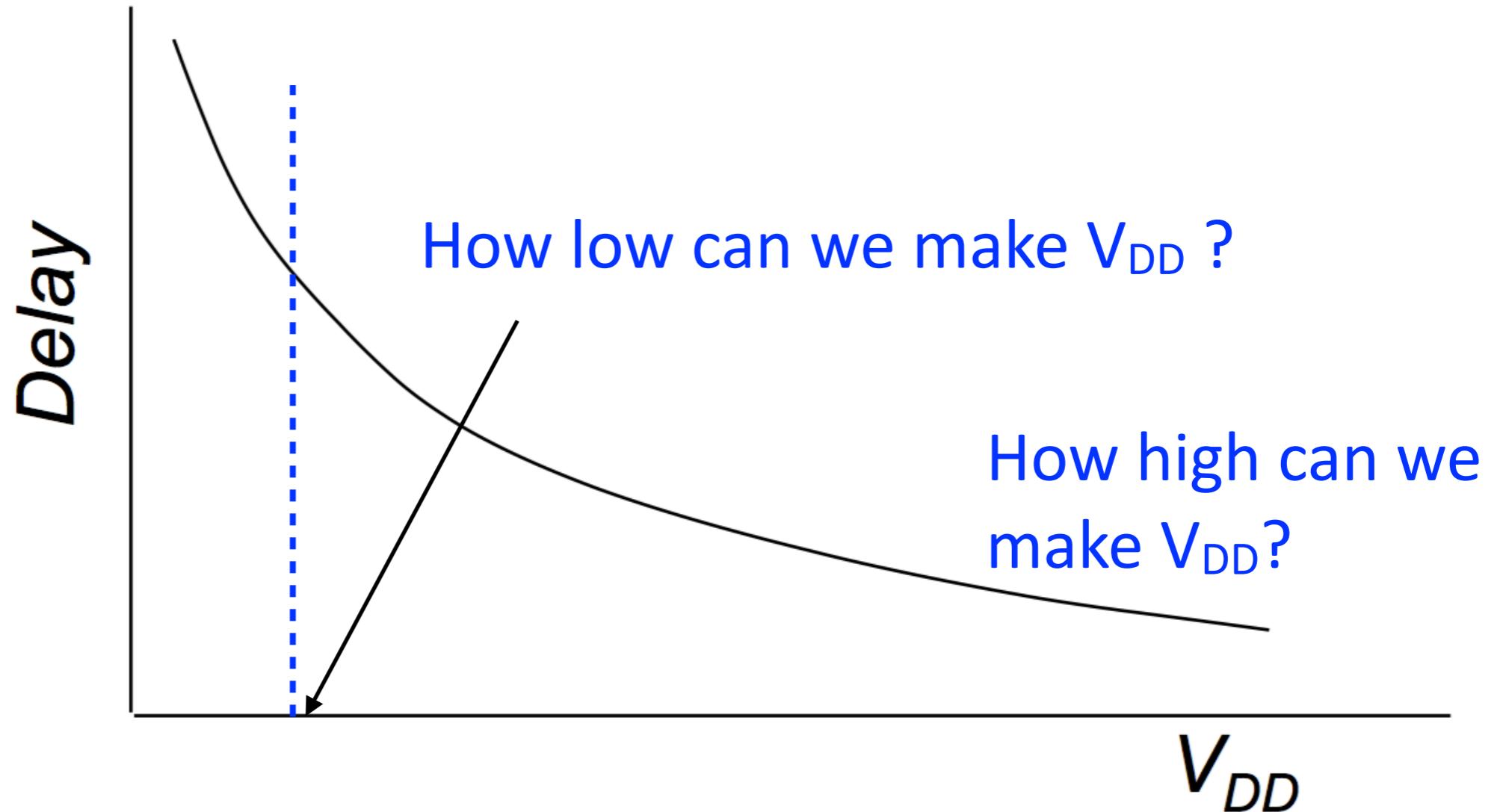
# A simple case for manual analysis

$$t_d = \frac{1}{2} (t_{pHL} + t_{pLH}) = \frac{C_L V_{DD}}{2} \left[ \frac{1}{(V_{DD} - V_{Tn})^2} + \frac{1}{(V_{DD} - |V_{Tp}|)^2} \right]$$

$$\text{For } V_{Tn} = |V_{Tp}| = V_T \Rightarrow t_d = \frac{C_L}{2V_{DD}} \left( \frac{1}{\beta_n} + \frac{1}{\beta_p} \right) \frac{1}{\left( 1 - \frac{V_T}{V_{DD}} \right)^2}$$

$$\text{For } V_{DD} \gg V_T \Rightarrow t_d = \frac{C_L}{2V_{DD}} \left( \frac{1}{\beta_n} + \frac{1}{\beta_p} \right)$$

# Delay versus $V_{DD}$ ?



- Delay reduces at a higher  $V_{DD}$

# Sizing for equal rise and fall delay

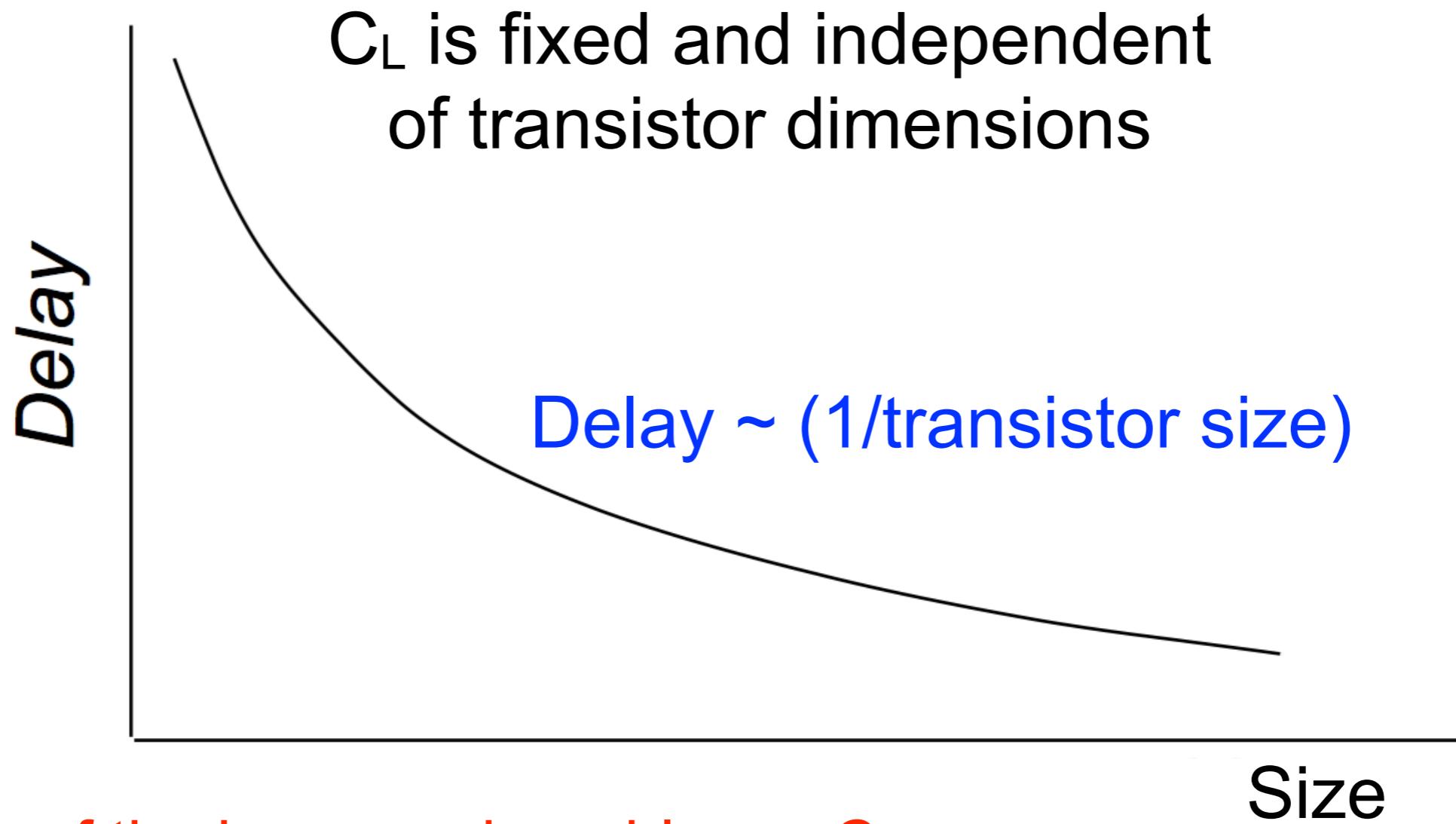
$$t_{pHL} = \frac{C_L V_{DD}}{\beta_n (V_{DD} - V_{Tn})^2} = t_{pLH} = \frac{C_L V_{DD}}{\beta_p (V_{DD} - |V_{Tp}|)^2}$$

$$\frac{W_n}{W_p} = \frac{\mu_p}{\mu_n} \frac{C_{oxp}}{C_{oxn}} \frac{L_n}{L_p} \left( \frac{V_{DD} - |V_{Tp}|}{V_{DD} - V_{Tn}} \right)^2 = \frac{\mu_p}{\mu_n} \left( \frac{V_{DD} - |V_{Tp}|}{V_{DD} - V_{Tn}} \right)^2$$

$\sim 1$

$$if |V_{Tp}| = V_{Tn} \Rightarrow \frac{W_n}{W_p} = \frac{\mu_p}{\mu_n}$$

# Delay versus size (fixed load capacitance)



In one of the homework problems,  $C_L$  is proportional to  $W$ . This plot will change in that case.

So far we have consider a constant load  $C_L$   
What about intrinsic transistor capacitances?

Intrinsic transistor capacitances depend on  
the size (width) of the transistor.

Inverter has both NFET and PFET, so we must  
consider intrinsic capacitances of both NFET  
and PFET.

# Recall: intrinsic transistor capacitances

*gate capacitance*:

$$C_{gate} = \frac{\epsilon}{t_{ox}} WL$$

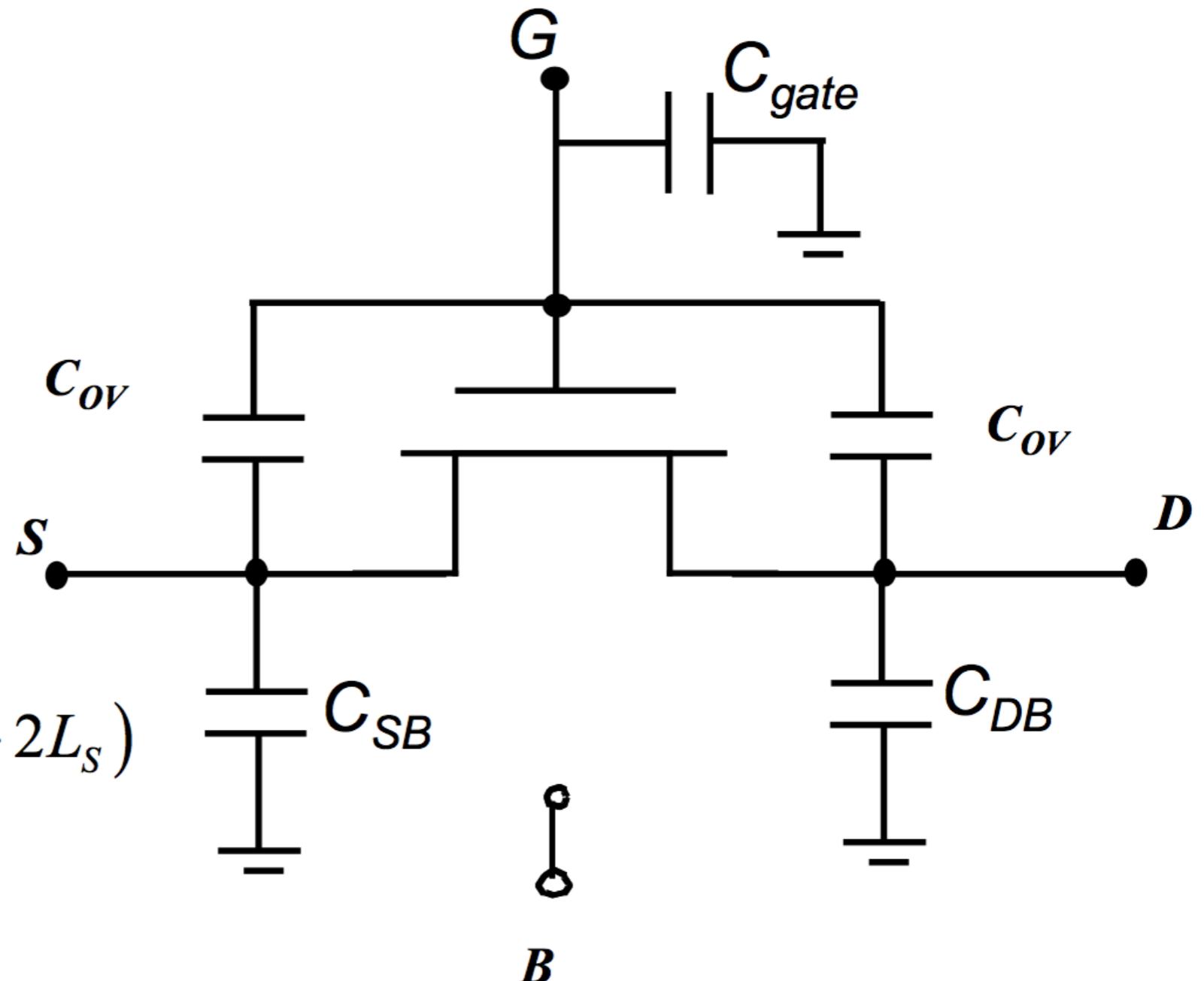
*overlap capacitance*:

$$C_{ov} = \frac{\epsilon}{t_{ox}} WX_{ov}$$

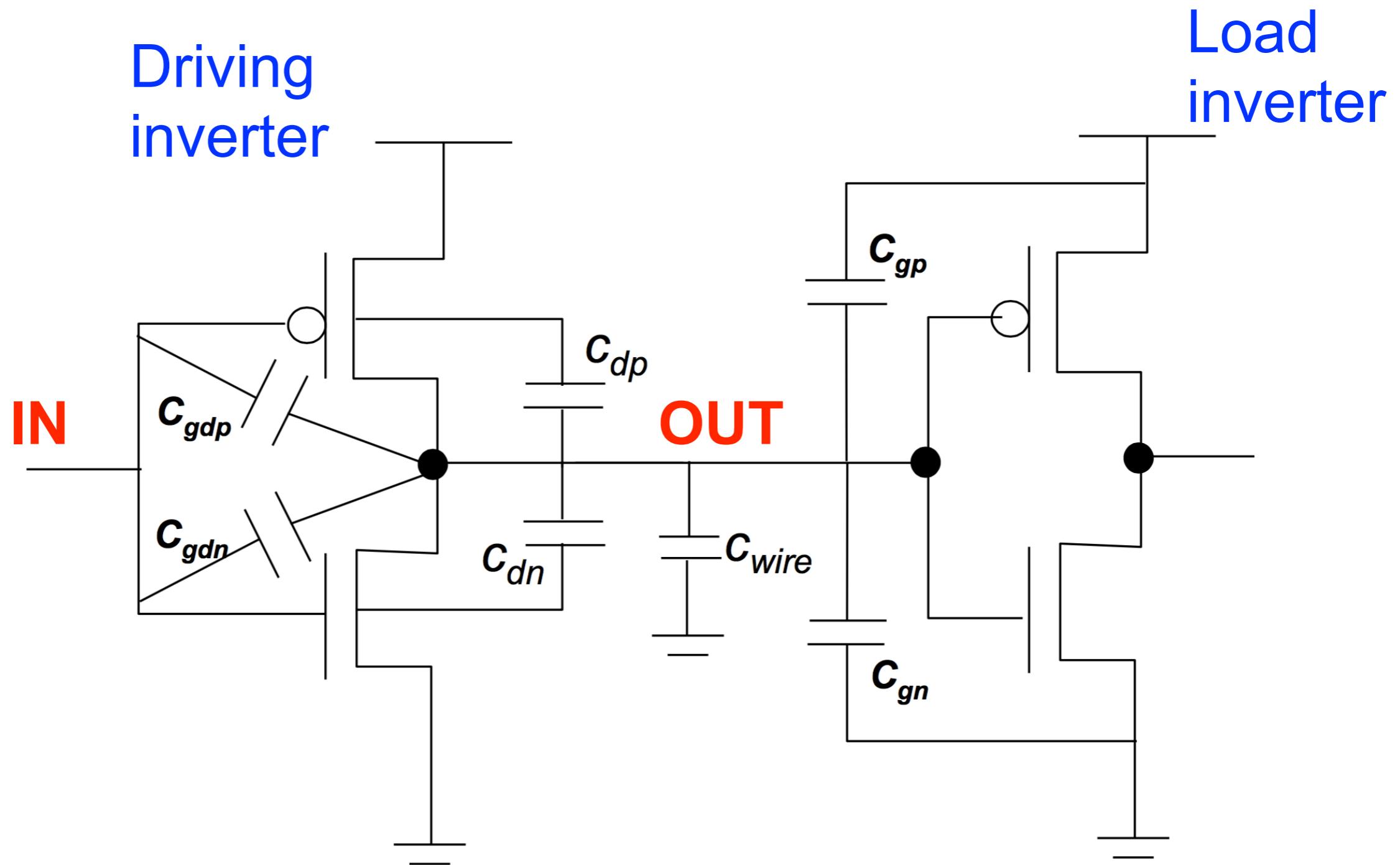
*Junction capacitance*:

$$C_{Junction} = C_j WL_S + C_{jsw} (W + 2L_S)$$

$C_j$  &  $C_{jsw}$  are tech. param.

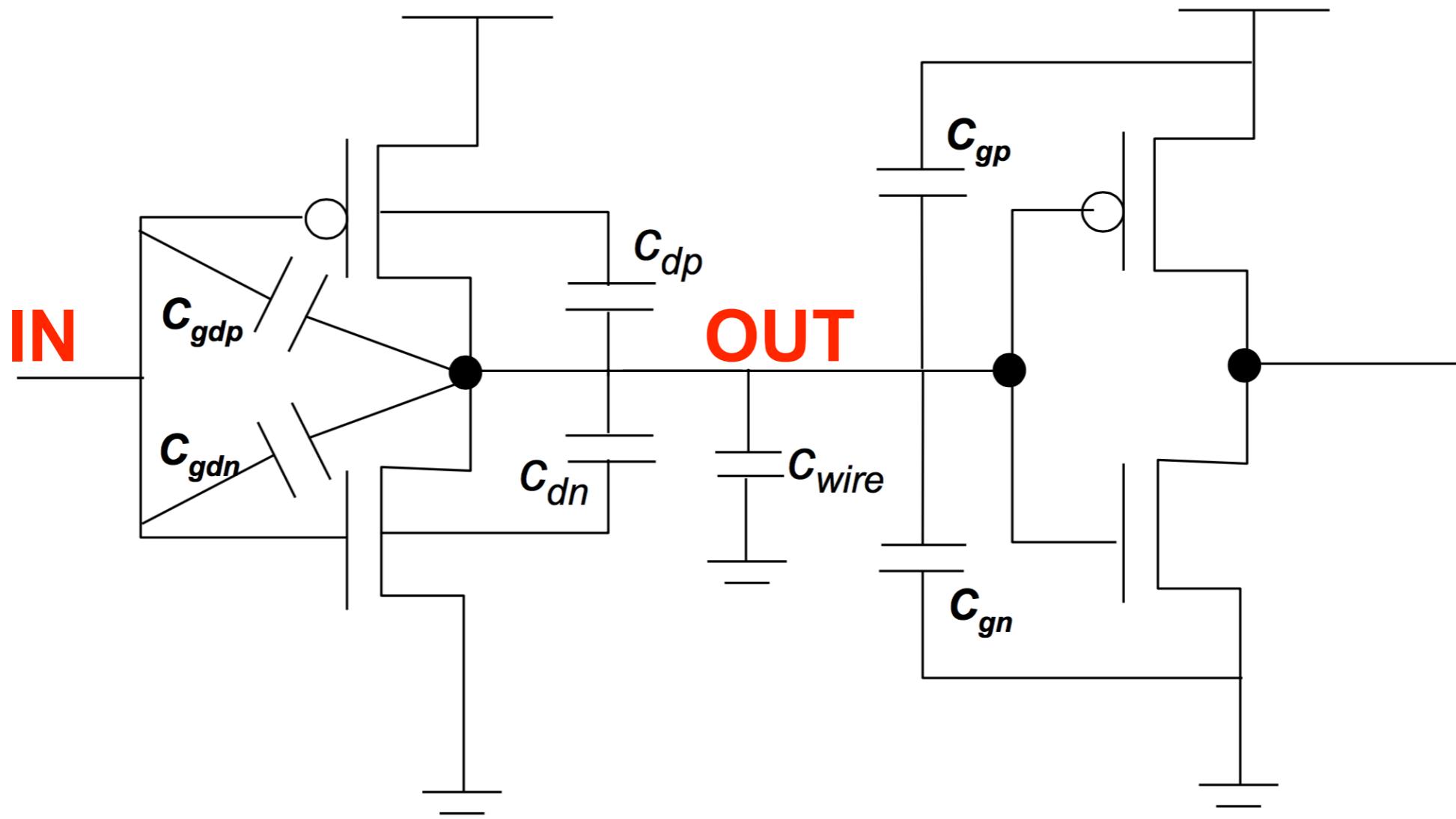


# Inverter capacitances



What is the capacitance at the OUT node?

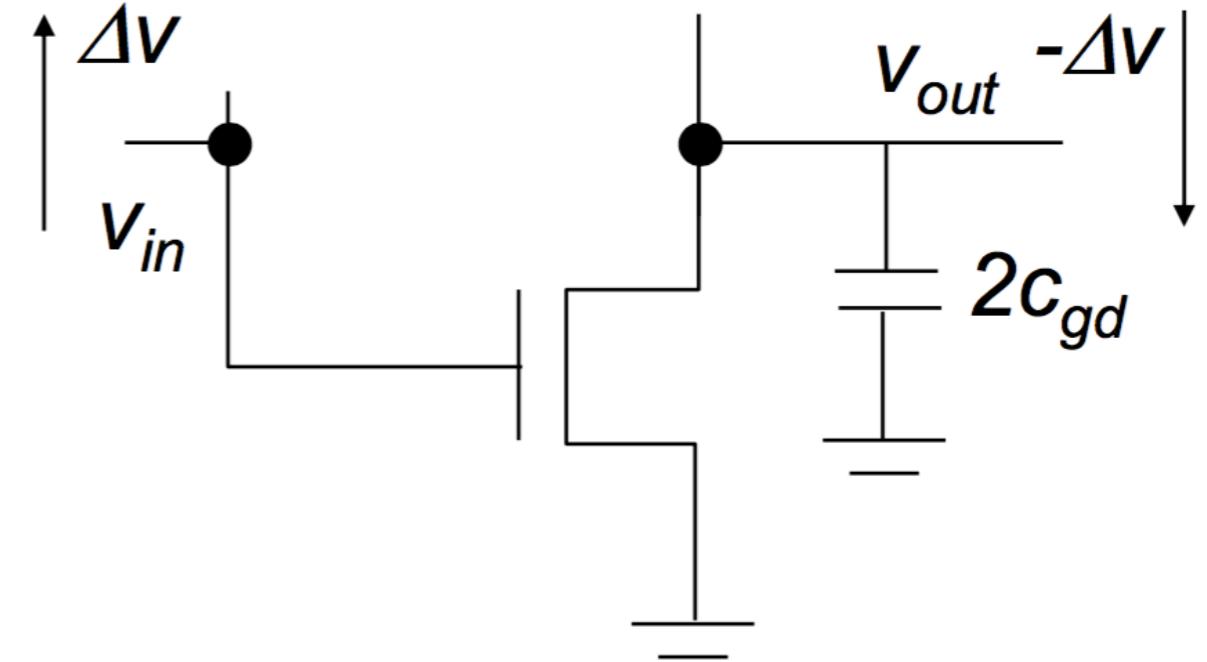
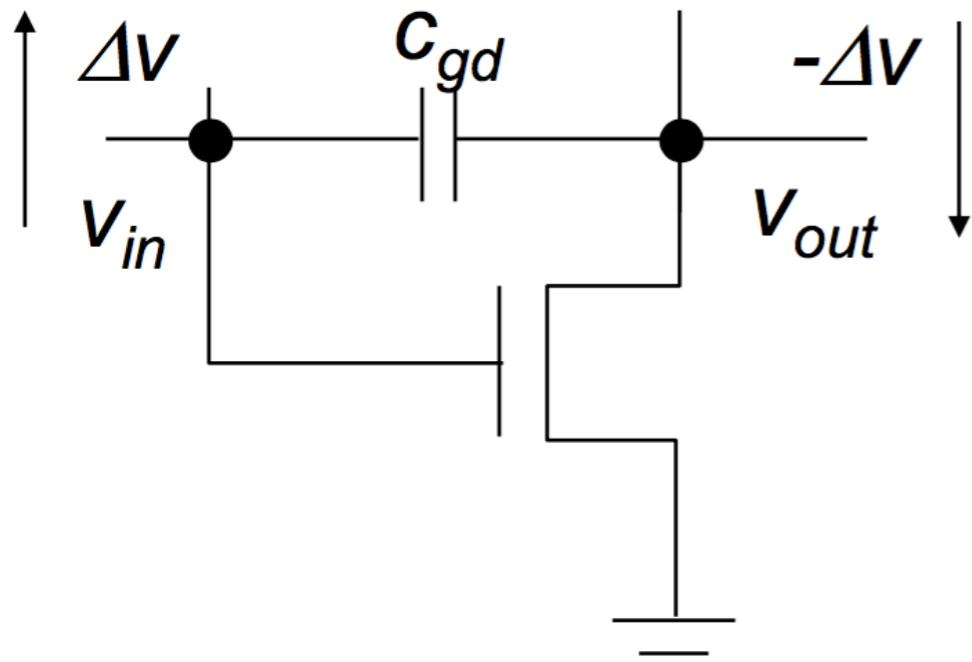
# Inverter capacitances



$$C_{OUT} = \left( C_{dp} + C_{dn} + \underbrace{2C_{gdp} + 2C_{gdn}}_{\text{Miller capacitance (doubled)}} \right) + C_{wire} + (C_{gp} + C_{gn})$$

Miller capacitance  
(doubled)

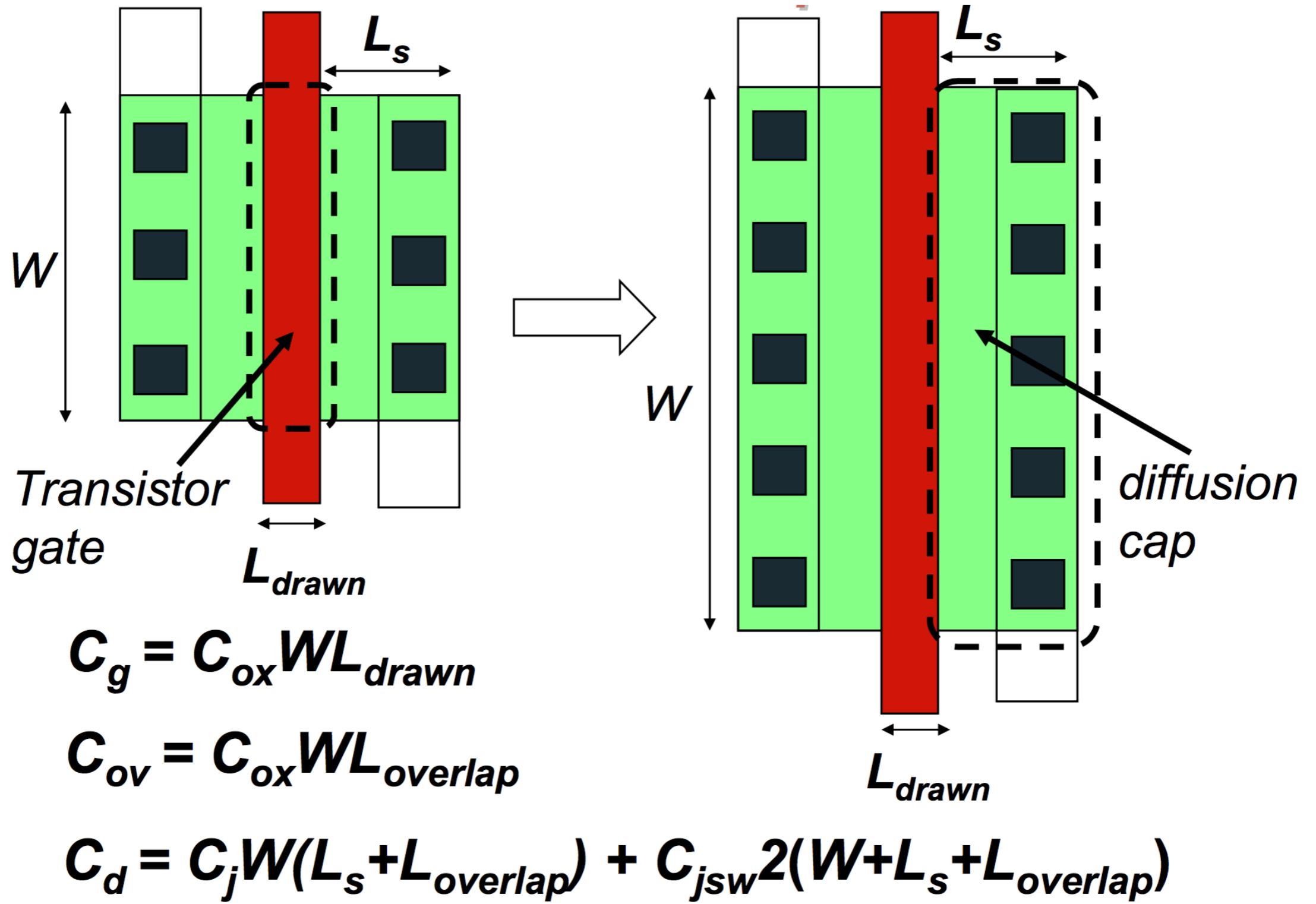
# Miller capacitance



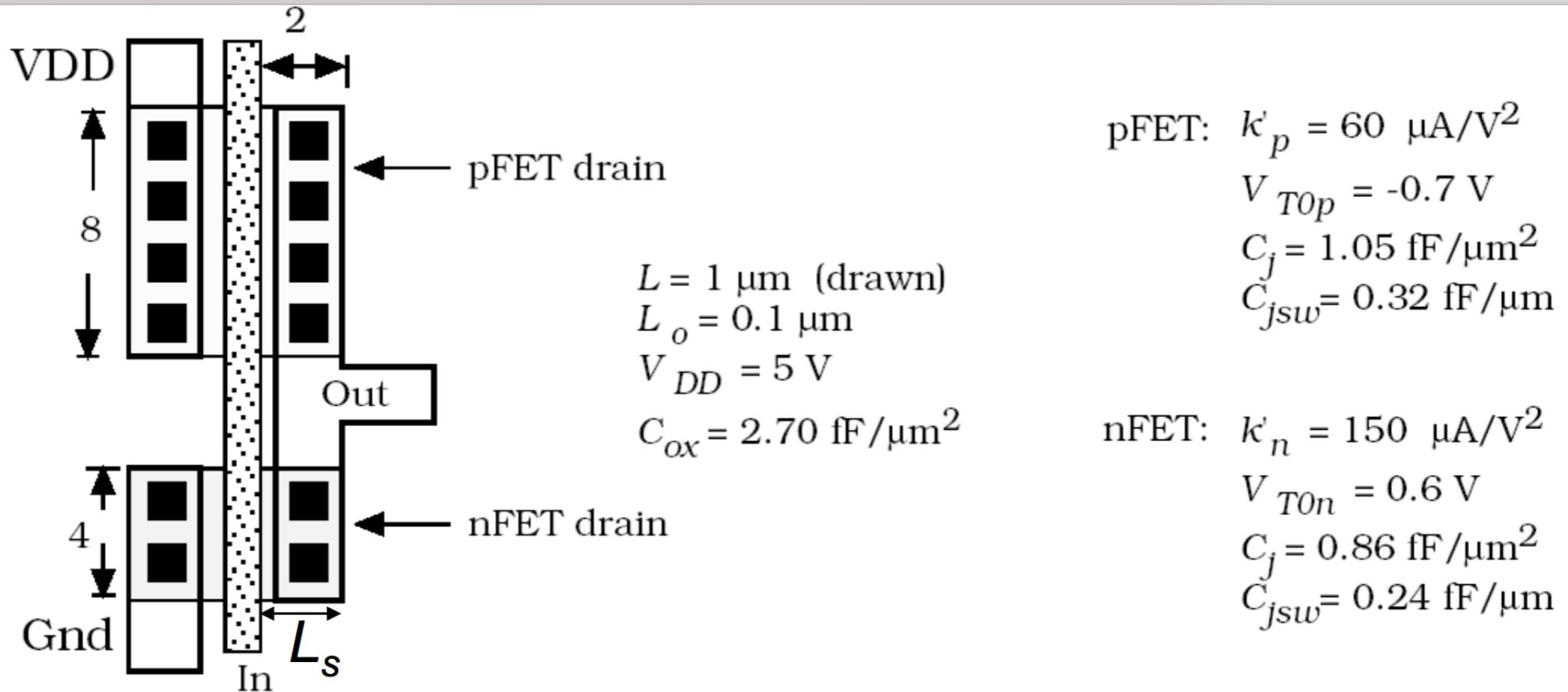
$$i = c_{gd} \frac{d(v_{out} - v_{in})}{dt} = c_{gd} \left( \frac{dv_{out}}{dt} - \frac{dv_{in}}{dt} \right) \sim c_{gd} \left( \frac{dv_{out}}{dt} + \frac{dv_{out}}{dt} \right) = (2c_{gd}) \frac{dv_{out}}{dt}$$

$$C_{Total} = \underbrace{\left( 2C_{gdn} + 2C_{gdp} + C_{dn} + C_{dp} \right)}_{C_{FET}} + \underbrace{\left( C_{wire} + C_{gn} + C_{gp} \right)}_{C_{LOAD}}$$

# Effect of device width on capacitance



# Example of capacitance calculation



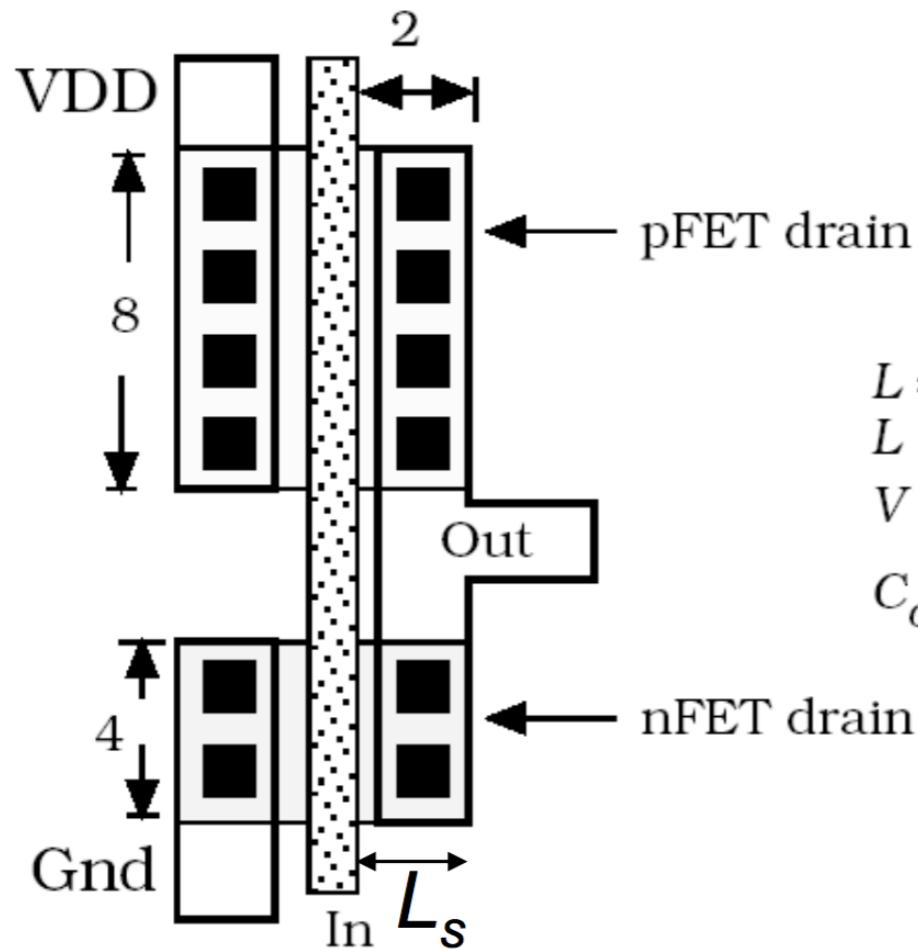
$$C_{dn} = C_{jn} \times W_n \times (L_{sn} + L_o) + C_{jswn} \times 2(W_n + L_{sn} + L_o)$$

$$= 0.86 \times 4 \times 2.1 + 0.24 \times 2 \times (4 + 2.1) = 10.15 \text{ fF}$$

$$C_{dp} = C_{jp} \times W_p \times (L_{sp} + L_o) + C_{jswp} \times 2(W_p + L_{sp} + L_o)$$

$$= 1.05 \times 8 \times 2.1 + 0.32 \times 2 \times (8 + 2.1) = 24.10 \text{ fF}$$

# Example of capacitance calculation



$$L = 1 \mu\text{m} \text{ (drawn)}$$

$$L_o = 0.1 \mu\text{m}$$

$$V_{DD} = 5 \text{ V}$$

$$C_{ox} = 2.70 \text{ fF}/\mu\text{m}^2$$

pFET:  $k'_p = 60 \text{ } \mu\text{A}/\text{V}^2$

$$V_{T0p} = -0.7 \text{ V}$$

$$C_j = 1.05 \text{ fF}/\mu\text{m}^2$$

$$C_{jsw} = 0.32 \text{ fF}/\mu\text{m}$$

nFET:  $k'_n = 150 \text{ } \mu\text{A}/\text{V}^2$

$$V_{T0n} = 0.6 \text{ V}$$

$$C_j = 0.86 \text{ fF}/\mu\text{m}^2$$

$$C_{jsw} = 0.24 \text{ fF}/\mu\text{m}$$

$$C_{gdn} = 2(C_{ox} \times W_n \times L_o) = 2(2.70 \times 4 \times 0.1) = 2.16 \text{ fF}$$

$$C_{gdः} = 2(C_{ox} \times W_p \times L_o) = 2(2.70 \times 8 \times 0.1) = 4.32 \text{ fF}$$

*For an Identical load :*

$$C_{gn} = C_{ox} W_n L_{drawn} = 10.8 \text{ fF}; \text{ and } C_{gp} = C_{ox} W_p L_{drawn} = 21.6 \text{ fF}$$

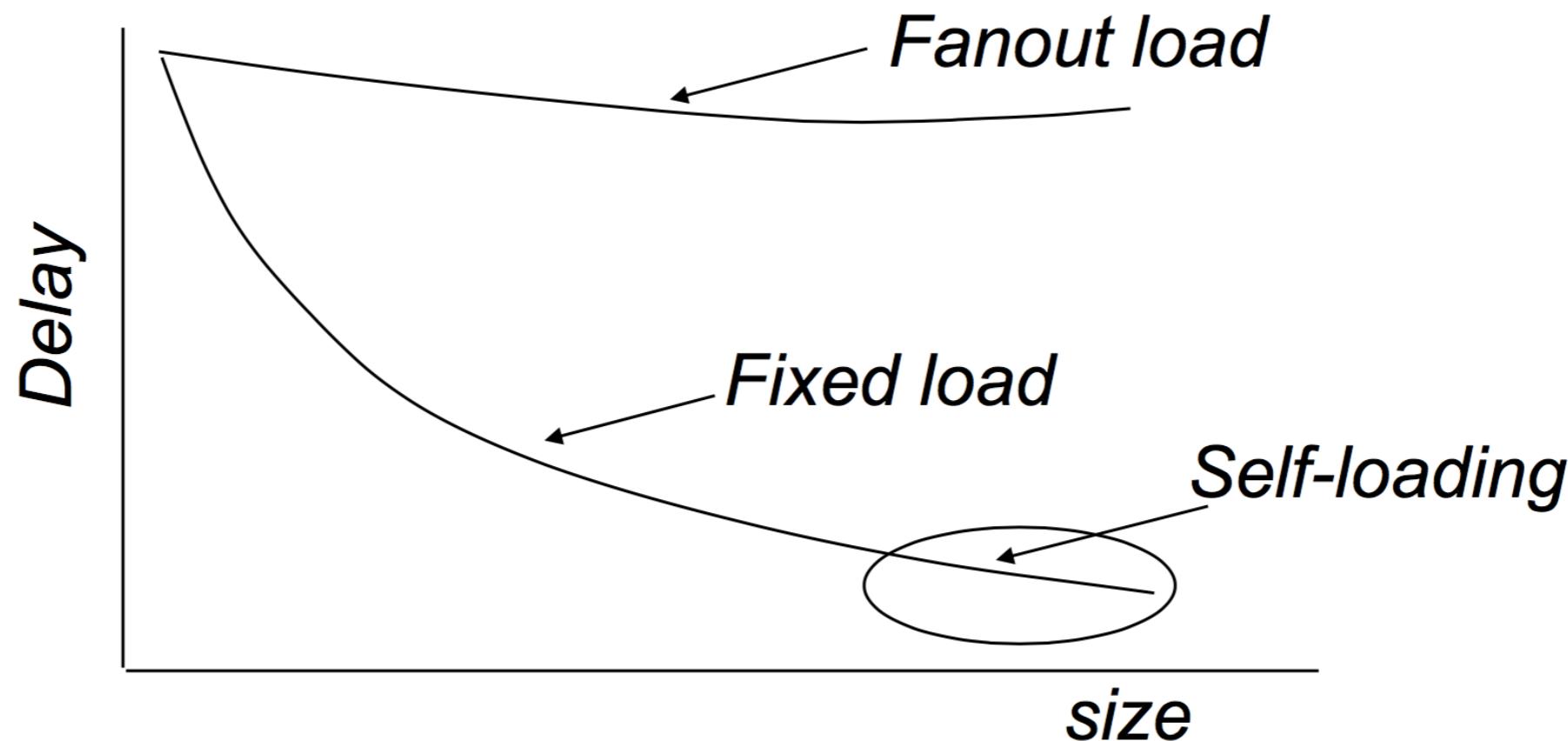
# Capacitance: key observation

Increasing the width of the transistor increases its own capacitance and may negatively affect its delay

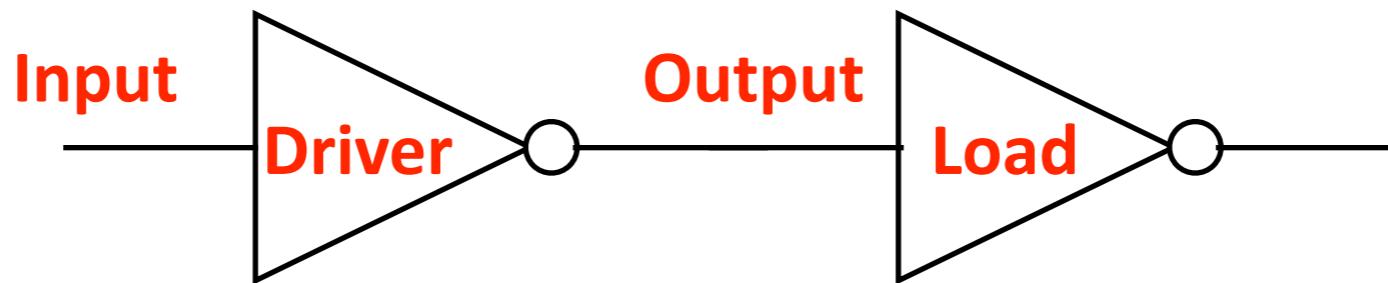
## ***Self-loading***

# Delay versus device size

- Fixed load: higher size => higher current => lower delay
  - Very large size may not be effective due to increase in intrinsic capacitance – self loading effect
- Fanout Load: A number of identical inverters constitute the load
  - Higher size => larger gate capacitance of the fanouts – there will not be much benefit

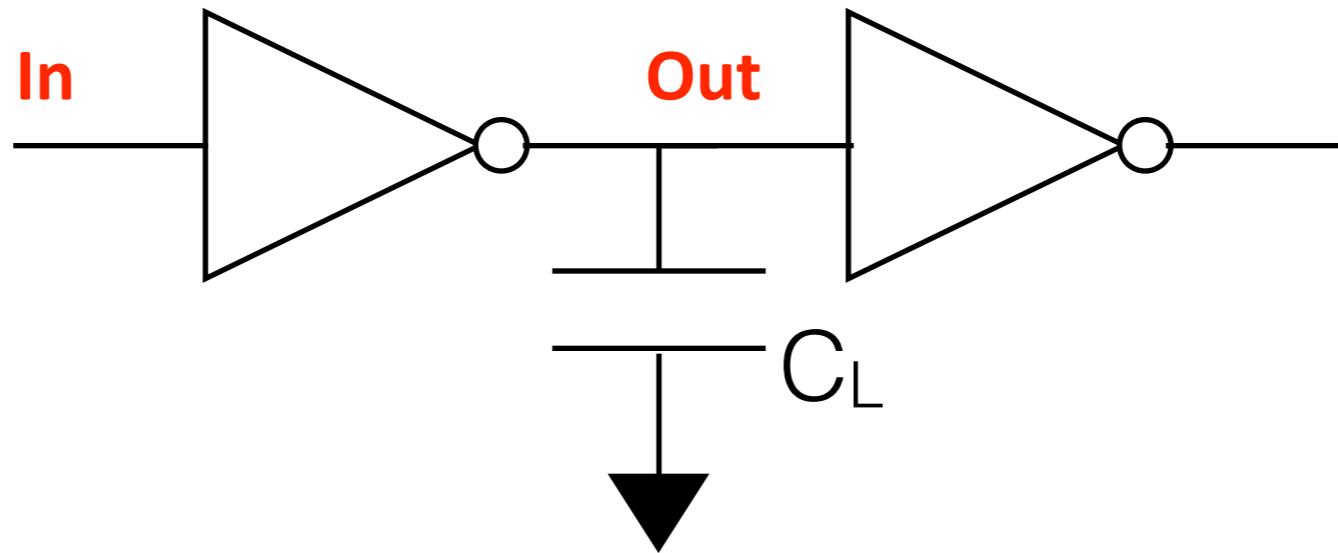


# Optimal choice of NFET/PFET ratio



- INV1 and INV2 are sized similarly.
- Choose  $(W_p/W_n) = \alpha$ .
- Find the value of  $\alpha$  such that the delay of INV1 is minimized.
- Recall expression of  $t_d$  from slide # 24.

# Optimal choice of NFET/PFET ratio



$$C_L = \underbrace{(1 + \alpha) C_{FET\_n}}_{\text{Driving inverter}} + C_{wire} + \underbrace{(1 + \alpha) C_{gn}}_{\text{Load inverter}} + \text{gate cap.}$$

Driving inverter: (Parasitic cap. PFET)/ (Parasitic cap. NFET) =  $\alpha$   
Load inverter: Gate cap. PFET)/(Gate cap. of NFET) =  $\alpha$

# Optimal choice of NFET/PFET ratio

$$\begin{aligned}
 t_d &= 0.5 \frac{C_L V_{DD}}{(V_{DD} - V_T)^2} \left( \frac{1}{\beta_n} + \frac{1}{\beta_p} \right) \\
 &= 0.5 \frac{V_{DD}}{\beta_n (V_{DD} - V_T)^2} \left[ (1 + \alpha) (C_{FET\_n} + C_{gn}) + C_W \right] \left( 1 + \alpha \frac{\mu_n}{\mu_p} \right)
 \end{aligned}$$

for  $\frac{\partial t_d}{\partial \alpha} = 0 \Rightarrow \alpha_{opt} = \sqrt{\frac{\mu_n}{\mu_p}} \sqrt{1 + \frac{C_W}{C_{FET\_n} + C_{gn}}}$

If  $C_W \ll C_{FET\_n} + C_{gn} \Rightarrow \alpha_{opt} = \sqrt{\frac{\mu_n}{\mu_p}}$

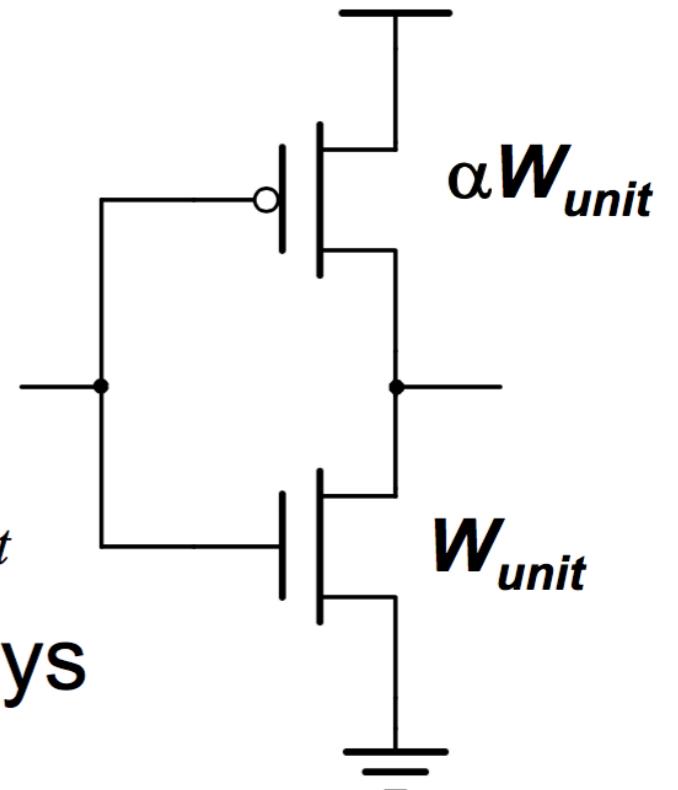
Sizing inverter chain for driving large capacitance

Goal: Minimize propagation delay !



# Standardize inverter delay

- Minimum length devices,  $L=0.25\mu\text{m}$
- Assume that for  $W_P = \alpha W_N = \alpha W_{unit}$ 
  - same pull-up and pull-down currents
  - approx. equal resistances  $R_N = R_P = R_{unit}$
  - approx. equal rise  $t_{pLH}$  and fall  $t_{pHL}$  delays

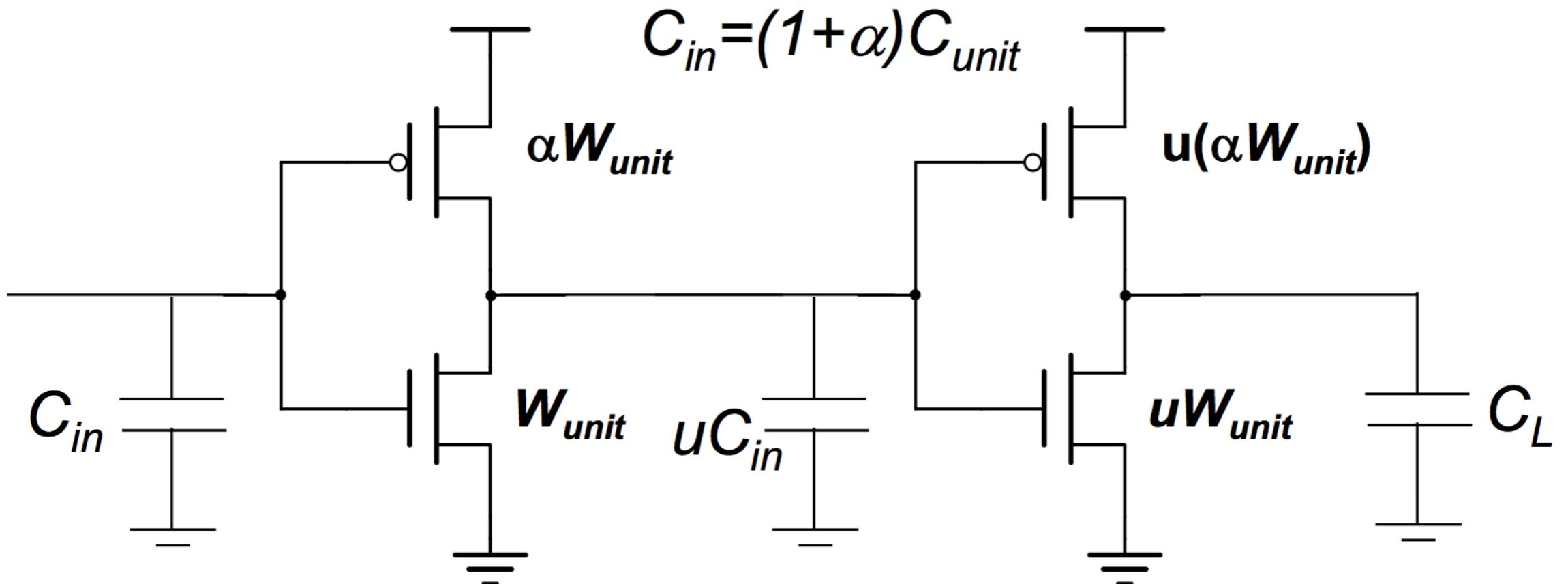


**Delay ( $D$ ):**  $t_d = t_{pHL} = t_{pLH} = (\ln 2) R_{unit} C_L$

Input capacitance = load for the previous stage

$$C_{in} = (1 + \alpha) C_N = (1 + \alpha) C_{unit}$$

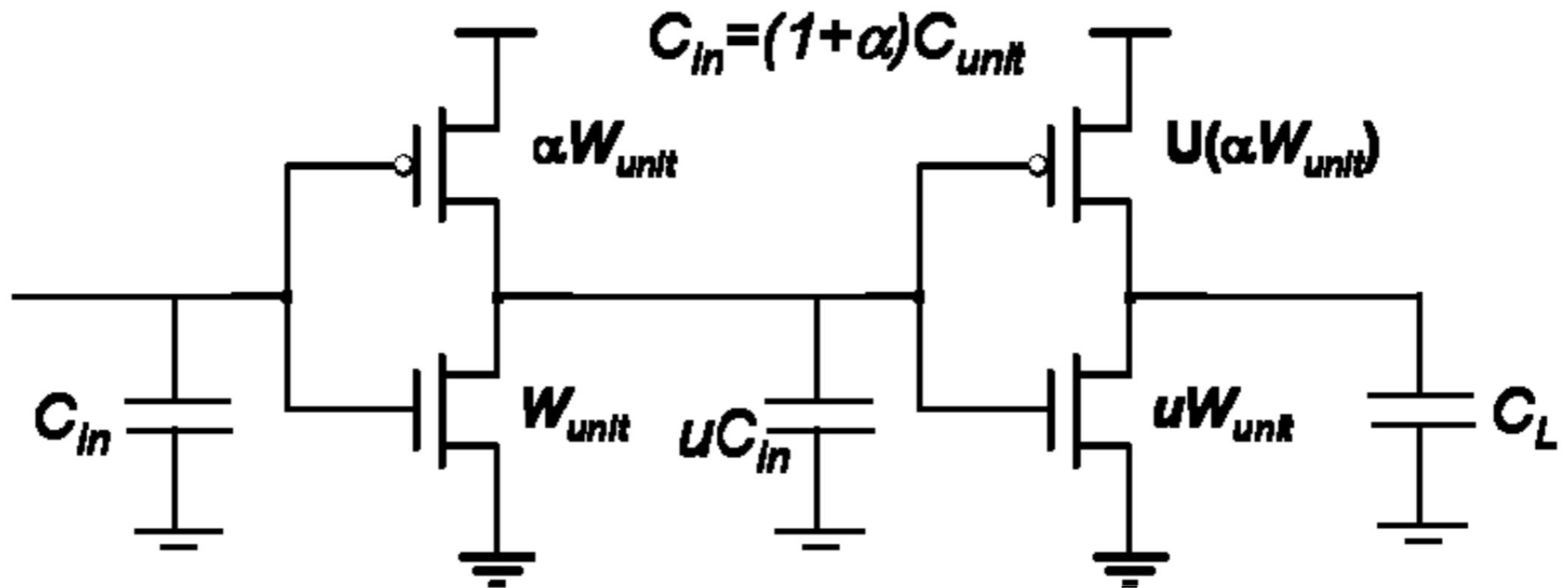
## 2-Inverter chain



*Delay of unit inv driving unit inv:*  $t_{p0} = 0.69R_{unit}C_{in}$

$$t_p = 0.69R_{unit}uC_{in} + 0.69\left(\frac{R_{unit}}{u}\right)C_L = t_{p0}\left(u + \frac{f}{u}\right); f = C_L/C_{in}$$

## 2-Inverter chain

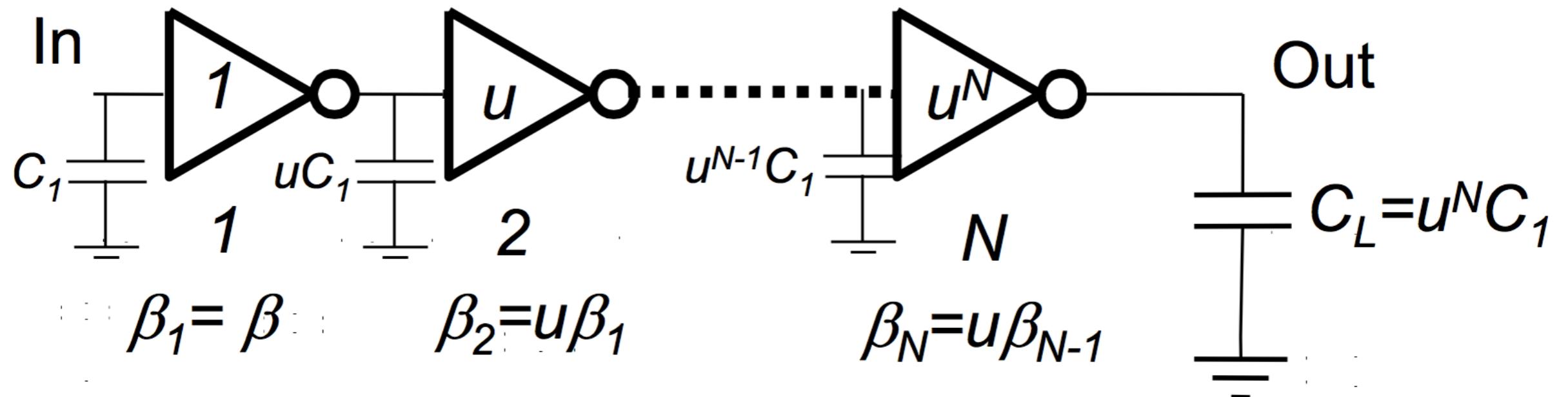


*Optimal Buffering*:  $\frac{\partial t_p}{\partial u} = 0 \Rightarrow u_{opt} = \sqrt{f} \Rightarrow t_{p,opt} = 2t_{p0}\sqrt{f}$

*Single Stage*:  $t_s = 0.69R_{unit}C_L = 0.69R_{unit}C_{unit} \left( C_L / C_{unit} \right) = ft_{p0}$

*Buffering* is helpful if:  $ft_{p0} > 2\sqrt{f}t_{p0} \Rightarrow f > 4$

# Inverter chain for driving large load



If  $C_L$  is given:

- How many stages are needed to minimize the delay?
- How to size the inverters?

# Inverter chain for driving large load

$$\text{Stage Delay: } t_{pj} = 0.69R_jC_{j+1} = 0.69 \frac{R_1}{u^j} C_1 u^{j+1} = u(0.69R_1C_1) = u(\tau_r)$$

$$\text{Total Delay: } t_p = t_{p1} + \dots + t_{pn} = N u \tau_r$$

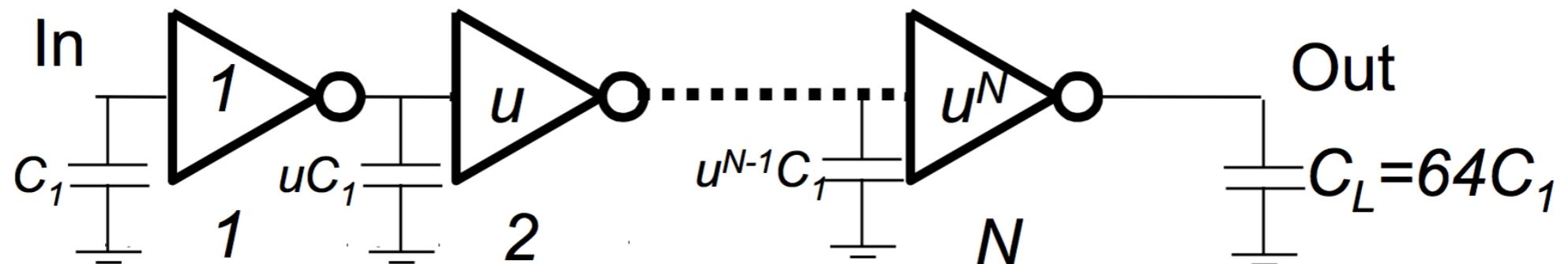
$$\text{Number of stage: } C_L = u^N C_1 \Rightarrow N = \frac{\ln(C_L/C_1)}{\ln(u)}$$

$$\text{Total Delay: } t_p = \tau_r \ln(C_L/C_1) \frac{u}{\ln(u)}$$

$$\text{Optimal Tapering: } \frac{\partial t_p}{\partial u} = 0 \Rightarrow \frac{\ln(u) - 1}{[\ln(u)]^2} = 0 \Rightarrow \ln(u) = 1 \Rightarrow u_{opt} = e$$

$$\text{Optimal Number of Stages: } N_{opt} = \ln(C_L/C_1)$$

# Application

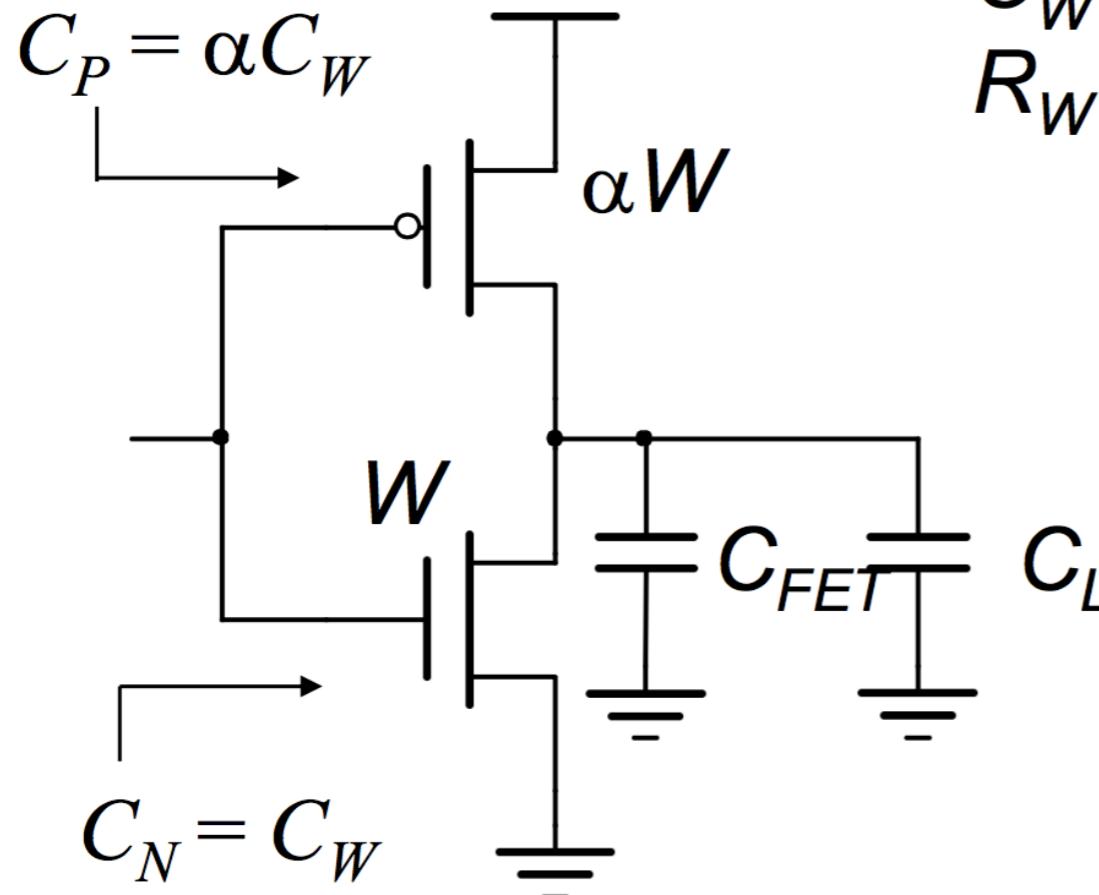


$$N = \ln(C_L/C_1) = \ln(64) = 4.15 \sim 4 \Rightarrow u = (C_L/C_1)^{1/N} = 2.82$$

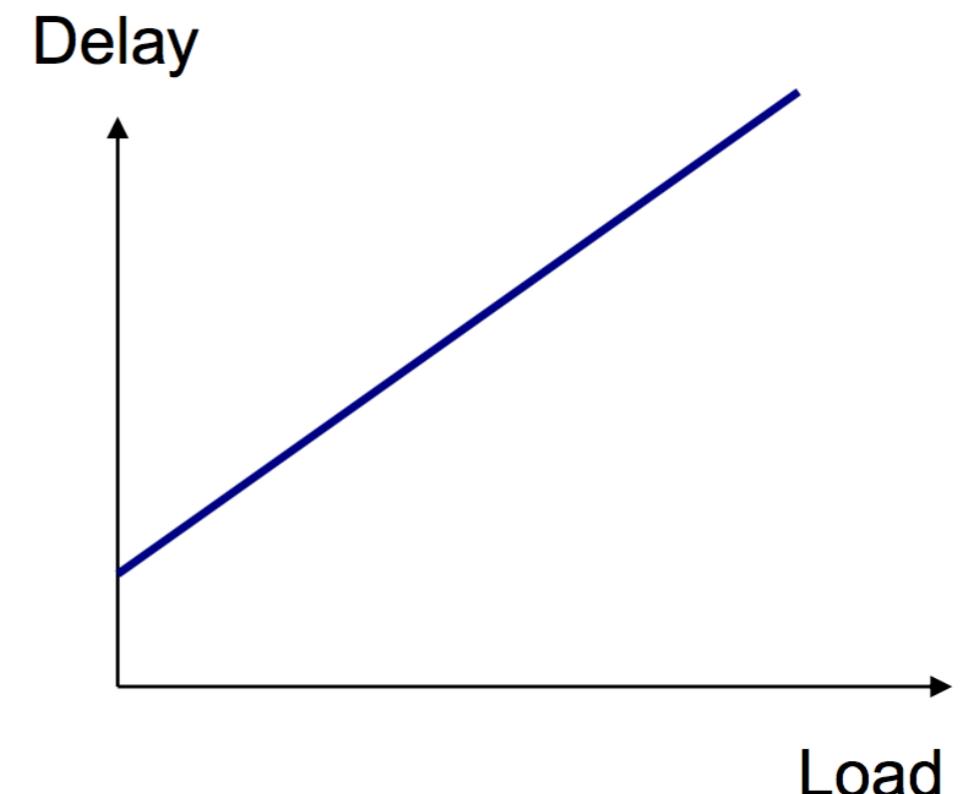
$$t_p = \tau_r \times 4 \times 2.82 = 11.28\tau_r$$

<b>N</b>	<b>u</b>	<b>tp</b>
<b>1</b>	<b>1</b>	<b>64</b>
<b>2</b>	<b>8</b>	<b>16</b>
<b>3</b>	<b>4</b>	<b>12</b>
<b>4</b>	<b>2.82</b>	<b>11.28</b>
<b>5</b>	<b>2.29</b>	<b>11.48</b>

# Inverter delay with intrinsic capacitance



$C_W$  = cap for width  $W$   
 $R_W$  = resistance for width  $W$



$$\begin{aligned} \text{Delay} &= kR_W(C_{FET} + C_L) = kR_W C_{FET}(1 + C_L / C_{FET}) \\ &= \text{Delay (Internal)} + \text{Delay (Load)} \end{aligned}$$

# Inverter chain for driving large load

$$\text{Stage Delay: } t_{pj} = 0.69R_j(C_{FET,j} + C_{j+1}) = 0.69 \frac{R_1}{u^j} (C_1 u^{j+1} + C_{FET,1} u^j)$$

$$\text{Total Delay: } t_p = t_{p1} + \dots + t_{pn} = N u \left( \underbrace{0.69 R_1 C_1}_{\tau_r} \right) + N \left( \underbrace{0.69 R_1 C_{FET,1}}_{\tau_x} \right)$$

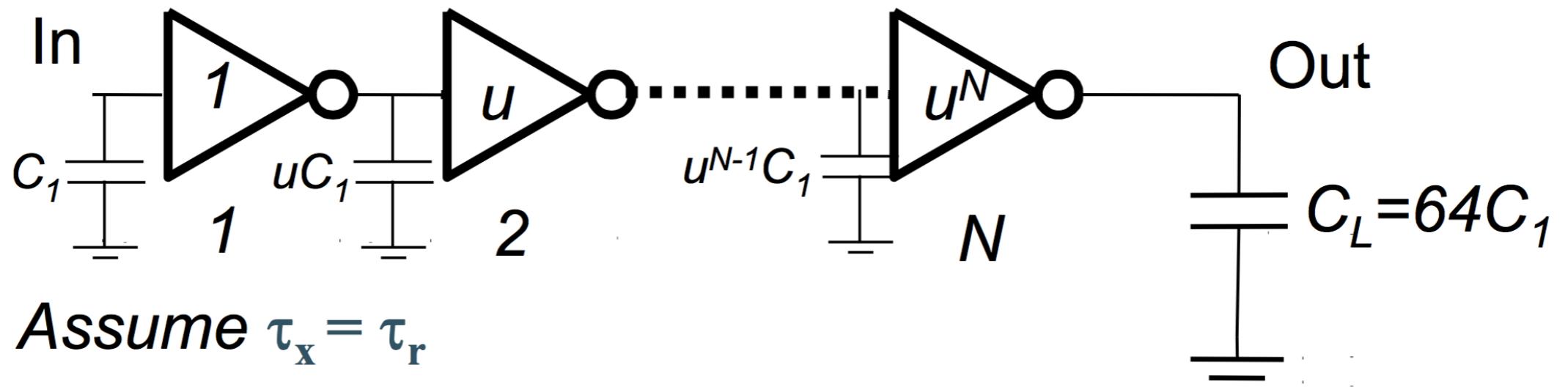
$$t_p = \ln \left( \frac{C_L}{C_1} \right) \left[ \frac{u}{\ln(u)} \tau_r + \frac{\tau_x}{\ln(u)} \right]$$

$$\text{optimal } u_{opt} \text{ is given by: } \frac{\partial t_p}{\partial u} = 0 \Rightarrow \frac{\ln(u) - 1}{[\ln(u)]^2} \tau_r - \frac{\tau_x}{u [\ln(u)]^2} = 0$$

$$\text{Optimal Tapering: } u_{opt} [\ln(u_{opt}) - 1] = \tau_x / \tau_r = C_{FET,1} / C_1$$

$$\text{Optimal Number of Stages: } N_{opt} = \frac{\ln(C_L / C_1)}{\ln(u_{opt})}$$

# Application



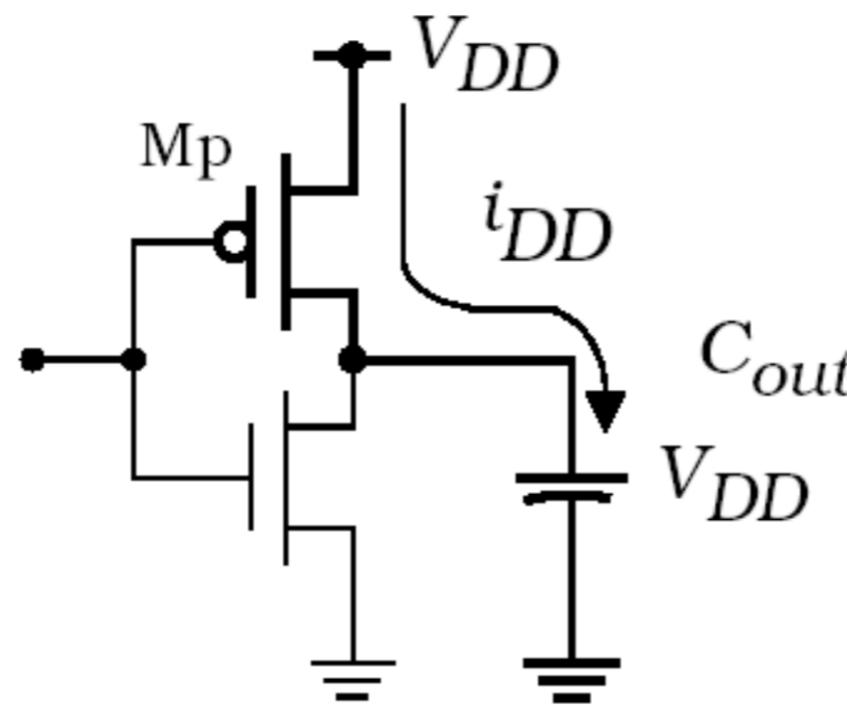
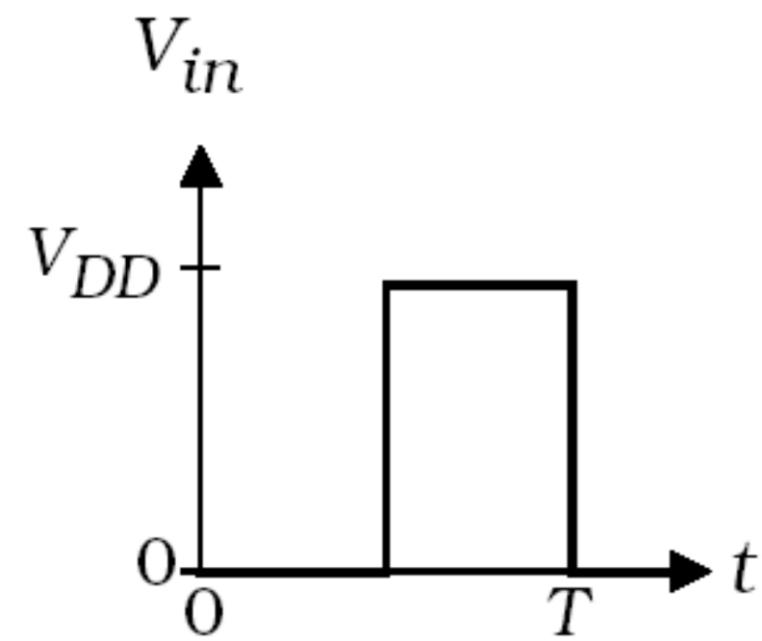
<b>N</b>	<b>u</b>	<b>Nuτ<sub>r</sub></b>	<b>Nτ<sub>x</sub></b>	<b>t<sub>p</sub></b>
1	1	<b>64</b>	1	<b>65</b>
2	8	<b>16</b>	2	<b>18</b>
<b>3</b>	<b>4</b>	<b>12</b>	<b>3</b>	<b>15</b>
4	<b>2.82</b>	<b>11.28</b>	4	<b>15.28</b>
5	<b>2.29</b>	<b>11.48</b>	5	<b>15.48</b>

# Inverter power dissipation

# Inverter power dissipation

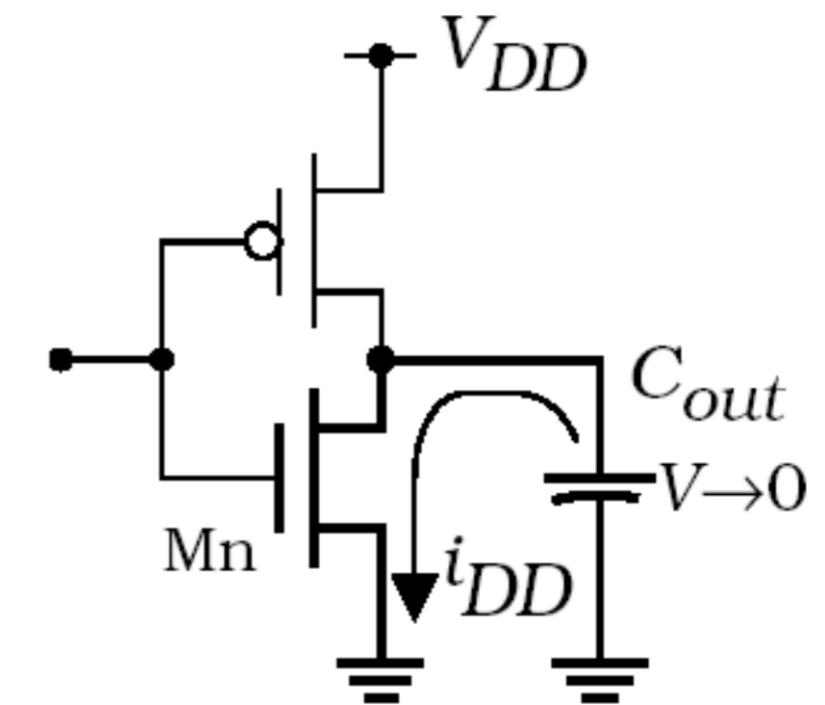
- **Dynamic Power Consumption**  
**Charging and Discharging Capacitors**
- **Short Circuit Currents**  
**Short Circuit Path between Supply Rails during Switching**
- **Leakage**  
**Leaking diodes and transistors**

# Dynamic power dissipation



(a) Input voltage

(b) Charge



(c) Discharge

# Dynamic power dissipation

## Charging

*Energy drawn from supply :*

$$E_{vDD} = \int_0^{\infty} i_{vDD}(t) V_{DD} dt = V_{DD} \int_0^{\infty} \frac{d(C_L v_{out})}{dt} dt = C_L V_{DD} \int_0^{V_{DD}} dv_{out} = C_L V_{DD}^2$$

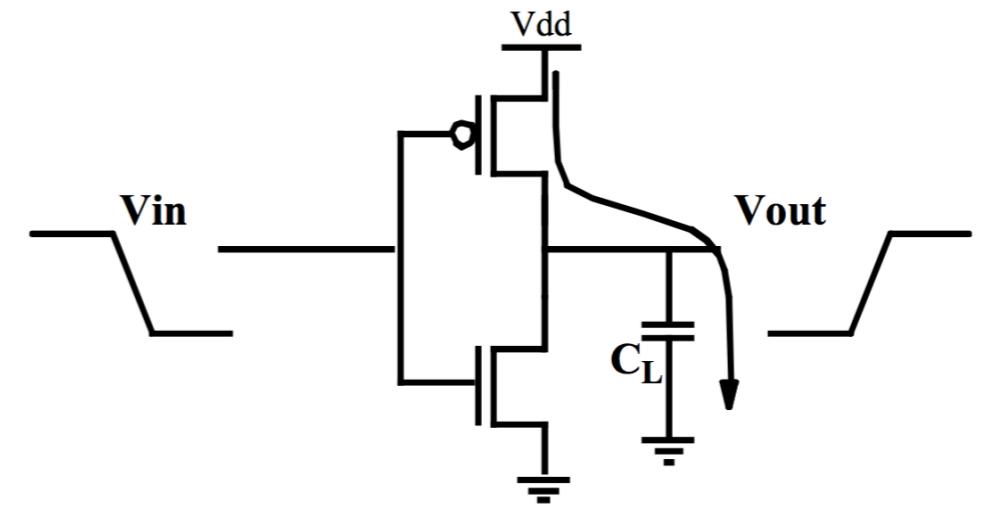
*Energy stored in capacitor :*

$$E_C = \int_0^{\infty} i_c(t) v_{out} dt = \int_0^{\infty} \frac{d(C_L v_{out})}{dt} v_{out} dt = C_L \int_0^{V_{DD}} v_{out} dv_{out} = \frac{1}{2} C_L V_{DD}^2$$

*Energy dissipated in resistor :*  $E_R = E_{vDD} - E_C = \frac{1}{2} C_L V_{DD}^2$

$$\text{Also, } E_R = \int_0^{\infty} i_R^2(t) R dt = \int_0^{\infty} i_R(t) \frac{V_{DD} - v_{out}}{R} R dt = \int_0^{\infty} \frac{d(C_L v_{out})}{dt} (V_{DD} - v_{out}) dt = \frac{1}{2} C_L V_{DD}^2$$

$\Rightarrow$  Independent of  $R$



# Total dynamic energy dissipation

*Charging :*

*Energy dissipated in resistor :  $\frac{1}{2}C_L V_{DD}^2$*

*Energy stored in capacitor :  $\frac{1}{2}C_L V_{DD}^2$*

*Dis – Charging :*

*Energy dissipated in resistor :  $\frac{1}{2}C_L V_{DD}^2$*

**Total energy dissipation per cycle:  $E_{dyn} = C_L V_{DD}^2$**

**Total power dissipation per cycle:  $P_{dyn} = f_{clk} C_L V_{DD}^2$**

# Node transition activity and power

**Consider switching a CMOS gate for N clock cycles**

$$E_N = C_L \cdot V_{dd}^2 \cdot n(N)$$

$E_N$  : the energy consumed for  $N$  clock cycles

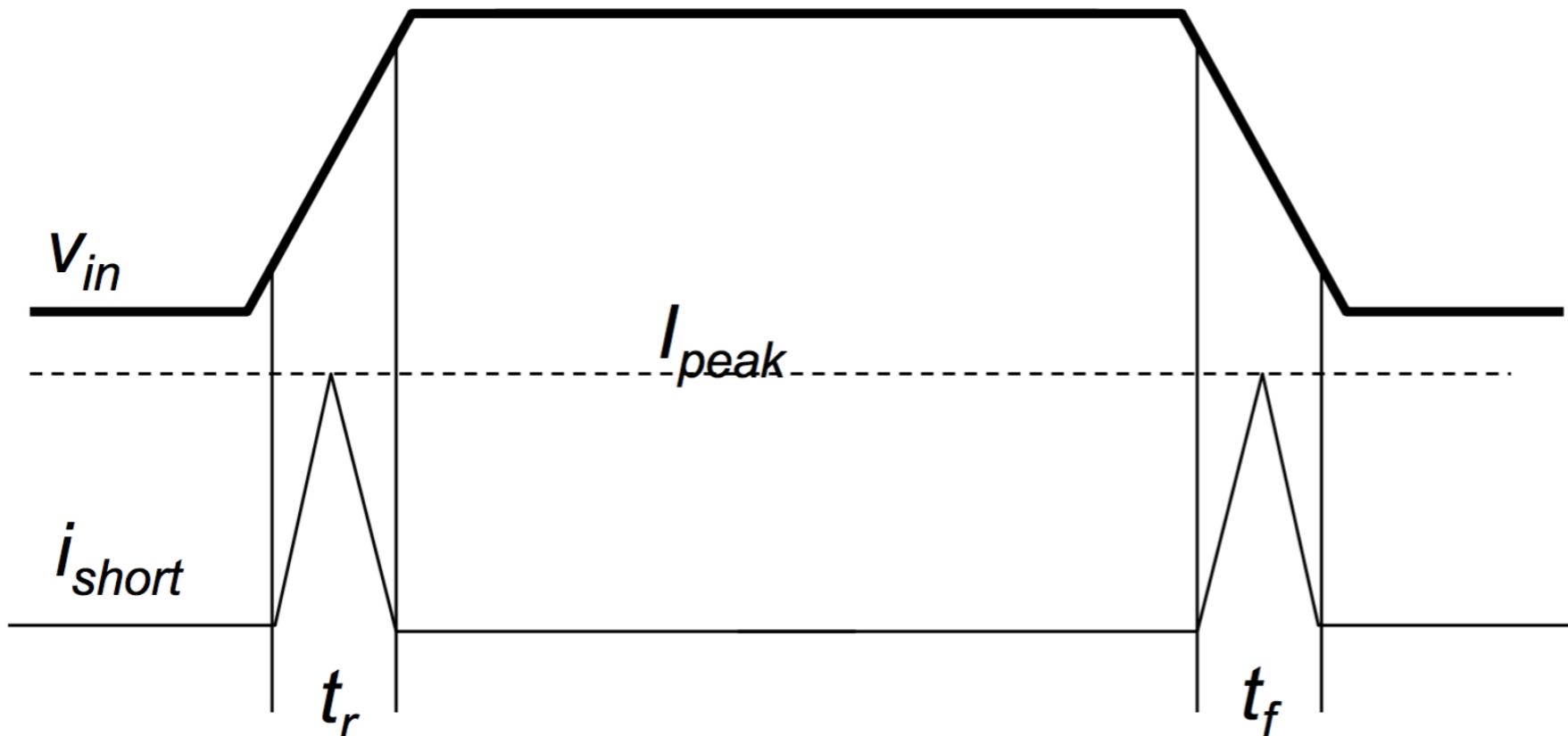
$n(N)$ : the number of 0->1 transition in  $N$  clock cycles

$$P_{avg} = \lim_{N \rightarrow \infty} \frac{E_N}{N} \cdot f_{clk} = \left( \lim_{N \rightarrow \infty} \frac{n(N)}{N} \right) \cdot C_L \cdot V_{dd}^2 \cdot f_{clk}$$

$$\alpha_{0 \rightarrow 1} = \lim_{N \rightarrow \infty} \frac{n(N)}{N}$$

$$P_{avg} = \alpha_{0 \rightarrow 1} \cdot C_L \cdot V_{dd}^2 \cdot f_{clk}$$

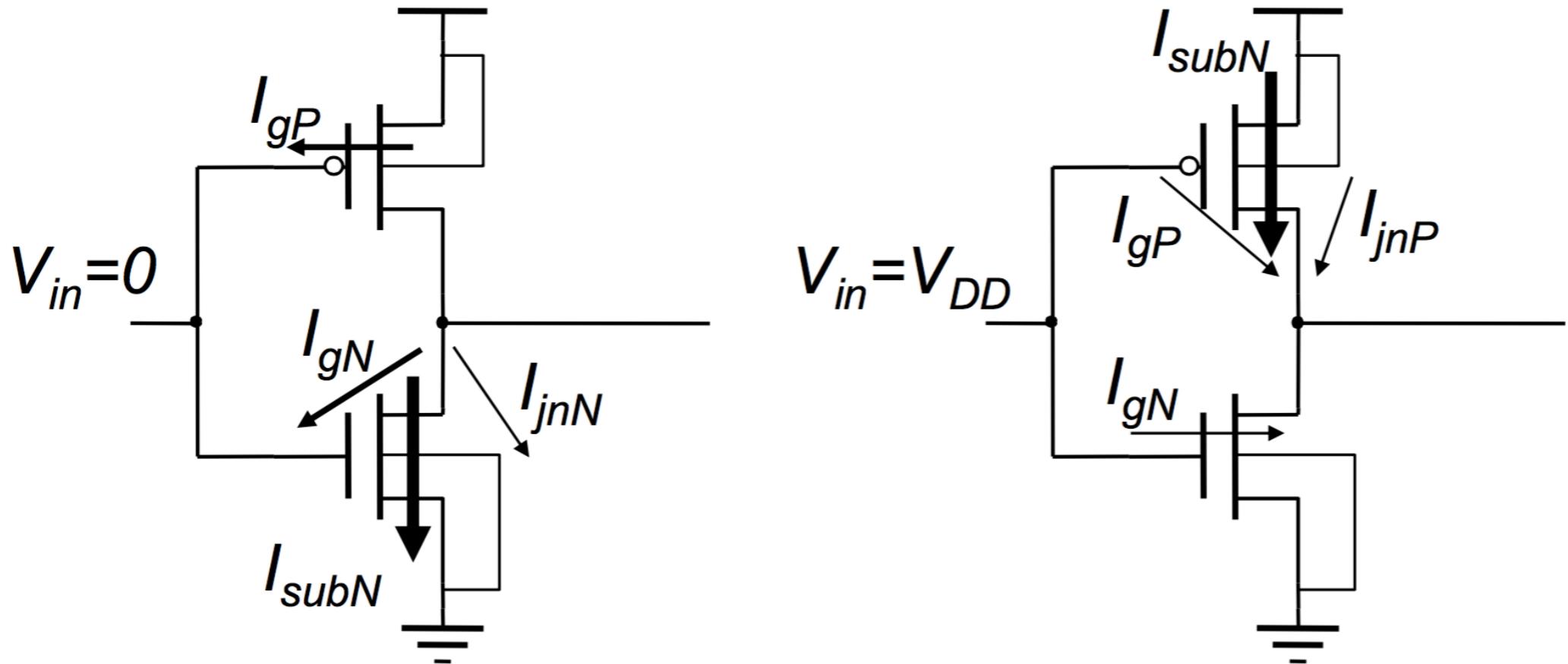
# Short-circuit power



$$E_{SC} = V_{DD} \frac{I_{peak} t_r}{2} + V_{DD} \frac{I_{peak} t_f}{2} = V_{DD} I_{peak} \frac{t_r + t_f}{2} \text{ and } P_{SC} = V_{DD} I_{peak} \frac{t_r + t_f}{2} f_{CLK}$$

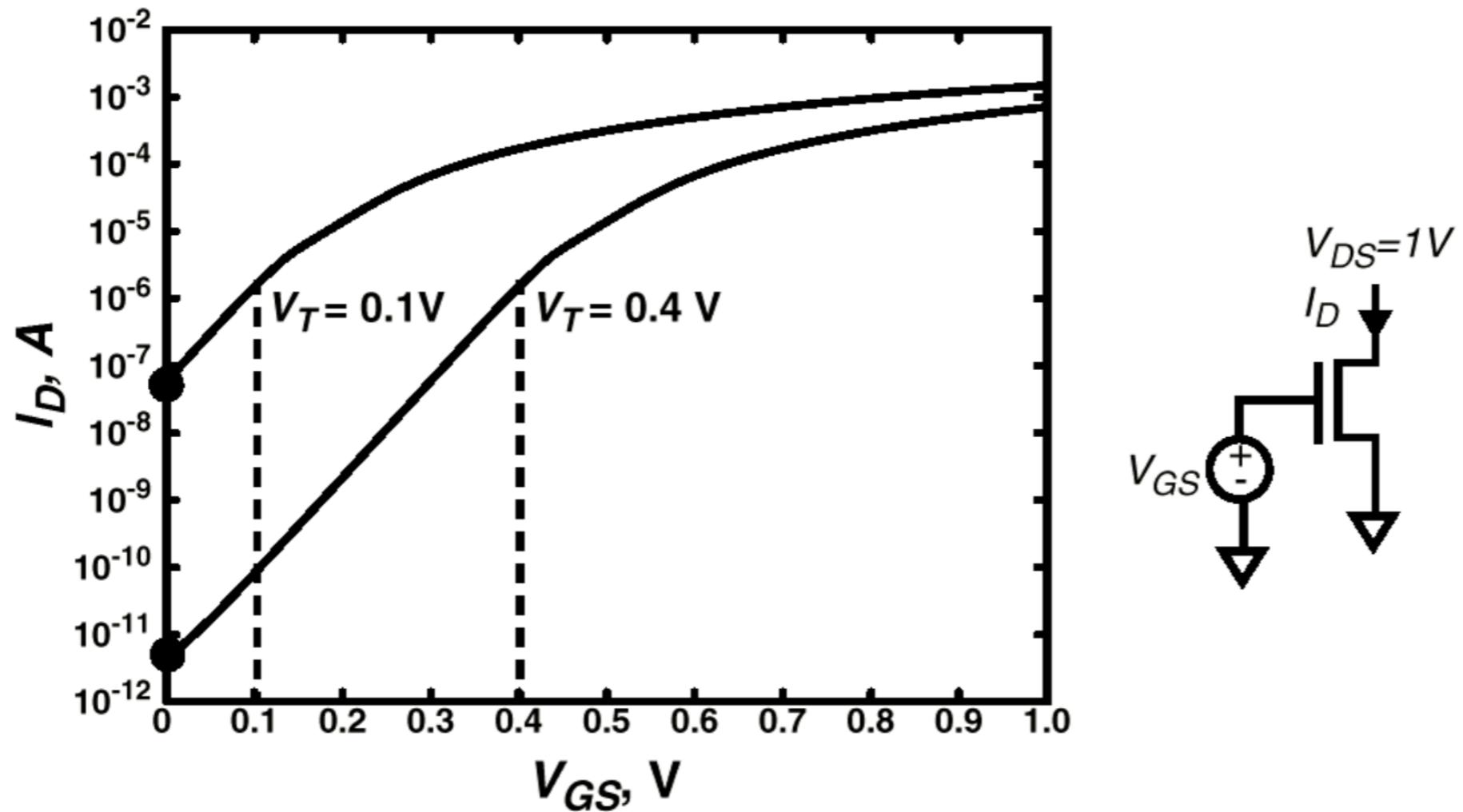
- ***Higher rise/fall time increases short-circuit power.***
- ***Short-circuit power is normally 10%-20% of dynamic power and can be neglected for first order analysis***

# Static or leakage power



- **Leakage: Subthreshold + Gate + Junction**
- **Most important: Subthreshold**
- $P_{static} = V_{DD}I_{static} = 0.5V_{DD} (I_{subN} + I_{subP})$

# Subthreshold Leakage component



$$\begin{aligned}
 P_{static} &= 0.5V_{DD} \left( I_{0N} \exp\left(\frac{-qV_{thn}}{n_N kT}\right) + I_{0P} \exp\left(\frac{-q|V_{thp}|}{n_P kT}\right) \right) \\
 &= 0.5V_{DD} (I_{0N} + I_{0P}) \exp\left(\frac{-qV_{th}}{n_N kT}\right) (\text{assuming } V_{thn} = |V_{thp}| = V_{th})
 \end{aligned}$$

# Power dissipation in a logic circuit

**Consider a logic circuit with ‘N’ number of logic gates.**

**Dynamic energy dissipation per transition per gate:**  $C_L V_{DD}^2$

**Short-circuit energy diss. per transition per gate:**  $E_{SC}$

**Assume:**  $T_{CLK} \gg$  delay of a single gate

**Assume:** ‘m’ number of gates switches per clock cycle

*Total energy dissipated in a cycle:*

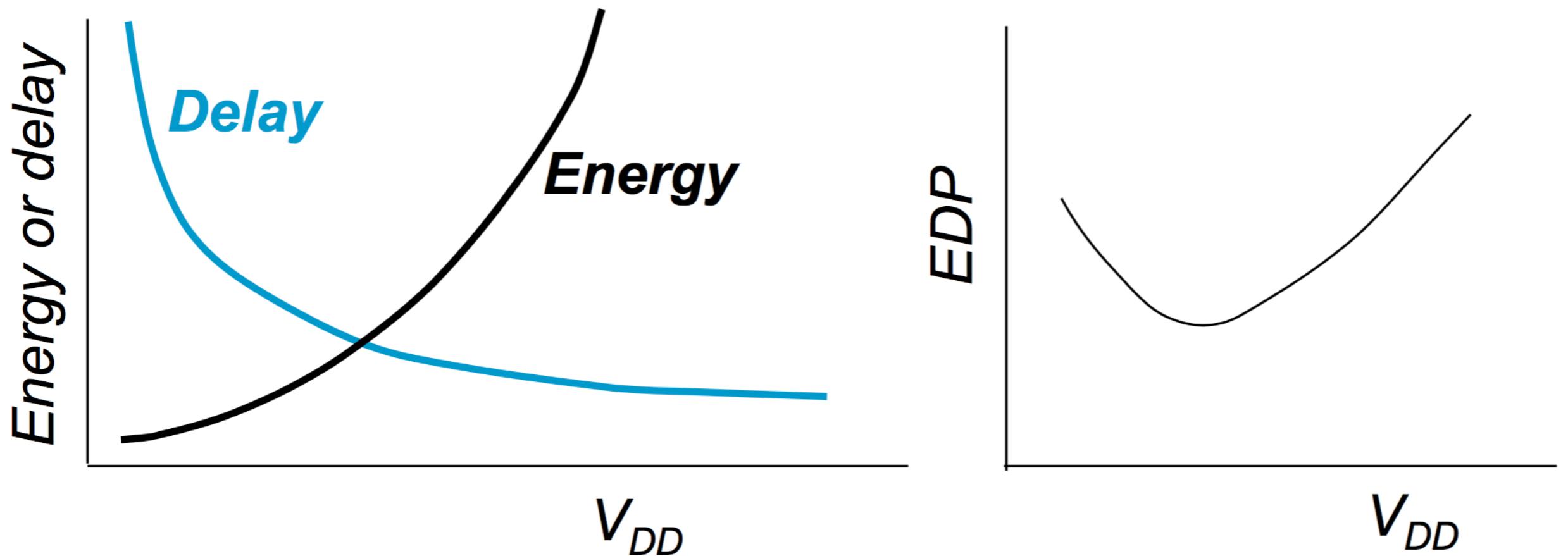
$$E_{Total} \sim mC_L V_{DD}^2 + mE_{SC} + NV_{DD}I_{static}T_{CLK}$$

*Average power dissipation per gate per cycle :*

$$P_{avg} = \frac{E_{Total}}{NT_{CLK}} = \alpha C_L V_{DD}^2 f_{CLK} + \alpha E_{SC} + V_{DD} I_{static}$$

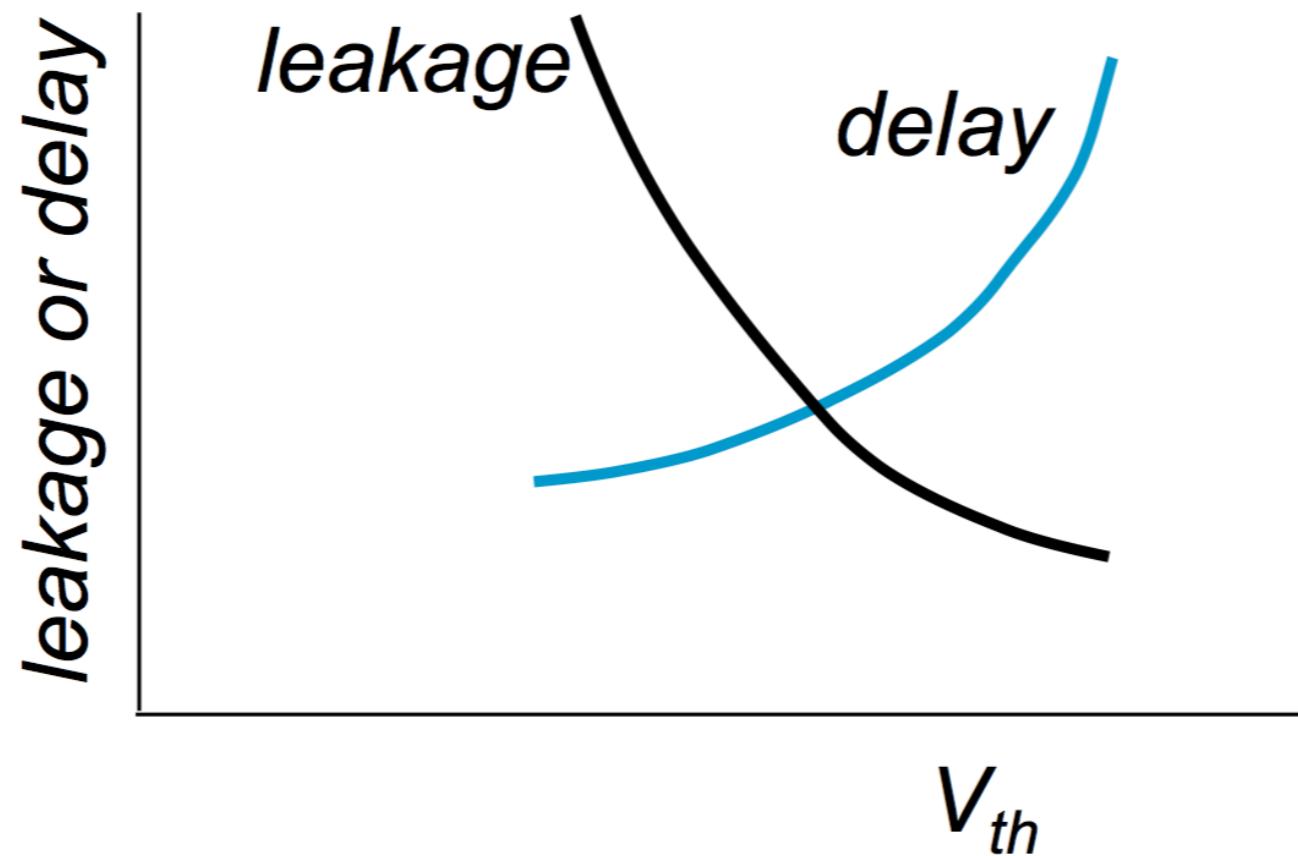
$\alpha$  = activity factor = frac. of gates switches per cycle < 0.1

# Dynamic energy-delay interaction



$$EDP = C_L V_{DD}^2 \times \frac{C_L}{\beta V_{DD}} \frac{1}{(1 - V_{th}/V_{DD})^2} = \frac{C_L^2 V_{DD}}{\beta} \frac{1}{(1 - V_{th}/V_{DD})^2}$$

# Static energy-delay interaction



***Delay reduces at a lower threshold voltage***

***Static energy increases exponentially at a lower threshold voltage***

# Design challenge for low-power/high-performance

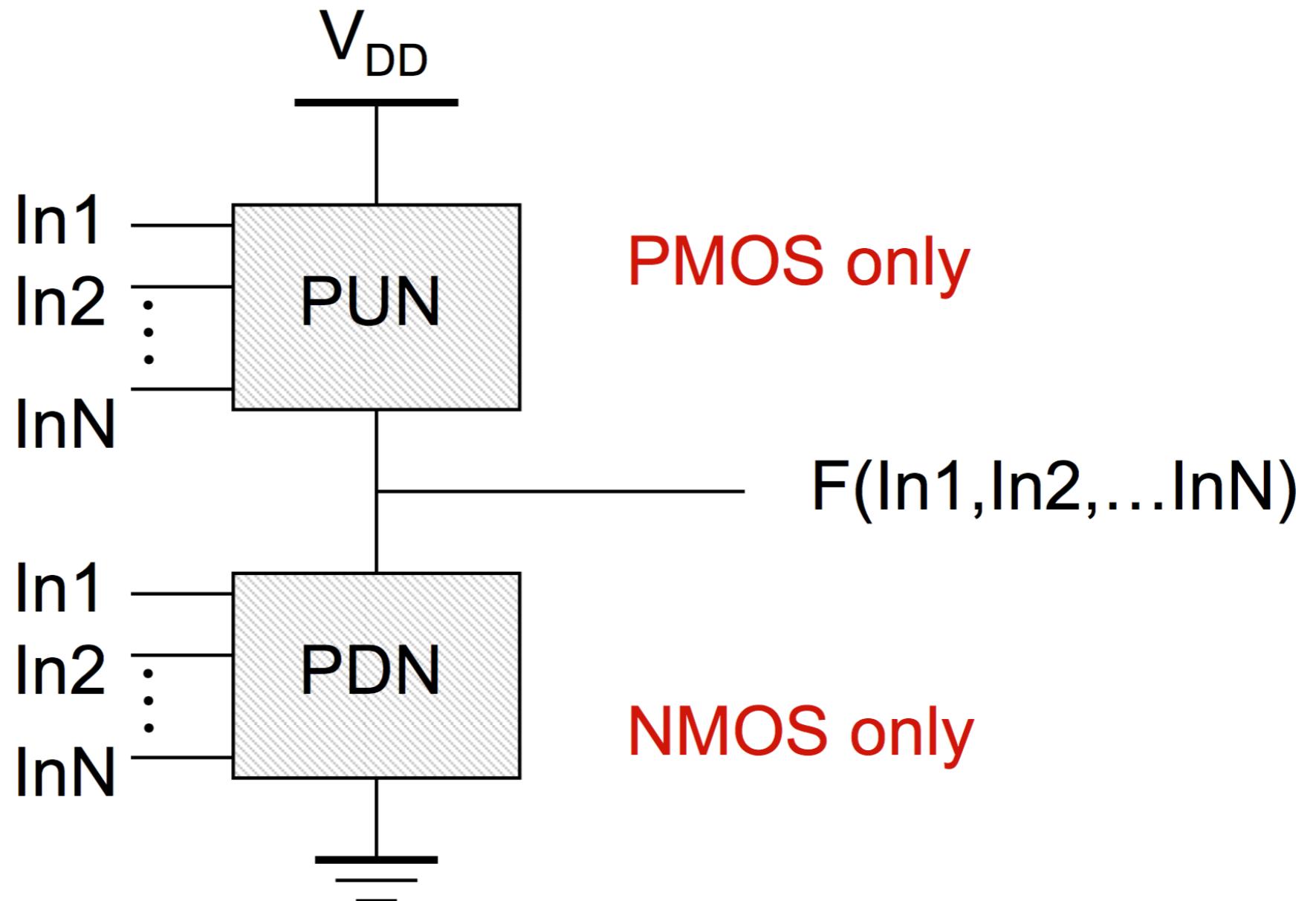
- ***The most efficient method of reducing power is to reduce supply voltage***
- ***A lower supply voltage increases the delay.***
- ***The delay can be improved by using devices with lower  $V_{th}$ .***
- ***A lower threshold voltage exponentially increases the subthreshold leakage and static power***
- ***Managing all of the above three requires innovative device, circuit, and system design methods.***

# Introduction to CMOS Logic gates

# CMOS logic devices

- **Static CMOS logic gates**
  - simple logic gates - NAND and NOR
  - Constructing complex gates
- **Principles for better performance**
- **Logical effort**
  - Concept and applications

# CMOS logic devices

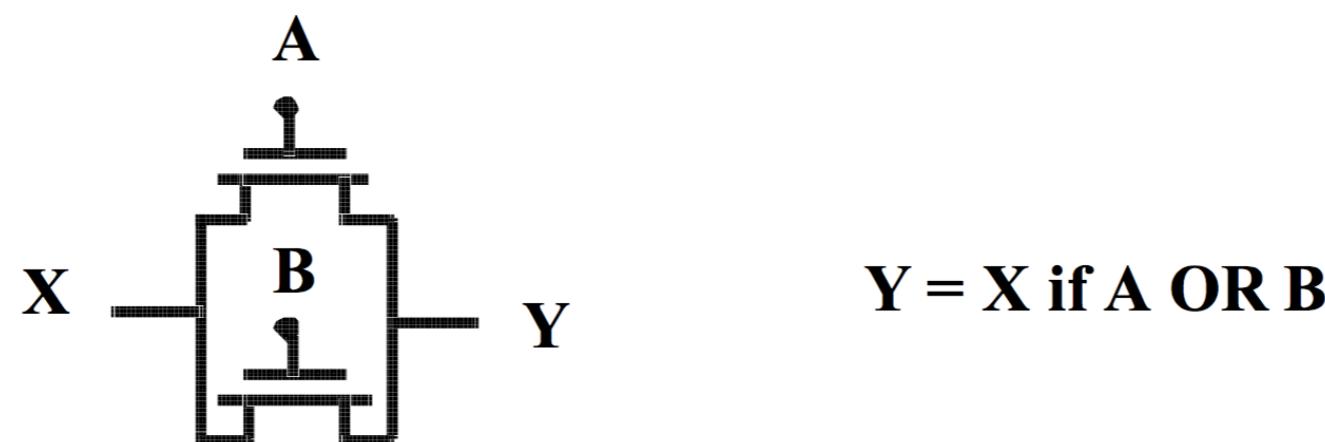


PUN and PDN are **dual** logic networks

# NMOS transistors in series and parallel

Transistors can be thought as a switch controlled by its gate signal

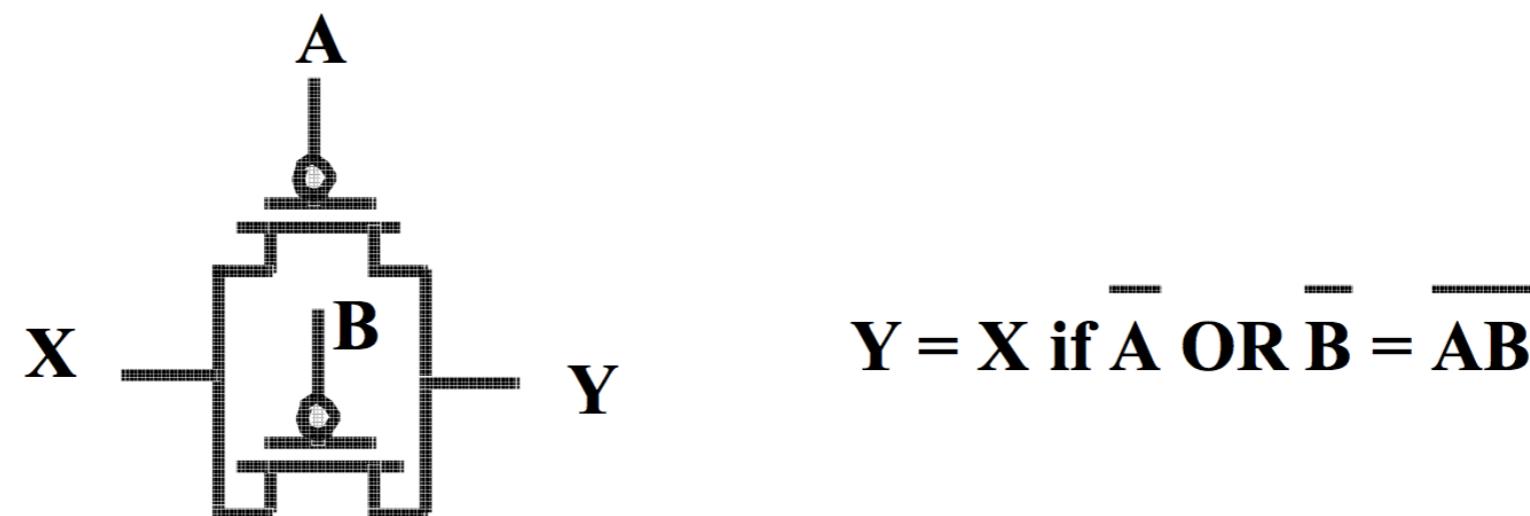
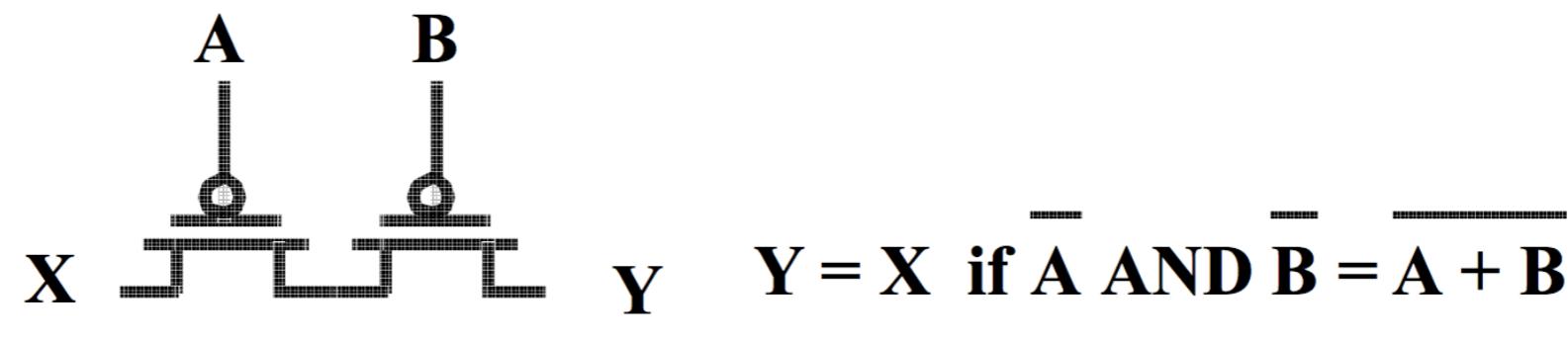
NMOS switch closes when switch control input is high



NMOS Transistors pass a “strong” 0 but a “weak” 1

# PMOS transistors in series and parallel

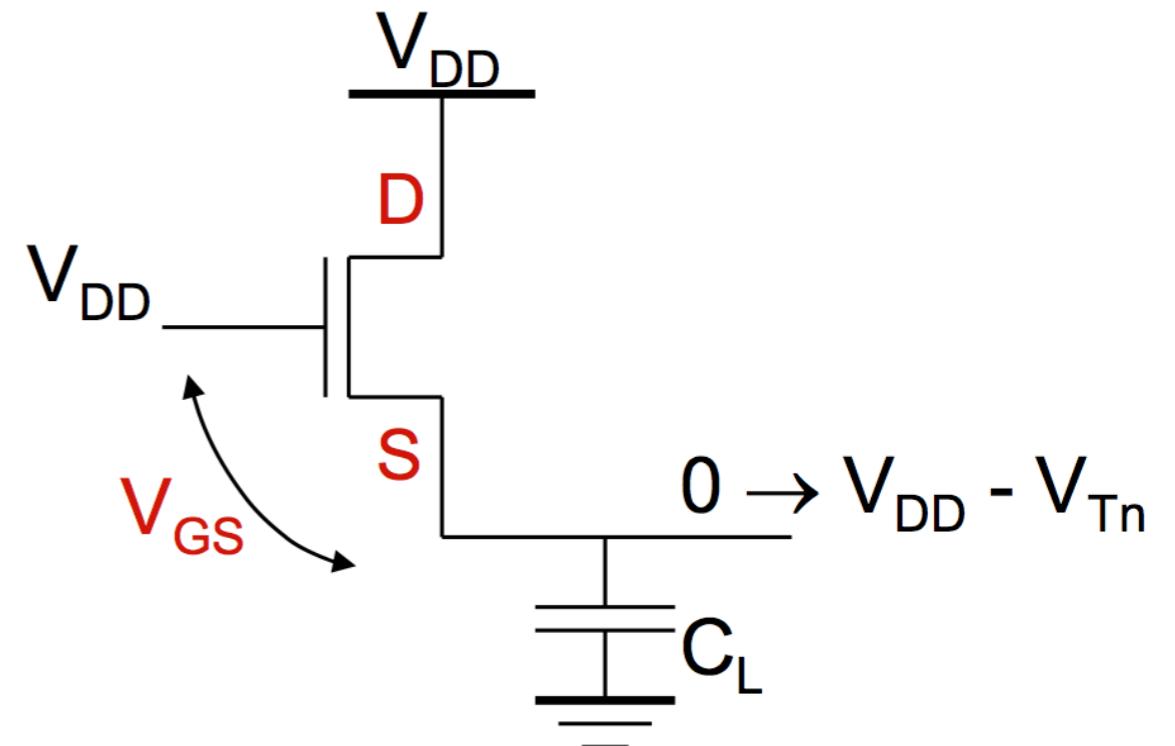
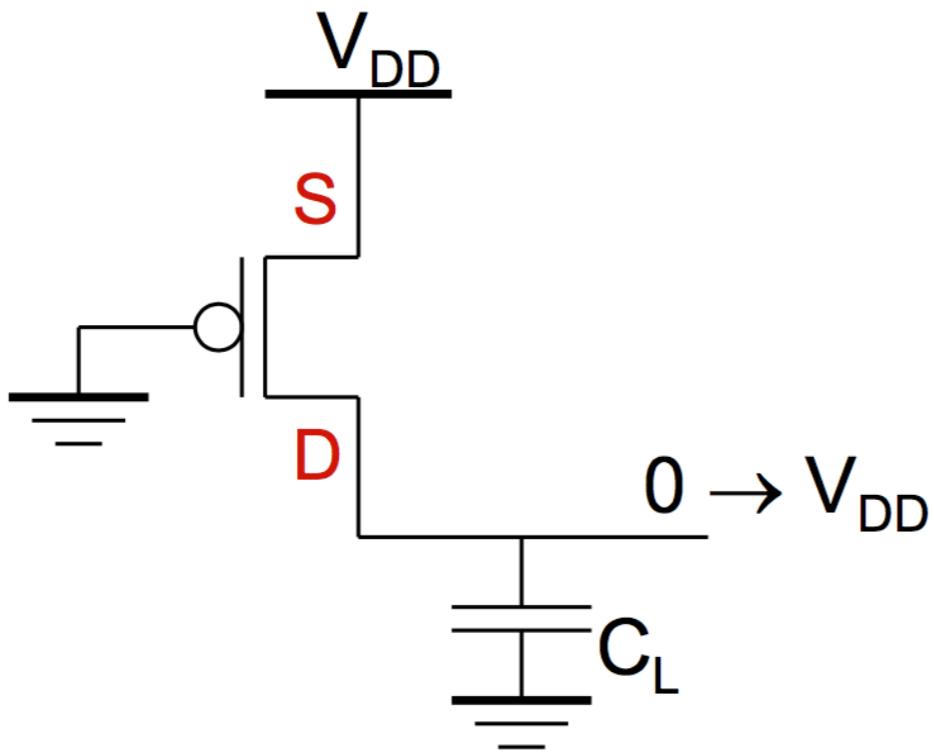
**PMOS switch closes when switch control input is low**



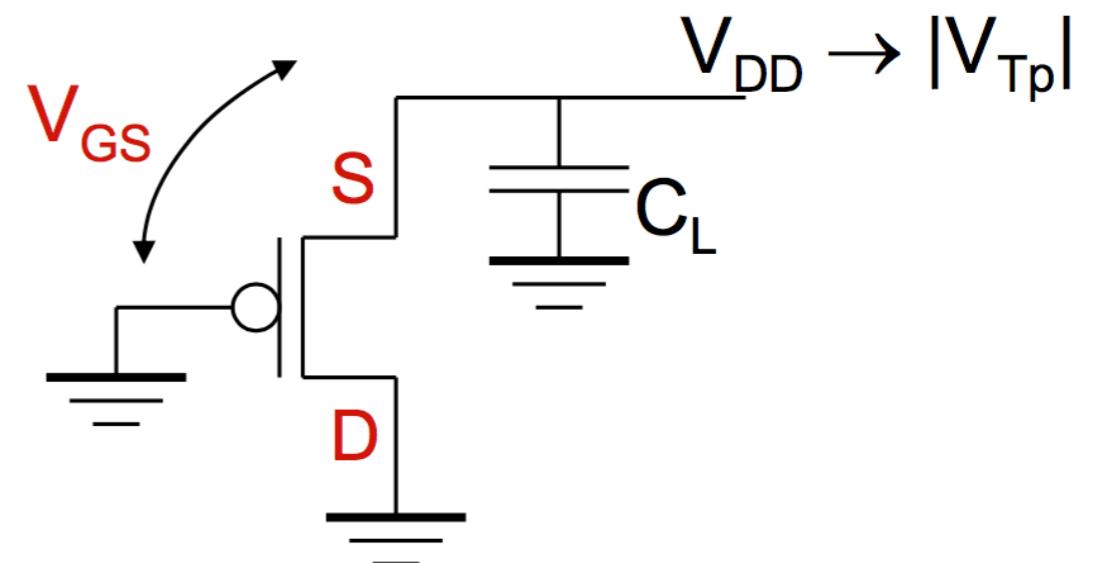
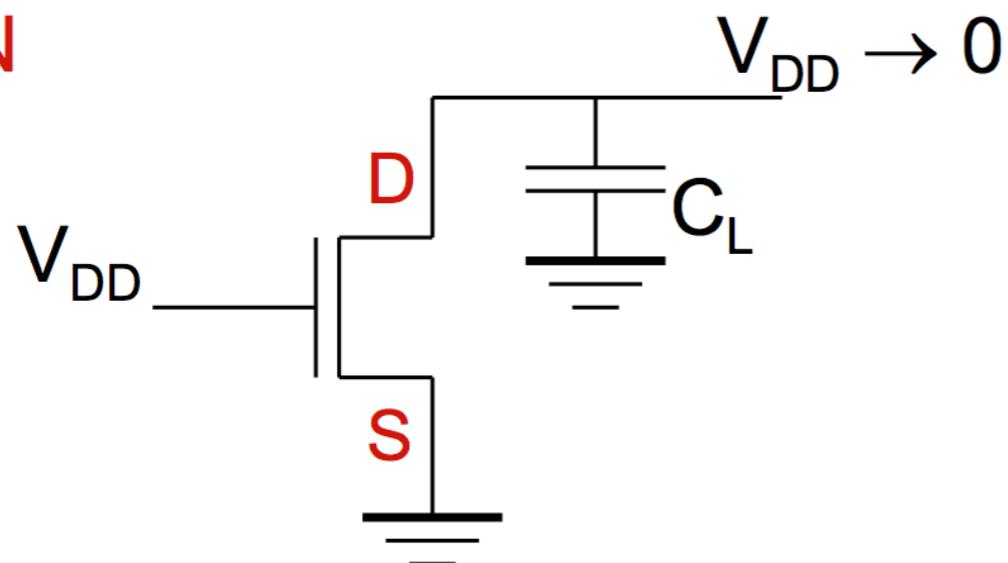
**PMOS Transistors pass a “strong” 1 but a “weak” 0**

# Threshold voltage drops

PUN



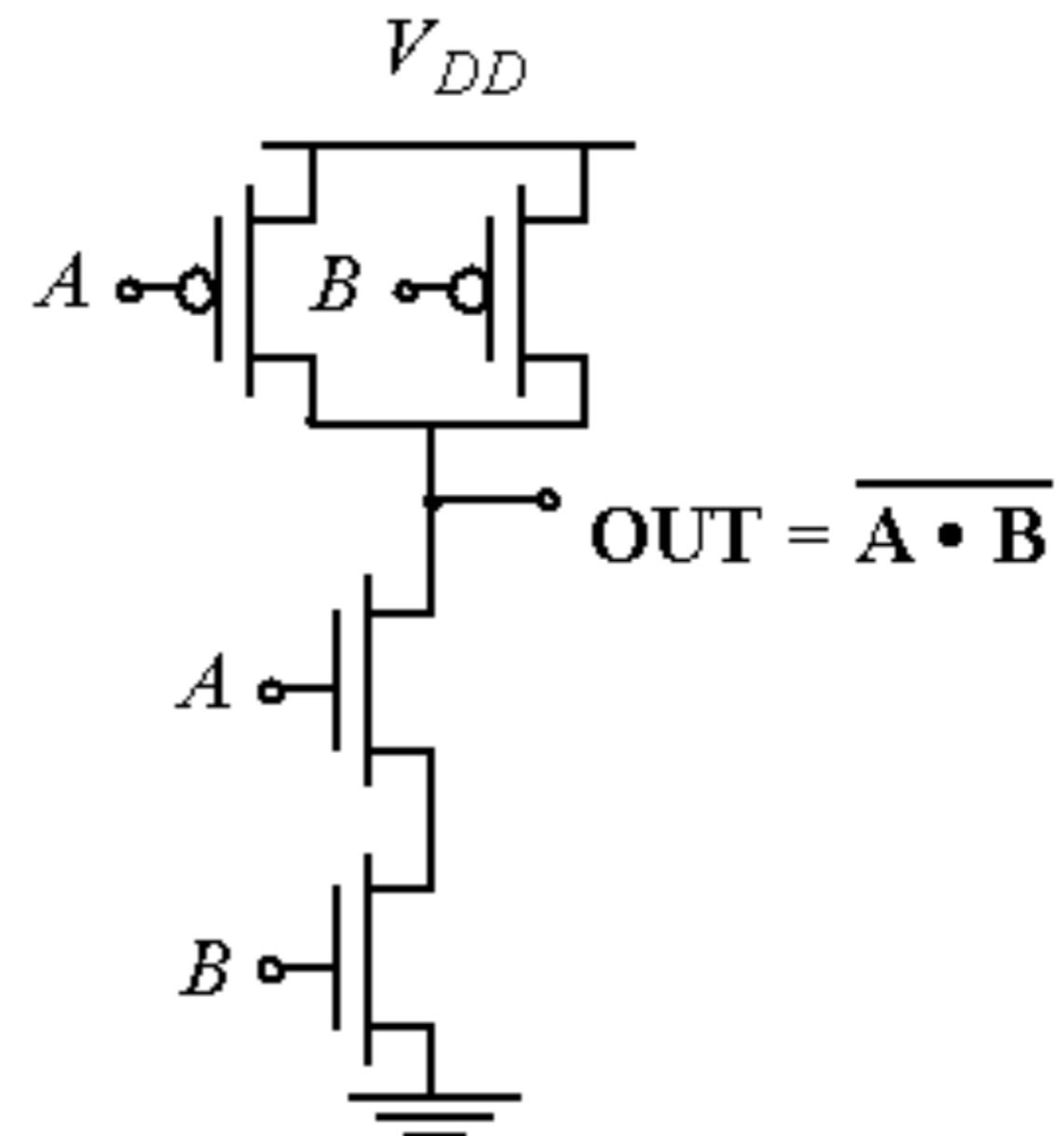
PDN



# CMOS NAND gate

A	B	Out
0	0	1
0	1	1
1	0	1
1	1	0

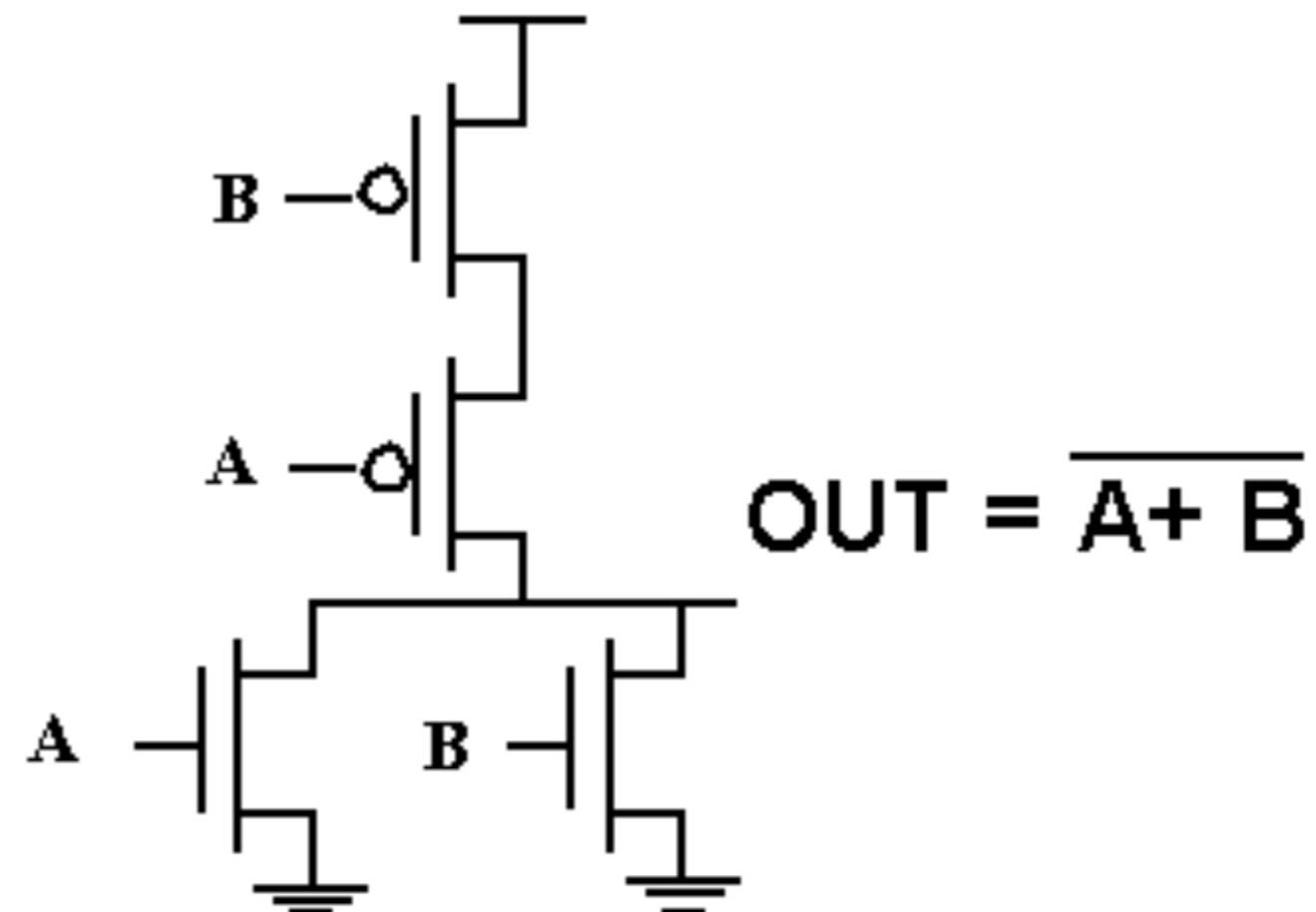
**Truth Table of a 2 input NAND gate**



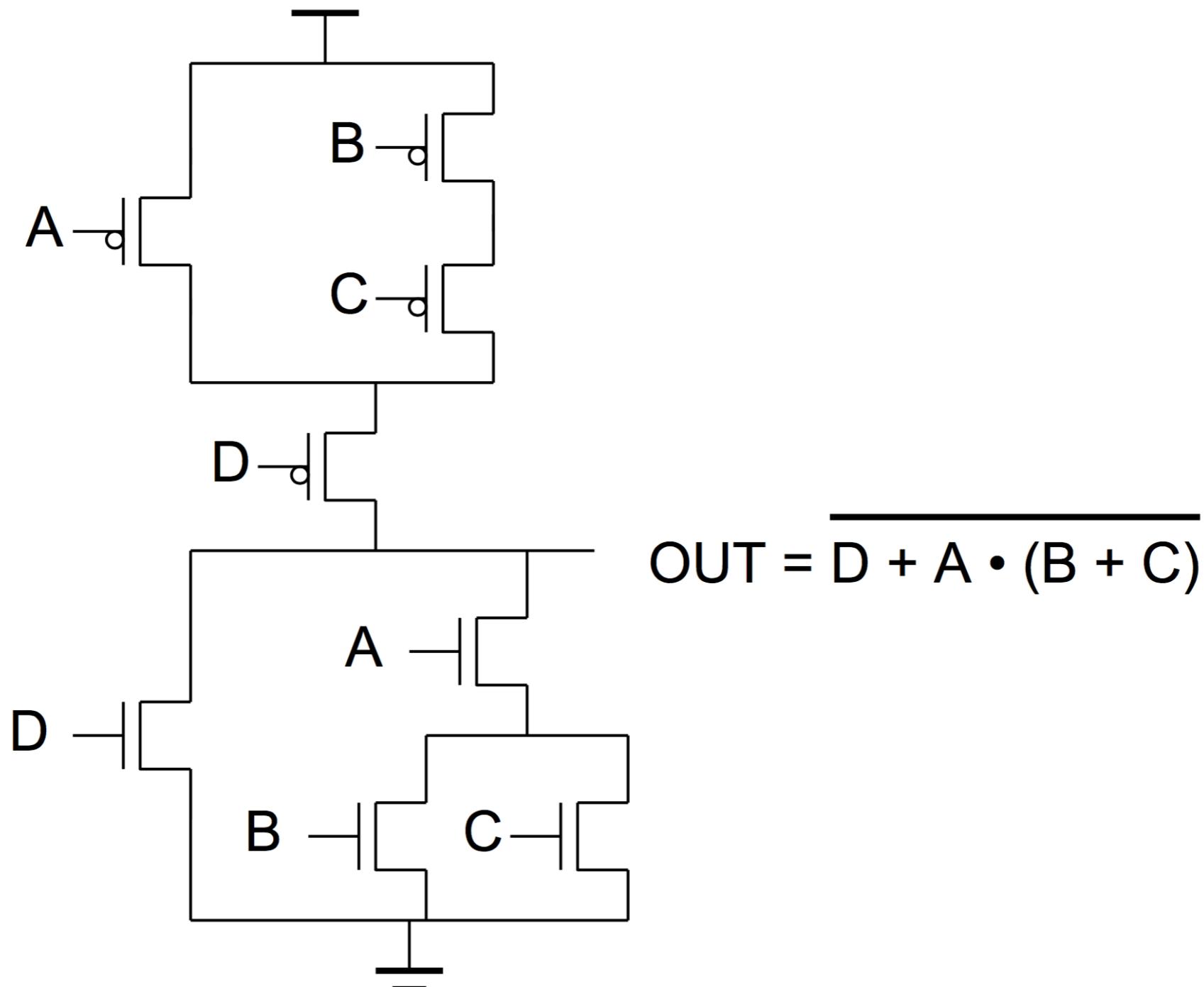
# CMOS NOR gate

A	B	Out
0	0	1
0	1	0
1	0	0
1	1	0

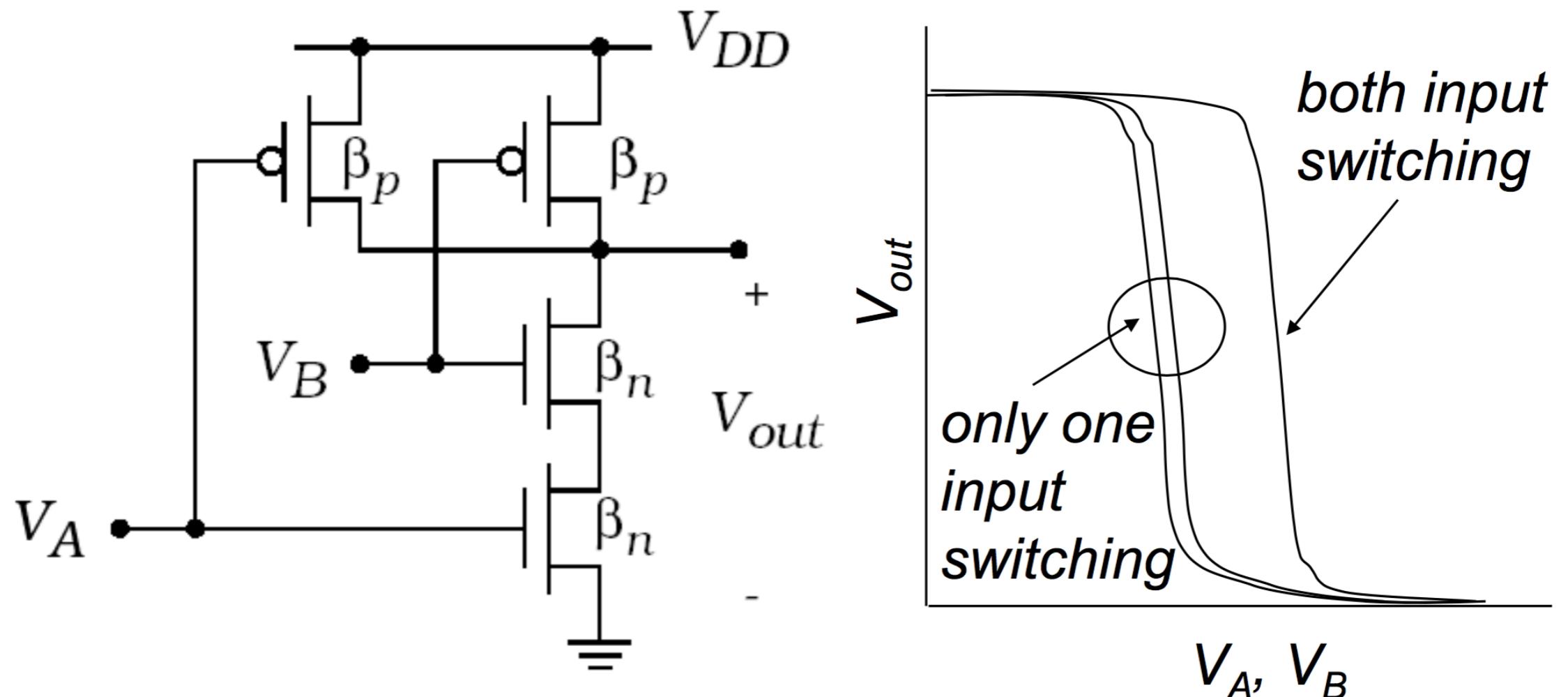
Truth Table of a 2 input NOR gate



# Complex CMOS logic gate

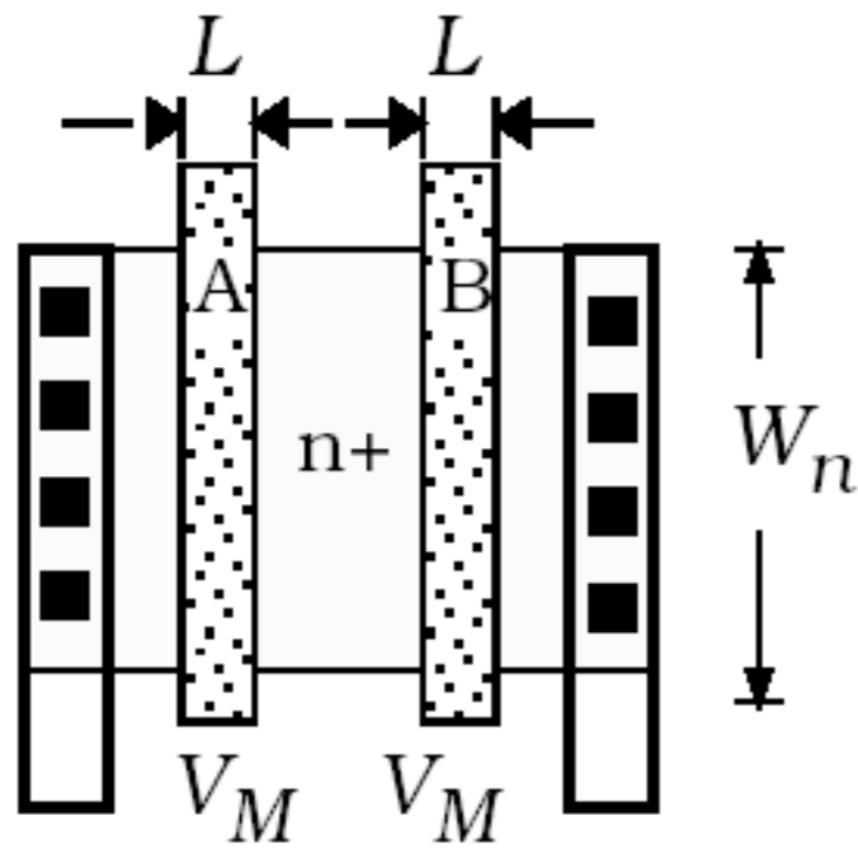


# Voltage transfer characteristics: NAND



If both inputs switches from 0 to  $V_{DD}$ , switching threshold is higher as both PMOS's are initially ON

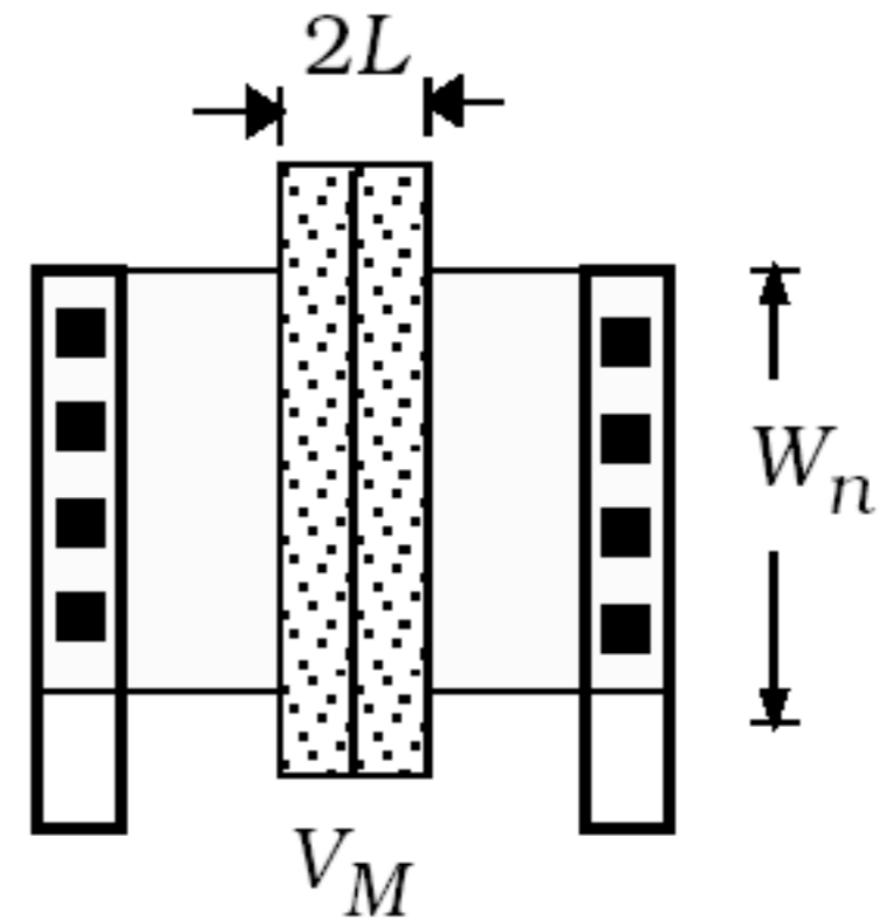
# Simplification series connected transistors



(a) Separate transistors

*Two devices with*

$$\beta = \left( \frac{W}{L} \right) \mu C_{ox}$$

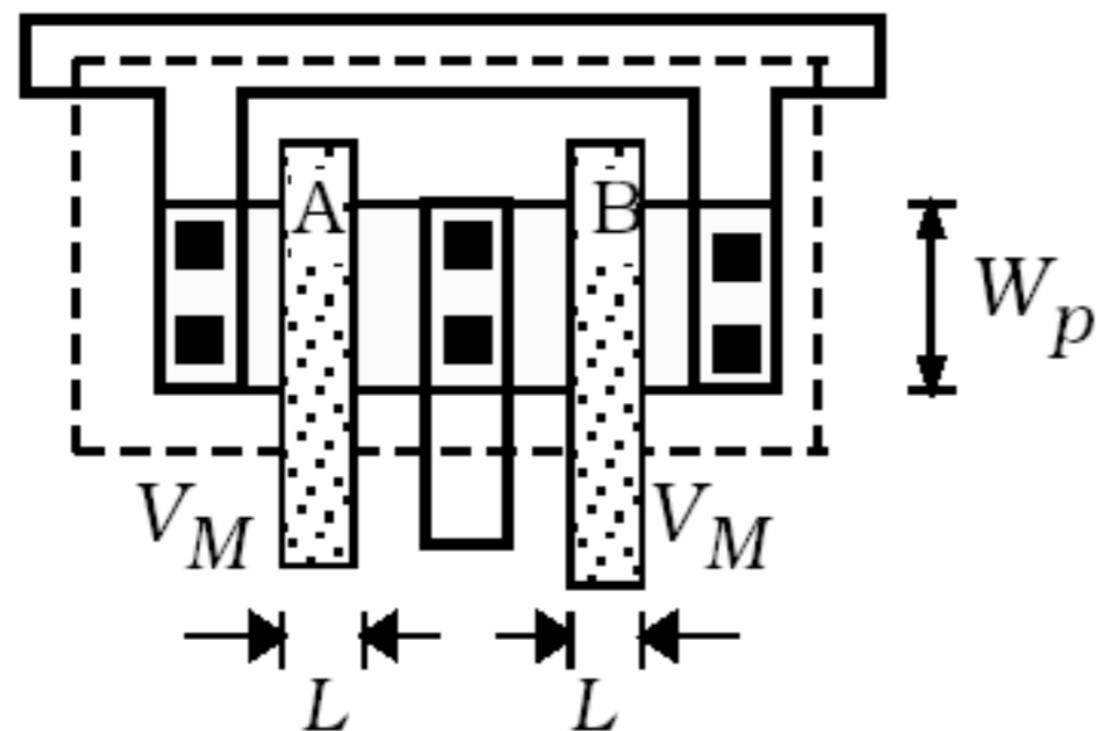


(b) Single equivalent FET

*Single device with*

$$\beta^{(1)} = \left( \frac{W}{2L} \right) \mu C_{ox} = \frac{\beta}{2}$$

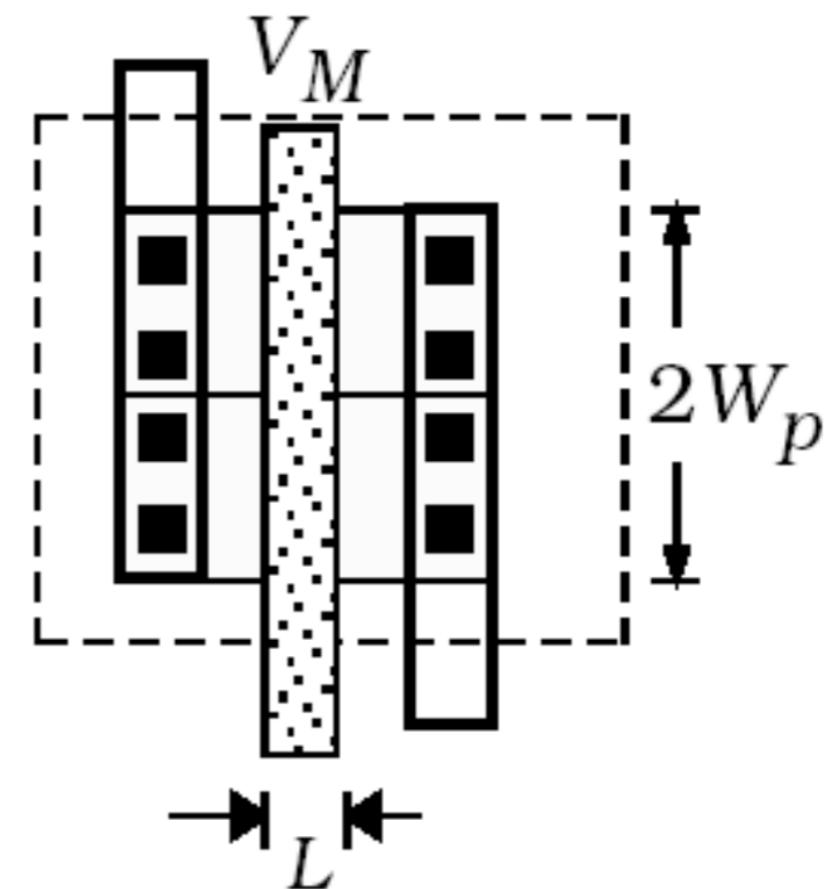
# Simplification parallel connected transistors



(a) Separate transistors

*Two devices with*

$$\beta = \left( \frac{W}{L} \right) \mu C_{ox}$$

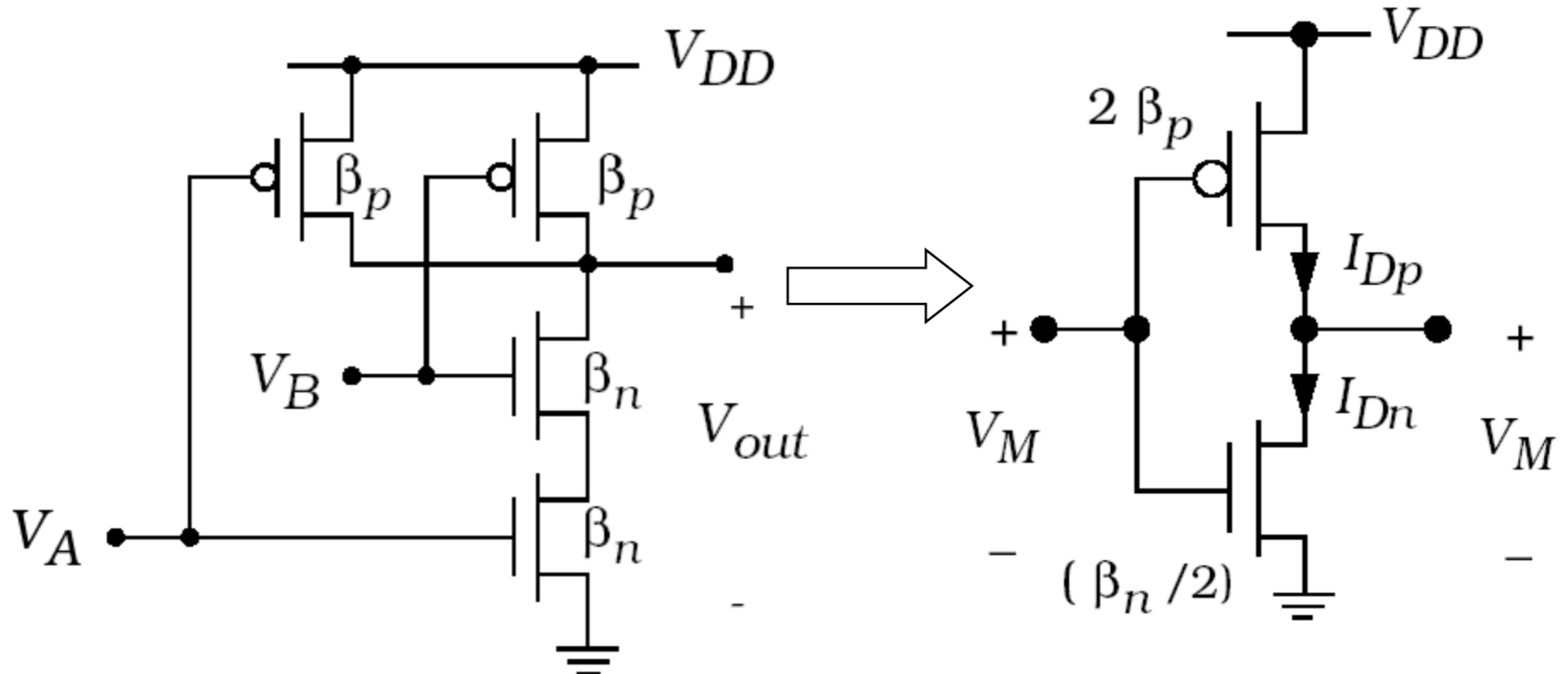


(b) Single equivalent FET

*Single device with*

$$\beta^{(1)} = \left( \frac{2W}{L} \right) \mu C_{ox} = 2\beta$$

# Switching threshold of NAND gate: simultaneous switching of inputs



$$V_M = \frac{V_{DD} - |V_{thp}| + (1/2)\sqrt{\beta_n/\beta_p} V_{thn}}{1 + (1/2)\sqrt{\beta_n/\beta_p}}$$

# Next class on 01/05/2015

- Recap from 09/28/2015
  - Sizing a chain of inverters
  - Inverter power dissipation
- Designing CMOS NAND and NOR gates for performance
- Logical effort
- Physical design (basics of layout)