ECE 6473
Homework # 4
Assigned Date: 10/20/2015
Due Date: 10/28/2015
Collaboration on the homework in not allowed.

Grading:
Problem 1: 10 points
Problem 2: 60 points
Problem 3: 30 points

For all CADENCE simulations below, use the following parameters:

V_{DD} = 1.2V Rise time of signal = fall time of signal = 10 ps Load capacitance at output node = 5 fF

Problem 1: Cadence design of reference inverter using FreePDK45
In class we studied the reference inverter circuit. A reference inverter is the minimum-sized inverter for a given technology node that has balanced pull-up and pull-down networks.

Use the minimum-sized NMOS allowed by FreePDF45 (W_n/L_n = 90 nm/50 nm). Then make PMOS width bigger than the NMOS width until low-to-high and high-to-low delays are matched. Keep the lengths of both NMOS and PMOS at 50 nm, which is the minimum allowed by the technology. Lets say, the reference inverter is now sized such that $(W_p/W_n) = r$, where $r > 1$.

a. Find "r" for FreePDK45 such that $t_{pLH} = t_{pHL}$ for the inverter. In your homework solution, attach the simulation result from Cadence and note the value of "r" and the values of t_{pLH} and t_{pHL}. In fact, you have already done this simulation in HW-2, but many of you did not realize that you were designing the reference inverter. **(10 points)**

Problem 2. Cadence design of NAND2 and NOR2 gates using FreePDK45
Now design two-input NAND2 and NOR2 gates with properly sized transistors that give you same low-to-high and high-to-low delays as the reference inverter. This means for NAND2 you will use PMOS the same size as in the reference inverter, but NMOS devices will be double that of reference inverter. For NOR2, PMOS sizes will be double that of reference inverter, while NMOS size will be the same as reference inverter.

a. Draw the schematic of both NAND2 and NOR2 gates in Cadence. Do not forget to add the load capacitance (5 fF) at the output. Attach the schematic with your homework solution. **(10 points)**

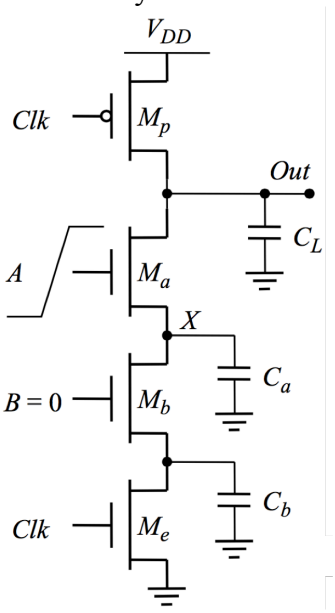
b. Simulate the low-to-high and high-to-low delays of NAND2 and NOR2 circuits for different input patterns. Attach your simulation results from Cadence. **(25 points)**

c. What are the worst-case t_{pLH} and t_{pHL} values for both NAND2 and NOR2 gates? Which of the two circuits NAND2 or NOR2 has the worse worst-case low-to-high and high-to-low delay? You will receive credit only if your Cadence simulations in part (b) show those results. **(10 points)**

d. Do the different input patterns result in different delays? Qualitatively explain your results. **(20 points)**

Problem 3: Charge sharing and timing in dynamic logic

Consider the dynamic circuit as shown in Figure below.



In precharge phase, V(Out) = V_{DD}. Now in evaluate phase, assume signal A makes a transition from "0" to "1". Assume VDD = 2.5V, Vtn = 0.5V. Ignore body effect in this problem.

a. What should the limits on the ratio C_a/C_L be so that the drop in V(out) is limited to between 0.6V and 0.8V ? **(20 points)**

b. Inputs A and B can only make "0" to "1" transition during the evaluate phase. Which of the two input pattern will result in the lower high-to-low delay: (i) A = 1, B = 0 to 1, (ii) B = 1, A = 0 to 1. Justify your answer. You can ignore charge sharing in this part. **(10 points)**