HW-2

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Q1

a

As $V_{GS} = V_{DD} - V_{OH}$ and only when $V_{OH} \leq V_{DD} - V_{Th}$ could guarentee the transistor is turned on. And the maximum value is the output voltage before t = 0.

$$\begin{aligned} V_{OH} &= V_{DD} - V_{Th} \\ &= V_{DD} - V_{T0} - \gamma(\sqrt{2|\phi_F| + V_{OH}} - \sqrt{2|\phi_F|}) \\ &= 1.8(V) \end{aligned} \tag{1}$$

b

As informed in the question, V_{Th} is constant and is the average of its maximum and minimum, which is

$$\begin{aligned} V_{Th} &= V_{T0} + \frac{1}{2}\gamma(\sqrt{2|\phi_F| + V_{OH}} + \sqrt{2|\phi_F| + V_{OH}/2}) - \gamma\sqrt{2|\phi_F|} \\ &= 0.67(V) \end{aligned} \tag{2}$$

As $V_{out} = V_{OH} \rightarrow V_{OH}/2$, $V_{DS} = V_{DD} - V_{OH} \rightarrow V_{DD} - V_{OH}/2$. Thus,

$$\begin{aligned} R_{eq} &= \frac{1}{2}\left[\frac{V_{DD} - V_{OH}}{\frac{1}{2}\kappa(V_{DD} - V_{OH} - V_{Th})^2} + \frac{V_{DD} - V_{OH}/2}{\frac{1}{2}\kappa(V_{DD} - V_{OH}/2 - V_{Th})^2}\right] \\ &= \frac{V_{DD} - V_{OH}}{\kappa(V_{DD} - V_{OH} - V_{Th})^2} + \frac{V_{DD} - V_{OH}/2}{\kappa(V_{DD} - V_{OH}/2 - V_{Th})^2} \\ &= 6.8 \times 10^6(\Omega) \end{aligned} \tag{3}$$

c

When $t \rightarrow \infty$,

$$\begin{aligned} V_{out} &= I_{DSAT}R_{SW} \\ &= \frac{1}{2}\kappa[V_{DD} - V_{out} - V_{T0} - \gamma(\sqrt{2|\phi_F| + V_{out}} - \sqrt{2|\phi_F|})]^2 R_{SW} \end{aligned} \tag{4}$$

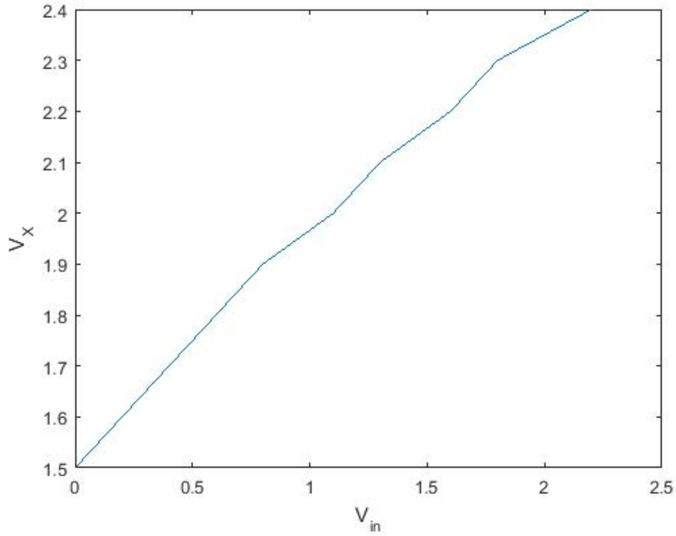

Figure 1: Q2_a

Q2

$$\begin{aligned} V_X =& V_{DD} - I_{SD}R_1 \\ =& V_{DD} + \frac{1}{2}\kappa\frac{W}{L}(V_X - V_{in} + V_{T0})^2(1+\lambda V_X)R_1 \end{aligned} \tag{5}$$

a

See Figure 1.

b

$$\frac{W}{L} = 1.1 \tag{6}$$

Q3

a

It is clear that $V_{X,max} = V_{DD} - V_{Th}$. And

$$\begin{aligned} V_{Th} &= V_{T0} + \frac{1}{2}\gamma(\sqrt{2|\phi_F| + V_{X,max}/2} - \sqrt{2|\phi_F|}) \\ &= 0.53(V) \end{aligned} \tag{7}$$

Thus, $V_{X,max} = 1.97(V)$. As well as

$$
\begin{aligned}
R_{eq} =& \frac{1}{2} R_{eq,max} \\
=& \frac{V_{DD} - \frac{V_{X,max}}{2}}{\kappa \frac{W}{L}(V_{DD} - V_{X,max}/2 - V_{Th})^2[1 + \lambda(V_{DD} - V_{X,max}/2)]} \\
=& 829.7861(\Omega)
\end{aligned}
\tag{8}
$$

Thus,

$$
\begin{aligned}
t_{pLH} &= R_{eq} C_L ln \frac{V_{DD}}{V_{DD} - V_{out}} \\
&= R_{eq} C_L ln \frac{2V_{DD}}{V_{DD} + V_{Th}} \\
&= 2.0781(ns)
\end{aligned}
\tag{9}
$$

b

$$
\begin{aligned}
\Delta t_{pLH} &= 0.69 R_{eq} C_0 W_0 \\
&= t_0
\end{aligned}
\tag{10}
$$

c

$$
\begin{aligned}
t_{pHL} &= 0.69 R C_L \\
&= 17.25(ns)
\end{aligned}
\tag{11}
$$

d

With $\beta_n = \beta_p$, and $|\gamma_n| = |\gamma_p|$ with $|\lambda_n| = |\lambda_p|$ from the table coming with questions. $\frac{t_{pLH,n}}{t_{pLH,p}}$ becomes,

$$
\begin{aligned}
\frac{t_{pLH,n}}{t_{pLH,p}} &= \frac{R_{eq,n}}{R_{eq,p}} \frac{ln \frac{2V_{DD}}{V_{DD}+V_{Tn}}}{ln \frac{2V_{DD}}{V_{DD}+V_{Tp,0}}} \\
&= \frac{(V_{DD} + V_{Tn})(V_{DD} - V_{Tp,0})^2[1 + \frac{1}{2}\lambda_p(V_{DD} + V_{Tp,0})] ln \frac{2V_{DD}}{V_{DD}+V_{Tn}}}{(V_{DD} + V_{Tp,0})(V_{DD} - V_{Tn})^2[1 + \frac{1}{2}\lambda_n(V_{DD} + V_{Tn})] ln \frac{2V_{DD}}{V_{DD}+V_{Tn}}} \\
&= 1.3001
\end{aligned}
\tag{12}
$$

Which means, using PMOS will make it a bit faster.

Q4

As how to use HSPICE is not taught, and therefore no tutorial was given. And this is the first time ever I've such a program, which means there is no way I could know how to use it before hand. I can only use what I can see from netlist figures.

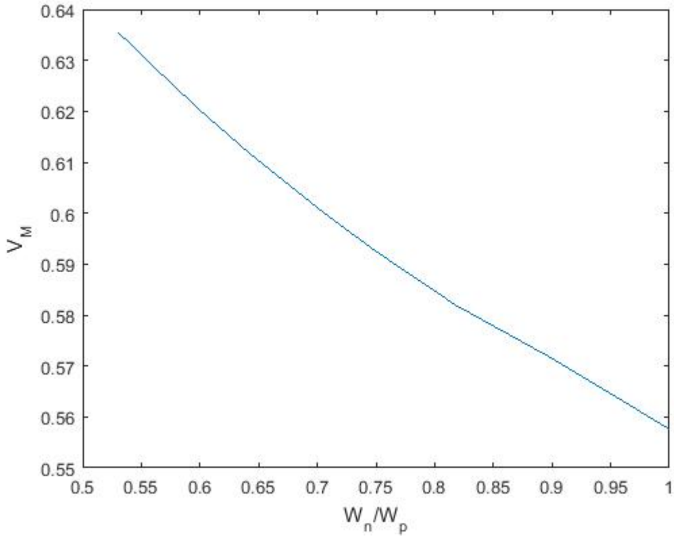

Figure 2: Q4_a

a

For $V_M = 0.5V_{DD}$, $\frac{W_n}{W_p} = \frac{90}{127.50575} \approx \frac{90}{127.5}$.

90/90	0.5576
90/100	0.5715
90/110	0.5819
90/120	0.5925
90/127.5	0.6
90/140	0.6116
90/150	0.6202
90/160	0.6283
90/170	0.6357

b

See Figure 3.
For high-to-low delay equals low-to-high delay, $\frac{W_n}{W_p} = \frac{90}{135.75}$.

c

See Figure 4.

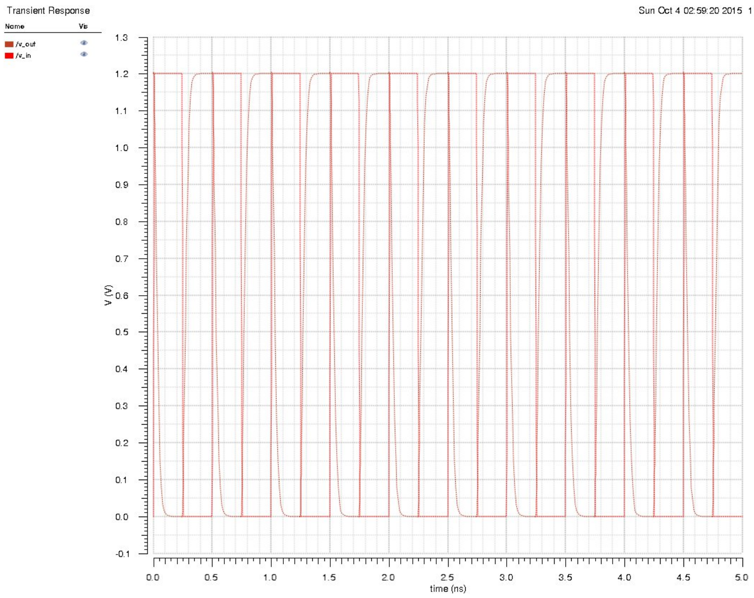

Figure 3: Q4_b

D_input(ps)	t_pHL(ps)	t_pLH(ps)
0.1	27	27
50	32	27
100	39	27
150	44	27
200	48	27
500	65	27

Quite clear that high-to-low delay is positively related with input rise time. And in fact it is still a fuction of input.

d

Except for high-to-low delay increased to 67ps, I saw no suspicious things. And here is my paramiters:

PMOS	L	50nm
	W	542.8nm
NMOS	L	50nm
	W	90nm
V_dd		1.2V
V_in	rise time	200ps
	fall time	10ps
	pulse width	235ps
	period	880ps
	voltage 1	0V
	voltage 2	1.2V
Cap		5fF

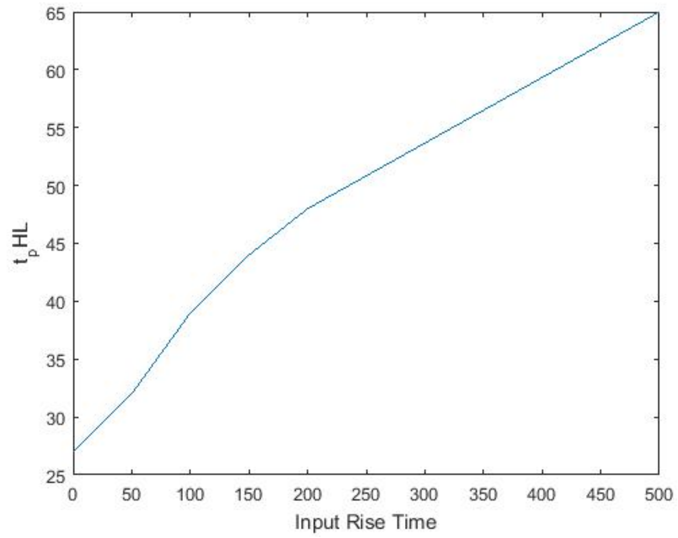

Figure 4: Q4_c

e

For what I got, it is the same as the result from part (b). And have no conflict with part(c).

$$
\begin{aligned}
\frac{t_{pHL}}{t_{pLH}} &= \frac{R_n}{R_p} \\
&= \frac{I_{DSAT,p}(1 - \frac{7}{9}\lambda_n V_{DD})}{I_{DSAT,N}(1 - \frac{7}{9}\lambda_p V_{DD})} \\
&= \frac{\kappa_p W_p (V_{DD} - V_{T0})^2 (1 - \frac{7}{9}\lambda_n V_{DD})}{\kappa_n W_n (V_{DD} - V_{Tn})^2 (1 - \frac{7}{9}\lambda_p V_{DD})}
\end{aligned}
\tag{13}
$$

Thus the ratio has nothing to do with input rise/fall time. But, ofcourse, signal frequency become too high, output will go wild.