

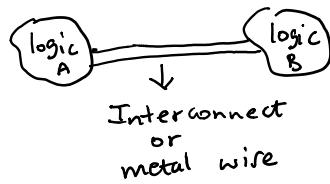
Interconnects

Sunday November 22 2015 3:05 PM

Interconnects are metal wires atop a dielectric on the chip that communicate information between different points on the chip.

So far we have considered only the delay of different logic gates and assumed that the wires are perfect.

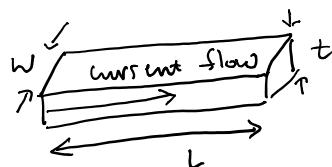
In reality, wires add delay to circuits, jitter and increase energy consumption of the chip. In a modern microprocessor, interconnects take up >50% power.



In real life, metal wires have finite resistance, Capacitance, & inductance. These R-L-C components are often referred to as wire parasitics. These are unwanted in any circuit. For an accurate timing analysis of the circuit, we must include wire parasitics. For this class, we will only consider the wire resistance & wire capacitance but ignore wire inductance. This is an OK approximation for low frequencies where resistance dominates inductive effects.

Resistance

$$R = \rho \frac{L}{A}$$



ρ = wire resistivity $\Omega \cdot m$

L = length (along the direction of current flow)

A = cross-sectional area $\{m^2\}$

$$A = wt$$

$$R = \frac{\rho L}{wt} = \left(\frac{\rho}{t}\right) \left(\frac{L}{w}\right)$$

$\{\Omega\}$ $\Omega \cdot m^2$ sheet resistance $\{\Omega\}$

$$R = R_{\text{sheet}} \left(\frac{L}{w}\right)$$

Fixed for a technology.

Decided upon Fabrication.
Typically as a designer,
you cannot change R_{sheet} .
What is really important to us is

$$R = \left(\frac{R_{sheet}}{W} \right) L$$

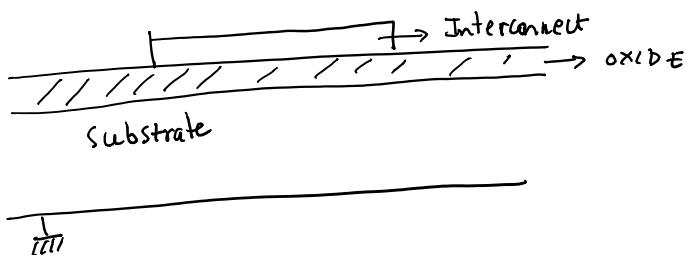
'r' → wire-resistance
per unit length

$R_{wire} = rL$ → as 'L' increases, R_{wire} increases.

∴ if two logic blocks are
far apart and the
wire length between them is long,
you will increase wire resistance
and the signal will be delayed.

Capacitance

Interconnects sit on top of a dielectric on a substrate



So there are two kinds of capacitances we must consider for the interconnect

- (a) Parallel-plate capacitance
- (b) Fringing-field capacitance

$$C_{parallel-plate} = \frac{\epsilon_{ox} WL}{t_{ox}}$$

If the wire length is long then $C_{parallel-plate} \uparrow$

Ideally we don't want any wire capacitance, so having a long wire is not a good idea.

Also as $W \uparrow C_{parallel-plate} \uparrow$
for the case of resistance as $W \uparrow r \downarrow$ } imp. difference.

Making a wire fat helps lower resistance but

tor the case + - -

Making a wire fat helps lower resistance but unfortunately increases capacitance!

Finally, we can put both parallel-plate and fringing capacitances together and simply write :-

$$C_{\text{wire}} = C L \rightarrow \text{as } L \text{ increases } C_{\text{wire}} \uparrow$$

Bottomline :- A wire will be represented by its per-unit-length resistance and capacitance values.

$$R_{\text{wire}} = r L \quad C_{\text{wire}} = C L$$

Do not forget that 'r' is simply $r = \frac{\rho}{A t}$ \rightarrow resistivity
Cross-sectional area

Typical (300 K) resistivities of metals

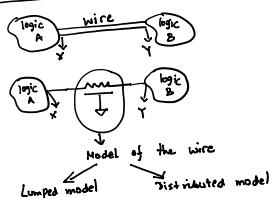
Silver $1.59 \times 10^{-8} \Omega \cdot \text{m} \rightarrow$ Best but too expensive to use in microprocessors

Copper $1.68 \times 10^{-8} \Omega \cdot \text{m}$

Copper (annealed) $1.72 \times 10^{-8} \Omega \cdot \text{m} \swarrow$ This is what we use in ICs.

Aluminum $2.65 \times 10^{-8} \Omega \cdot \text{m}$

Equivalent circuit representation of wires



Lumped model
In the lumped model, we basically just replace the wires with their entire capacitance and resistance at one node in the circuit.

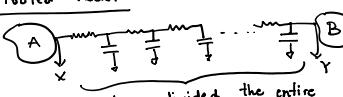


The above is a lumped wire circuit.
The delay of signal from X to Y is given as

$$t_{XY} = 0.69 R_{\text{wire}} C_{\text{wire}} = 0.69 r c L^2$$

It turns out that lumped model is a very pessimistic model.
This means that according to lumped model, the delay t_{XY} is more than it actually is in reality.

Distributed Model

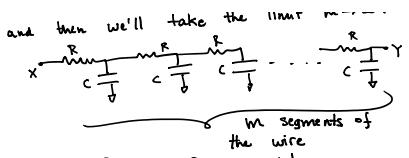


We have divided the entire length of the wire into several segments. Each segment is now represented using an RC equivalent circuit.

The question is how many segments?

Answer :- Infinite !!!

Let's say we divide the wire into 'm' segments.



What is R ? $R = \frac{R_{\text{wire}}}{m} \rightarrow \text{total}$

What is C ? $C = \frac{C_{\text{wire}}}{m} \rightarrow \text{total}$

$$t_{XY} = 0.69 \left[RC + 2RC + 3RC + \dots + mRC \right]$$

$$= 0.69 \left[1 + 2 + 3 + \dots + m \right] RC$$

↓
Recall: $\sum_{n=1}^m n = \frac{m(m+1)}{2}$

$$= \frac{0.69}{2} \left[m(m+1) \right] \frac{R_{\text{wire}} C_{\text{wire}}}{m^2}$$

$$t_{XY} = \frac{0.69}{2} R_{\text{wire}} C_{\text{wire}} \left[\frac{m(m+1)}{m^2} \right]$$

Now let's take the limit $m \rightarrow \infty$

$$\lim_{m \rightarrow \infty} \frac{m(m+1)}{m^2} \rightarrow 1$$

$$\boxed{t_{XY} = \frac{0.69}{2} R_{\text{wire}} C_{\text{wire}} = 0.69 \text{rcL}^2}$$

Note that the distributed model says the delay of the signal in going from X to Y is $\frac{0.69}{2} \text{rcL}^2$. This is half of the lumped delay model.

For an even more accurate analysis, one must solve the voltage diffusion equation, which gives the result:

$$\text{Voltage diff.} \Rightarrow \boxed{t_{XY} = 0.38 R_{\text{wire}} C_{\text{wire}} = 0.38 \text{rcL}^2}$$

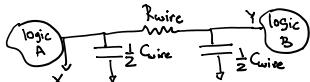
SUMMARY

LUMPED MODEL :- $t_{\text{wire}} = 0.69 \text{rcL}^2$

DISTRIBUTED MODEL :- $t_{\text{wire}} = 0.345 \text{rcL}^2$

VOLTAGE DIFFUSION MODEL :- $t_{\text{wire}} = 0.38 \text{rcL}^2 \rightarrow \text{MOST ACCURATE}$

For the distributed model, we use the following interconnect model



The delay of the wire in this circuit is:-
 $t_{\text{wire}} = 0.345 \text{rcL}^2$

This equivalent circuit representation gives us the same delay as a distributed model gives us but it's a much simpler circuit to use for hand calculation.

Note all models say that the delay of the wire increases quadratically with the wire length!

This becomes a serious problem when designing fast complex circuits. Complex circuits have several long wires and therefore incur severe delay penalty.

In this class we will use the equivalent RC distributed model of the wire, but always remember that the pre-factor in the delay is 0.38 and not 0.345.

Considering wire delays :- When wire delay \geq logic delay

$$t_{\text{wire}} \geq t_{\text{logic}}$$

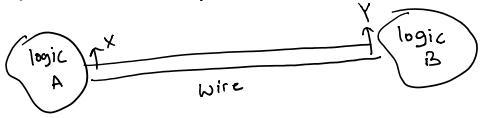
$$0.38 \text{rcL}^2 \geq t_{\text{logic}}$$

$$L^2 \geq \frac{t_{\text{logic}}}{0.38 \text{rc}} \Rightarrow L \geq \sqrt{\frac{t_{\text{logic}}}{0.38 \text{rc}}}$$

Critical length

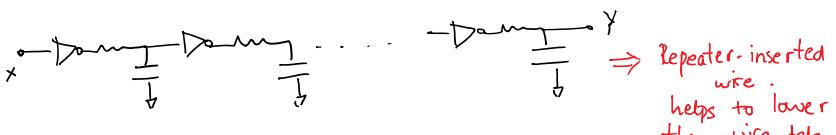
Critical wire length is the length for which the wire delay matches the delay of the gate.

Repeater or buffer insertion :-



If the wire delay is significant, one can add buffers or repeaters to reduce the delay.

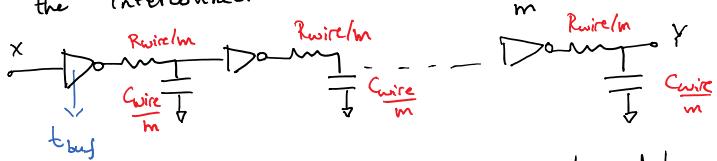
$$t_{xy} = 0.38 r c L^2 \text{ without the buffers}$$



\Rightarrow Repeater inserted
wire.
helps to lower
the wire delay.

Question :- How many repeaters do we need?

Let's say we need 'm' repeaters. Then each segment of the interconnect has resistance R_{wire}/m and capacitance of C_{wire}/m .



Each repeater has the same size so the delay is t_{buf} .

$$t_{\text{stage}} = t_{\text{buf}} + t_{\text{wire}} = t_{\text{buf}} + 0.38 \frac{R_{\text{wire}} C_{\text{wire}}}{m^2}$$

$$t_{\text{stage}} = t_{\text{buf}} + \frac{0.38 r c L^2}{m^2}$$

$$t_{xy} = m t_{\text{stage}} = \underbrace{m t_{\text{buf}}}_{\text{increases with } m} + \underbrace{\frac{0.38 r c L^2}{m}}_{\text{decreases with } m}$$

optimal 'm' will be found :- $\frac{\partial t_{xy}}{\partial m} = 0$

$$\frac{\partial t_{xy}}{\partial m} = t_{\text{buf}} - \frac{0.38 r c L^2}{m^2} \Rightarrow m_{\text{opt}} = \sqrt{\frac{0.38 r c L^2}{t_{\text{buf}}}}$$

$$\text{Optimal delay} : t_{xy} (m = m_{\text{opt}}) = 2 \sqrt{t_{\text{wire}} t_{\text{buf}}} \\ \downarrow \text{increases linearly with wire length.}$$

The main advantage of adding repeaters is that it makes the wire delay only linearly dependent on the wire length. Therefore, the total saving of delay is huge, especially for longer wires. In IC design, longer wires are always repeater inserted.

Energy dissipation of interconnects (not included in slides)

$$E_{\text{wire}} = \frac{1}{2} C_{\text{wire}} V_{\text{DD}}^2 = \frac{1}{2} C V_{\text{DD}}^2 L$$

As opposed to the wire delay, the energy dissipation of the wire increases only linearly with the length.

Repeater - inserted wire energy dissipation :-

the wire increases \rightarrow

Repeater - inserted wire energy dissipation :-

$$E = E_{buf} M_{opt} + M_{opt} \left[\frac{1}{2} \frac{C_{wire} V_{DD}^2}{M_{opt}} \right]$$

$$E = \underbrace{E_{buf} M_{opt}}_{\text{increases with adding repeaters}} + \underbrace{\frac{1}{2} C V_{DD}^2 L}_{\substack{\text{does not get affected by adding repeaters}}}$$

By adding repeaters, one necessarily incurs more energy dissipation.

Therefore, repeaters must be added when delay is the major issue & one can live with large energy dissipation.