ECE 6473
Homework 2
Date Assigned: Sep. 25, 2015
Date Due: Oct. 5th
Collaboration on this homework is NOT ALLOWED

Grading for questions
Q1, Q2, Q3: 20 points each
Q4: 40 points

0.25 micron CMOS process data to be used for Q1, Q2, Q3.

	V_{T0} (V)	γ ($V^{0.5}$)	κ (A/V^2)	λ (V^{-1})
NMOS	0.43	0.4	115×10^{-6}	0.06
PMOS	-0.4	-0.4	-30×10^{-6}	-0.1

Q1. Consider the circuit in Fig. 1. Before time $t = 0$ the switch is open and V_{out} is charged up to some V_{OH}. At time $t = 0$, switch closes and output starts dropping. The switch has a nonzero but small on resistance (R_{sw}). Use, W/L = 2.5μm/2.5μm, so that the long channel models are valid. Furthermore, you can neglect the channel length modulation. For the rest of the device parameters use the V_{th}, γ, and κ parameters from the 0.25μm CMOS parameters given at the top of page one. You can further assume V_{th} is constant throughout the transition and equal to the average of its highest and lowest values. Choose $|\phi_f| = 0.3\ V$ for the transistor. Here, ϕ_f is the Fermi potential.

a. Calculate the output voltage V_{OH} right before $t = 0$.
b. Calculate the equivalent resistance of the transistor during the V_{OH} to $V_{OH}/2$ transition by computing the transistor resistance at the two end points and averaging the two values.
c. What will V_{out} be after infinitely long time? That is, find V_{out} when t → ∞.

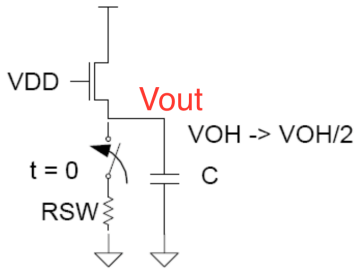

Fig. 1

Q2. Consider the circuit shown in Fig. 2. Write down the equations (and only those) that are needed to determine the voltage at node X. Do not plug in any values yet.

a. Draw the voltage transfer characteristics of the circuit (note X is the output node)
b. Determine the W/L ratio for the transistor such that $V_{out} = 1.5$ V at $V_{in} = 0$V.

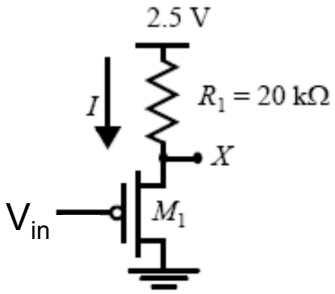

Fig. 2: R_1 is 20 KOhm.

Q3. Assume an NMOS is used to charge a large capacitor, C_L as shown in Fig. 3.

a. Determine t_{pLH} of this circuit assuming an ideal input step of 0V to 2.5V at the gate terminal of the transistor. Assume that the intrinsic capacitance of the transistor is negligible compared to C_L.
b. Assume the load capacitor scales with the width of the transistor. That is $C_L = C_0 \times (W)$, where C_0 is a process dependent parameter and W is the transistor width. If $t_{pLH} = t_0$ for $W = W_0$, how will t_{pLH} change if W is increased to $2W_0$.
c. Now assume a resistor of 5KΩ is used to discharge the capacitance $C_L = 5$ pF determine t_{pHL}.
d. If the NFET is replaced with a PFET such that $\beta_n = \beta_p$. Will the resulting circuit be faster? Explain why or why not.

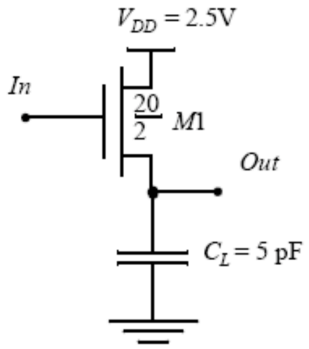

Fig. 3

Q4. **Inverter design problem using Cadence using FreePDK45.**

Draw the schematic of a CMOS inverter driving a constant 5fF load in Cadence. Extract the netlist for HSPICE simulation. Vdd = 1.2V.

a. DC Sizing: Size the inverter for switching threshold = 0.5Vdd. Report the W_n/W_p. Vary the Wn/Wp ratio and plot the switching threshold.
b. Sizing for performance: Consider an input signal with finite and equal rise and fall time = 10ps and size the inverter for equal high-to-low and low-to-high delay. Report Wn/Wp.
c. Vary the rise time (keep fall-time constant) of the input signal and measure high-to- low delay. Plot high-to-low delay for rise time 0.1 ps, 50 ps, 100 ps, 150 ps, 200 ps, and 500 ps. Do you see the effect of finite input slew on delay?
d. Consider the rise time for V_{in} = 200 ps. Now increase the PMOS width by 4 times. What happens to the high-to-low delay and why?
e. Again consider the rise time = fall time = 200ps and re-size the inverter to achieve equal rise and fall delay. Is there any difference in required Wn/Wp from part (c). Explain your answer.