Ratioed Logic

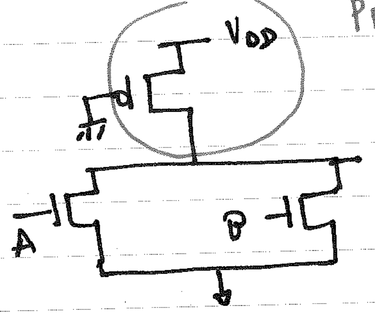
Ratioed logic is a logic style where the logic levels depend on the ratio of device sizes.

In CMOS logic, the logic levels are always "0" or "V_{DD}" independent of the ratio of the device sizes. However, the CMOS logic uses 2N number of transistors for N inputs. Therefore, the area consumption could be high. For ratioed logic, you can reduce the # of transistors required to implement the logic.

In Pseudo-NMOS logic, the pull-up is implemented with A PMOS device that is always ON. That is, the gate of the PMOS device is connected to ZERO.

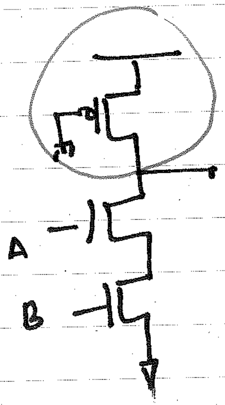
PSEUDO-NMOS

PMOS is always ON ⇒ static power dissipation ~~when the pull-down is ON~~



$F = \overline{A+B}$ (NOR)

PMOS is always ON. ⇒ static power dissipation!



$F = \overline{A \cdot B}$ (NAND)

$V_{OH} = V_{DD}$ since PMOS is good connect to V_{DD}.

$V_{OL} > 0$ since PMOS is always bleeding.

To calculate the Value of V_{OL}, we know PMOS will be in saturation but NMOS will be in linear regime.

$$0.5\,\beta_P\left(V_{DD}-|V_{THP}|\right)^2 = \beta_n\left(V_{DD}-V_{TN}-0.5\,V_{OL}\right)V_{OL}$$

Assuming $V_{OL} << V_{DD}-V_{TN}$

$$0.5\,\beta_P\left(V_{DD}-|V_{THP}|\right)^2 = \beta_n\left(V_{DD}-V_{TN}\right)V_{OL}$$

So $$V_{OL} = 0.5\left(\frac{W_p}{W_n}\;\frac{\mu_p}{\mu_n}\right)\left[\frac{(V_{DD}-|V_{THP}|)^2}{V_{DD}-V_{TN}}\right]$$

For $|V_{THP}| = V_{TN} = V_T$

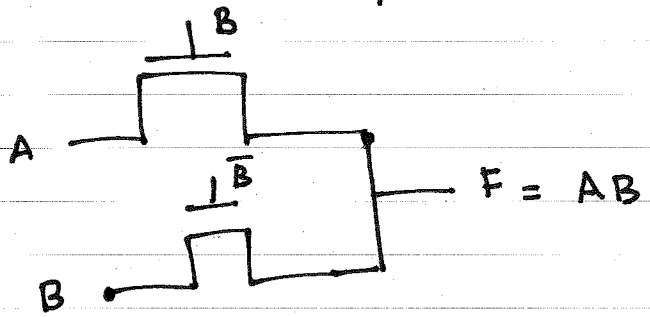
$$V_{OL} = 0.5\left(\frac{W_p}{W_n}\right)\left(\frac{\mu_p}{\mu_n}\right)\left(V_{DD}-V_T\right)$$

NOTE:- As $\frac{W_p}{W_n}$ ↑ the value of V_{OL} increases.

If V_{OL} is too close to zero, it means W_p is small. However, a drawback of small W_p is that V_m is also close to ground. The noise margin on the lower side "V_{IL}" will be reduced too.

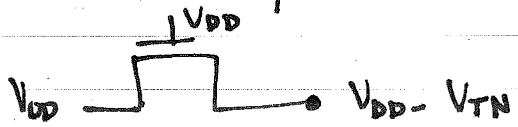
PASS TRANSISTOR LOGIC (PTL)

PTL uses fewer transistors to implement logic. This also helps to reduce the power dissipation due to the lower capacitance.



Note that PTL directly implements the non-inverting logic.

However the challenge is that NMOS does not pass a good "1". That is there is always a V_{TN} drop.



Another issue is that this NMOS has body effect & therefore its threshold voltage will be even higher.

$$V_{TN} = V_{TO} + \gamma\left[\sqrt{|2\phi_f| + V_{DD} - V_{TN}} - \sqrt{|2\phi_f|}\right]$$

This is a 2nd order [quadratic] equation in V_{TN}. You can solve it to find what the value of V_{TN} is.

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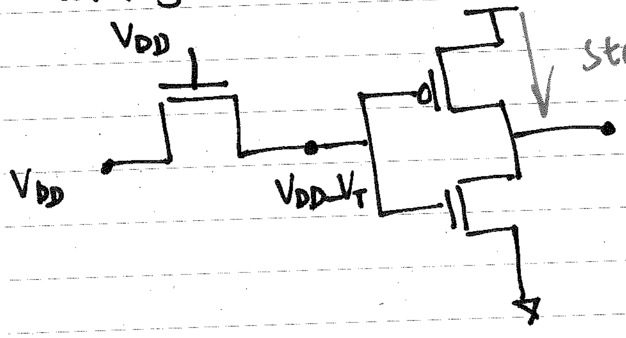
Now consider that this PTL is used to input a signal into an inverter in the following configuration :-

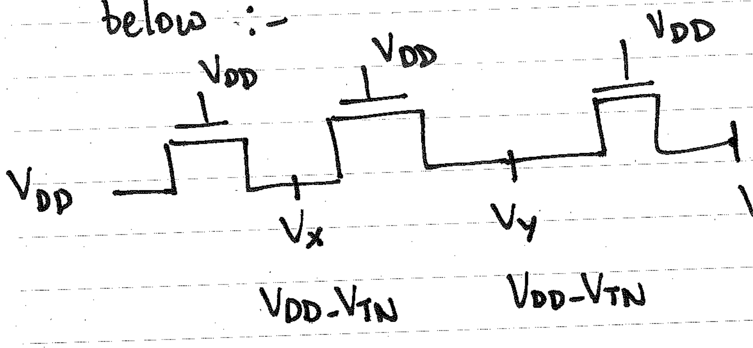


↳ the swing here is complete, from "0" to "V_{DD}".

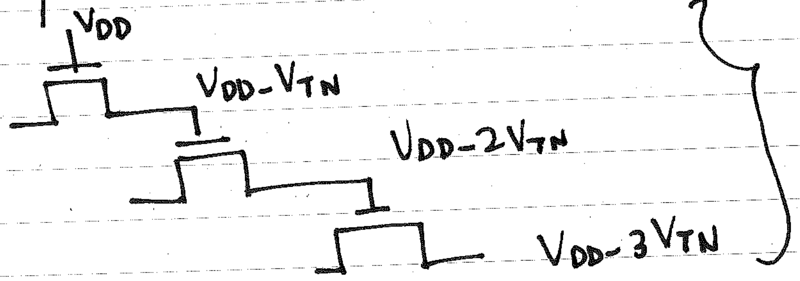
But because the input to the inverter is at lower voltage $[V_{DD} - V_{TN}]$, the delay of the inverter will be more.

Also the static power consumption will be there.

The proper way of cascading PTL is as shown below :-



Improper way to cascade PTL is :-



Multiple V_{TN} drops.

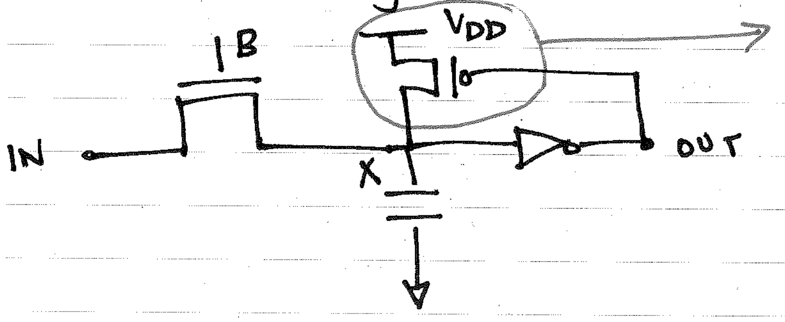
Also note PTL is typically implemented with NMOS only devices.

This is because PMOS only logic will be slower for the same area consumption.

Hence, PTL is NMOS - only.

LEVEL RESTORATION

A very useful concept in PTL is the use of a level restoring transistor.

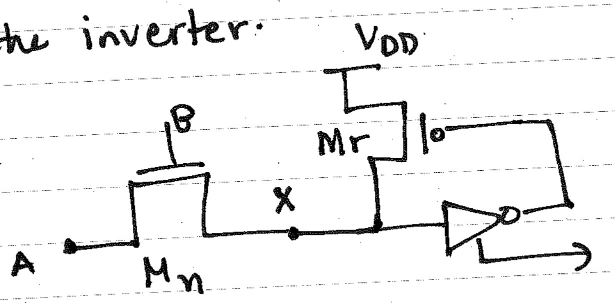


a) When IN = 1 (B = 1) 'X' goes to $V_{DD}-V_T$, so OUT goes to "0" and the level restorer kicks in and pulls V_x to V_{DD}.

b) When node 'x' is pulled to V_{DD}, there is no static power dissipation in the inverter.

c) Challenge is the sizing of the level restorer. If the level restorer is too strong then 'X' may not be able to go down & therefore may not be able to turn off the level restorer device.

Hence size the level restorer and the pass transistor device such that the voltage at node 'X' goes below the switching threshold of the inverter.



→ switching threshold = V_m

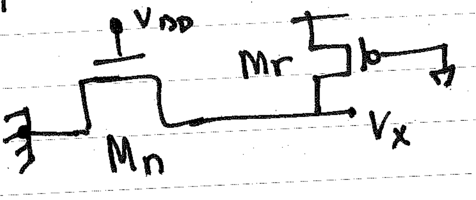
M_n :- pass transistor device

M_r :- level restorer

Size M_n & M_r such that $V_x < V_m$.

Analyze quantitatively :-

open the feedback loop and ground the gate of the PMOS device.



$\Rightarrow$ This now resembles a pseudo-NMOS logic.

Lets say $V_x = V_m = \frac{V_{DD}}{2}$

For 'Mn' $V_{DS} = \frac{V_{DD}}{2}$, $V_{GS} = V_{DD}$] $V_{DS} < V_{Dsat}$ if $V_{DD} = 2.5V$, $V_T = 0.4V$

Linear

For 'Mr' $V_{SD} = \frac{V_{DD}}{2}$, $V_{SG} = V_{DD}$] $V_{SD} < V_{SDsat}$ if $V_{DD} = 2.5V$, $|V_T| = 0.4V$

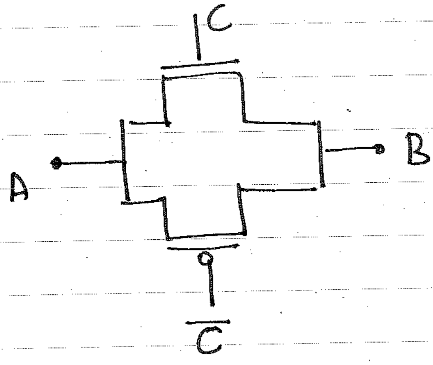
Linear

Solve for current equation to get W_p/W_n.

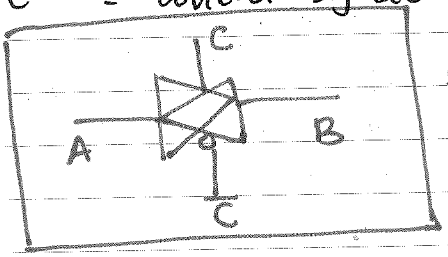
TRANSMISSION GATE (TG) LOGIC

Transmission gate logic is used to deal with the problem of threshold voltage drop in pass transistor design. In TG logic style, we use both PMOS and NMOS devices to restore the logic to "0" and VDD.

So TG acts as a bidirectional switch that is controlled by the gate voltage.



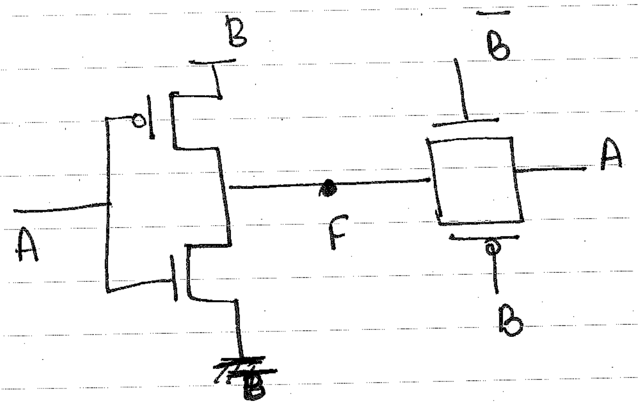
'C' = control signal



symbol

$$\boxed{A = B \text{ if } C=1}$$

Efficient implementation of TG - XOR



When $B = 1$ then the transmission gate on the right is off and $F = \bar{A}$

So $F = \bar{A}B$

Now when $B = 0$, then the left hand circuit is disabled and $F = A$ so $F = A\overline{B}$

Hence, combing the two $\boxed{F = \bar{A}B + A\overline{B}}$

TG-XOR requires overall SIX transistors including the transistors required to invert the signals.

imp.

XOR

CMOS requires 12 transistors
Complementary pass transistor logic requires 8 transistors.
Transmission gate requires 6 transistors.