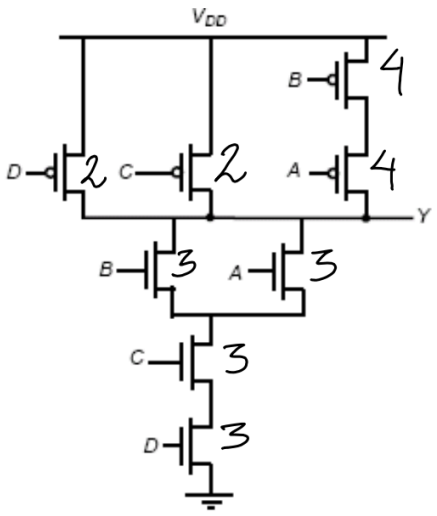
ECE 6473 HW-3 solution

Problem 1.

a) $F = \overline{(A+B)CD}$

b)



c) High-to-Low Delay:
Initial: A = 1, B = 0, C = 1, D = 0 (or A=0, B=1, C = 1, D = 0)
Final: A = 1, B = 0, C = 1, and D = 1 (or A = 0, B = 1, C = 1, and D = 1)
A = 1 (or B = 1), C = 1 will charge all the intermediate node capacitance and D makes a transition from 0 to 1.

Low-to-High Delay:
Initial: A = 0, B = 1, C = 1, D = 1
Final: A = 0, B = 0, C = 1, D = 1
B makes a 1 to 0 transition. This transition needs to charge the intermediate node capacitance in the series path (i.e. A and B) from Vtp to VDD and the output from 0 to VDD.

Problem 2.

(a) To derive energy in one complete cycle for the chain of inverters:

$$E_{total} = \sum_{j=1,N} E_j$$

Where E_j is the energy of the j^{th} stage.

$$E_j = V_{DD}^2 . C_1 u^j$$

$$E_{total} = \sum_{j=1...N} C_1 V_{DD}^2 u^j = C_1 V_{DD}^2 . u . \frac{u^N - 1}{u - 1}$$

$$E_{total} = C_1 V_{DD}^2 . \frac{u}{u-1} . \left(\frac{C_L}{C_1} - 1 \right)$$

$$E_{total}(in\ terms\ of\ E_r) = E_r . \frac{u}{u-1} . \left(\frac{C_L}{C_1} - 1 \right)$$

(b) To derive the expression for EDP in terms of reference EDP and to find the expression that optimized EDP

Using the fact that the delay of the chain is: $Nu\tau_r$

$$EDP_{chain} = E_r . \frac{u}{u-1} . \left(\frac{C_L}{C_1} - 1 \right) . Nu\tau_r$$

Using the fact that $N = \ln\left(\frac{C_L}{C_1}\right) / \ln(u)$

$$EDP_{chain} = E_r \tau_r . \frac{u^2}{u-1} . \left(\frac{C_L}{C_1} - 1\right) . \frac{\ln\left(\frac{C_L}{C_1}\right)}{\ln(u)}$$

$$\frac{EDP_{chain}}{EDP_{ref}} = \ln\left(\frac{C_L}{C_1}\right) . \left(\frac{C_L}{C_1} - 1\right) . \left[\frac{u^2}{\ln(u) . (u-1)}\right]$$

To optimize the EDP:

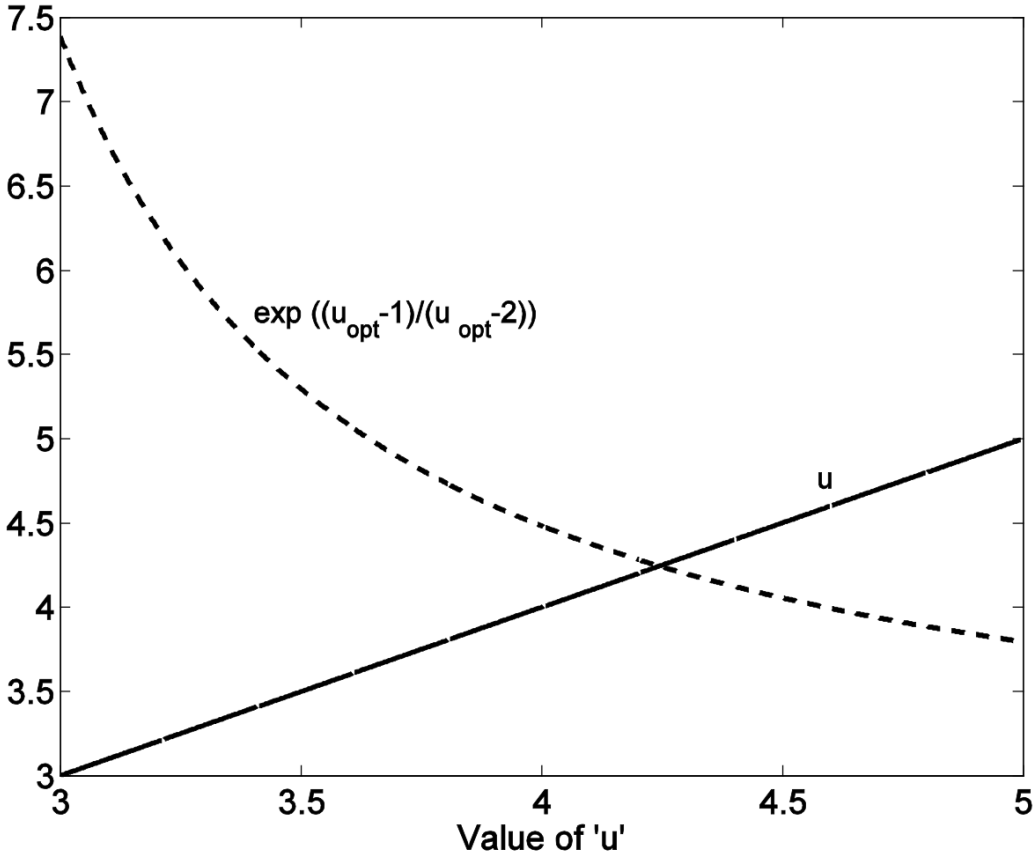
$$\frac{\partial}{\partial u}\left(\frac{EDP_{chain}}{EDP_{ref}}\right) = 0$$

$$u^2 \ln(u) - 2uln(u) - u(u-1) = 0$$

$$\ln(u)\,(u-2) - \,(u-1) = 0$$

$$\ln(u) = \frac{u-1}{u-2}$$

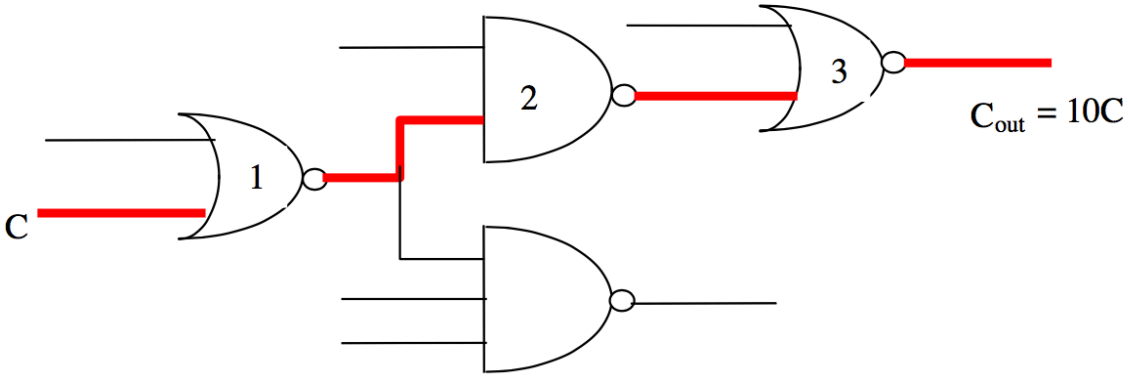
$$\boldsymbol{u_{opt} = e^{\frac{u_{opt}-1}{u_{opt}-2}}}$$



From Fig. 2, the optimum value of sizing is obtained as ~ 4.2443

The optimal value of "u" for delay optimization is equal to e = 2.72 (for FET capacitance =0). The optimized value of "u" for EDP is more than that for delay optimization.

Problem 3:



First, we calculate path effort.

g1 = (1+2r) / (1+r) = 6/3.5 = 1.71
g2 = (2+r) / (1/r) = 4.5/3.5 = 1.29
g3 = g1 = 1.71
G = g1 * g2 * g3 = 3.772
H = 10C / C = 10
B = Ctotal / Cpath = (2+r+3+r) / (2+r) = 10/4.5 = 2.22
F = G H B = 83.8
$f = F^{1/3} = 4.38$

We now work backwards.

h3 = 10C * (6/3.5) / 4.38 = 3.91 C
h2 = 3.91C * (4.5/3.5) / 4.38 = 1.15 C
h1 = 2.22 * 1.15C * (6/3.5) / 4.38 = C