✱ Top-down view of design hierarchy

- Start from system specifications (Functionality, speed, power, size etc.) for the entire project.

- Using the specifications, we create an ABSTRACT high-level model. The languages used for creating the high-level model are VHDL, Verilog, C, C++.

- After the code is written, it is verified to ensure that it satisfies the functionality.

- The next step is logic synthesis, where the HDL model is taken and converted into a logic design of the network with gates.

- The gate level logic design is verified. Post verification it is mapped onto an electronic circuit design. In the electronic circuit, transistors are used as switches.

- The level below the circuit design is the physical design level. Physics of transistor is used; complex/manual layout of the circuit.

Top-down design flow for a microprocessor

a) Initial conception includes instruction set and components. Instruction set is just a collection of all the instructions that the µP is able to execute. Component is a digital logic unit that implements a given function.

b) Using the instruction set + components, a system-level or architectural level model is created with the help of a standard Hardware description language.

c) note, the architecture model is only abstract. It does not invoke any details of how the hardware will be implemented. In some sense, the design exists only as a piece of software/code. This is also known as Register-transfer level (RTL) description.

d) The abstract model is tested and verified for Functionality. After this, the system blocks are translated into a logic model that is based upon Boolean equations and logic gates. This is the logic synthesis step in the design flow.

e) After logic synthesis, the network is mapped onto electronic circuits where the characteristics of silicon circuits become important.

f) Physical design involves defining the transistors as 2D structures on a piece of silicon chip. Placement & routing are often also done using CAD tools.

g) Once the physical design is verified, a database is created that allows the manufacturing line to actually build the chip.

Logic synthesis

automated

→ based on a set of CAD tools that typically accept an HDL code and create the logic networks with a predefined set of rules.

custom

→ special cases when the synthesis tool does not meet the necessary specifications.

* Finding a logic design that is optimized is a non-trivial problem.

A given Boolean expression may be represented in several equivalent ways. All of these equivalent ways will produce the same output but will use different equations and gates. The complication arises from the fact that each representation of the same logic function has different characteristics at the hardware level. By characteristics, we mean design aspects like area or power dissipation or performance.

From the given set of equivalent logic and electronic circuit representations, one must find the "best" solution for the task at hand.

☆ LOGIC DESIGN

In digital electronics, data is represented using only two values.

Logic "1" (High)
Logic "0" (Low)

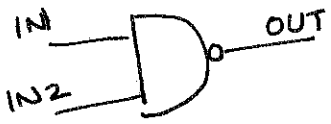
A digital logic circuit consists of gates to implement BOOLEAN Logic.

Basic building blocks

a) INVERTER

IN	OUT
1	0
0	1

b) NAND



IN1	IN2	OUT
0	0	1
0	1	1
1	0	1
1	1	0

c) NOR

IN1	IN2	OUT
0	0	1
0	1	0
1	0	0
1	1	0

Side Note :-

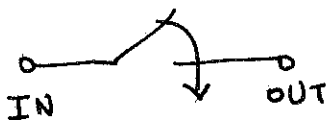
A NAND gate behaves as an inverter if one of its inputs is held at logic "1".

A NOR gate behaves as an inverter if one of its inputs is held at logic "0".

For all of the digital circuits, the basic building unit is a transistor. While there are several kinds of transistors, in this course we focus only on MOSFETs.

MOSFET :- Metal oxide Semiconductor Field Effect transistor.

A transistor behaves as a voltage controlled switch.



The connection between IN and OUT is established when the switch is closed.
When the switch is open, there is no connection from IN to OUT.

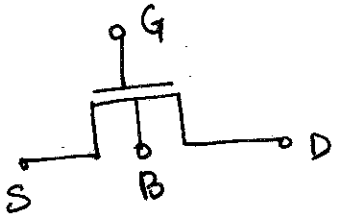
The opening and closing of the switch is done with the help of a CONTROL voltage.

There are two kinds of MOSFETs :-

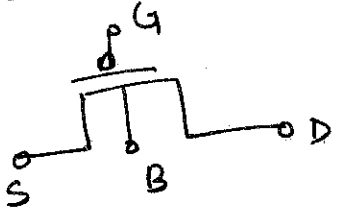
(a) n- type
(b) p- type

} Presence of both types of transistors is possible through the CMOS fabrication process.

CMOS :- complementary metal oxide semiconductor.



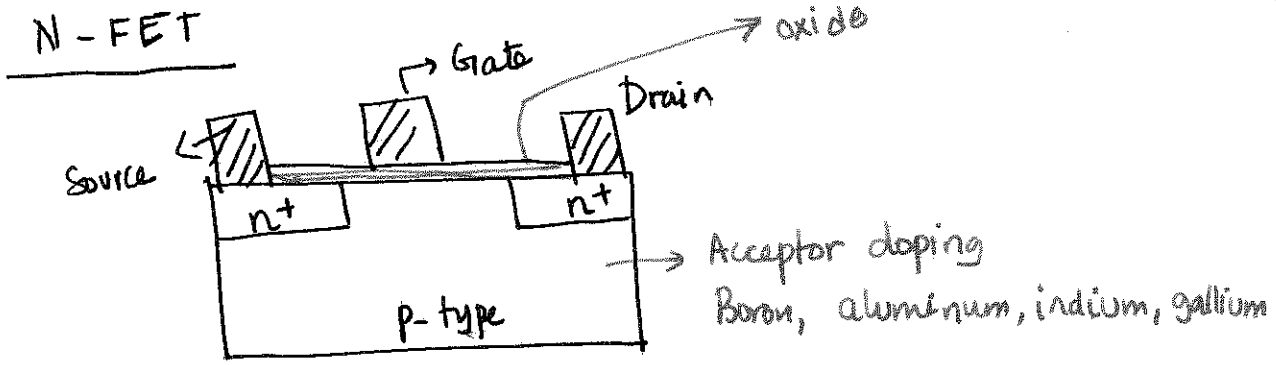
n FET symbol



p FET symbol

* Usually "B" terminal is omitted.

N-FET



a) substrate or body is p-type

b) source and drain doping is n-type.

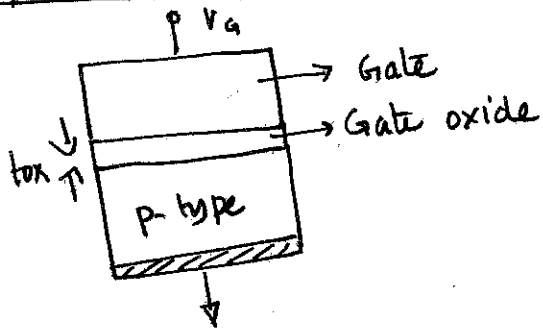
c) An oxide (thin) separates the channel and the body.

For now, we will focus on only three terminals, the source (S), drain (D), and the gate (G).

G :- control terminal

A current flows between drain and source terminal :- I_{DS}

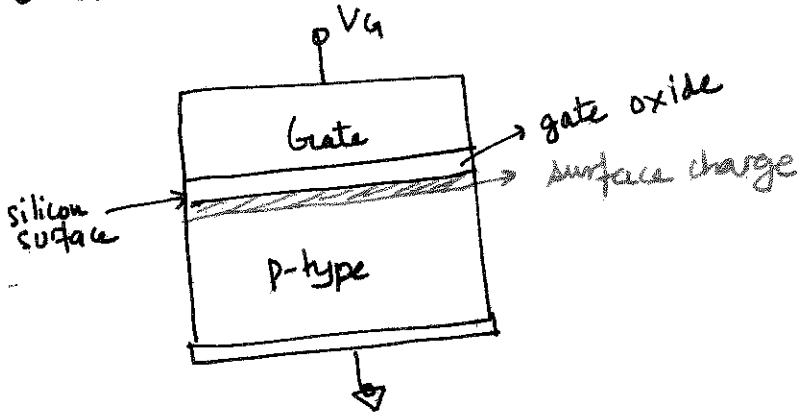
MOS Capacitor analysis



$$C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}} \Rightarrow$$ Parallel plate capacitor of thickness of t_{ox}.

C_{ox} determines the amount of coupling that exists b/w the gate and the channel in silicon.

When $V_G > 0$, then it starts to deplete the silicon surface and negatively charged acceptor ions are uncovered.



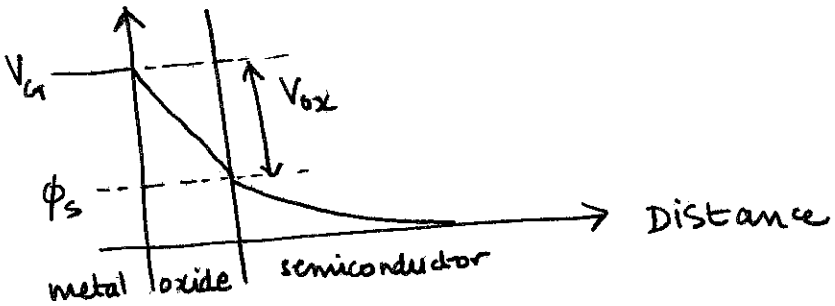
$$Q_S = - C_{ox} V_G$$

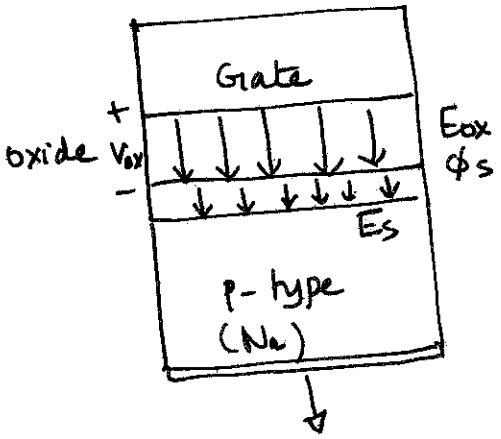
From KVL, we can write

$V_G = V_{ox} + \phi_s$

V_{ox}: drop across the oxide

ϕ_s: surface potential.





Electric Fields.

→ This equation must be updated in the presence of oxide charges plus metal–semiconductor work function diff.

$$V_G = V_{ox} + \phi_s + \frac{Q_{ox}}{C_{ox}} + \phi_{ms}$$

Threshold voltage is defined when $\phi_s = 2|\phi_f|$

where ϕ_F = bulk Fermi level set up by the doping concentration in the p-type semiconductor.

$$\phi_F = \left(\frac{kT}{q}\right) \ln\left(\frac{N_A}{n_i}\right)$$

Further, $V_{ox} = -\frac{Q_B}{C_{ox}}$ where Q_B = substrate depletion charge

Hence, $V_{TN} = -\frac{Q_B}{C_{ox}} + 2|\phi_f| + \underbrace{\frac{Q_{ox}}{C_{ox}} + \phi_{ms}}$

dependent mostly on process, manufacturing

$$Q_B = -\sqrt{2q\epsilon_{si} N_a (2|\phi_f|)}$$

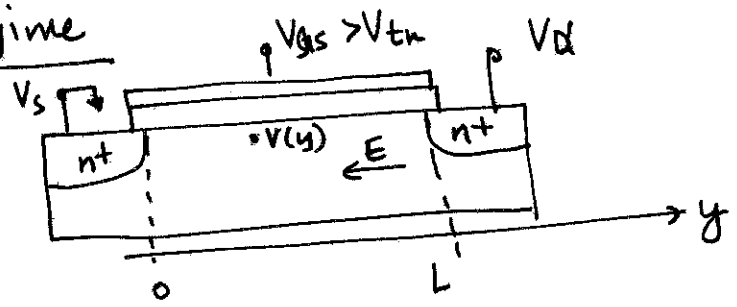
Hence, $$\boxed{V_{TN} = \frac{\sqrt{4q\epsilon_{si} N_a |\phi_f|}}{C_{ox}} + 2|\phi_f| + \underbrace{\frac{Q_{ox}}{C_{ox}} + \phi_{ms}}_{V_{fb}}}$$

V_{fb} → Flatband voltage.

Derivation of the current flow equations

The mosfet exhibits linear and saturation transport regimes. So we will first derive the result for the linear regime.

Linear Regime



For a positive V_{DS}, electrons flow from source to drain.

But current flows from drain to source.

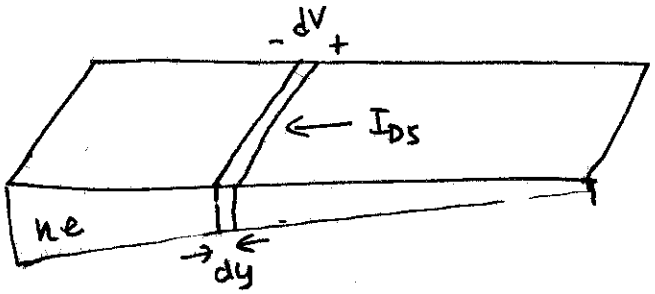
$$E(y) = -\frac{dV(y)}{dy}.$$

$V(0) = 0$
$V(L) = V_{ds}$ } Boundary conditions.

Due to the parallel plate gate capacitor, the charge in the semiconductor is given as

$$Q(y) = -C_{ox}\left(V_{gs} - V_t - V(y)\right)$$

From the expression, it is clear that the maximum charge occurs at $y = 0$ and the minimum charge occurs at $y = L$.



$dV = I_{DS}\, dR$ ← differential resistance

$$dR = \frac{dy}{\sigma_n A_n}$$

σ_n = conductivity $\{1/\Omega\text{-m}\}$

A_n = cross-sectional area $\{m^2\}$

$$\sigma_n A_n = q \mu_n n_e [W x_e]$$

- q: charge
- μ_n: mobility
- n_e: electron density

$$Q_c = -q n_e x_e$$

Combining everything,

$$dV = \frac{-I_{DS}\,dy}{\mu_n W Q_e} = \frac{-I_{DS}\,dy}{\mu_n W C_{ox}(V_{gs} - V_t - V(y))}$$

$$\int_0^{V_{ds}} \mu_n W C_{ox}(V_{gs} - V_t - V(y))\,dV = -\int_0^L I_{ds}\,dy$$

$$I_{DS} = \underbrace{\mu_n \frac{W}{L} C_{ox}}_{\text{design parameter}} \left[(V_{gs} - V_t)V_{ds} - \frac{V_{ds}^2}{2}\right]$$

$\mu_n C_{ox}$:– Process parameter "K_n"

$\mu_n C_{ox} \frac{W}{L}$:– design parameter "β_n"

SATURATION

Saturation occurs when $V_{DS} > V_{DSat} = V_{GS} - V_t$

Substituting $V_{ds} = (V_{gs} - V_t)$ in previous equation,

$$I_{DS} = \frac{1}{2} \mu_n C_{ox} \left(\frac{W}{L}\right) \left[(V_{gs} - V_t)^2 \right]$$

At this particular value of V_{ds}, the channel @ the drain end is pinched off.

→ From this expression it is clear that the transistor current does not depend on V_{ds}. And in this case, the transistor really acts as an ideal current source.

However, in reality, this is not quite correct. The effective length of the channel is actually modulated by V_{ds}. This is known as Channel length modulation.

Increasing V_{ds} causes the length to decrease slightly. This means that the current would slightly increase due to CLM.

$$I_{DS} = \frac{1}{2} \mu_n C_{ox} \left(\frac{W}{L}\right) \left[(V_{gs} - V_t)^2 \right] \left[1 + \underset{\text{CLM.}}{\lambda} V_{ds} \right]$$