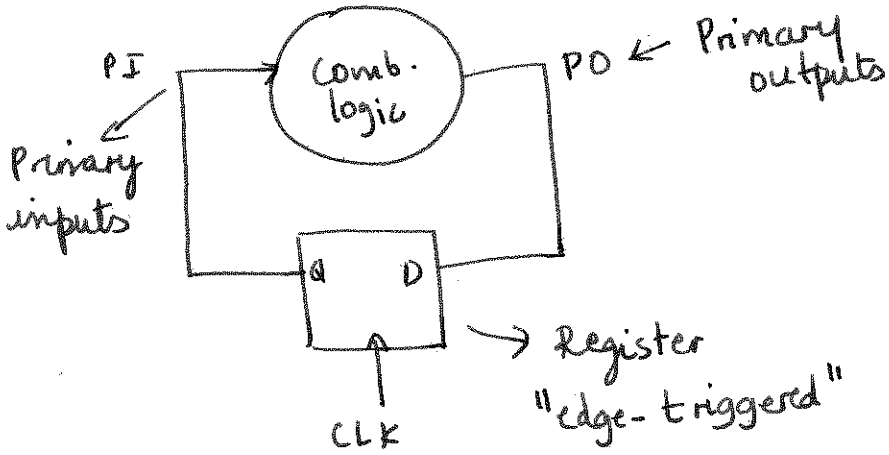
Sequential circuits

a) Storage of information

b) o/p depends not only on the curent value of the input but also on the preeceding value.

c) System has memory.

d) In synchronous sequential systems, all registers are under the control of a global clock signal.



$$t_{clk} \geq t_{su} + t_{plogic} + t_{c-q}$$

$$F_{clk} \leq \frac{1}{t_{su} + t_{plogic} + t_{c-q}}$$

What about hold time?

First we define the contamination delay of a circuit element as the fastest/quickest time (as opposed to the worst case time for propagation delay) that it produces an output.

Let $t_{cd,comb}$ be the contamination delay of the combinational logic

$t_{cd,reg}$ be the contamination delay of the register.

→ After a positive clock edge, new data can propagate through the register and the comb. circuit in $t_{cd,reg} + t_{cd,comb}$ time units

→ But we want the input to the register to be stable for t_{hold} units of time.

$$\boxed{t_{cd,reg} + t_{cd,comb} \geq t_{hold}}$$

∴ if circuit is too fast, it may be a problem.

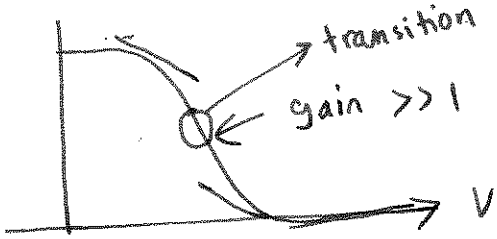
Principle of Bistability

A cross-coupled pair of inverters is a bistable circuit as it has two stable points.

If the circuit is left in a metastable state, a little bit of noise will push it to one of the two stable states.

In the meta stable state, the loop gain is much greater than unity which helps to bring the circuit toward one of the stable states. Once the circuit is in the stable state, the loop gain $<< 1$ which means even a large noise will not disturb the state of the inverter.

Recall !-



$$\text{gain} = \left| \frac{\partial V_{out}}{\partial V_{in}} \right|$$

A bistable circuit has two stable states. It is also called a Flip Flop. However, this circuit is useful if there is a means to bring it from one state to another.

Two methods are commonly used :-

(a) <u>cutting the feedback loop</u> :- In this case a new value can be easily written. Such a latch is a mux-based latch and it realizes the operation :-

$$Q = \overline{clk}\ Q + clk\ In$$

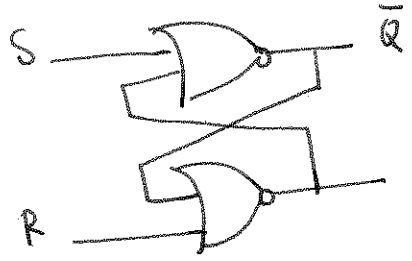
When $clk = 1$ then $Q = In$

$clk = 0$ then $Q = Q$ (retains the previous value)

(b) <u>overpowering the feedback loop</u> :- We can apply a trigger at the input of the flip flop and make it temporary unstable by increasing the loop gain G to a value larger than 1.

However, in this approach a strong trigger circuit is needed to overpower the feedback loop.

NOR set-reset



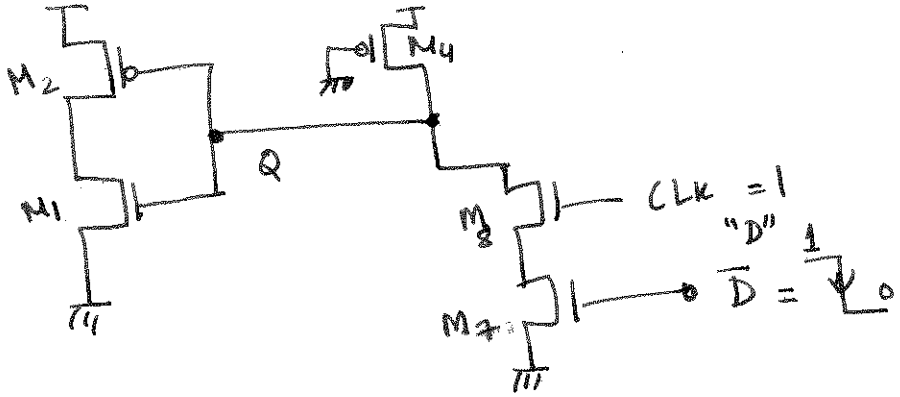
The input condition S = R = 1 is forbidden.

First, we want Q and $\bar{Q}$ to be complimentary of each other.

Second if S = R = 1 and then they go to 0, the final output is unpredictable. It would depend on whichever input is the last to go low.

D-latch with clock or enable

This is also called a ratioed latch. In order to make this latch switch, we must succeed in bringing Q below the switching threshold of the other inverter.



Bring V_Q below V_M of "M_1" & "M_2".

Lets say the switching threshold of M_1-M_2 inverter is $V_m = \frac{V_{DD}}{2}$.

In this case we solve the equation by equating current flowing through M_4 into M_7-M_8.

$$I_{M4} = \frac{\beta_{P,M4}}{2}\left[V_{DD} - |V_{TP}|\right]^2\left[1 + |\lambda_{p,M4}|\left(V_{DD} - V_Q\right)\right]$$

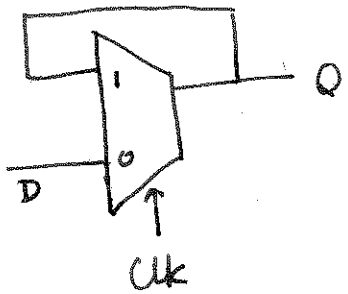
$$= \frac{\beta_{N,M7/M8}}{2}\left[\left(V_{DD} - V_{TN}\right)^2\right]\left[1 + \lambda_{n,M7/M8}\left(V_Q\right)\right]$$

Solve this equation for $V_Q = V_m = \frac{V_{DD}}{2}$. You will get the proper sizing for M7/M8 and M4.

A few assumptions when writing the above equations, We ignored the voltage at the internal node b/w M_7 and M_8. And when the gates of both transistors switch together, we can actually combine them into one transistor.

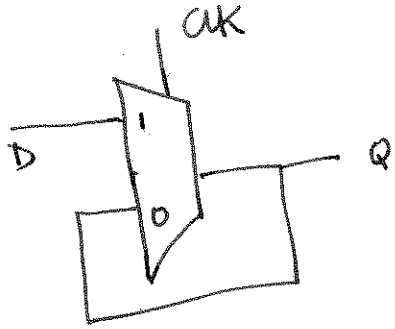
Question :- Why is the CLK signal put on transistor M_8 and not on M_7?

Making Latch with Transmission gate



$Q = D \cdot \overline{clk} + Q \cdot \overline{clk}$

Negative latch



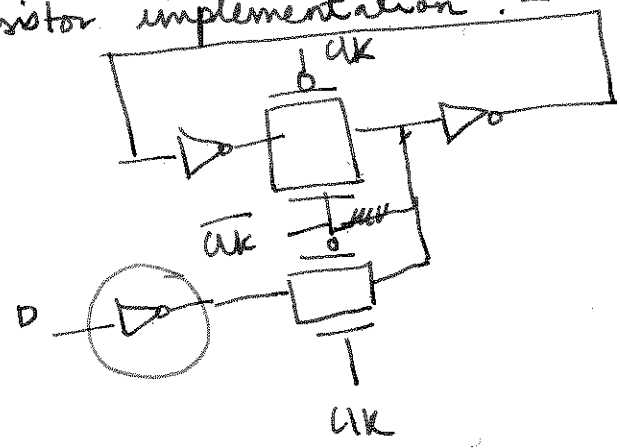
$Q = D \cdot clk + Q \cdot \overline{clk}$

Positive latch

- Negative latch is transparent when clk = low
- Positive latch is transparent when clk = high

"opaque" state of the latch is when the latch is simply holding the data.

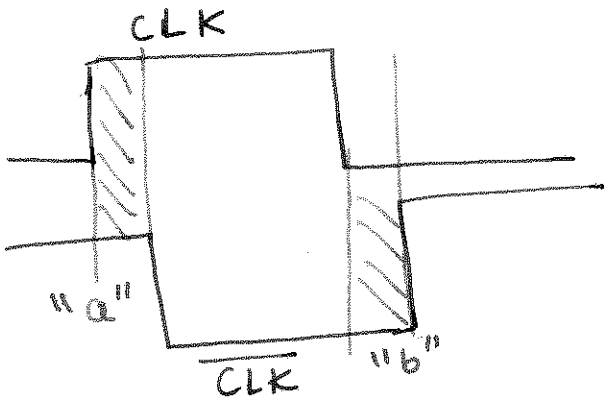
Transistor implementation :-



Positive latch.

why do we need this inverter?

Imagine if clk and $\overline{clk}$ signals are Non-overlapping



Lets say there is a finite delay in generating $\overline{CLK}$ from Clk signal. That means, Clk and $\overline{CLK}$ will actually have a finite overlap as shown in shaded regions "a" & "b". Ideally in region "b" "Q" should be in hold mode. However, because $\overline{Clk}$ is also low, the output Q remains connected to Data D for a brief time.

If the delay of the path from "D" to "Q" is smaller than the overlap region of Clk and $\overline{Clk}$, there will be a glitch & it could also lead to wrong output Q.

CREATING EDGE-SENSITIVE REGISTERS OR FLIP FLOPS

To create a positive edge triggered register, we cascade two latches in series. The First latch is a negative latch, while the second latch is a positive latch.

First latch is also called the "Master" and the second latch is called the "slave".

This kind of an edge-triggered register is called the Master-Slave Flip Flop.

To create a negative edge-triggered Master-Slave Flip Flop, you must reverse the series connection of the latches. That is, the Master latch must be a positive latch, while the slave latch must be a negative latch.

Issue of clock overlap in Positive edge triggered Master-slave Flip Flop

For positive M-S Flip Flop, the master samples data when clk = low and slave samples data (Qm) when clk = high.

However when both clk and $\overline{clk}$ are high / low simultaneously then T_1 & T_3 (Slide #34) are conducting which creates the Race problem.

Second issue arises when the master gets driven by both the data as well as the Feedback loop, and it could result in an undefined state.