EL-GY-6473 (Fall 2015)
INTRODUCTION TO VLSI DESIGN
LAYOUT DESIGN

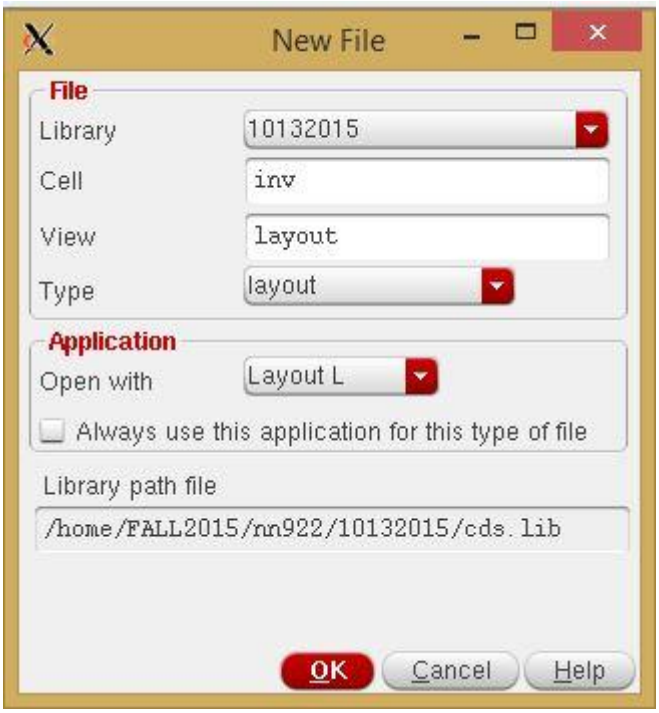
By now, we have already created the schematic and have simulated our design with verilog-XL . The next step in the design process is to create the layout for the circuit. A layout is basically a drawing of the masks from which your design will be fabricated. Therefore, layout is the most critical step in the design process because it determines whether your design is finally going to be working or not.

There are two ways to draw layout. You can create a layout from scratch. You will have more flexibility with it, but it takes more time. You may also create a layout using Layout XL, which will be much faster. Following is a tutorial how you can create layout by LayoutXL.

Step 1: You have to include the following two commands every time before starting cadence. (This are used to source your file so as to you get the instances)

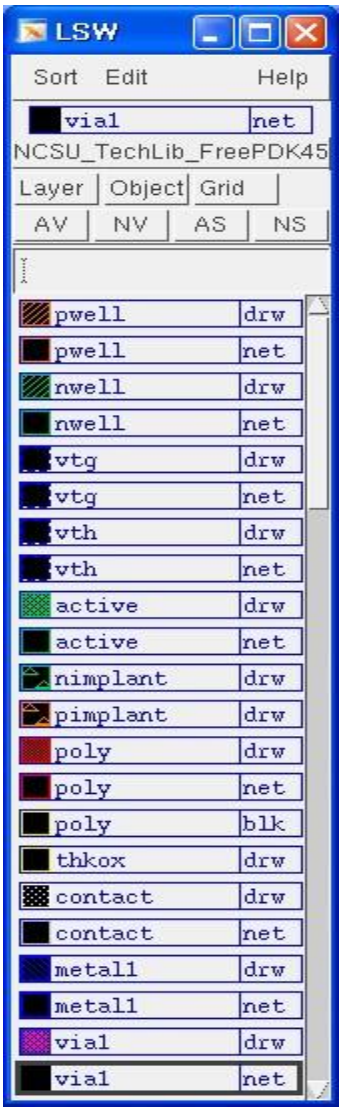
source /softw/cadence/local/FreePDK45/ncsu_basekit/cdssetup/icoa_setup.csh
source /softw/cadence/local/FreePDK45/ncsu_basekit/cdssetup/setup.csh
virtuoso

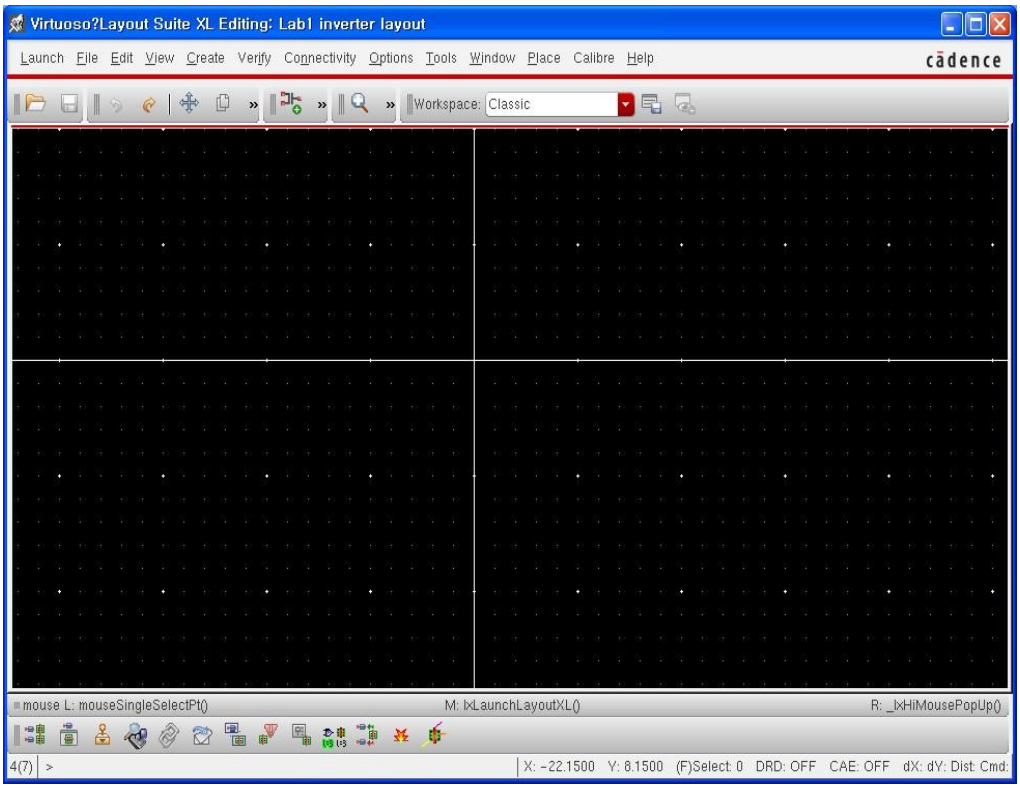
Step 2: Create a view under the cell where you have created your inverter schematic
Select **type → layout**
Open with → Layout L



Select **Launch → Layout XL**

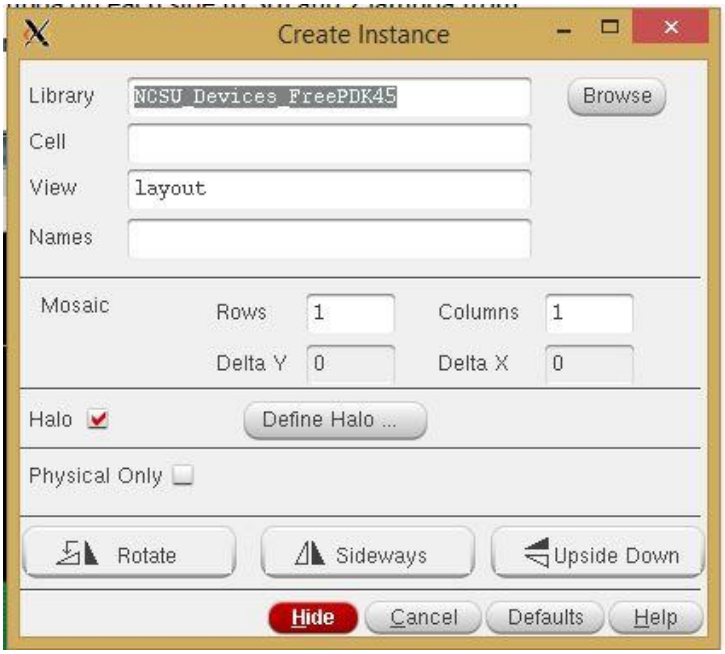
This opens up the virtuoso XL Layout editing window and the Layer select window (LSW)

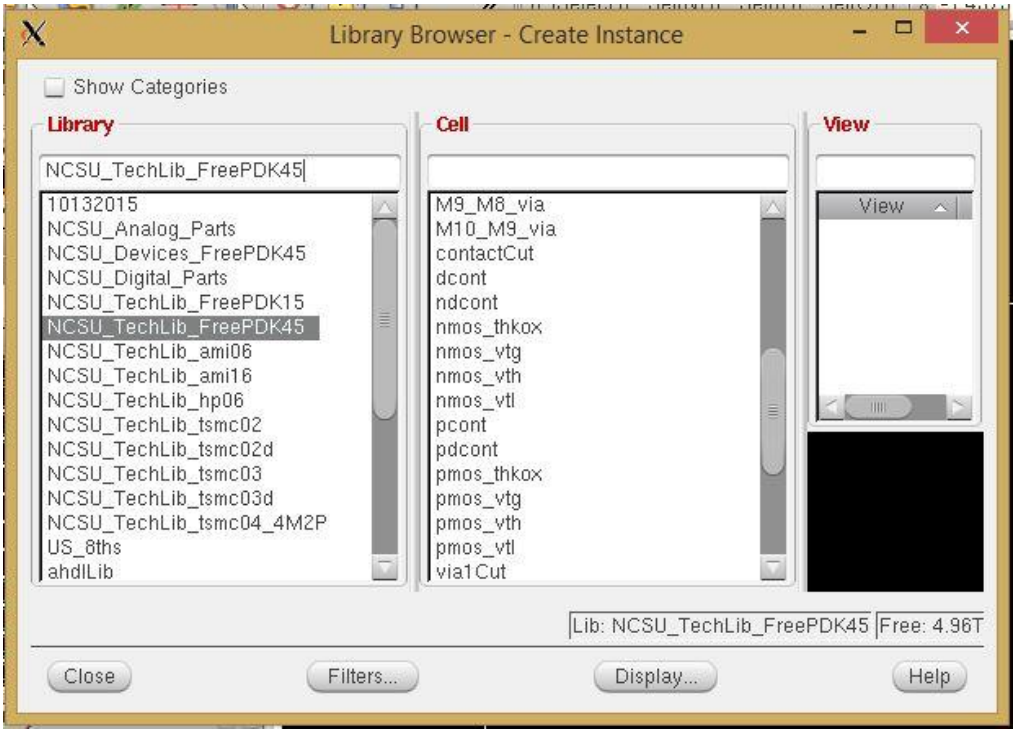


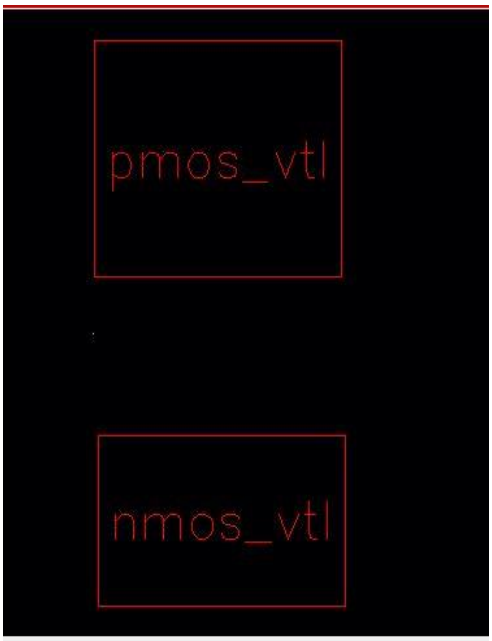


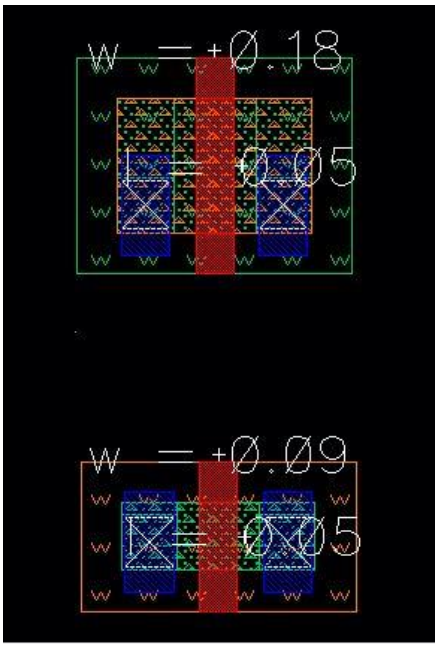
Step 3: Creating instances (shortcut I)

Create → Instance









To change the view: Hit **Shift + f**

To edit the **properties** of instances, select the instance and hit "**q**"

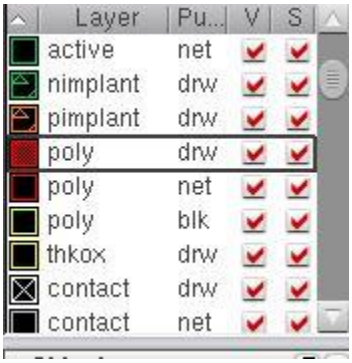
Note:

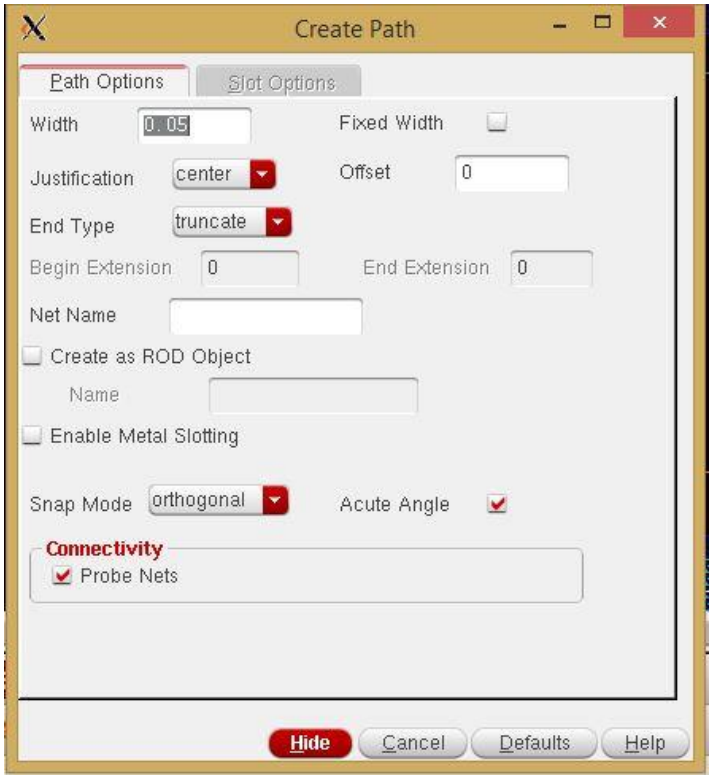
1. **The width for PMOS should be 135nm ideally and you can change it according to schematic.**
2. **When you change the width of Nmos or Pmos it should be in the multiple of 2.5nm.**

i.e. 135 → 137.5, no intermediate values

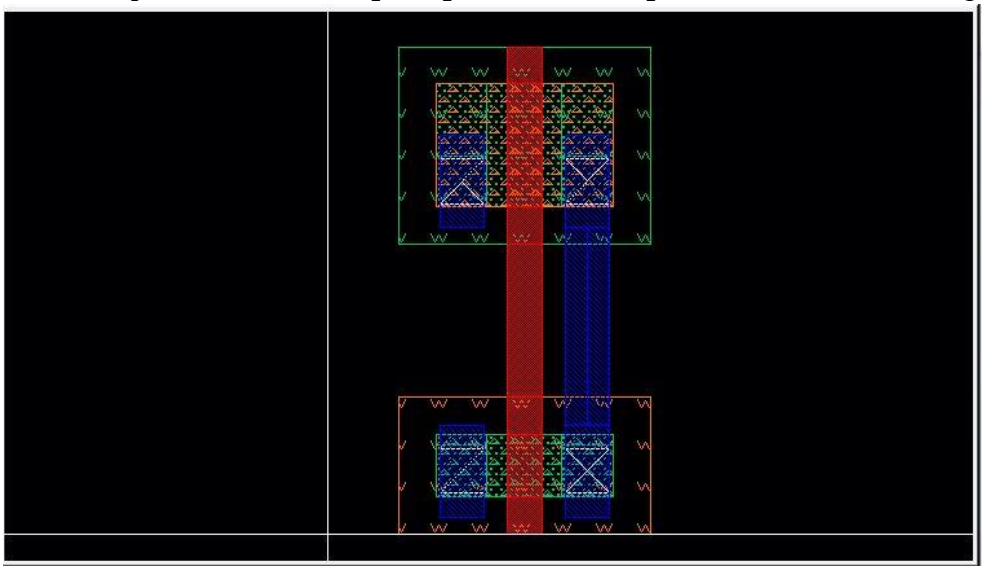
Step 4: Creating path

Layer selection window, select **poly**





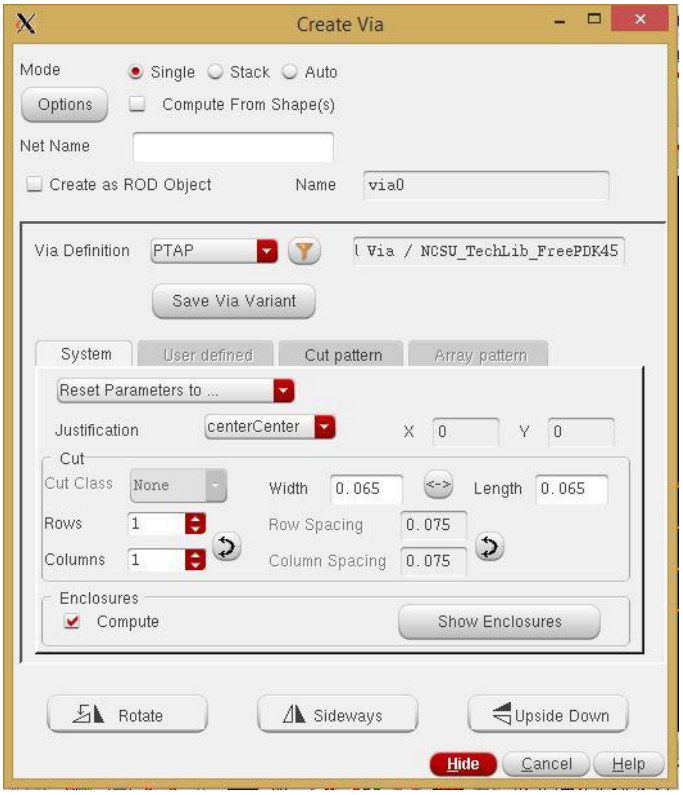
To create path, **create→ shape→ path**, shortcut "**p**". You have to connect poly's of NMOS and PMOS.

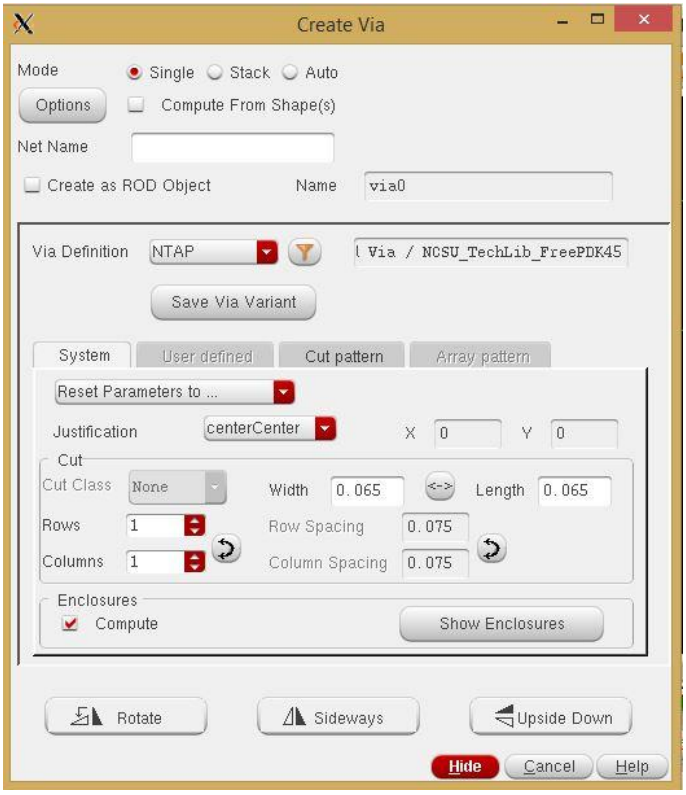


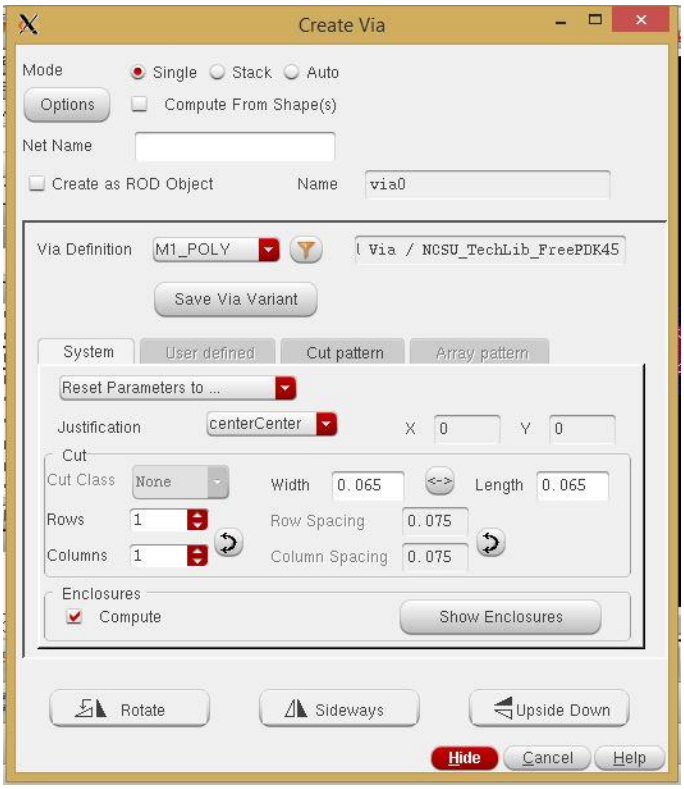
For connecting metal select **metal1** in layer selection window.

Step 5: Creating taps:
Create → via, Shortcut "**o**"

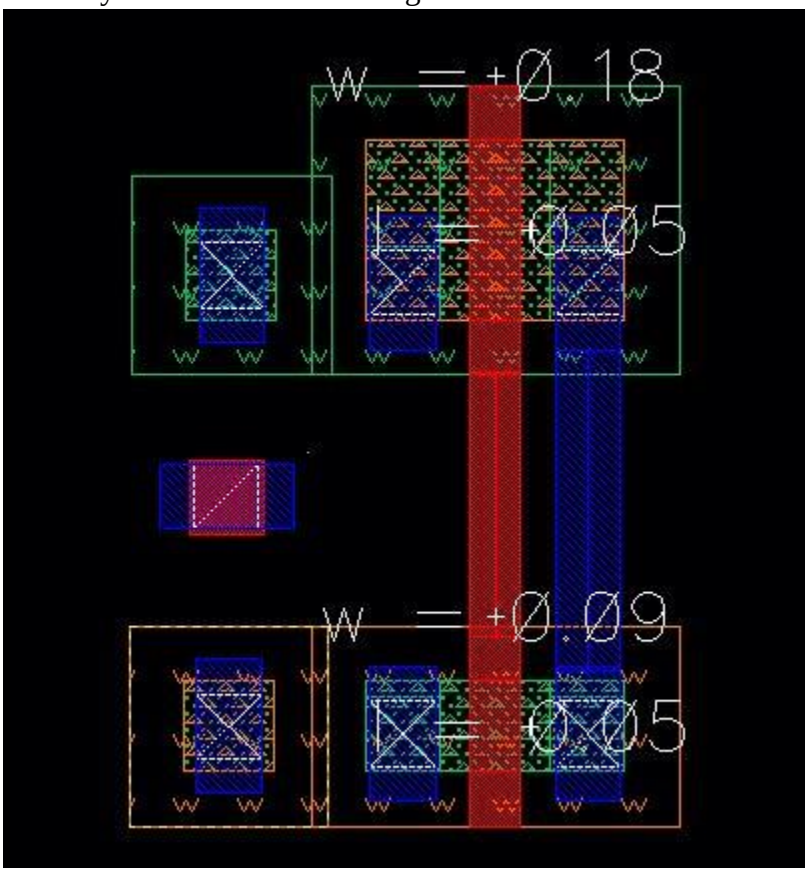
To connect two different layers, we use taps. In our design, we'll be using NTAP, PTAP and M1_poly taps as shown below.



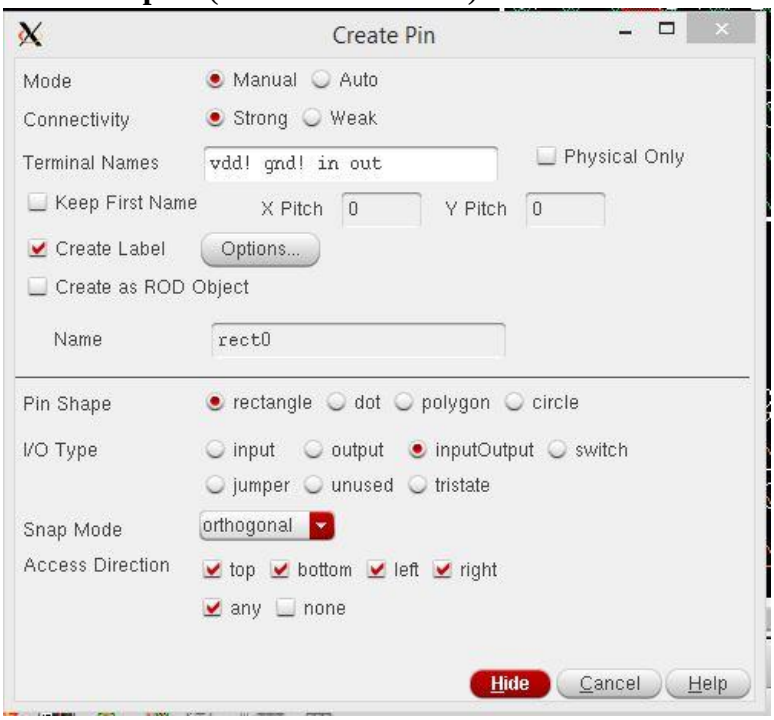




Your layout will look something like this.



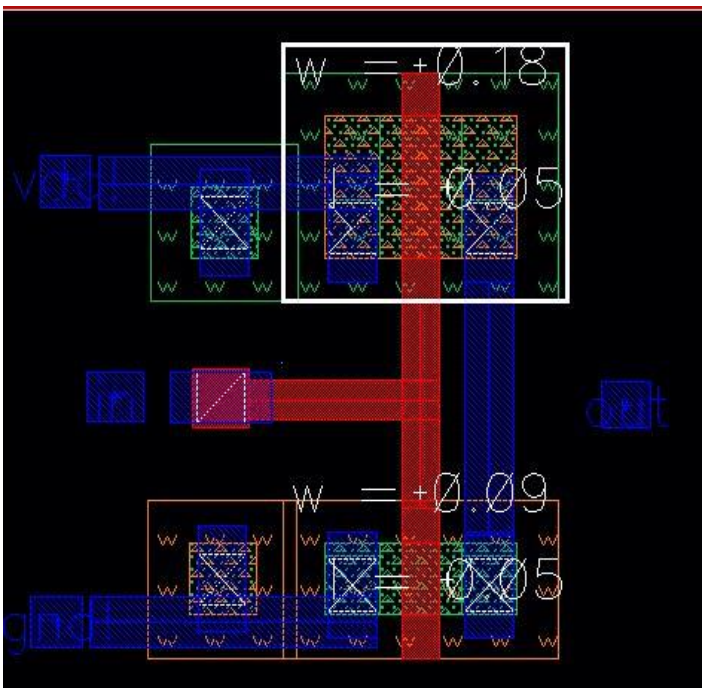
Step 6: Adding pins:
Create → pins (No shortcut for this)

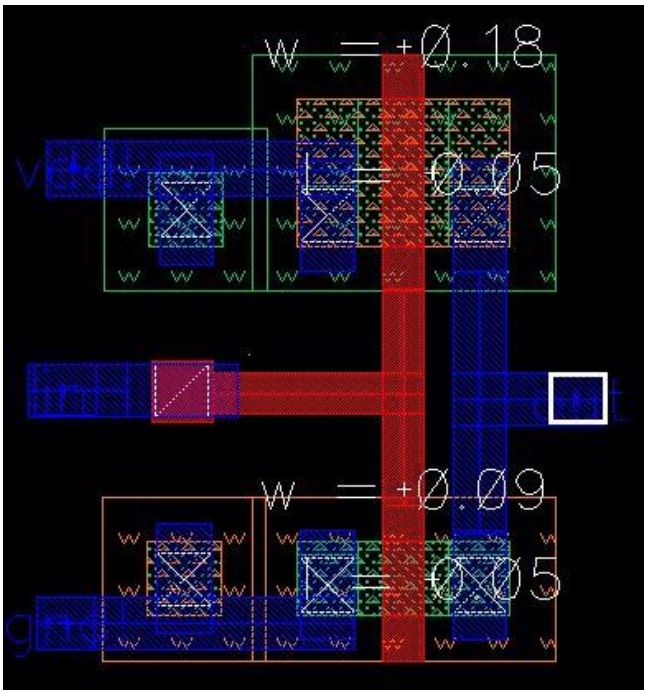


In the terminal name, type the names of all the pins you have used in your schematic. For vdd and gnd you have to add an exclamation (!). **vdd → vdd!** **gnd → gnd!**

Select create label, then click on options.
Height = 0.05
Layer name = metal1
Layer purpose = drawing

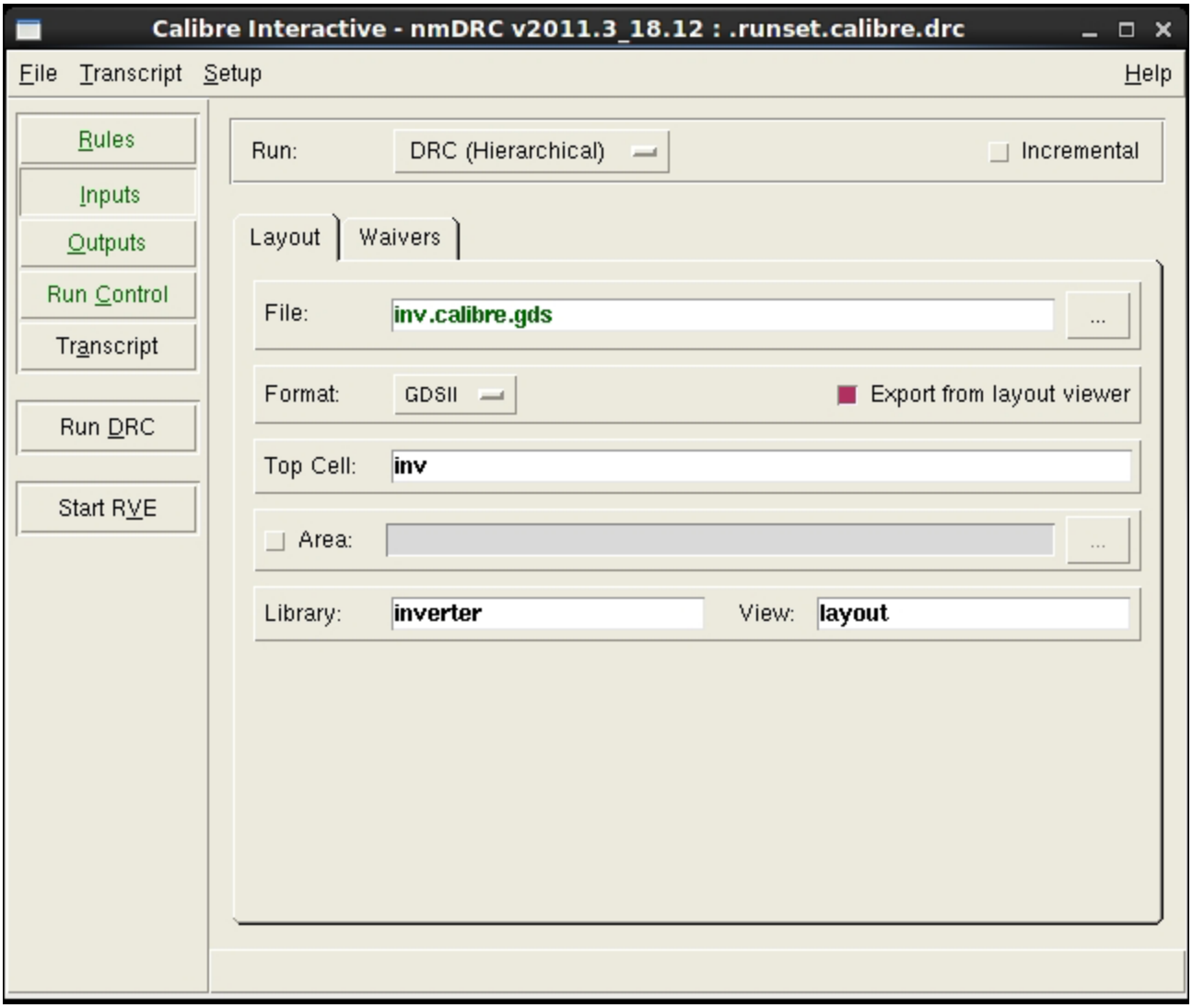
Finally





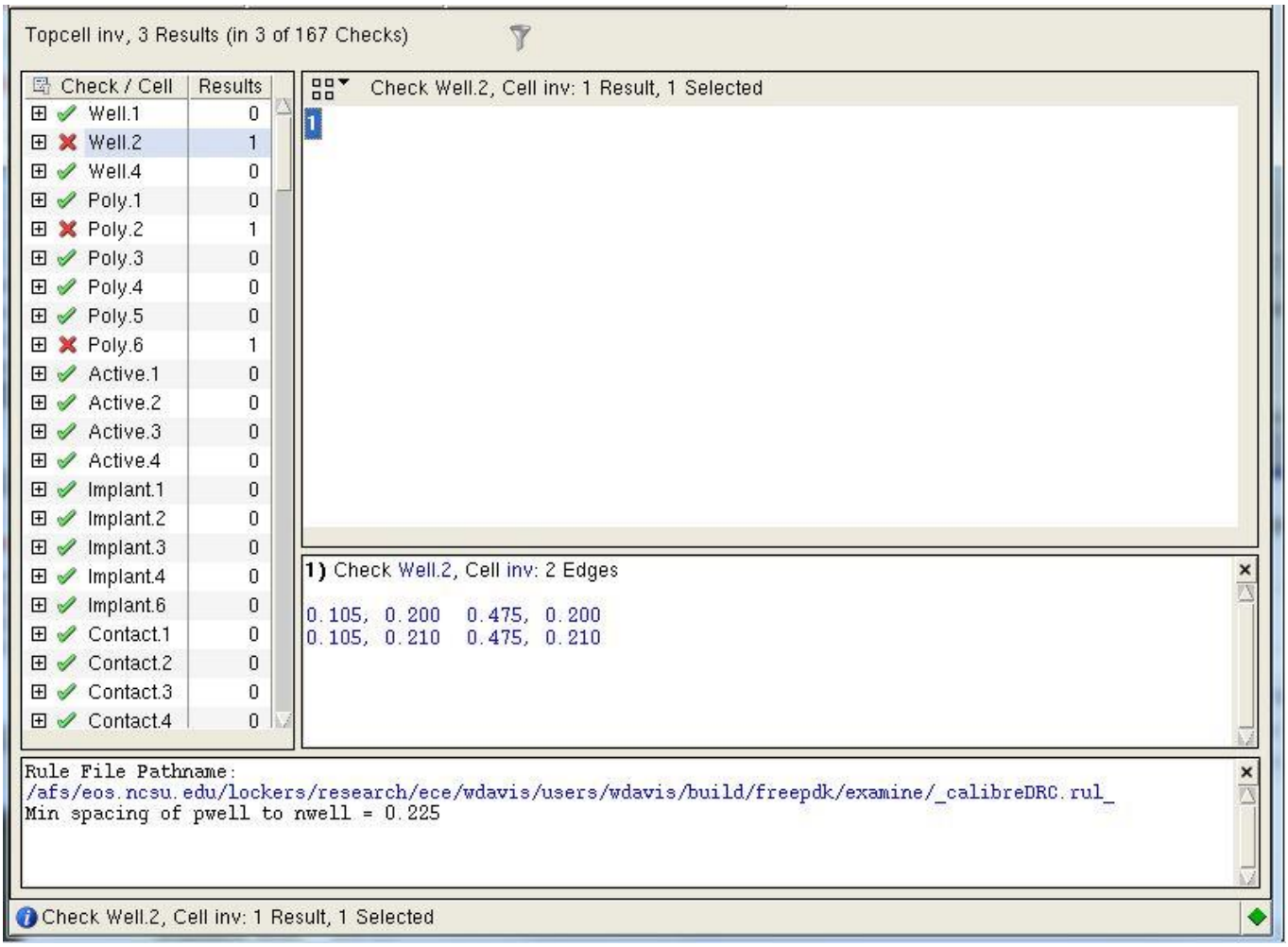
Step 7: Run DRC

To perform a Design Rule Check (DRC), choose **Calibre->Run DRC…**. The DRC form appears, as shown below. Then click "Run DRC". In **inputs**, change file to **inv.calibre.gds (inv is the name of the cell)**

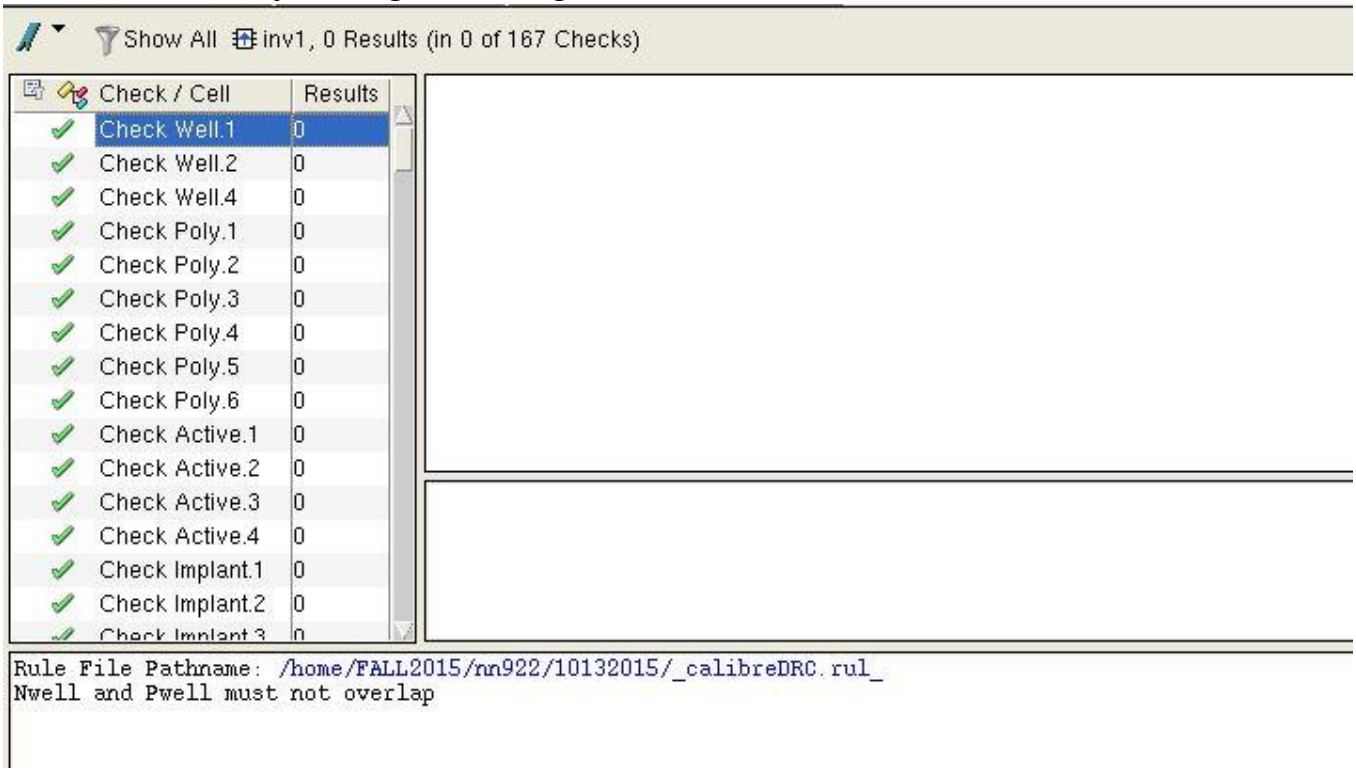


Viewing DRC Errors

You can learn about the errors by clicking on the rule in the Results Viewing Environment (RVE) window that pops up after DRC is complete. Click on an error and hit "shift-H" to highlight the error in the layout viewer as shown. NOTE: In order for Shift-H to work as described here, in the DRC RVE window, choose **Setup->Options,** select "Zoom cell view to highlights by 0.7", and click "OK".

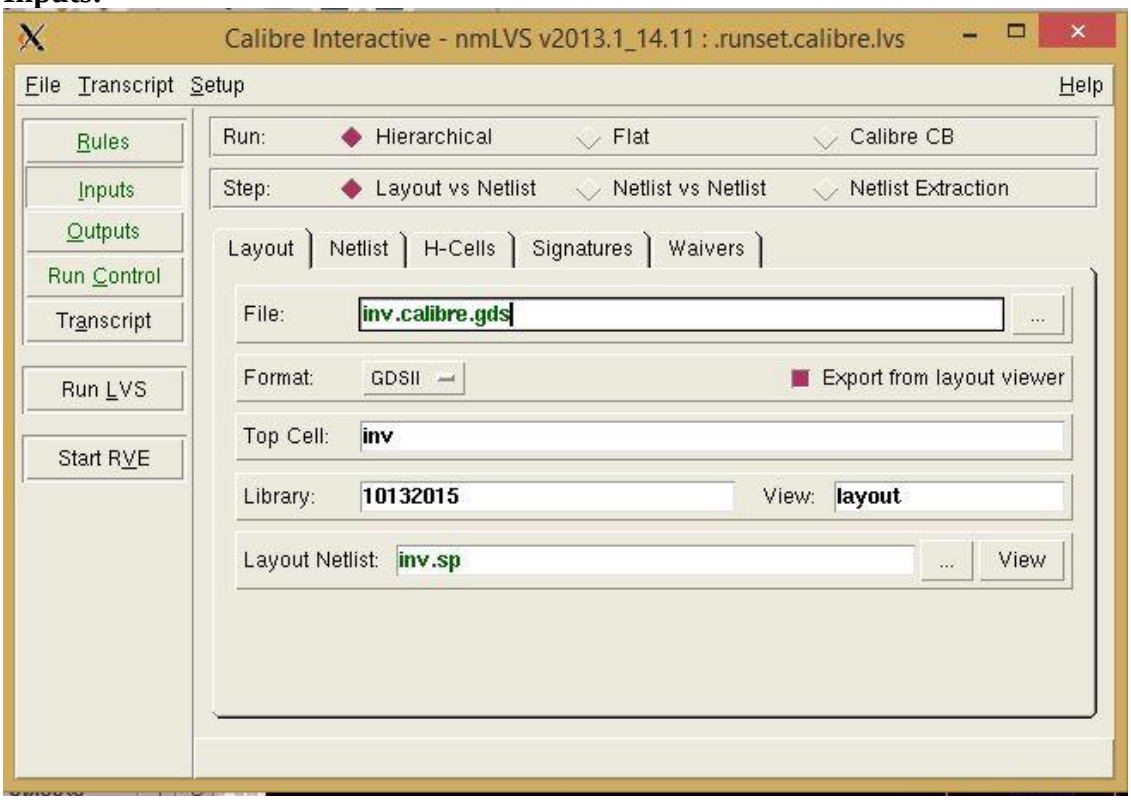


If there are no errors you will get something like this.



Step 8: LVS
Calibre → run LVS

Inputs:

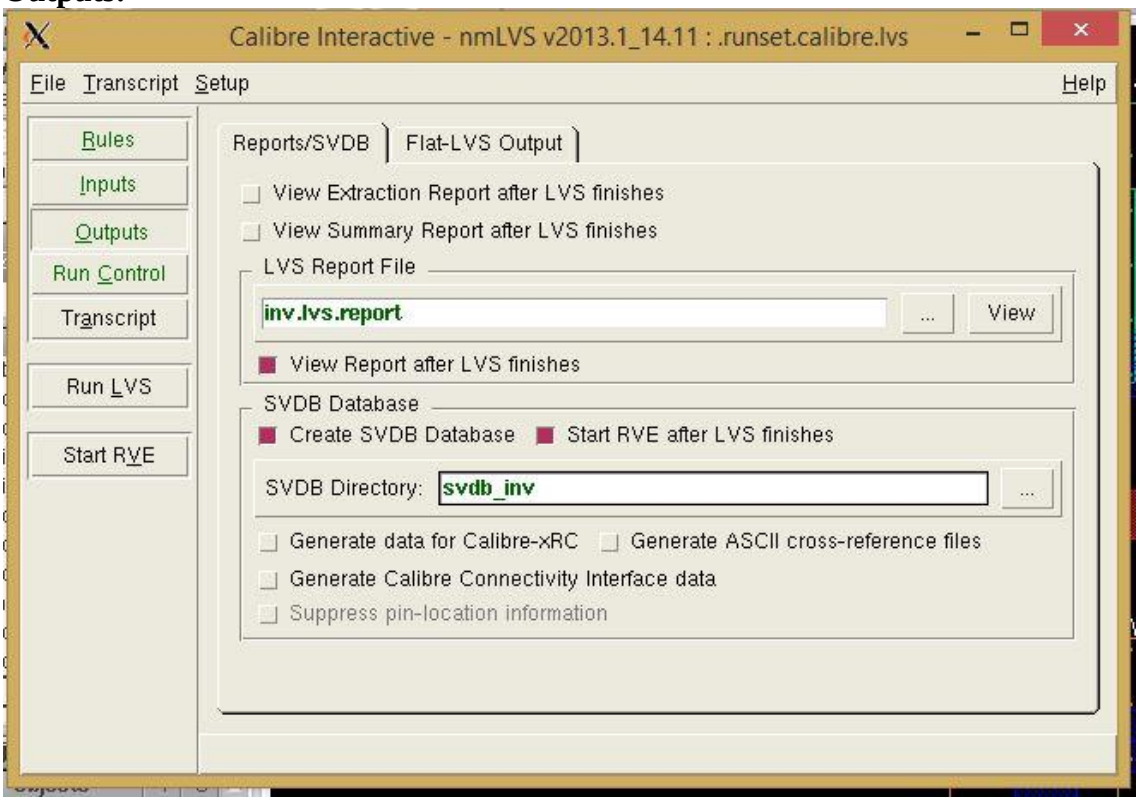


Select "Hierarchial", "Layout vs Netlist" Under the Layout tab
Files : inv.calibre.gds(what names you did save as:inv would be changed) Top Cell: inv

Layout Netlist: inv.sp
These options are already be filled in by the tool, leave them as is
Format: select "GDSII" and select the option "Export from layout viewer" (This is very important)

Under the Netlist tab
Files: inv.src.net Top Cell:inv
These options are already be filled in by the tool, leave them as it is
Format: select "SPICE" and select the option "Export from schematic viewer" (This is very important)

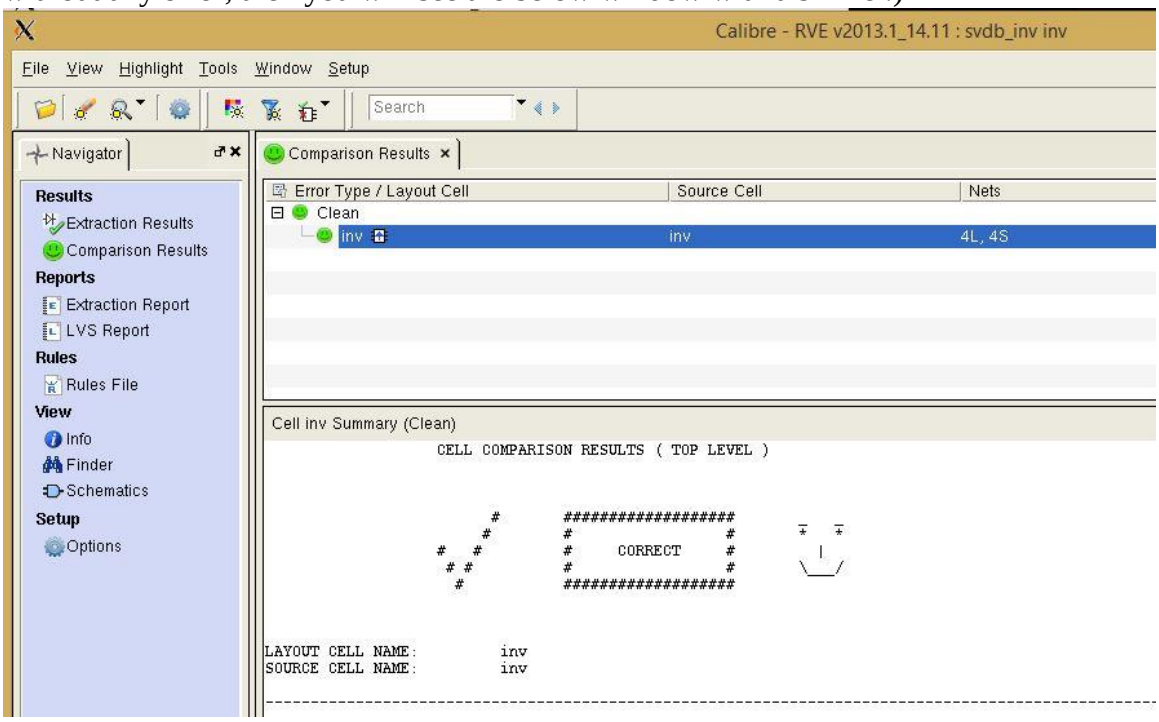
Outputs:



Under the Report/SVDB
LVS Report File: inv.lvs.report
This option is already be filled in by the tool, leave it as is svdb directory: svdb_inv
Select "View Report after LVS Finishes"

Perform an LVS Check without Errors

Set the LVS form with the options shown above. Then click the “Run LVS” button. If LVS runs successfully, without any error, then you will see the below window with a smilie :)



Click on the "Transcript" tab in Calibre Interactive - LVS to see the log file.

Note: Hot keys that are used during design.
i: Add instances
q: Edit properties
r: Add rectangles
p: Add path
P: Add Polygon
ctrl+p: Add a pin
l: Label on a wire (Note - it sometimes does not work. Please use Create -> Label in this case.
z: Zoom in
Z: Zoom out by 2X
ctrl+z: Zoom in by 2X
f: fit the layout in your layout window
right mouse button: repeat last command
Hit "ESC" to come out of any mode.