HW-3

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Problem 1

a

$$Y = \overline{(B + A) \cdot C \cdot D} \tag{1}$$

b

As from the figure, suppose β_N denodes β for NMOS used in this design, β_n denodes β for NMOS in equivalent generic design. And β_P and β_p respectively. Thus we have $\beta_P = 2\beta_p$ and $\beta_N = 3\beta_n$. Thus for MOSFET really used in this design

$$\begin{aligned} \frac{W}{L}_{NMOS} &= 3 \\ \frac{W}{L}_{PMOS} &= 4 \end{aligned} \tag{2}$$

c

Suppose internal capacitance for each NMOS is C_n, and C_p for PMOS respectively.

Initial State	Final State	Delay
$A_1B_0C_1D_0$	$A_1B_0C_1D_1$	$t_{pHL} \propto 3R_NC_N + R_NC_Y$
$A_0B_1C_1D_0$	$A_0B_1C_1D_1$	
$A_0B_1C_1D_1$	$A_0B_0C_1D_1$	$t_{pLH} \propto R_PC_P + R_PC_Y$

Problem 2

Problem 3