HW-4

Chi Zhang

14/10/2015

Problem 1

$r = \frac{135.75}{90}$. $t_{pLH} = t_{pHL} = 0.05ns$.

Please see Figure 1 for Candence simulation result.

Problem 2

a

Please see Figure 2 for NAND2 schematic, and Figure 3 for NOR2 schematic.

b

Please see Figure 4 to 7 for simulation results.

Gate	Input Pattern	t_{pLH}	t_{pHL}
NAND2	A = 1, B pulse	84 ps	48 ps
	A pulse, B = 1	81 ps	59 ps
NOR2	A = 0, B pulse	52 ps	83 ps
	A pulse, B = 0	61 ps	80 ps

c

For NAND2, input pattern A = 1, B is 0 to 1 has the worst low-to-high delay; input pattern A is 1 to 0, B = 1 has the worst high-to-low delay.

For NOR2, input pattern A = 0, B is 1 to 0 has the worst high-to-low delay; input pattern A is 0 to 1, B = 0 has the worst low-to high delay.

d

Gate	Input Pattern	Propogation delay p
NAND2	A = 1, B pulse	66 ps
	A pulse, B = 1	70 ps
NOR2	A = 0, B pulse	67.5 ps
	A pulse, B = 0	70.5 ps

Evidently, there is defferences as for propogation delay related to input pattern.

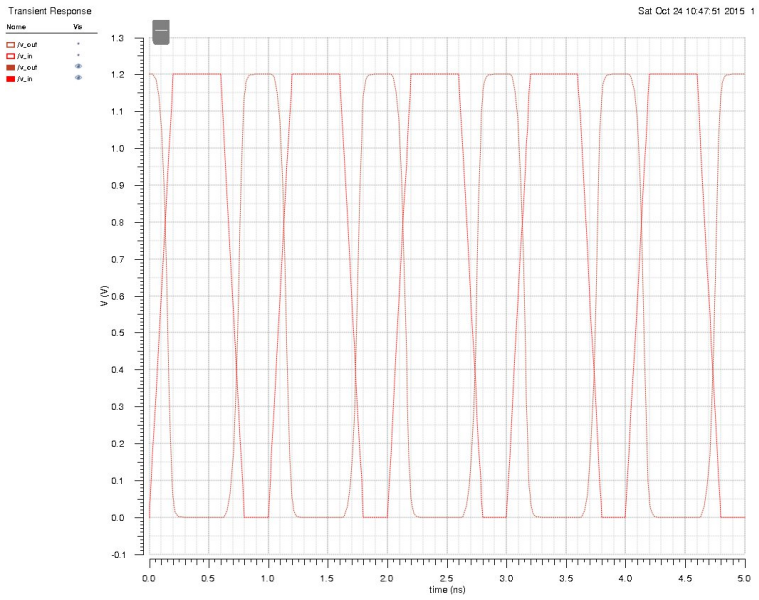

Figure 1: Q1

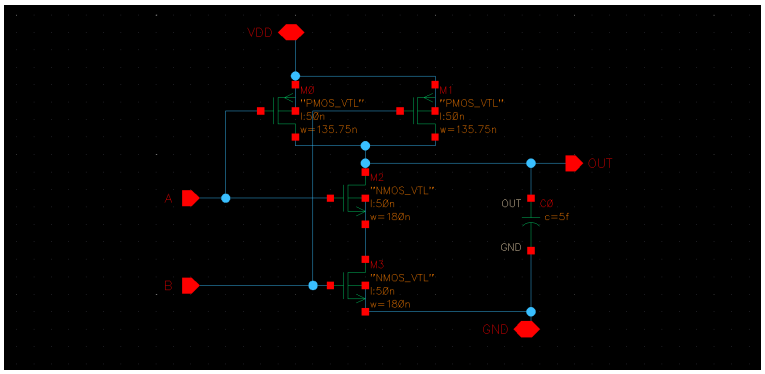

Figure 2: Q2.a: NAND2 schematic

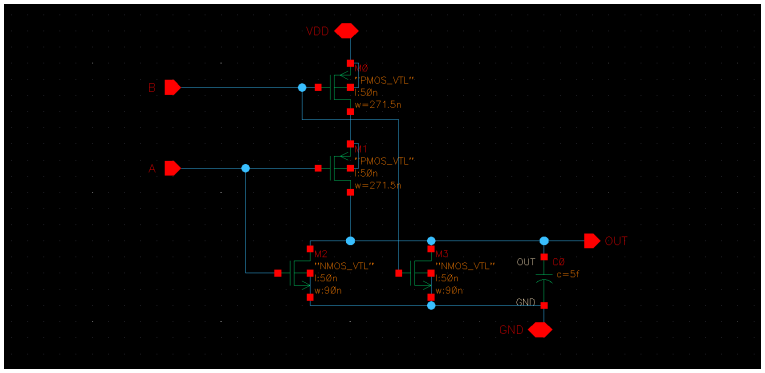

Figure 3: Q2.a: NOR2 schematic

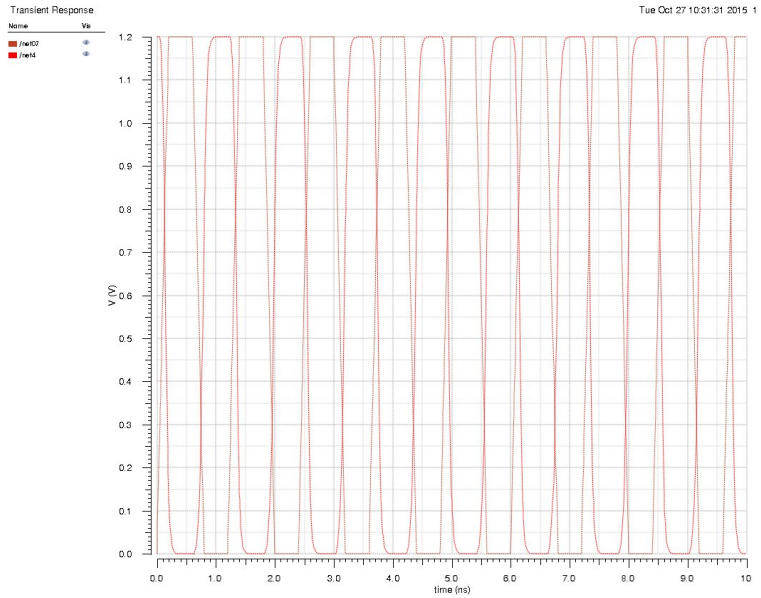

Figure 4: Q2.b: NAND2: A = 1, B pulse.

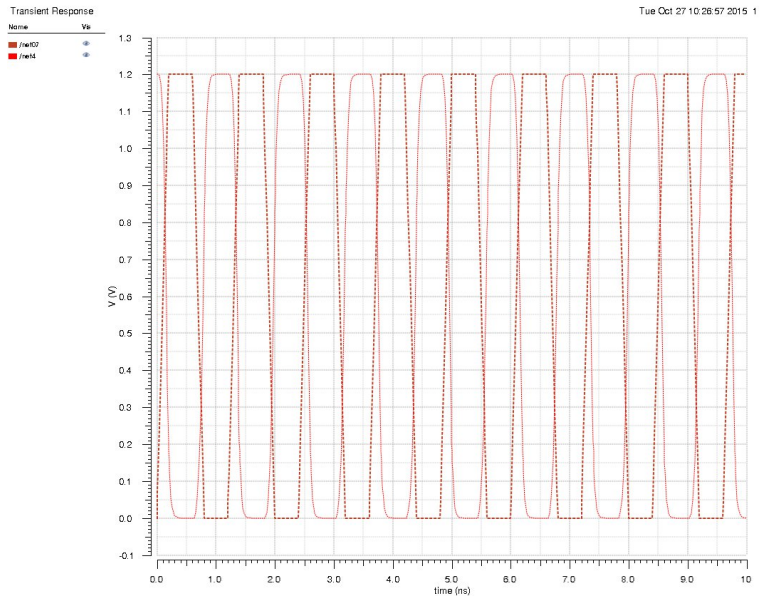

Figure 5: Q2.b: NAND2: A pulse, B = 1.

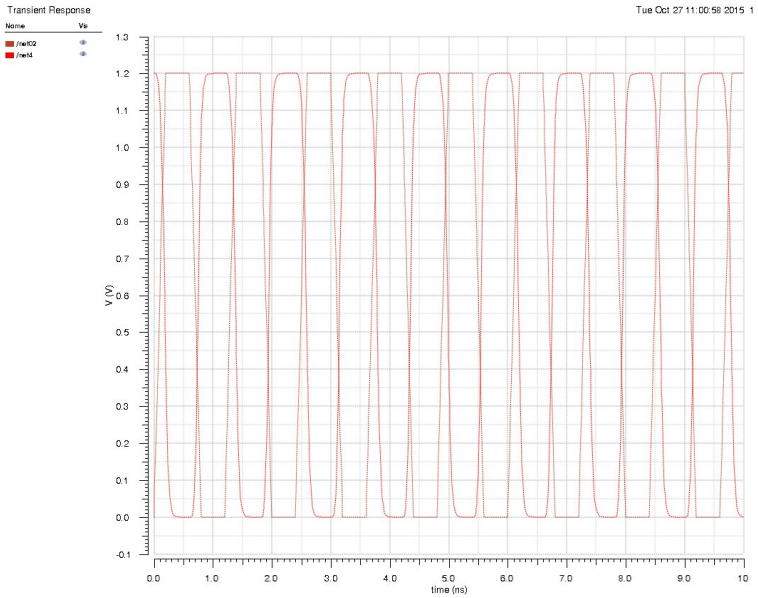

Figure 6: Q2.b: NOR2: A = 0, B pulse.

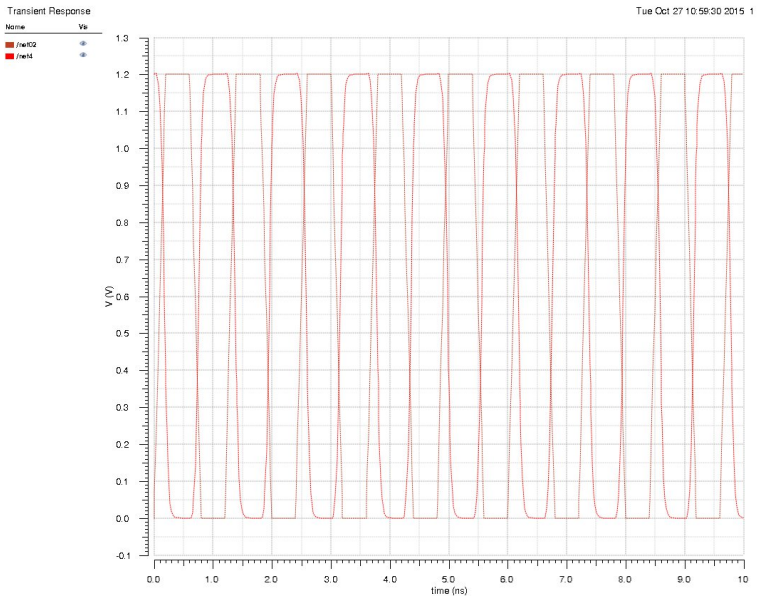

Figure 7: Q2.b: NOR2: A pulse, B = 0.

Problem 3

a

t_{pLH} for C_a should equals to t_{pLH} for C_L, hence,

$$R_n C_a ln(\frac{1}{1-\frac{\Delta V_a}{V_{DD}-V_{Tn}}}) = R_n C_L ln(\frac{1}{1-\frac{\Delta V_{out}}{V_{DD}}})$$
$$\frac{C_a}{C_L} = \frac{ln(\frac{1}{1-\frac{\Delta V_{out}}{V_{DD}}})}{ln(\frac{1}{1-\frac{\Delta V_a}{V_{DD}-V_{Tn}}})} \quad (1)$$

For $\Delta V_{out} = 0.6V$, $\Delta V_a = 1.4V$, thus $\frac{C_a}{C_L} = 0.2279$.
For $\Delta V_{out} = 0.8V$, $\Delta V_a = 1.2V$, thus $\frac{C_a}{C_L} = 0.4209$.
Thus, $0.2279 \leq \frac{C_a}{C_L} \leq 0.4209$.

b

For (i) A = 0, B = 0 to 1:
C_a is charged in precharge phase. Thus both C_L and C_a need to be discharged in evaluation phase.
For (ii) B = 1, A = 0 to 1:
Only C_L is charged in precharge phase. Thus only C_L needs to be discharged in evaluation phase.
Thus, case (ii) results in the lower high-to-low delay.