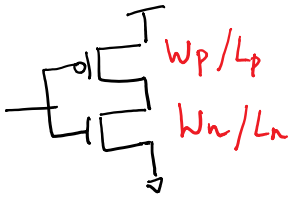
Sizing inverters for performance

Saturday, September 26, 2015 11:12 PM

By sizing we mean adjusting the Widths of PFET and NFET to achieve a given set of design constraints.



$L_p = L_n =$ minimum set by the technology

Lets say $\frac{W_p}{W_n} = \alpha$ where $W_n = W_{unit}$

Lets say we choose 'α' such that

$R_p = R_n = R_{unit}$.

With this we can achieve $t_{pLH} = t_{pHL}$ if $V_{tn} = |V_{tp}| = V_t$

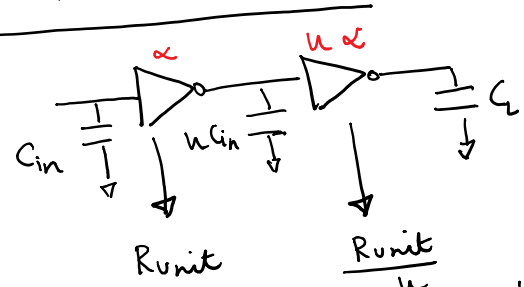
$t_d = 0.69 R_{unit} C_L$

The input capacitance of this inverter will be

$C_{in} = (1+\alpha) C_{gn}$ since $C_{gp} = \alpha C_{gn}$

Remember:- gate capacitance scales with the width.

2 inverter chain



At this time, we ignore the device parasitic capacitances

$t_d = t_{d,inv1} + t_{d,inv2}$

$t_{d,inv1} = 0.69 R_{unit} (u C_{in})$

$t_{d,inv2} = 0.69 \frac{R_{unit}}{u} (C_L)$

$t_d = 0.69 \underbrace{R_{unit} C_{in}}_{t_{p0}} \left[u + \frac{C_L}{C_{in}} \cdot \frac{1}{u} \right]$

$\underbrace{\quad}_{f}$

t_{po} f

f = Fan-out

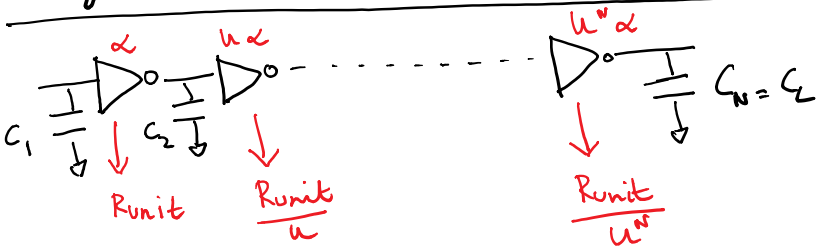
Fan-out tells us the ratio of the net load capacitance to the input gate capacitance of the first inverter.

$t_d = t_{po}\left[u + f/u\right]$ where $t_{po} = 0.69\, R_{unit}\, C_{in}$

to minimize $t_d \Rightarrow \frac{\partial t_d}{\partial u} = 0 \Rightarrow u_{opt}$

$$\boxed{\begin{aligned} u_{opt} &= \sqrt{f} \\ t_{d,opt} &= 2\sqrt{f}\, t_{po} \end{aligned}}$$

Sizing a chain of inverters for driving a large load



$C_2 = u\, C_1$

$C_3 = u\, C_2 = u^2 C_1$

$C_N = u^N C_1$

Each inverter is sized "u" times bigger than the previous stage.

$$t_{d,j} = 0.69\, R_j\, C_{j+1} = 0.69 \frac{R_{unit}}{u^j}\left(u^{j+1} C_1\right)$$

$$= \underbrace{0.69\, R_{unit}\, C_1\, u}_{\tau_r \text{ or } t_{po}}$$

$$t_{d,j} = \tau_r\, u$$

$$t_d = \sum_{j=1}^{N} \tau_r u = N u \tau_r$$

What is N? $\frac{C_L}{C_1} = u^N$ so $N = \frac{\ln\left(\overbrace{C_L/C_1}^{\text{FAN-OUT}}\right)}{\ln(u)} = \frac{\ln(f)}{\ln(u)}$

$$t_d = \frac{\ln(f)}{\ln(u)}\, u\, \tau_r$$

$t_d \Rightarrow \frac{\partial t_d}{\partial u} = 0 \Rightarrow u_{opt}$

$\ln(u)$

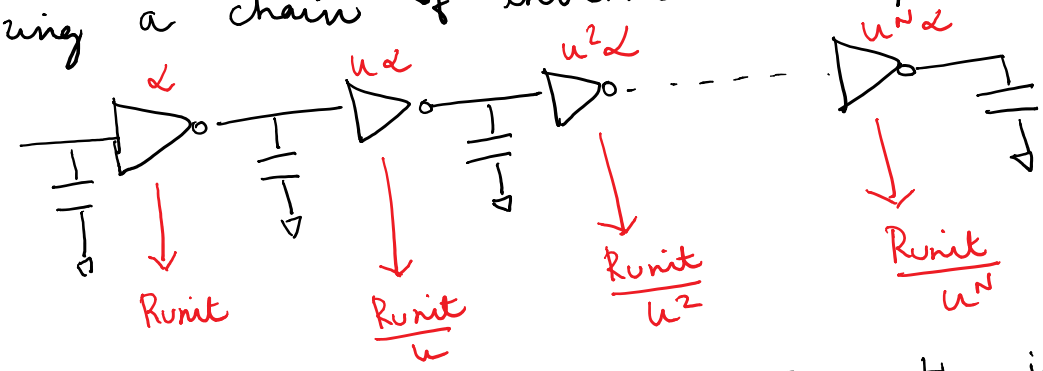
Minimize $t_d \Rightarrow \frac{\partial t_d}{\partial u} = 0 \Rightarrow u_{opt}$

$u_{opt} = e$

$N_{opt} = \ln(f)$

$\Rightarrow$ No parasitics were considered.

Sizing a chain of inverters with parasitics



Each capacitance now comes from the input cap. of the following stage and the parasitic cap. of that particular stage.

$$t_{d,j} = 0.69\, R_j \left[C_{FET,j} + C_{g,j+1} \right]$$

$C_{FET,j}$ ⇓ Parasitic; $C_{g,j+1}$ ⇓ gate

$$t_{d,j} = 0.69 \frac{R_{unit}}{u^j} \left[C_{FET,1}\, u^j + C_1\, u^{j+1} \right]$$

$$t_{d,j} = 0.69\, R_{unit} C_{FET,1} + 0.69\, R_{unit} C_1 u$$

$$t_d = \sum_{j=1}^{N} t_{d,j} = \underbrace{0.69\, R_{unit} C_{FET,1} N}_{\tau_x} + \underbrace{0.69\, R_{unit} C_1 N u}_{\tau_r}$$

"PARASITIC"

$$t_d = \underbrace{\tau_x N}_{\text{Does not depend on}} + \tau_r N u$$

does not depend on the sizing at all.

$$N = \frac{\ln(f)}{\ln(u)}$$

Minimize $t_d \Rightarrow \frac{\partial t_d}{\partial u} = 0 \Rightarrow u_{opt}$

$$u_{opt}\left[\ln(u_{opt}) - 1\right] = \tau_x/\tau_r = \frac{C_{FET,1}}{C_1}$$

$$N_{opt} = \frac{\ln(f)}{\ln(u_{opt})} \qquad f = C_L/C_1 \;(\text{FAN-OUT})$$

FINAL RESULT

Note:- When $\frac{\tau_x}{\tau_r} << 1$

then $u_{opt} = e$

Also, when τ_x is non-negligible, then # stages needed to optimize the delay are fewer than would be the case without τ_x.