Optimal choia of NFET/PFET ratio (shides 38-40) Saturday, September 26, 2015 8-40 PM



ASSUME: - Load suze = Driver size

That is, (W/L) LOAD = (W/L) rever for both PFET/NFET.

Lets say (WP/Wm) = 2 For both LOAD & DRIVER.

Ques: What should 'x' be for minimum delay?

CL = (1+ x) (FET-n + Cw + (1+x) (gn - gate capacitance)

 $t_{d} = 6.5 \frac{C_{L}V_{DD}}{\left(V_{DD}-V_{T}\right)^{2}} \left(\frac{1}{\beta_{W}} + \frac{1}{\beta_{P}}\right) V_{TM} = |V_{TP}| = V_{T}$

For CL = (I+ d) CFET-n + Cw+ (I+d) Cgn

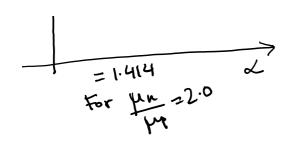
he see that to is a non-monotonic Function of 'd'.

. o For minimum delay, one must some

minimum
$$\frac{\partial t_d}{\partial x} = 0 \Rightarrow \frac{\partial t_d}{\partial y} = \frac{\int Im}{\int I + \frac{Gw}{G_{\text{Fein}} + G_{\text{gn}}}}$$

Final Answer

Typically In = 2 Mp



Typicary Mr = 2 Mp So Lopt ~ 1.414