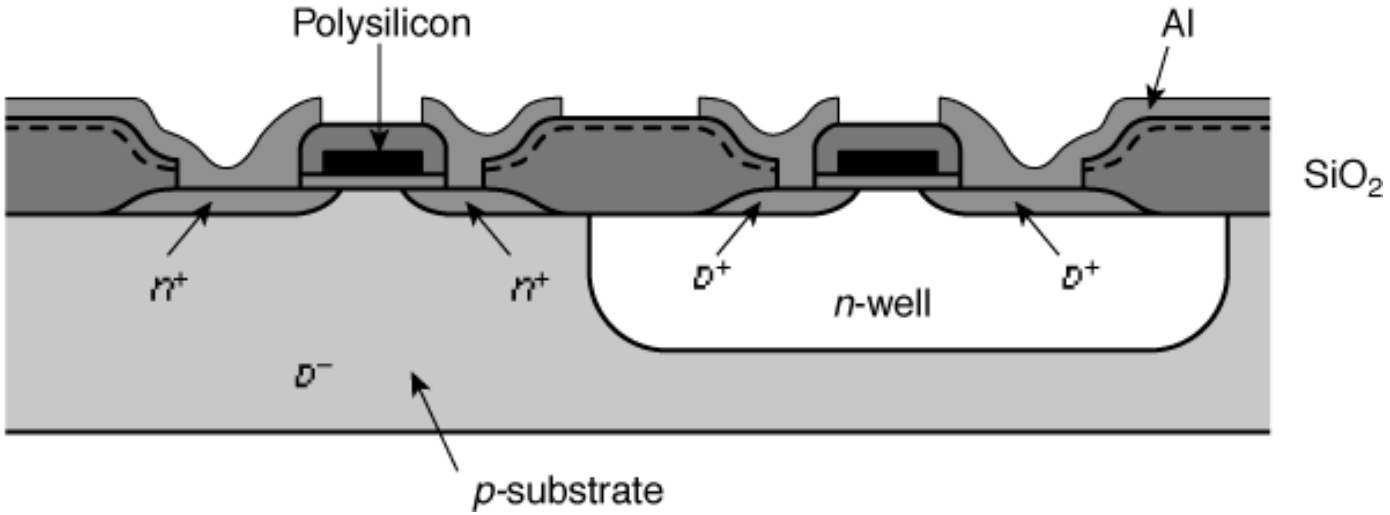
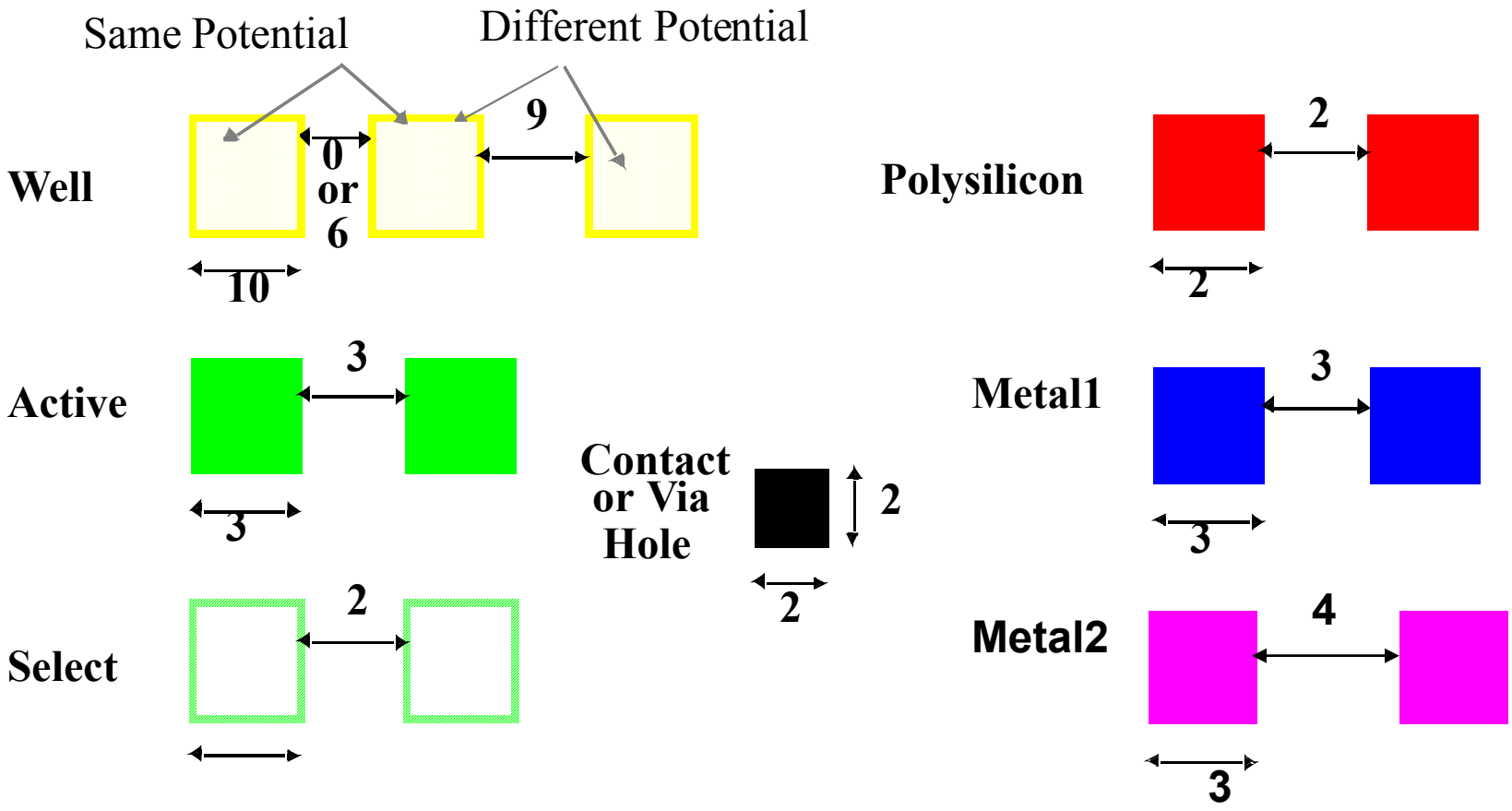
CMOS Process



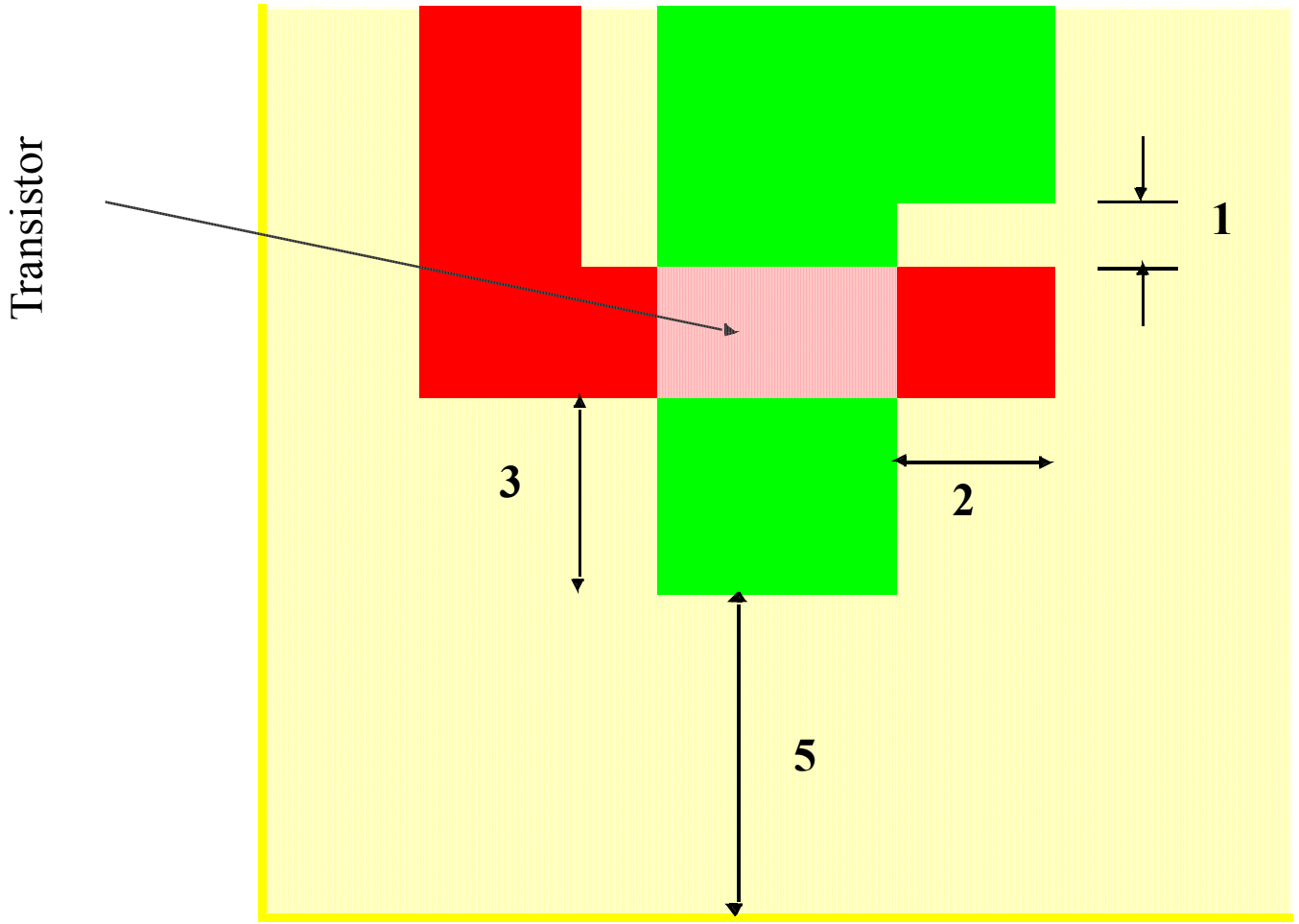
Design Rules

- Interface between designer and process engineer
- Guidelines for constructing process masks
- Unit dimension: Minimum line width
  - scalable design rules: lambda parameter
  - absolute dimensions (micron rules)

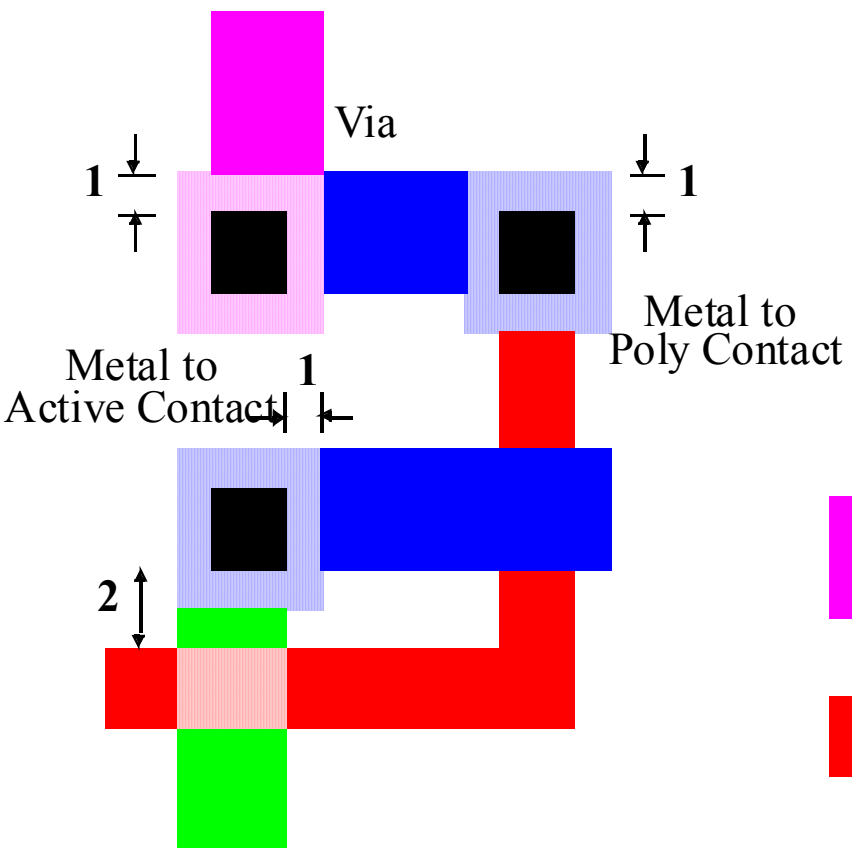
Intra-Layer Design Rules

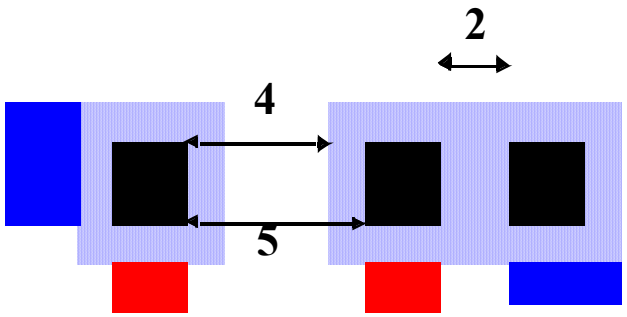


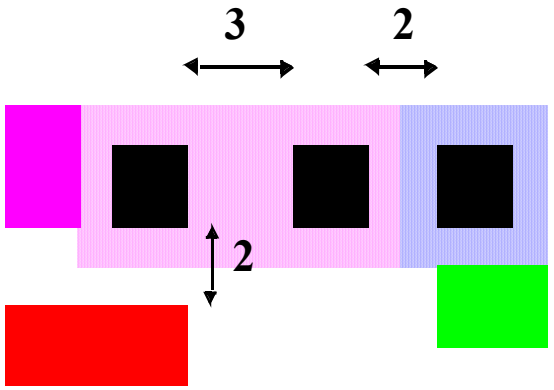
Transistor Layout



Vias and Contacts







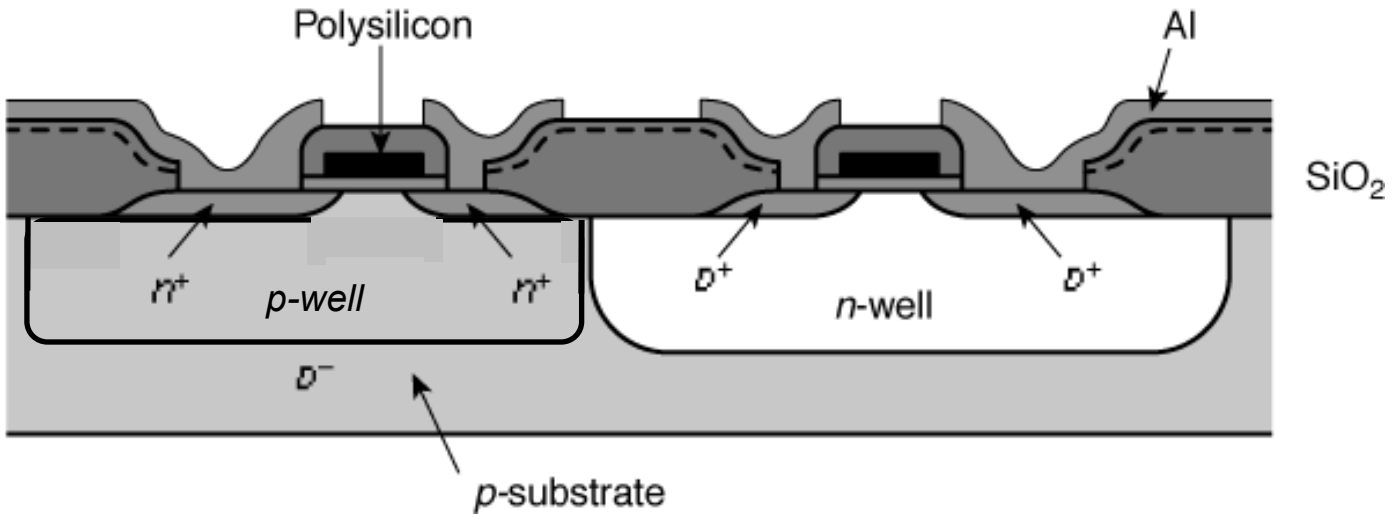
45nm Process

Layer	Purpose
Active	Active for NMOS and PMOS
Poly	Polysilicon line for NMOS/PMOS
Nwell	Nwell region for PMOS
Pwell	Pwell region for NMOS
Nimplant	Implant N+ to source/drain for NMOS
Pimplant	Implant P+ to source/drain for PMOS
Contact	Contacts - connect Metal1 to Poly or active
vthg	General use threshold implant
vthh	High threshold implant

45nm Process

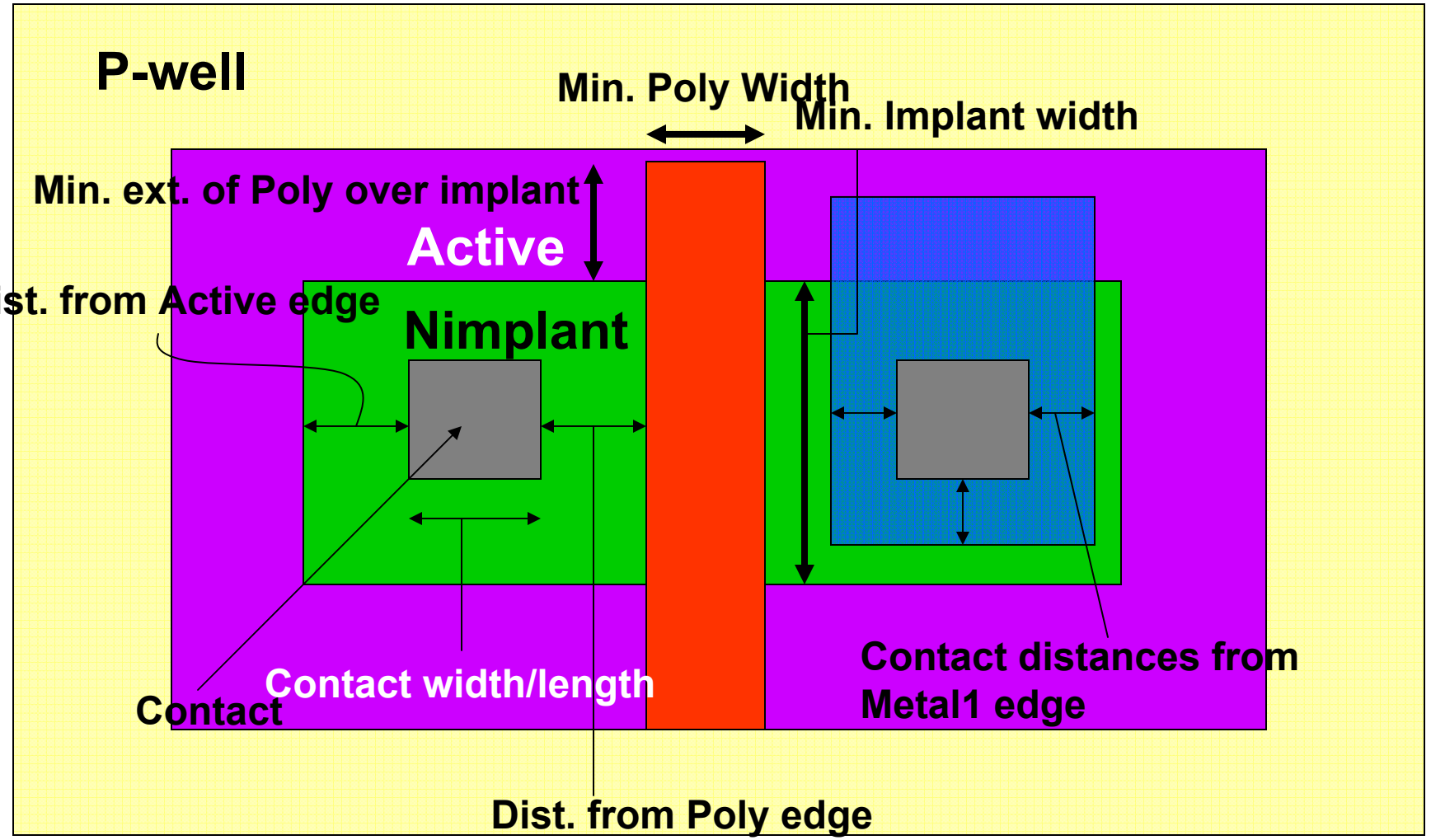
Layer	Purpose
Metal1 and Via1	**Metal 1 and Via 1 to connect Metal1 to Metal2**
Metal2 and Via2	**Metal 2 and Via 2 to connect Metal2 to Metal3**
Metal3 and Via3	**Metal 3 and Via 3 to connect Metal3 and Metal4**
Metal4	**Metal 4**
You should not need more than 4 levels of metals for the project	

NFET – Process View

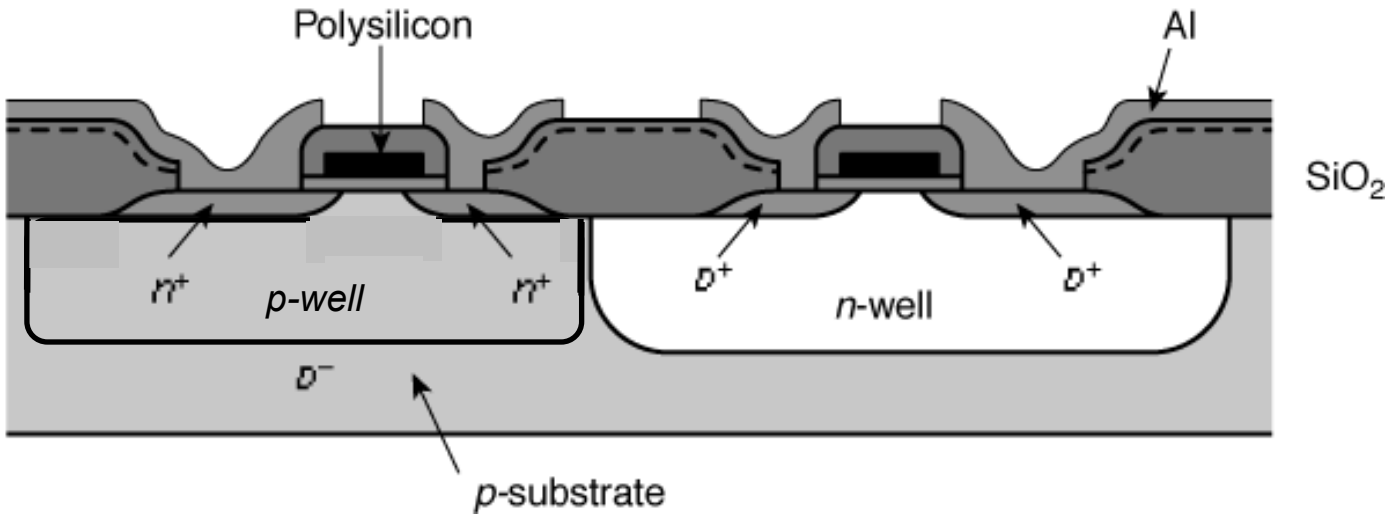


You need to identify the gate and source-drain -> Poly and Active
Poly-> gate,
Active -> total diffusion area
nimplant -> N+ implant for Source/Drain
Poly & nimplant overlap -> Transistor
You need to add P-well contact

Create NFET

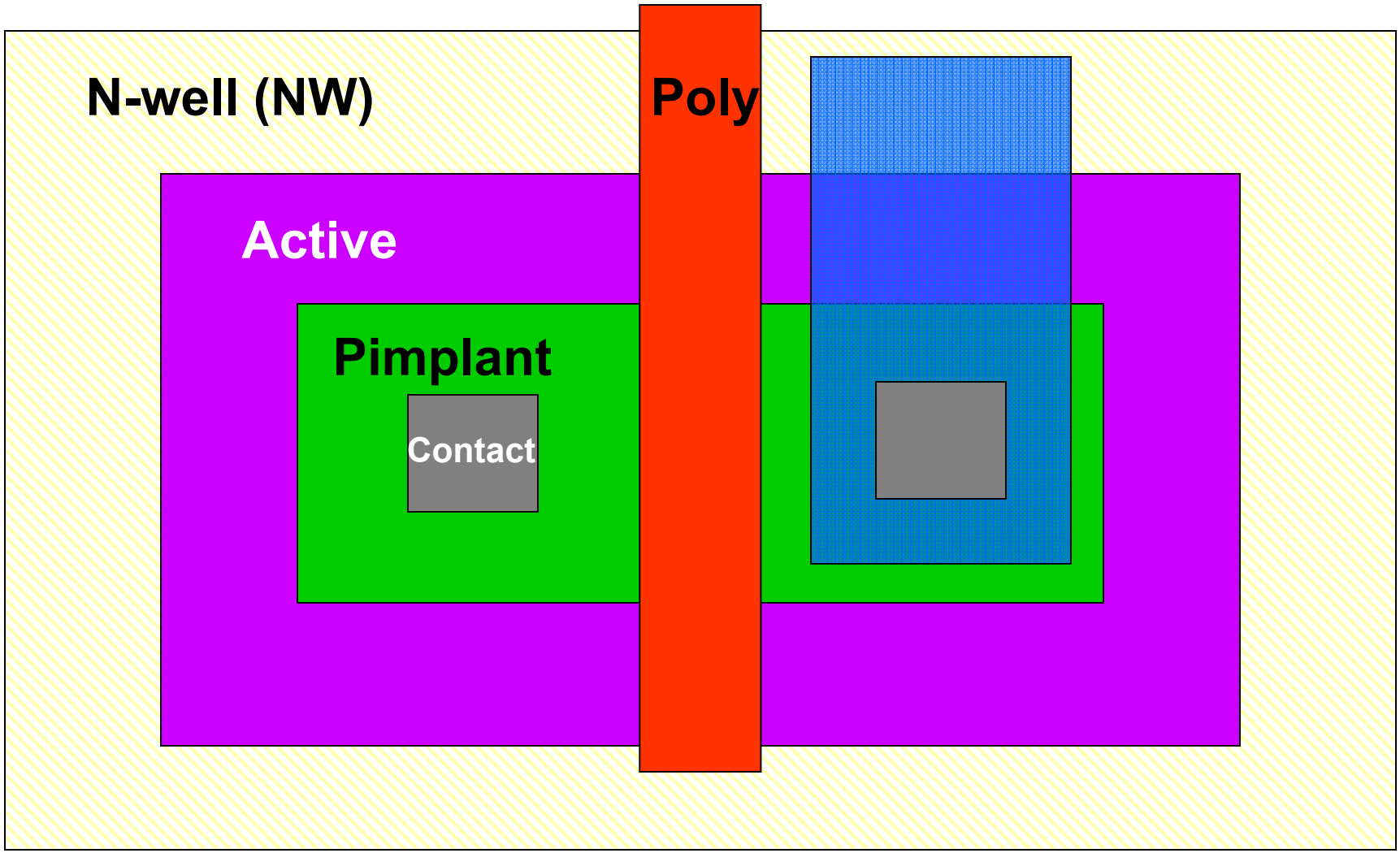

P-well
Min. Poly Width
Min. Implant width
Min. ext. of Poly over implant
Active
Dist. from Active edge
Nimplant
Contact
Contact width/length
Contact distances from
Metal1 edge
Dist. from Poly edge

PFET – Process View

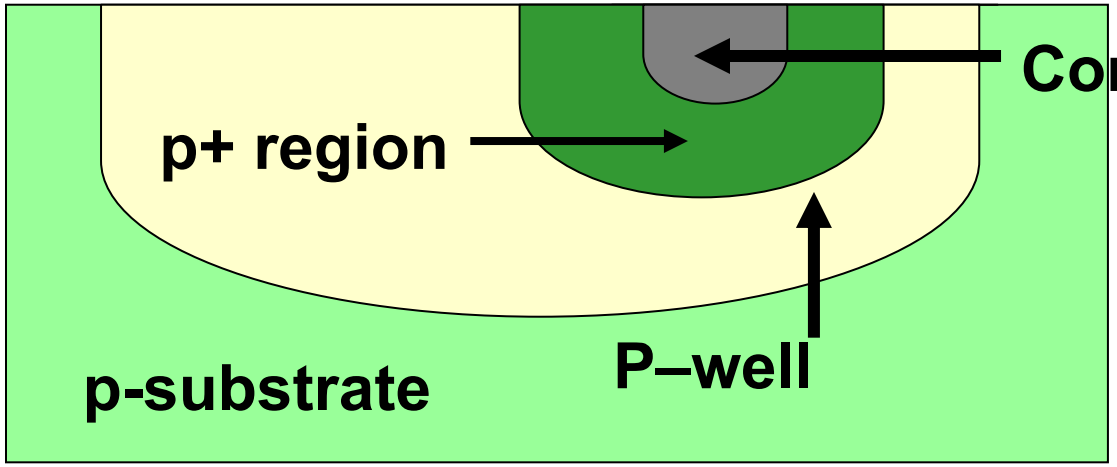


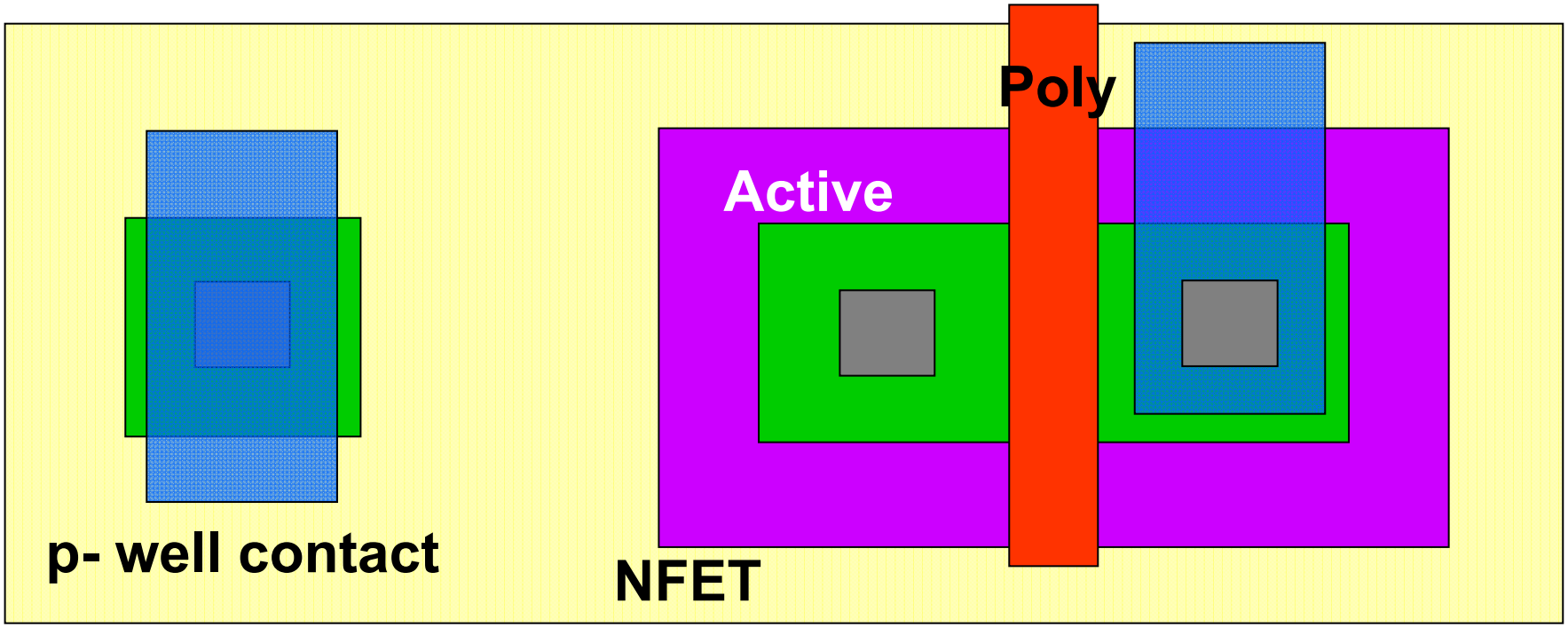
You need to identify the gate and source-drain -> Poly and Active
Poly -> gate,
Active -> total diffusion area
pimplant -> P+ implant for Source/Drain
Poly & pimplant overlap -> Transistor
You need to add N-well contact

Create PFET

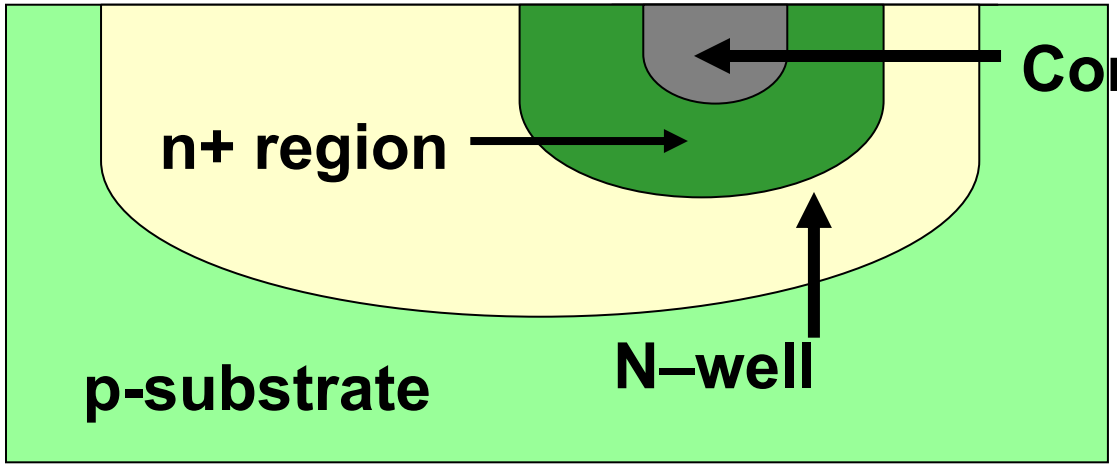


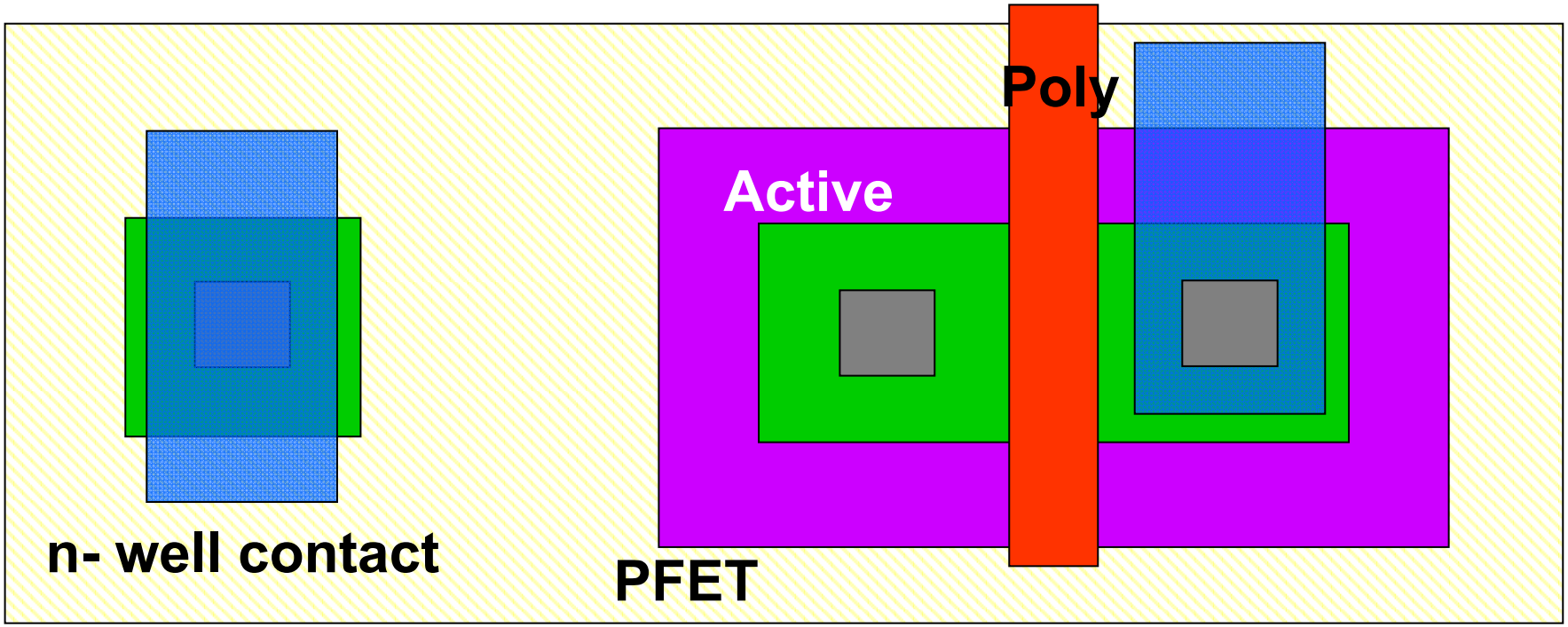
NFET with p-well Contact



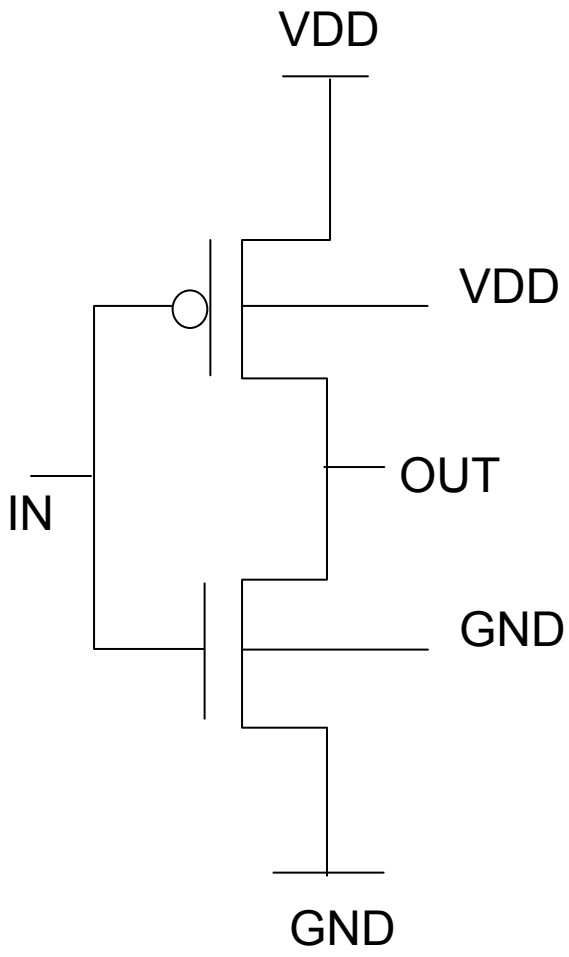


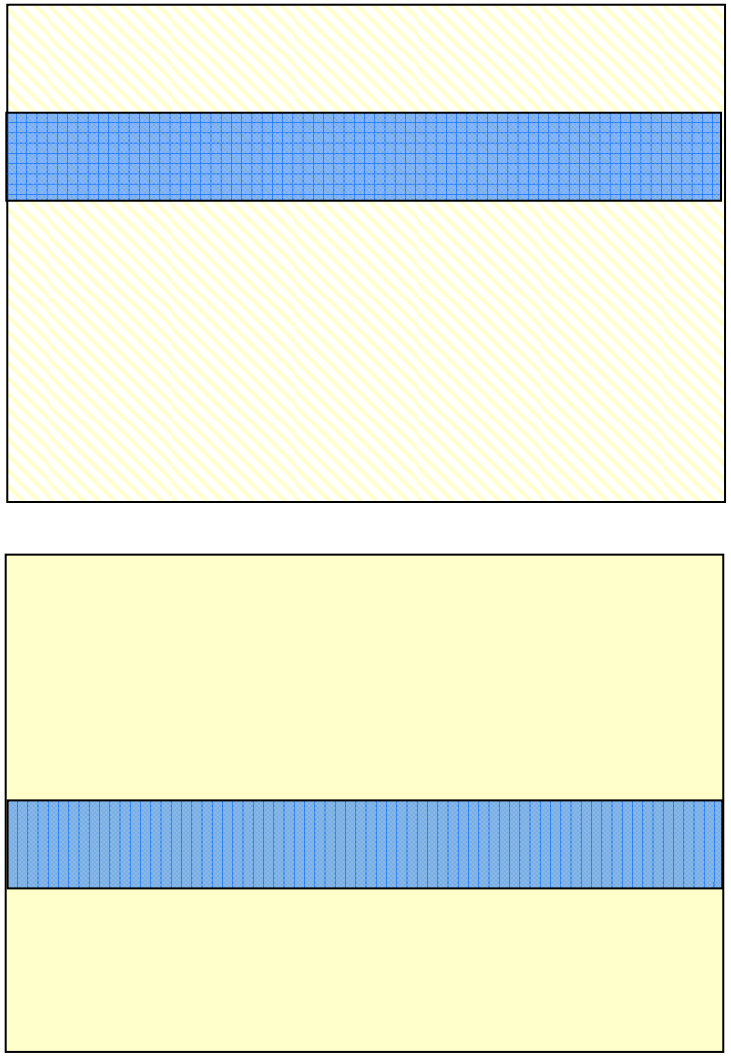
PFET with n-well Contact





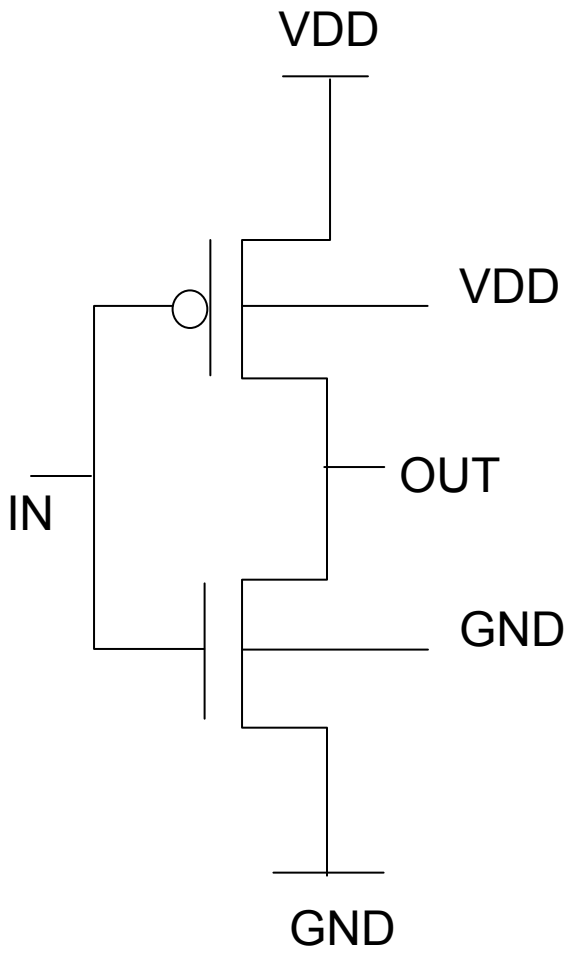
Create INVERTER

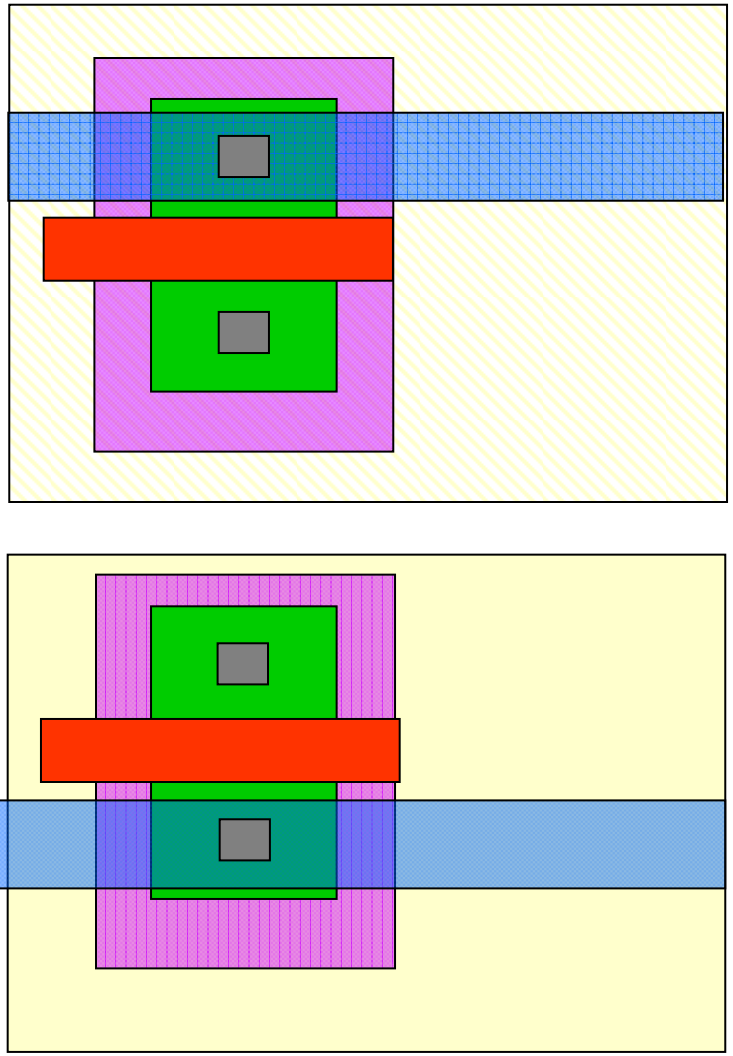




Set pitch of the cell using the power and ground buses.

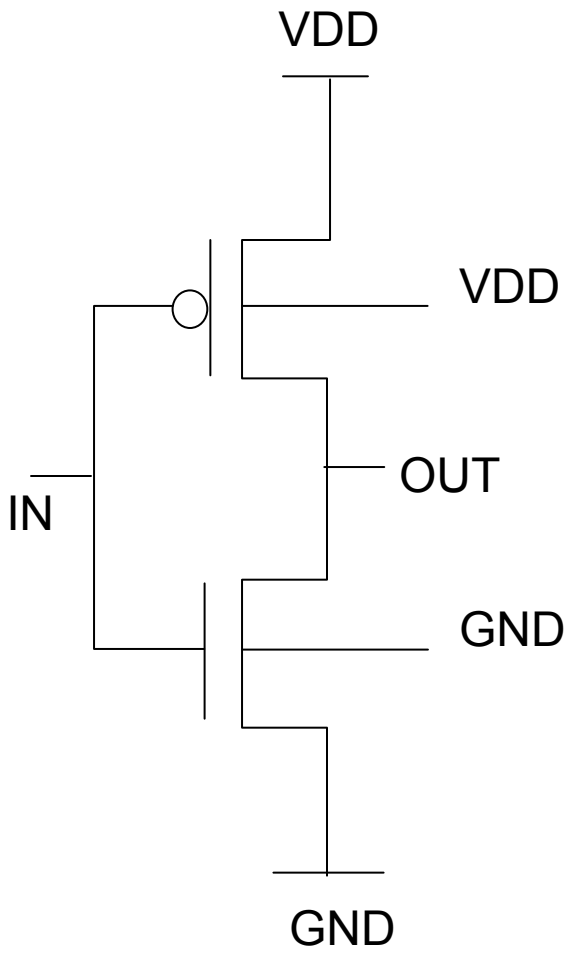
Create INVERTER

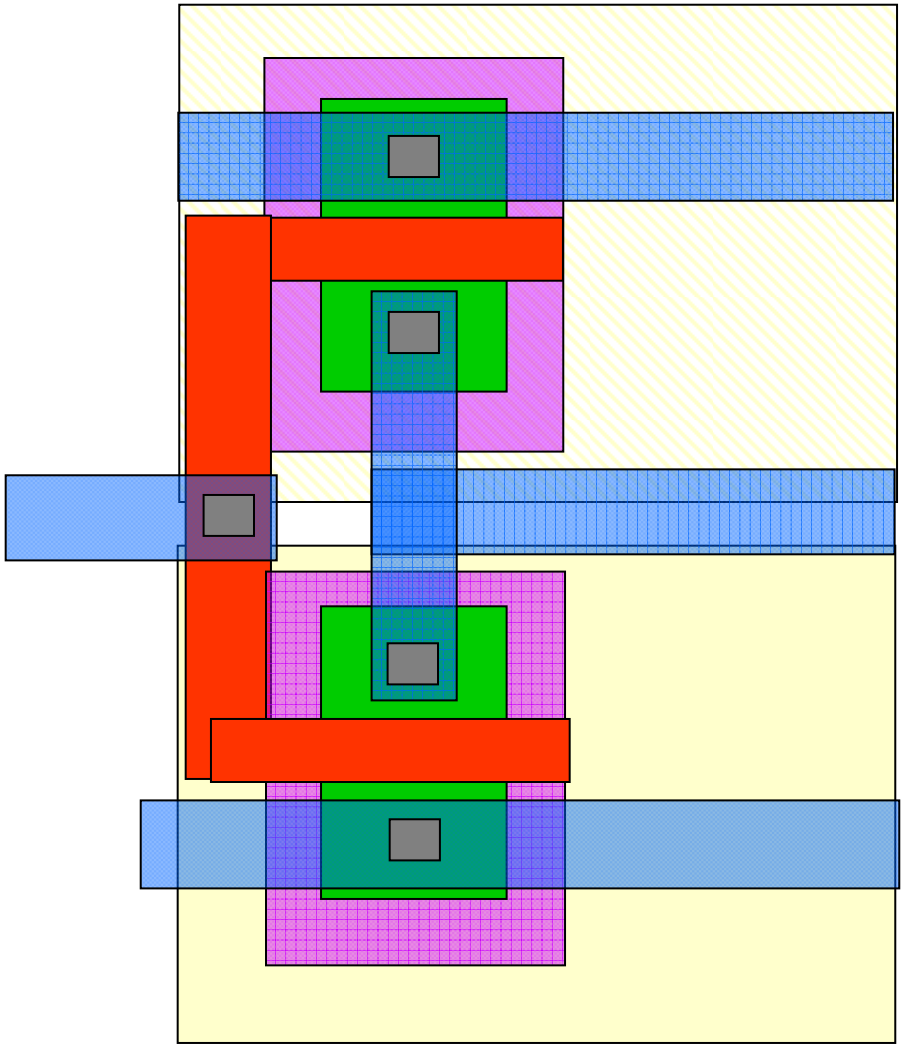




Add the transistors

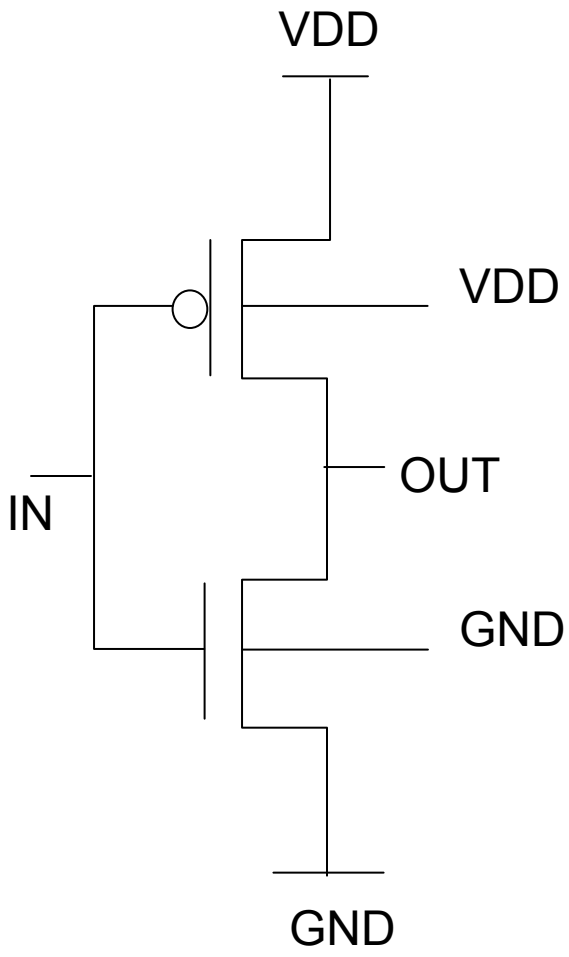
Create INVERTER

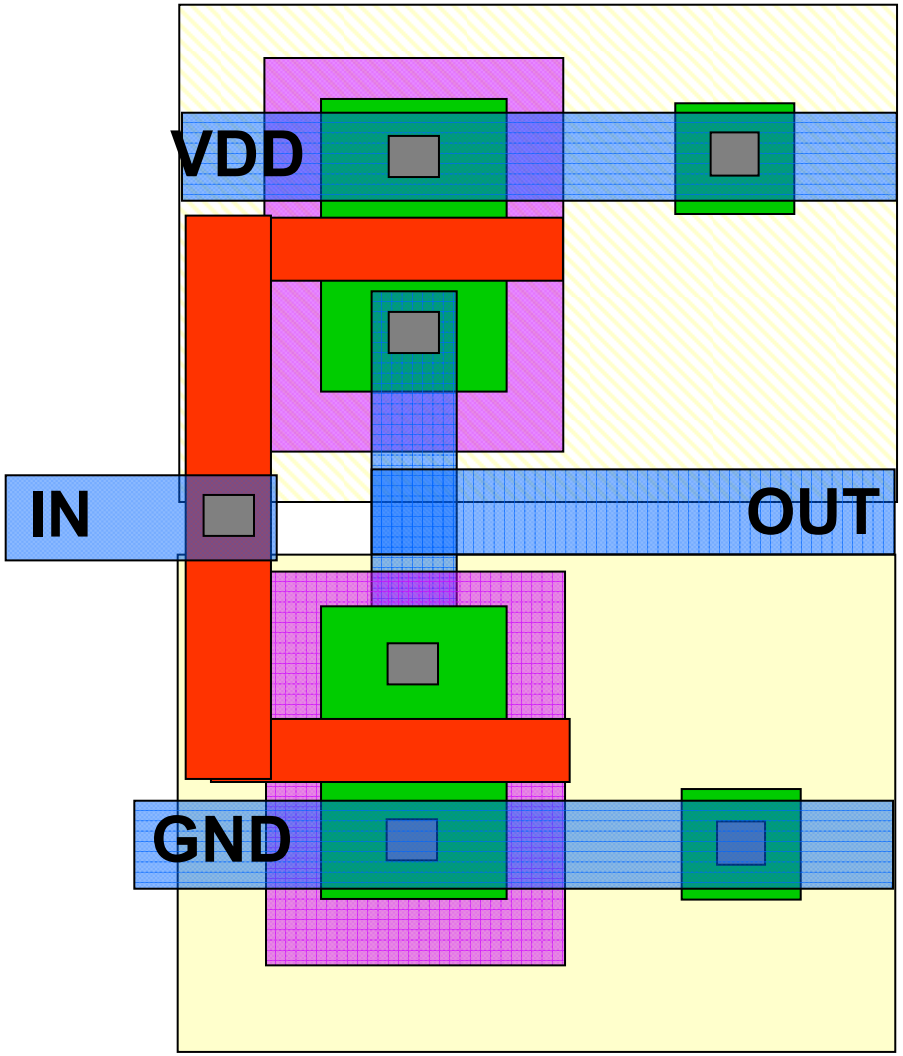




Connect the input/output lines

Create INVERTER





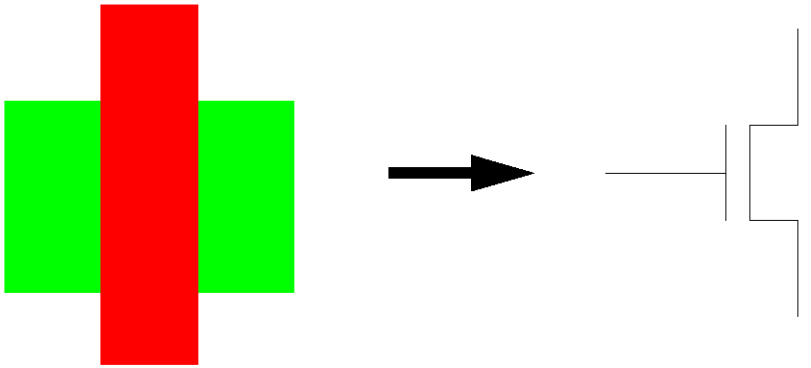
Add the p-well and n-well contacts

Design Error Check

- Design Rule Checker (DRC) –
  - Check whether design has validated any design rules
  - Ensures ‘manufacturability of design’
- Layout vs Schematic (LVS)
  - Ensures your layout matches with your schematic
  - Checks for shorts opens etc. in layout
  - Transistors and wire connections

Design Extraction

- Circuit extraction extracts a schematic representation of a layout, including transistors, wires, and possibly wire and device resistance and capacitance.



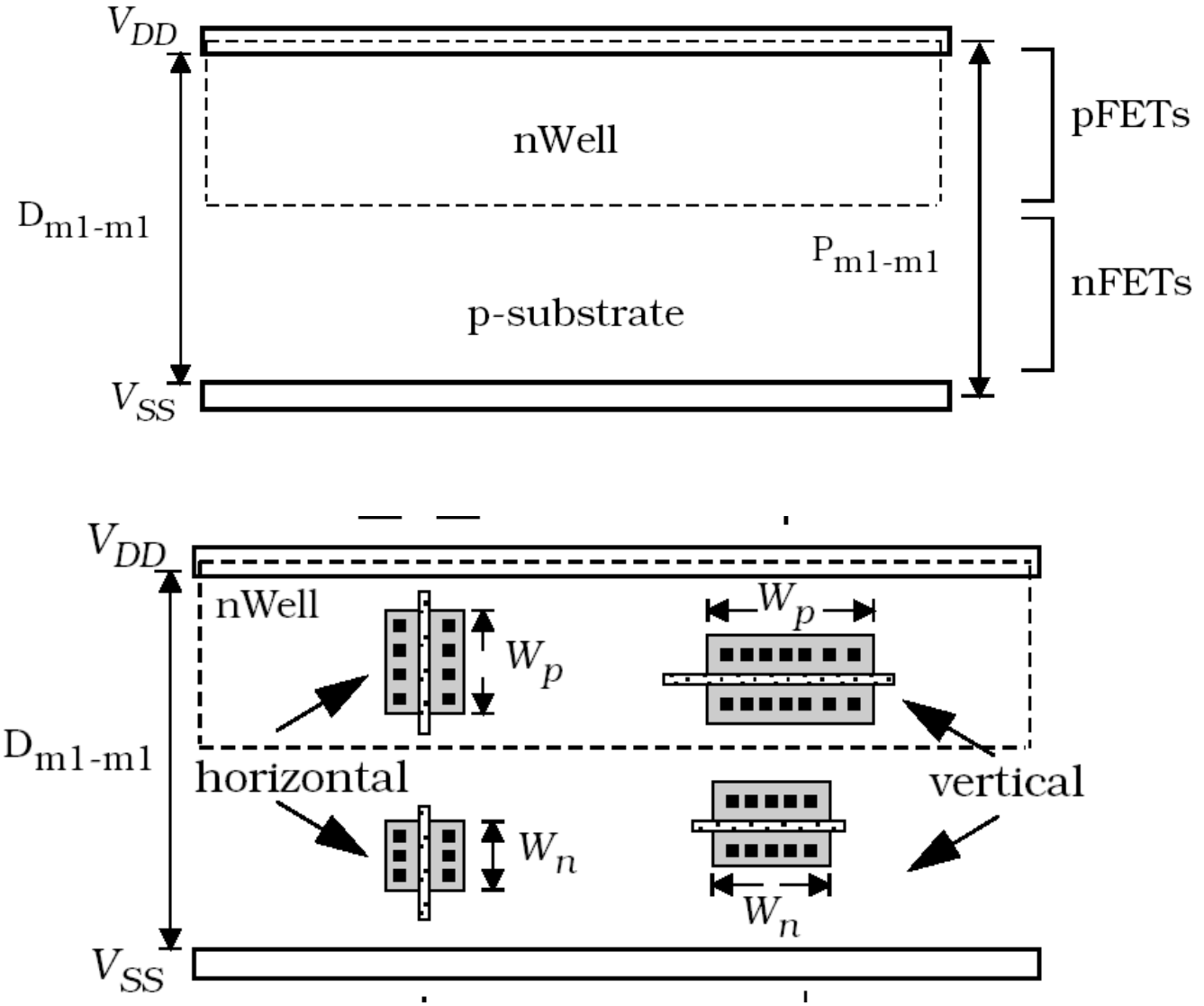
- Circuit extraction is used for LVS, and for spice simulation of layouts

Verification

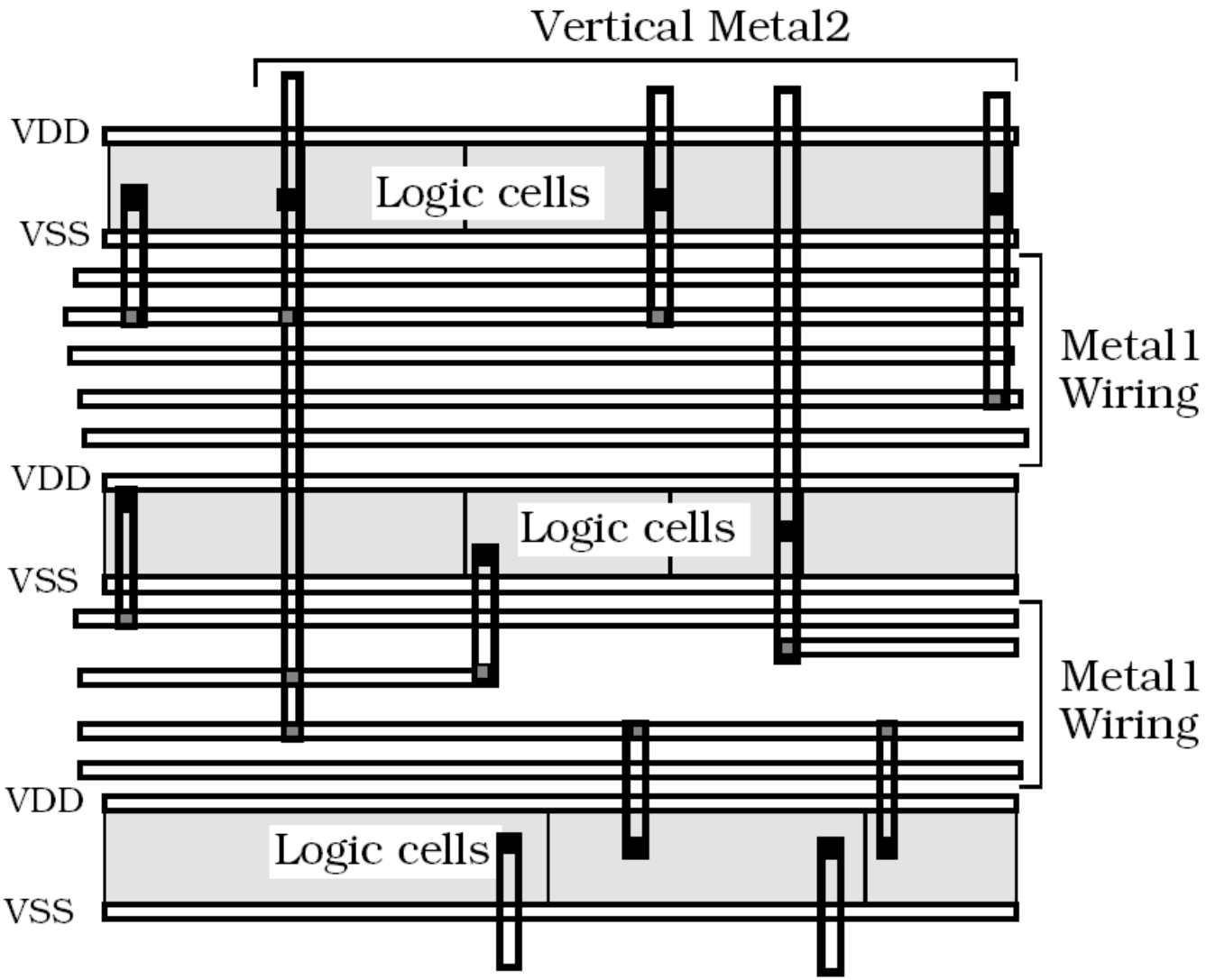
- Schematic simulation
  - Ensures functionality and provides an approximate estimate of timing
- Simulation of extracted layout
  - Ensures timing in the presence of parasitic capacitances/resistances (wires, junctions stc.)
  - Provides ‘more accurate’ estimation of timing
- Formal verification
  - Mathematically verify the functionality of the circuit from its logic level description
  - Very important for large circuits where circuit simulation will take long time

Physical Design: Logic Cells to Small Systems

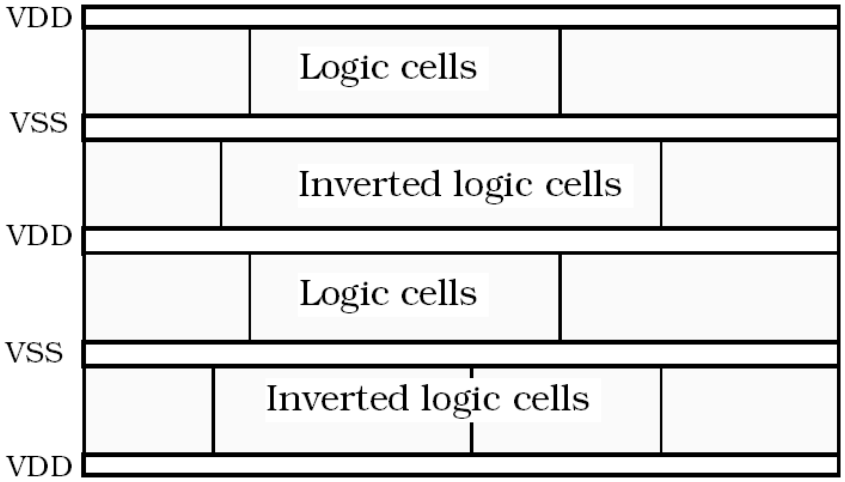
Physical Design for Large Number of Cells



Wiring channels.

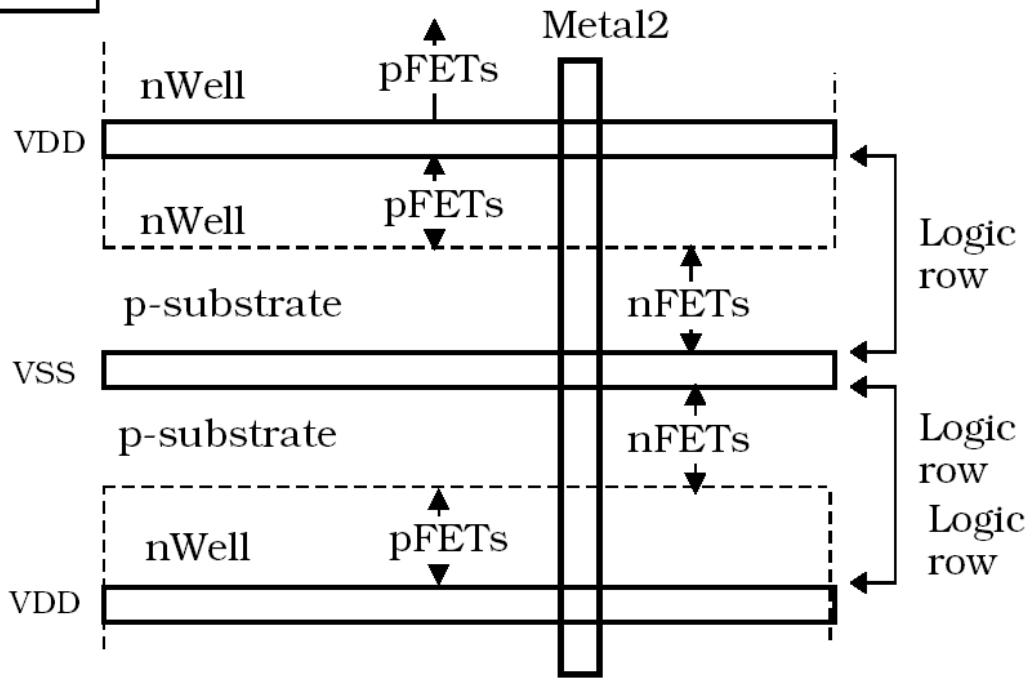


Weinberger image array.

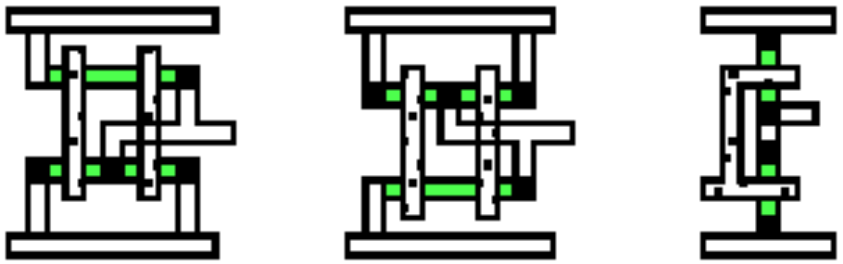


Cell placements

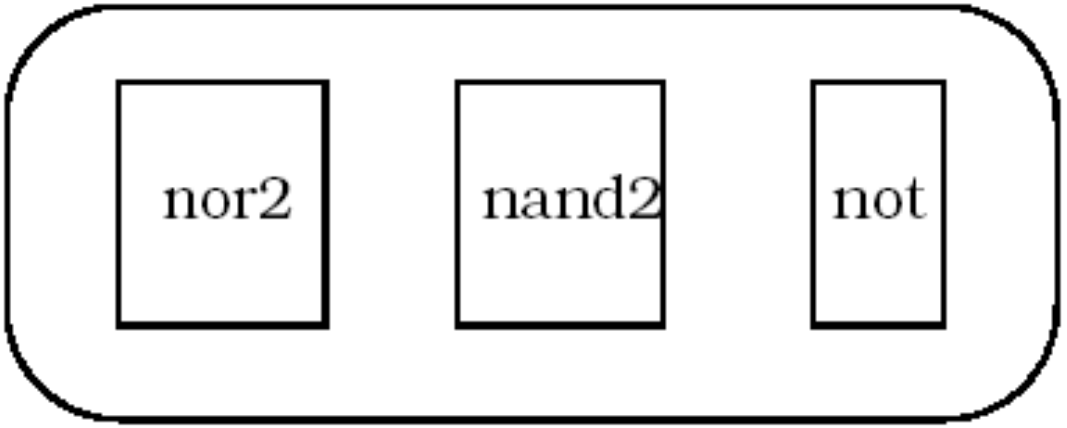
FETs



Primitive polygon-level library entries.

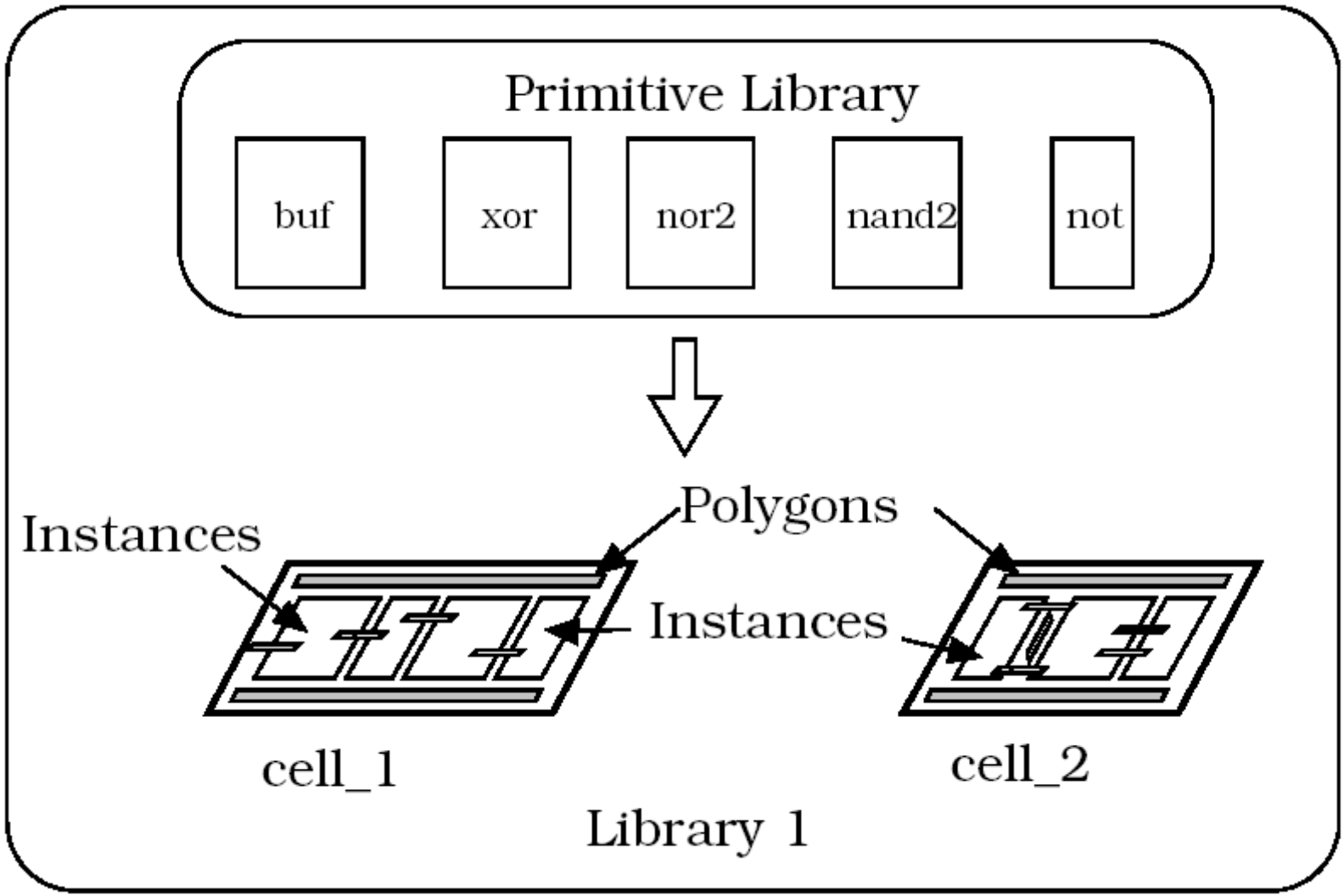


Polygon level

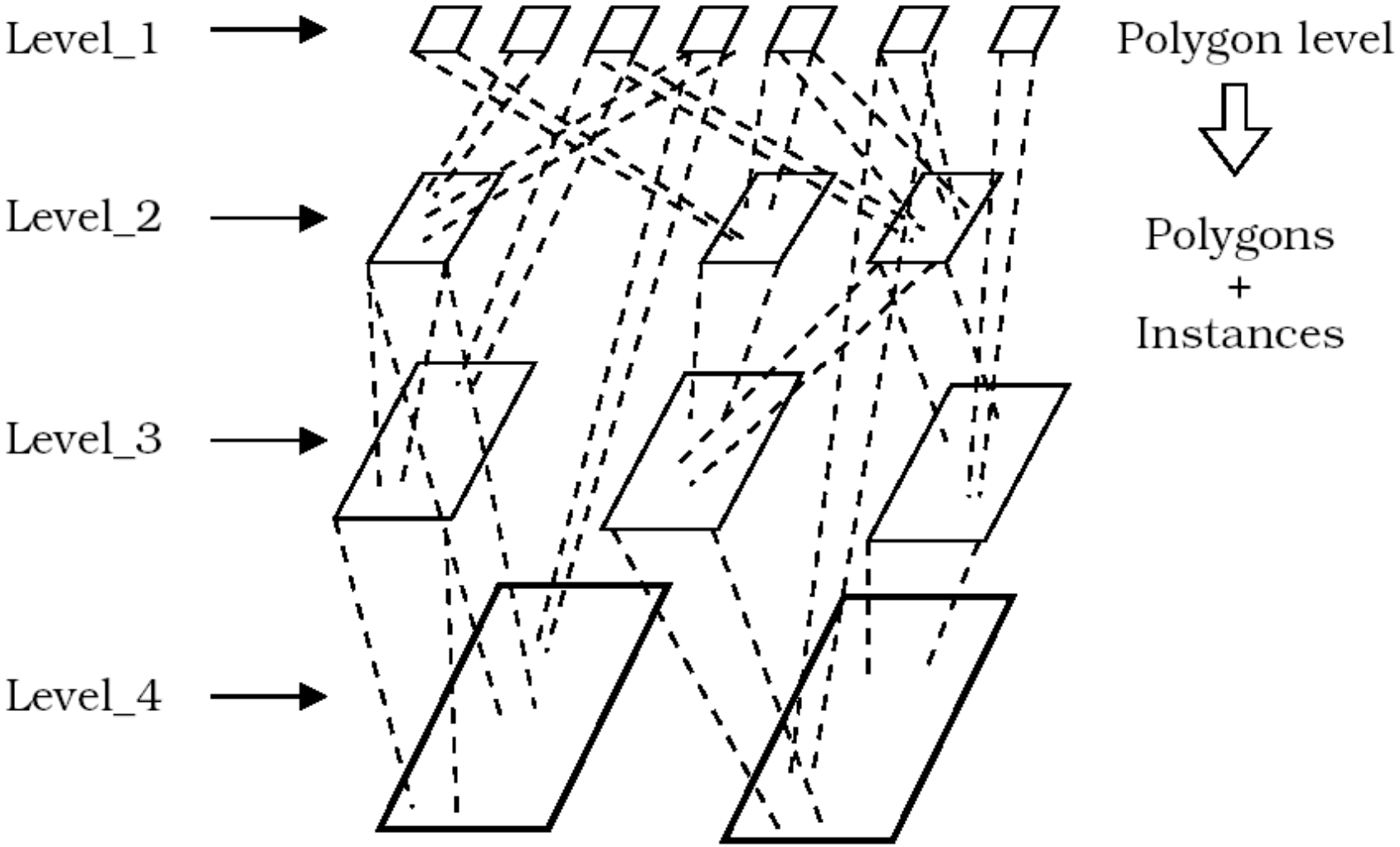


Cells in the library

Expanding the library with more complex cells.



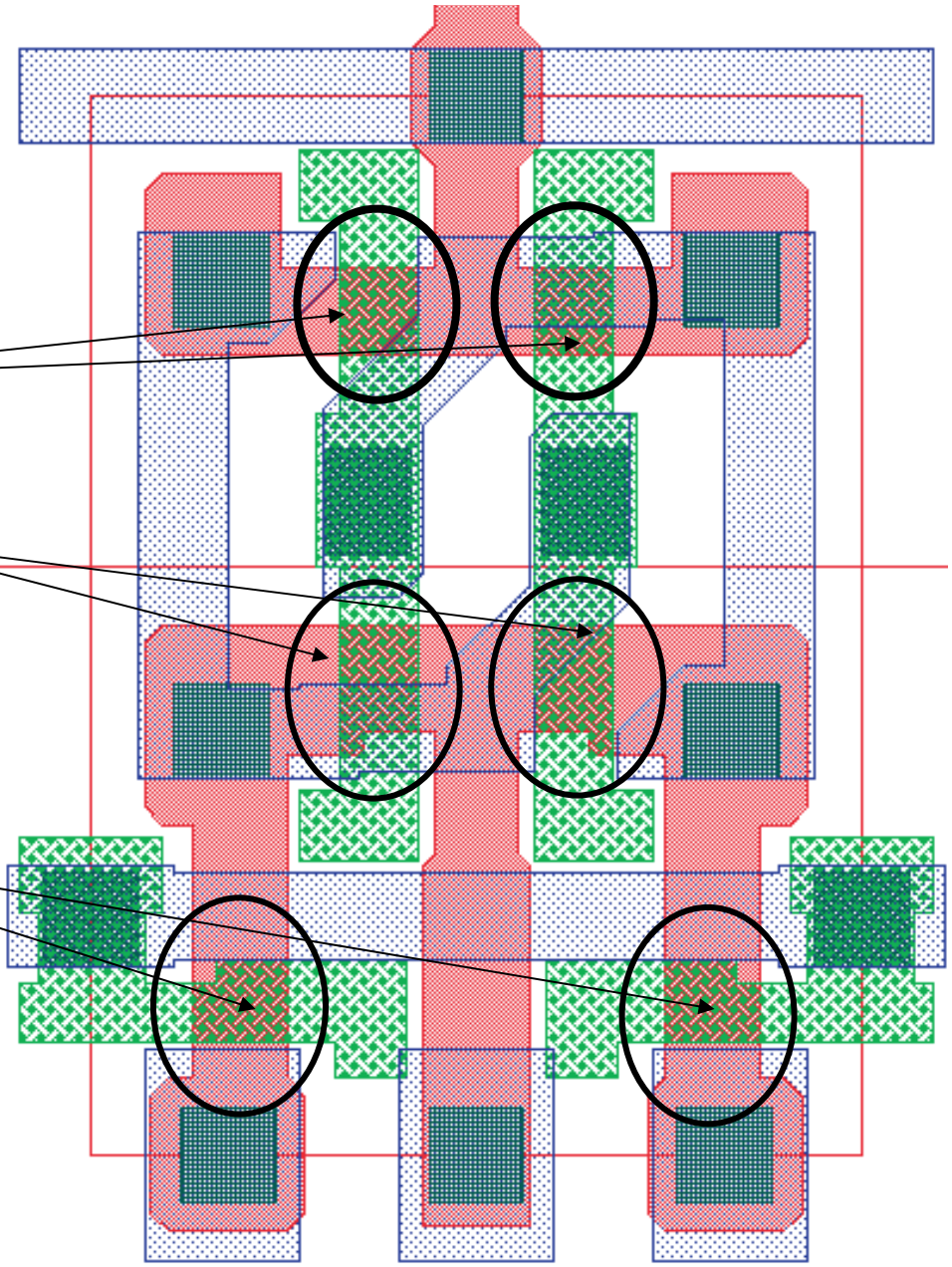
Cell hierarchy



Large Design Layout: Example: SRAM Important for Project

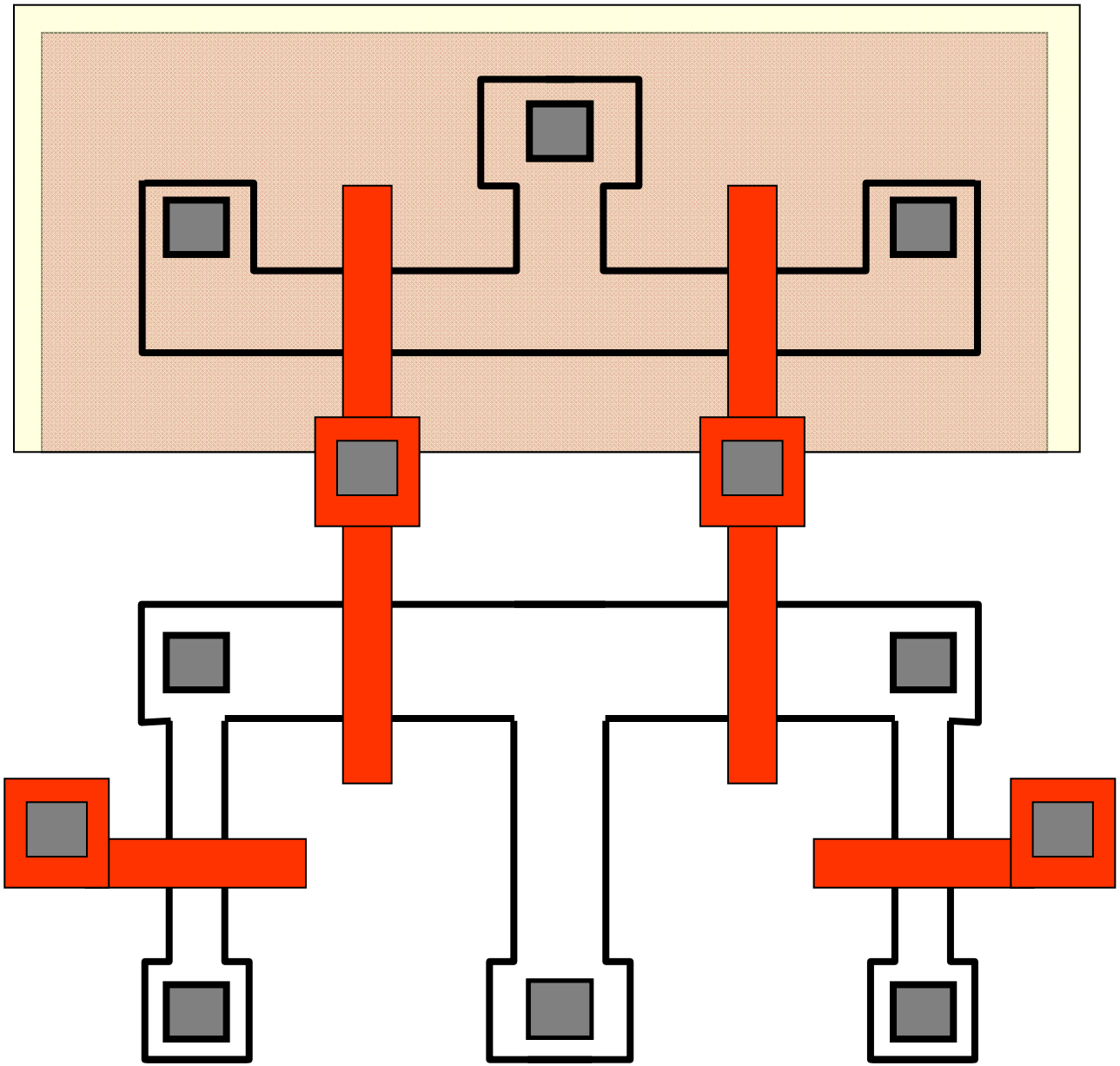
Layout of SRAM Cell

Green – PC
Red - RX

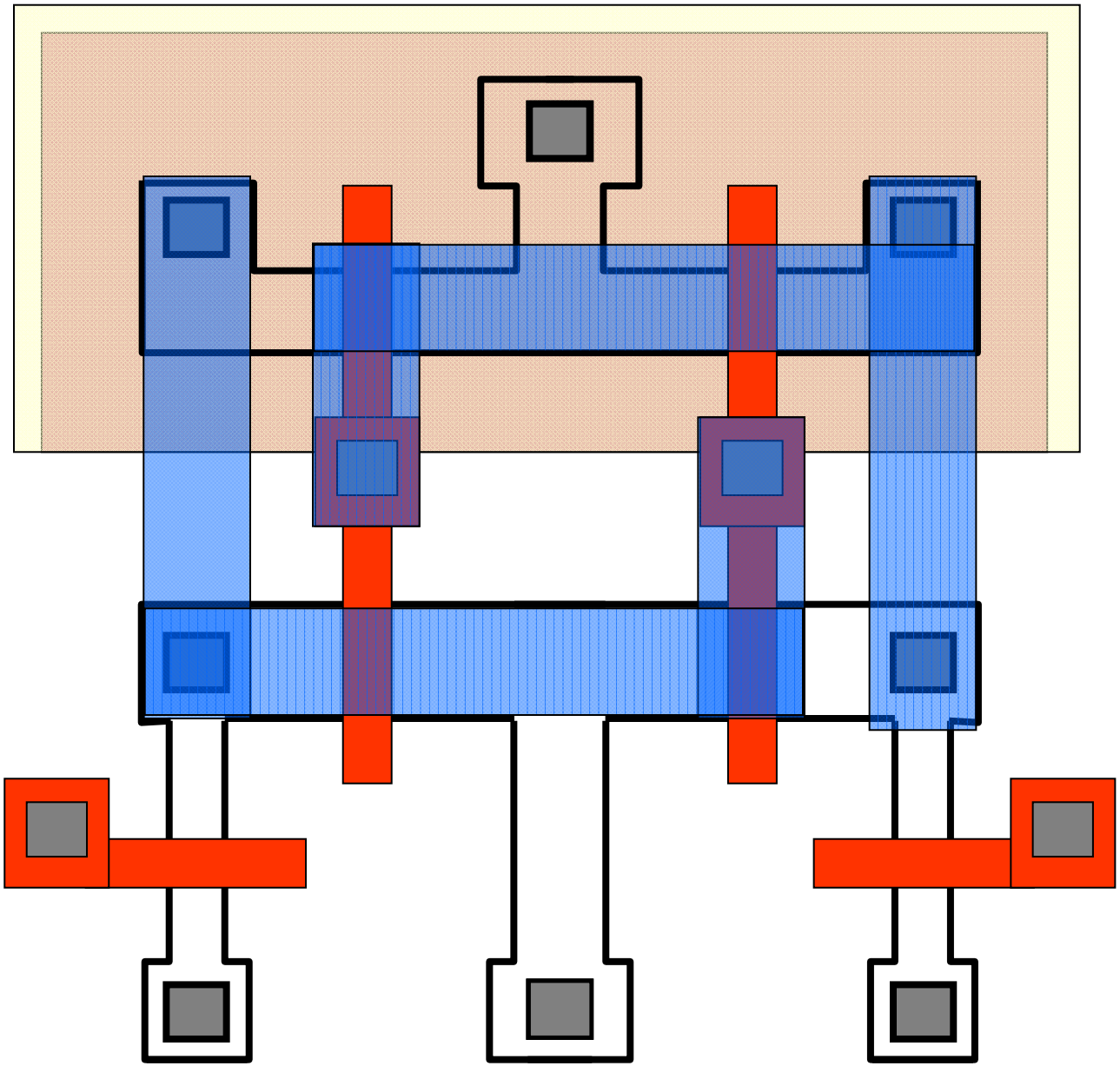


Ref.
R.W. Mann, et. al.
IBM J. R&D

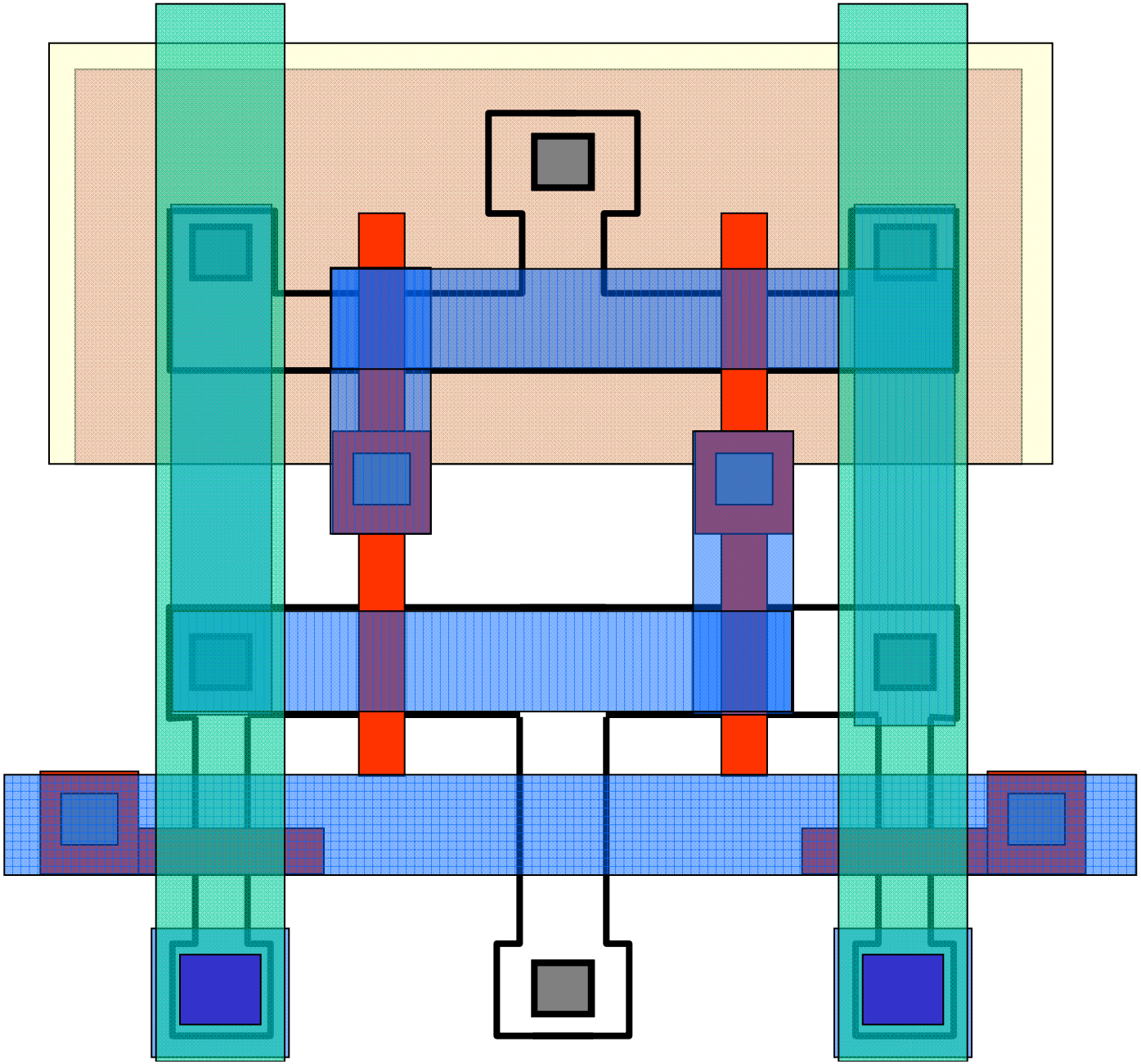
Layout of SRAM Cell



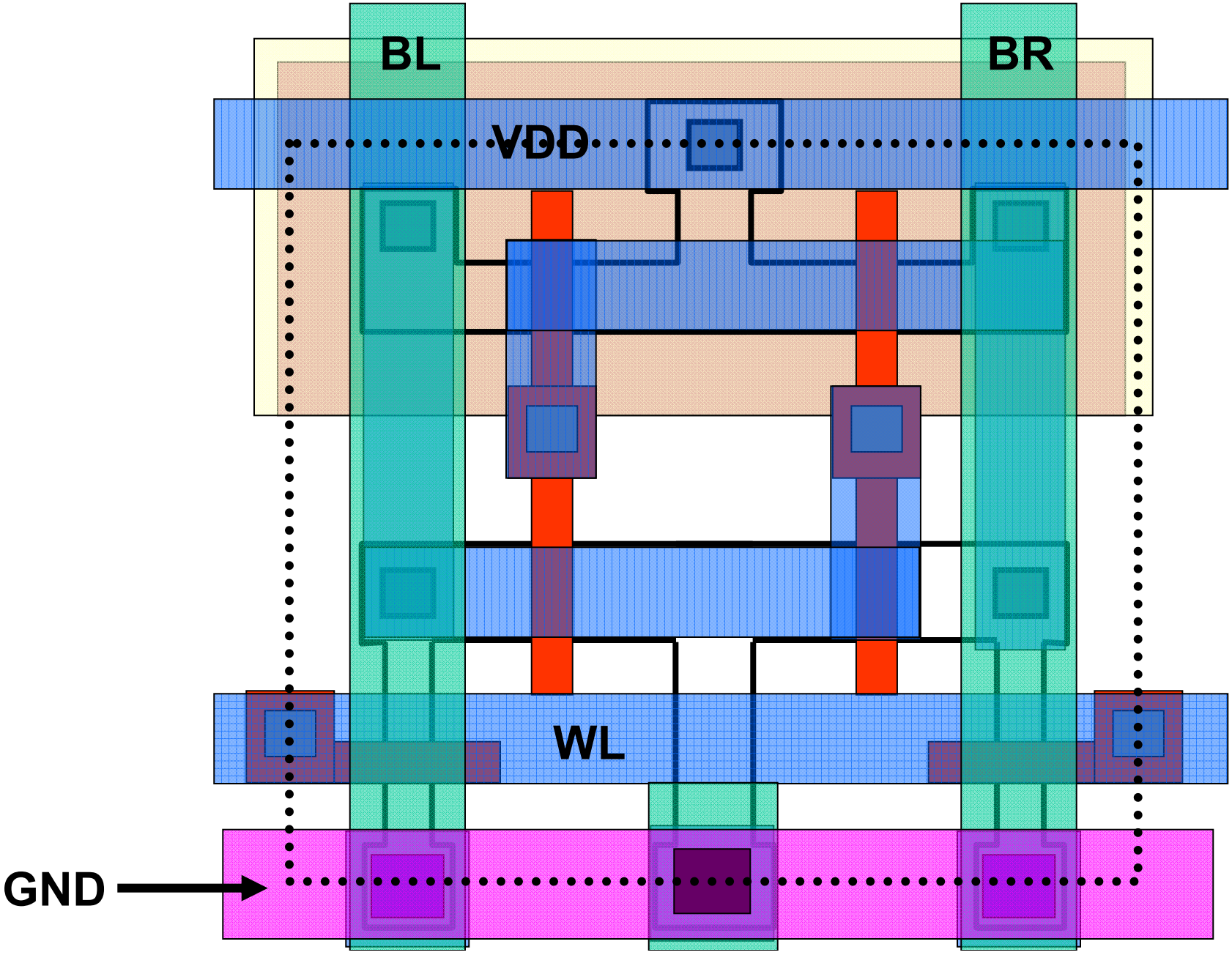
Layout of SRAM Cell



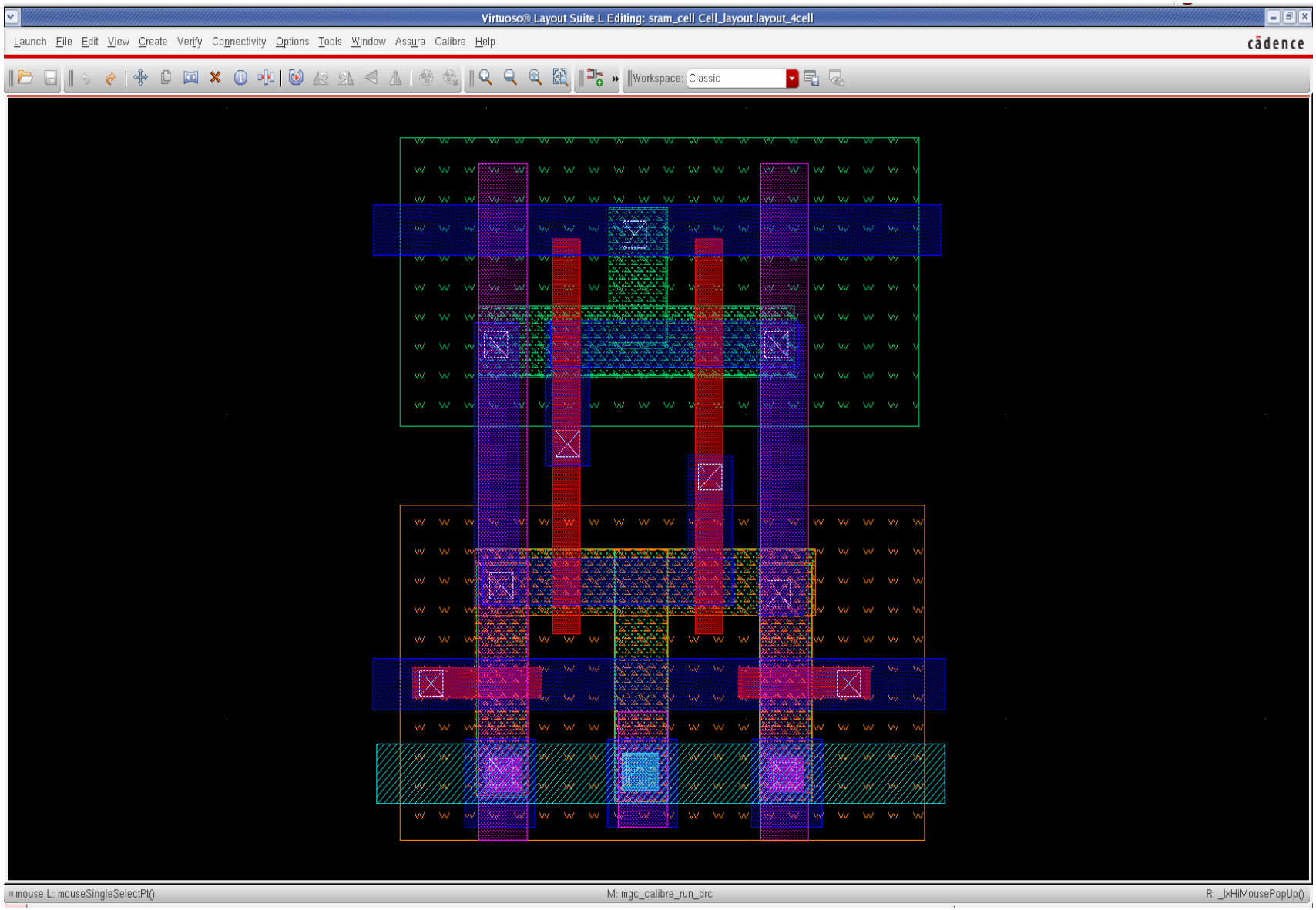
Layout of SRAM Cell

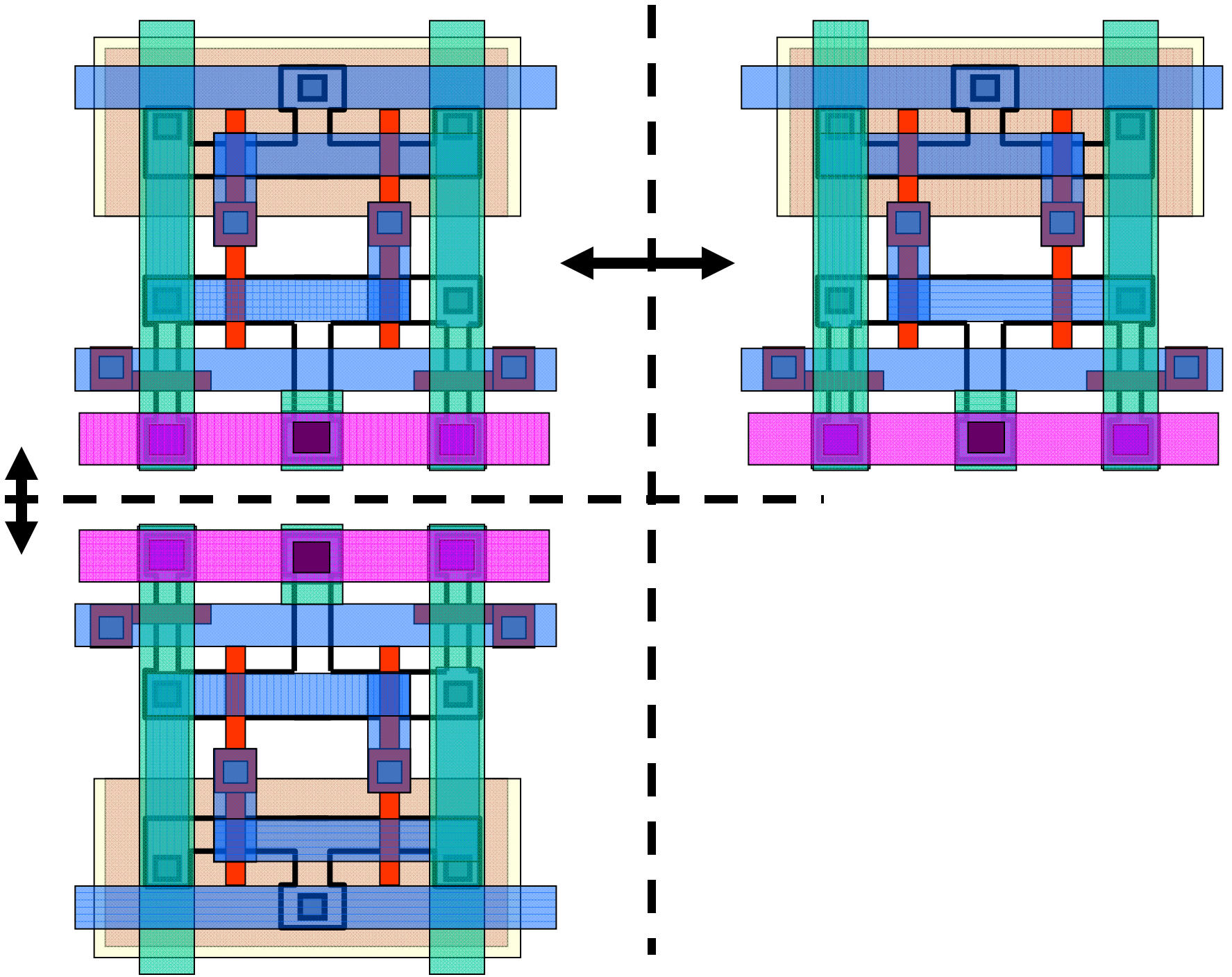


Layout of SRAM Cell

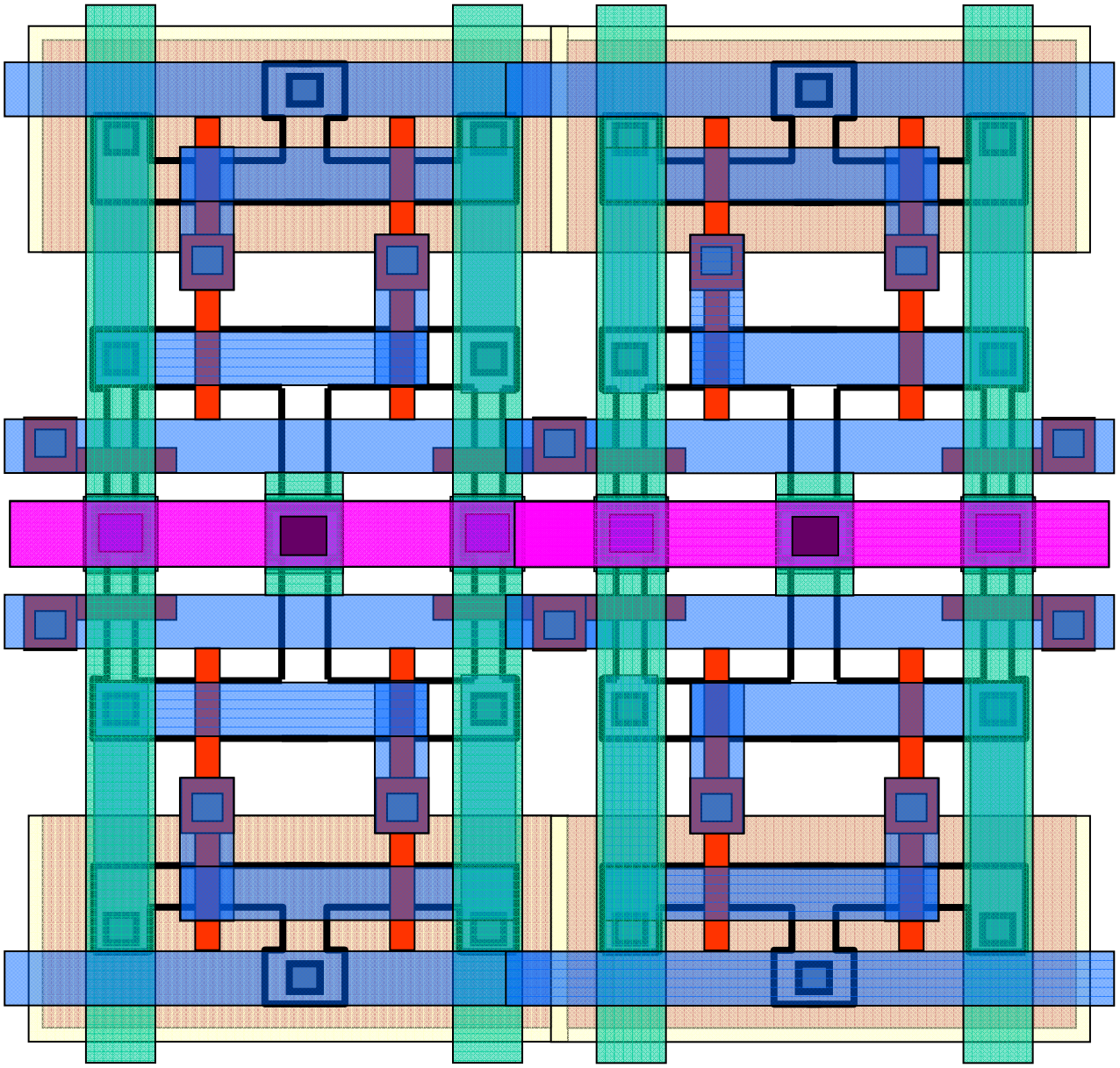


Layout of SRAM Cell

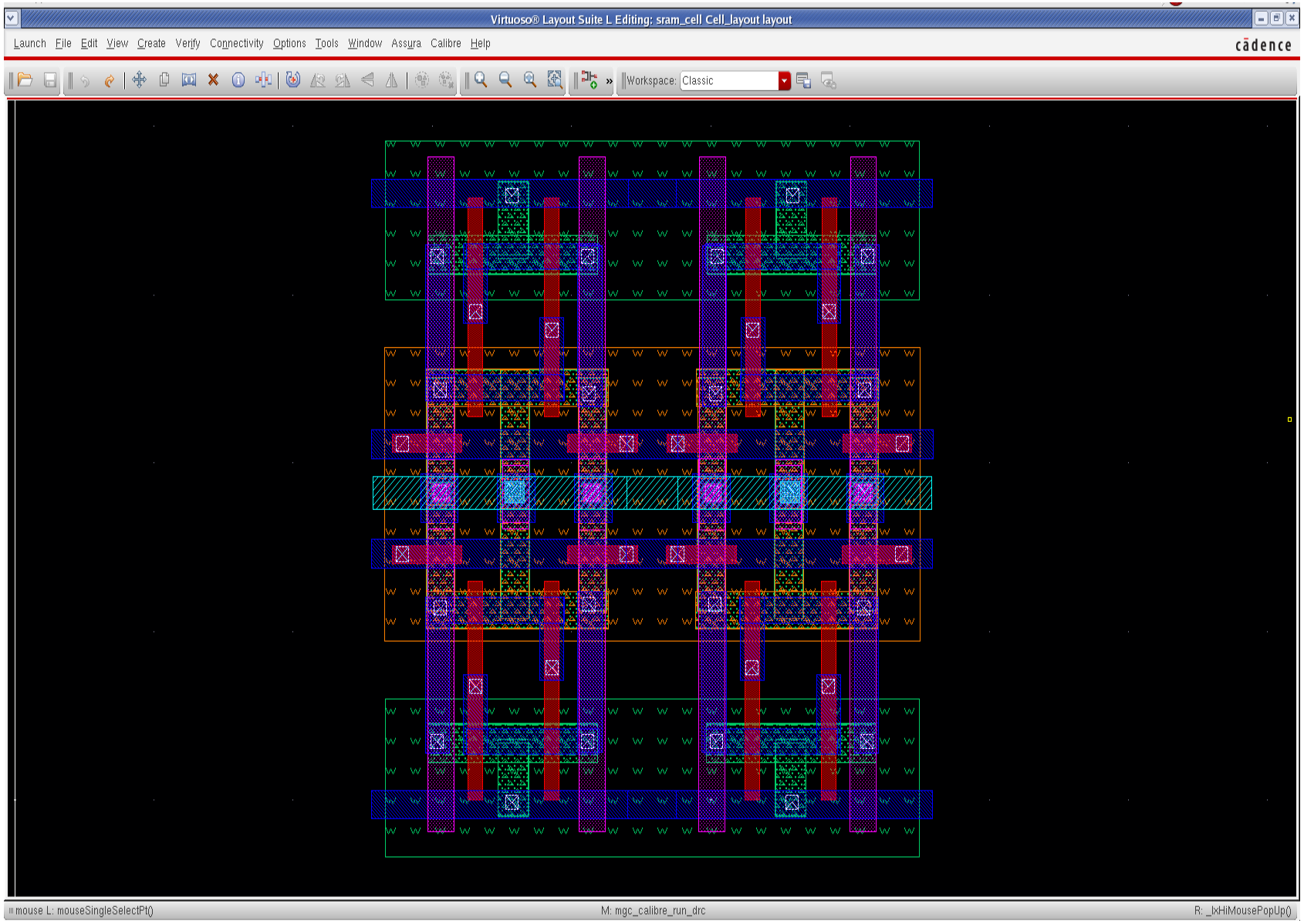




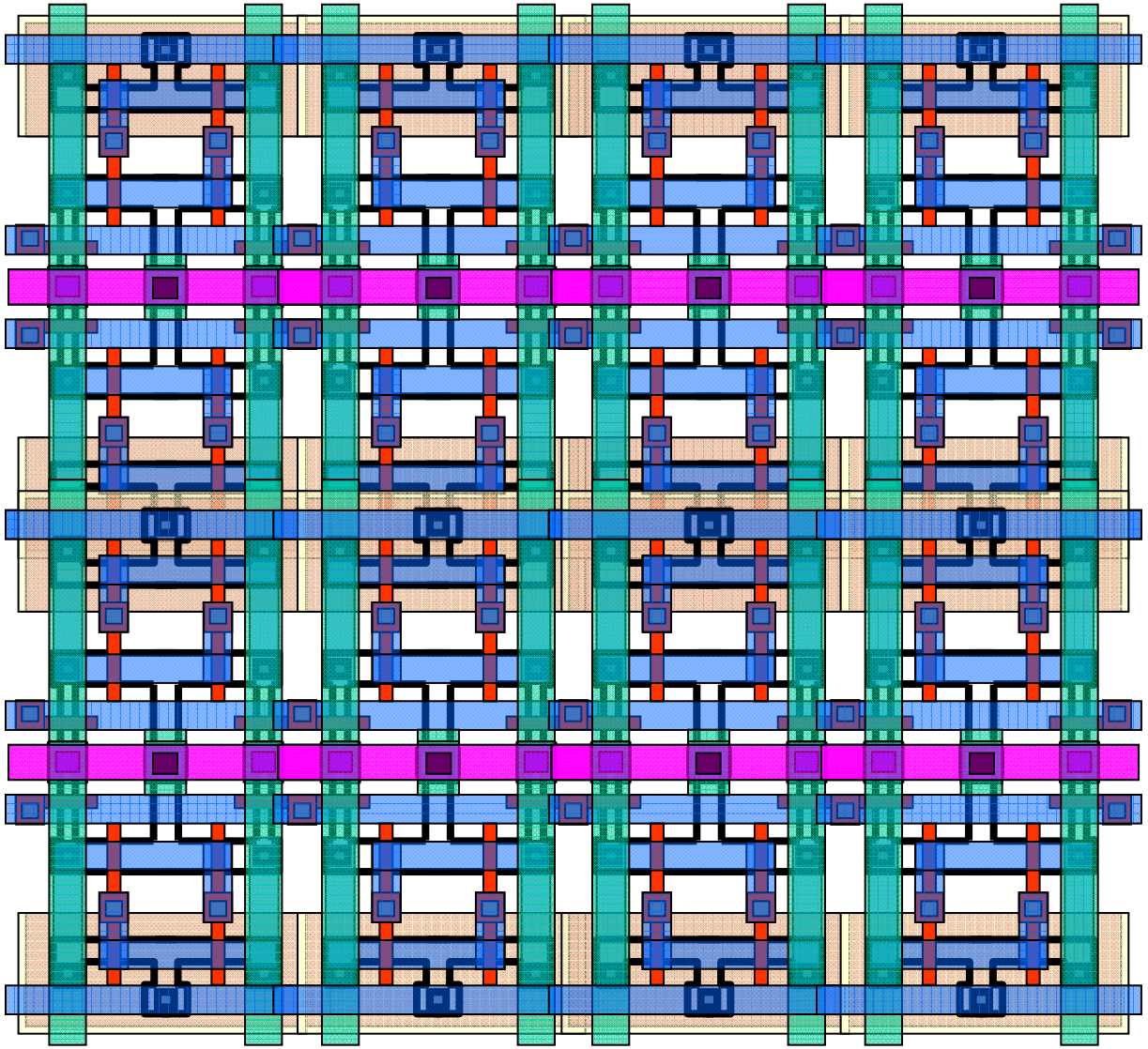
Basic ‘Standard Cell’ for Array – 4 Cells



Basic ‘Standard Cell’ for Array – 4 Cells

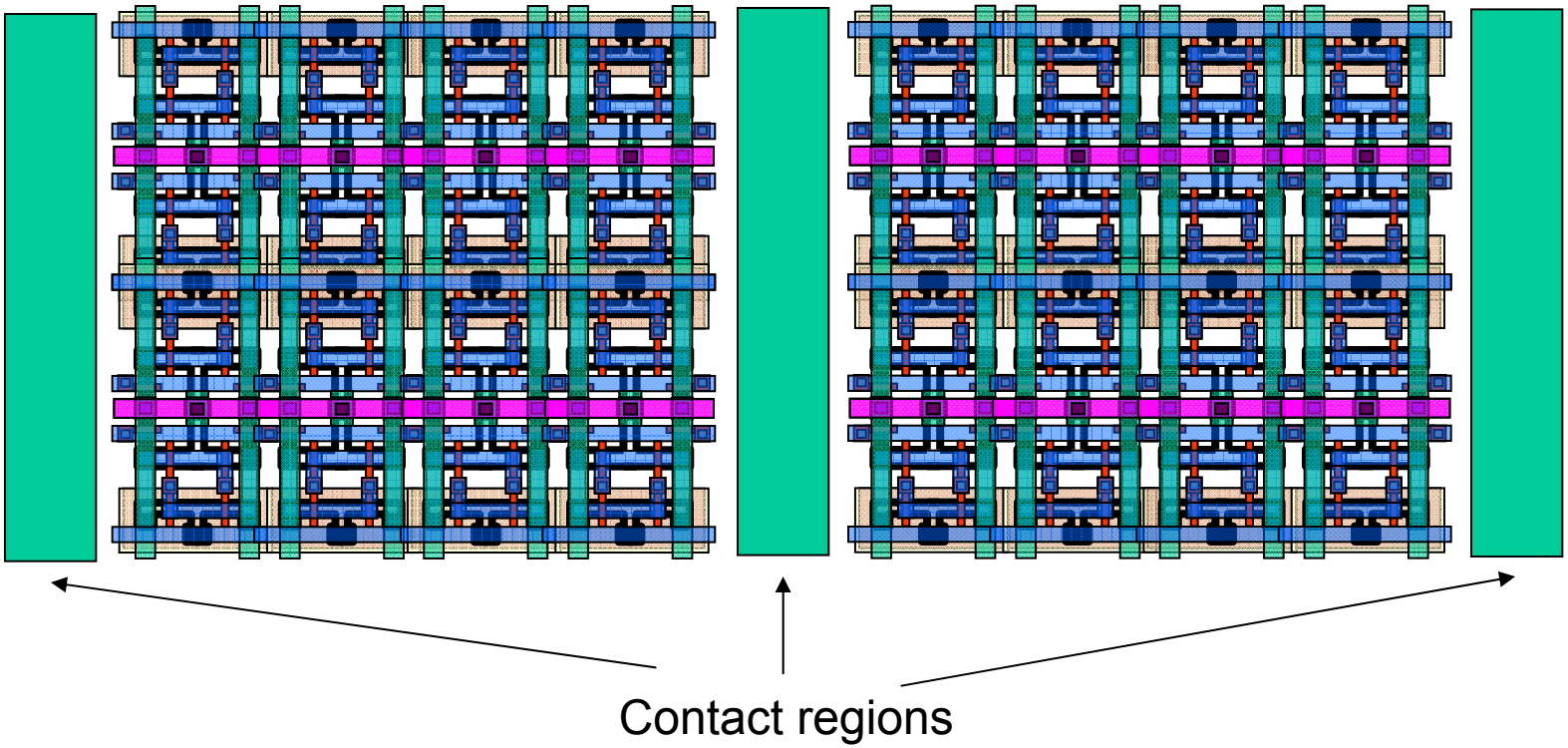


Array Construction – 4 x 4 = 16 Cells



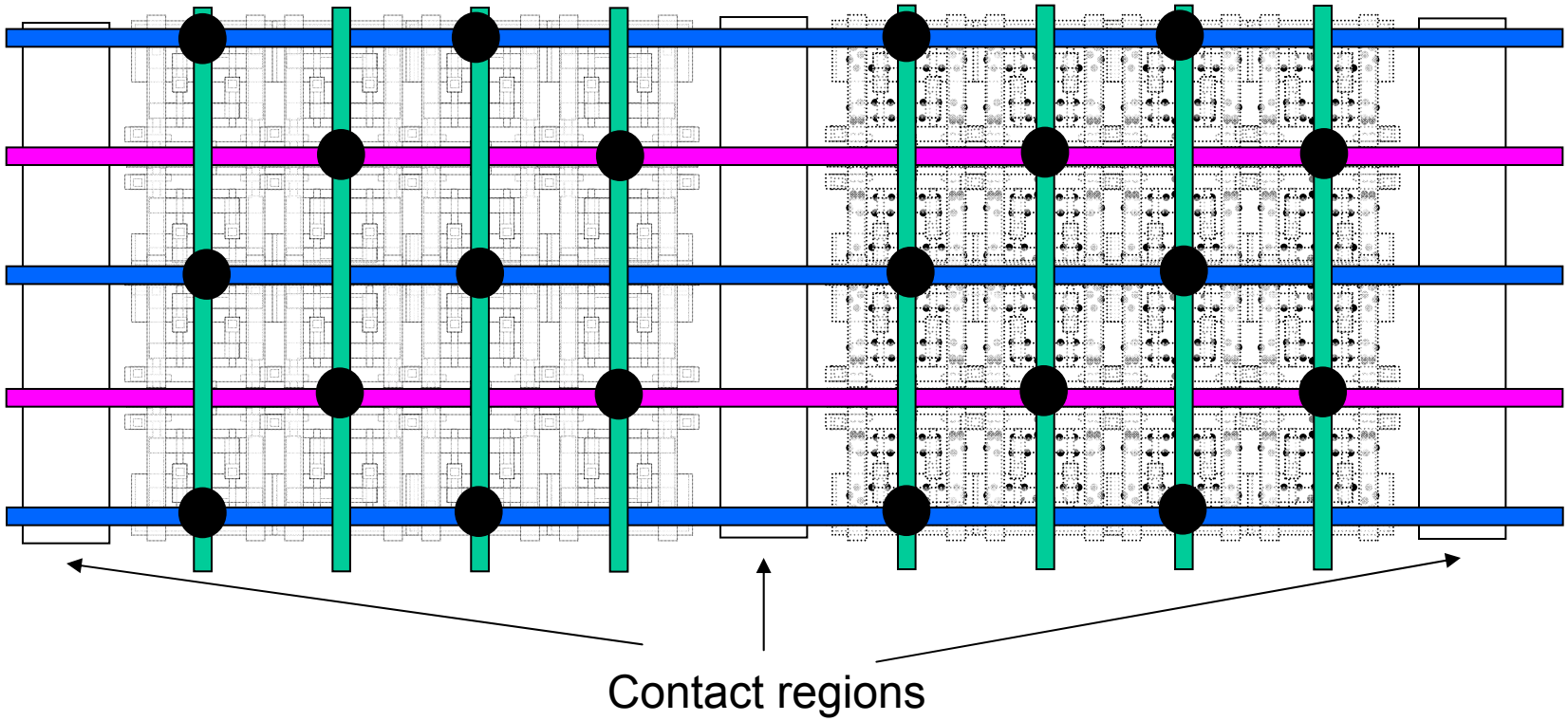
Next repeat this block for 8 x 8 array, and so on

Array Construction – Substrate/N-well contacts



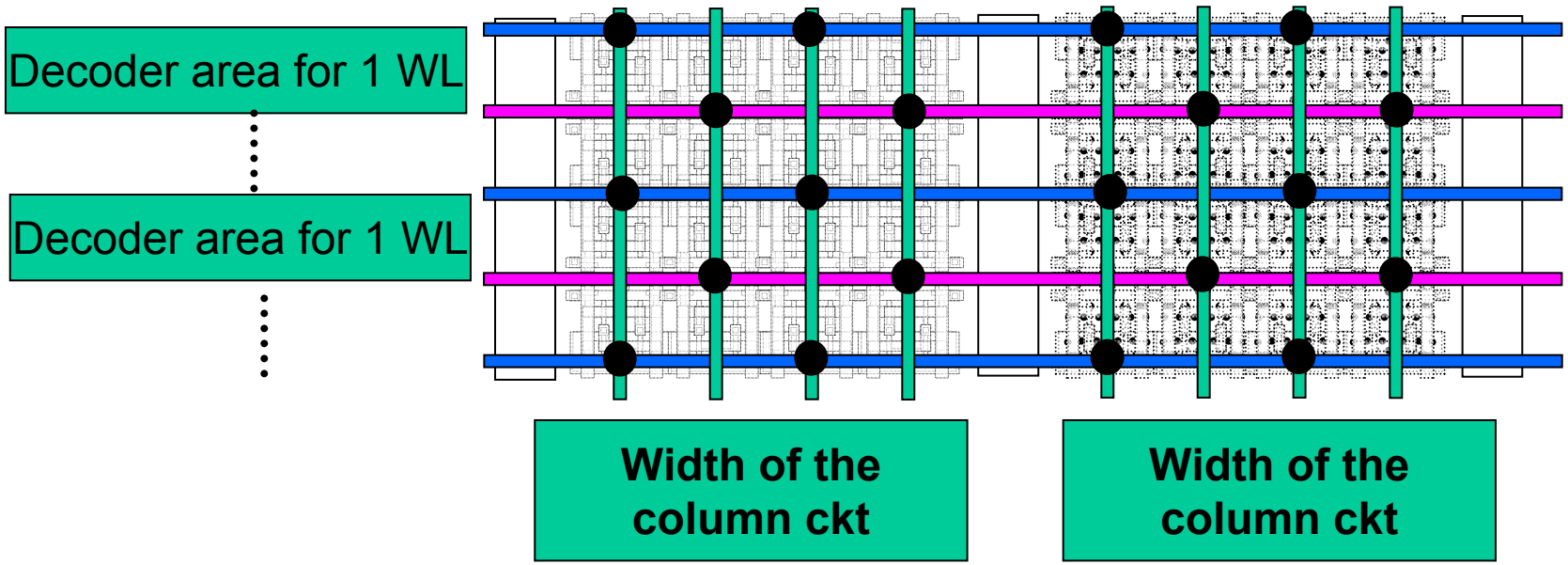
- **Normally, to save area n-well and substrate contacts are not present in every SRAM cell.**
- **The DRC rules specifies the maximum allowable distance between a NMOS (or PMOS) device and substrate (or n-well) contact.**
- **In array design, normally contacts are placed only to satisfy the constraints so that area can be lower.**

Array Construction – Supply Network



- **Only horizontal supply and ground lines are not enough as these lines are not connected to each other**
  - **Lower stability and higher variability in supply network**
- **A network is supply is normally used with vertical lines connecting the horizantal lines**

System Level Physical Design of the Array



- **Each decoded bit the row decoder needs to fit within the height of the memory cell.**
- **Width of the column circuit need to fit the pitch of 4 columns (if using a 4 x 1 column multiplexer)**