**CDA3101 Test 3 Review Problem Set**

1. How many total bits are required for a four-way set associative cache with 32 KB of data and 2-word blocks, assuming a 32-bit address?

2. Consider a direct-mapped cache with 256 blocks and a block size of 4 words. To what block number does byte address 1208 map?

3. Consider a processor with a single data cache. What is the average memory access time for the processor with a clock period of 1ns, a miss penalty of 25 clock cycles, a miss rate of .05, and a cache access time (or hit time) of 1 clock cycle? Assume read and write miss penalties are the same and ignore other write stalls.

4. Assume a cache with 8K blocks, a 4-word block size, and a 32-bit address. Find the total number of sets and the total number of tag bits for:

a. Direct-mapped
b. Two-way set associative
c. Four-way set associative
d. Fully-associative

5. For a direct-mapped cache design with 32-bit addresses, the following bits of the address are used to access the cache.

a. Tag: 31-10 Index: 9-4 Offset: 3-0
b. Tag: 31-12 Index: 11-5 Offset: 4-0

For each configuration above, answer the following questions:
- What is the cache size in words? Bytes?
- How many entries are there in the cache?

Now assume the following references are made from power-on: 0, 4, 16, 132, 232, 160, 1024, 30, 140, 3100, 180, 2180. For each configuration:
- How many blocks are replaced?
- What is the hit ratio?
- What does the final state of the cache look like? Express valid entries in the form <index, tag, data>.

6. Assume a 2-way set-associative cache with 32 cache sets, 4 words per block, and an LRU replacement policy. For both a write-through, no write-allocate and a write-back, write-allocate cache, fill in the appropriate information for the following memory references (see slide 65 of Lecture 11).

| | |
|---|---|
| W | 1840 |
| R | 1844 |
| R | 304 |
| W | 308 |
| R | 820 |
| R | 824 |

7. The following table is a stream of virtual addresses as seen on a system. Assume 4KB pages, a four-entry full associative TLB and true LRU replacement. If pages must be brought in from disk, assign the next largest physical page number.

| | |
|---|---|
| a. | 4095, 31272, 15789, 7193, 4096, 8912 |
| b. | 9452, 30964, 19136, 46502, 38110, 16653, 48480 |

TLB

| Valid | Tag | Physical Page Number |
|---|---|---|
| 1 | 11 | 12 |
| 1 | 7 | 4 |
| 1 | 3 | 6 |
| 0 | 4 | 9 |

Page Table

| Valid | Physical Page Number or Disk |
|---|---|
| 1 | 5 |
| 0 | Disk |
| 0 | Disk |
| 1 | 6 |
| 1 | 9 |
| 1 | 11 |
| 0 | Disk |
| 1 | 4 |
| 0 | Disk |
| 0 | Disk |
| 1 | 3 |
| 1 | 12 |

Given the two address streams in the table above, for each stream show the final state of the system given the initial state of the TLB and Page Table. Also, for each reference, indicate whether it was a hit in the TLB, a hit in the page table, or a page fault. What is the physical address that corresponds to every virtual address?