

SOURASISH MITRA

B. Tech | Kolkata, IN | [smitra0916.github.com](#)

+91 8013445866 | mitrasourasish@gmail.com | [sourasishmitra](#) | [smitra0916](#)

EDUCATION

- Jalpaiguri Government Engineering College, West Bengal, IN** Expected 2025
BACHELOR OF TECHNOLOGY IN ELECTRONICS & COMMUNICATION ENGINEERING CGPA: 8.98
- APC Ray Polytechnic Jadavpur, Kolkata, IN** 2022
DIPLOMA IN ELECTRICAL ENGINEERING CGPA: 8.9

TECHNICAL SKILLS

Programming Languages:	C, C++, Python
Electronics Design & Prototyping:	Cadence Virtuoso, Xilinx Vivado, KiCad, Arduino IDE
Tools & Platforms:	Git/GitHub, MATLAB, MS Office, Linux, Windows
Soft Skills:	Problem Solving, Self-learning, Presentation, Adaptability
Areas of Interest:	Electronics & Automation, VLSI Design, IoT, Embedded System
Relevant Subjects:	Analog & Digital Electronics, Digital Circuits, DSP

EXPERIENCE

- Celebal Technologies** June 2024 - August 2024
Summer Intern Remote
 - Implemented and deployed a **Python-based anomaly detection system** utilizing unsupervised learning techniques to analyze network traffic data for identification of unusual patterns and anomalies indicative of potential security breaches or system malfunctions.
 - Optimized the performance by tuning the latent dimension in auto encoder. Achieved maximum accuracy while **minimizing false positives**.
- University of Calcutta** May 2024 - July 2024
Research Intern Kolkata, India
 - Designed and implemented **PWM control system** using Verilog on Xilinx FPGA to regulate MOSFETs driving a pump for a cold collision experiment at the Chemistry Lab.
 - Ensured **efficient signal transmission** through **impedance matching** and verified functionality using an **Oscilloscope**.

PERSONAL PROJECTS

- 32-bit pipelined MIPS processor in Verilog** [LINK](#) [↗](#) Ongoing
Technology Used: Verilog, Xilinx Vivado, Xilinx FPGA
 - Designed and implemented a 32-bit MIPS microprocessor with a **5-stage pipeline architecture** using Verilog, achieving efficient RISC instruction set execution.
 - Successfully implemented it on a Xilinx FPGA board, demonstrating **high-performance operation and reliability**.
- Real-Time Health Monitoring with Scalable Data Management** [LINK](#) [↗](#) May 2024
Technology Used: Firebase, ESP8266(NodeMCU), MX30100 sensor.

Presented and Published at **32nd West Bengal State Science & Technology Congress**
Department of Science & Technology and Biotechnology, Govt of WB

 - Implemented sophisticated system that will remotely monitor a patient and warn doctor/hospital in necessary condition for simplified **detection of cardiovascular diseases, Easier Hospital Ward management. Elderly Home care.**
 - Used Firebase Authentication(SDK) to facilitate authentication & Cloud Firestore to store data.

PUBLICATIONS

- Development of a FPGA-Based Timing Sequence Generator with MOSFET-Driven Nanosecond Pulse Precision for Cold Collision Experiments** March 2025
National Conference on Recent Trends in Science and Technology 2025
- Real-Time Health Monitoring integrating Low-cost IoT with Bluetooth LE and Cloud through a Local Server** February 2025
32nd West Bengal State Science & Technology Congress, Dept of Science & Technology and Biotechnology, Govt of WB

POSITION OF RESPONSIBILITY

- Technical Member Core Team** CFI (Centre for Innovation), JGEC. Aug 2023 - Present
 - Mentored young team members, developed engaging workshops to ignite their passion for technology and problem-solving in the Electronics field.

CERTIFICATION

- VLSI SoC Design using Verilog HDL** MAVEN SILICON
- AUTOCAD TRAINING** L&T Construction, NIELIT Kolkata

ACHIEVEMENTS

- Outstanding Paper Presentation - 1st** at 7th Regional Science & Technology Congress 2025, Siliguri College
- Hackathon Round 2 Finalist** at Department of Health and Family Welfare, Govt. of WB, Hack-O-Med 2023.
- Achieved Highest SGPA 9.71** in 5th Semester of BTech.