SOURASISH MITRA

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EDUCATION

• **Jalpaiguri Government Engineering College, West Bengal** — Expected 2025
Bachelor of Technology in Electronics and Communication Engineering — CGPA: 8.87/10

• **APC Ray Polytechnic Jadavpur, Kolkata** — 2022
Diploma in Engineering — CGPA: 8.9/10

TECHNICAL SKILLS

Languages: C / C++, Python
HDL: Verilog, System Verilog
EDA Tools: Cadence Virtuoso, Xilinx Vivado, Xilinx ISE, KiCad, NgSpice, eSim
Libraries: TensorFlow, NumPy, Pandas, Scikit-learn

EXPERIENCE

• **Celebal Technologies** — June - July 2024
Summer Intern — Remote

– Deployed a Python-based anomaly detection system, leveraging **unsupervised learning techniques** to analyse network traffic data to identify unusual patterns and anomalies, which could signal potential security breaches or system malfunctions
– Optimized the performance by **tuning the latent dimension in auto encoder**. Achieved maximum accuracy while minimizing false positives.

• **University of Calcutta** — May- June 2024
Research Intern — Kolkata, India

– Designed and implemented **PWM control** system using Verilog on Xilinx FPGA to regulate MOSFETs driving a pump for a cold collision experiment at the Chemistry Lab.
– Ensured efficient signal transmission through **impedance matching** and verified PWM functionality using an **Oscilloscope**.
– **Achieved precise control** of the pump's operation within the experiment's critical temperature requirements, ensuring optimal cold collision environment

PERSONAL PROJECTS

• **32-bit pipelined MIPS processor in Verilog** — Ongoing
Technology Used: Verilog, Xilinx Vivado, Xilinx FPGA

– Designed and implemented a 32-bit MIPS microprocessor with a **5-stage pipeline architecture** using Verilog, achieving efficient **RISC** instruction set execution.
– Simulated and **verified the processor functionality** in Xilinx Vivado and successfully implemented it on a Xilinx FPGA board, demonstrating high-performance operation and reliability.

• **SR Flip Flop to JK Flip Flop using Mixed Signal Design** — May 2024
Technology Used: Kicad, NgSpice, eSim, SKY 130 PDK, Verilog

– Conversion of F/F was implemented using SKY 130. The SR Flip Flop was made of **analog block using Kicad and Ngspice** and the gates which provide input to the SR Flip Flop is made of digital block using Verilog.
– Simulated the **whole design was using open-source software** eSim and SKY 130

• **Communication Protocols in Verilog** — April, 2024
Technology Used: Verilog/System Verilog, Xilinx ISE, Spartan 3E FPGA

– Designed the transmitter and receiver units of inter-system communication protocols like **UART**, and designed the interface of **I2C** communication protocol for EEPROM in Verilog.
– Simulated and **tested** the performance of the design in **Xilinx ISE**.

POSITION OF RESPONSIBILITY

• **Technical Member Core Team CFI (Centre for Innovation), JGEC.** — Aug 2023- Present

– **Led and mentored** young team members, developing engaging workshops to ignite their passion for technology and problem-solving in the IoT field.

ACHIEVEMENTS

• Hackathon Round 2 **Finalist** at Department of Health and Family Welfare, Govt. of WB, Hack-O-Med 2023.
• **Collaborated** in Open-Source Event JGEC Winter of Code- 2023.
• Achieved Highest SGPA **9.71** in 5th Semester of BTech.