SOURASISH MITRA

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EDUCATION

- **Jalpaiguri Government Engineering College, West Bengal, IN** *Expected 2025*
  BACHELOR OF TECHNOLOGY IN ELECTRONICS & COMMUNICATION ENGINEERING CGPA: 8.89
- **APC Ray Polytechnic Jadavpur, Kolkata, IN** *2022*
  DIPLOMA IN ENGINEERING CGPA: 8.9

TECHNICAL SKILLS

Languages:	C / C++, Python
HDL:	Verilog, System Verilog
EDA Tools:	Cadence Virtuoso, Xylinx Vivado, Xylinx ISE, KiCad, NgSpice, eSim
Libraries:	Numpy, Pandas, Scikit-learn, TensorFlow
Tools & Platforms:	UVM, Shell-scripting, Arduino, MATLAB, Git/GitHub, MS Office. Linux, Windows
Relevent Coursework:	Analog & Digital Electronics, Semiconductor Physics, Maths, DSP, VLSI

EXPERIENCE

- **Celebal Technologies** *June 2024 - August 2024*
  Summer Intern Remote
  - Implemented and deployed a ***Python-based anomaly detection system*** utilizing unsupervised learning techniques to analyze network traffic data for identification of unusual patterns and anomalies indicative of potential security breaches or system malfunctions.
  - Optimized the performance by tuning the latent dimension in auto encoder. Achieved maximum accuracy while ***minimizing false positives.***
- **University of Calcutta** *May 2024 - June 2024*
  Research Intern Kolkata, India
  - Designed and implemented ***PWM control system*** using Verilog on Xilinx FPGA to regulate MOSFETs driving a pump for a cold collision experiment at the Chemistry Lab.
  - Ensured ***efficient signal transmission*** through ***impedance matching*** and verified functionality using an ***Oscilloscope.***

PERSONAL PROJECTS

- **32-bit pipelined MIPS processor in Verilog** *Ongoing*
  Technology Used: Verilog, Xilinx Vivado, Xilinx FPGA
  - Designed and implemented a 32-bit MIPS microprocessor with a ***5-stage pipeline architecture*** using Verilog, achieving efficient RISC instruction set execution.
  - Simulated and verified the processor functionality in Xilinx Vivado and successfully implemented it on a Xilinx FPGA board, demonstrating ***high-performance operation and reliability.***
- **SR Flip Flop to JK Flip Flop using Mixed Signal Design** *May 2024*
  Technology Used: KiCad, NgSpice, eSim, SKY 130 PDK, Verilog
  - Conversion of F/F was implemented using SKY 130. The SR Flip Flop was made of ***analog block using Kicad and Ngspice*** and the gates which provide input to the SR Flip Flop is made of ***digital block using Verilog.***
  - Simulated the whole design was using open source software eSim and SKY 130
- **Communication Protocols in Verilog** *April 2024*
  Technology Used: Verilog/SystemVerilog, Xilinx ISE, Spartan 3E FPGA
  - Designed the transmitter and receiver units of inter-system communication protocols like UART, and designed the interface of 12C ***communication protocol for EEPROM in Verilog.***
  - Simulated and tested the performance of the design in Xilinx ISE.

POSITION OF RESPONSIBILITY

- **Technical Member Core Team** CFI (Centre for Innovation), JGEC. *Aug 2023 - Present*
  - Mentored young team members, developed engaging workshops to ignite their passion for technology and problem-solving in the IoT field.

ACHIEVEMENTS

- **Hackathon Round 2 Finalist** at Department of Health and Family Welfare, Govt. of WB, Hack-O-Med 2023.
- **Participated and Collaborated** in Open Source Event JGEC Winter of Code - 2023.
- **Achieved Highest** SGPA 9.71 in 5th Semester of BTech.