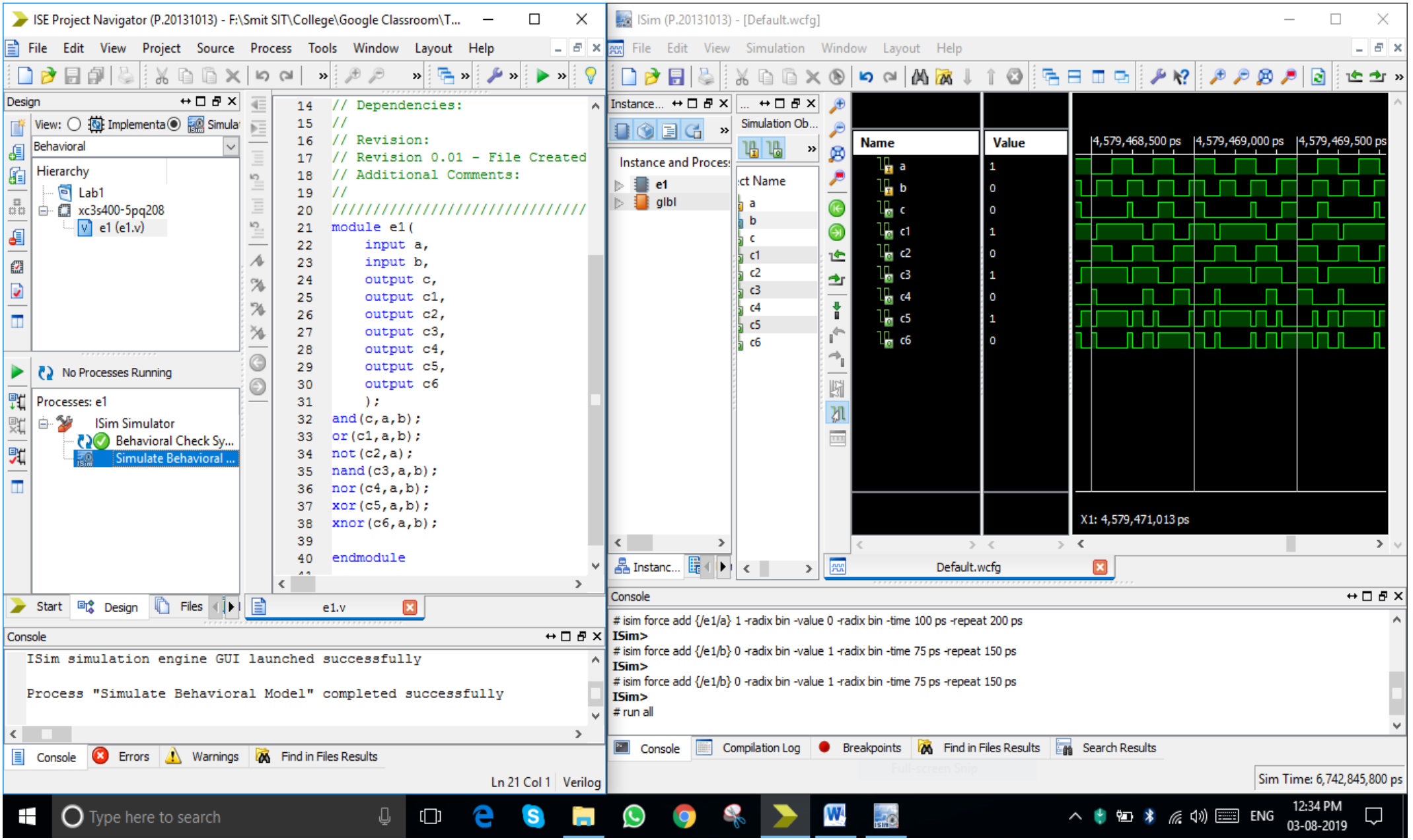
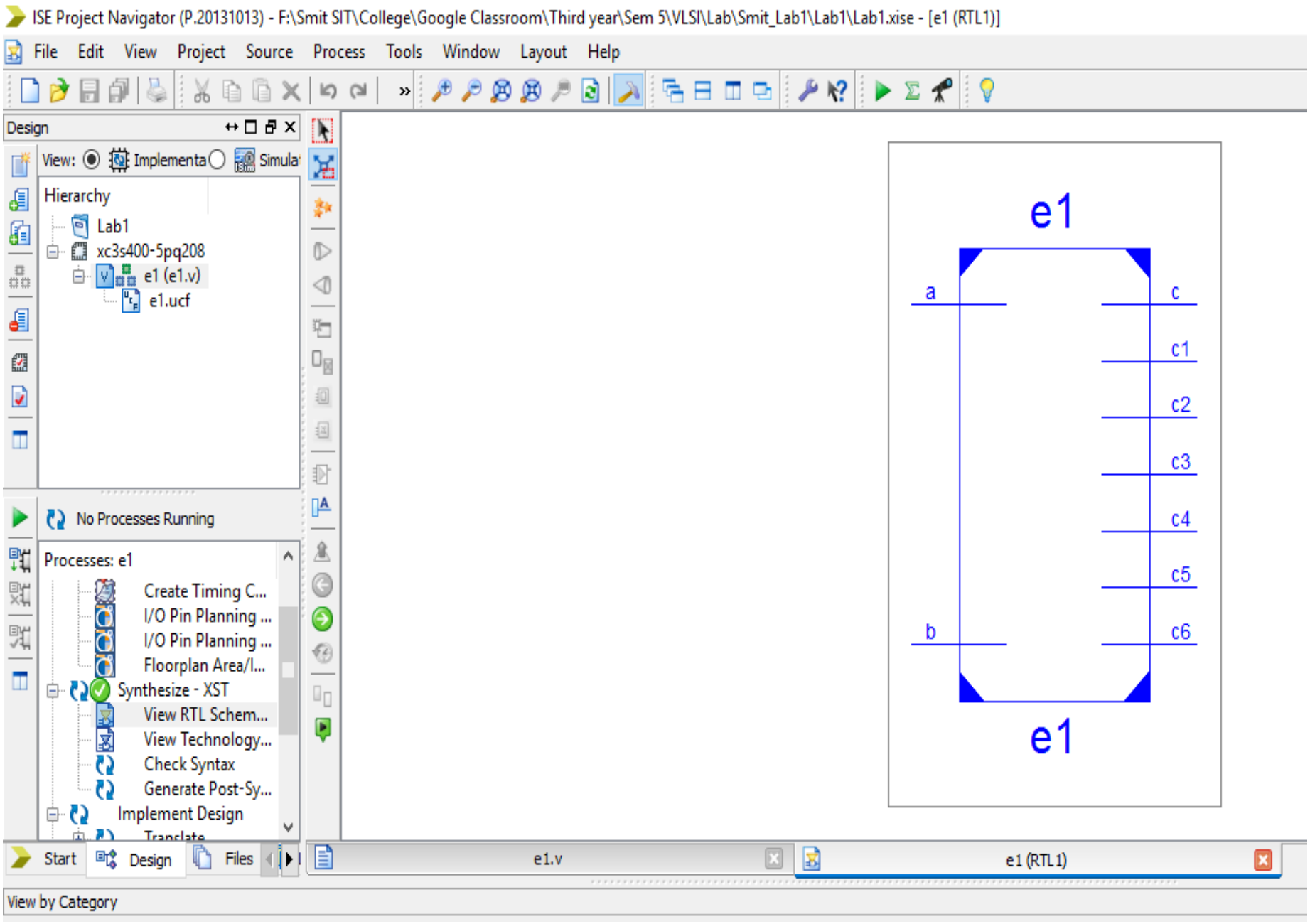
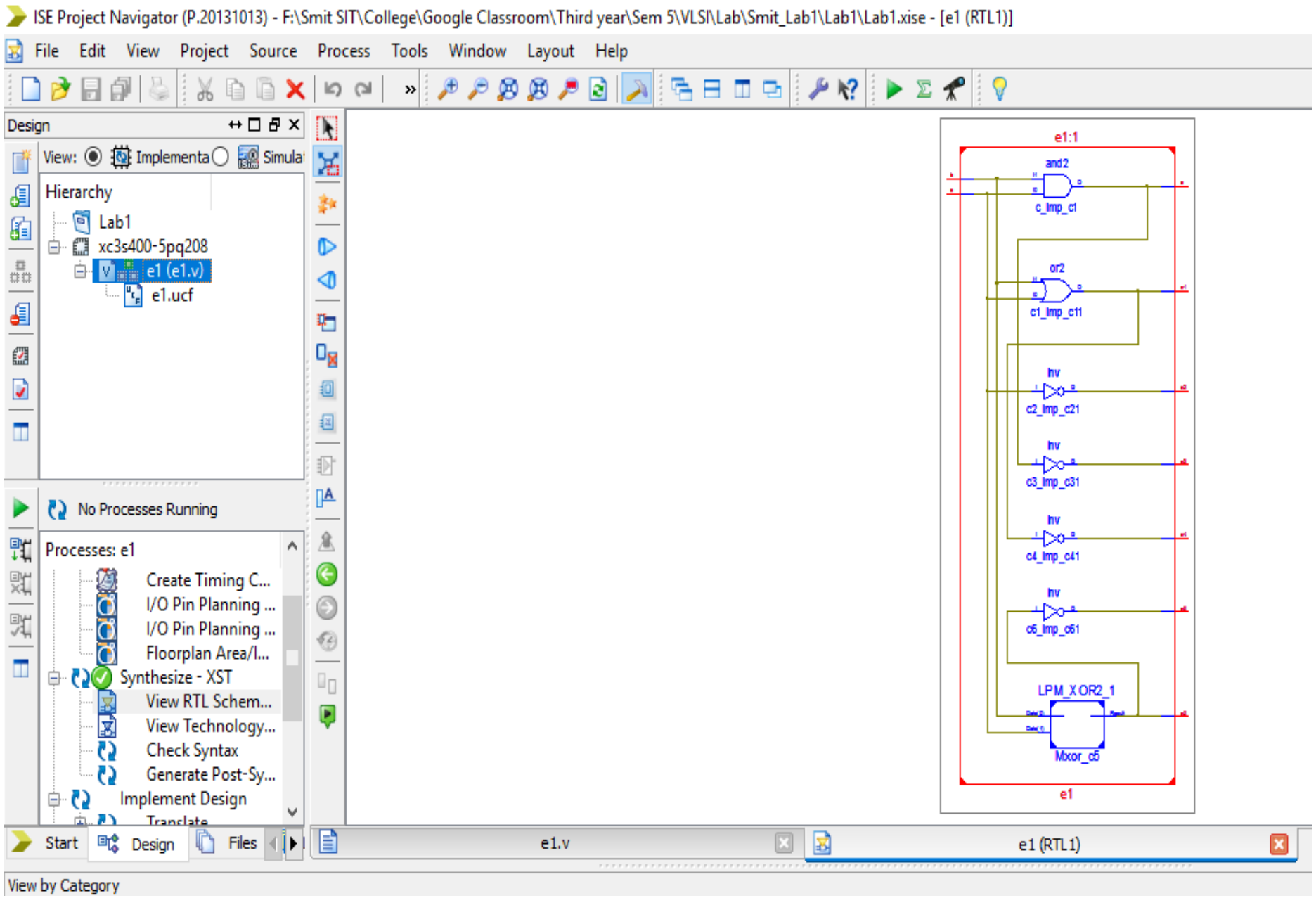
Source Code And Output




ISE Project Navigator (P.20131013) - F:\Smit SIT\College\Google Classroom\Third year\Sem 5\VLSI\Lab\Smit_Lab1\Lab1\Lab1.xise - [e1 (RTL1)]
File Edit View Project Source Process Tools Window Layout Help
Design
View: Implementa Simula
Hierarchy
Lab1
xc3s400-5pq208
e1 (e1.v)
e1.ucf
No Processes Running
Processes: e1
Create Timing C...
I/O Pin Planning ...
I/O Pin Planning ...
Floorplan Area/I...
Synthesize - XST
View RTL Schem...
View Technology...
Check Syntax
Generate Post-Sy...
Implement Design
Start
Design
Files
e1.v
e1 (RTL1)
View by Category
e1
a
b
c
c1
c2
c3
c4
c5
c6
e1

RTL Schematic



Technology Schematic