

SR Flip Flop

Source Code, Test Bench And Output

ISE Project Navigator (P.20131013) - F:\Smit SIT\College\Google Classroom\Third year\Sem 5\VLSI\Lab\Lab5\exp5\exp5.xise - [sr_ff.v]

File Edit View Project Source Process Tools Window Layout Help

Design

View: ☐ Implementa ☒ Simula

Behavioral

Hierarchy

- xc3s400-5pq208
 - d_ff_tb (d_ff_tb.v)
 - uut - d_ff (d_ff.v)
 - jk_ff_tb (jk_ff_tb.v)
 - uut - jk_ff (jk_ff.v)
 - sr_ff_tb (sr_ff_tb.v)
 - uut - sr_ff (sr_ff.v)
 - t_ff_tb (t_ff_tb.v)
 - uut - t_ff (t_ff.v)

No Processes Running

Processes: uut - sr_ff

- ISim Simulator
- Behavioral Check Sy...
- Simulate Behavioral ...

```
17 // Revision 0.01 - File Created
18 // Additional Comments:
19 //
20 ///////////////////////////////////////////////////////////////////
21 module sr_ff(s,r,preset,clr,clk,q,qbar);
22 input s,r;
23 input preset, clr, clk;
24 output reg q, qbar;
25
26 initial
27     begin
28         q=0;
29         qbar=1;
30     end
31
32 always @(posedge clk)
33     case({preset,clr,s,r})
34         4'b1100: begin q=1; qbar=0; end
35         4'b0000: begin q=0; qbar=1; end
36         4'b0100: begin q=q; qbar=qbar; end
37         4'b0101: begin q=0; qbar=1; end
38         4'b0110: begin q=1; qbar=0; end
39         4'b0111: begin q=1'bx; qbar=1'bx; end
40     endcase
41 endmodule
42
```

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Processes: uut - sr_ff

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```
24
25 module sr_ff_tb;
26
27     // Inputs
28     reg s;
29     reg r;
30     reg preset;
31     reg clr;
32     reg clk;
33
34     // Outputs
35     wire q;
36     wire qbar;
37
38     // Instantiate the Unit Under Test (UUT)
39     sr_ff uut (
40         .s(s),
41         .r(r),
42         .preset(preset),
43         .clr(clr),
44         .clk(clk),
45         .q(q),
46         .qbar(qbar)
47     );
48
49     initial begin
```

sr_ff_tb.v

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No Processes Running

Processes: uut - sr_ff

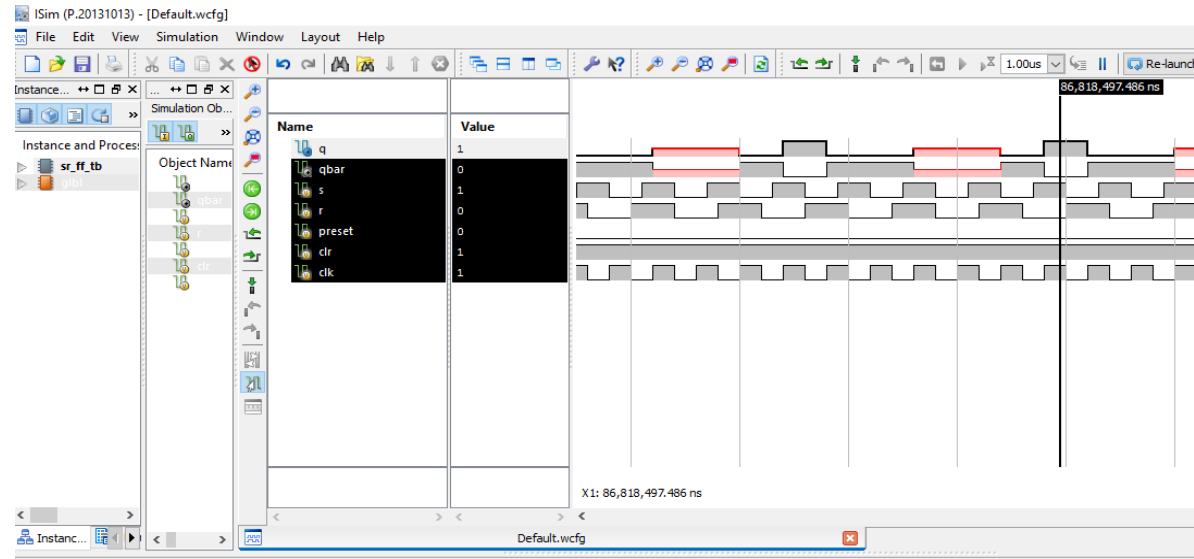
- ISim Simulator
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```
48
49 initial begin
50     // Initialize Inputs
51     #1 $monitor("s=%b",s,"r=%b",r,"clk=%b",clk,"clr=%b",clr,"preset=%b",preset,"q=%b",q,"qbar=%b",qbar);
52     // For Preset
53     preset=1;
54     clr=1;
55     s=1'b0;
56     r=1'b0;
57     clk=1; #10;
58
59     // For Clear
60
61     preset=0;
62     clr=0; #10;
63
64     // For SR Flip Flop
65
66     clr=1;
67     s=1'b0;
68     r=1'b0; #10;
69
70
71     s=1'b0;
72     r=1'b1; #10;
73
```

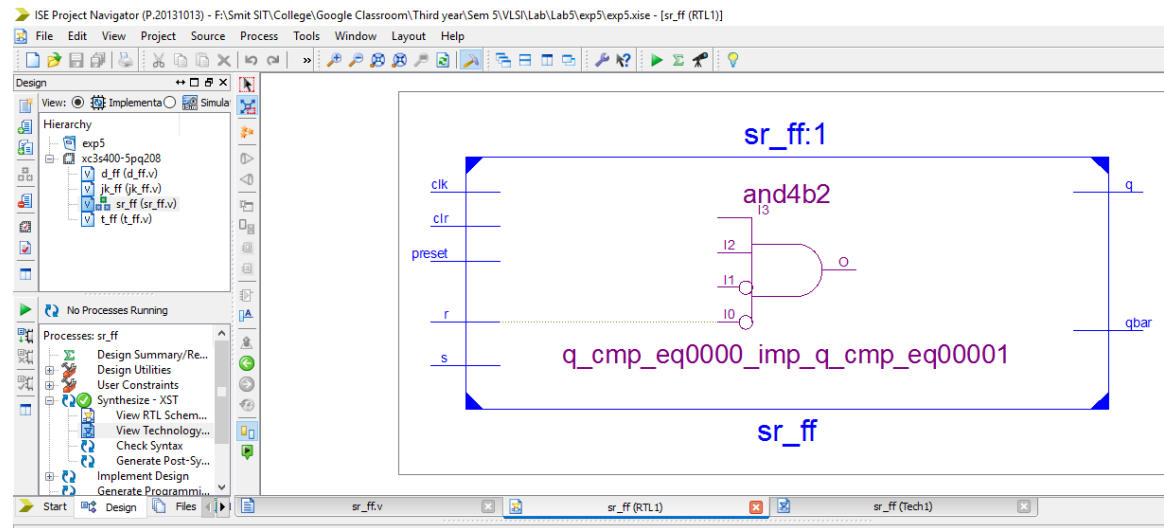
sr_ff_tb.v

sr_ff.v

```
74
75     s=1'b1;
76     r=1'b0; #10;
77
78
79     s=1'b1;
80     r=1'b1; #10;
81 end
82 always #10 clk=~clk;
83 endmodule
84
85
```



RTL Schematic of SR Flip Flop



Technology Schematic of SR Flip Flop

