

# ALU Operator

## Source Code, Test Bench And Output

ISE Project Navigator (P.20131013) - F:\Smit SIT\College\Google Classroom\Third year\Sem 5\VLSI\Lab\Lab8\exp8\_alu\exp8\_alu.xise - [alu\_operation.v]

File Edit View Project Source Process Tools Window Layout Help

Design

View: ☐ Implementa ☒ Simula

Behavioral

Hierarchy

exp8\_alu  
xa7a100t-2lcs324  
alu\_operation\_tb (alu\_ope  
uut - alu\_operation (a

No Processes Running

Processes: alu\_operation\_tb  
ISim Simulator  
Behavioral Check Sy...  
Simulate Behavioral ...

```

16 // Revision:
17 // Revision 0.01 - File Created
18 // Additional Comments:
19 //
20 ///////////////////////////////////////////////////////////////////
21 module alu_operation(
22     input [7:0] a,
23     input [7:0] b,
24     input [7:0] c,
25     output reg [8:0] z, z1, z2, z3, z4, z5, z6, z7
26 );
27 always@(a or b)
28 begin
29     case(c)
30         3'd0: z=a+b;
31         3'd1: z1=a-b;
32         3'd2: z2=a*b;
33         3'd3: z3=a<<1;
34         3'd4: z4=b<<1;
35         3'd5: z5=a&b;
36         3'd6: z6=a|b;
37         3'd7: z7=a^b;
38     endcase
39 end
40 endmodule
41

```

alu\_operation.v

alu\_operation\_tb.v

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```

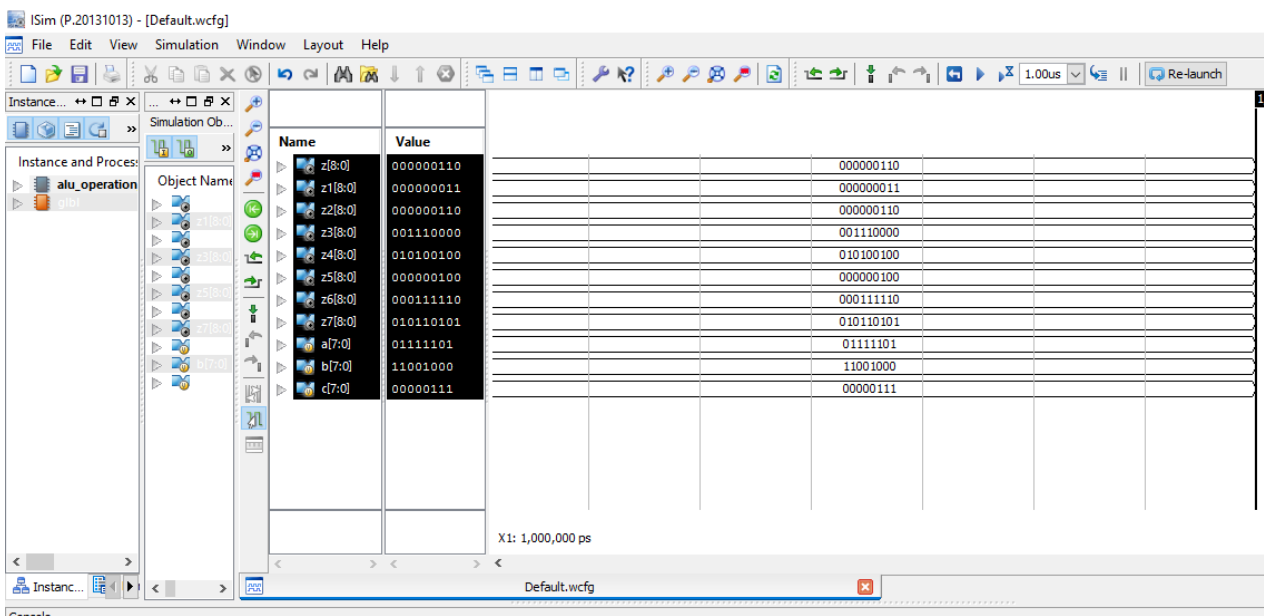
25 module alu_operation_tb;
26
27 // Inputs
28 reg [7:0] a;
29 reg [7:0] b;
30 reg [7:0] c;
31
32 // Outputs
33 wire [8:0] z, z1, z2, z3, z4, z5, z6, z7;
34
35 // Instantiate the Unit Under Test (UUT)
36 alu_operation uut (
37     .a(a),
38     .b(b),
39     .c(c),
40     .z(z),
41     .z1(z1),
42     .z2(z2),
43     .z3(z3),
44     .z4(z4),
45     .z5(z5),
46     .z6(z6),
47     .z7(z7)
48 );
49
50 initial begin
51     // Initialize Inputs
52     c = 0;
53     a = 1;
54     b = 5;
55
56     #20 c=1; a=5; b=2;
57
58     #20 c=2; a=3; b=2;
59
60     #20 c=3; a=56;
61
62     #20 c=4; b=82;
63
64     #20 c=5; a=15; b=20;
65
66     #20 c=6; a=50; b=62;
67
68     #20 c=7; a=125; b=200;
69
70 end
71 endmodule
72
73
74

```

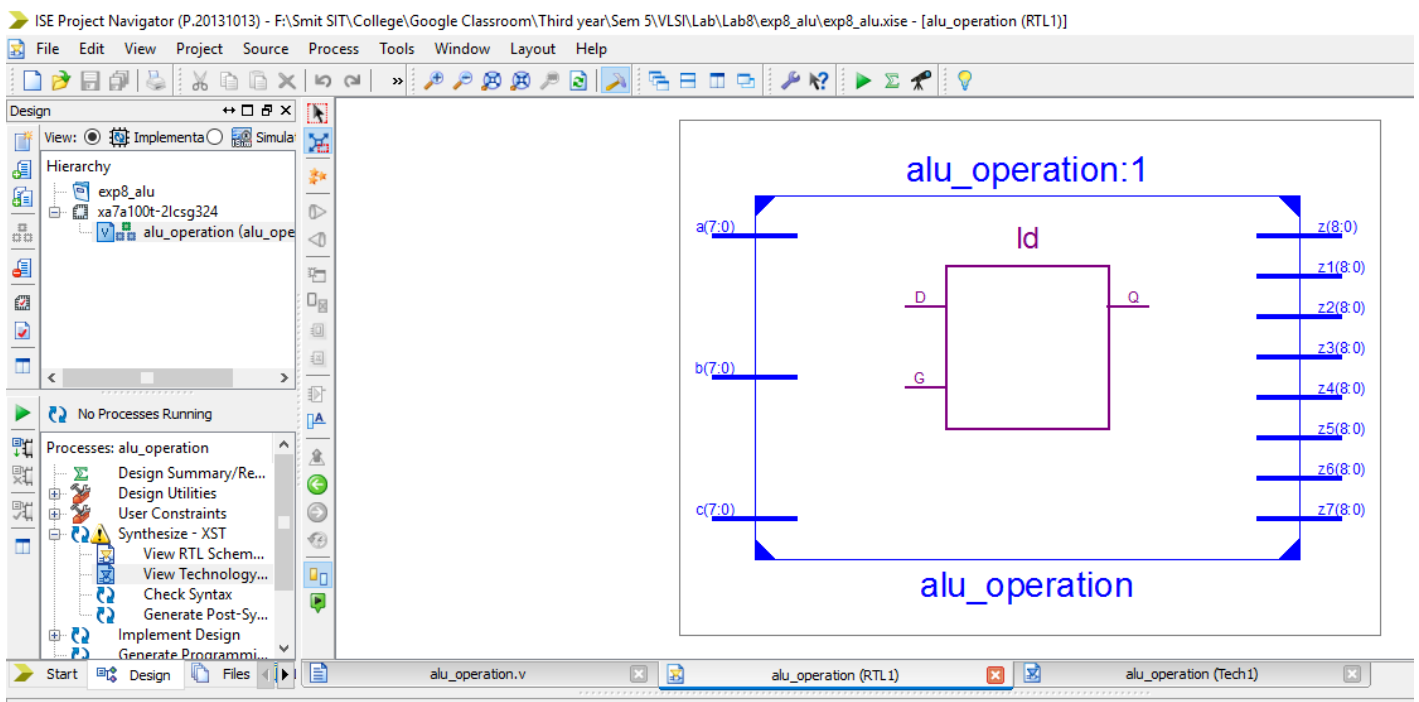
alu\_operation.v

alu\_operation\_tb.v

Console



## RTL Schematic



# Technology Schematic

