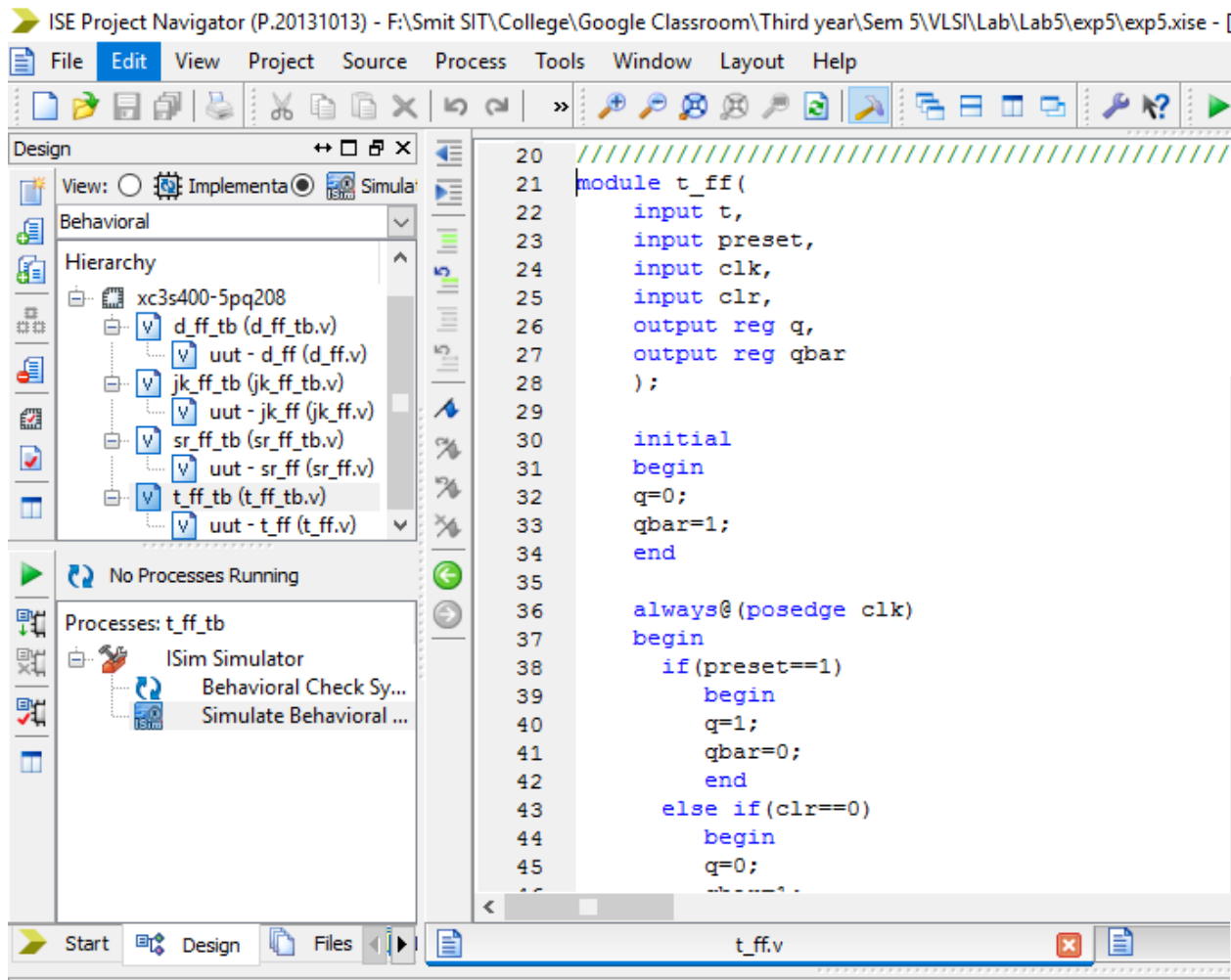


T Flip Flop

Source Code, Test Bench And Output



```
42     end
43     else if(clr==0)
44     begin
45         q=0;
46         qbar=1;
47     end
48     else if(t==0)
49     begin
50         q=q;
51         qbar=qbar;
52     end
53     else
54     begin
55         q=~q;
56         qbar=~qbar;
57     end
58 end
59 endmodule
60
```

File Edit View Project Source Process Tools Window Layout Help

Design

View: ☐ Implementation ☒ Simulation

Behavioral

Hierarchy

xc3s400-5pq208

d_ff_tb (d_ff_tb.v)

ut - d_ff (d_ff.v)

jk_ff_tb (jk_ff_tb.v)

ut - jk_ff (jk_ff.v)

sr_ff_tb (sr_ff_tb.v)

ut - sr_ff (sr_ff.v)

t_ff_tb (t_ff_tb.v)

ut - t_ff (t_ff.v)

No Processes Running

Processes: t_ff_tb

ISim Simulator

Behavioral Check Sy...

Simulate Behavioral ...

```

25 module t_ff_tb;
26
27 // Inputs
28 reg t;
29 reg preset;
30 reg clk;
31 reg clr;
32
33 // Outputs
34 wire q;
35 wire qbar;
36
37 // Instantiate the Unit Under Test (UUT)
38 t_ff uut (
39     .t(t),
40     .preset(preset),
41     .clk(clk),
42     .clr(clr),
43     .q(q),
44     .qbar(qbar)
45 );
46
47 initial begin
48     // Initialize Inputs
49     #1 $monitor("t=",t,"clk=",clk,"clr=",clr,"preset=",preset,"q=",q,"qbar=",qbar);
50     clk=1;

```

Start Design Files

t_ff.v t_ff_tb.v

```

51
52 // For preset
53 clr=1;
54 preset=1; #100;
55
56 // For Clear
57 clr=0;
58 preset=0; #100;
59
60 // For T=0
61 clr=1;
62 t=0; #100;
63
64 // For T=1
65 t=1; #100;
66 end
67 always #10 clk=~clk;
68 always #30 t=~t;
69 endmodule
70

```

File Edit View Simulation Window Layout Help

Instance... Simulation Ob...

Instance and Process

t_ff_tb

Object Name

q

qbar

presel

clk

clr

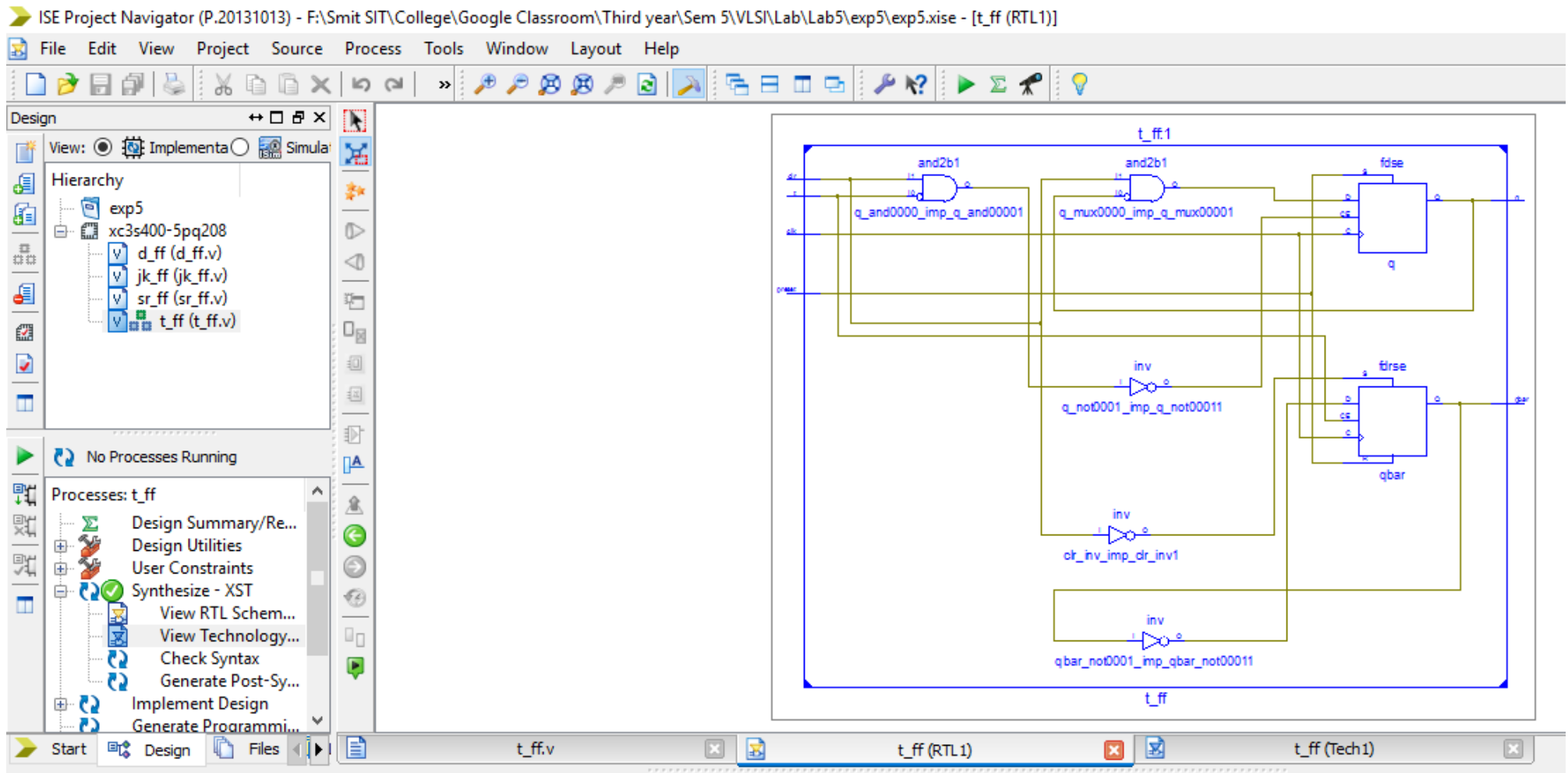
Name	Value
q	0
qbar	1
t	1
presel	0
clk	0
clr	1

2,950,393.367 ns

X1: 2,950,393.367 ns

Default.wcfg

RTL Schematic of T Flip Flop



Technology Schematic of T Flip Flop

