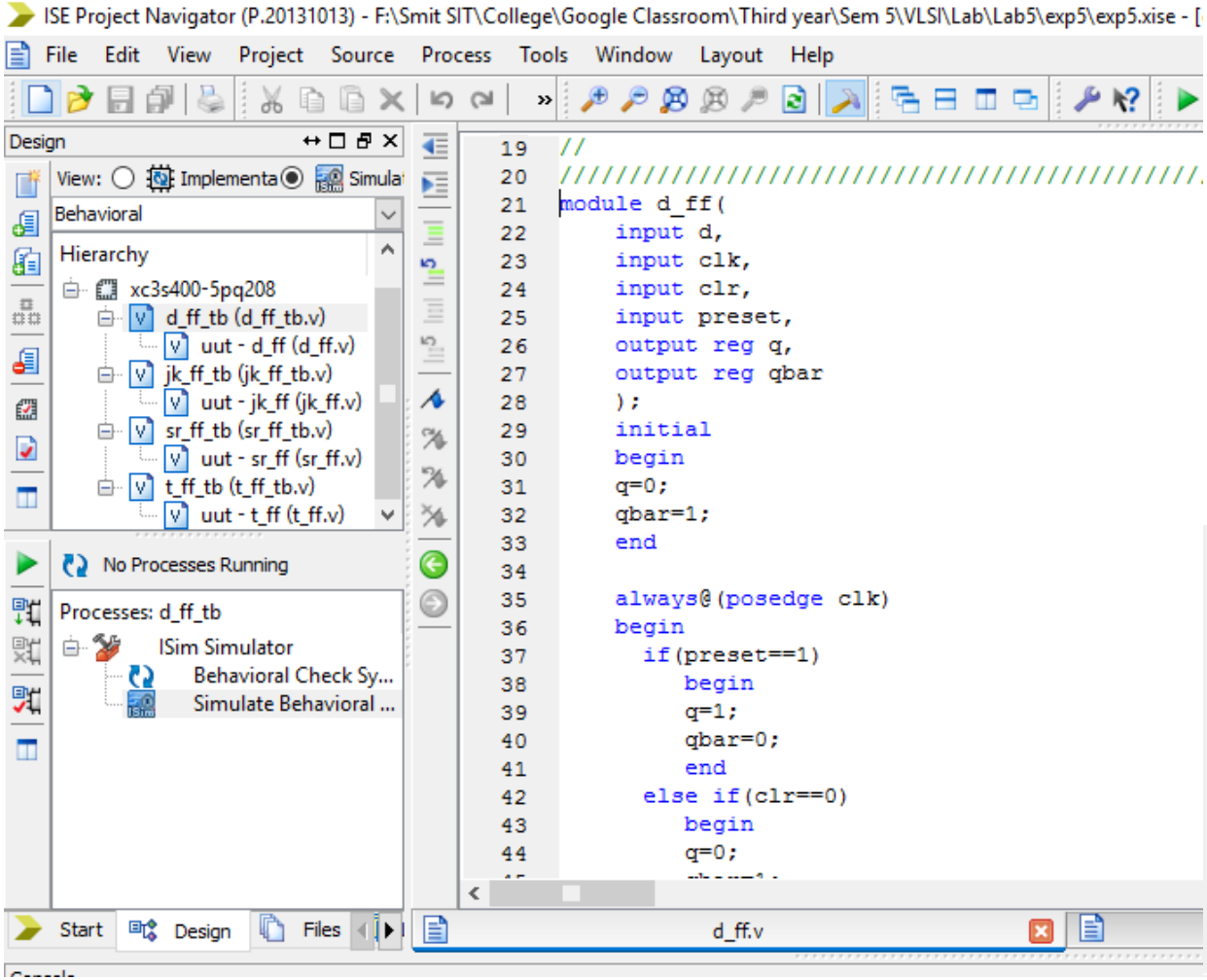
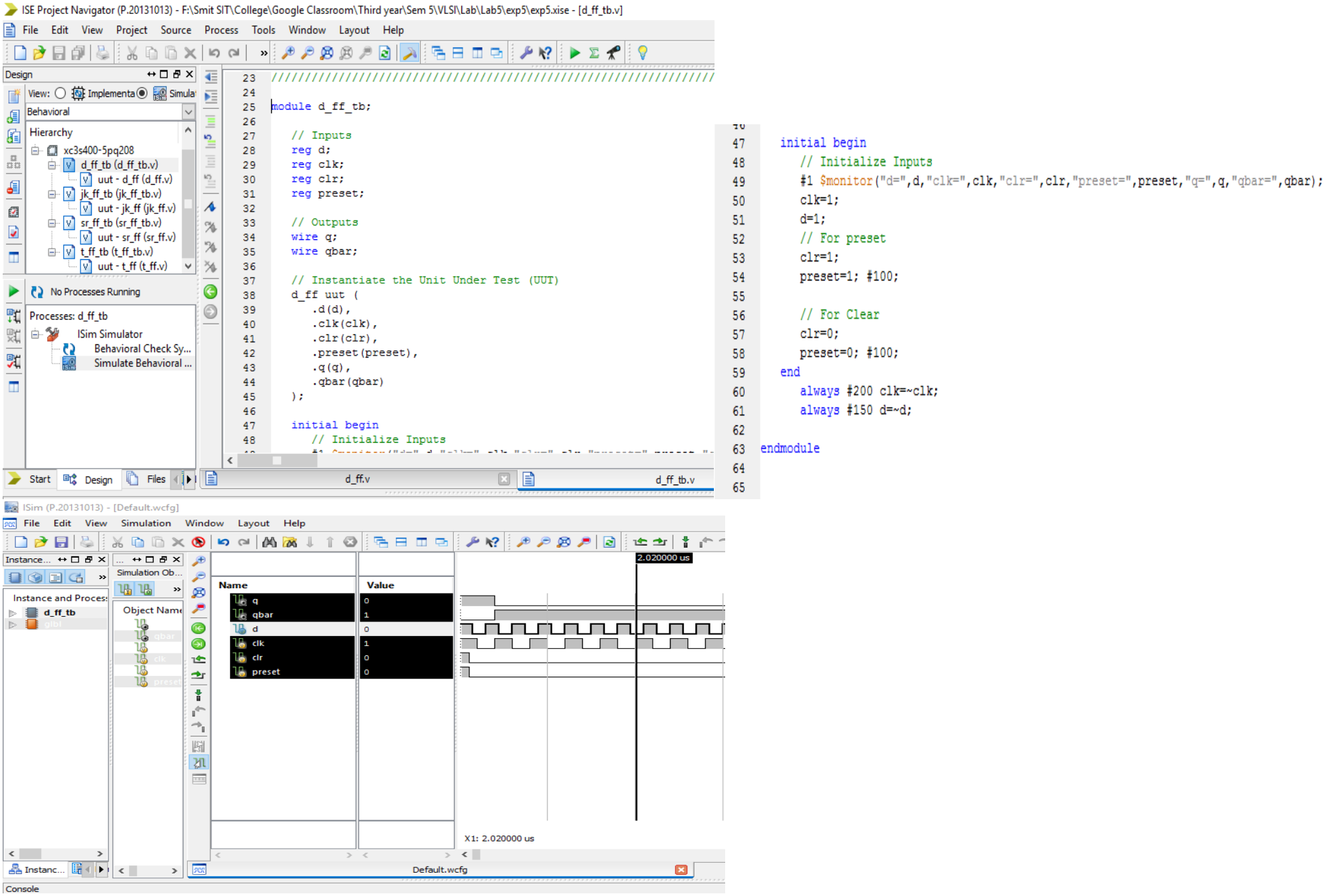
D Flip Flop

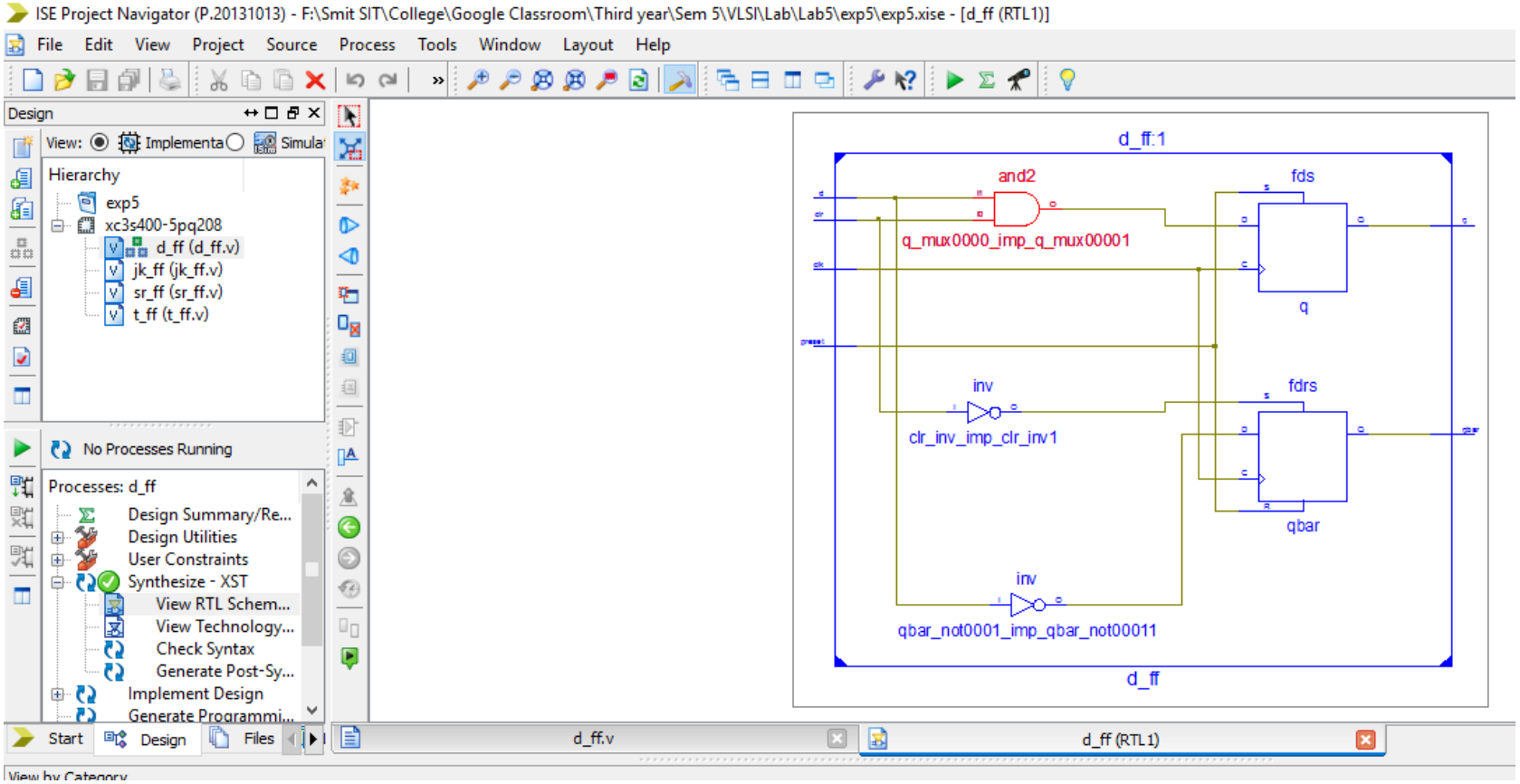
Source Code, Test Bench And Output




```
41            end
42        else if(clr==0)
43            begin
44            q=0;
45            qbar=1;
46            end
47        else
48            begin
49            q=d;
50            qbar=~d;
51            end
52    end
53 endmodule
54
```


ISE Project Navigator (P.20131013) - F:\Smit SIT\College\Google Classroom\Third year\Sem 5\VLSI\Lab\Lab5\exp5\exp5.xise - [d_ff_tb.v]
File Edit View Project Source Process Tools Window Layout Help
Design
Behavioral
Hierarchy
xc3s400-5pq208
d_ff_tb (d_ff_tb.v)
uut - d_ff (d_ff.v)
jk_ff_tb (jk_ff_tb.v)
uut - jk_ff (jk_ff.v)
sr_ff_tb (sr_ff_tb.v)
uut - sr_ff (sr_ff.v)
t_ff_tb (t_ff_tb.v)
uut - t_ff (t_ff.v)
No Processes Running
Processes: d_ff_tb
ISim Simulator
Behavioral Check Sy...
Simulate Behavioral ...
Start Design Files
d_ff.v
d_ff_tb.v
23 //
24
25 module d_ff_tb;
26
27 // Inputs
28 reg d;
29 reg clk;
30 reg clr;
31 reg preset;
32
33 // Outputs
34 wire q;
35 wire qbar;
36
37 // Instantiate the Unit Under Test (UUT)
38 d_ff uut (
39 .d(d),
40 .clk(clk),
41 .clr(clr),
42 .preset(preset),
43 .q(q),
44 .qbar(qbar)
45);
46
47 initial begin
48 // Initialize Inputs
47 initial begin
48 // Initialize Inputs
49 #1 $monitor("d=",d,"clk=",clk,"clr=",clr,"preset=",preset,"q=",q,"qbar=",qbar);
50 clk=1;
51 d=1;
52 // For preset
53 clr=1;
54 preset=1; #100;
55
56 // For Clear
57 clr=0;
58 preset=0; #100;
59 end
60 always #200 clk=~clk;
61 always #150 d=~d;
62
63 endmodule
64
65
ISim (P.20131013) - [Default.wcfg]
File Edit View Simulation Window Layout Help
Instance and Proces:
d_ff_tb
glbl
Simulation Ob...
Object Name
qbar
clk
preset
Name
Value
q
qbar
d
clk
clr
preset
0
1
0
1
0
0
2.020000 us
X1: 2.020000 us
Default.wcfg
Console

RTL Schematic of D Flip Flop



Technology Schematic of D Flip Flop