

Spartan 3 FPGA Kit

The screenshot displays the ISE Project Navigator (P.68d) interface for a project named 'b2'. The main window shows the Verilog code for a fulladder module. The left pane shows the project hierarchy with 'fulladder (D:\B2\b2\b2.v)' selected. The bottom pane shows the 'I/O Ports' table, which lists the ports and their properties.

Verilog Code:

```
6 // Create Date: 16:44:59 10/12/2019
7 // Design Name:
8 // Module Name: b2
9 // Project Name:
10 // Target Devices:
11 // Tool versions:
12 // Description:
13 //
14 // Dependencies:
15 //
16 // Revision:
17 // Revision 0.01 - File Created
18 // Additional Comments:
19 //
20 ///////////////////////////////////////////////////////////////////
21 module fulladder(
22 input a, b, cin,
23 output s,c
24 );
25 wire y1,y2,y3;
26 xor(s,a,b,cin);
27 and(y1,a,b);
28 and(y2,cin,b);
29 and(y3,a,cin);
30 or(c,y1,y2,y3);
31
32 endmodule
33
```

I/O Ports Table:

Name	Direction	Neg Diff Pair	Site	Fixed	Bank	I/O Std	Vcco	Vref	Drive Stre...	Slew Type	Pull Type
All ports (5)											
Scalar ports (5)											
a	Input		P34	<input checked="" type="checkbox"/>		6 default (LVCMOS25)	2.500				NONE
b	Input		P35	<input checked="" type="checkbox"/>		6 default (LVCMOS25)	2.500				NONE
c	Output		P71	<input checked="" type="checkbox"/>		5 default (LVCMOS25)	2.500		12 SLOW		NONE
cin	Input		P36	<input checked="" type="checkbox"/>		6 default (LVCMOS25)	2.500				NONE
s	Output		P72	<input checked="" type="checkbox"/>		5 default (LVCMOS25)	2.500		12 SLOW		NONE

