

# Source Code And Output

The screenshot displays the ISE Project Navigator and ISim simulation windows. The Project Navigator on the left shows the project hierarchy with 'Lab1' and 'xc3s400-5pq208' selected. The ISim window on the right shows the simulation results for 'e1.v'.

**Source Code (e1.v):**

```
14 // Dependencies:
15 //
16 // Revision:
17 // Revision 0.01 - File Created
18 // Additional Comments:
19 //
20 //////////////////////////////////////////////////
21 module e1(
22     input a,
23     input b,
24     output c,
25     output c1,
26     output c2,
27     output c3,
28     output c4,
29     output c5,
30     output c6
31 );
32 and(c,a,b);
33 or(c1,a,b);
34 not(c2,a);
35 nand(c3,a,b);
36 nor(c4,a,b);
37 xor(c5,a,b);
38 xnor(c6,a,b);
39
40 endmodule
```

**Simulation Results:**

The simulation results show the values of signals a, b, c, c1, c2, c3, c4, c5, and c6 over time. The signals are represented by green waveforms on a black background. The time range shown is from 4,579,468,500 ps to 4,579,469,500 ps. The simulation time is 6,742,845,800 ps.

**Console Output:**

```
ISim simulation engine GUI launched successfully
Process "Simulate Behavioral Model" completed successfully
```

**Simulation Commands:**

```
# isim force add {/e1/a} 1 -radix bin -value 0 -radix bin -time 100 ps -repeat 200 ps
ISim>
# isim force add {/e1/b} 0 -radix bin -value 1 -radix bin -time 75 ps -repeat 150 ps
ISim>
# isim force add {/e1/b} 0 -radix bin -value 1 -radix bin -time 75 ps -repeat 150 ps
ISim>
# run all
```

ISE Project Navigator (P.20131013) - F:\Smit SIT\College\Google Classroom\Third year\Sem 5\VLSI\Lab\Smit\_Lab1\Lab1.xise - [e1 (RTL1)]

File Edit View Project Source Process Tools Window Layout Help

Design

View: ☒ Implementa ☐ Simula

Hierarchy

- Lab1
  - xc3s400-5pq208
    - e1 (e1.v)
    - e1.ucf

No Processes Running

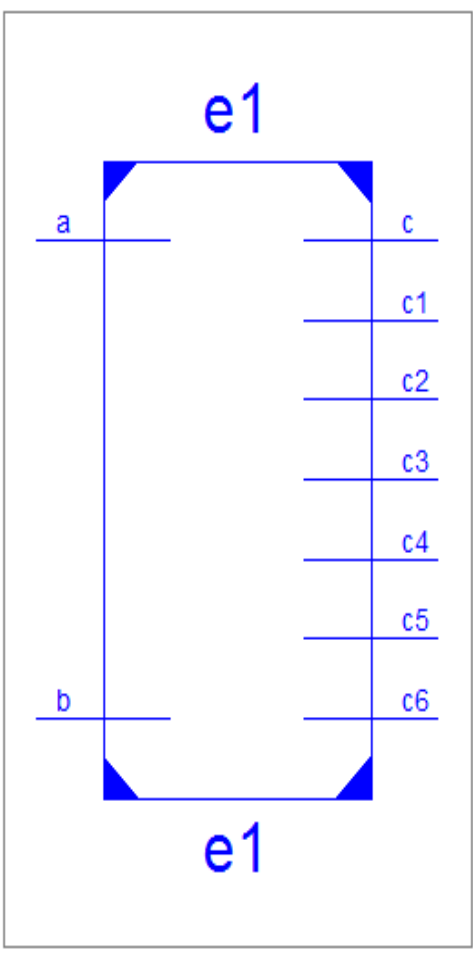
Processes: e1

- Create Timing C...
- I/O Pin Planning ...
- I/O Pin Planning ...
- Floorplan Area/I...
- Synthesize - XST
- View RTL Schem...
- View Technology...
- Check Syntax
- Generate Post-Sy...
- Implement Design
- Translate

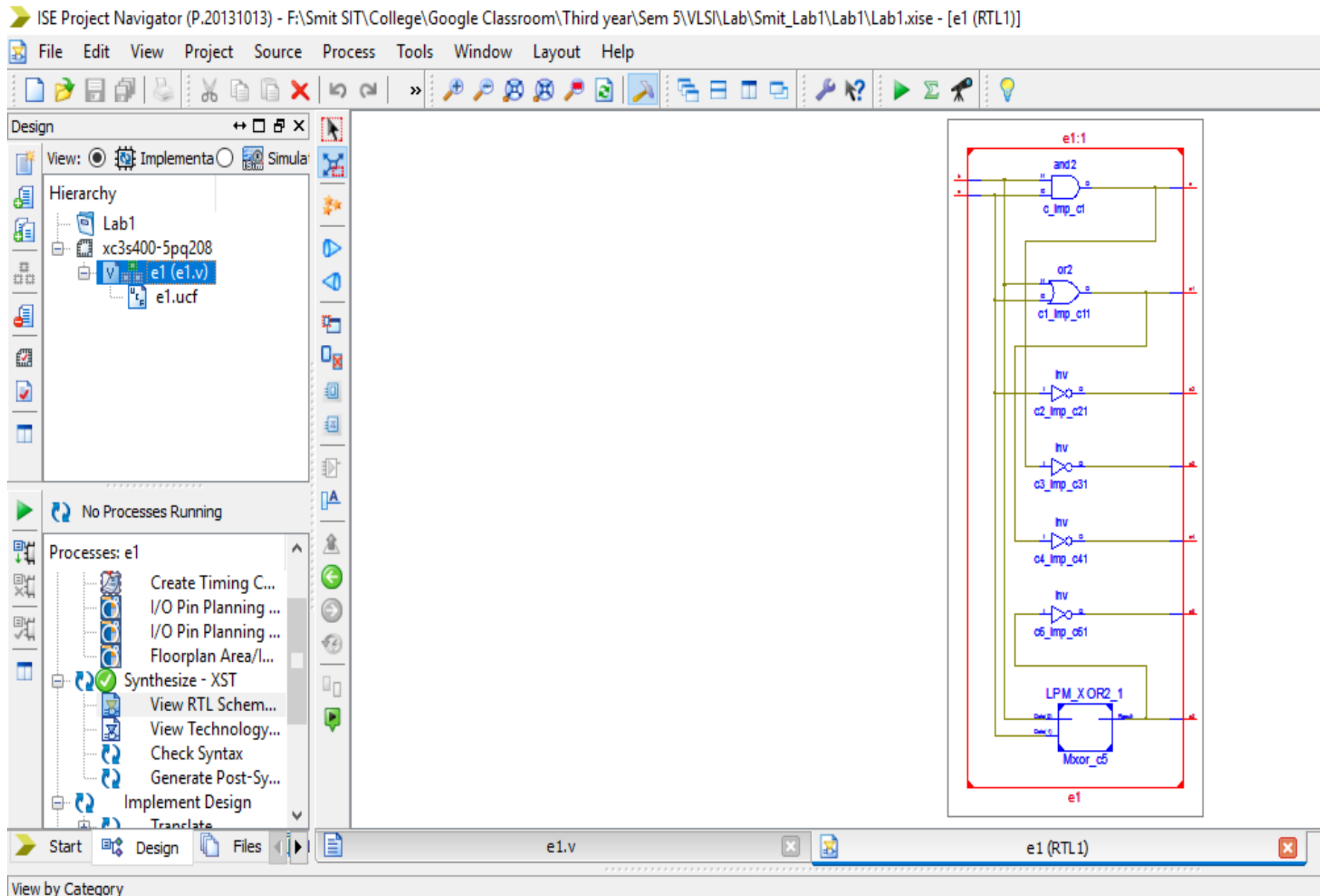
Start Design Files

e1.v e1 (RTL1)

View by Category



## RTL Schematic



## Technology Schematic

