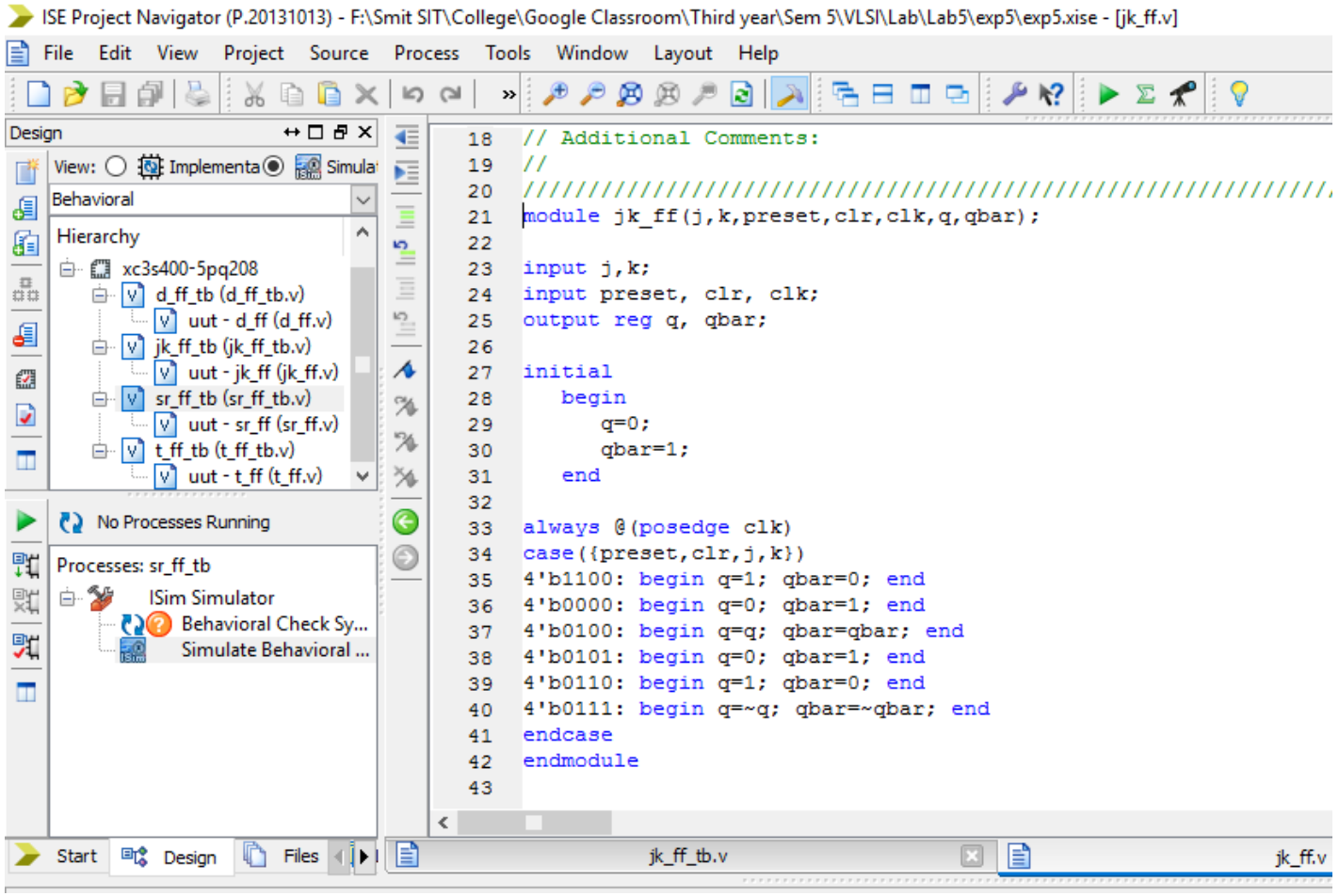
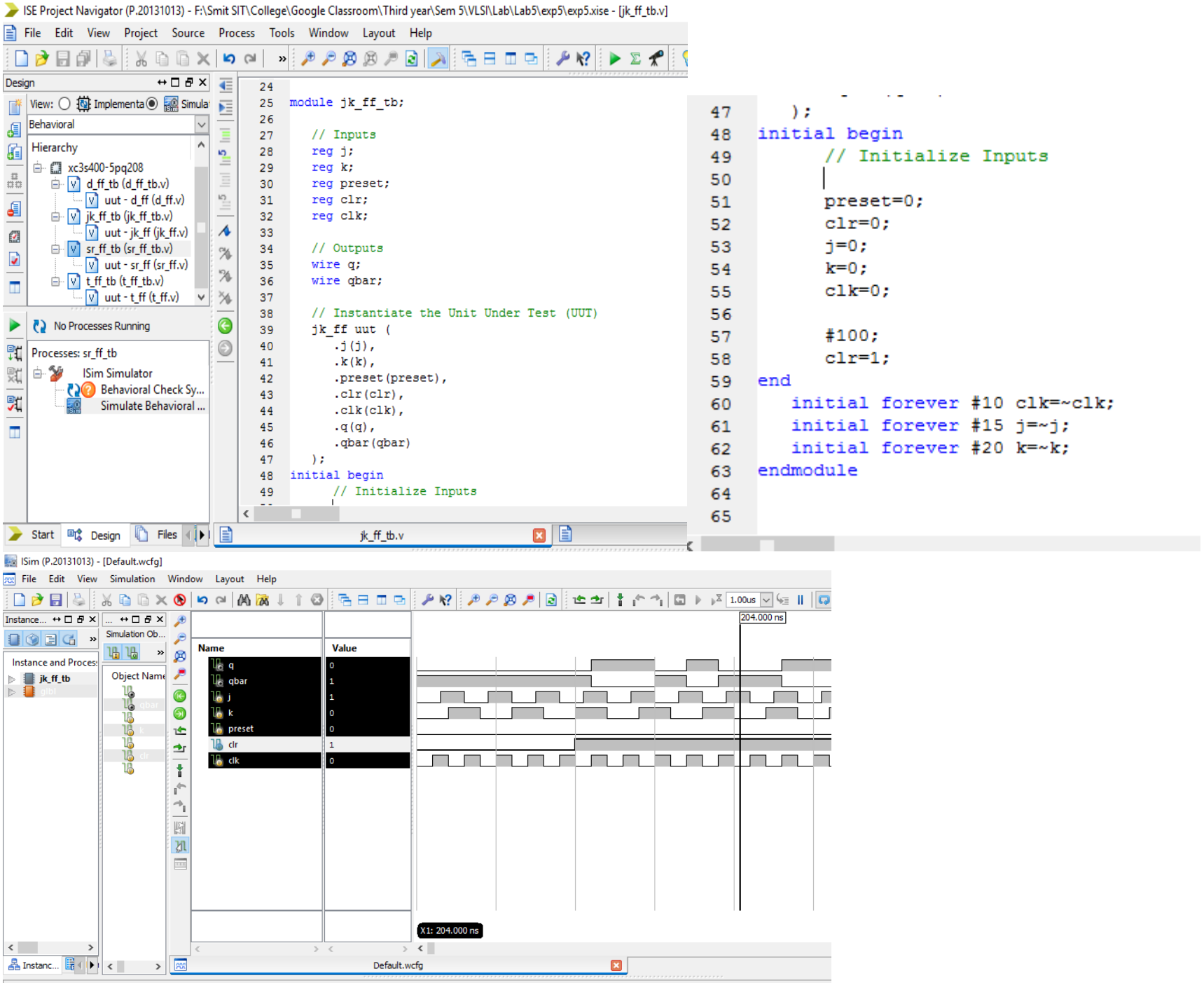
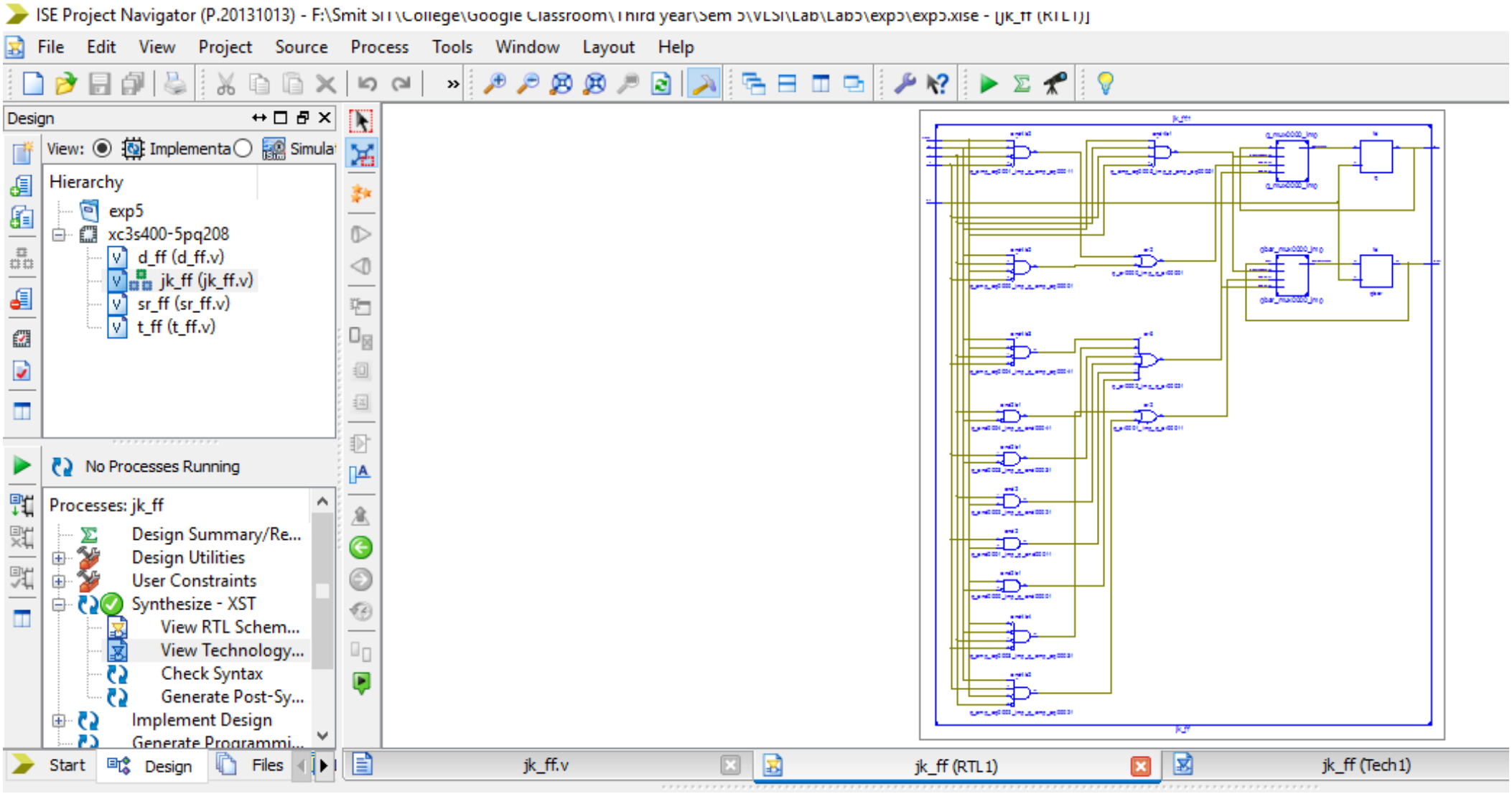
JK Flip Flop

Source Code, Test Bench And Output




ISE Project Navigator (P.20131013) - F:\Smit SIT\College\Google Classroom\Third year\Sem 5\VLSI\Lab\Lab5\exp5\exp5.xise - [jk_ff_tb.v]
File Edit View Project Source Process Tools Window Layout Help
Design
Behavioral
Hierarchy
xc3s400-5pq208
d_ff_tb (d_ff_tb.v)
uut - d_ff (d_ff.v)
jk_ff_tb (jk_ff_tb.v)
uut - jk_ff (jk_ff.v)
sr_ff_tb (sr_ff_tb.v)
uut - sr_ff (sr_ff.v)
t_ff_tb (t_ff_tb.v)
uut - t_ff (t_ff.v)
No Processes Running
Processes: sr_ff_tb
ISim Simulator
Behavioral Check Sy...
Simulate Behavioral ...
Start Design Files
jk_ff_tb.v
24
25 module jk_ff_tb;
26
27 // Inputs
28 reg j;
29 reg k;
30 reg preset;
31 reg clr;
32 reg clk;
33
34 // Outputs
35 wire q;
36 wire qbar;
37
38 // Instantiate the Unit Under Test (UUT)
39 jk_ff uut (
40 .j(j),
41 .k(k),
42 .preset(preset),
43 .clr(clr),
44 .clk(clk),
45 .q(q),
46 .qbar(qbar)
47);
48 initial begin
49 // Initialize Inputs
47);
48 initial begin
49 // Initialize Inputs
50
51 preset=0;
52 clr=0;
53 j=0;
54 k=0;
55 clk=0;
56
57 #100;
58 clr=1;
59 end
60 initial forever #10 clk=~clk;
61 initial forever #15 j=~j;
62 initial forever #20 k=~k;
63 endmodule
64
65
ISim (P.20131013) - [Default.wcfg]
File Edit View Simulation Window Layout Help
1.00us
204.000 ns
Name
Value
q 0
qbar 1
j 1
k 0
preset 0
clr 1
clk 0
X1: 204.000 ns
Default.wcfg

RTL Schematic of JK Flip Flop



Technology Schematic of JK Flip Flop