

Mealy State Machine

Source Code, Test Bench And Output

ISE Project Navigator (P.20131013) - F:\Smit SIT\College\Google Classroom\Third year\Sem 5\VLSI\Lab\Lab9\mealy_4bit\mealy_4bit.xise - [mealy_4bit.v]

File Edit View Project Source Process Tools Window Layout Help

Design

View: Behavioral

Hierarchy

- mealy_4bit
- xa7a100t-2lcs324
- mealytb (mealytb.v)
- ut - mealy_4bit (mealy_4bit.v)

No Processes Running

Processes: ut - mealy_4bit

- ISim Simulator
- Behavioral Check Sy...
- Simulate Behavioral ...

```
21
22 // ....1010....
23 module mealy_4bit(din, reset, clk, y);
24
25     input din;
26     input reset, clk;
27     output reg y;
28
29     reg [1:0] cst, nst;
30
31     parameter s0=2'd0,
32               s1=2'd1,
33               s2=2'd2,
34               s3=2'd3;
35
36     always@(posedge clk)
37     begin
38         if(reset)
39             cst<=s0;
40         else
41             cst<=nst;
42     end
43
44     always@(din or cst)
45     begin
46         case(cst)
47             s0: if(din==1)
48                 begin
49                     nst=s1;
50                     y=0;
51                 end
52             else
53                 begin
54                     nst=s0;
55                     y=0;
56                 end
57             s1: if(din==1)
58                 begin
59                     nst=s1;
60                     y=0;
61                 end
62             else
63                 begin
64                     nst=s2;
65                     y=0;
66                 end
67             s2: if(din==1)
68                 begin
69                     nst=s3;
70                     y=0;
71                 end
72             else
73                 begin
74                     nst=s0;
75                     y=0;
76                 end
77             s3: if(din==1)
78                 begin
79                     nst=s1;
80                     y=0;
81                 end
82             else
83                 begin
84                     nst=s2;
85                     y=1;
86                 end
87             endcase
88         end
89     end
90 endmodule
91
```

mealytb.v

mealy_4bit.v

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File Edit View Project Source Process Tools Window Layout Help

Design

View: ☐ Implementa ☒ Simula

Behavioral

Hierarchy

- mealy_4bit
 - xa7a100t-2lcs9324
 - mealytb (mealytb.v)
 - uut - mealy_4bit (mealytb.v)

No Processes Running

Processes: uut - mealy_4bit

- ISim Simulator
- Behavioral Check Sy...
- Simulate Behavioral ...

```

24 module mealytb;
25
26
27 // Inputs
28 reg din;
29 reg reset;
30 reg clk;
31
32 // Outputs
33 wire y;
34
35 // Instantiate the Unit Under Test (UUT)
36 mealy_4bit uut (
37     .din(din),
38     .reset(reset),
39     .clk(clk),
40     .Y(y)
41 );
42
43 initial begin
44     // Initialize Inputs
45     din = 0;
46     clk = 0;
47     reset = 1;
48
49
50
51
52
53
54
55
56
57
58
59
60

```

mealytb.v mealy_4bit.v

```

42
43 initial begin
44     // Initialize Inputs
45     din = 0;
46     clk = 0;
47     reset = 1;
48
49
50     // Wait 100 ns for global reset to finish
51     #100;
52     reset=0;
53     // Add stimulus here
54
55 end
56 always #5 clk=~clk;
57 always #12 din=~din;
58 endmodule
59
60

```

ISim (P.20131013) - [Default.wcfg*]

File Edit View Simulation Window Layout Help

Instances and Processes

Object Name

- din
- reset
- clk
- y
- cst[1:0]
- nst[1:0]
- s0[1:0]
- s1[1:0]
- s2[1:0]
- s3[1:0]

Value

Name	Value
y	0
din	1
reset	0
clk	0
din	1
reset	0
clk	0
y	0
cst[1:0]	00
nst[1:0]	01
s0[1:0]	00
s1[1:0]	01
s2[1:0]	10
s3[1:0]	11

55,711,844.400 ns

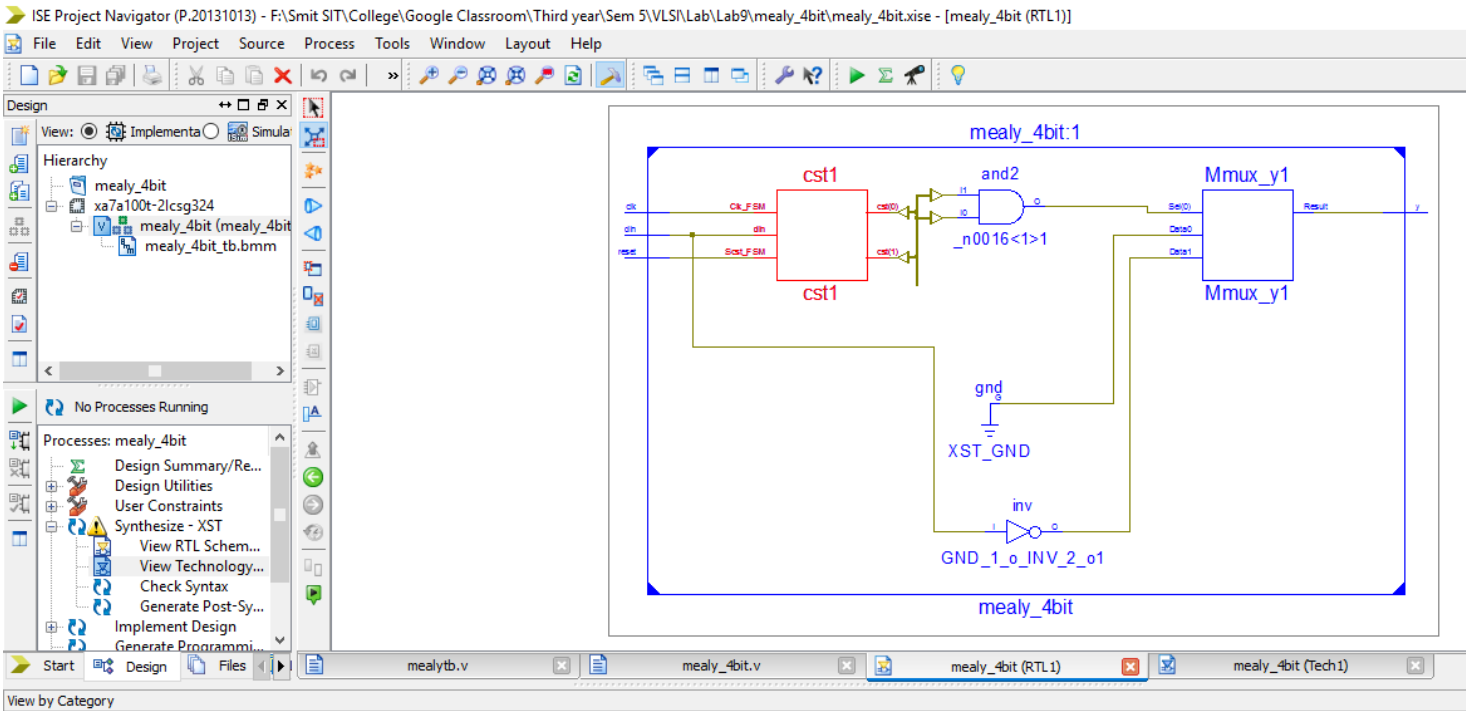
1.00us

Re-launch

55,711,844.400 ns

Default.wcfg*

RTL Schematic



Technology Schematic

