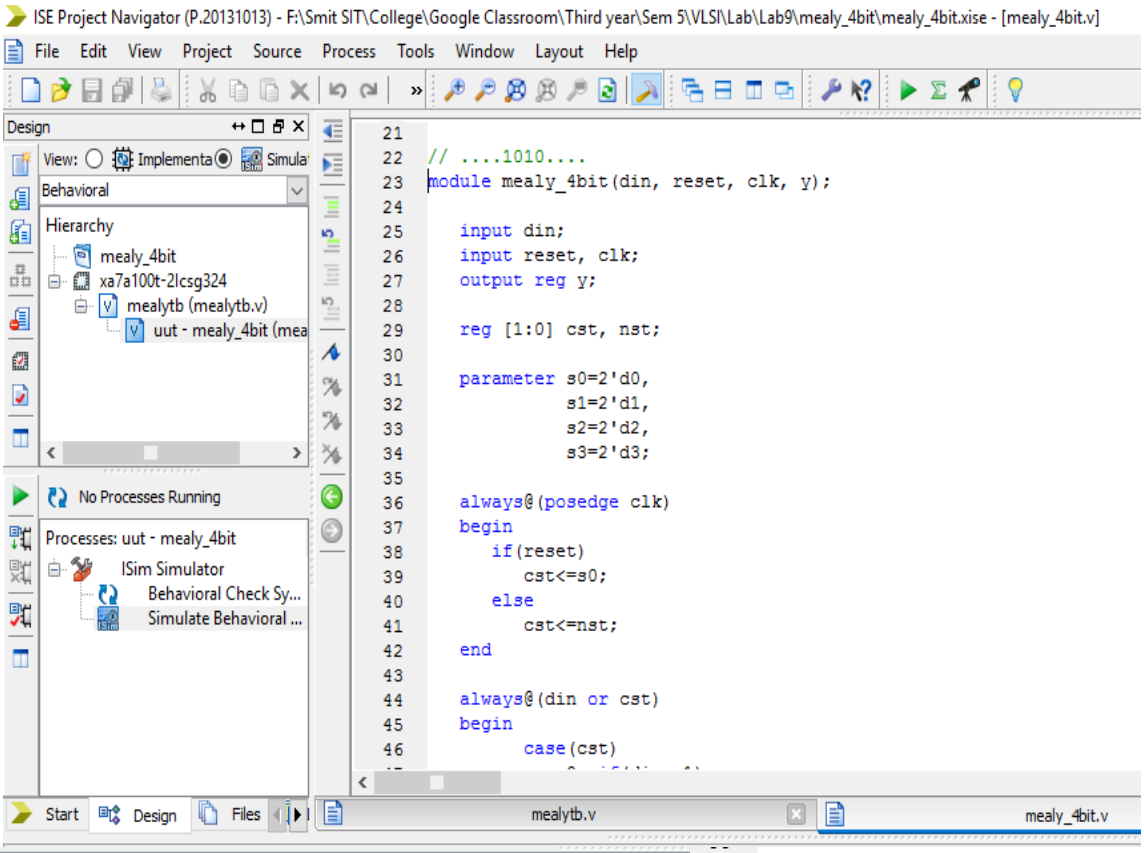
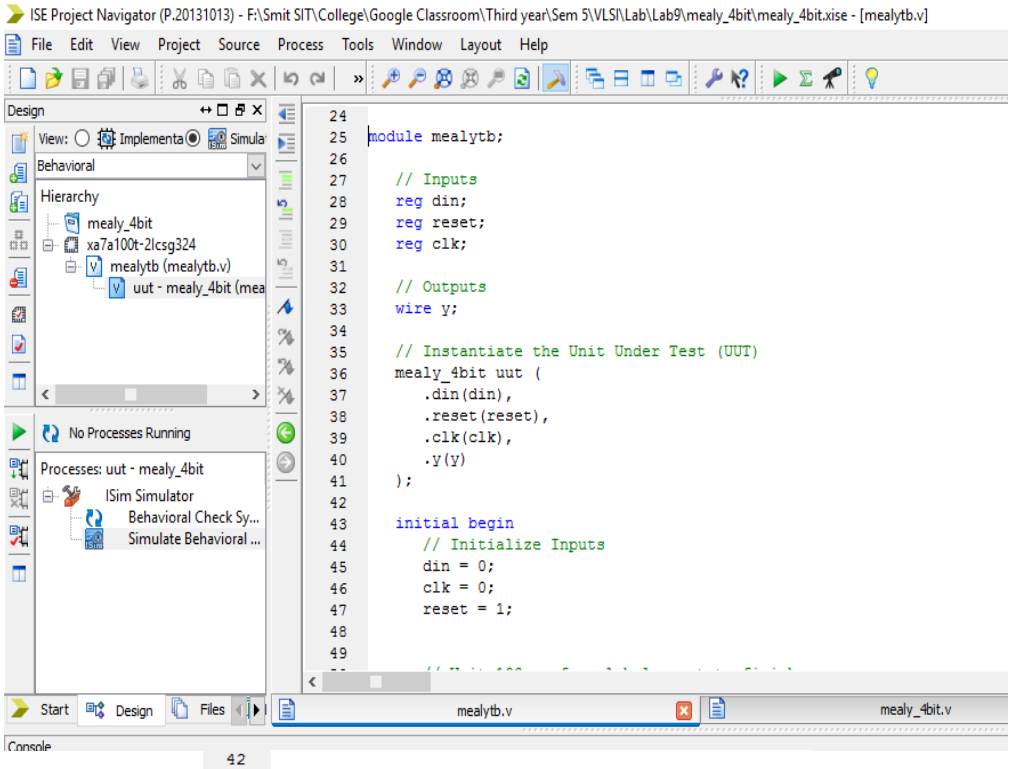
Mealy State Machine

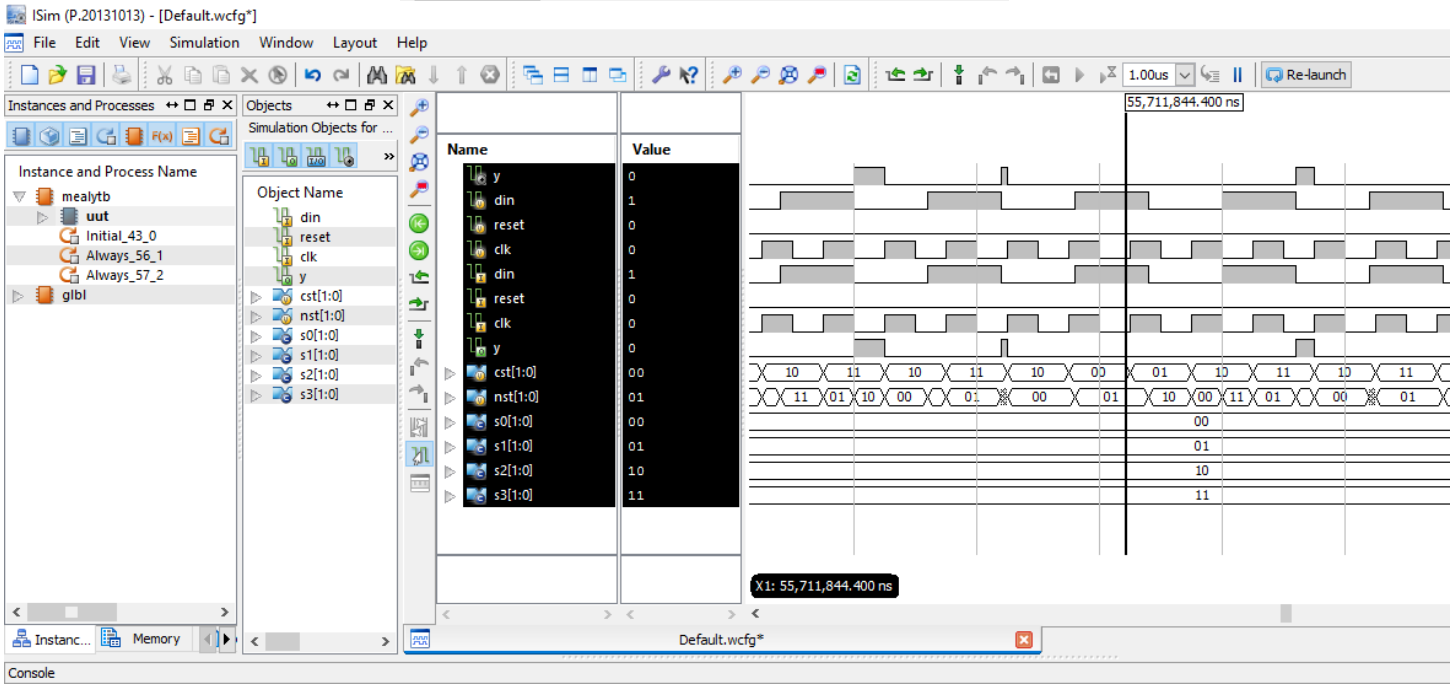
Source Code, Test Bench And Output



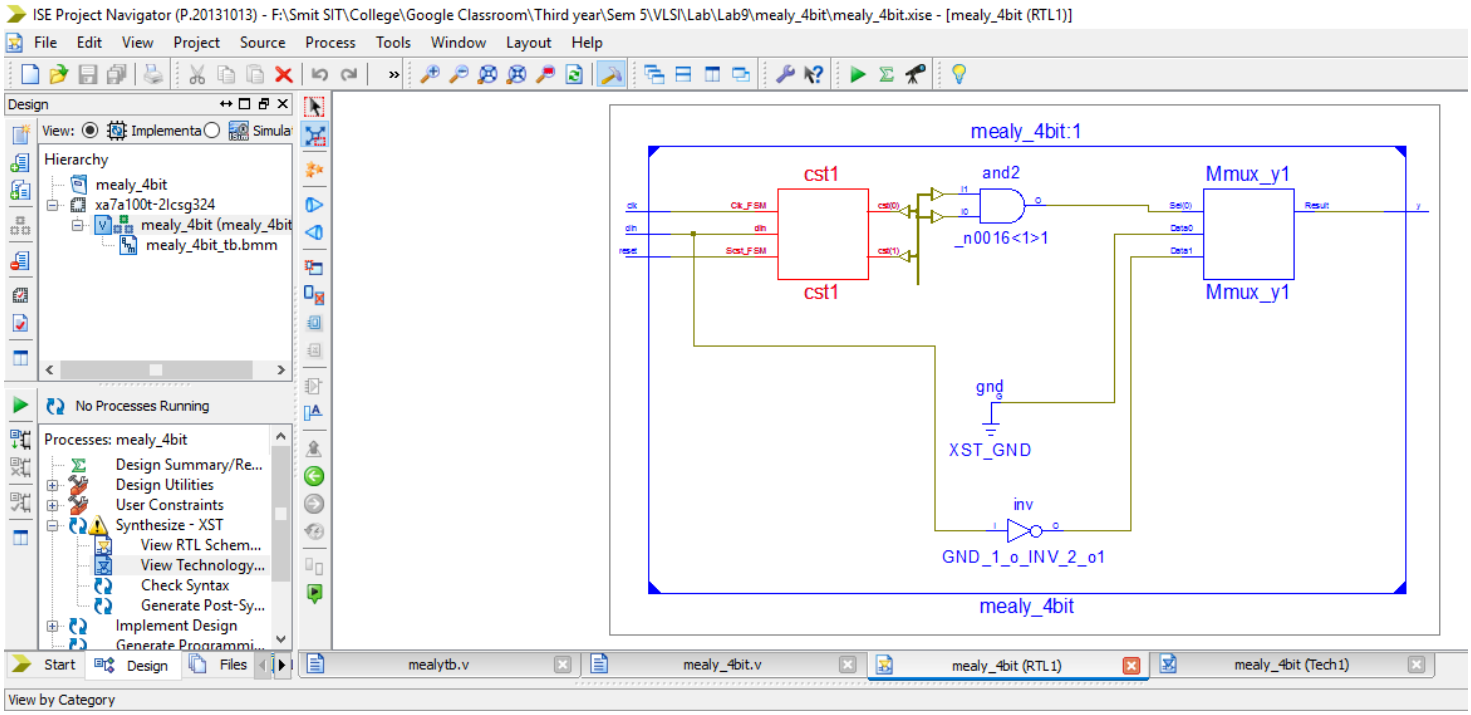

```
44    always@(din or cst)
45    begin
46          case(cst)
47             s0: if(din==1)
48                   begin
49                      nst=s1;
50                      y=0;
51                   end
52                 else
53                   begin
54                      nst=s0;
55                      y=0;
56                   end
57             s1: if(din==1)
58                   begin
59                      nst=s1;
60                      y=0;
61                   end
62                 else
63                   begin
64                      nst=s2;
65                      y=0;
66                   end
67             s2: if(din==1)
68                   begin
69                      nst=s3;
70                      y=0;
71                   end
72                 else
73                   begin
74                      nst=s0;
75                      y=0;
76                   end
77             s3: if(din==1)
78                   begin
79                      nst=s1;
80                      y=0;
81                   end
82                 else
83                   begin
84                      nst=s2;
85                      y=1;
86                   end
87          endcase
88    end
89
90 endmodule
91
```




```
42
43    initial begin
44        // Initialize Inputs
45        din = 0;
46        clk = 0;
47        reset = 1;
48
49
50        // Wait 100 ns for global reset to finish
51        #100;
52          reset=0;
53        // Add stimulus here
54
55    end
56        always #5 clk=~clk;
57        always #12 din=~din;
58 endmodule
59
60
```



RTL Schematic



Technology Schematic