

Full Adder

Source Code And Output

The image displays two side-by-side screenshots of the ISE Project Navigator interface. Both windows show the same project structure and source code for a Full Adder module.

Left Window (e22.v):

- Module Name:** e22
- Project Name:** Exp2
- Target Devices:** xc3s400-5pg208
- Tool versions:** e21 (e21.v), e21_1 (e21_1.v), e21_2 (e21_2.v), e22 (e22.v), e22_1 (e22_1.v), e22_2 (e22_2.v)
- Dependencies:**
- Revision:** Revision 0.01 - File Created
- Additional Comments:**
- Code:**

```
module e22(  
    input a,  
    input b,  
    input cin,  
    output sum,  
    output carry  
);  
wire y1, y2, y3;  
xor(sum, a, b, cin);  
and(y1, a, b);  
and(y2, a, cin);  
and(y3, b, cin);  
or(carry, y1, y2, y3);  
endmodule
```

Right Window (e22_1.v):

- Module Name:** e22_1
- Project Name:** Exp2
- Target Devices:** xc3s400-5pg208
- Tool versions:** e21 (e21.v), e21_1 (e21_1.v), e21_2 (e21_2.v), e22 (e22.v), e22_1 (e22_1.v), e22_2 (e22_2.v)
- Dependencies:**
- Revision:** Revision 0.01 - File Created
- Additional Comments:**
- Code:**

```
module e22_1(  
    input a,  
    input b,  
    input cin,  
    output sum,  
    output carry  
);  
assign sum= a^b^c;  
assign carry= (a&b) | (a&cin) | (b&cin);  
endmodule
```

The image displays the ISE Project Navigator interface with the simulation results for the Full Adder module.

Left Window (e22.v):

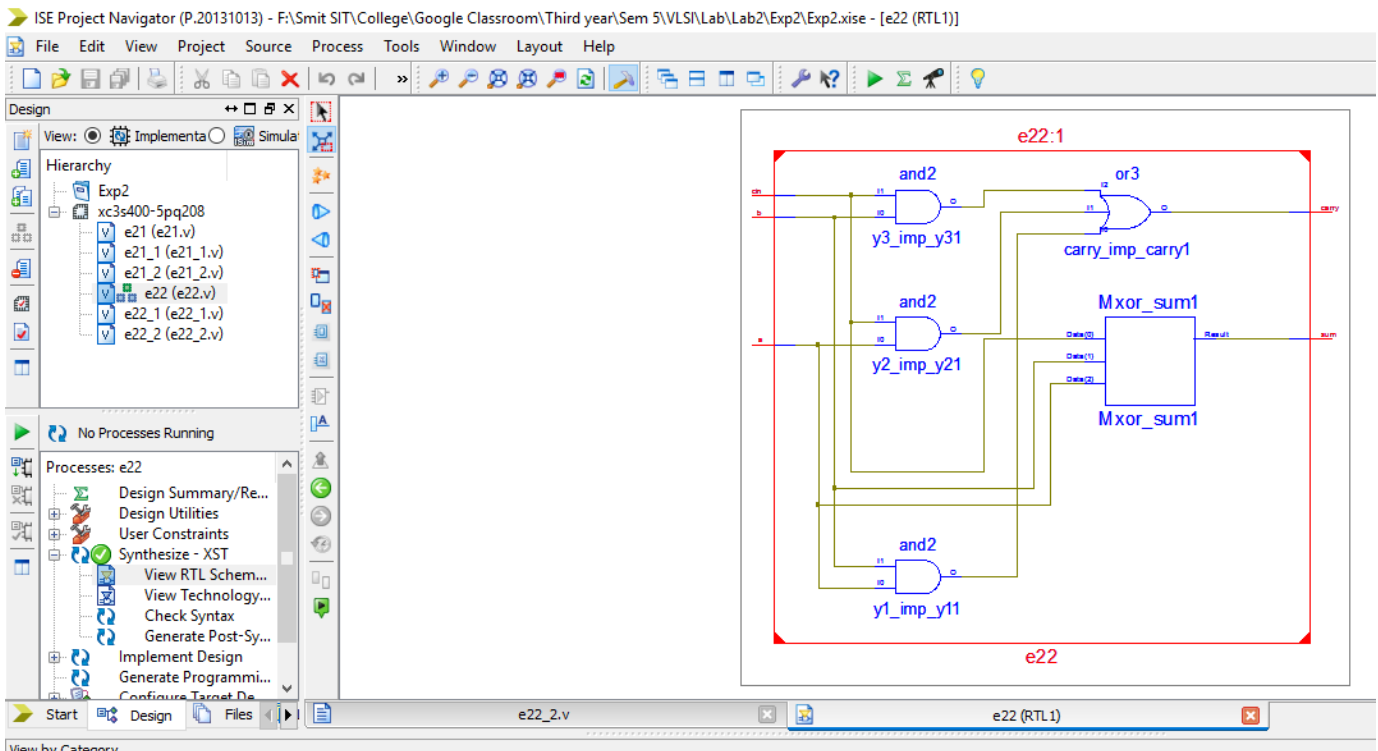
- Module Name:** e22_2
- Project Name:** Exp2
- Target Devices:** xc3s400-5pg208
- Tool versions:** e21 (e21.v), e21_1 (e21_1.v), e21_2 (e21_2.v), e22 (e22.v), e22_1 (e22_1.v), e22_2 (e22_2.v)
- Dependencies:**
- Revision:** Revision 0.01 - File Created
- Additional Comments:**
- Code:**

```
module e22_2(  
    input a,  
    input b,  
    input cin,  
    output sum,  
    output carry  
);  
assign sum= a^b^c;  
assign carry= (a*b)+(cin*(b+a));  
endmodule
```

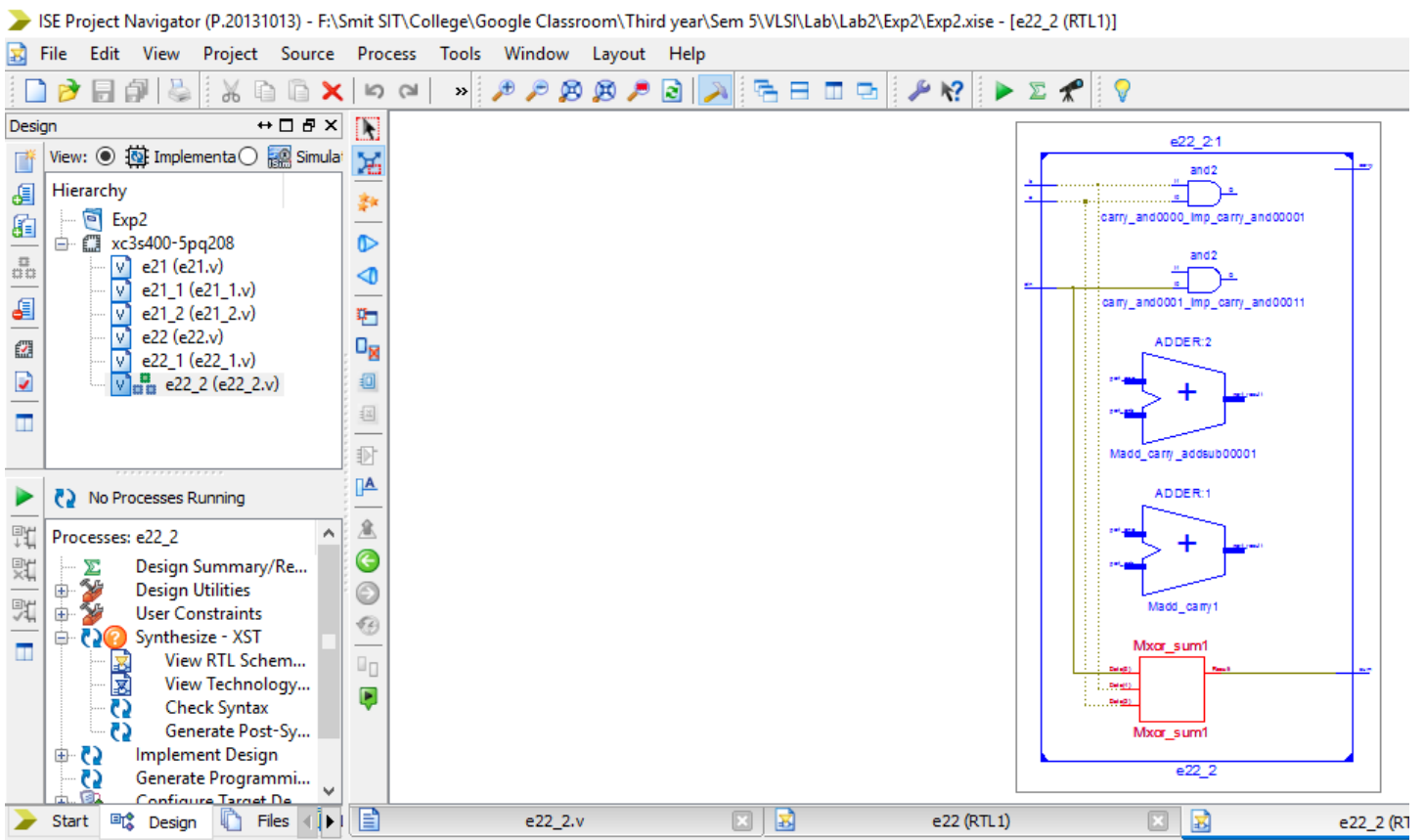
Right Window (Default.wcfg):

- Simulation Object:** e22_2
- Object Name:** e22_2
- Simulation Results:** A timing diagram showing the waveforms for inputs a, b, cin and outputs sum, carry, y1, y2, y3. The simulation time is 584,622,800 ps.

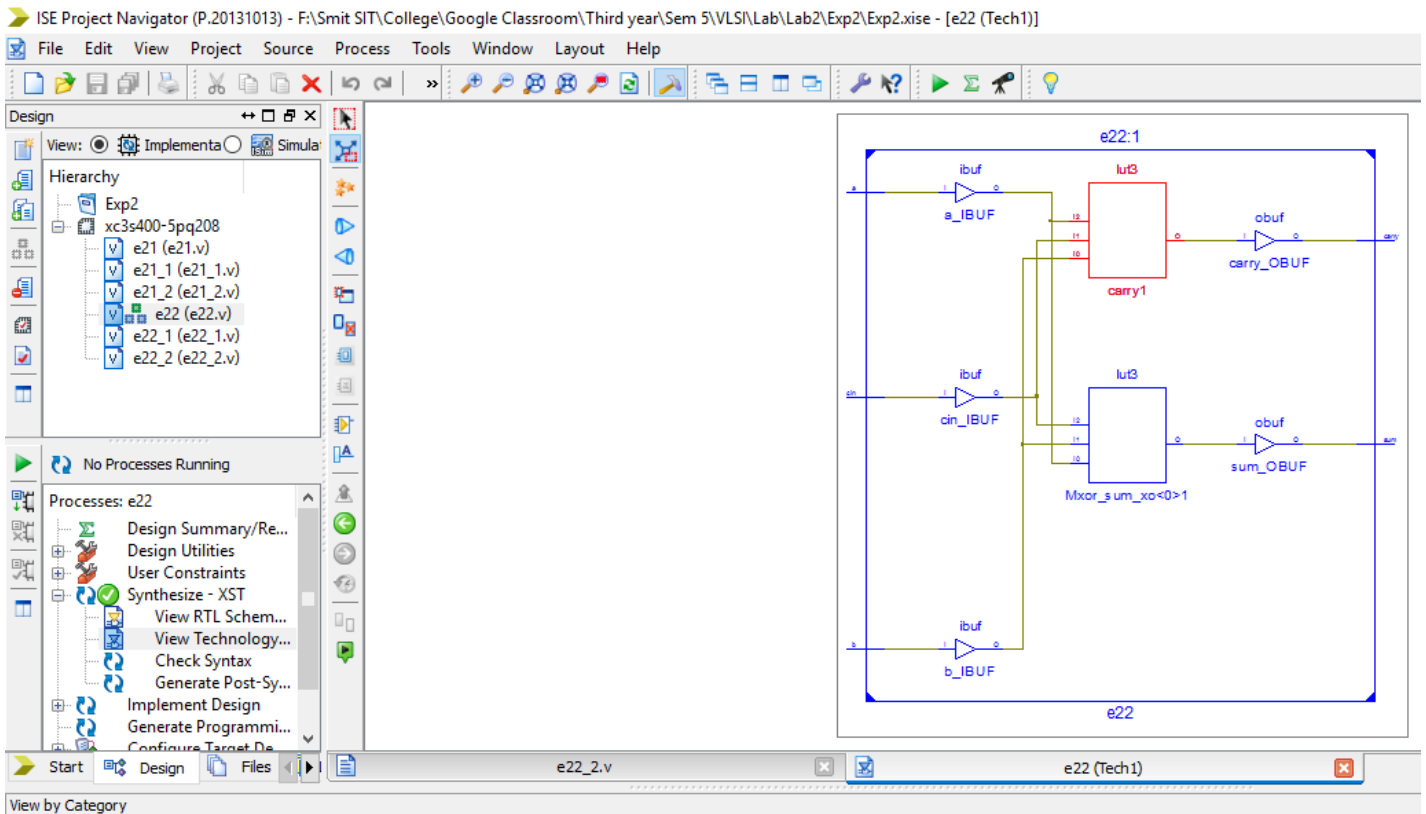
RTL Schematic without Arithmetic Operator



RTL Schematic with Arithmetic Operator



Technology Schematic without Arithmetic Operator



Technology Schematic with Arithmetic Operator

