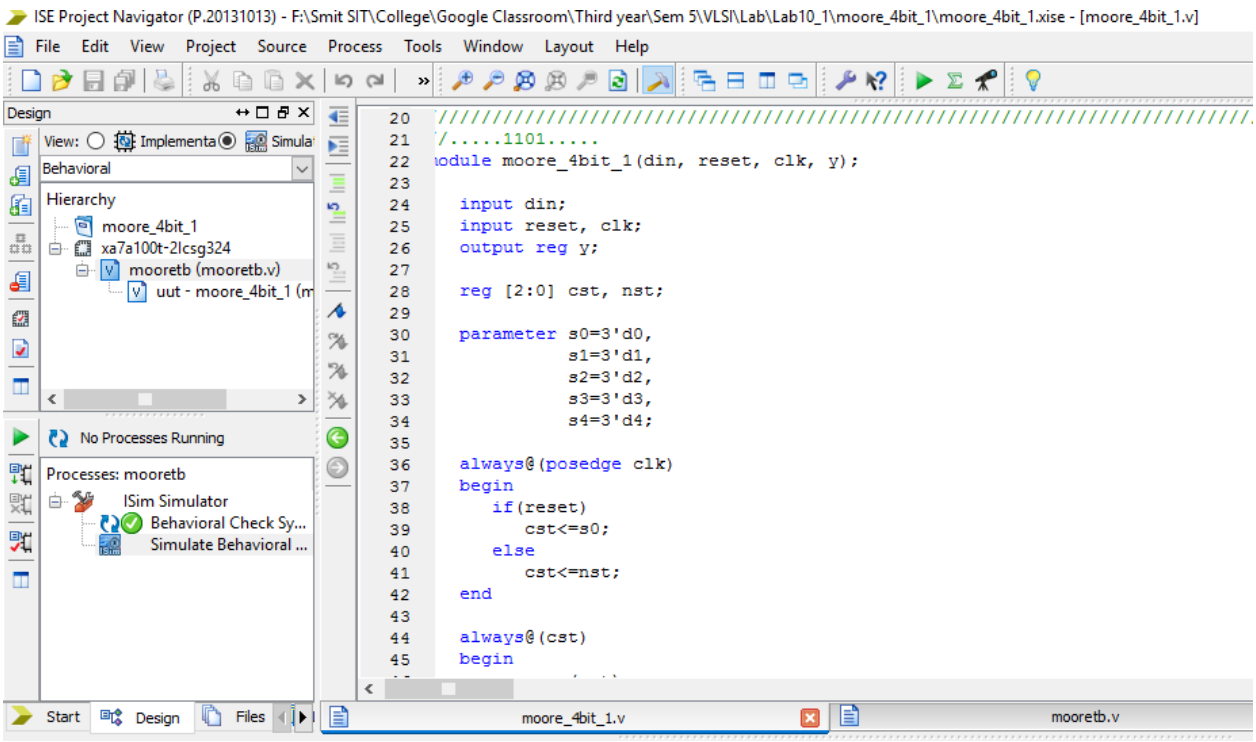
# Mealy State Machine

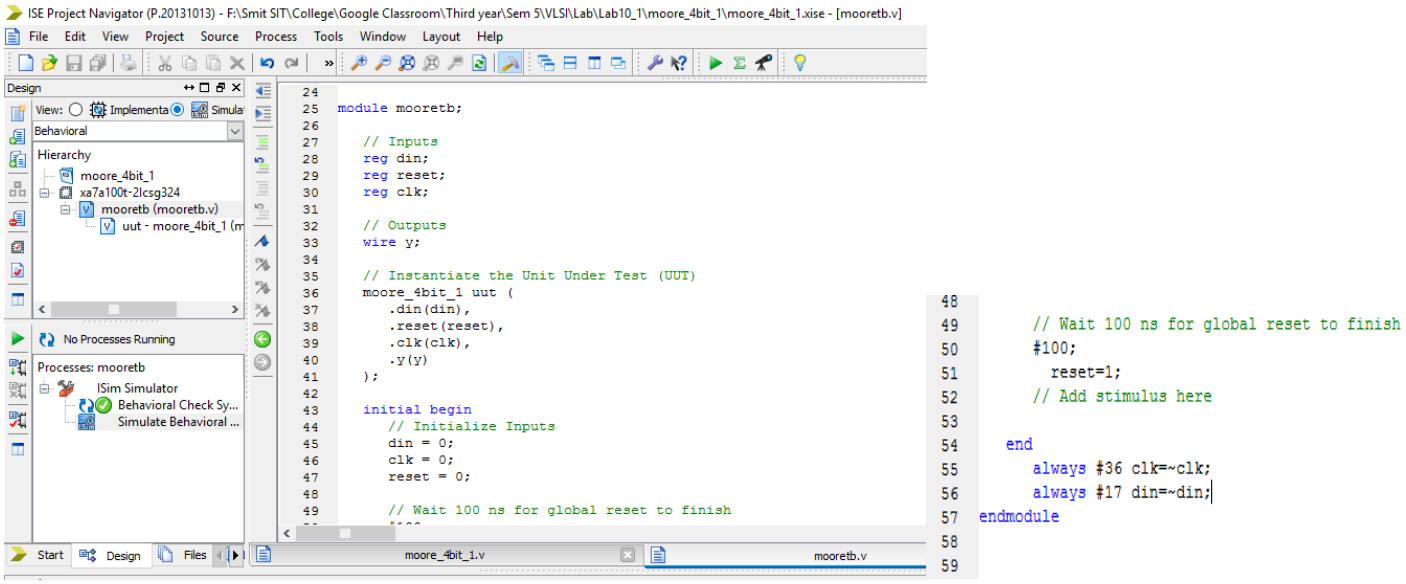
## Source Code, Test Bench And Output

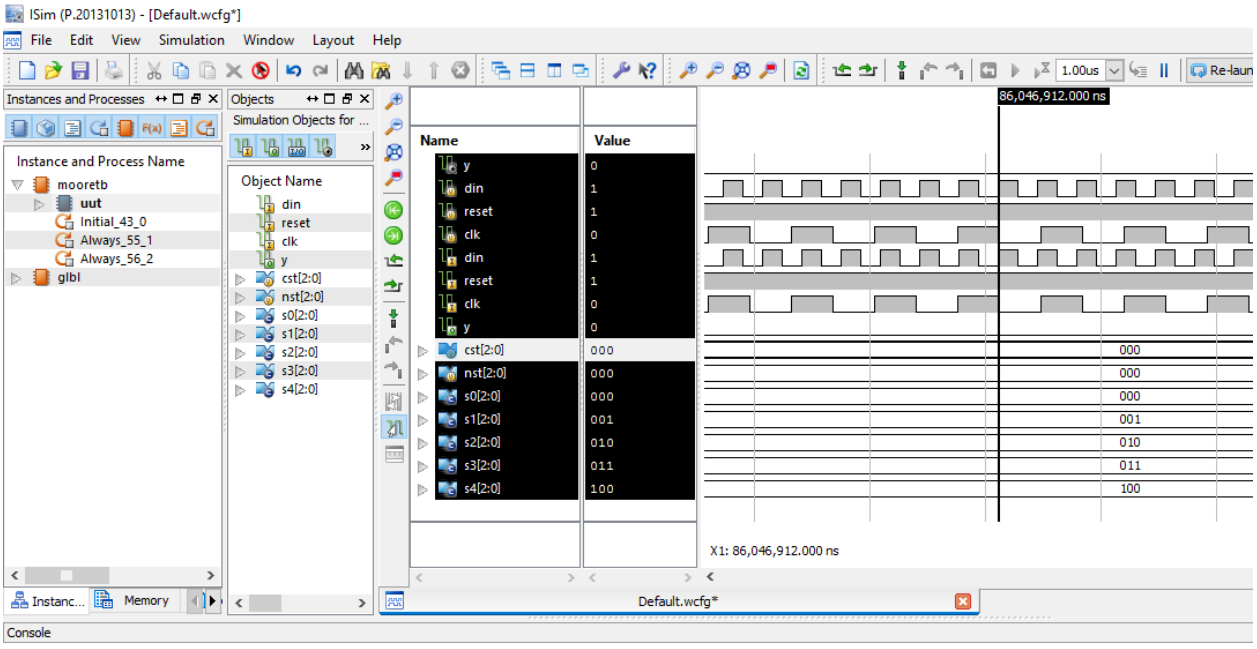



```
44  always@(cst)
45  begin
46        case(cst)
47           s0: if(din==1)
48                 nst=s1;
49              else
50                 nst=s0;
51           s1: if(din==1)
52                 nst=s2;
53              else
54                 nst=s0;
55           s2: if(din==1)
56                 nst=s2;
57              else
58                 nst=s3;
59           s3: if(din==1)
60                 nst=s4;
61              else
62                 nst=s0;
63           s4: if(din==1)
64                 nst=s2;
65              else
66                 nst=s0;
67        endcase
68  end
69
```

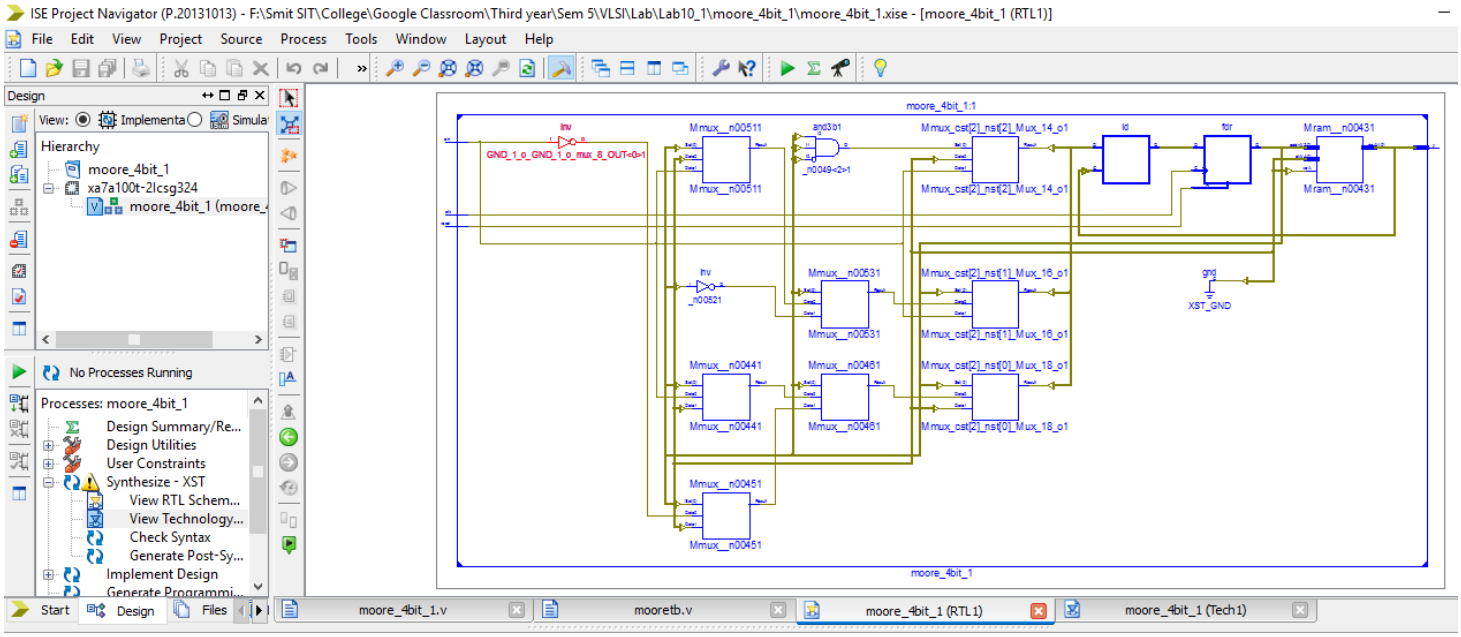
moore_4bit_1.v

```
69
70  always@(cst)
71  begin
72     case(cst)
73           s0: y=0;
74           s1: y=0;
75           s2: y=0;
76           s3: y=0;
77           s4: y=1;
78           default: y=0;
79     endcase
80  end
81 dmodule
82
```


ISE Project Navigator (P.20131013) - F:\Smit SIT\College\Google Classroom\Third year\Sem 5\VLSI\Lab\Lab10_1\moore_4bit_1\moore_4bit_1.xise - [mooretb.v]
File Edit View Project Source Process Tools Window Layout Help
Design
Hierarchy
moore_4bit_1
xa7a100t-2lcsg324
mooretb (mooretb.v)
uut - moore_4bit_1
No Processes Running
Processes: mooretb
ISim Simulator
Behavioral Check Sy...
Simulate Behavioral ...
Start Design Files
moore_4bit_1.v
mooretb.v
24 module mooretb;
25
26 // Inputs
27 reg din;
28 reg reset;
29 reg clk;
30
31 // Outputs
32 wire y;
33
34 // Instantiate the Unit Under Test (UUT)
35 moore_4bit_1 uut (
36 .din(din),
37 .reset(reset),
38 .clk(clk),
39 .y(y)
40 );
41
42 initial begin
43 // Initialize Inputs
44 din = 0;
45 clk = 0;
46 reset = 0;
47
48 // Wait 100 ns for global reset to finish
49 // Wait 100 ns for global reset to finish
50 #100;
51 reset=1;
52 // Add stimulus here
53
54 end
55 always #36 clk=~clk;
56 always #17 din=~din;
57 endmodule
58
59


ISim (P.20131013) - [Default.wcfg*]
File Edit View Simulation Window Layout Help
Instances and Processes
Instance and Process Name
mooretb
uut
Initial_43_0
Always_55_1
Always_56_2
glbl
Objects
Simulation Objects for ...
Object Name
din
reset
clk
y
cst[2:0]
nst[2:0]
s0[2:0]
s1[2:0]
s2[2:0]
s3[2:0]
s4[2:0]
Name
Value
y 0
din 1
reset 1
clk 0
din 1
reset 1
clk 0
y 0
cst[2:0] 000
nst[2:0] 000
s0[2:0] 000
s1[2:0] 001
s2[2:0] 010
s3[2:0] 011
s4[2:0] 100
86,046,912.000 ns
X1: 86,046,912.000 ns
Default.wcfg*
Console

# RTL Schematic




# Technology Schematic