

## 4:1 Multiplexer

### Source Code And Output

ISE Project Navigator (P.20131013) - F:\Smit SIT\College\Google Classroom\Third year\Sem 5\VLSI\Lab\Lab3\exp3\exp3.xise - [exp3\_1.v]

File Edit View Project Source Process Tools Window Layout Help

Design

View: Implementa Simula

Hierarchy

- exp3
- xa7a100t-2lcs324
- exp3 (exp3.v)
- exp3\_1 (exp3\_1.v)
- exp3\_2 (exp3\_2.v)

Running: Synthesis

Processes: exp3\_1

- Design Summary/Re...
- Design Utilities
- User Constraints
- Synthesize - XST
- View RTL Schem...
- View Technology...
- Check Syntax
- Generate Post-Sy...
- Implement Design
- Generate Programmi...
- Configure Target De...

```
5 //
6 // Create Date: 09:28:10 08/22/2019
7 // Design Name:
8 // Module Name: exp3_1
9 // Project Name:
10 // Target Devices:
11 // Tool versions:
12 // Description:
13 //
14 // Dependencies:
15 //
16 // Revision:
17 // Revision 0.01 - File Created
18 // Additional Comments:
19 //
20 ///////////////////////////////////////////////////
21 module exp3_1(
22     input s1,
23     input s0,
24     input i0,
25     input i1,
26     input i2,
27     input i3,
28     output y
29 );
30 assign y= ((~s1 & (~s0) & i0) | ((~s1) & (s0) & i1) | ((s1) & (~s0) & i2) | ((s1) & (s0) & i3);
31 endmodule
32
```

exp3\_1.v

Warnings

ISE Project Navigator (P.20131013) - F:\Smit SIT\College\Google Classroom\Third year\Sem 5\VLSI\Lab\Lab3\exp3\exp3.xise - [exp3\_2.v]

File Edit View Project Source Process Tools Window Layout Help

Design

View: Implementa Simula

Hierarchy

- exp3
- xa7a100t-2lcs324
- exp3 (exp3.v)
- exp3\_1 (exp3\_1.v)
- exp3\_2 (exp3\_2.v)

No Processes Running

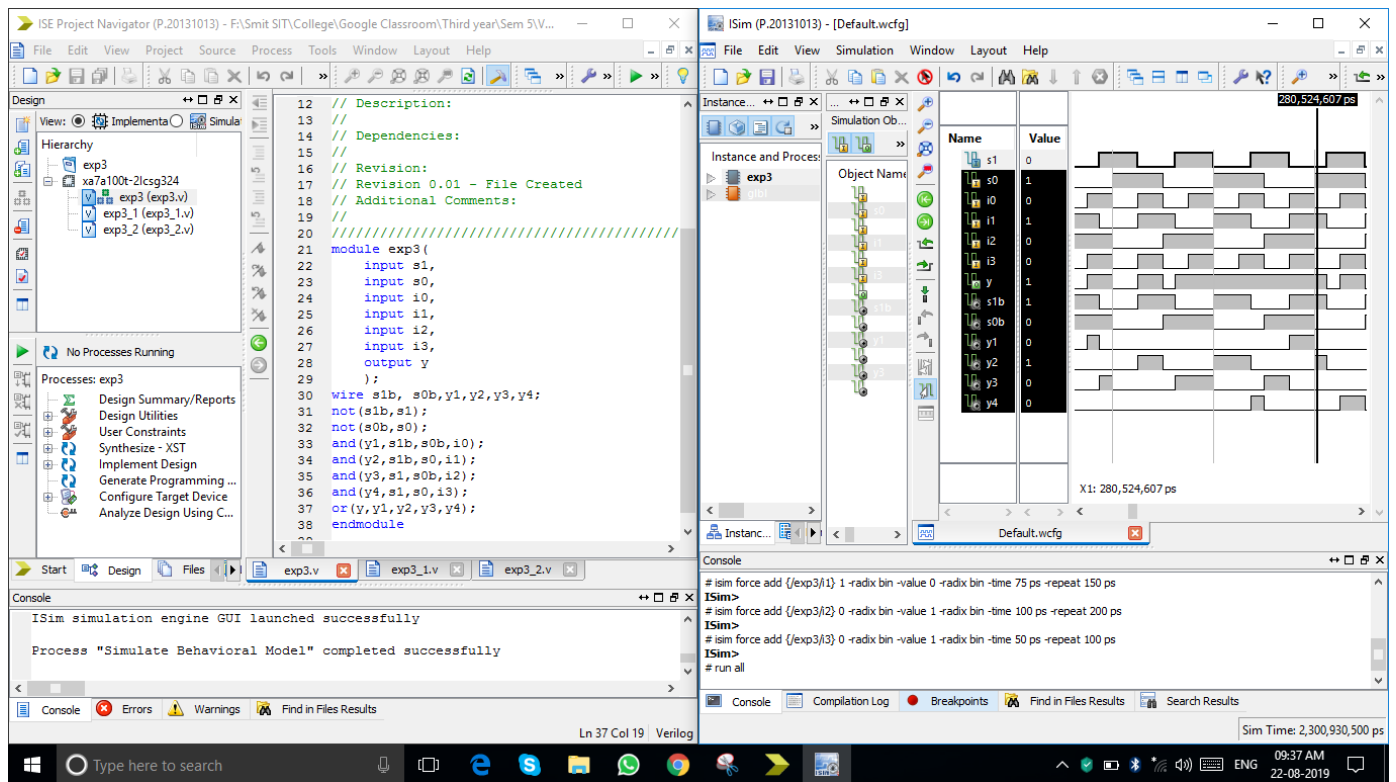
Processes: exp3

- Design Summary/Reports
- Design Utilities
- User Constraints
- Synthesize - XST
- Implement Design
- Generate Programming ...
- Configure Target Device
- Analyze Design Using C...

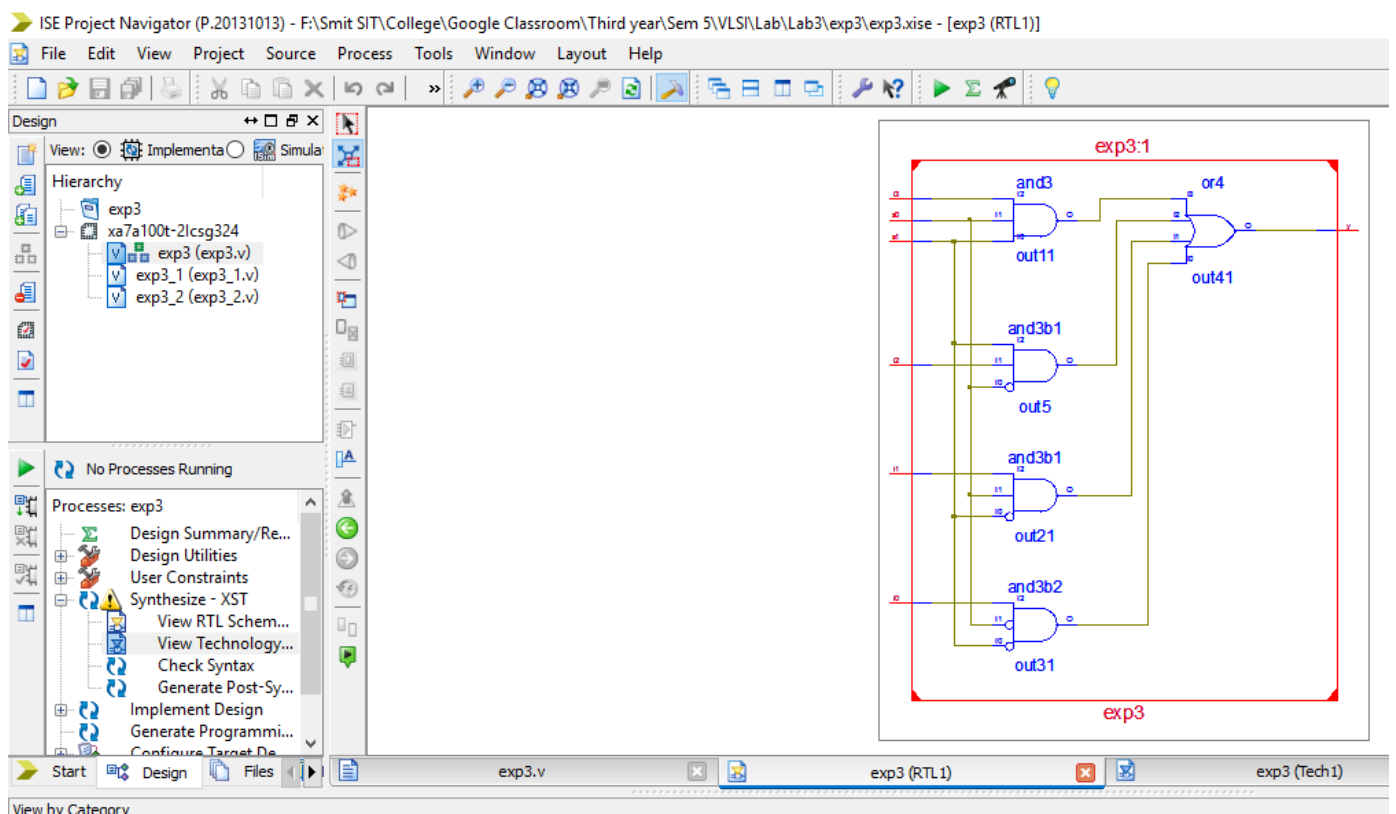
```
5 //
6 // Create Date: 09:30:51 08/22/2019
7 // Design Name:
8 // Module Name: exp3_2
9 // Project Name:
10 // Target Devices:
11 // Tool versions:
12 // Description:
13 //
14 // Dependencies:
15 //
16 // Revision:
17 // Revision 0.01 - File Created
18 // Additional Comments:
19 //
20 ///////////////////////////////////////////////////
21 module exp3_2(
22     input s1,
23     input s0,
24     input i0,
25     input i1,
26     input i2,
27     input i3,
28     output y
29 );
30 assign y= s0?(s1?i3:i1):(s1?i2:i0);
31 endmodule
32
```

exp3.v exp3\_1.v exp3\_2.v

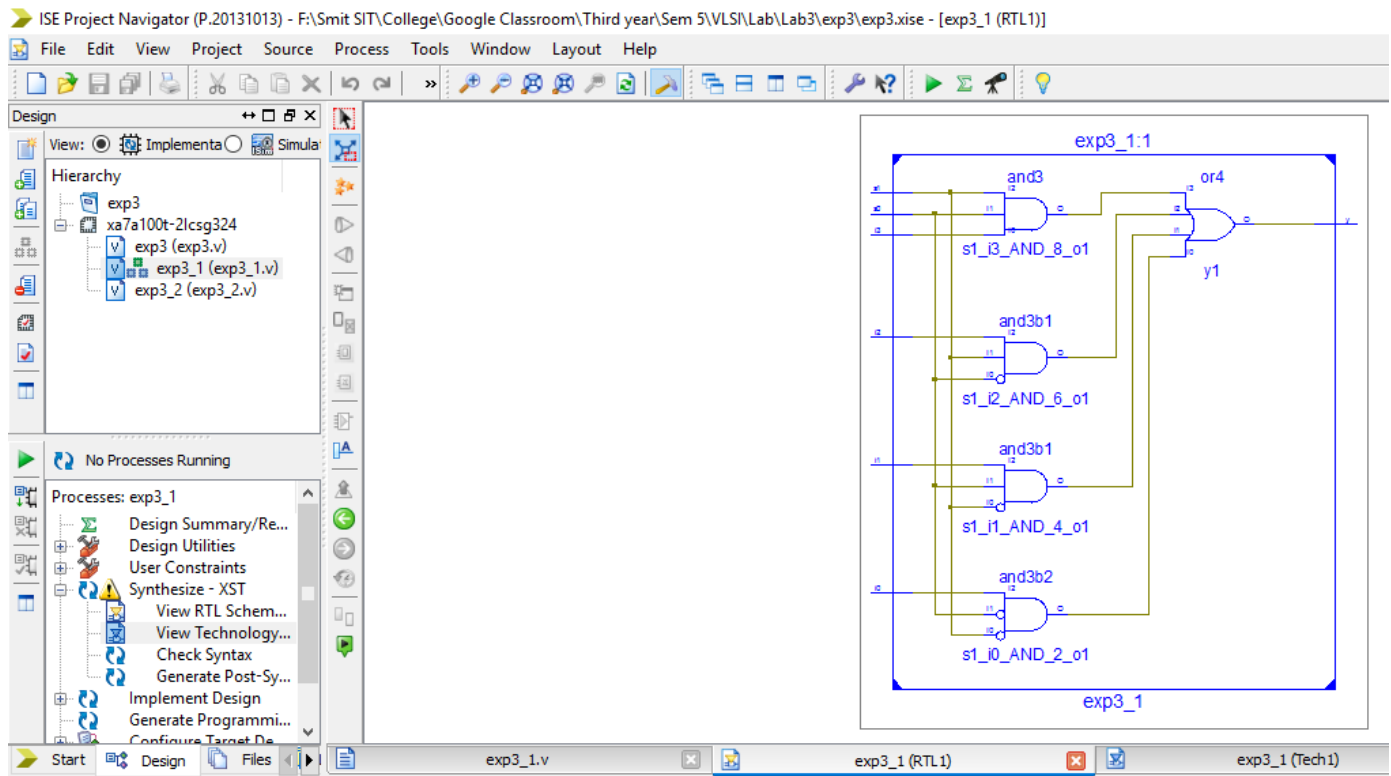
Console



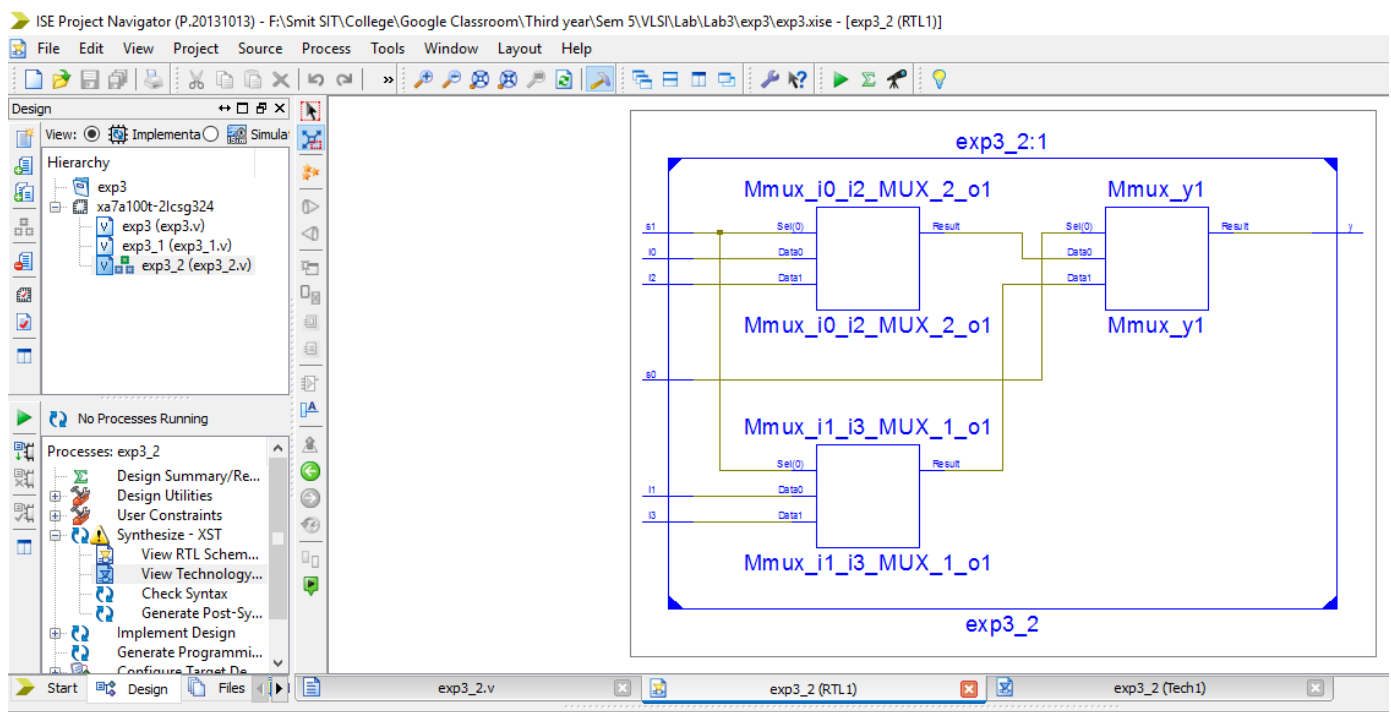
## RTL Schematic with Gate Level Modelling



# RTL Schematic with Data Flow Modelling



# RTL Schematic with Assignment Operator



# Technology Schematic

