[컴퓨터구조] Homework 6

국방정보공학과 2학년 2020032206 송민경

Chap 13.

13.1) a. 20 b. 40 c. 60 d. 30 e. 50 f. 70

13.3) a. the address field
b. memory location 14
c. the memory location whose address is in memory location 14.
d. register 14.
e. memory location whose address is in register 14

13.4)

	EA	operand		EA	Operand
a.	500	1100	e.	600	1200
b.	201	500	f.	R1	400
c.	1100	1700	g.	400	1000
d.	702	1302	h.	400	1000

13.7) a. 3 times / fetch instruction, fetch operand reference, fetch operand
b. 2 times / fetch instruction, fetch operand reference and load into PC.

Chap 14.

14.1) a.

```
 00000010
 00000011
 --------
 00000101
```

Carry = 0, Zero = 0, Overflow = 0, Sign = 0,
Even parity = 1, Half-carry = 0

b.

```
  11111111
  00000001
 ---------
 100000000
```

Carry = 1, Zero = 1, overflow = 1, sign = 0
Even parity = 1, Half-carry = 1

14.2) To perform A-B, the ALU takes the twos complement of B

$A: 11110000$

$\overline{B}+1: 11101100$

11011100

Carry = 1, Zero = 0, overflow = 0, sign = 1
Even parity = 0, Half-carry = 0.

14.3) a. 0.2ns b. 0.6ns

14.4) a. The length of a clock cycle is 0.1ns. The length of the instruction cycle for this case is $(10+(15\times64))\times0.1 = 960$ns.

b. The worst-case delay is when the instruction occurs just after the start of the instruction, which is 960 ns.

c. In this case, the instruction can be interrupted after the instruction fetch, which takes 10 clock cycles, so the delay is 1ns. The instruction can be interrupted between byte transfers, which results in a delay of more than 15 clock cycles = 1.5ns. ∴ The worst-delay is 1.5ns.

14.5) a. A factor of 2.

b. A factor of 1.5

14.7)

Time →

	1	2	3	4	5
instruction 1	F	E			
instruction 2		F	E		
instruction 3			F	E	
instruction 4				F	E

14.8)

	1	2	3	4	5	6	7	8	9	10
I1	FI	DA	FO	EX						
I2		FI	DA	FO	EX					
I3			FI	DA	FO	EX				
I4				FI	DA	FO				
I5					FI	DA				
I6						FI				
I15							FI	DA	FO	EX

14.9) a. We can ignore the initial filling up of the pipe line and the final emptying of the pipeline, because this involves only a few instructions out of 1.5 million instructions. ∴ The speed up is a factor of 5.

b. One instruction is completed per clock cycle, for an throughput of 2500 MIPS.

14.11) The number of instructions causing branches to take place is pqn, and the number that do not cause branch is $(1-pq)n$.

We can replace equation (12.1) with:

$$T_k = pqnk\tau + (1-pq)[k+(n-1)]\tau$$

Equation (12.2) becomes

$$S_k = \frac{T_1}{T_k} = \frac{nk\tau}{(pq)nk\tau + (1-pq)[k+(n-1)]\tau} = \frac{nk}{(pq)nk + (1-pq)[k+(n-1)]}$$

ibis