[컴퓨터 구조] Homework 2

국방정보공학과 2학년 20200322306 심민경

Chap 3.

Review questions

3.1) The processor interprets the instruction and performs the required action. In general, these actions fall into 4 categories.

① Processor – memory : Data may be transferred from processor to memory or from memory to processor.

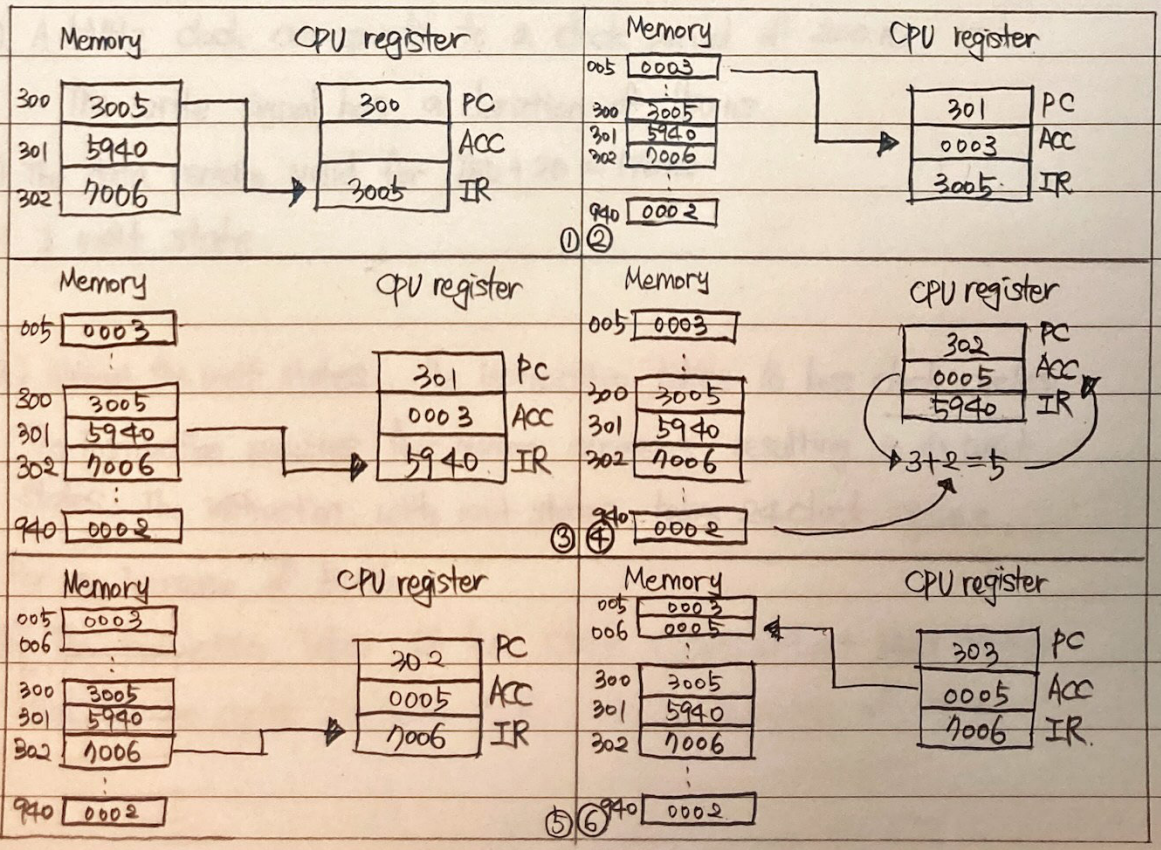
② Processor – I/O : Data may be transferred to or from a peripheral device by transferring between the processor and an I/O module.

③ Data processing : The processor may perform some arithmetic or logic operation on data.

④ Control : An instruction may specify that the sequence of execution be altered.

Problems

3.1)



3.3) (a) 2^{24} = 16 MBytes

(b) (1) If the local address bus is 32 bits, the whole address can be transferred at once and decoded in memory. However, because the data bus is only 16 bits, it will require 2 cycles to fetch a 32-bit instruction or operand.

(2) The 16 bits of the address placed on the address bus can't access the whole memory. Thus a more complex memory interface control is needed. In addition to the two-step address operation, it will need 2 cycles to fetch the 32-bit instruction or operand.

(c) PC : At least 24 bits
IR : 32 bits (whole), 8 bits (only the op code)

3.4) (a) 2^{16} = 64K bytes (each access transfers a byte)

(b) 2^{16} = 64K bytes (each access transfers a byte or a 16-byte word)

3.13) (a) A 5MHz clock corresponds to a clock period of 200 ns.
∴ The write signal has a duration of 150 ns.

(b) The data remain valid for 150+20 = 170 ns

(c) 1 wait state.

3.14) (a) Without the wait states, the instruction takes 16 bus clock cycles. The instruction requires four memory accesses, resulting in 8 wait states. The instruction, with wait states, takes 24 clock cycles, for an increase of 50%

(b) The instruction takes 26 bus clock cycles without wait states and 34 bus cycles with wait states, for an increase of 31%

3.15) (a) The clock period is 125ns.

One bus read cycle takes 500ns = 0.5μs.

If the Bus cycles repeat one to another, we can achieve a data transfer rate of 2MB/s.

(b) 125ns × 5 = 0.625μs

The corresponding data transfer rate is $\frac{1}{0.625}$ = 1.6MB/s