[컴퓨터 구조] Home work 5

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Chap 7.

Review questions

7.2) The International Reference Alphabet (IRA) is the most commonly used text code, in which each character is represented by a unique 7-bit binary code. 128 different characters can be represented.

7.3) Control timing / Processor communication / Device communication / Data buffering / Error detection

7.4) ① Programmed I/O : The processor issues an I/O command, on behalf of a process, to an I/O module that process then busy-waits for the operation to be completed before proceeding.

② Interrupt-driven I/O : The processor issues an I/O command on behalf of a process, continues to execute subsequent instructions, and is interrupted by the I/O module when the latter has completed its work.

③ Direct memory access (DMA) : A DMA module controls the exchange of data between main memory and an I/O module.

7.5) ① memory-mapped I/O : There is a single address space for memory locations and I/O devices. The processor treats the status and data registers of I/O modules as memory locations and uses the same machine instructions to access both memory and I/O devices.

② Isolated I/O : A command specifies whether the address refers to a memory location or an I/O device. The full range of addresses may be available for both.

Problems

7.1) In the first addressing mode, $2^8 = 256$ ports can be addressed. Typically, this would allow 128 devices to be addressed. However, an opcode specifies either an input or output operation, so it is possible to reuse the addresses, so that there are 256 input port addresses and 256 output port addresses. In the second addressing mode, $2^{16} = 64K$ port addresses are possible.

7.3) 64KB can be transferred.

7.6) a. The printing rate is slowed to 5 cps.

b. The situation must be treated differently with input devices such as the keyboard. It is necessary to scan the buffer at a rate of a least once per 60 ms.

7.9) a. The processor scans the keyboard 10 times per second. In 8 hours, the number of times the keyboard is scanned is $10 \times 60 \times 60 \times 8 = 288000$.

b. Only 60 visits would be required. The reduction is $1 - (60/288000) = 0.999 = 99.9\%$

7.11) a. The device generates 8000 interrupts per second or a rate of one every 125 μs. If each interrupt consumes 100 μs, then the fraction of processor time consumed is $100/125 = 0.8$.

b. In this case, the time interval between interrupts is $16 \times 125 = 2000\ \mu s$. Each interrupt now requires $100\ \mu s$ for the first character plus the time for transferring each remaining character, which adds up to $8 \times 15 = 120\ \mu s$, for a total of $220\ \mu s$. The fraction of processor time consumed is $220/2000 = 0.11$.

c. The time per byte has been reduced by $6\ \mu s$, so the total time reduction is $16 \times 6 = 96\ \mu s$. The fraction of processor time consumed is $(220-96)/2000 = 0.062$.

Chap 8.

Review questions

8.7) No, if virtual memory is used.

8.8) No.

Problems

8.6) a. Split binary address into virtual page number and offset; use VPN as index into page table; extract page frame number; concatenate offset to get physical memory address.

b. (i) $1052 = 1024 + 28$ maps to VPN 1 in PFN 7. $(7 \times 1024 + 28 = 2196)$

(ii) $2221 = 2 \times 1024 + 173$ maps to VPN 2, page fault

(iii) $5499 = 5 \times 1024 + 379$ maps to VPN 5 in PFN 0. $(0 \times 1024 + 379 = 379)$

8.8) 9 and 10 page transfers, respectively.

8.9) A total fifteen pages are referenced, the hit ratio are:

N	1	2	3	4	5	6	7	8
Ratio	0/15	0/15	2/15	3/15	5/15	8/15	8/15	8/15