Profetcher

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Problem:

Hardware prefetchers and cache management policies are two of the most successful ways to hide high memory latency. But most state-of-the art prefetchers and cache management policies work independently and do not take care of the interaction between them.

State-of-the-art:

[1] Wu, Carole-Jean, Aamer Jaleel, Margaret Martonosi, Simon C. Steely Jr, and Joel Emer. **"PACMan: prefetch-aware cache management for high performance caching."** In *Proceedings of the 44th Annual IEEE/ACM International Symposium on Microarchitecture*, pp. 442-453. 2011.
Link: https://people.csail.mit.edu/emer/papers/2011.12.micro.pacman.pdf

[2] Jain, Akanksha, and Calvin Lin. **"Rethinking belady's algorithm to accommodate prefetching."** In *2018 ACM/IEEE 45th Annual International Symposium on Computer Architecture (ISCA)*, pp. 110-123. IEEE, 2018.
Link: https://www.cs.utexas.edu/~lin/papers/isca18.pdf

[3] Kim, Jinchun, Elvira Teran, Paul V. Gratz, Daniel A. Jiménez, Seth H. Pugsley, and Chris Wilkerson. **"Kill the program counter: Reconstructing program behavior in the processor cache hierarchy."** *ACM SIGPLAN Notices* 52, no. 4 (2017): 737-749.
Link: https://dl.acm.org/doi/pdf/10.1145/3037697.3037701

Tentative project proposal:

Feb end: To design and implement a mechanism to quantify the interaction between prefetchers and cache management policies. To estimate the approximate performance improvement in case of an ideal environment where negative interactions between the prefetchers and cache management policies are minimized to the extent possible.

March end: To design and experiment with ideas to minimize/remove the negative interactions across the cache hierarchy agnostic of the prefetch and management policy used.

April end: To implement and fine-tune the ideas that show the most performance improvement. To extend the design to be compatible with multicore execution environment.