Exam 1 CECS 341 (Chapters 1&2)

Last Name: _____ Student ID: _____ .

(*Turn in both exam paper and scantrons*)

MIPS assembly language

Category	Instruction	Example	Meaning	Comments
Arithmetic	add	add $s1,$s2,$s3	$s1 = $s2 + $s3	Three register operands
	subtract	sub $s1,$s2,$s3	$s1 = $s2 – $s3	Three register operands
	add immediate	addi $s1,$s2,100	$s1 = $s2 + 100	Used to add constants
Data transfer	load word	lw $s1,100($s2)	$s1 = Memory[$s2 + 100]	Word from memory to register
	store word	sw $s1,100($s2)	Memory[$s2 + 100] = $s1	Word from register to memory
	load half	lh $s1,100($s2)	$s1 = Memory[$s2 + 100]	Halfword memory to register
	store half	sh $s1,100($s2)	Memory[$s2 + 100] = $s1	Halfword register to memory
	load byte	lb $s1,100($s2)	$s1 = Memory[$s2 + 100]	Byte from memory to register
	store byte	sb $s1,100($s2)	Memory[$s2 + 100] = $s1	Byte from register to memory
	load upper immed.	lui $s1,100	$s1 = 100 * 2^{16}	Loads constant in upper 16 bits
Logical	and	and $s1,$s2,$s3	$s1 = $s2 & $s3	Three reg. operands; bit-by-bit AND
	or	or $s1,$s2,$s3	$s1 = $s2 | $s3	Three reg. operands; bit-by-bit OR
	nor	nor $s1,$s2,$s3	$s1 = ~ ($s2 |$s3)	Three reg. operands; bit-by-bit NOR
	and immediate	andi $s1,$s2,100	$s1 = $s2 & 100	Bit-by-bit AND reg with constant
	or immediate	ori $s1,$s2,100	$s1 = $s2 | 100	Bit-by-bit OR reg with constant
	shift left logical	sll $s1,$s2,10	$s1 = $s2 << 10	Shift left by constant
	shift right logical	srl $s1,$s2,10	$s1 = $s2 >> 10	Shift right by constant
Conditional branch	branch on equal	beq $s1,$s2,25	if ($s1 == $s2) go to PC + 4 + 100	Equal test; PC-relative branch
	branch on not equal	bne $s1,$s2,25	if ($s1 != $s2) go to PC + 4 + 100	Not equal test; PC-relative
	set on less than	slt $s1,$s2,$s3	if ($s2 < $s3) $s1 = 1; else $s1 = 0	Compare less than; for beq, bne
	set less than immediate	slti $s1,$s2,100	if ($s2 < 100) $s1 = 1; else $s1 = 0	Compare less than constant
Uncondi-tional jump	jump	j 2500	go to 10000	Jump to target address
	jump register	jr $ra	go to $ra	For switch, procedure return
	jump and link	jal 2500	$ra = PC + 4; go to 10000	For procedure call

1. A computer in an Amazon building accessed by thousands of people for online shopping.
   a. Embedded
   b. Server
   c. PC

2. A terabyte is one _____ bytes.
   a. Thousand
   b. Million
   c. Billion
   d. Trillion

3. The collection of software on a computer that provides services to application software.
   a. System software
   b. Application software
   c. Compiler

4. The ISA includes anything programmers need to know to make a binary machine language program work correctly, including instructions, I/O devices, and so on.
   a. True
   b. False

5. "Bit" is short for "binary digit."
   a. True
   b. False

6. Computers use binary because binary is more powerful than decimal numbers.
   a. True
   b. False

7. Operating system and compiler are central to every computer system.
    a. True
    b. False

8. Although binary's alphabet contains only two "letters", 0 and 1, the binary alphabet can represent as much information as the English alphabet's 26 letters.
    a. True
    b. False

9. The number 12 can be represented in binary as 1100. If a computer's memory location contains 00001100, then that location contains the number 12.
    a. True
    b. False

10. The corresponding binary representation of number 5C in hexadecimal is __.
    a. 10101110
    b. 01011101
    c. 01011100
    d. 10111100

11. An advantage of a high-level language (HLL) is allowing a programmer to _____.
    a. Think more naturally
    b. Think like a machine

12. The following could be an assembly language instruction: 1000110010100000.
    a. True
    b. False

13. Computer A requires 10 seconds to compress a file. Computer B requires 5 seconds. Which computer ha the higher performance?
    a. A
    b. B

14. Computer A: 2GHz, 10s CPU time. In order to design a computer B with 6s CPU time and 2.4 times clock cycles (CPI) of computer A assuming both use the same amount of instruction count, how fast must computer B clock be?
    a. 2 GHz
    b. 4 GHz
    c. 6 GHz
    d. 8 GHz
    e. None of above

15. To determine how many times faster Computer C is than Computer D, which is the correct calculation?
    a. PerfC / PerfD
    b. PerfD / PerfC

16. A given application written in Java runs 15 seconds on a desktop processor. A new Java compiler is released that requires only 0.6 as many instructions as the old compiler. Unfortunately, it increases the CPI by 1.1. How fast can we expect the application to run using this new compiler?
    a. 15x 0.6 /1.1 = 8.2 sec

b. 15 x 0.6 x 1.1 = 9.9 sec
c. 15 x 1.1 / 0.6 = 27.5 sec

17. Replacing a processor in a computer with a faster processor has what effect?
    a. Decreases response time
    b. Increases throughput
    c. Both (decreases response time and increases throughput)

18. As clock rates increased in early Intel processors, power _____.
    a. Increased
    b. Decreased

19. Which improvement has a bigger impact on power?
    a. 25% reduction in voltage
    b. 25% reduction in frequency switching

20. Instructions, as well as data, can be stored in memory as numbers.
    a. True
    b. False

21. Multiple operations are allowed per MIPS instruction.
    a. True
    b. False

22. The alignment restriction refers to that words must start at addresses that are multiple of 4 in MIPS.
    a. True
    b. False

23. Since registers are faster to access than memory, the compiler should keep all used variables in registers.
    a. True
    b. False

24. rt is always referred as the second source register for MIPS instruction.
    a. True
    b. False

25. Indicate whether name $t9 refers to a MIPS register.
    a. True
    b. False

26. Indicate whether name $one refers to a MIPS register.
    a. True
    b. False

27. Indicate whether name Memory[0] refers to a MIPS register.
    a. True
    b. False

28. Indicate whether addi $s1, $s3, 50 is a valid MIPS instruction.
    a. True

b. False

29. Indicate whether lw $s1, 20($s8) is a valid MIPS instruction.
    a. True
    b. False

30. More registers may benefit an assembly program, but may directly lead to a _____ clock frequency.
    a. Faster
    b. Same
    c. Slower
    d. Broken

    Assume $s3 has 5000, and words addressed 5000..5002 have the data shown:
    5000: 99
    5001: 77
    5002: 323

31. What address will be computed by lw $t0, 2($s3):
    a. 5000
    b. 5001
    c. 5002

    Assume $s3 has 5000, and words addressed 5000..5002 have the data shown:
    5000: 99
    5001: 77
    5002: 323

32. Assume $s2 has 5001. What value will be put in $t2 by lw $t2, 1($s2)?
    a. 323
    b. 99
    c. 77
    d. 88

33. Consider the 32-bit binary number 11100000 11000000 00000000 00000001, stored in the word with address 5000. For a big-endian architecture, what value is stored in byte 5003?
    a. 11100000
    b. 00000000
    c. 00000001
    d. 11000000

34. Consider the 32-bit binary number 11100000 11000000 00000000 00000001, stored in the word with address 5000. For a big-endian architecture, what value is stored in byte 5001?
    a. 11100000
    b. 00000000
    c. 00000001
    d. 11000000

35. Consider the 32-bit binary number 11100000 11000000 00000000 00000001, stored in the word with address 5000. For a little-endian architecture, what value is stored in byte 5001?
    a. 11100000

b. 00000000
c. 00000001
d. 11000000

36. If $s3 has 900, $t0 has 77, and memory locations 900, 904, and 908 have 10, 15, 20 respectively, what does location 904 have after the following instruction?
sw $t0, 8($s3)

a. 10
b. 15
c. 20
d. 77

37. Given the following 32-bit number, what is the most significant bit's value?
1000 0000 0000 0000 0000 0000 0000 0000
a. 0
b. 1

38. In two's complement, is the following number positive or negative?
1111 0000 0000 0000 0000 0000 0000 0000
a. Positive
b. Negative

39. Knowing that 2^{31} is 2,147,483,648, what is the base ten value of the following two's complement number?
1000 0000 0000 0000 0000 0000 0000 0000
a. 0
b. -1
c. 1
d. 2,147,483,648
e. -2,147,483,648

40. Indicate if the binary operation (two's complement representation) resulted in overflow.

```
  0111 0000 0000 0000 0000 0000 0000 0000
+ 1111 0000 0000 0000 0000 0000 0000 0000
```

a. Overflow
b. No overflow

41. For both add and addi instructions, field 3 (rt) represents a register.
a. True
b. False

42. Opcode 0 and a funct field of 34 indicates a(n) _____ instruction.
a. Add immediate
b. Add
c. Sub
d. Logic AND

43. For the MIPS instruction lw $t0, 32($s3) assuming the opcode for lw is 35, the correspond machine code represented in Hexadecimal is _____ .
    a. 6E5A0020
    b. 4E680020
    c. 8E680020
    d. None of above

0000 0000 0000 0000 0000 1101 1100 0000
0000 0000 0000 0000 0011 1100 0000 0000

add $t0, $s1, $s2

44. For above add instruction, what is the corresponding output in HEX for the above two given source operands?
    a. 00002B00
    b. 02324020
    c. 000049C0
    d. None of above

op	rs	rt	rd	shamt	funct
0	8	9	10	0	34

45. What MIPS instruction does above represent?
    a. Sub $t0, $t1, $t2
    b. Add $t2, $t0, $t1
    c. Sub $t2, $t1, $t0
    d. Sub $t2, $t0, $t1
    e. None of above

46. For the MIPS instruction sw $t0, 1200($t1) assuming the opcode for sw is 43, the correspond machine code represented in Hexadecimal is _____ .
    a. AD5800B0
    b. AD2804B0
    c. 8E680020

sll $t2, $s0, 4

47. What is the register number of rs for the above MIPS instruction?
    a. 00000
    b. 10000
    c. 01010
    d. 00100

sll $t2, $s0, 4

48. What is the register number of rt for the above MIPS instruction?
    a. 00000
    b. 10000
    c. 01010
    d. 00100
    e. None of above

sll $t2, $s0, 4

49. What is the register number of rd for the above MIPS instruction?
    a. 00000
    b. 10000
    c. 01010
    d. 00100
    e. None of above

50. $a0-$a3, $v0, $v1, and $t0-$t9 are the only registers used by the compiler to handle procedure calling.
    a. True
    b. False

51. What is the binary representation for a 16 bit negative 21?
    a. 0000 0000 0001 0101
    b. 1111 1111 1110 1010
    c. 0000 0000 0000 1011
    d. 1111 1111 1110 1011
    e. None of above

52. What is the value of the register $t0 after executing the instruction slt $t0, $s0, $s1 when $s0 = 1101 and $s1 = 0010?
    a. 0
    b. 1
    c. -1
    d. None of above

53. What is the value of the register $t0 after executing the instruction sltu $t0, $s0, $s1 when $s0 = 1101 and $s1 = 0010?
    a. 0
    b. 1
    c. -1
    d. None of above

54. What is the value of the register $t1 after executing the instruction sll $t1, $s3, 2 when $s3 = 1101 0011 1101 0000 0111 1100 1000 0011 for above MIPS codes?
    a. D3D07C83
    b. 43D07C8C
    c. 4F41F20C
    d. None of above

55. What is the corresponding machine code in HEX for the shift left logic instruction sll $t1, $s3, 2 MIPS codes?
    a. 00134261
    b. 00134880
    c. 00134AB1
    d. None of above

opcode: 000000 (6 bits)
rs: 00000 (5 bits); rs is ALWAYS 0 for SHIFT INSTRUCTIONS
rt ($s3): 10011 (5 bits)
rd($t1): 01001 (5 bits)
shamt (shift amount 2): 00010 (5 bits)
funct: 000000 (6 bits)

000000 00000 10011 01001 00010 000000

Assume $s1 has 50 and $s2 has 30. Given this code:

```
bne $s3, $s4, Else
add $s0, $s1, $s2
j Exit
```

Else: sub $s0, $s1, $s2
Exit:

56. If $s3 is 9 and $s4 is 9, which instruction executes after bne?
    a. Add
    b. Sub
    c. J
    d. Else
    e. Exit

57. j Exit is executed when $s3 and $s4 values _____.
    a. Are equal
    b. Are not equal

58. A first part of a main program calls procedure Power to compute x^y, where x is in $s0, y is in $s1. Later, the program is to call Power again, but this time x is in $s3 and y is in $s7. How might the program pass the parameter values to Power?
    a. Copy $s3 to $a0, and $s7 to $a1
    b. Not possible; x and y must be in $s0 and $s1

59. A main program calls a Power procedure using the instruction: jal Power. That instruction is at address 1000. What happens to $ra?
    a. Nothing; jal is unrelated to $ra
    b. $ra is set to 1000
    c. $ra is set to 1004

60. A procedure Power computes $a0 to the power of $a1. How should the procedure jump back to the next instruction in the caller?
    a. jr caller
    b. jr $ra
    c. jal $ra

61. What is $s0 after: lui $s0, 7?
    a. 0000 0000 0000 0000 0000 0000 0000 0111
    b. 0000 0000 0000 0000 0000 0000 0111 0000
    c. 0000 0000 0000 0111 0000 0000 0111 0000
    d. 0000 0000 0000 0111 0000 0000 0000 0000
    e. 0000 0000 0000 1111 0000 0000 0000 0000

62. What is $s0 after executing the following MIPS codes?

```
lui $s0, 7
ori $s0, $s0, 8
```

    a. 0000 0000 0000 0000 0000 0000 0000 1111
    b. 0000 0000 0000 0000 0000 0000 0111 1000
    c. 0000 0000 0000 0111 0000 0000 0111 0000
    d. 0000 0000 0000 0111 0000 0000 0000 1000
    e. 0000 0000 0000 1111 0000 0000 0000 0000

Exam 2 CECS 341 (Chapters 3 and 4)

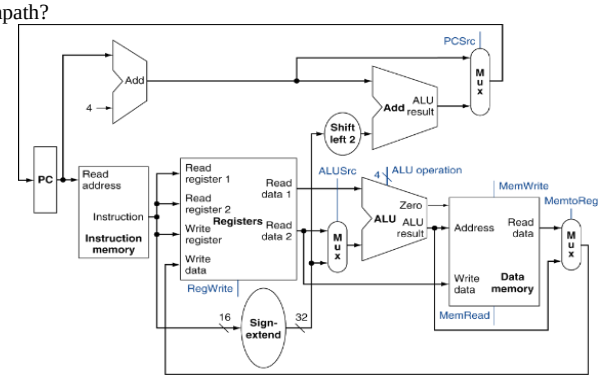
Last Name: _____ Last Four Student ID: _____ .
(Turn in both exam paper and scantrons)

```
 0 0 ... 0 1 1 0      0 0 ... 0 1 1 0
- 0 0 ... 0 1 0 0    + 1 1 ... d c b a
----------------     -----------------
                      s 0 0 ... z y x w
```

1. Consider the subtraction of base ten numbers 6 - 4 using 32-bit binary numbers, and achieved by adding 6 with the two's complement of 4. What is the value of dcba?
   a. 1011
   b. 1100
   c. 1010
   d. 0010
2. Consider the subtraction of base ten numbers 6 - 4 using 32-bit binary numbers, and achieved by adding 6 with the two's complement of 4. What is the value of zyxw?
   a. 1011
   b. 1100
   c. 1010
   d. 0010
3. The MIPS add, addi, and sub instructions may result in an exception.
   a. True
   b. False
4. A multiplexor is also called a selector, where its output is one of the inputs that is selected by a control.
   a. True
   b. False
5. A datapath element that has internal storage is called a _____ element.
   a. Combinational
   b. State
6. A register is a _____ element.
   a. Combinational
   b. State
7. An ALU is a _____ element.
   a. Combinational
   b. State
8. An edge-triggered clocking methodology means that any values stored in a sequential logic element are updated on a clock edge either from low to high or vice versa.
   a. True
   b. False
9. We can use the word asserted to indicate a signal that is logically high and assert to specify that a signal should be driven logically high.
   a. True
   b. False
10. A rising clock edge refers to the clock changing from _____.
    a. 0 to 1
    b. 1 to 0
    c. Either 0 to 1, or 1 to 0
11. The design of register file can read from two registers and write to one register during the same clock cycle.
    a. True
    b. False
12. The design of register file allows writes to a register during the same cycle that the same register is read.
    a. True
    b. False
13. The inputs carrying the register number to the register file are all__bits wide, whereas the lines carrying data values are 32 bits wide.
    a. 3
    b. 4
    c. 5
    d. 6
    e. 16
14. A register write must be explicitly indicated by asserting the write control signal.
    a. True
    b. False
15. A register read must be explicitly indicated by asserting the read control signal.
    a. True
    b. False
16. For R-type instruction with three register operands, we need to read __data(s) word from the register file.
    a. One
    b. Two
    c. Three
17. For R-type instruction with three register operands, we need to write __data word(s) into the register file.
    a. One
    b. Two

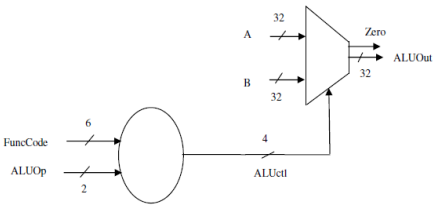
18. For R-type instruction with three register operands, to write a data word, we will need___ inputs for the register file.
    a. One
    b. Two
19. For R-type instruction with three register operands, we will need a total of ___ outputs for the register file.
    a. One
    b. Two
20. For the load instruction lw $t1, offset_value($t2), the value read from memory must be written into the register file in the specified register, which is____.
    a. $t1
    b. $t2
21. For the store instruction sw $t1, offset_value($t2), the value to be stored must also be read from the register file where it resides in ___.
    a. $t1
    b. $t2
22. For the data memory, the control signals should be ___for a store instruction.
    a. MemWrite = 0 and MemRead = 0
    b. MemWrite = 0 and MemRead = 1
    c. MemWrite = 1 and MemRead = 0
    d. MemWrite = 1 and MemRead = 1
23. For the *beq* instruction, branch taken is referred to the situation where the branch target address becomes the new PC when the condition is true.
    a. True
    b. False
24. In the MIPS architecture for a branch instruction, the branch target address is given by ____.
    a. sum of the offset field of the instruction and the address of the instruction following the branch.
    b. the offset field of the instruction
    c. the address of the instruction following the branch

25. Which of the following is correct for an *load* instruction referring to the right datapath?
    a. MemtoReg should be set to cause the read data from the data memory to be sent to the register file
    b. MemtoReg should be set to cause the ALUresult to be sent to the register file
    c. MemtoReg should be set to cause the Readdata2 from RF to be sent to the register file
26. hich of the following is correct for an *store* instruction referring to the right datapath?
    a. ALUSrc should be set to cause the Readdata1 from the RF to be sent to the ALU as the second input
    b. ALUSrc should be set to cause the Readdata2 from the RF to be sent to the ALU as the second input
    c. ALUSrc should be set to cause the sign-extended 16-bit offset field from the instruction to be sent to the ALU as the second input
    d. We do not care about the setting of ALUSrc for loads



27. The single-cycle datapath conceptually must have separate instruction and data memories due to the fact that _____ .
    a. The formats of data and instructions are different in MIPS, and hence different memories are needed
    b. Having separate memories is less expensive
    c. The processor operates in one cycle and cannot use a single-ported memory for two different accessed within that cycle

28. The MIPS ALU defines five different arithmetic and logic operations depending on four ALU control inputs. For the *branch* equal operation, the four ALUctl lines should be___.
    a. 0000
    b. 0010
    c. 0110
    d. 0111
29. The MIPS ALU defines five different arithmetic and logic operations depending on four ALU control inputs. For the *store* word instructions, the four ALUctl lines should be___.
    a. 0000
    b. 0010
    c. 0110
    d. 0111

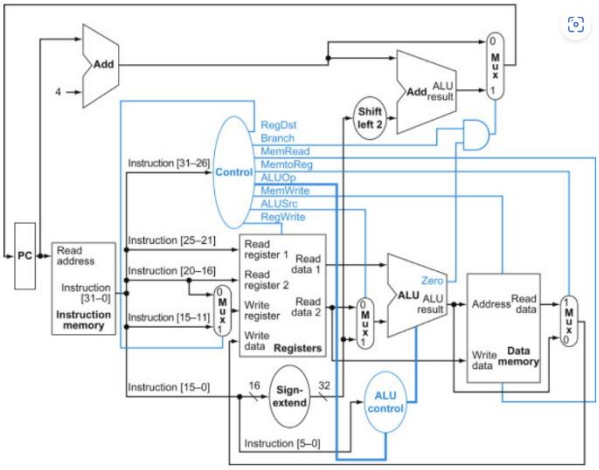


30. The MIPS ALU defines five different arithmetic and logic operations depending on four ALU control inputs. For the *slt* word instructions, the four ALUctl lines should be___.
    a. 0000
    b. 0010
    c. 0110
    d. 0111
31. The MIPS ALU defines five different arithmetic and logic operations depending on four ALU control inputs. For the logic *OR* instructions, the 2-bit ALUOp control lines should be___.
    a. 00
    b. 01
    c. 10
32. The MIPS ALU defines five different arithmetic and logic operations depending on four ALU control inputs. For the *sw* instructions, the 2-bit ALUOp control lines should be___.
    a. 00
    b. 01

c. 10

33. The MIPS ALU defines five different arithmetic and logic operations depending on four ALU control inputs. For the *beq* instructions, the 2-bit ALUOp control lines should be___.
    a. 00
    b. 01
    c. 10
34. The MIPS ALU defines five different arithmetic and logic operations depending on four ALU control inputs. For the *ADD* instructions, the 2-bit ALUOp control lines should be___.
    a. 00
    b. 01
    c. 10
35. The MIPS ALU defines five different arithmetic and logic operations depending on four ALU control inputs. The 4-bit ALU control input uses a small control unit that has inputs coming from ___.
    a. the 6-bit function fields of the instruction
    b. 2-bit control called ALUOp
    c. Both a and b

36. For LW and SW instructions, the ALU function _____.
    a. Is the same
    b. Differs



37. If the instruction is OR, then as well as examining the ALUOp bits, the ALU control will also examine _____.
    a. Instruction[31:26]
    b. Instruction[5:0]
38. The main control unit sends _____ bits to the ALU control.
    a. 0
    b. 1
    c. 2
39. The control unit enables a write to the register file using the _____ signal.
    a. RegDst
    b. MemWrite
    c. RegWrite
    d. MemRead
    e. MemWrite
40. When MemToReg is 0, the data appearing at the register file's data input comes from the _____.
    a. ALU result
    b. Read data from DM
    c. Register file's output
41. When MemToReg is 1, the data appearing at the register file's data input comes from the _____.
    a. ALU result
    b. Read data from DM
    c. Register file's output
42. The control unit's Branch output will be 1 for a branch equal instruction. However, the branch's target address is only loaded into the PC if the ALU's Zero output is _____. Otherwise, PC is loaded with PC + 4.
    a. 0
    b. 1
43. Assume the current instruction is beq $t1, $t2, offset, and $t1 is 90 while $t2 is 85. How will the PC be updated next?
    a. PC
    b. PC+4
    c. Target address
44. The ALU is used for both branch on equal and jump instructions.
    a. True
    b. False
45. Launching multiple instructions per stage allows the instruction execution rate to exceed the clock rate, or saying the CPI to be less than 1. This multiple issuing method can potentially increase the level of Instruction-Level Parallelism (ILP).
    a. True
    b. False
46. Throughput is defined as the number of instructions completed per unit of time. Pipelining can_____instruction throughput even no single instruction runs faster.
    a. increase
    b. decrease
47. Suppose Instr1 is fetched in stage 1. Instr1 then proceeds to stage 2, Reg read. In a pipelined implementation, can Instruction2 be fetched simultaneously with that Reg read?
    a. Yes
    b. No
48. On computer X, a nonpipelined instruction execution would require 12 ns, and thus 12 ns exists between instructions. A pipelined implementation uses 6 equal-length stages of 2 ns each, resulting in _____ ns between instructions.
    a. 1
    b. 2
    c. 4
    d. 6
    e. 12

49. On computer X, a nonpipelined instruction execution would require 12 ns. A pipelined implementation uses 6 equal-length stages of 2 ns each. Assuming one million instructions execute and ignoring empty stages at the start/end, what is the speedup of the pipelined vs. non-pipelined implementation?
    a. 1
    b. 2
    c. 4
    d. 6
    e. 12
50. Does the following cause a data hazard for the 5-stage MIPS pipeline?
    i1: add $s0, $s1, $s2
    i2: add $s3, $s1, $s4
    a. Yes
    b. No
51. The following causes a data hazard for the 5-stage MIPS pipeline. "Forwarding" can resolve the hazard by providing the ALU's output (for i1's stage 3) directly to the ALU's input (for i2's stage 3).
    i1: add $s0, $t0, $t1
    i2: sub $t2, $s0, $t3
    a. Yes
    b. No
52. Forwarding resolves some data hazards. Reordering resolves some others. If neither can resolve a data hazard, a stall may become necessary.
    a. True
    b. false
53. Can these instructions be reordered to avoid a pipeline stall?
    i1: add $s0, $s1, $s2
    i2: add $s3, $s4, $s5
    i3: lw $t1, 0($t0)
    i4: add $t3, $t1, $t4
    a. Yes
    b. No
54. i1: add $t1, $t0, $t0
    i2: lw $t2, $t0, 4($s0)
    i3: addi $t4, $t1, $t2
    a. must stall
    b. can avoid stalls using only forwarding
    c. can execute without stalling or forwarding
55. Two instructions could possibly access the register file simultaneously.
    a. True
    b. False
56. Two largely separable approaches to exploit branch prediction are *static* approach that relies on software technology to find parallelism statically at the compiler time and *dynamic* approach that relies on hardware to help discover and exploit the parallelism dynamically.
    a. True
    b. False
57. The sum is placed into the___pipeline register at the end of the EX stage for an *load* instruction using a pipelined MIPS architecture.
    a. IF/ID
    b. ID/EX
    c. EX/MEM
    d. MEM/WB
58. The data read from the data memory using the address calculated in the previous stage is placed into the___pipeline register at the end of the MEM stage for a *load* instruction using a pipelined MIPS architecture.
    a. IF/ID
    b. ID/EX
    c. EX/MEM
    d. MEM/WB
59. The data is written to the memory during the____half stage of the MEM for a *store* instruction using a pipelined MIPS architecture.
    a. First
    b. Second
60. The pipelined control signals are created during the _____stage and placed into the pipeline register and passed to the proper stage.
    a. IF
    b. ID
    c. ALU
    d. MEM
    e. WB
61. The store and load instructions differ in stage 5 (WB: write back) in that load writes to the register file whereas store reads the register file.
    a. True
    b. False
62. The read and written to a register can happen in the same clock cycle without any incurred dependence regarding these two accesses for a pipelined MIPS architecture.
    a. True
    b. False
63. In the pipelined datapath, for a R-type instruction, the control signals ALUOp and ALUSrc are used in the instruction's 3rd clock cycle, RegWrite is used in the instruction's 5th clock cycle.
    a. True
    b. false
64. The MIPS pipelined control approach determines all control line values during an instruction's 1st clock cycle, the instruction fetch stage.
    a. True
    b. false

```
36: sub  $10, $4, $8
40: beq  $1,  $3, 7
44: and  $12, $2, $5
48: or   $13, $2, $6
52: add  $14, $4, $2
56: slt  $15, $6, $7
---
72  lw $4, 50($7)
```

65. The processor will jump to the location___ if the comparison result for the branch instruction happens to be true for the above code sequence?
    a. 44
    b. 48
    c. 52
    d. 56
    e. 72
66. The processor will start to fetch the *lw* instruction in ___ if the comparison result for the branch instruction happens to be true for the above code sequence?
    a. cc1
    b. cc2
    c. cc3
    d. cc4
    e. cc5
67. How many stalls are needed if a comparison register for the branch instruction is a destination of immediately preceding load instruction considering the forwarding technique is available?
    a. 0
    b. 1
    c. 2
    d. 3
    e. 4

```
lw $t0, address
beq $t0, $t1, target address
```

68. How many stalls are needed for the above codes while early ID stage branch target address determination is allowed and the forwarding technique is not available?
    a. 0
    b. 1
    c. 2
    d. 3
    e. 4
69. According to MIPS convention, the term interrupt refers to an unscheduled event caused by an external source.
    a. True
    b. false
70. The action of computing the beq's target address can be done earlier, in the ID stage rather than the EX stage. That action means the target address will be computed for *all* instructions, not just beq instructions. A problem that may occur with such computing for all instructions is _____.
    a. Branching to a wrong target address
    b. No problem exists
    c. Longer flushing

CECS 341 Exam 3 (Chapter 5)

Name: Student ID:
Turn in both scantron exam papers!!!

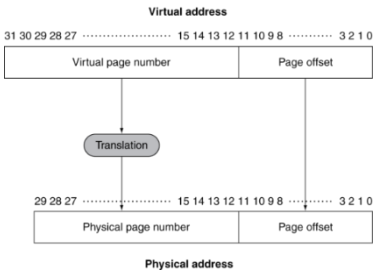
1. What are possible solutions to solve the memory wall problem?
   (a) hierarchy of multiple levels of caches
   (b) lock-up free caches
   (c) pre-fetched data and instructions
   (d) all of above
2. Instructions may exhibit temporal locality, but never spatial locality.
   a. True
   b. False
3. Data may exhibit temporal locality, but never spatial locality.
   a. True
   b. False
4. If a memory location is referenced, the locations with nearby addresses will tend to be referenced soon. This is referred to _____.
   (a) temporal locality
   (b) spatial locality
5. The minimum unit of information that can be either present or not present in the memory hierarchy is a__.
   a. Bit
   b. block
6. RAM can perform both write and read operations.
   (a) true
   (b) false
7. Memories in personal mobile devices are typically _____.
   a. Flash memory
   b. Magnetic disk
8. Byte address 360 maps to block number _____ assuming a direct-mapped cache with 32 blocks and a block size of 8 bytes.
   a. 12
   b. 13
   c. 18
   d. 32
   e. 50
9. Byte address 360 maps to a block address _____ assuming a direct-mapped cache with 32 blocks and a block size of 8 bytes.
   a. 12
   b. 13
   c. 18
   d. 32
   e. 45
10. Write-back technique will only update the block in the cache.
    a. True
    b. False
11. Assume a direct-mapped cache with 8 one-word blocks. Given the following sequence of block addresses, indicate if each request results in a cache hit or miss: 1, 9, 6, 5, 1, 6. The first memory block address of 1 will result in a __.
    a. Miss
    b. Hit
12. Assume a direct-mapped cache with 8 one-word blocks. Given the following sequence of block addresses, indicate if each request results in a cache hit or miss: 1, 9, 6, 5, 1, 6. The fifth memory block address of 1 will result in a __.
    a. Miss
    b. Hit
13. Assume a direct-mapped cache with 8 one-word blocks. Given the following sequence of block addresses, indicate if each request results in a cache hit or miss: 1, 9, 6, 5, 1, 6. The sixth memory block address of 1 will result in a __.
    a. Miss
    b. Hit
14. Assume a two-way set-associative cache with 8-one word blocks. Given the following sequence of block addresses, indicate if each request results in a cache hit or miss: 1, 9, 6, 5, 1, 6. The fourth memory block address of 5 will result in a __ .
    a. Miss
    b. Hit
15. Assume a two-way set-associative cache with 8-one word blocks. Given the following sequence of block addresses, indicate if each request results in a cache hit or miss: 1, 9, 6, 5, 1, 6. The fifth memory block address of 1 will result in a __ .

a. Miss
b. Hit

16. Assume a two-way set-associative cache with 8-one word blocks. Given the following sequence of block addresses, indicate if each request results in a cache hit or miss: 1, 9, 6, 5, 1, 6. The sixth memory block address of 6 will result in a __ .
    a. Miss
    b. Hit
17. Assume a fully associative cache with 8-one word blocks. Given the following sequence of block addresses, indicate if each request results in a cache hit or miss: 1, 9, 6, 5, 1, 6. The fifth memory block address of 1 will result in a __ .
    a. Miss
    b. Hit
18. Assume a fully associative cache with 8-one word blocks. Given the following sequence of block addresses, indicate if each request results in a cache hit or miss: 1, 9, 6, 5, 1, 6. The sixth memory block address of 6 will result in a __ .
    a. Miss
    b. Hit
19. A four-way set-associative cache with 32-one word blocks requires _____ comparators to compare the tags of each element within the set.
    a. 2
    b. 4
    c. 8
    d. 16
    e. 32
20. A direct mapped cache with 32-one word blocks requires _____ comparator(s) to compare the tags of of an element with the memory block address.
    a. 1
    b. 2
    c. 4
    d. 8
    e. 16
21. Which block in the cache is replaced by memory block 29?
    Cache configuration: 4-way set-associative cache with 8-one word blocks. Replacement scheme: LRU. Sequence of previously accessed block addresses: 5, 13, 21, 13, 5 *(Note: All memory block addresses map to cache set 1).*
    a. Mem[5]
    b. Mem[13]
    c. Mem[21]
    d. None. An element in set 1 is unused, so Mem[29] is placed in the fourth element of set 1.
22. Block access sequence 0, 8, 0, 6, and 8 are used to compare three different caches such as direct mapped, 2-way associative, and fully associative assuming each cache consisting of *four* one-word block (LCU is used for the replacement policy). Which cache will exhibit the *lowest* miss rate?
    (a) direct-mapped
    (b) 2-way associative
    (c) fully associative
23. Block access sequence 0, 8, 0, 6, and 8 are used to compare three different caches such as direct mapped, 2-way associative, and fully associative assuming each cache consisting of *eight* one-word block (LCU is used for the replacement policy). Which cache will exhibit the *highest* miss rate?
    a. direct-mapped
    b. 2-way associative
    c. fully associative
24. Block access sequence 0, 8, 0, 6, and 8 are used to compare three different caches such as direct mapped, 2-way associative, and fully associative assuming each cache consisting of *sixteen* one-word block (LCU is used for the replacement policy). Which cache will exhibit the *lowest* miss rate?
    a) direct-mapped
    b) 2-way associative
    c) fully associative
    d) all of them
25. For a direct mapped cache of 64 K Byte size with each block 128 bit and the memory address is composed of 32 bit, what is the size of byte offset?
    a) 0
    b) 2

c) 4

26. For a direct mapped cache of 64 K Byte size with each block 128 bit and the memory address is composed of 32 bit, what is the size of word offset?
    a. 0
    b. 2
    c. 4
27. For a direct mapped cache of 64 K Byte size with each block 128 bit and the memory address is composed of 32 bit, what is the size of index?
    a) 0
    b) 8
    c) 10
    d) 12
    e) None of above
28. For a direct mapped cache of 64 K Byte size with each block 128 bit and the memory address is composed of 32 bit, what is the size of tag field?
    a) 8
    b) 10
    c) 12
    d) 16
    e) None of above
29. The following sequence of nine memory references in word address (22, 26, 22, 26, 16, 3, 16, 18, and 12) is *directly* mapped to an empty eight-block cache with one word per block. What is the hit rate?
    (a) 4/9
    (b) 5/9
    (c) 6/9
    (d) 7/9
    (e) None of above
30. A physical page can be shared by more than one virtual page.
    (a) true
    (b) false
31. The page offset field in the virtual page will be copied directly without changes to the page offset field in the physical page if the request page is present in memory.
    (a) false
    (b) true
32. The number of virtual pages should be equal to the number of physical pages.
    (a) True
    (b) False



33. What is the page size specified by the right virtual address?
    (a) 2 KB
    (b) 4 KB
    (c) 8 KB
    (d) None of above
34. A zero value in the hit field of TLB shows a page fault.
    (a) True
    (b) False
35. A one value in the reference field of TLB shows a miss.
    (a) False
    (b) True
36. A zero value in the dirty field of TLB shows a write operation.
    (a) True
    (b) False
37. The first access to a block cannot be in the cache, so the block must be brought into the caches. Also called cold-start misses or first-reference misses. This is referred to:
    (a) Compulsory miss
    (b) Capacity miss
    (c) Conflict miss
38. Given: I/D-cache miss rates are 2% and 4% respectively, miss penalty for all misses are 100 clock cycles, the base CPI (ideal cache) without any memory stalls is 2, load & store are 36% of instructions, how much faster a processor would run with a perfect cache that never missed assuming IC =1?
    (a) 2.72
    (b) 1

(c) 1.72
(d) None of above

39. The 2:1 cache rule of thumb: a direct-mapped cache of size N has about the same miss rate as a two_way set associative cache of size of N/2.
(a) True
(b) False

40. Check contents of the write buffer on a read miss and if there are no conflicts and the memory system is available let read miss continue. This strategy can reduce the miss penalty.
(a) True
(b) False

41. For a two-level cache, the first-level cache can be_____enough to match the clock cycle time of the processor and the second level cache can be__large____ enough to capture many accesses that would go to main memory, thereby lessening the effective miss penalty.
(a) fast
(b) slow

42. Suppose that in 1000 memory references there are 40 misses in the first-level cache and 20 misses in the second-level cache. Assume the miss penalty from the L2 cache to memory is 200 clock cycles, the hit time of the L2 cache is 10 clock cycles, the hit time of the L1 is 1 clock cycle, and there are 1.5 memory references per instruction. Ignore the impact of writes. What is the local miss rate of the first-level cache?
(a) 50%
(b) 2%
(c) 4%

43. Suppose that in 1000 memory references there are 40 misses in the first-level cache and 20 misses in the second-level cache. Assume the miss penalty from the L2 cache to memory is 200 clock cycles, the hit time of the L2 cache is 10 clock cycles, the hit time of the L1 is 1 clock cycle, and there are 1.5 memory references per instruction. Ignore the impact of writes. What is the global miss rate of the first-level cache?
(a) 50%
(b) 2%
(c) 4%

44. Suppose that in 1000 memory references there are 40 misses in the first-level cache and 20 misses in the second-level cache. Assume the miss penalty from the L2 cache to memory is 200 clock cycles, the hit time of the L2 cache is 10 clock cycles, the hit time of the L1 is 1 clock cycle, and there are 1.5 memory references per instruction. Ignore the impact of writes. What is the local miss rate of the second-level cache?
(a) 50%
(b) 2%
(c) 4%

45. Suppose that in 1000 memory references there are 40 misses in the first-level cache and 20 misses in the second-level cache. Assume the miss penalty from the L2 cache to memory is 200 clock cycles, the hit time of the L2 cache is 10 clock cycles, the hit time of the L1 is 1 clock cycle, and there are 1.5 memory references per instruction. Ignore the impact of writes. What is the global miss rate of the second-level cache?
(a) 50%
(b) 2%
(c) 4%

46. Volatile memory retains stored information when power is turned off.
(a) True
(b) False

47. If an instruction access results in a miss, then the address of the instruction at _____ is fetched from the memory.
a. PC
b. PC-4
c. PC+4

48. AMAT considers the average time to access data for _____.
a. Misses
b. Hits
c. Both misses and hits