SCH56xx
Silicon Errata and Data Sheet Clarification

TABLE 1: SILICON DEV/REV VALUES

Part Number	Device ID(1)	Revision ID for Silicon Revision(2)
		A
SCH5627P	C6h	01h
SCH5636	C7h	01h

Note 1: The Device ID is visible as an 8-bit number at Plug and Play Configuration Index 20h.
2: The HW Revision Number is visible as an 8-bit number at Plug and Play Configuration Index 21h.

TABLE 2: SILICON ISSUE SUMMARY

Module	Feature	Item Number	Issue Summary	Affected Revisions(1)
				A
Keyboard Controller	KBDRST#	1.	KBDRST# Assertion on LRESET#	X
Keyboard Controller	Lockout	2.	Keyboard Controller Lockup	X
Host Interface	SERIRQ	3.	8 Clock SERIRQ Start Pulse	X
System WDT	WDT output	4.	GPIO Output on System Watchdog Timer	X

Note 1: Only those issues indicated in the last column apply to the current silicon revision.

Silicon Errata Issues

1. Module: Keyboard Controller

DESCRIPTION

The KBDRST# output will follow the LRESET# signal on cold boot: if LRESET# is asserted, KBDRST# will be driven low. For example, if LRESET# is driven for 100ms there will be a 100mS low pulse on KBDRST#

END USER IMPLICATIONS

On Intel platforms, the KBDRST# signal is edge-triggered, so that if LRESET# is asserted it stays asserted past the assertion of KBDRST#, there is no impact. This is normal system behavior in Intel platforms.

On AMD platforms, the KBDRST# signal is level-sensitive. When LRESET# is asserted, the assertion of KBDRST# will keep LRESET# asserted, preventing the completion of the boot process and locking up the system.

Work Around

For Intel platforms, no workaround is necessary.

For AMD platforms, set Virtual Register 0xC3, bit 0, to 1. The KBDRST# signal will then be decoupled from LRESET#.

For AMD platforms, there is a firmware patch available. Because the KBDRST# function is not the default function on the pin, the BIOS can load the patch before configuring the pin. Users should contact their Microchip FAE for information on the patch and instructions on how the BIOS needs to load the patch.

2. Module: Keyboard Controller

De-activating the 8042 Keyboard Controller (by setting Configuration Register 0x30 to 0) does not properly reset the device and may leave its internal state in an inconsistent configuration. Subsequent activations (by setting the Configuration Register 0x30 to 1) do not restore the keyboard controller to a consistent state, which may lead to undesirable behavior.

END USER IMPLICATIONS

Since the Keyboard Controller may come up in an indeterminate state, various anomalous behaviors may occur. For example, the Input Buffer Full flag may be set and never cleared, causing the device to hang.

Work Around

Software should manually reset the Keyboard Controller every time it is activated. The activation sequence should be:

1. Enter configuration mode and set the Current Logical Device to Keyboard Controller
2. Write a 0x1 to Configuration Register offset 0x30. This is the Activate bit.
3. Write a 0x1 to Configuration2014 Register offset 0xF2.
4. Write a 0x0 to Configuration Register offset 0xF2. This can be performed immediately after step 3); there is no delay requirement.
5. After Step 4) is completed the Keyboard Controller will be in a consistent state and will function normally.

3. Module: Host Interface

The SCH563xx only supports a SERIRQ start pulse with a duration of 4 to 7 clocks. The SERIRQ specification states that a SERIRQ pulse can last from 4 to 8 clocks.

END USER IMPLICATIONS

The SERIRQ start pulse cannot be configured to be 8 clocks long.

Work Around.

The system should configure the SERIRQ start pulse for 4 or 6 cycles. This is possible on most systems. At this writing, the only device that cannot be configured for 4 or 6 cycles is Intel's Whitney Point PCH (Oak Trail platform), which uses a fixed 8 clock SERIRQ start pulse. The Whitney Point PCH cannot be used with the SCH56xx if SERIRQ is required.

4. Module: System WDT

In certain circumstances, the pin GPIO25 may not be asserted if the System Watchdog Timer times out

END USER IMPLICATIONS

The system may not respond properly if the System Watchdog Timer times out.

Work Around

The workaround assumes that the EMI functions VREGWrite(address,data) and DCCMWrite(region,offset,data) exist.

The following sequence of operations should be performed (by the BIOS or Host CPU) before the System Watchdog Timer is enabled:

```
VREG_Write (0x0F, 0x5C);
VREG_Write (0x0F, 0x23);
VREG_Write (0x0F, 0x14);
VREG_Write (0x0F, 0x08);
VREG_Write (0x0F, 0x01);
DCCMWrite (0x01, 0x00, 0x7F);
DCCMWrite (0x01, 0x01, 0x01);
```

DCCMWrite (0x01, 0x02, 0x10);
DCCMWrite (0x01, 0x03, 0x00);
DCCMWrite (0x01, 0x07, 0x00);
DCCMWrite (0x01, 0x06, 0x80);
DCCMWrite (0x01, 0x05, 0x0C);
DCCMWrite (0x01, 0x04, 0x94);
DCCMWrite (0x01, 0x07, 0x00);
DCCMWrite (0x01, 0x06, 0x80);
DCCMWrite (0x01, 0x05, 0x09);
DCCMWrite (0x01, 0x04, 0x0E);
DCCMWrite (0x01, 0x08, 0x00);
EMI_IOWrite (EC_TO_HOST, 0xFF);
EMI_IOWrite (HOST_TO_EC, 0xD0);

After the sequence of EMI commands is completed, poll the EC_TO_HOST register and wait for it to return 0xD0.

Data Sheet Clarifications

The following typographic corrections and clarifications are to be noted for the latest version of the device data sheet (Revision 0.28) and firmware addendum (Revision 0.1).

Note: Where appropriate, corrections are shown in **bold**. Where possible, the original bold text formatting has been removed for clarity.

TABLE 3: DATA SHEET CLARIFICATION SUMMARY

Module	Item Number	Issue Summary
Electrical Characteristics	1.	Updated Power Consumption Table
Electrical Characteristics	2.	V_{REF} for AMD-TSI
Electrical Characteristics	3.	Missing Pin Characteristics
Timing Diagrams	4.	CLOCKI Timing specification
GPIO	5.	GPIO Pin connections
Fan Monitoring	6.	Tach SMI Acceleration Mode
PROCHOT features	7.	Clarification of Prochot Throttling Control
Fan Control	8.	Additional PWM Frequencies
Timing Diagrams	9.	Minimum LPC Clock Frequency

1. Module: Electrical Characteristics

The table below replaces the equivalent table from the data sheet.

TABLE 4: POWER CONSUMPTION

VCC	VTR	System State	EC State	Clock State	Supply Current			Comments
						Typical (25° C)	Max (70° C)	
3.3V	3.3V	S0-S2	Run	Ring OSC Active	VTR	15 mA	22 mA	
0V	3.3V	S3-S5	Run		VTR	11 mA	17 mA	
0V	0V	G3	Off	None	VBAT	2.5 µA	4.5 µA (@ 25° C)	2.0V < Vbat < 3.0V

2. Module: Electrical Characteristics

The V_{REF} buffer is specified for both PECI and AMD-TSI use. Refer to the following table for use of the V_{REF} buffer.

V_{REF} Buffer						Connects to VTT
Input Voltage, PECI	VI	0.95		1.26	V	Processor dependent
Input Voltage, AMD-TSI		1.425		1.9	V	
Input current	IDC			100	µA	
Input Low Current	ILEAK	-10		+10	µA	

In addition, the pin description for VREF should be called VREF and not PECI VREF in the Pinout figure as well as the Pin Table and the Signal Description table. When used as the AMD-TSI voltage reference, V_{REF} should be connected to 1.8V for DDR2 VDDIO and 1.5V for DDR3 VDDIO.

3. Module: Pin Description

The following pin characteristics should be added to the hardware specification:

Backdrive Protection

All pins except pins with buffer type PCI_IO and IAN are backdrive protected. The signals are listed in the specification. The backdrive leakage maximum at 5V is 10mA.

5V Tolerance

5V tolerant leakage is maximum 10mA. The maximum leakage at 5.5V is 16mA.

4. Module: Timing Diagrams

The following timing specifications will be added to the data sheet:

FIGURE 1: INPUT CLOCK TIMING

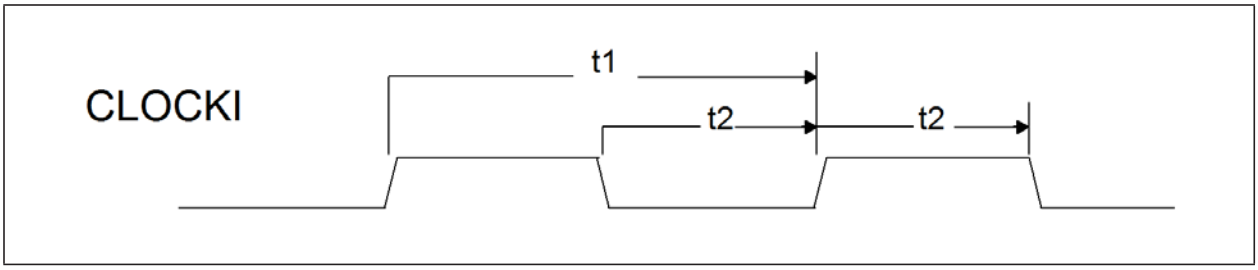

TABLE 5: INPUT CLOCK TIMING PARAMETERS

NAME	DESCRIPTION	MIN	TYP	MAX	UNITS
t1	Clock Cycle Time for 14.318MHZ		69.84		ns
t2	Clock High Time/Low Time for 14.318MHz	20	35		ns
	Clock Rise Time/Fall Time (not shown)			5	ns

5. Module: GPIO

The following requirement will be added to the pin description section:

No GPIO pin should be left floating in a system. If a GPIO pin is not in use, it should be either tied high, tied low, or pulled to either power or ground through a resistor.

6. Module: Fan Monitoring

The Tach SMI Acceleration Mode was not defined in the specification. This mode is enabled by default for Tach1 through Tach3. To disable the mode on those three Tachs, the BIOS should initialize VREG 2FBh to 0 before setting the Start bit to 1.

Register 2FBh: Tach SMI Action Control Register

VREG Address	Read /Write	Register Name	Bit 7 (MSb)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSb)	VVTR POR Default	PWRGD Reset
2FBh	R/W	Tach SMI Action Control Register	RES	RES	RES	TACH 4-Lpc-busTs	TACH3-Lpc-busTsk	TACH2 -Lpc-busTsk	TACH1 -Lpc-busTsk	RES	0Eh	N/A

This register is used to determine if the EC enables the Self-Clear function for TACH alert events. The Self-Clear function will automatically clear the HWM Tach interrupt enable bit when the corresponding Tach Status bit is read.

This register defaults to 0x0E, which enables the SMI Self-Clear mode for TACH1 through TACH3. The TACH4 SMI Self-Clear function defaults to disabled.

Bit[0] Reserved.

Bit[1] TACH1-LpcbusTsk

TACH1, control bit to enable TACH1 SMI event self-clear action. =1, enable, =0, disable.

Bit[2] TACH2-LpcbusTsk

TACH2, control bit to enable TACH2 SMI event self-clear action. =1, enable, =0, disable.

Bit[3] TACH3-LpcbusTsk

TACH3, control bit to enable TACH3 SMI event self-clear action. =1, enable, =0, disable.

Bit[4] TACH4-LpcbusTsk

TACH4, control bit to enable TACH4 SMI event self-clear action. =1, enable, =0, disable.

Bits[45:7] Reserved

Note: These control bits only have an effect if SMI acceleration is enabled.

7. Module: PROCHOT Features

The description of the control bits for Prochot throttling is unclear in the specification. The following sections show the revised definitions for the control bits in question.

Register 0CBh: PHOT_Forced_PR Status

VREG Address	Read/ Write	Register Name	Bit 7 (MSb)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSb)	VTRPOR Default	PWRGD Reset
0CBh	R-C	PHOT_Forced_PR Status	PHOT1 CPU0 Reading Valid	PHOT1 CPU0 Reading Valid	RES	CPU1 Throttle STS	CPU0 Throttle STS	Forced_ PR_ST S	RES	PHOT1	00h	00h
Note: This register is cleared on a read if no events are active.												

Bit[4] CPU1 Throttle Status

The CPU1 Throttle status bit is set (if enabled) when the processor exceeds the CPU1 Trigger High Limit causing a Throttling event. The status bit can be cleared by a read when the CPU1 temperature is less than the CPU1 Throttle Low Limit. See Section 14.4.44, "Register 1CCh - 1CDh: CPU0 Trigger," on page 258. The CPU1 Throttle event is enabled by the CPU1_THROT_EN bit located in Register 1CBh: Forced_PR Throttle Control. See Register 1CBh: Forced_PR Throttle Control.

Bit[3] CPU0 Throttle Status

The CPU0 Throttle status bit is set (if enabled) when the processor exceeds the CPU0 Trigger High Limit causing a Throttling event. The status bit can be cleared by a read when the CPU0 temperature is less than the CPU0 Throttle Low Limit. See Section 16.4.39, "Register 1CCh - 1CDh: CPU0 Trigger," on page 356. The CPU0 Throttle event is enabled by the CPU0_THROT_EN bit located in Register 1CBh: Forced_PR Throttle Control. See Register 1CBh: Forced_PR Throttle Control.

Register 1CBh: Forced_PR Throttle Control

VREG Address	Read/ Write	Register Name	Bit 7 (MSb)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSb)	VTR POR Default	PWRGD Reset
1CBh	R/W	Forced_PR Throttle Control	RES	CPU1_THROT_EN	CPU0_THROT_EN	RES	PROCHOT_IO#_POL	RES	FPHOT_Assert_EN	FPHOT_THROT_EN	00h	N/A

Bit[6] CPU1_THROT_EN

0= CPU1 throttle events are not enabled

1= CPU1 throttle events are enabled if an out-of-limit PROCHOT event occurs on CPU1

Bit[5] CPU0_THROT_EN

0= CPU0 throttle events are not enabled

1= CPU0 throttle events are enabled if an out-of-limit PROCHOT event occurs on CPU0

Bit[0] FPHOT_THROT_EN

This bit enables the ability to throttle the Forced_PR pin if a CPU throttle event occurs

0=PROCHOT_IO# throttling is disabled (default)

1=If an out-of-limit CPU event occurs and the event is enabled by CPU0_THROT_EN (for CPU0 throttle events) or by CPU1_THROT_EN (for CPU1 throttle events), throttle the Forced_PR pin. In addition, set the Forced_PR_STS bit in Register 0CBh: PHOT_Forced_PR Status to 1.

8. Module: Fan Control

The table describing the PWM frequency options controlled by VREGs 83h and 84h does not list all the frequency options. The following table includes the additional low frequency options:

TABLE 6: PWM FREQUENCY SELECT OPTIONS

Frequency Select Bits PxFRQ[3:0]	PWM Frequency (90kHz clock)	PWM Frequency (10MHz clock)
0000	11.0Hz	-
0001	14.6Hz	-
0010	21.9Hz	-
0011	29.3Hz	-
0100	35.2Hz	-
0101	44.0Hz	-
0110	58.6Hz	-

TABLE 6: PWM FREQUENCY SELECT OPTIONS (CONTINUED)

Frequency Select Bits PxFRQ[3:0]	PWM Frequency (90kHz clock)	PWM Frequency (10MHz clock)
0111	87.7Hz	-
1000	-	15kHz
1001	-	20kHz
1010	-	30kHz
1011	-	25kHz (default)
1100	-	500Hz
1101	-	2KHz
111x	Undefined	

9. Module: Timing Diagrams

The maximum period for the PCI Clock is 55.5nS. This permits an LPC clock of 18MHz.

The Floppy Interface will not work properly if the PCI Clock is below 24MHz.

APPENDIX A: DOCUMENT REVISION HISTORY

REVISION LEVEL AND DATE	DESCRIPTION
DS80000614A (05-15-14)	REV A replaces the previous SMSC version 1.10 (04-12-13) Added Data Sheet Clarification Number 9.
Rev. 1.1 (04-17-12)	Last SMSC release

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