Saurabh Raje

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Education

Birla Institute of Technology and Science, Pilani
Pilani, India

BE (Hons.) in Computer Science and Engineering

Aug. 2015 - Dec. 2018

Work Experience

ETH Zurich
Zurich, Switzerland

Scientific Assistant

High Performance Computing for Deep Learning

March 2019 - Present

- Working on accelerating training process of Deep Neural Networks using the **DACE** language developed in-house.
- DACE is a domain specific language for HPC workloads that uses a novel Stateful Dataflow Graph (SDFG) based Intermediate Representation.
- Many graph based transformations can be done on this SDFG IR, and generate code for CPU/GPU/FPGA clusters.
- Current efforts are to extend the **Tensorflow** frontend of DACE, which parses a TF computation graph to build a DACE SDFG.
- Future efforts would be to apply domain specific graph transformations on the SDFG to generate optimal code.

INRIA
Grenoble, France

Bachelor Thesis

High Performance Computing

September 2018 - February 2019

- Contributed to the development of **Rayon Adaptive API** for parallelization of iterators in the **Rust** language.
- This splits sequential iterators adaptively at runtime to create parallel tasks that can be stolen by the running threads.
- Revamped the **Rayon Logs** library that generates animated SVGs to visualise the task splitting and nested parallel iterators.
- The adaptive API was used to speed up a merge sort implementation which hence outperformed the optimised default sorting routine.
- Also explored various parallelization strategies for nested iterators in the context of a graph algorithm.

IBM Research
New Delhi, India

Research Intern

High Performance Computing for Deep Learning

May 2018 - July 2018

- Implemented the **GoogleNet** with variable batch sizing and activation checkpointing.
- This led to a 20% reduction in training time under memory constraints.
- Also worked on various optimisation heuristics for decomposition of sparse tensors.
- These outperformed best known heuristics in literature by 30%.

BITS Pilani
Pilani, India

Research Assistant

Parallelizing Compilers

August 2017 - December 2018

- Worked on the DWARF domain specific language compiler developed in-house.
- The compiler parallelizes code for various data mining applications, written in the DWARF language.
- Contributed to the modelling of various data dependencies in the context of density based and hierarchical clustering algorithms.
- Finally deployed a new optimisation layer that increased the granularity of parallelism.
- The system hence achived linear speedup for DBSCAN, SNN, and RECOME clustering algorithms.

Team Anant - A nanosatellite development team
Pilani, India

Team lead, on board computing

Systems development

January 2016 - January 2018

- Contributed to the development of an on board computer for a nanosatellite.
- Lead a group of ten students to this effect.
- Built a fault tolerant software to run complex monitoring and control algorithms for the satellite.
- Several device drivers for the Linux kernel were built from scratch to interface sensors and actuators on the satellite bus.
- The satellite will be launched by the Indian Space Research Organisation.

Publications

Distributed Non-Negative Tucker Decomposition

(submitted to) ACM International Conference on Supercomputing, 2019

Venkatesan Chakravarthy, Shivmaran Pandian, Saurabh Raje and Yogish Sabharwal

Automatic Parallelization of Density-based Clustering Algorithms
(submitted to) Pacific-Asia Conference on Knowledge Discovery and Data Mining (PAKDD), 2019
Saiyedul Islam, Sundar Balasubramaniam, Poonam Goyal, Ankit Sultana, Lakshit Bhutani, Saurabh Raje and Navneet Goyal

In-Loop Simulation of Attitude Control of a Nanosatellite
IEEE International Aerospace Conference, 2019
Vatsal Badami, Tushar Goyal, Shubham Sharma, Saurabh Raje and Kushagra Aggarwal

Development of an on board computer for a nanosatellite
International Astronautical Congress, 2017
Saurabh Raje, Abhishekh Goel, Shubham Sharma, Dhananjay Mantri, Kushagra Aggarwal and Tanuj Kumar

Decentralised firewall for malware detection
IEEE International Conference on Advances in Computing, Communication and Control (ICAC3), 2017
Saurabh Raje, Shyamal Vaderia, Neil Wilson and Rudrakh Panigrahi

Honors & Awards

2018 **Winner,** Best Poster Award - IBM Research Labs
2017 **Winner,** Mercedes Benz Hack.Banglore 2018
2016 **Winner,** Best Paper Award - APOGEE (BITS Pilani's technical festival)

Presentations

Mobile World Congress 2018
Barcelona, Spain
Presenter for Daimler AG
February 2018

- Invited by Daimler AG to present our winning hackathon prototype at the MWC.
- The prototype was built to detect pedestrians using low cost IR sensors.
- This would allow for level 4+ automated driving.

Academic Projects

Design of a scalable, spatially distributed data structure
In partial fulfilment of CS F422 - Parallel Computing
March 2018

- Designed an RTree based distributed data structure.
- This supports bulk multidimensional spatial queries in logarithmic time.
- Space taken by index per node was shown to grow sub linearly.

Parallel construction of inverted index
In partial fulfilment of CS F422 - Parallel Computing
Feb. 2018

- Conceptualised, developed and tested a scalable inverted index for document corpuses.
- Local word indices were to be computed on each node
- The indices were merged at the master while maintaining a sorted order.
- A network file system and a Beowulf cluster was set up for testing this solution.
- Obtained near linear speedup for up to 16 nodes.

Skills

Languages Rust, C, Python, Java, Haskell, TeX
Frameworks PyTorch, Tensorflow, Caffe, Git
Libraries openMPI, openMP