SMRITI GUPTA

+91 8750133274 **http://linkedin.com/in/smriti-gupta-b92a7b181** **guptasmriti110@gmail.com**

EDUCATION

M.TECH (Signal Processing and Digital Design)	2022-2024	Delhi Technological University, New Delhi	7/10
B.TECH (Electronics Engineering)	2017-2021	Bharati Vidpyapeeth College of Engineering, Pune	9.36/10
CBSE (Class XII)	2017	Vikas Bharati Public School	82.2 %
CBSE (Class X)	2015	Vikas Bharati Public School	85.5 %

EXPERIENCE

Engineer, Stryker, Gurugram *Mar 2025-Present*

- Successfully led two projects as a Manufacturing Engineer (ME), delivering key outcomes.
- Supporting five Ireland-based projects as ME, collaborating with cross-functional teams to drive manufacturing improvements.

Post Graduate Engineering Trainee, Stryker, Gurugram *Jun 2024-Mar 2025*

- Participated in 4 projects with supplier interaction, reviewing validation documents for gauges and manufacturing processes.
- Gained in-depth knowledge of medical implant manufacturing.

Intern, Stryker, Gurugram *Jul 2023-Jun 2024*

- Contributed to a value engineering project on PCBA and mechanical parts; created implant inspection sheets.
- Experienced in Adobe Pro and MBDVidia

Software Engineer, Capgemini, Hyderabad *Sept 2021-Oct 2022*

- Created API blueprints and developed Mule applications using Anypoint Platform and Studio.
- Extensive experience in writing and optimizing SQL queries.

PROJECTS

Designed and simulated a Sequence Detector using FSM in Verilog HDL with Xilinx Vivado

- Implemented a finite state machine (FSM) in Verilog HDL to detect a specific binary sequence. Defined state transitions and output logic, and performed functional simulation and verification using Xilinx Vivado.

Implementation of Vending Machine using FSM in Verilog HDL on Xilinx Vivado.

- FSM-based vending machine accepts ₹5 and ₹10 coins, dispensing a product at ₹15 and returning ₹5 change for ₹20. It operates through five states (RESET, RST5, RST10, RST15, RST20) and resets after 4 clock cycles if no coins are inserted.

FIFO & Counter DUT Verification

- Designed FIFO and counter in SystemVerilog; developed a complete UVM testbench with all components for thorough verification.

TECHNICAL SKILLS

Hardware Skills	Programming Skills	Simulation Tools
SystemVerilog | SV Assertions | UVM | Digital Electronics | STA | Basics of physical design | Low power VLSI Design | Knowledge of UART, I2C, SPI & CAN protocol | Computer Architecture	Basics of C & C++ | Verilog HDL	Xilinx Vivado | Proteus | VS Code | EDA Playground

CERTIFICATIONS

- Design Verification with SystemVerilog / UVM by Cristan Slav - Udemy

EXTRA-CURRICULAR ACTIVITIES AND ACHIEVEMENTS

- College Sports Captain at BVDU, Pune
  - Helped the college women basketball team win multiple intra-university and inter- university tournaments as a captain/mentor