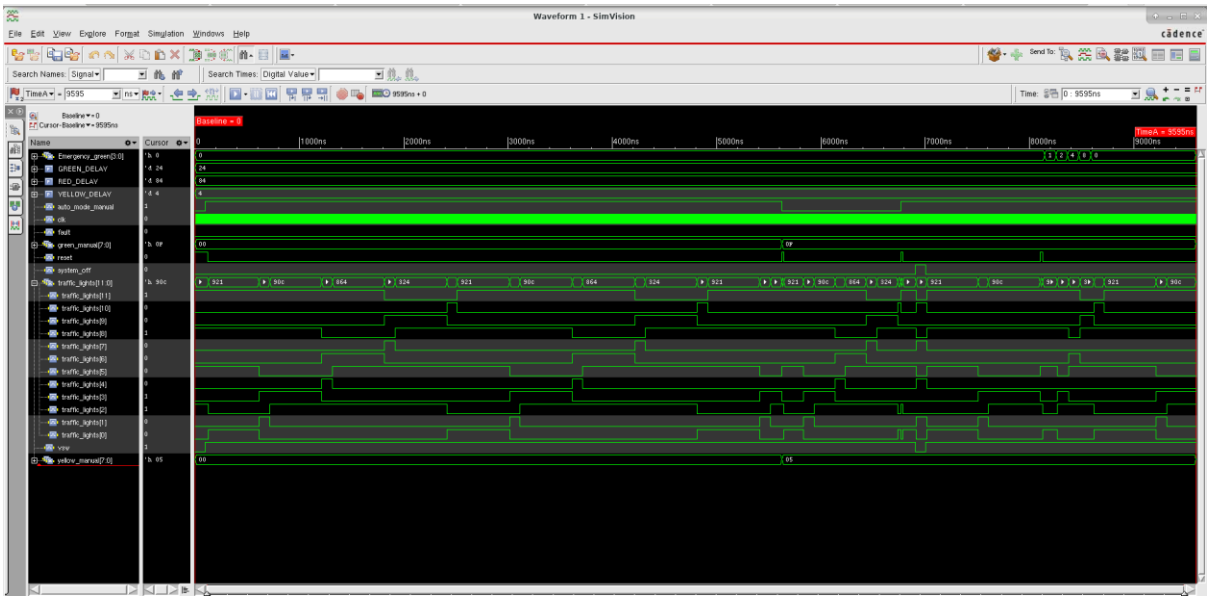
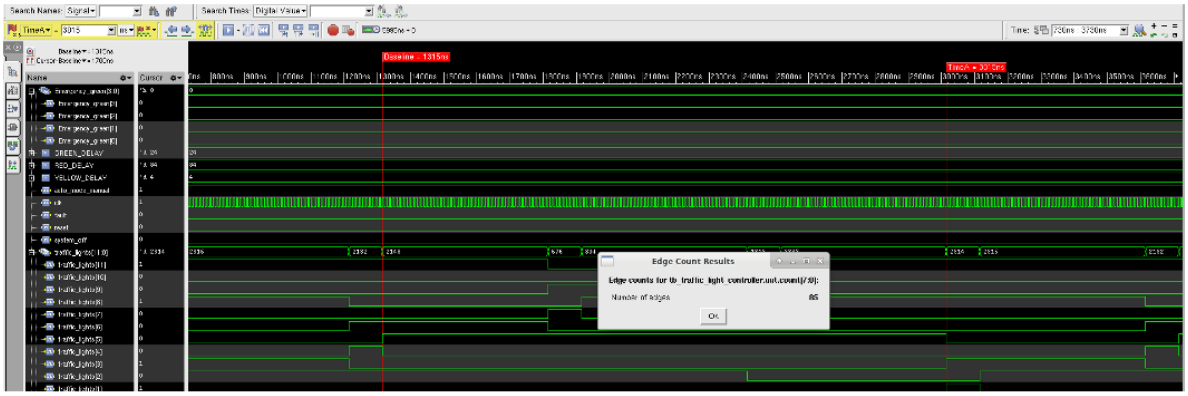
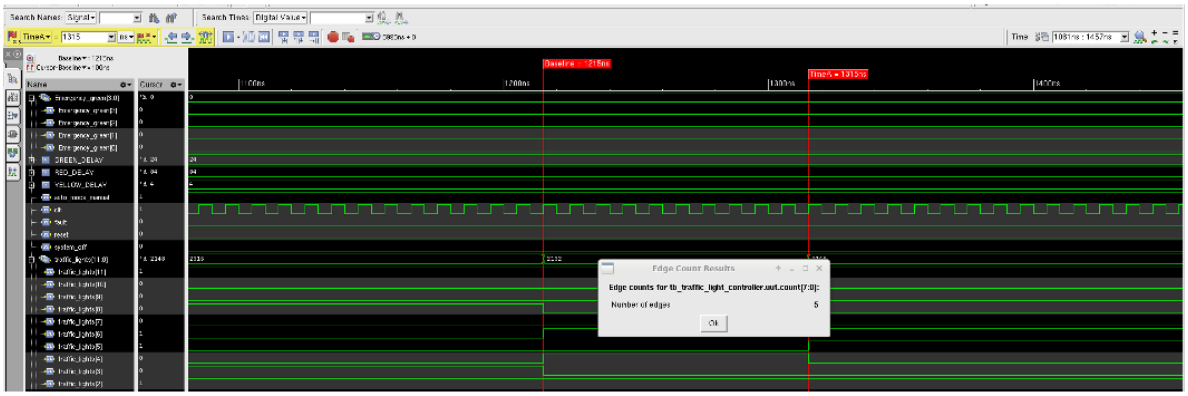
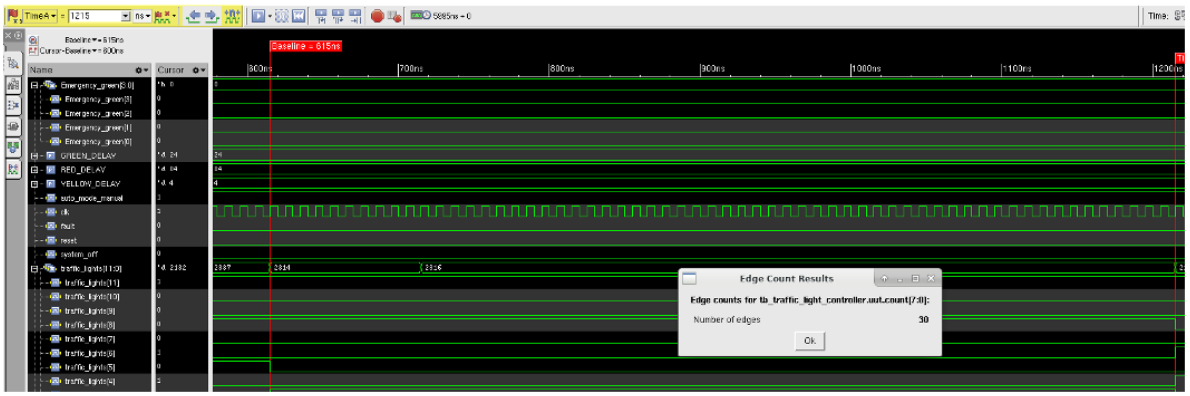
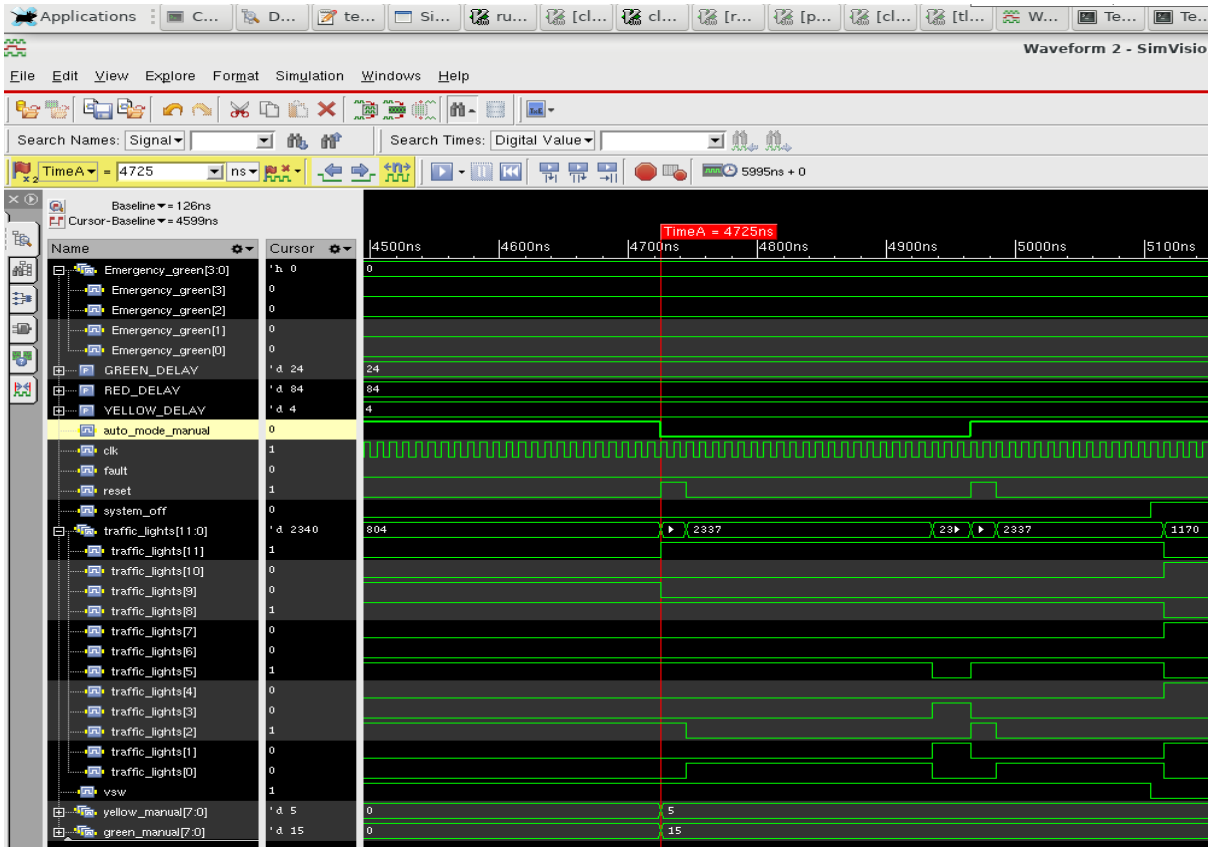
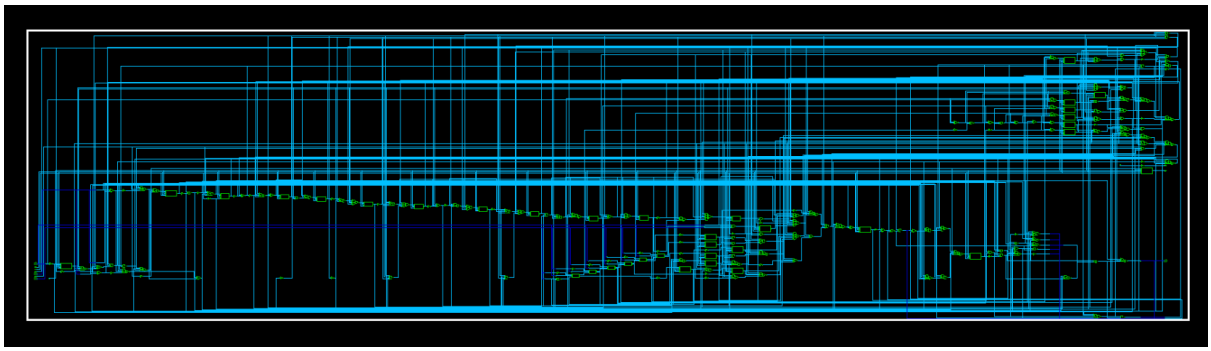

Waveform 1 - SimVision
File Edit View Explore Format Simulation Windows Help
cadence

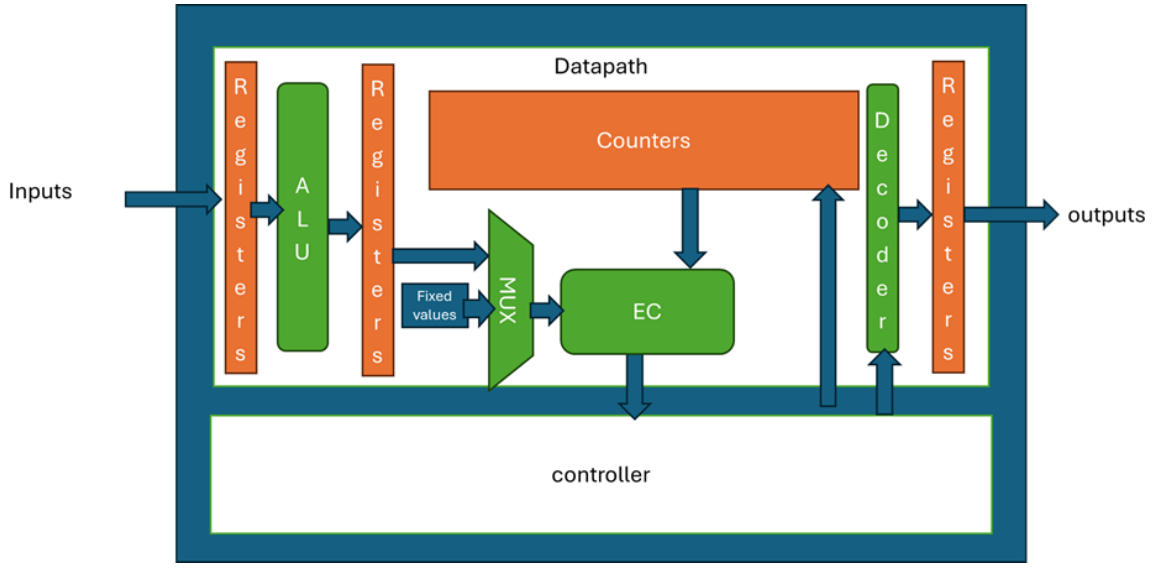

Edge Count Results
Edge counts for tb_traffic_light_controller.uut.count[7:0]:
Number of edges
85
Ok

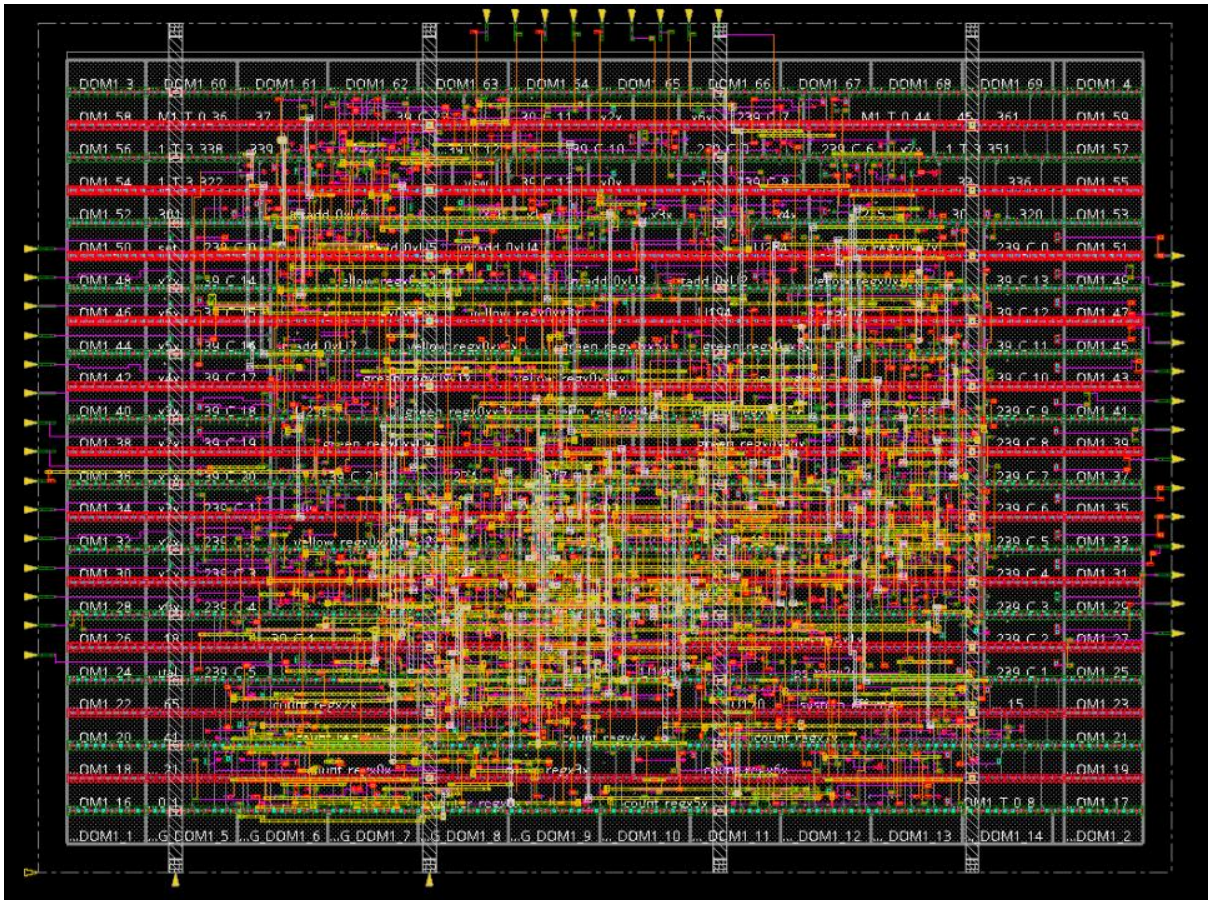

Edge Count Results
Edge counts for tb_traffic_light_controller.uut.count[7:0]:
Number of edges
5
Ok


Edge Count Results
Edge counts for tb_traffic_light_controller.uut.count[7:0]:
Number of edges
30
Ok


Waveform 2 - SimVisio
File Edit View Explore Format Simulation Windows Help
Search Names: Signal
Search Times: Digital Value
TimeA = 4725ns
4500ns
4600ns
4700ns
4800ns
4900ns
5000ns
5100ns
Name
Cursor
Emergency_green[3:0]
Emergency_green[3]
Emergency_green[2]
Emergency_green[1]
Emergency_green[0]
GREEN_DELAY
RED_DELAY
YELLOW_DELAY
auto_mode_manual
clk
fault
reset
system_off
traffic_lights[11:0]
traffic_lights[11]
traffic_lights[10]
traffic_lights[9]
traffic_lights[8]
traffic_lights[7]
traffic_lights[6]
traffic_lights[5]
traffic_lights[4]
traffic_lights[3]
traffic_lights[2]
traffic_lights[1]
traffic_lights[0]
vsw
yellow_manual[7:0]
green_manual[7:0]




Datapath
Inputs
Registers
ALU
Registers
Counters
Fixed values
MUX
EC
Decoder
Registers
outputs
controller



```
 /* ##################################################################################### */
 /*  Generated with Design Compiler STANDARD WLM (version U-2022.12-SP3)   */
 /*  using DC_WLM_SYN_RTL2NET task with       *** FrontEndKit 6.2-00 ***         */
 /*  Generate Date      : Fri May 10 11:26:36 2024       */
 /*  Working  directory : /prj/R2G_DMIPS/P18/P18_ROADRUNNER_MDG_LOCK_CKT_2024/development/digital/synth_STA_fm/DEEPAK/sm/WORKSPACE9may24/FRONTEND/DC_WLM_SYN_RTL2NET  */
 /*  Generated by       : katariyd      */
 /* ##################################################################################### */
////////////////////////////////////////////////////////////////
// Created by: Synopsys DC Ultra(TM) in wire load mode
// Version   : U-2022.12-SP3
// Date      : Fri May 10 11:26:36 2024
////////////////////////////////////////////////////////////////


module traffic_light_controller ( clk, reset, Emergency_green,
        auto_mode_manual, yellow_manual, green_manual, vsw, fault, system_off,
        traffic_lights );
  input [3:0] Emergency_green;
  input [7:0] yellow_manual;
  input [7:0] green_manual;
  output [11:0] traffic_lights;
  input clk, reset, auto_mode_manual, vsw;
  output fault, system_off;
  wire   sub_counterx0x, N260, N272, N273, N274, N275, N276, N277, N278, N279,
         N281, N282, N283, N284, N285, N286, N287, N288, n125, n126, n127,
         n128, n129, n130, n131, n132, n133, n134, n135, n136, n137, n138,
         intadd_0xBx5x, intadd_0xBx4x, intadd_0xBx3x, intadd_0xBx2x,
         intadd_0xBx1x, intadd_0xBx0x, intadd_0xCI, intadd_0xSUMx5x,
         intadd_0xSUMx4x, intadd_0xSUMx3x, intadd_0xSUMx2x, intadd_0xSUMx1x,
         intadd_0xSUMx0x, intadd_0xn6, intadd_0xn5, intadd_0xn4, intadd_0xn3,
         intadd_0xn2, intadd_0xn1, n141, n142, n143, n144, n145, n146, n147,
         n150, n151, n152, n153, n154, n155, n156, n157, n158, n159, n160,
         n161, n162, n163, n164, n165, n166, n167, n168, n169, n170, n171,
         n172, n173, n174, n175, n176, n177, n178, n179, n180, n181, n182,
         n183, n184, n185, n186, n187, n188, n189, n190, n191, n192, n193,
         n194, n195, n196, n197, n198, n199, n200, n201, n202, n203, n204,
         n205, n206, n207, n208, n209, n210, n211, n212, n213, n214, n215,
         n216, n217, n218, n219, n220, n221, n222, n223, n224, n225, n226,
         n227, n228, n229, n230, n231, n232, n233, n237, n238, n239, n240,
         n241, n242, n243, n244, n245, n246, n247, n248, n249, n250, n251,
         n252, n253, n254, n255, n256, n257, n258, n259, n2600, n261, n262,
         n263, n264, n265, n267, n268;
  wire   [2:0] ps0;
  wire   [3:0] ns0;
  wire   [7:0] count;
  wire   [31:24] internal_green;
  wire   [31:24] internal_yellow;

  P18_9T_SDFPSQN_X10_PB4_L internal_green_regx0xx4x ( .D(N276), .TI(1'b0),
        .TE(1'b0), .CP(clk), .SN(n126), .QN(n129) );
  P18_9T_SDFPSQN_X10_PB4_L internal_green_regx0xx3x ( .D(N275), .TI(1'b0),
        .TE(1'b0), .CP(clk), .SN(n126), .QN(n128) );
  P18_9T_SDFPSQN_X10_PB4_L internal_yellow_regx0xx2x ( .D(N283), .TI(1'b0),
        .TE(1'b0), .CP(clk), .SN(n126), .QN(n127) );
  P18_9T_SDFPR1Q_AX10_PB4_L internal_green_regx0xx7x ( .D(N279), .TI(1'b0),
        .TE(1'b0), .CP(clk), .R(reset), .Q(internal_green[31]) );
  P18_9T_SDFPR1Q_AX10_PB4_L internal_green_regx0xx6x ( .D(N278), .TI(1'b0),
        .TE(1'b0), .CP(clk), .R(reset), .Q(internal_green[30]) );
  P18_9T_SDFPR1Q_AX10_PB4_L internal_green_regx0xx5x ( .D(N277), .TI(1'b0),
        .TE(1'b0), .CP(clk), .R(reset), .Q(internal_green[29]) );
  P18_9T_SDFPR1Q_AX10_PB4_L internal_green_regx0xx2x ( .D(N274), .TI(1'b0),
        .TE(1'b0), .CP(clk), .R(reset), .Q(internal_green[26]) );
  P18_9T_SDFPR1Q_AX10_PB4_L internal_green_regx0xx1x ( .D(N273), .TI(1'b0),
```

```
Startpoint: ps_regx3x (rising edge-triggered flip-flop clocked by clk)
  Endpoint: ps_regx2x (rising edge-triggered flip-flop clocked by clk)
  Path Group: clk
  Path Type: max

  Des/Clust/Port     Wire Load Model       Library
  ------------------------------------------------
  traffic_light_controller wl_zero         P18_SC_9T_CORE_PB4_L

Attributes:
    d - dont_touch
    u - dont_use
   mo - map_only
   so - size_only
    i - ideal_net or ideal_network
  inf - infeasible path

  Point                                Fanout     Trans      Incr       Path      Attributes
  ---------------------------------------------------------------------------------------------
  clock clk (rise edge)                                    0.0000     0.0000
  clock network delay (ideal)                              0.0000     0.0000
  ps_regx3x/CP (P18_9T_SDFPSQN_X5_PB4_L)      0.2000      0.0000     0.0000 r
  ps_regx3x/QN (P18_9T_SDFPSQN_X5_PB4_L)      0.0570      0.2241     0.2241 f
  n125 (net)                           4                  0.0000     0.2241 f
  U161/Z (P18_9T_CTIV_BX10_PB4_L)             0.0575      0.0621     0.2862 r
  n239 (net)                           5                  0.0000     0.2862 r
  U226/Z (P18_9T_NOR2_BX5_PB4_L)              0.0513      0.0568     0.3431 f
  n228 (net)                           3                  0.0000     0.3431 f
  U268/Z (P18_9T_CTIV_BX10_PB4_L)             0.0384      0.0460     0.3891 r
  n185 (net)                           3                  0.0000     0.3891 r
  U269/Z (P18_9T_OAI21_X5_PB4_L)              1.0390      0.6161     1.0052 f
  traffic_lights[9] (net)              2                  0.0000     1.0052 f
  U195/Z (P18_9T_NOR2_BX5_PB4_L)              0.1546      0.3075     1.3127 r
  n232 (net)                           2                  0.0000     1.3127 r
  U192/Z (P18_9T_OAI21_X5_PB4_L)              0.0548      0.0760     1.3888 f
  n160 (net)                           1                  0.0000     1.3888 f
  U191/Z (P18_9T_AOI22_X5_PB4_L)              0.0454      0.0541     1.4428 r
  n167 (net)                           1                  0.0000     1.4428 r
  U288/Z (P18_9T_OAOI211_X5_PB4_L)            0.0612      0.0713     1.5142 f
  ns0[2] (net)                         1                  0.0000     1.5142 f
  ps_regx2x/D (P18_9T_SDFPR1Q_AX10_PB4_L)     0.0612      0.0000     1.5142 f
  data arrival time                                                   1.5142

  clock clk (rise edge)                                    8.0000     8.0000
  clock network delay (ideal)                              0.0000     8.0000
  clock uncertainty                                       -0.3000     7.7000
  ps_regx2x/CP (P18_9T_SDFPR1Q_AX10_PB4_L)                 0.0000     7.7000 r
  library setup time                                      -0.2486     7.4514
  data required time                                                  7.4514
  ---------------------------------------------------------------------------------------------
  data required time                                                  7.4514
  data arrival time                                                  -1.5142
  ---------------------------------------------------------------------------------------------
  slack (MET)                                                         5.9372
```