Mini MOSbius Proposal

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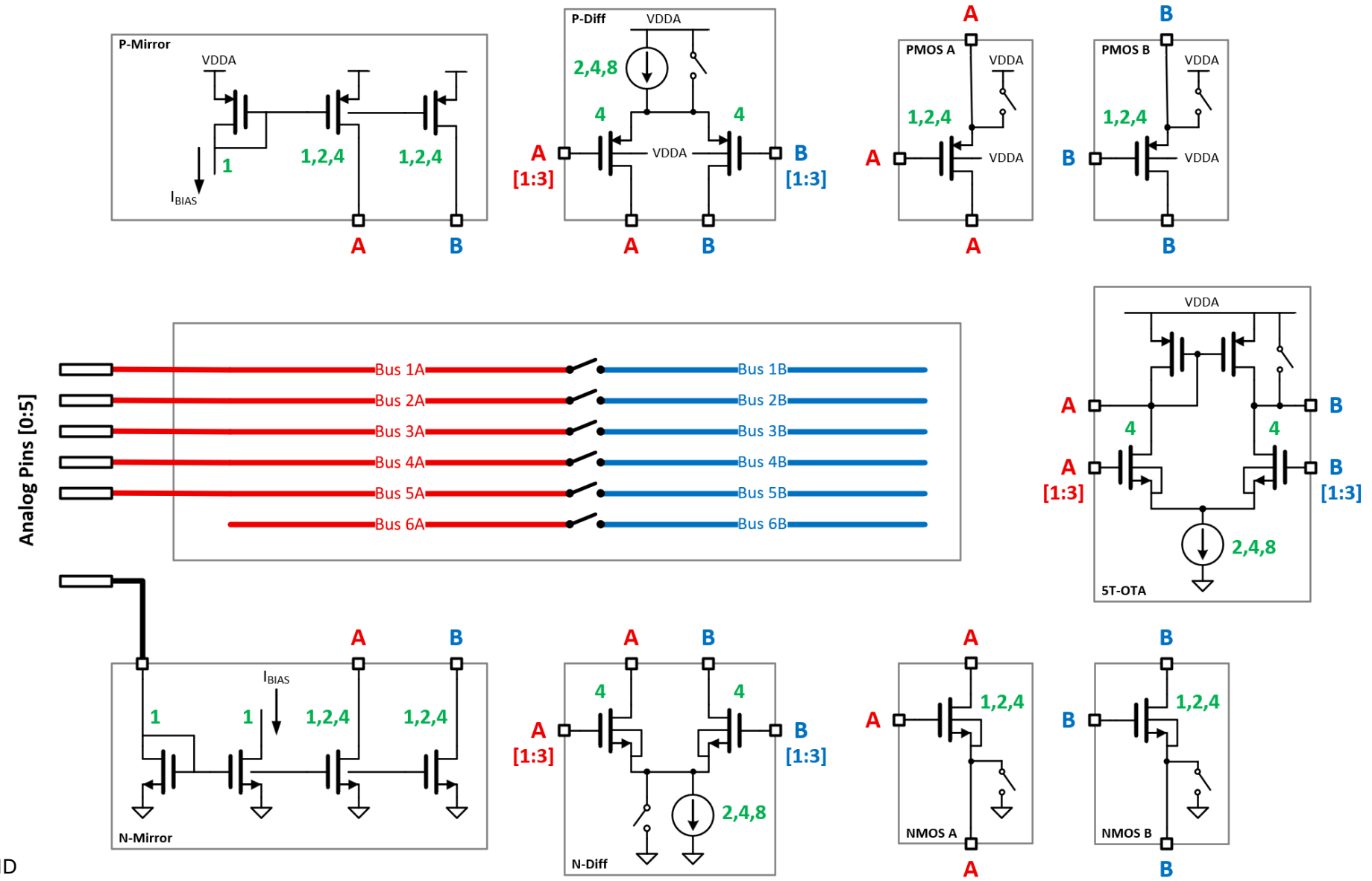
Proposed System Diagram



*Also includes VDDA/GND connections to Bus A[1:6]

Proposed System Description

- Analog Pins: 6
  - 5 Pins connect to busses
  - 1 Pin for bias current input
- Area: approx. 480um x 225um for 3x2 Tiny Tapeout
- Power: 3.3V (analog) and 1.8V (digital)
- Crosspoint Switch:
  - 6 Busses
    - 5 can connect to analog pins, 1 is internal only
    - Split into A/B sections to allow a joint bus or isolated busses
  - 30 Nodes
    - All nodes can connect to Bus[1:6], except 6 nodes can connect to Bus[1:3] only
  - Transmission Gates: 168
    - Per Matt's estimation, 6 tile supports 188 T-Gates with 70% area allocation
- *Strategy: To achieve sufficient functionality with limited pins and area compared to MOSbius, four techniques are proposed (1) use programmable width devices (2) allow busses to be split into A/B sections (3) some nodes may only be connected to a subset of busses (4) allow device source to be shorted to VDDA/GND so that we can avoid "wastefully" assigning VDDA/GND to Bus[1:6] whenever possible.*

Included Blocks

QTY	Block	Comments
1	N-Current Mirror	Fanout 2, each programmable 1:1, 2, 4
1	P-Current Mirror	Fanout 2, each programmable 1:1, 2, 4 Input bias current comes from NMOS Current Mirror
1	N-Diff Pair	Programmable tail current Shorting source to ground allows common-source usage
1	P-Diff Pair	Programmable tail current Shorting source to VDDA allows common-source usage
2	NMOS	Programmable Width Source may be connected to ground even if Bus[1:6] does not contain ground
2	PMOS	Programmable Width Source may be connected to VDDA even if Bus[1:6] does not contain VDDA
1	5T OTA	Programmable tail current Two single-ended output options: (1) diode connected load (2) active load

Possible Applications

#	Application	Blocks Used	Busses Used	Comments
1	5 Transistor OTA	N-Diff Pair PMOS (x2)	1A, 1B, 2, 3	
2	Two Stage Amplifier	N-Diff Pair P-Diff Pair (Common-Source Mode) PMOS N-Current Mirror	1A, 1B, 2, 3, 4	External R and C for Miller Compensation
3	Ring Osc 3 Stage	N-Diff Pair (Common-Source Mode) P-Diff Pair (Common-Source Mode) PMOS NMOS	1,2,3	
4	5 Transistor Fully Differential OTA (with CMFB)	N-Diff Pair P-Diff Pair (Common-Source Mode) 5T OTA	1A, 1B, 2, 3, 4, 5, 6	External R and C, and bias voltage
5	Harald Pretl 50 Nifty Two Transistor	Varies	Varies	Many/Most variants can be done.

Design Schedule

- Current Status (21 July): Proposal Pending Acceptance/Approval by Matt
- Target Shuttle: TTSKY25a
- Schematic Review: By 08 August
- Layout Review: By 29 August
- Submission: By 15 September