CS223 DIGITAL DESIGN

SECTION 02

LAB 02

Sümeyye ACAR

22103640

24.04.2023

Half Adder

b.1) Behavioral SystemVerilog module

```
module my_half_adder(input logic a, b, output logic sum, cout);
assign sum = a ^ b;
assign cout = a & b;
endmodule
```

---

b.2) Testbench

```
module my_half_adder_testbench();
logic a, b;
logic sum, cout;

my_half_adder ha(a,b,sum,cout);

  initial begin
    a = 0; b = 0; #10;
    b = 1; #10;
    a = 1; b = 0; #10;
    b = 1; #10;
    $finish;
  end
endmodule
```

Half Subtractor

c.1) Behavioral SystemVerilog module

```
module my_half_subtractor(input logic a, b, output logic diff, bout);
assign diff = a ^ b;
assign bout = ~a & b;
endmodule
```

---

c.2) Testbench

```
module my_half_subtractor_testbench();
logic a, b;
logic diff, bout;

my_half_subtractor hs(a,b,diff,bout);

   initial begin
        a = 0; b = 0; #10;
        b = 1; #10;
        a = 1; b = 0; #10;
        b = 1; #10;
        $finish;
   end
endmodule
```

Full Adder

d.1) Structural SystemVerilog module (using the half adder in part b)

```
module my_full_adder(input logic a, b, cin, output logic sum, cout);
wire tempSum, tempCout1, tempCout2;
my_half_adder ha1(a,b,tempSum,tempCout1);
my_half_adder ha2(tempSum, cin, sum, tempCout2);
assign cout = tempCout1 | tempCout2;
endmodule
```

---

d.1) Testbench

```
module my_full_adder_testbench();
logic a, b, cin;
logic sum, cout;
my_full_adder fa(a,b,cin,sum,cout);
   initial begin
         a = 0; b = 0; cin = 0; #10;
         cin = 1; #10;
         b = 1; cin = 0; #10;
         cin = 1; #10;
         a = 1; b = 0; cin = 0; #10;
         cin = 1; #10;
         b = 1; cin = 0; #10;
         cin = 1; #10;
         $finish;
   end
endmodule
```

Full Subtractor

e.1) Structural SystemVerilog module (using the half subtractor in part c)

```
module my_full_subtractor(input logic a, b, bin, output logic diff, bout);
wire tempDiff, tempBout1, tempBout2;
my_half_subtractor hs1(a,b,tempDiff,tempBout1);
my_half_subtractor hs2(tempDiff, bin, diff, tempBout2);
assign bout = tempBout1| tempBout2;
endmodule
```

---

e.1) Testbench

```
module my_full_subtractor_testbench();
logic a, b, bin;
logic diff, bout;
my_full_subtractor fs(a,b,bin,diff,bout);
   initial begin
        a = 0; b = 0; bin = 0; #10;
        bin = 1; #10;
        b = 1; bin = 0; #10;
        bin = 1; #10;
        a = 1; b = 0; bin = 0; #10;
        bin = 1; #10;
        b = 1; bin = 0; #10;
        bin = 1; #10;
        $finish;
   end
endmodule
```