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### QUESTION 1

Table 1 gives hypothetical relevant chip statistics that influence the cost of several current and future chips. Study it and answer the questions that follow:

Chip	Die Size (mm <sup>2</sup> )	Estimated defect rate (per cm <sup>2</sup> )	N	Manufacturing size (nm)	Transistors (billion)	Cores
BlueDragon	180	0.03	12	10	7.5	4
RedDragon	120	0.04	14	7	7.5	4
Phoenix8	200	0.04	14	7	1.2	8

(a) What is the yield for the Phoenix chip? (3 marks)

$$\begin{aligned}\text{Yield} &= 1 / (1 + (0.04 \times 2))^{14} \\ &= 0.34\end{aligned}$$

(b) Why does Phoenix have a higher defect rate than BlueDragon (2 marks)

Phoenix is manufactured in a much older technology, which is an older plant. As plants age, their process gets tuned, and the defect rate decreases.

(c) Assuming that a company produces the above chips for sale. Phoenix is manufactured with the 7nm technology in mind, whereas RedDragon uses the technology used for the 10nm BlueDragon chip. RedDragon will make a profit of USD 15 per defect-free chip and Phoenix \$30 per defect-free chip. Each wafer has a 450 mm diameter.

i. How much profit will be made from each wafer of Phoenix chips (3 marks)

$$\begin{aligned}\text{Dies per Wafer} &= (\pi \times (45/2)^2) / 2 - (\pi \times 45) / \sqrt{2 \times 2} \\ &= 795 - 70.7 \\ &= 724.5 \\ &= 724\end{aligned}$$

$$\begin{aligned}\text{Yield} &= 1 / (1 + (0.04 \times 2))^{14} \\ &= 0.340\end{aligned}$$

$$\begin{aligned}\text{Profit} &= 724 \times 0.34 \times 30 \\ &= 7384.80\end{aligned}$$

ii. How much profit will be made from each wafer of RedDragon chip (3 marks)

$$\begin{aligned}\text{Dies per Wafer} &= (\pi \times (45/2)^2)/2 - (\pi \times 45)/\sqrt{(2 \times 1.2)} \\ &= 1325 - 91.25 \\ &= 1234\end{aligned}$$

$$\begin{aligned}\text{Yield} &= 1/(1 + (0.04 \times 1.2))^{14} \\ &= 0.519\end{aligned}$$

$$\begin{aligned}\text{Profit} &= 1234 \times 0.519 \times 15 \\ &= 9601.71\end{aligned}$$

## **QUESTION 2**

**(a) According to the trend in device scaling observed by Moore's Law, the number of transistors on a chip in 2025 should be how many times the number in 2015? ( 2 marks)**

Difference in years = 2025 - 2015 = 10

Number of cycles = 10/2 = 5 cycles

Number of times =  $2^5 = 32$

Moore's law predicts that the number of transistors on a chip will double every 2 years. The number of transistors on a chip in 2025 should be 32 times that of a chip in 2015.

**(b) The increase in performance once mirrored the trends in 2(a) above. Had this trend continued, approximately what performance would chips have over VAX-11/780 in 2025? (2 marks)**

6043 in 2003, 52% growth rate per year for 12 years is 60,500,000

**(c) At the current rate of increase in performance, what is the more realistic growth projection by 2025 based on recent statistics? (2 marks)**

24,129 in 2010, 22% growth rate per year for 15 years is 1,920,000

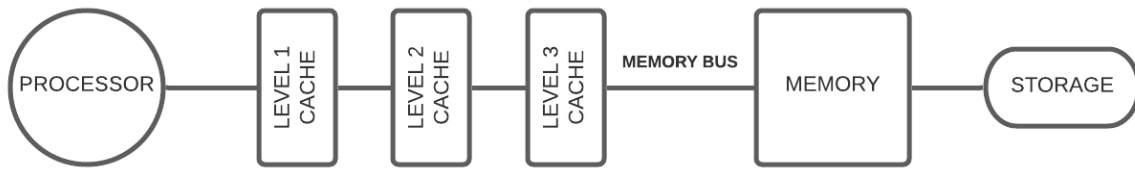
**(d) What has limited the rate of growth of clock speed? (2 marks)**

Higher clock speed means higher power dissipation which in turn causes chips to get hotter and burn, blow up or melt. Instead of increasing the clock rate, manufacturers have opted to place more cores on the chips

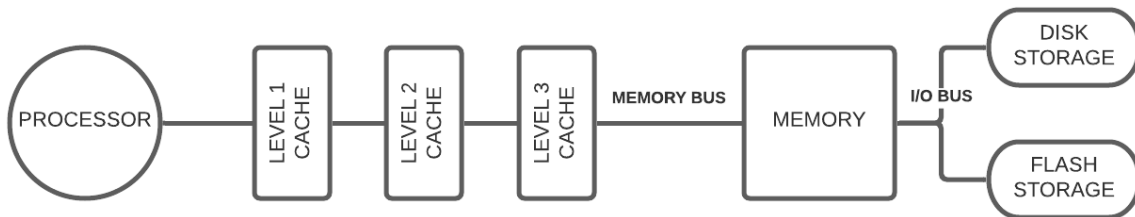
**(e) Discuss key differences between memory hierarchies of a mobile device, PC, and server. Use block diagrams to explain your answer. ( 9 marks)**



Memory Hierarchy for a mobile device



Memory Hierarchy for a PC



Memory Hierarchy for a server

**(f) What strategies are used to improve memory hit rates? ( 2 marks)**

1. Reducing the miss rate
2. Reducing the miss penalty