EXPERIMENT 5 LAB REPORT

ECEN 5517 (Spring 2017)
Power electronics and Photovoltaic Power Systems Laboratory

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Objectives

The objectives of this experiment are:

- To design, construct and test an inverter to interface the high-voltage (120 – 200 V) dc bus to a 120 Vrms ac load

Experimental data

Equipments used

Power	**Measurement**
Power Supply: 30V-5A Dual Power Supply	Meters: FLUKE 45 Oscilloscope: TDS3012C

C Code

PWM Generation

- PWM generated using TimerA. The 3 functions below were used to configure the Inverter PWMs

```
void inverter_port_init()
{
    /* TA1. Basically left leg top pulse */
    P3SEL |= BIT6;      // P3.6 to TA0.TA1
    P3DIR |= BIT6;      // P3.6 output

    /* TA2. Basically right leg top pulse */
    P3SEL |= BIT5;      // P3.7 to TA0.TA2
    P3DIR |= BIT5;      // P3.7 output
}
```

```
#define TIMER_60HZ_PRD          26042
#define INVERTER_DUTY           0.4260      // Set for 120Vrms with 150V input
#define INVERTER_LEFT_DUTY      (1-INVERTER_DUTY)*TIMER_60HZ_PRD
#define INVERTER_RIGHT_DUTY     (INVERTER_DUTY)*TIMER_60HZ_PRD

void timerA_initialise()
{
    TA0CCR0 = TIMER_60HZ_PRD;
    TA0CCR1 = INVERTER_LEFT_FUTY;
    TA0CCR2 = INEVRTER_RIGHT_DUTY;

    TA0CCTL1 = OUTMOD_6;                                    // TA1 toggle/set
    TA0CCTL2 = OUTMOD_2;                                    // TA2 toggle/reset

    TA0CTL = TASSEL__SMCLK + ID__8 + MC_3 + TACLR;          // SCLK, divide clk_src/8, up_down mode
}

void inverter_set_duty(uint16_t duty_counts)
{
    TA0CCR1 = TIMER_60HZ_PRD-duty_counts;
    TA0CCR2 = duty_counts;
}
```

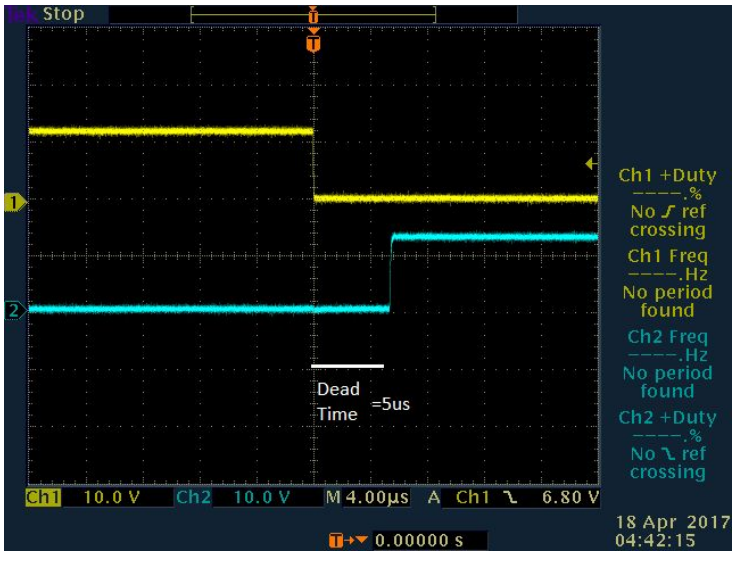
Boost Reference

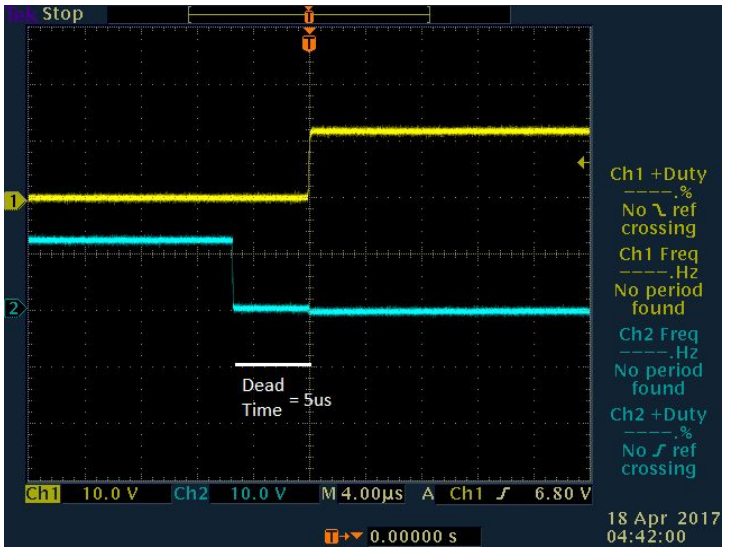
- The boost reference was set using the 50KHz PWM on Timer D1 of the MSP430. The DC value of the PWM corresponds to the boost reference. This DC value was extracted using an R-C low pass with a corner placed at 500Hz

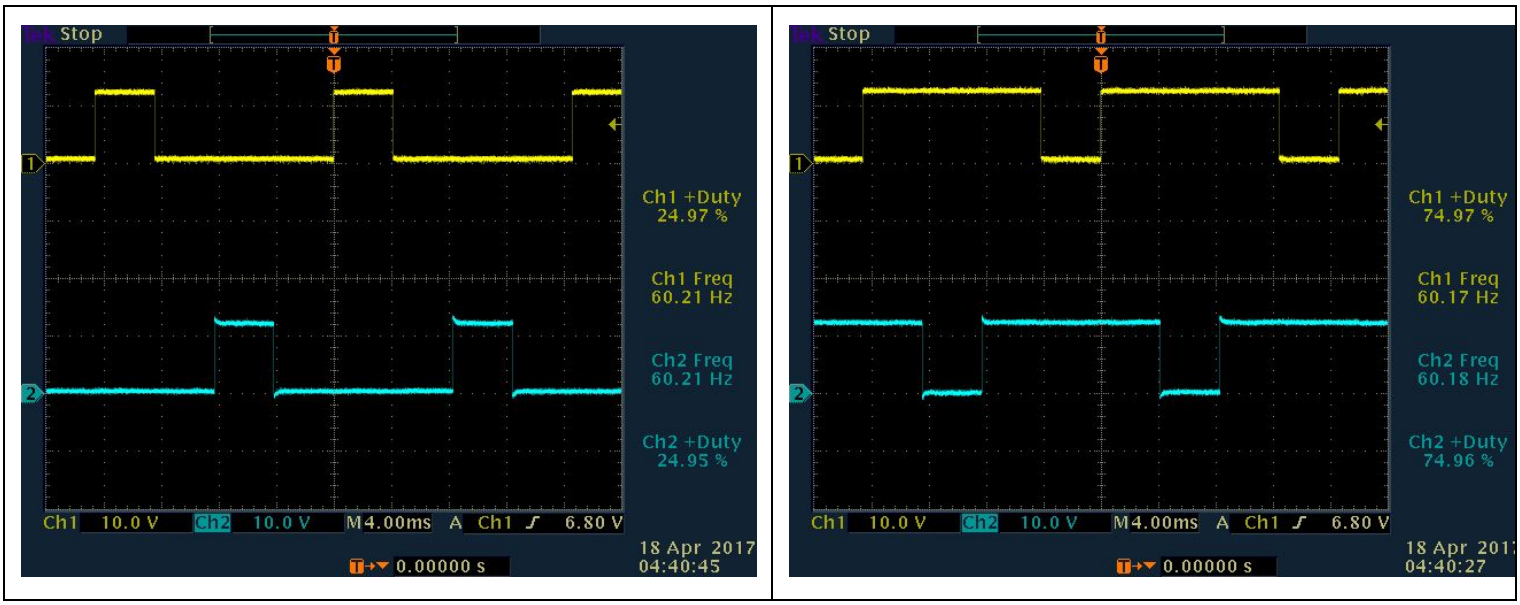
```
void timerD_initialise()
{
    /* Timer D1 configured to use high resolution mode */
    TD1CTL0 = TDSSEL_2;                       // TDCLK=SMCLK=25MHz=Hi-Res input clk select
    TD0CTL1 |= TDCLKM_1;                      // Select Hi-res local clock
    TD0HCTL1 |= TDHCLKCR;                     // High-res clock input >15MHz
    TD0HCTL0 = TDHM_0 +                       // Hi-res clock 8x TDCLK = 200MHz
    TDHREGEN +                                // Regulated mode, locked to input clock
    TDHEN;                                    // Hi-res enable

    __delay_cycles(500000);
    while(!TDHLKIFG);                        // Wait until hi-res clock is locked

    TD1CCR0 = 4000;                           // PWM Period. So sw freq = 200MHz/4000 = 50kHz
    TD1CCTL1 = OUTMOD_6 + CLLD_1;             // CCR1 toggle/set
    TD1CCR1 = 0;
    TD1CTL0 |= MC_1 + TDCLR;                  // up-mode, clear TDR, Start timer
}

void boost_set_ref(uint16_t duty_counts)
{
    TD1CCR1 = duty_counts;
}
```

Gate Drive Signals and Deadtime

200K Rd was used



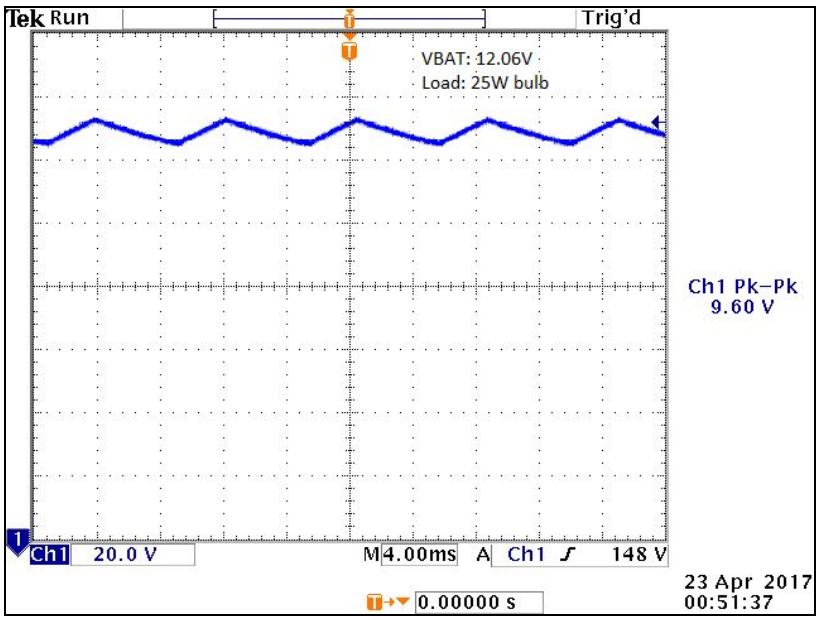




HVDC control

- PWM average to HVDC scaling: 66.67 (i.e 3.3V on MSP430 PWM (average value) corresponds to 220V on the HVDC bus)

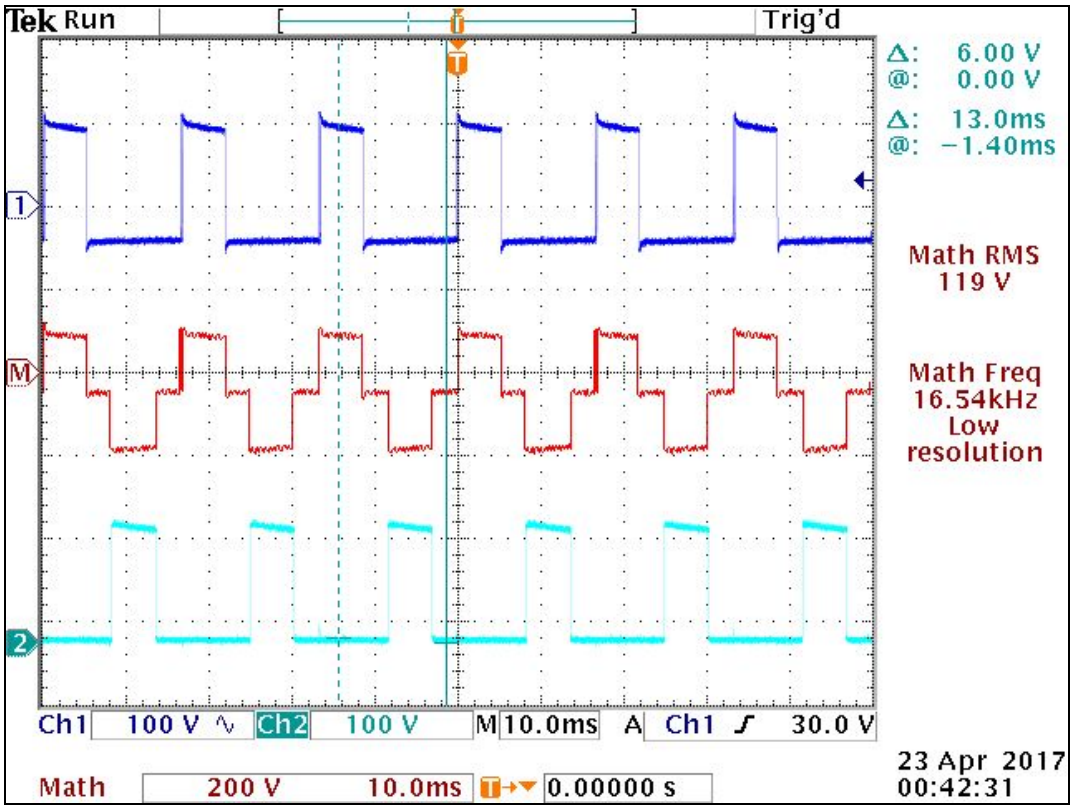
PWM set point (Vavg V)	HVDC reference (V)	HVDC measured value (V)
2.25	150.0	151.3



Low HVDC (V_{HVDC} = 130V; D = 0.42)

Vin (Boost)	Iin (Boost)	Pin	Vout (AC)	Iout (AC)	Pout (W)	Efficiency
12.49	2.165	27.04085	121.3	0.21	25.473	0.942

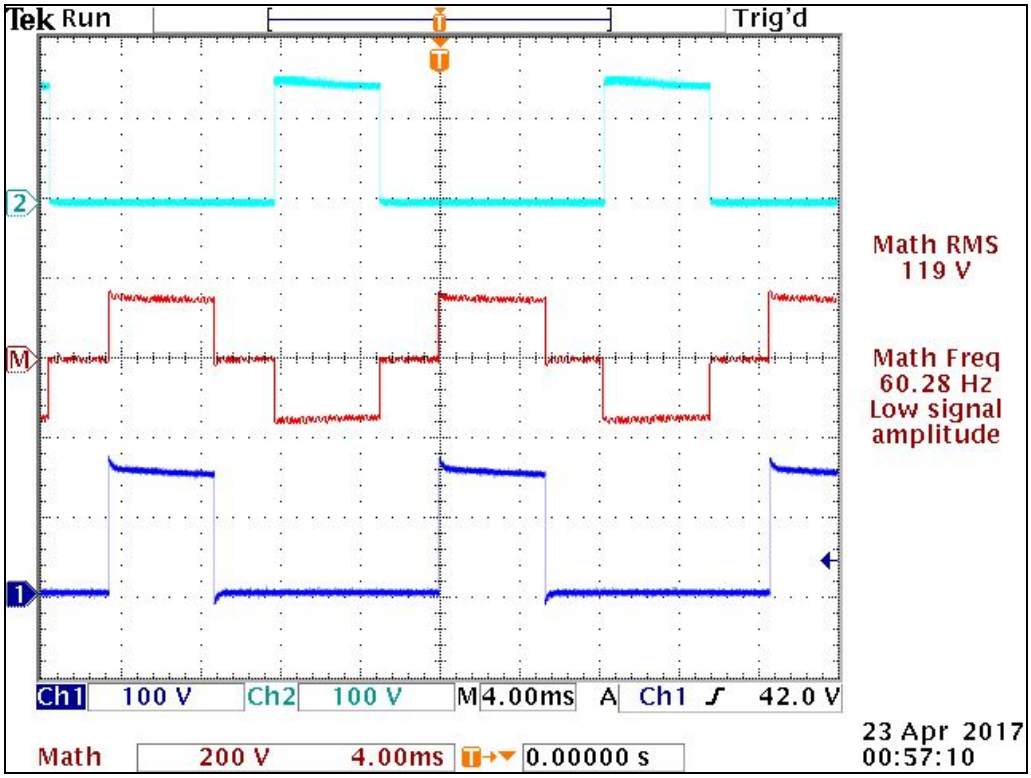
Differential Waveforms across Light Bulb (Pout = 25W, Vin = 12.49V)



High HVDC (V_{HVDC} = 150V; D = 0.32)

Vin	Iin	Pin	Vout (AC)	Iout (AC)	Pout (W)	Efficiency
12.07	2.212	26.7	118.3	0.215	25.43	0.953

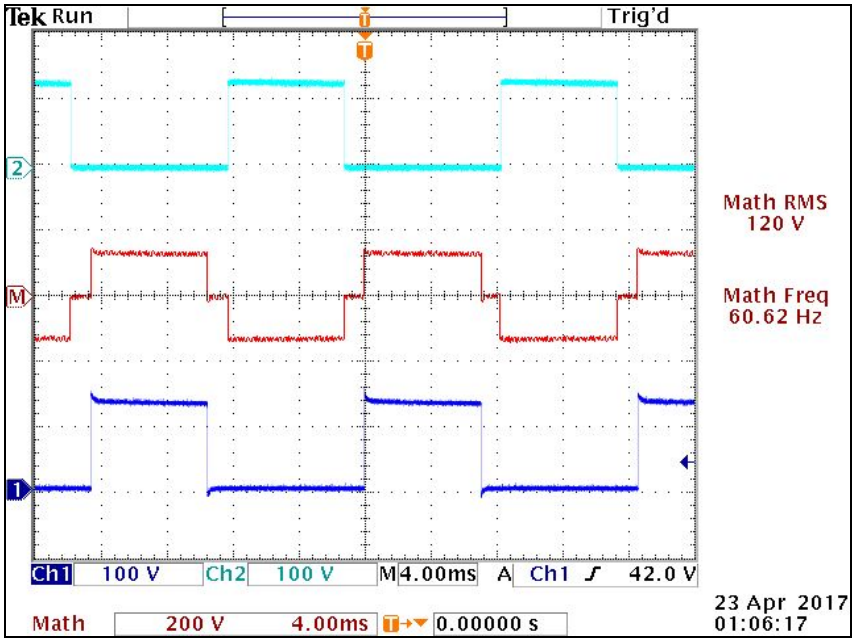
Differential Waveforms across Light Bulb (Pout = 25W, Vin = 12.07V)



Inverter Tests with battery and 25W bulb load (V_{HVDC} = 150.0V)

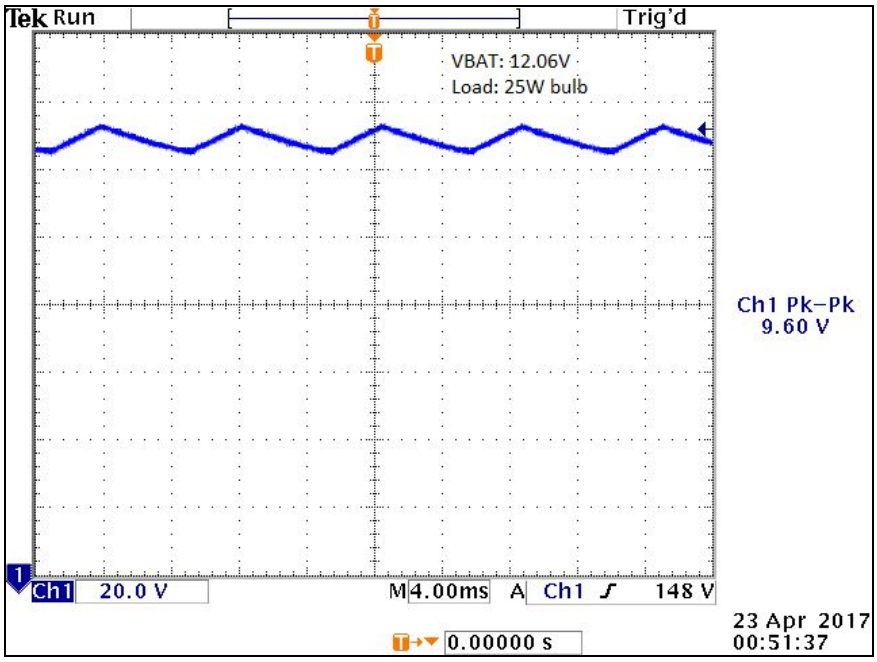
Vin	Iin	Pin	V(HVDC)	Duty	Vout (AC)	Iout (AC)	Pout (W)	Efficiency
12.25	2.194	26.88	151.3	0.31	120.6	0.213	25.69	0.956

Differential Waveforms across Light Bulb (Pout = 25W, Vbat = 12.25V)



HVDC waveform with Pout = 25W, Vbat = 12.25, HVDC_ref = 150.0V

HVDC Average: 148.0V



Theoretical and Measured HVDC comparison

$$V_{RMS} = \sqrt{D_H} * V_{HVDC}$$
$$D_F = D_H/2$$

Operating conditions: 150V HVDC; 120 Vrms

Theoretical Duty Cycle (D_F)	Measured Duty Cycle (D_F)
0.32	0.34

Extra Credit: Pure Sine wave inverter

Inductor Design

- 5 inductors in total were used
- 4 Toroidal cores and one PQ26-25 core

TOROIDAL CORES:

- The toroidal cores used were 28B0500 Laird cores
- A 23 AWG Gauge was used for the windings. The core was wound with maximum possible turns

PQ26-25 Core

- Air gap: 0.0296mm
- Gauge: 23 AWG Maximum possible turns

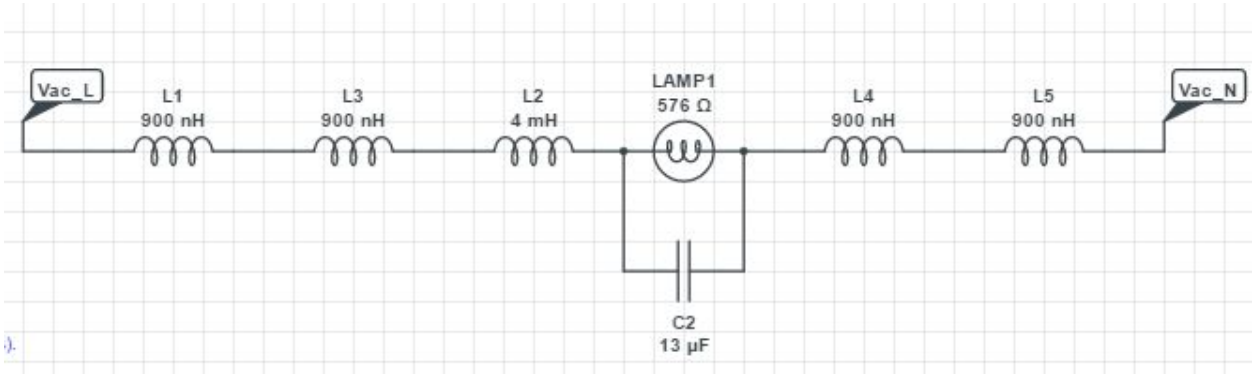
Measured Inductance

Toroidal	0.9mH
PQ26-25	4mH
Total (4*Toroidal + PQ26-25)	7.6 mH

Filter Capacitance

- 13 1uF 250V ceramic capacitors in parallel

- Total capacitance = 13uF



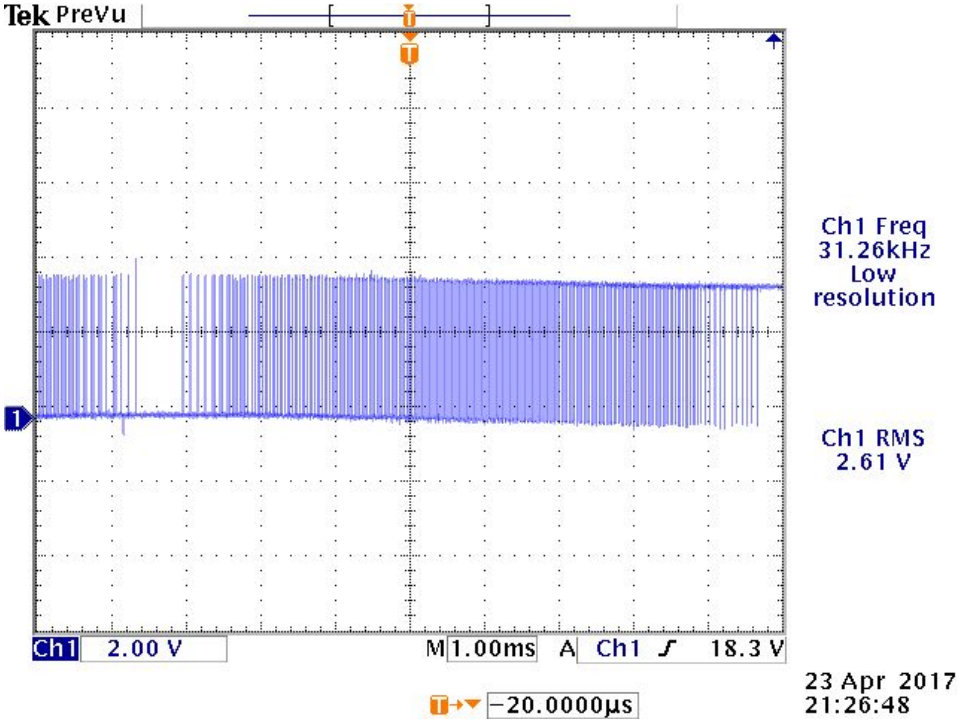
Pulse Generation for pure sine wave inverter

- The 60Hz sine wave divided into 64 samples. Thus sampling frequency is 60*64 = 3840Hz. Timer D1 generates an interrupt at this frequency
- The sine wave carrier frequency (i.e MOSFET switching frequency) was set to 25KHz. The duty cycle was sine modulated using the QsinPU function in the MSP430 Qmath library. Timer D0 CCR0, CCR1 and CCR2 were used for Inverter pulse generation
- The pulse scheme was used was (**Bipolar Modulation**)

```
void timerD_initialise()
{
    // Configure TimerD in Hi-Res Regulated Mode
    TD0CTL0 = TDSSEL_2;                       // TDCLK=SMCLK=25MHz=Hi-Res input clk select
    TD0CTL1 |= TDCLKM_1;                      // Select Hi-res local clock
    TD0HCTL1 |= TDHCLKCR;                     // High-res clock input >15MHz
    TD0HCTL0 = TDHM_0 +                       // Hi-res clock 8x TDCLK = 200MHz
    TDHREGEN +                                // Regulated mode, locked to input clock
    TDHEN;                                    // Hi-res enable

    __delay_cycles(500000);
    while(!TDHLKIFG);                         // Wait until hi-res clock is locked

    // Configure the CCRx blocks
    TD0CCR0 = 6667;                           // PWM Period. So sw freq = 200MHz/6667 = 25 kHz
    TD0CCTL1 = OUTMOD_6 + CLLD_1;             // CCR1 toggle/set
    TD0CCR1 = 0;                              // CCR1 PWM duty cycle of 1000/2000 = 50%
    TD0CCTL2 = OUTMOD_2 + CLLD_1;             // CCR1 toggle/reset
    TD0CCR2 = 0;                              // CCR1 PWM duty cycle of 1000/2000 = 50%
    TD0CTL0 |= MC_1 + TDCLR;                  // up-mode, clear TDR, Start timer

    /* Timer D1 generates a 3840 KHz sampling interrupt */
    TD1CCTL0 = CCIE;
    TD1CCR0 = 3255;
    TD1CTL0 = TDSSEL_2 + MC_1 + TDCLR;          // Clock source 25MHZ (SMCLK)
}
```

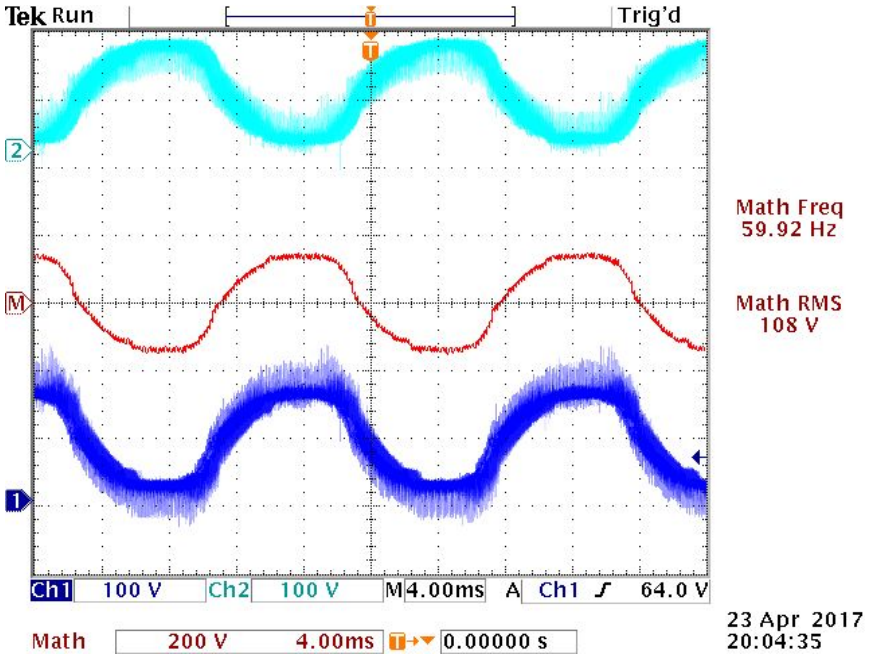
```
int16_t theta = 0;
int16_t idx = 0;
#pragma vector=TIMER1_D0_VECTOR
__interrupt void TIMER1_D0_ISR (void)
{
    int16_t sinPU;
    P1OUT ^= BIT3;
    if(idx == 64)
    {
        idx = 0;
        theta = 0;
    }
    theta += _Q15(0.015625);
    sinPU = (_Q15mpy(_Q15sinPU(theta),_Q15(0.49))) + _Q15(0.5);
    idx++;
    TD0CCR1 = _Q15rmpy(sinPU,TD0CCR0);
    TD0CCR2 = TD0CCR1;
    TD1CCTL0 &= ~CCIFG;
}
```

Timer D0 Inverter waveforms



Pure Sine wave Inverter waveforms

Differential H-Bridge output with high frequency PWM

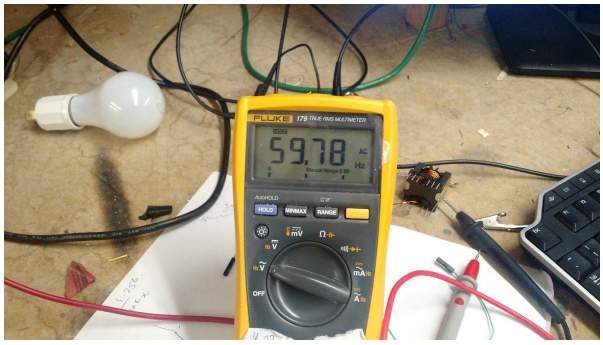


V_{HVDC}: 170V
V_{AC}: 110 Vac

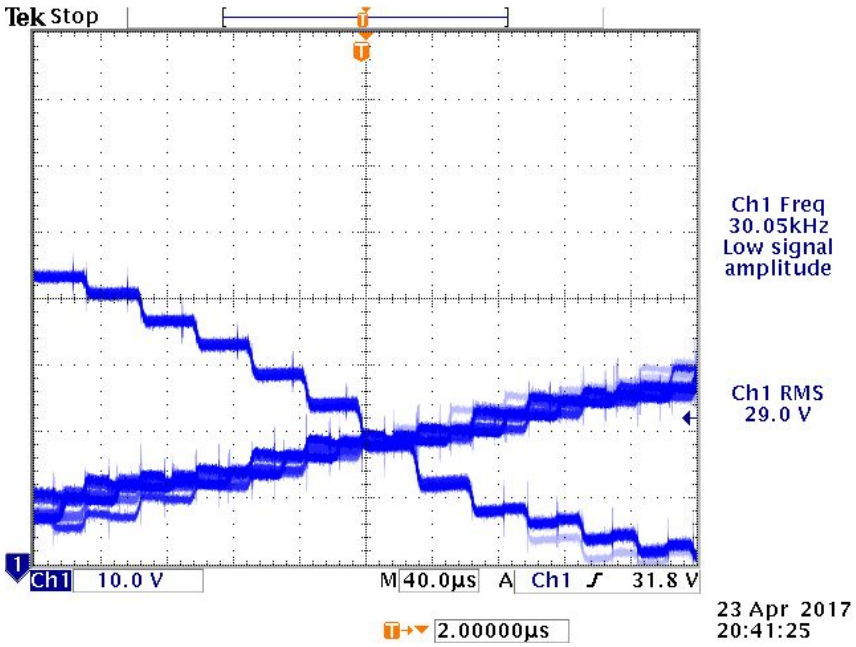
Meter Readings for the Inverter

Output voltage (Vrms)

Output frequency (Hz)



Output Ripple



The AC ripple on the output waveform is shown on the left.

Peak AC ripple: ~5Vpp

Since the ripple is higher than 2 Vpp “Kill-A-Watt” measurements were not taken

Conclusion

- A Modified Sine-Wave Inverter was designed and interfaced with 150V Boost DC bus and interfaced to a 120 V_{RMS} AC load
- The switching scheme of the above inverter was modified to generate a pure sine-wave output. An output LC filter was also designed to filter out high frequency switching harmonics.
- Pure sine wave operation was verified for 110V AC output and interfaced with 25W light bulb load