ECEN 4517/5517

Power Electronics and Photovoltaic Power Systems Laboratory

Lecture 3

DC-DC Converter

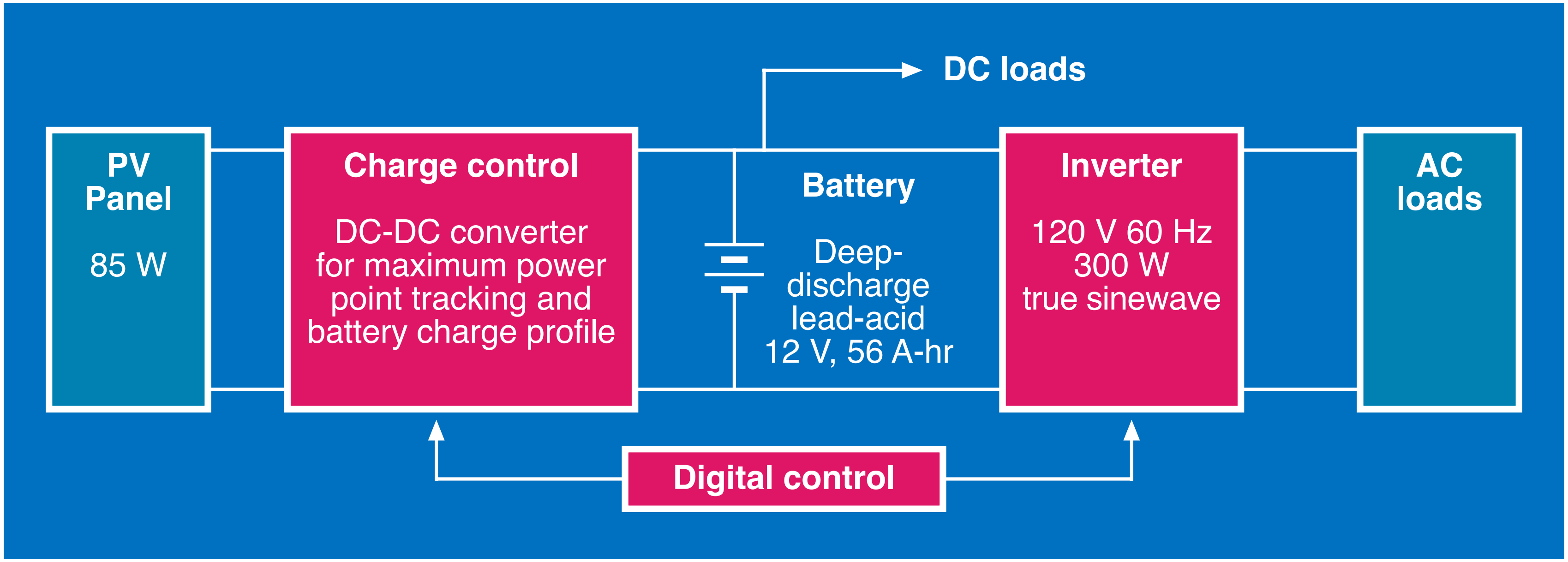
Announcements

- This week's lab: Experiment 3-1
  - Lab Assignment and related documents posted on D2L
  - Experiment 3-1 had a pre-lab
  - Have 3 weeks to work on Experiment 3-1
  - Exp 3-1 Lab Report due by 11:59 pm (MT) on Friday February 24, 2017

- After this: Experiment 3-2
  - Experiment 3-2 has a pre-lab (due 11:59 pm, Friday February 17, 2017)
  - Have 2 weeks to work on Experiment 3-2
  - Exp 3-2 Lab Report due by 11:59 pm (MT) on Friday March 10, 2017

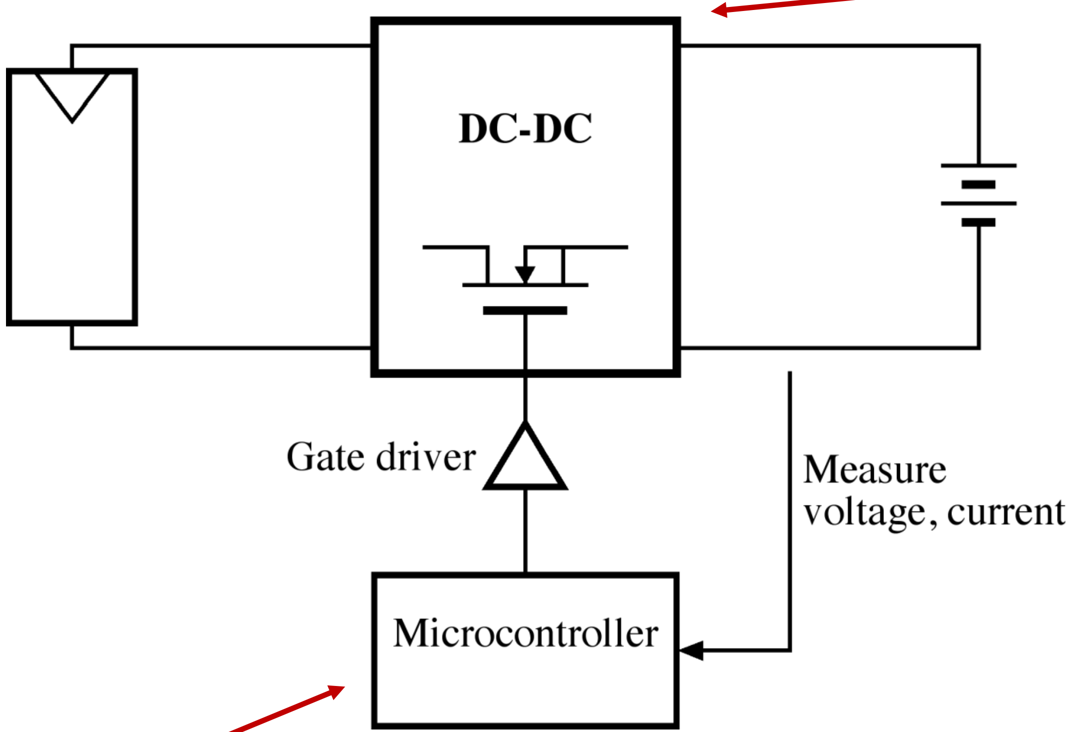
- Turn in all Pre-Lab Assignments and Lab Reports as pdf files

Experiments



- Exp 1 – PV panel and battery characteristics and direct energy transfer
- Exp 2 – TI MSP430 microcontroller introduction
- Exp 3-1, 3-2 – Buck dc-dc converter for PV MPPT and battery charge control
- Exp 4 – Step-up 12V-200V dc-dc converter
- Exp 5 – Single-phase dc-ac converter (inverter)
- Expo – Complete system demonstration

Experiments 2 and 3



Exp 3: DC-DC Converter

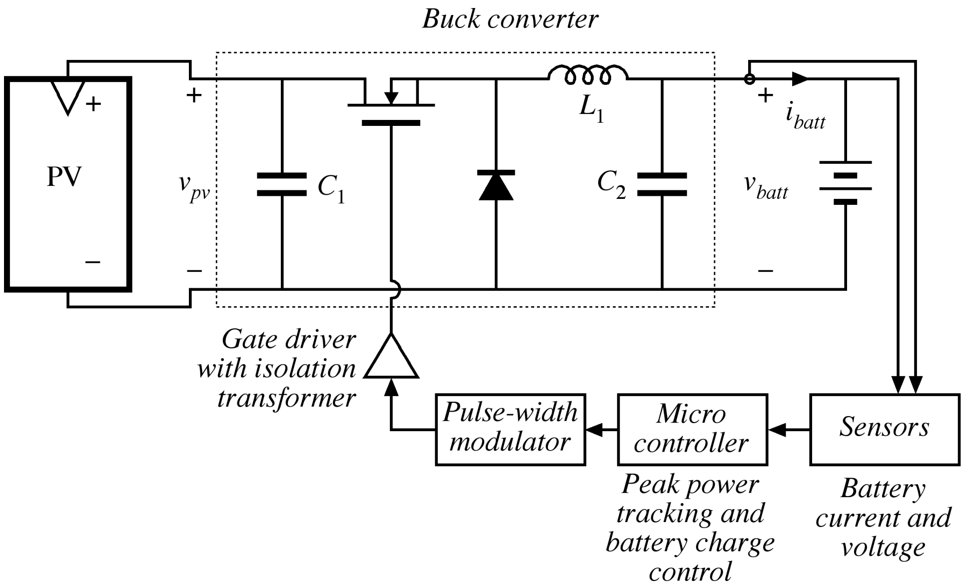
- Exp 3-1: Design and construct dc-dc converter
- Exp 3-2: Employ microcontroller to achieve MPPT and battery charge control

Exp 2: Introduction to MSP430 Microcontroller

- Learn to use TI MSP430 microcontroller
- Set up your MSP430 to drive a MOSFET at a programmable duty cycle

Experiments 3-1 and 3-2

- Experiment 3-1
  - Demonstrate dc-dc converter power stage operating open loop, driven by MSP430 PWM output
  - Inside, with input power supply and resistive load
  - Outside, between PV panel and battery
  - DC system simulation



- Experiment 3-2
  - Demonstrate working sensor circuitry, interfaced to microprocessor
  - Demonstrate peak power tracker and battery charge controller algorithms, outside with converter connected between PV panel and battery

Experiment 3-1 Pre-lab

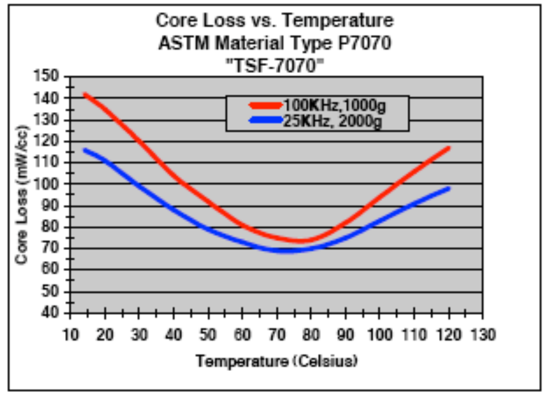
- Design buck converter power stage
  - Determine current waveforms of each component: MOSFET, diode, inductor, capacitors (C_1 and C_2)
  - Design the inductor
    - Use K_g method - you decide how much ripple, loss, etc. to allow
  - Select other components: MOSFET, diode, capacitors (C_1 and C_2)
    - Choose components that operate within their datasheet specified ratings
      - MOSFETs: peak voltage, average current
      - Diodes: peak reverse voltage, average current
      - Capacitors: maximum working voltage, rms current
    - Wise to apply derating factors to many datasheet limits
      - Example: 75% of datasheet max voltage value for power semiconductor devices (use worst-case peak transient voltage)

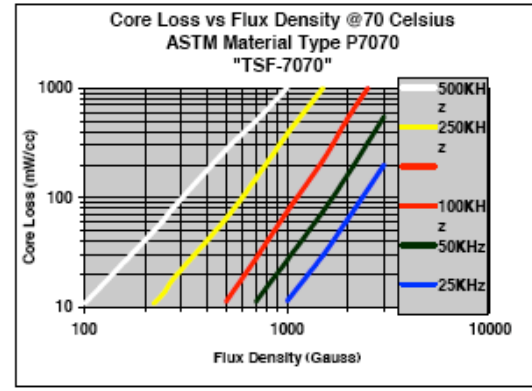
- Contents of last year's parts kit and links to their datasheets are at: http://ecee.colorado.edu/ecen4517/components/kit.html

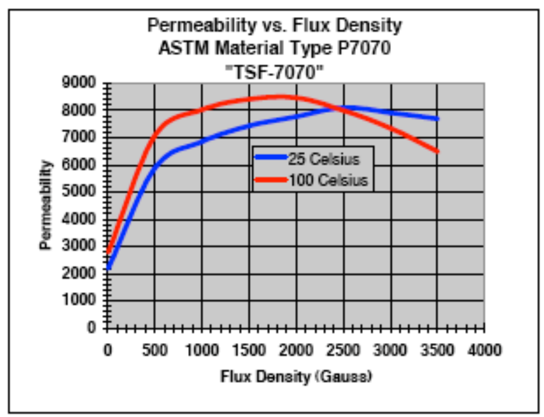
Core Material and Geometries

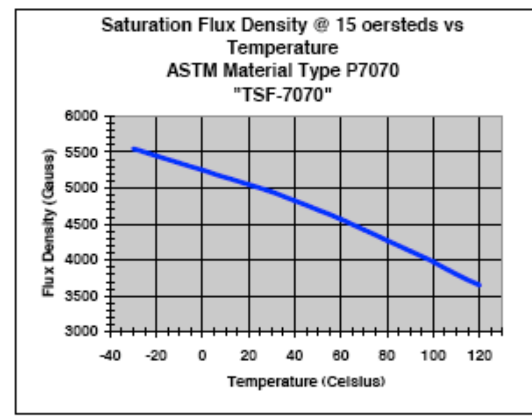
- Kit includes ferrite cores from TSC Ferrite made of TSF-7070 material
- Following core geometries included in the kit:
  - PQ 32/20
  - PQ 26/25
  - 13-07-06 toroid

ASTM Material Type P7070
TSC Ferrite Material Grade TSF-7070
Low Core Loss, minimum at 70 Celsius
Initial Permeability 2,200 +-20%
Curie Temperature >210 Celsius
Core Loss Density = $P_c = 0.147\ f^{1.34}\ B^{2.54}$ in mW/cc at 70 Cesius



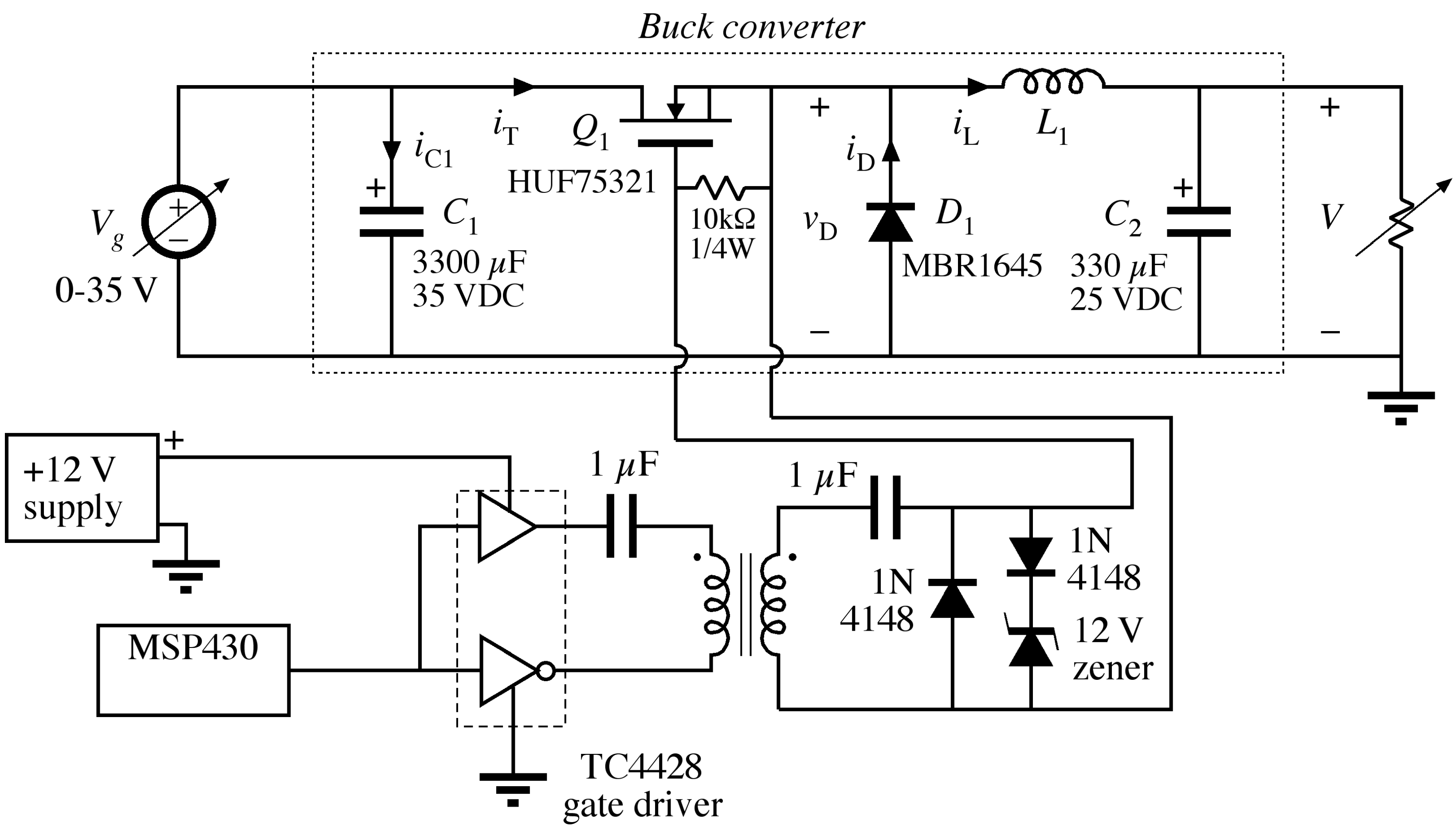






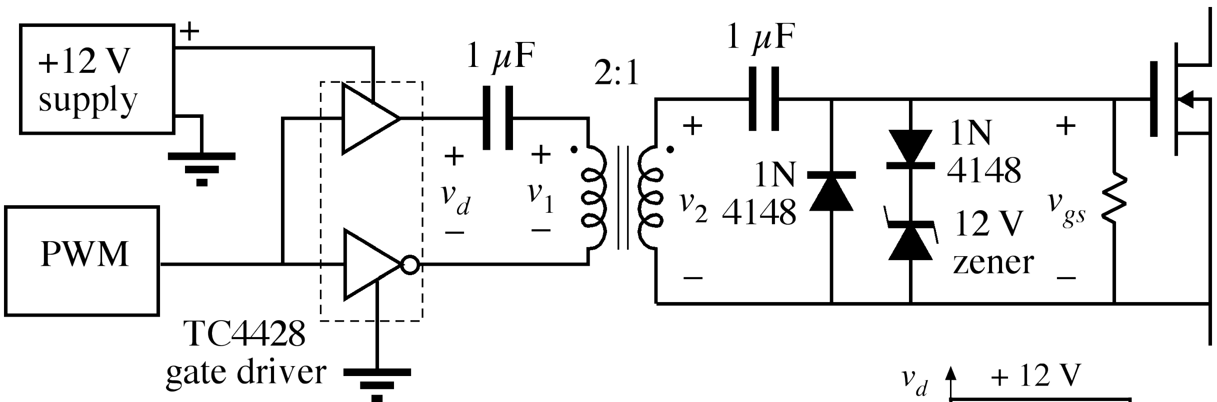
Experiments 3-1 Week 1

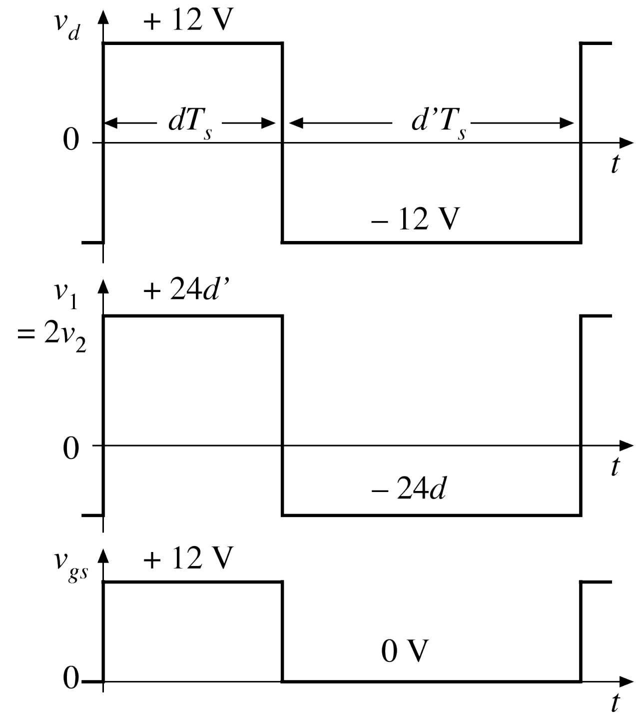
- Demonstrate dc-dc converter power stage inside



Gate Drive Circuit Option 1

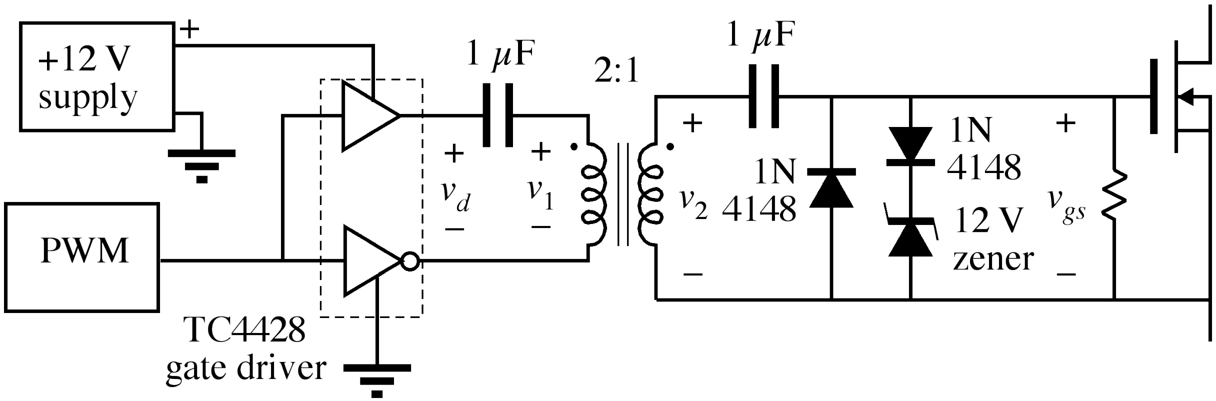
Gate Drive Circuit with Transformer Isolation





- Gate driver output $v_d(t)$ has a dc component when $d \neq 0.5$
- Transformer will saturate if we apply dc
- Primary blocking capacitor removes dc component
- Secondary capacitor and diodes form a diode clamp circuit that restores the dc component

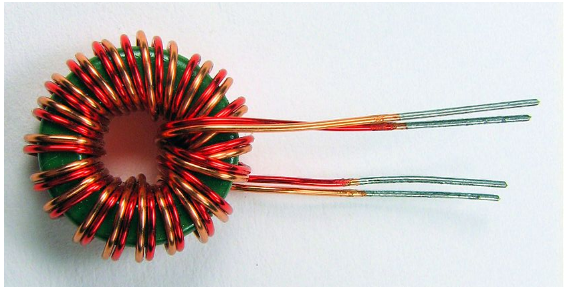
Gate Drive Circuit Option 1 – Transformer Design

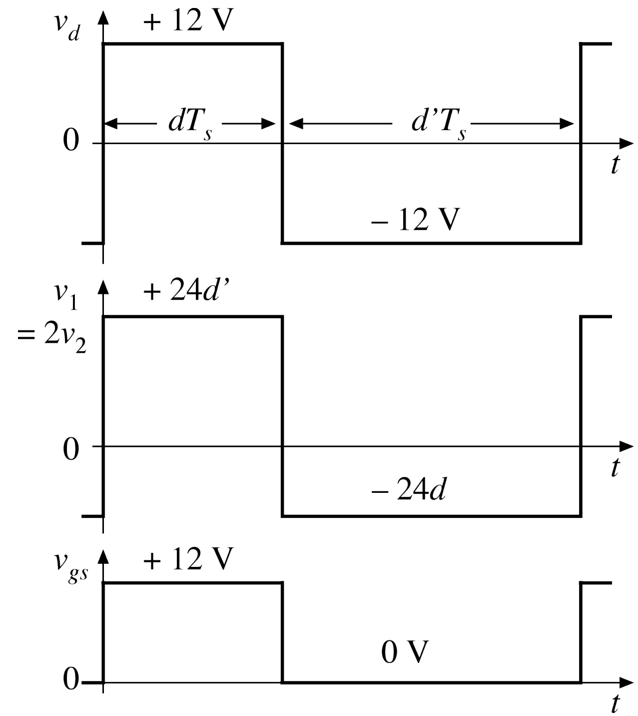


- Use ferrite toroid in your kit
- Need enough turns so that applied volt-seconds do not saturate core:

$$\Delta B = V_1 D T_s / N_1 A_c$$

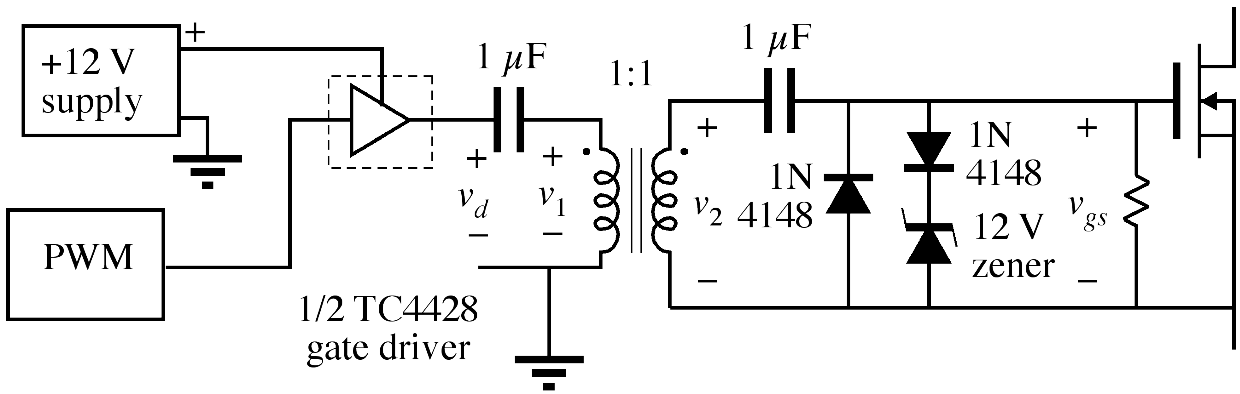
- Leakage inductance is minimized if bifilar winding is used



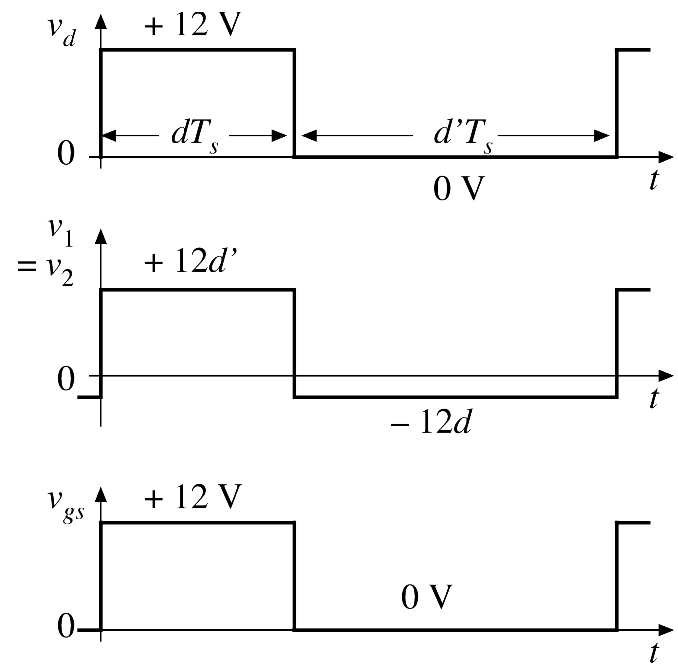


Gate Drive Circuit Option 2

Gate Drive Circuit with One Driver and Transformer Isolation

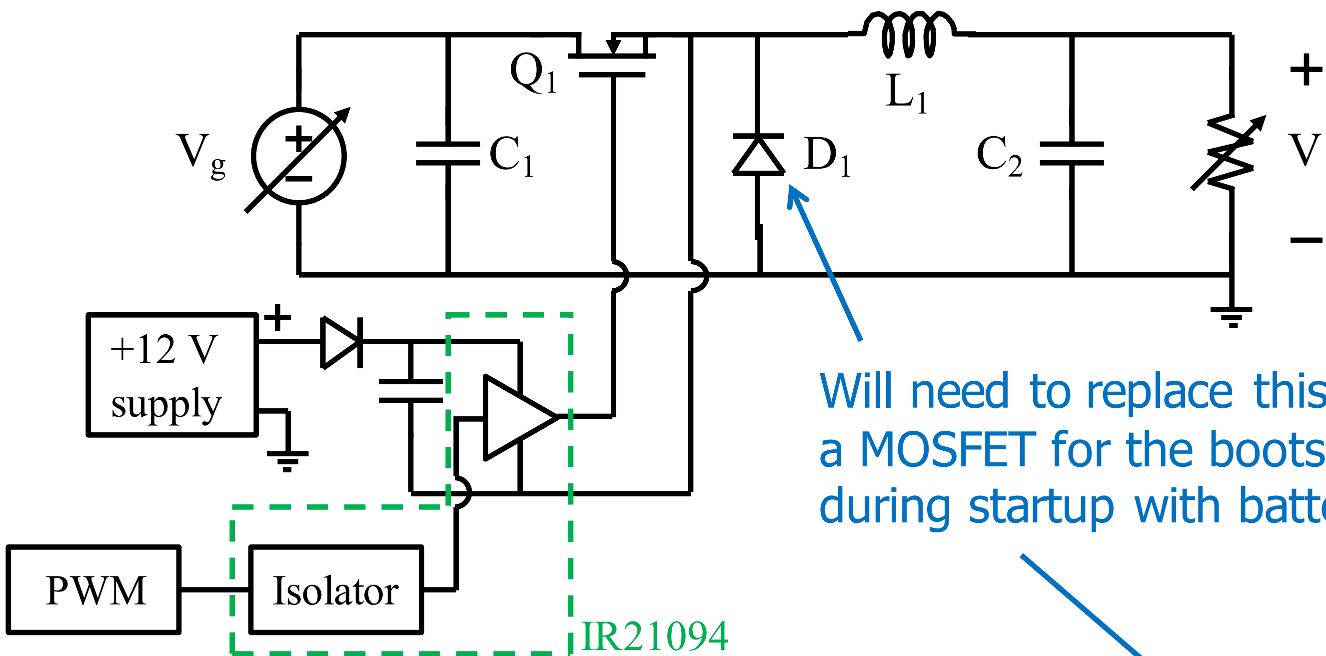


- Uses only one gate driver instead of two, to produce half the voltage swing on primary
- Transformer turns ratio is 1:1
- Produces half as much gate current
- Suitable for smaller MOSFETs

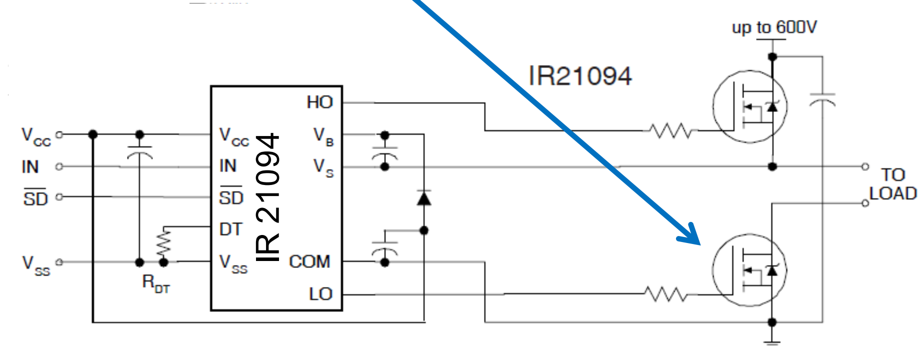


Gate Drive Circuit Option 3

Gate Drive Circuit using Bootstrapped High Side Driver

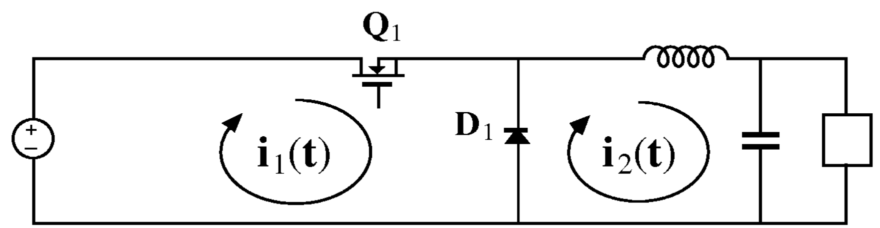


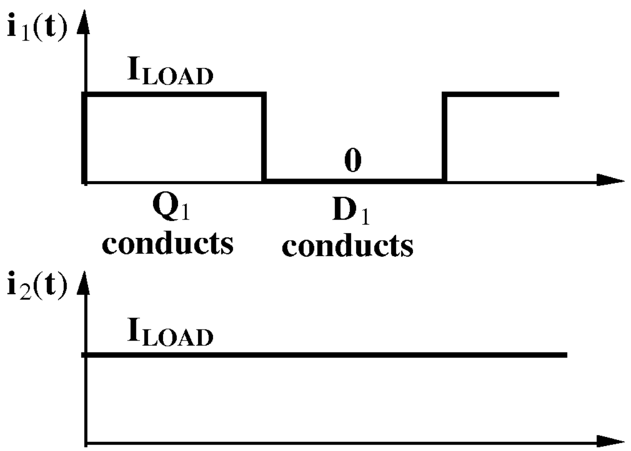
Will need to replace this diode D_1 with a MOSFET for the bootstrap to work during startup with battery as the load



- Can use IR21094 Half Bridge Driver

Buck Converter Layout Issues





switched input current $i_1(t)$ contains large high frequency harmonics

—hence inductance of input loop is critical

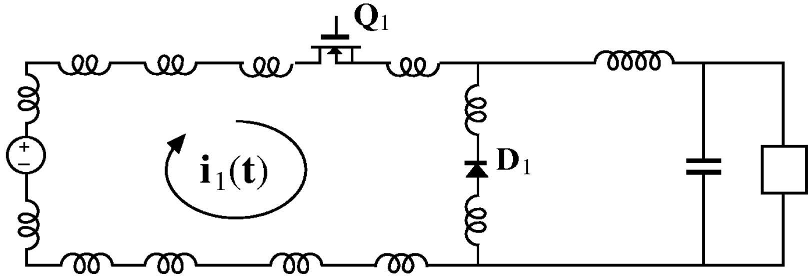
inductance causes ringing, voltage spikes, switching loss, generation of B- and E-fields, radiated EMI

the second loop contains a filter inductor, and hence its current $i_2(t)$ is nearly dc

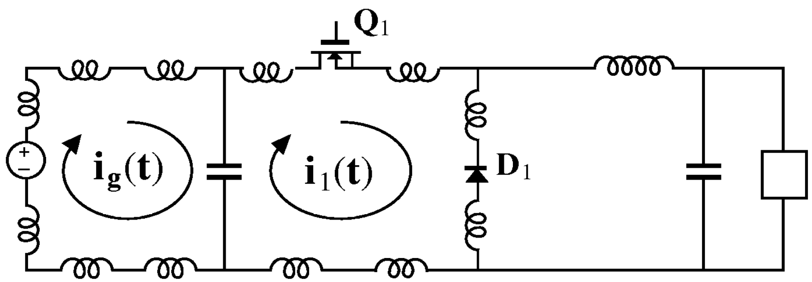
—hence additional inductance is not a significant problem in the second loop

Buck Converter Layout Best Practice

Parasitic inductances of input loop explicitly shown:



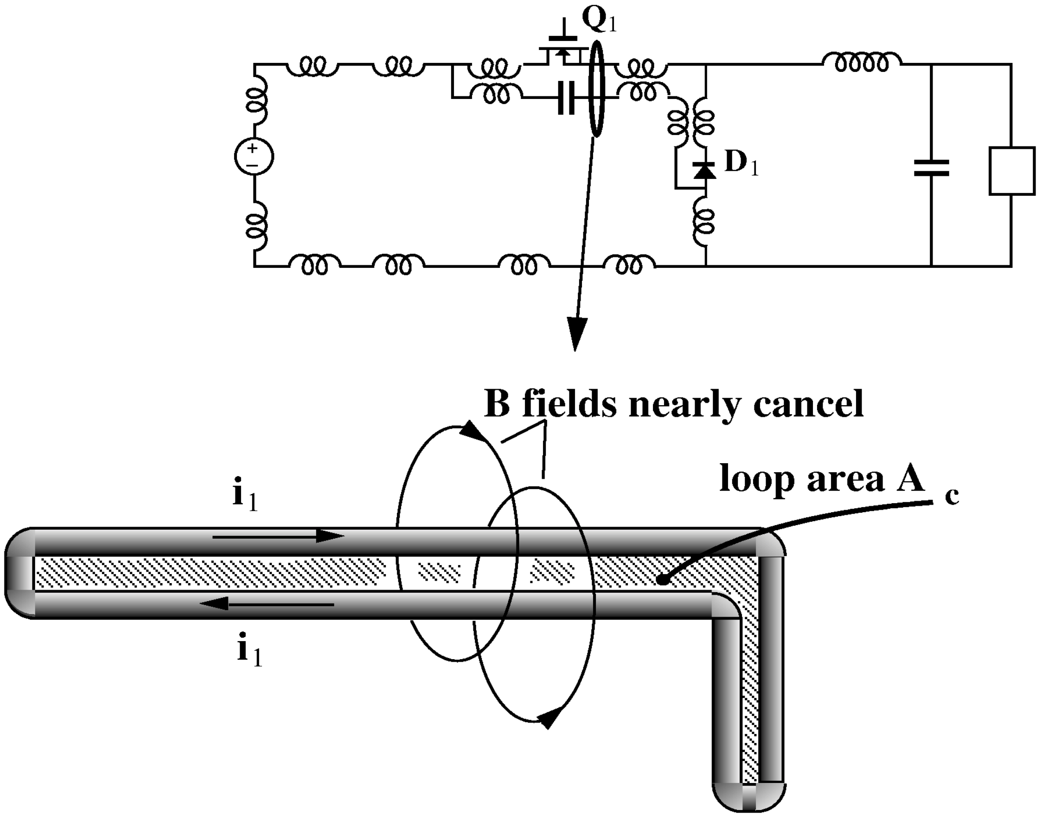
Addition of bypass capacitor confines the pulsating current to a smaller loop:



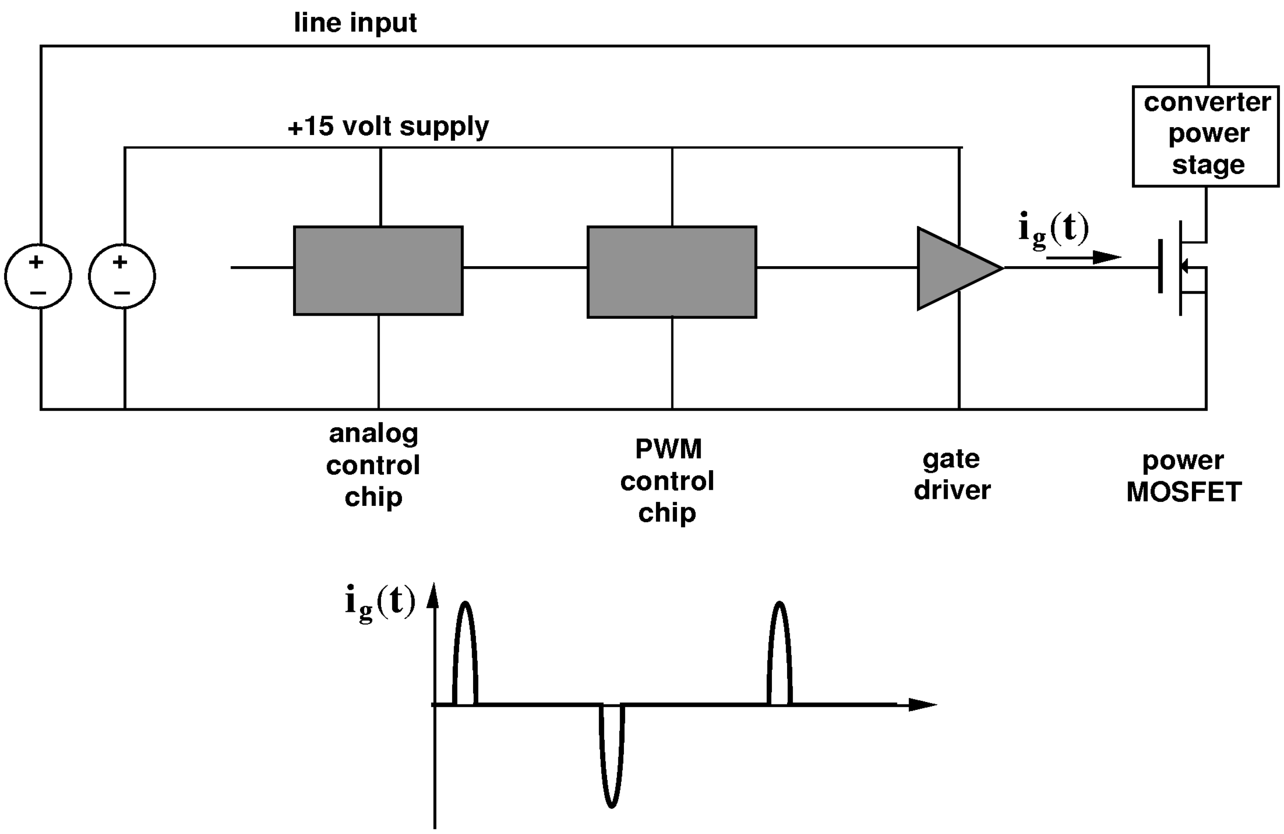
high frequency currents are shunted through capacitor instead of input source

Buck Converter Layout Best Practice (Cont.)

Even better: minimize area of the high frequency loop, thereby minimizing its inductance

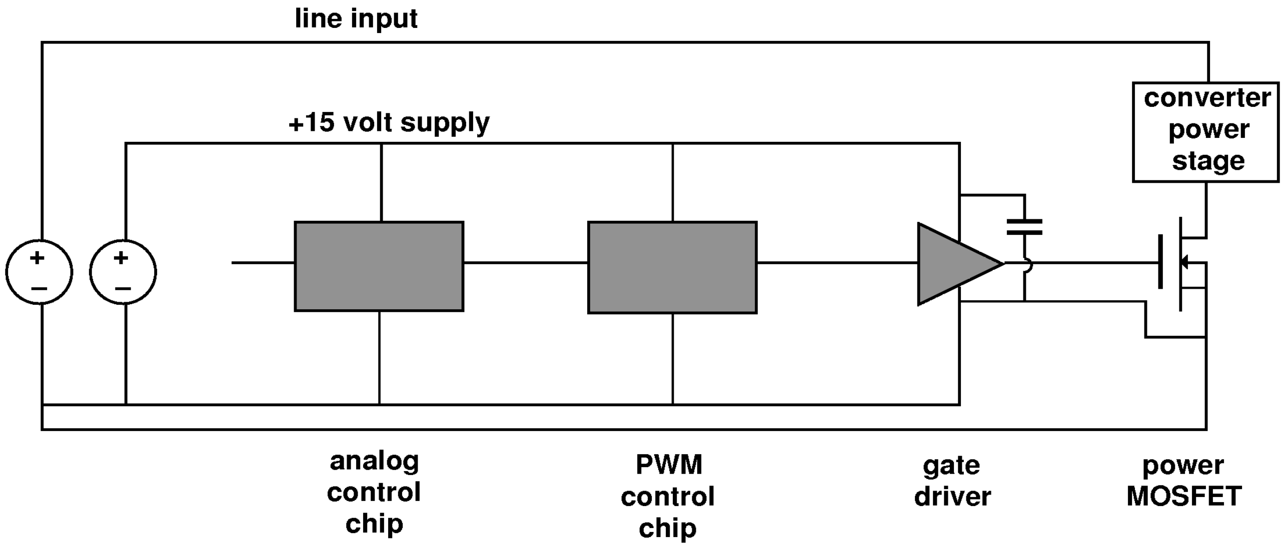


Gate Driver Layout Issues



Gate Driver Layout Best Practice

Solution: bypass capacitor and close coupling of gate and return leads

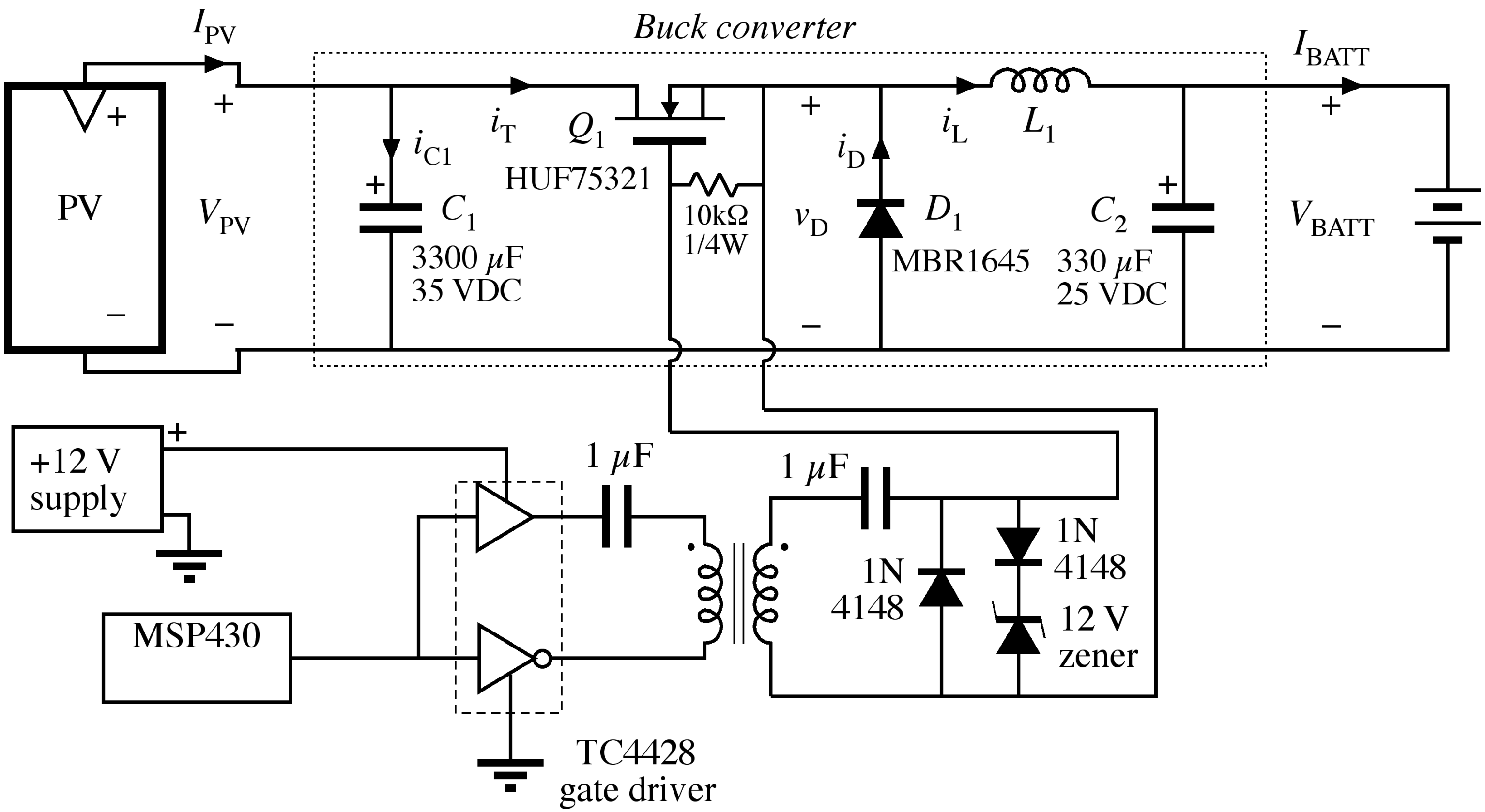


High frequency components of gate drive current are confined to a small loop

A dc component of current is still drawn output of 15V supply, and flows past the control chips. Hence, return conductor size must be sufficiently large

Experiments 3-1 Week 2

- Demonstrate dc-dc converter power stage outside



- Explore how duty ratio controls the PV and battery voltages and currents