ECEN 4517/5517

Power Electronics and Photovoltaic Power Systems Laboratory

Lecture 7

Cascaded Boost Converter using

Analog Pulse Width Modulator

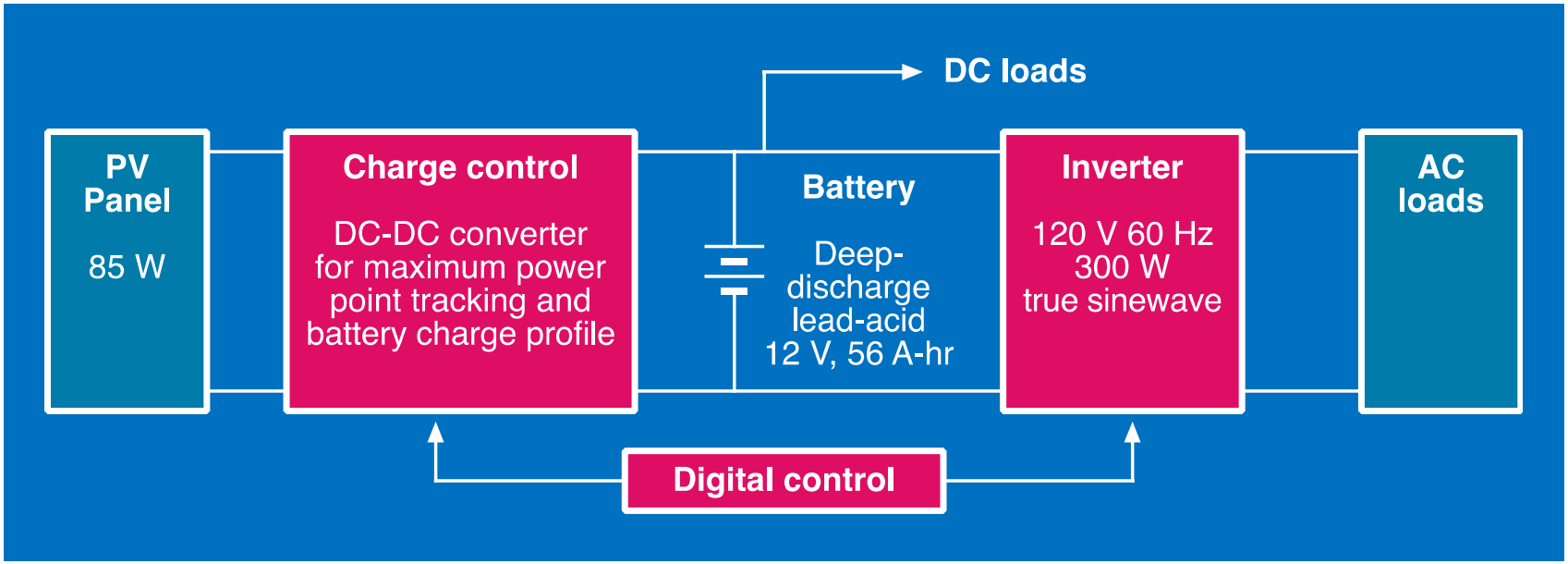
Announcements

- Exp 3-2 Lab Report due by 11:59 pm (MT) on Friday March 10, 2017

- This week's lab: Start Experiment 4
  - Have 3 weeks to work on Experiment 4
  - Exp 4 Lab Report due by 11:59 pm (MT) on Friday April 7, 2017

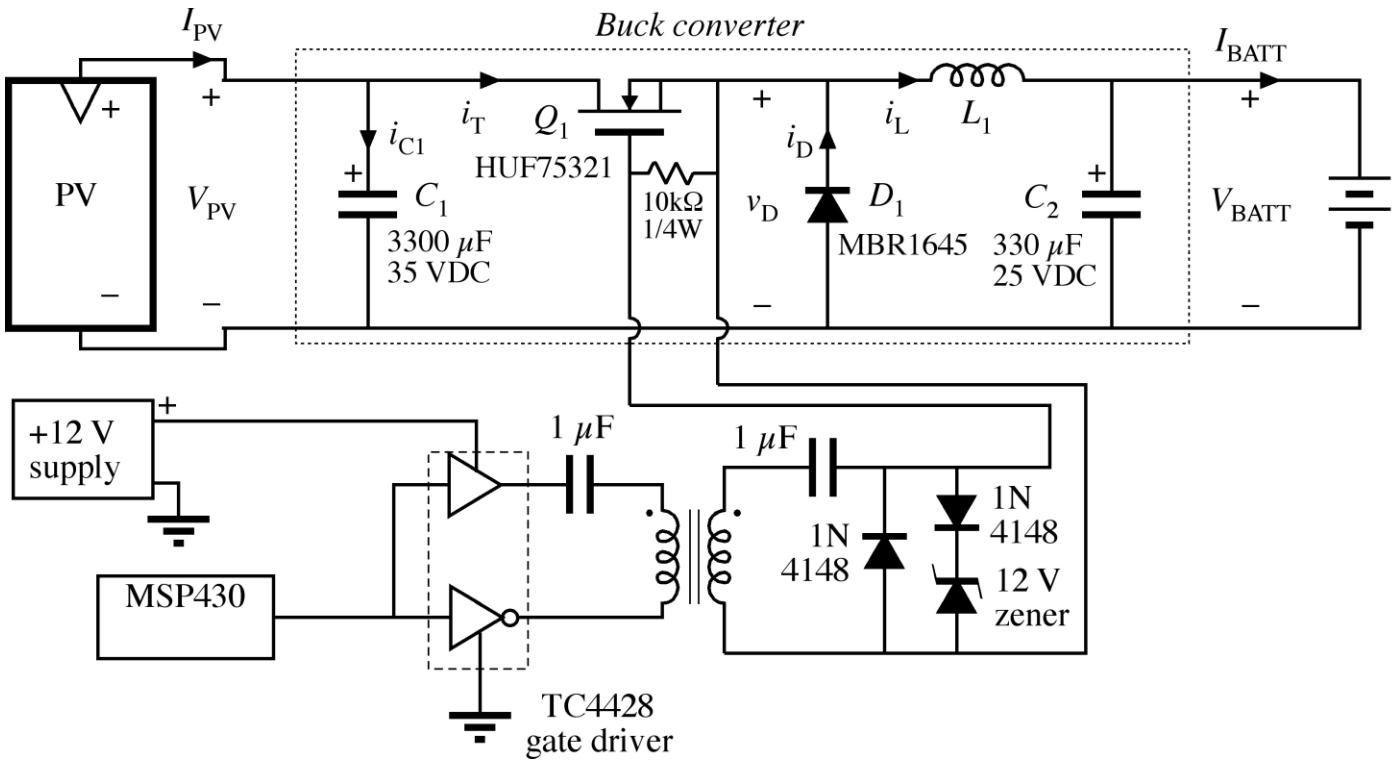
- Following this: Experiment 5
  - Experiment 5 has a pre-lab (due 11:59 pm on Friday March 24, 2017)
  - Have 2 weeks to work on Experiment 5 (after Spring Break)
  - Exp 5 Lab Report due by 11:59 pm (MT) on Friday April 21, 2017

Experiments



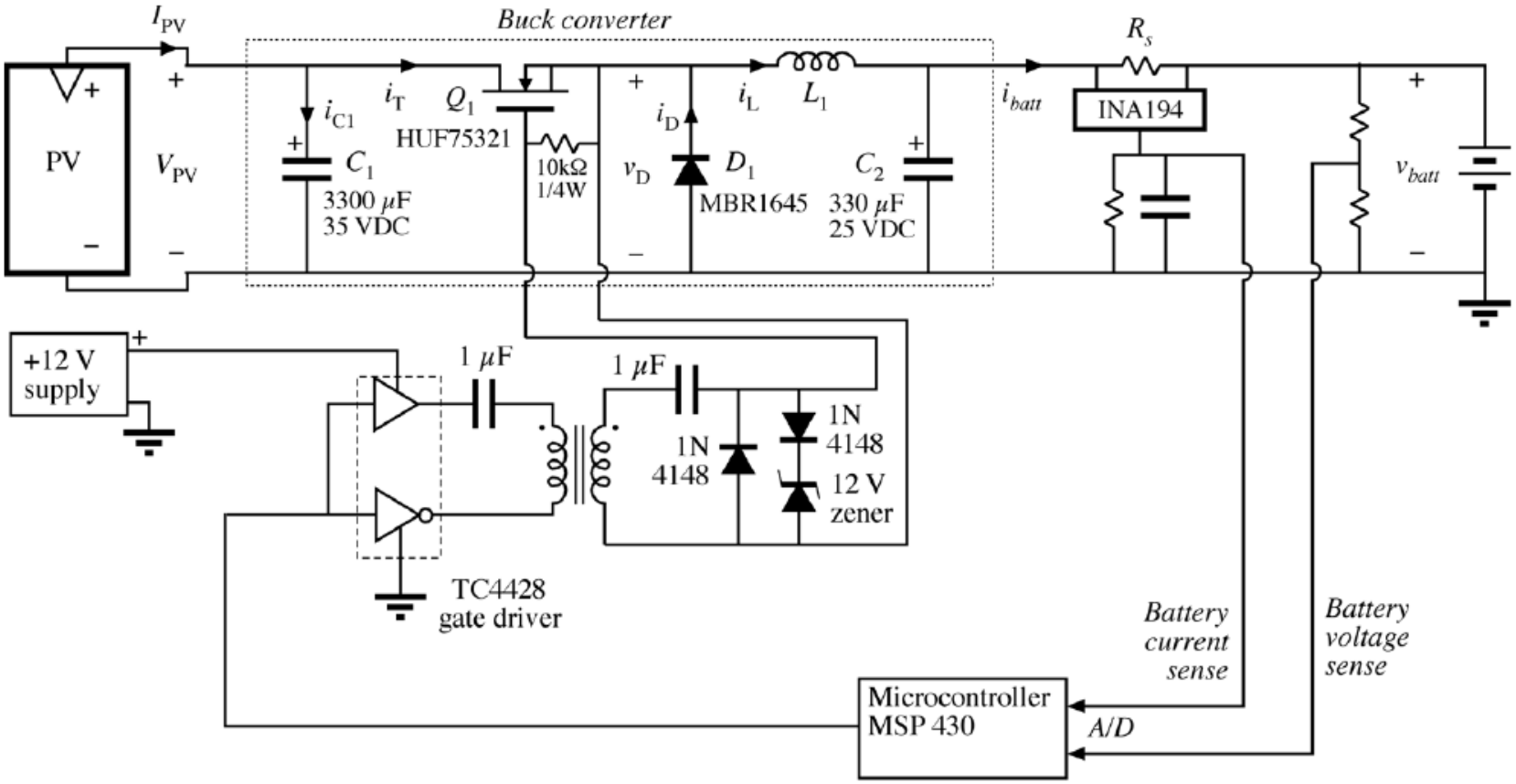
- Exp 1 – PV panel and battery characteristics and direct energy transfer
- Exp 2 – TI MSP430 microcontroller introduction
- Exp 3-1, 3-2 – Buck dc-dc converter for PV MPPT and battery charge control
- Exp 4 – Step-up 12V-200V dc-dc converter
- Exp 5 – Single-phase dc-ac converter (inverter)
- Expo – Complete system demonstration

Experiment 3-1



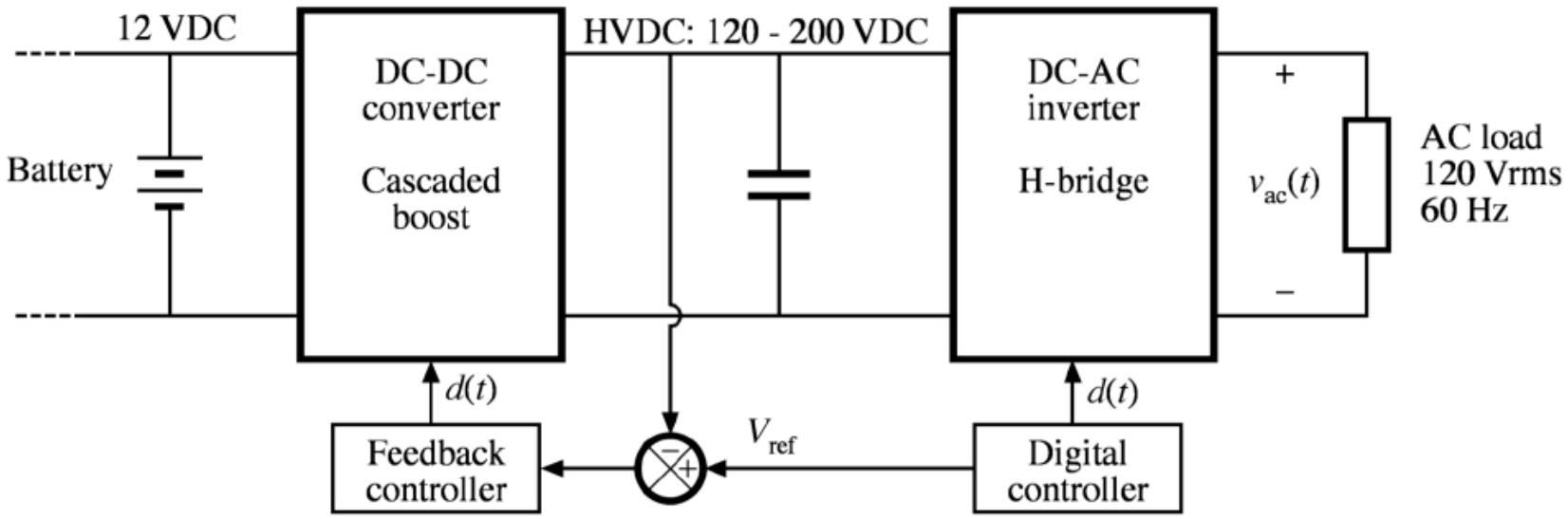
- Demonstrate dc-dc converter power stage operating open loop, driven by MSP430 PWM output:
  - Inside, with input power supply and resistive load
  - Outside, between PV panel and battery
- Compare experimental results with simulation

Experiment 3-2



- Demonstrate working sensor circuitry, interfaced to microcontroller
- Demonstrate maximum power point tracking algorithm, outside with converter connected between PV panel and battery

Experiments 4 and 5



- **Exp 4**: Cascaded boost step-up dc-dc converter (using analog PWM and feedback controller to regulate HVDC)

- **Exp 5**: H-bridge dc-ac inverter

Experiment 4 - Cascaded Boost Converters

- **Controller IC**: Demonstrate operating PWM controller IC (UC 3525)
- **Power Stage**: Demonstrate operating cascaded boost power converters
- **Closed-Loop Analog Control**: Demonstrate analog feedback system that regulates the dc output voltage; and measure and document loop gain and compensator design
- **Additional Analysis** [ECEN 5517 Only]: Develop and verify system loss budget; and analytical model of control-to-output transfer function

Experiment 4 Pre-lab Assignment

- Step up 12 V battery voltage to HVDC (120-200V)
- Will use this for inverter capable of producing same rated power as PV panel (85W)

- Need to choose: duty cycles, switching frequency, inductances
- Design inductors
- Must insure that all components operate within their specified limits
- How much power can you get using the parts in your kit?
- How efficient can your design be?
- Key limitations:
  - MOSFET on-resistances, rated voltages
  - Capacitor rms current ratings, rated working voltages
  - Switching losses
  - Inductor (core & winding) losses, saturation current

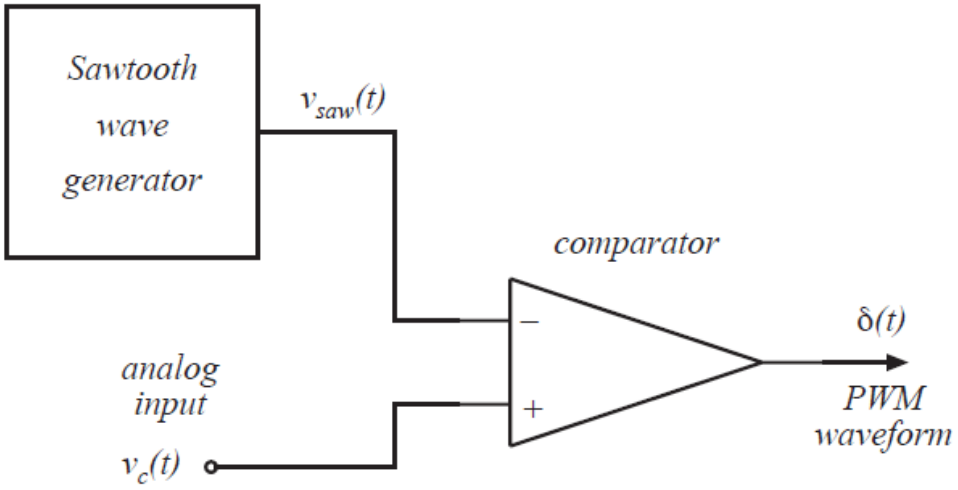
Example Converter Loss Budget

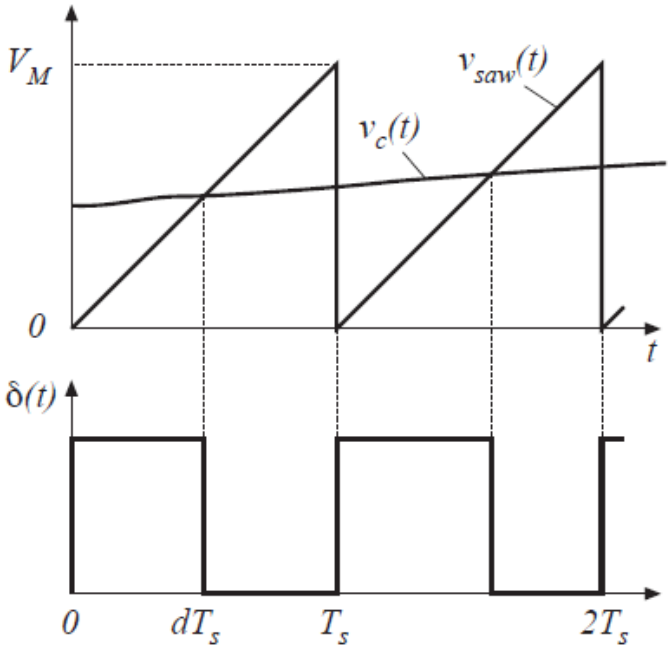
Operating point: V_{in} = 13 V, V_{out} = 200 V, P_{out} = 85 W

MOSFET conduction loss	2.2 W
Diode conduction loss	1.5 W
Switching loss	3.5 W
Inductor loss (core + dc copper + proximity)	4.3 W
Total loss:	11.5 W
Predicted efficiency:	88%

(must document calculations to support above values)

Analog Pulse Width Modulator Operation





For a linear sawtooth waveform:

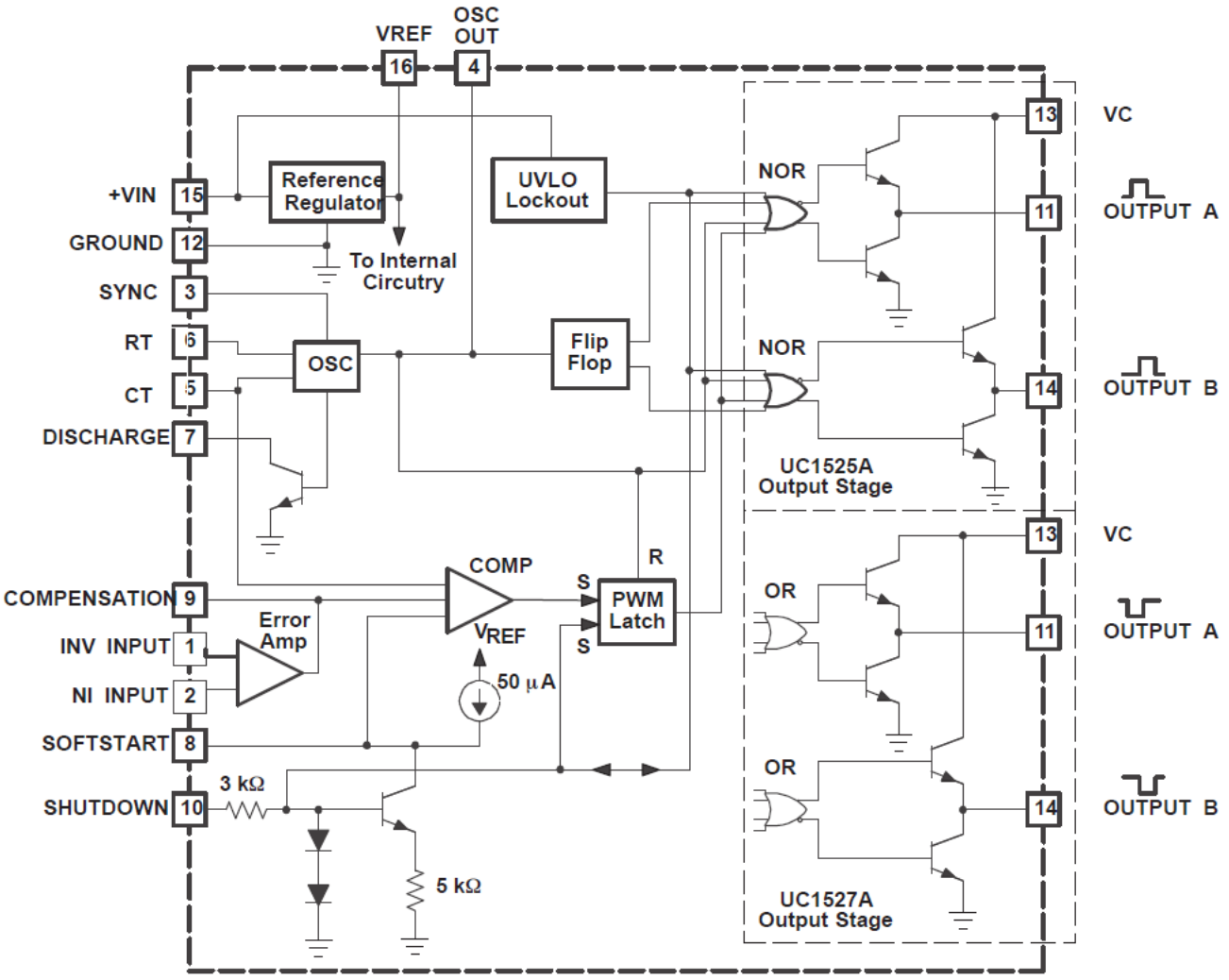
$$d(t) = \frac{v_c(t)}{V_M} \qquad for\ 0 \le v_c(t) \le V_M$$

So $d(t)$ is a linear function of $v_c(t)$.

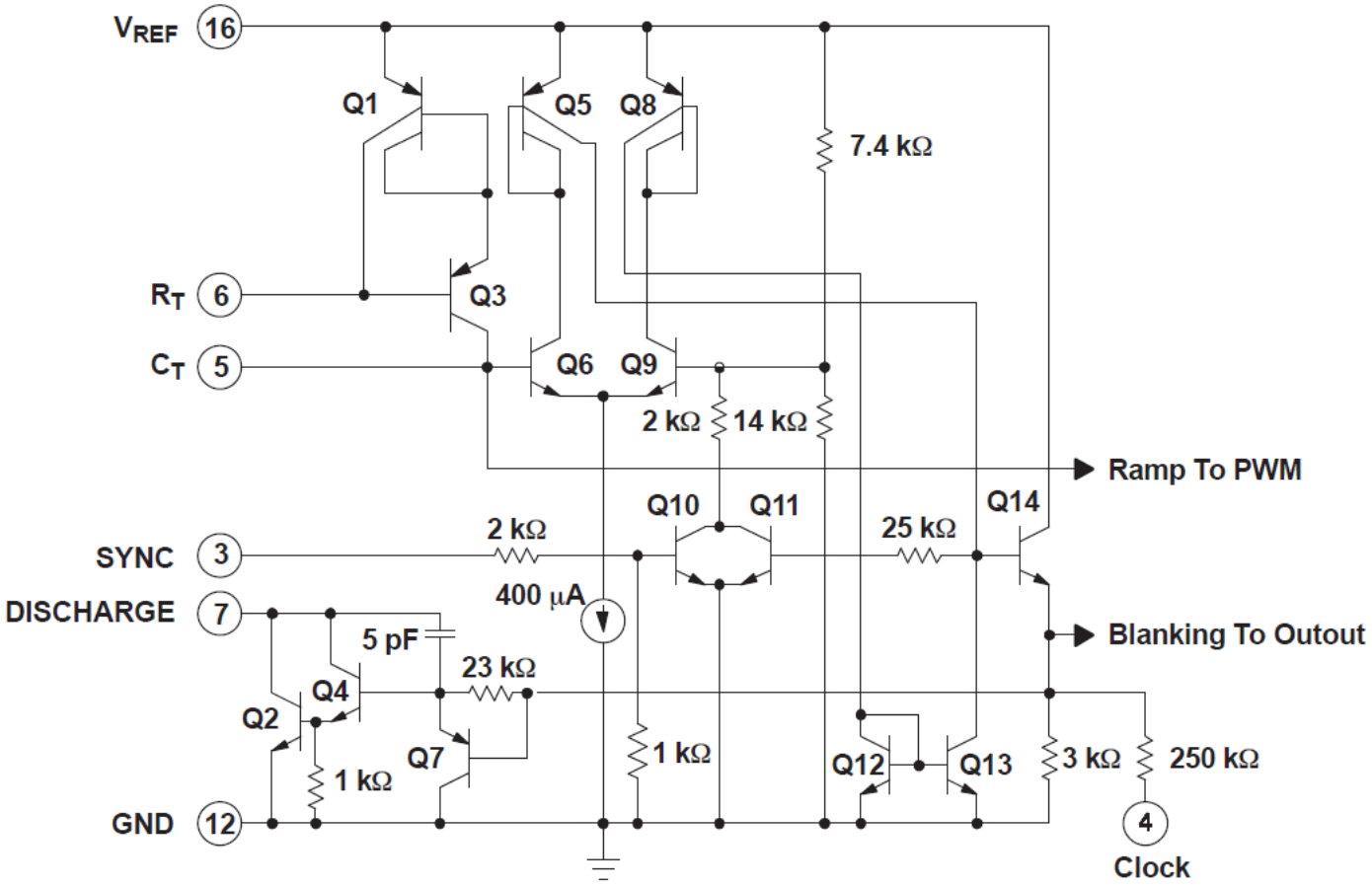
UC3525A Pulse Width Modulator (PWM) IC

Key Functions

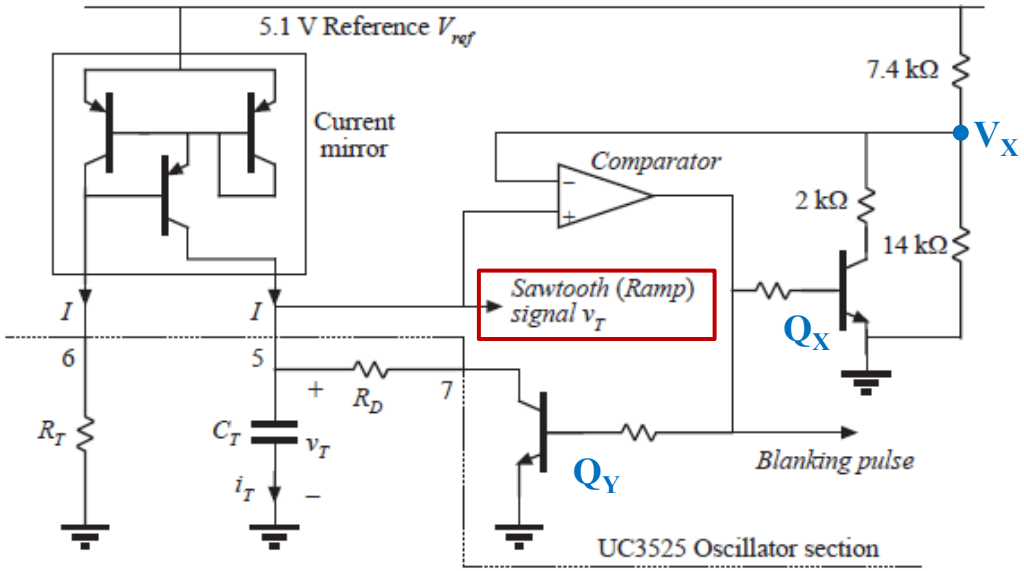
- Sawtooth wave generator (oscillator)
- PWM comparator and latch
- Error amplifier
- 5.1 V reference
- Output drivers
- Shutdown and soft-start circuitry



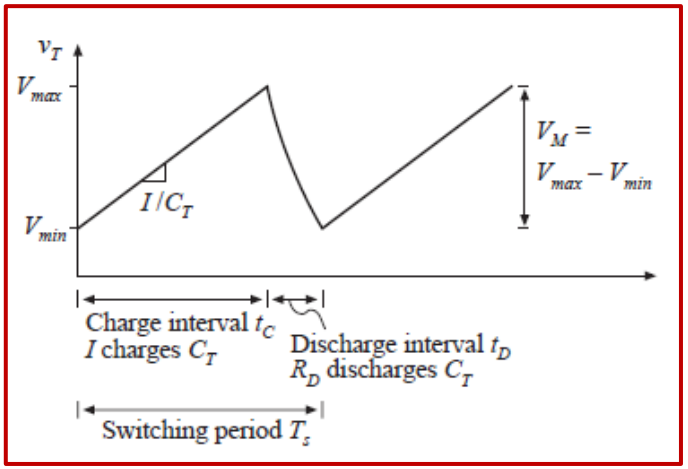
Sawtooth (Ramp) Oscillator Schematic



Sawtooth (Ramp) Oscillator Operation



$$i_T = C_T \frac{dv_T}{dt} \qquad \text{hence} \qquad \frac{dv_T}{dt} = \frac{i_T}{C_T}$$



$$I = \frac{(5.1\text{ V}) - 2(0.7\text{ V})}{R_T}$$

$$V_{max} = (5.1\text{ V})\frac{14\text{ k}\Omega}{14\text{ k}\Omega + 7.4\text{ k}\Omega} = 3.3\text{ V}$$

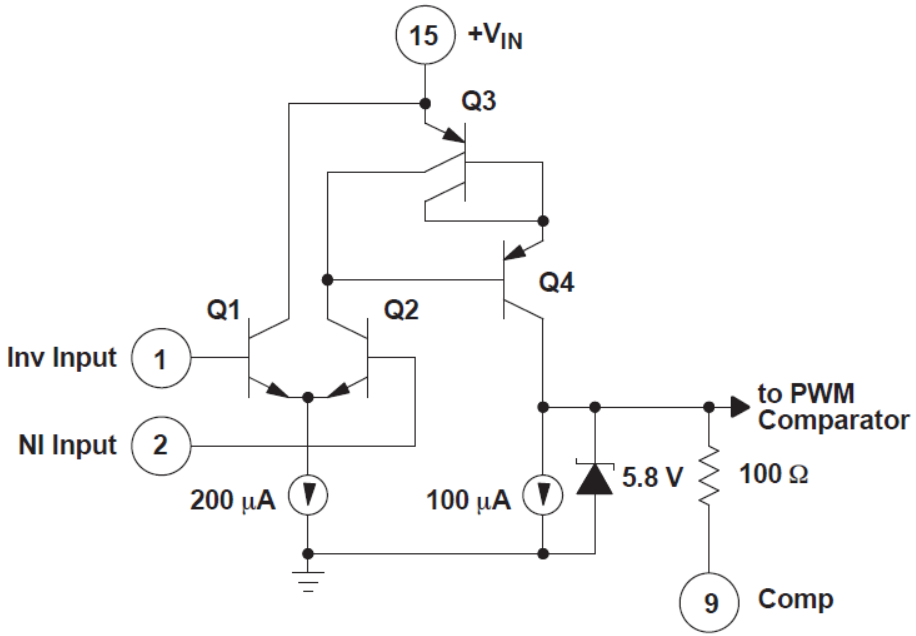
$$V_{min} = (5.1\text{ V})\frac{(2\text{ k}\Omega \parallel 14\text{ k}\Omega)}{(2\text{ k}\Omega \parallel 14\text{ k}\Omega) + 7.4\text{ k}\Omega} = 1.0\text{ V}$$

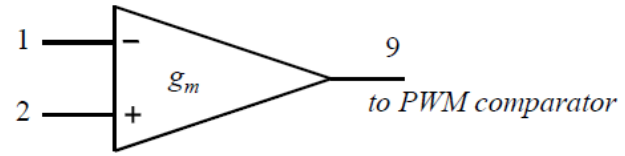
Blanking pulse causes driver outputs to be low, so that $dT_s \le t_c$

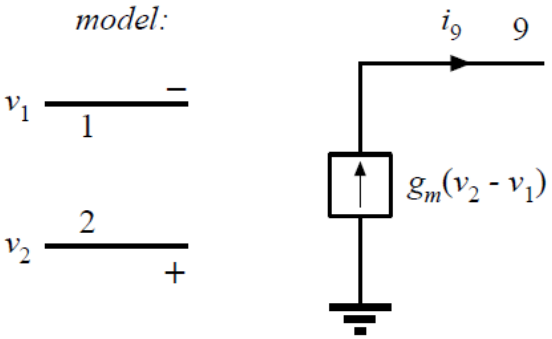
Increasing R_D reduces maximum allowed duty cycle D_{max}

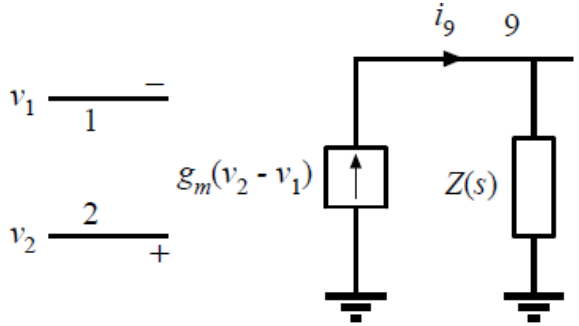
- R_T must be greater than 2kΩ; otherwise the UC3525 oscillator will not work
- R_D must be substantially smaller then R_T; R_D is usually a few hundred Ohms

Error Amplifier





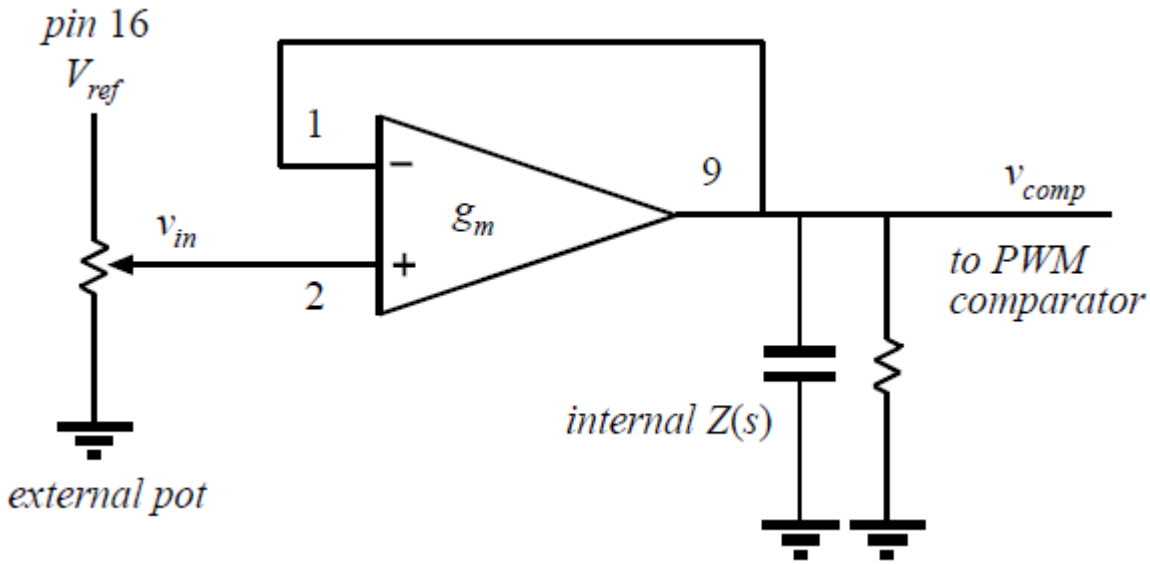




- The differential voltage gain is: $g_m Z(s)$
- With large Z(s), the differential voltage gain is large; the data sheet specifies a low-frequency differential voltage gain of at least 1000 (60 dB)

$$v_9 = g_m Z(s)(v_2 - v_1)$$

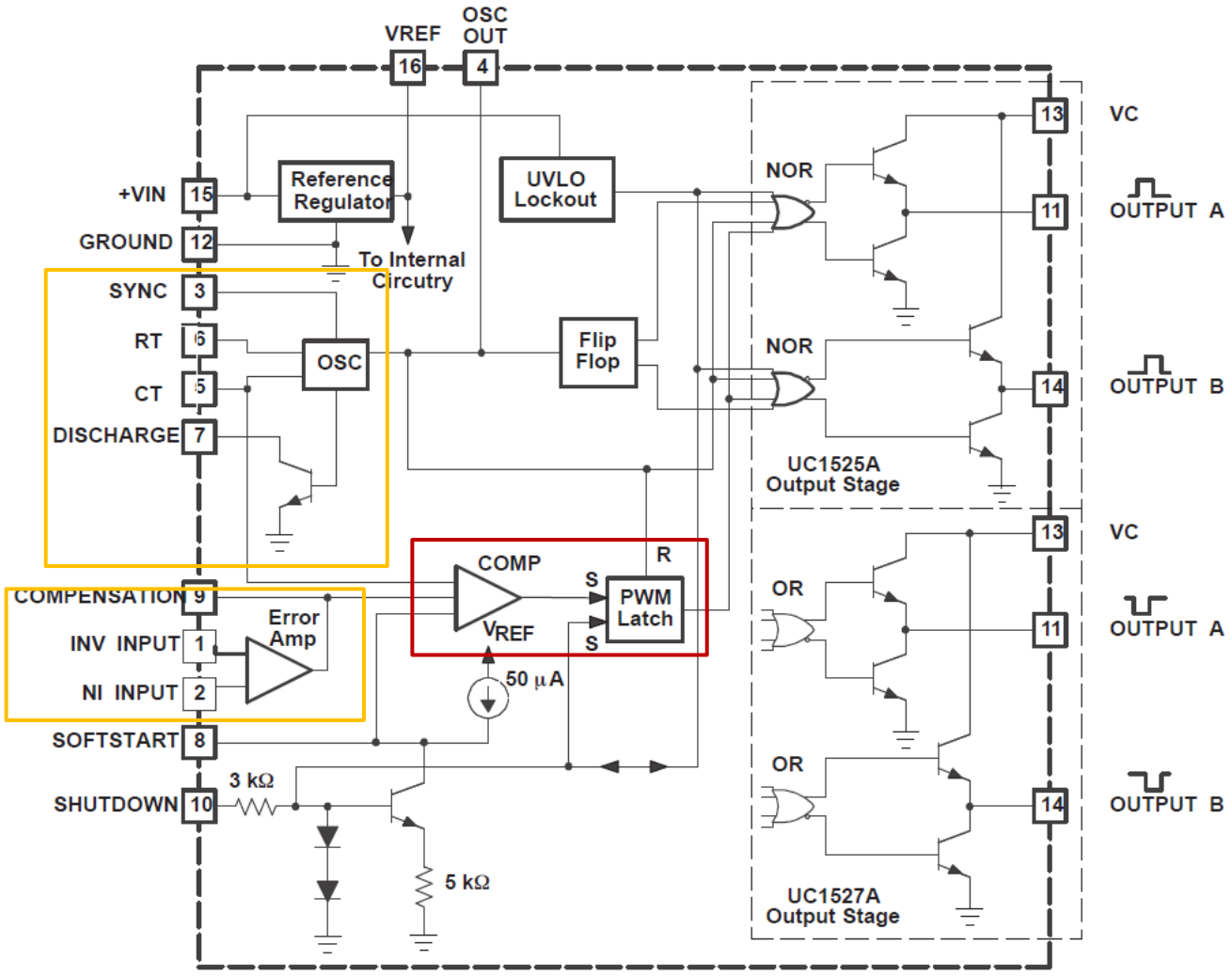
Adjustable Duty Ratio using Error Amplifier



The error amplifier is connected as a unity-gain stage: $v_{comp} = v_{in}$

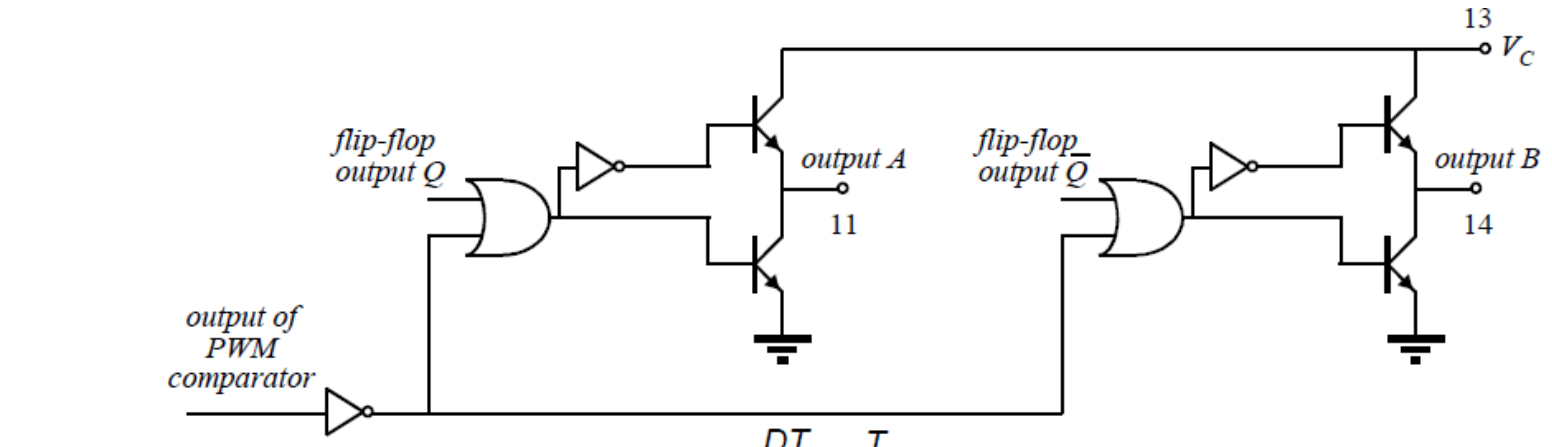
The duty cycle D can be adjusted by the external pot.

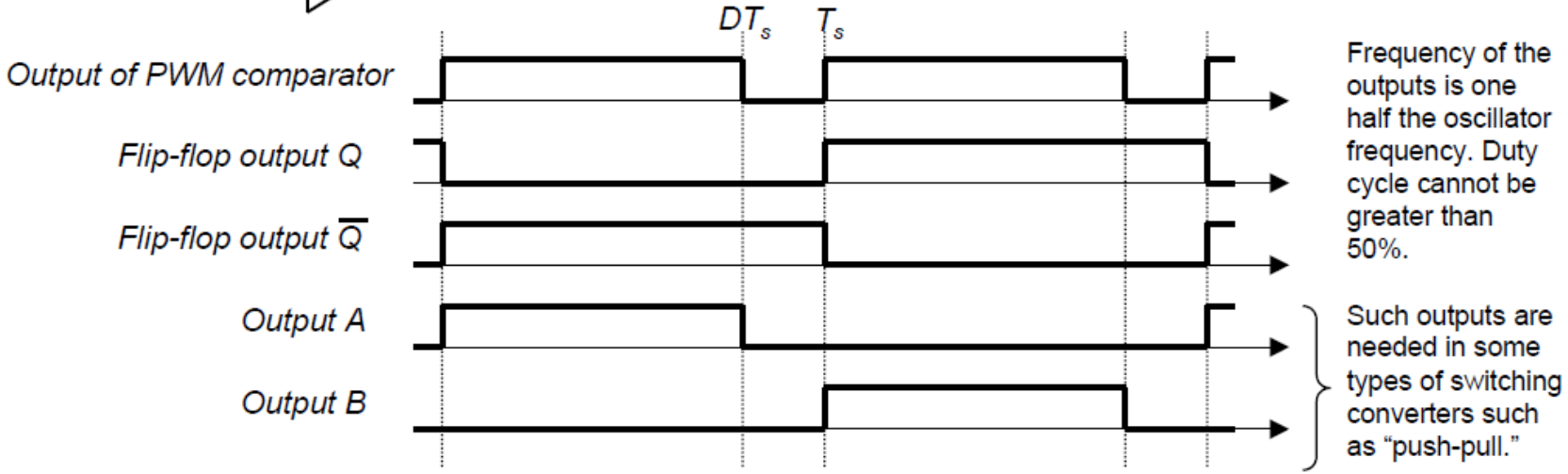
PWM Function Implementation



- PWM latch prevents from having multiple pulses in a switching period

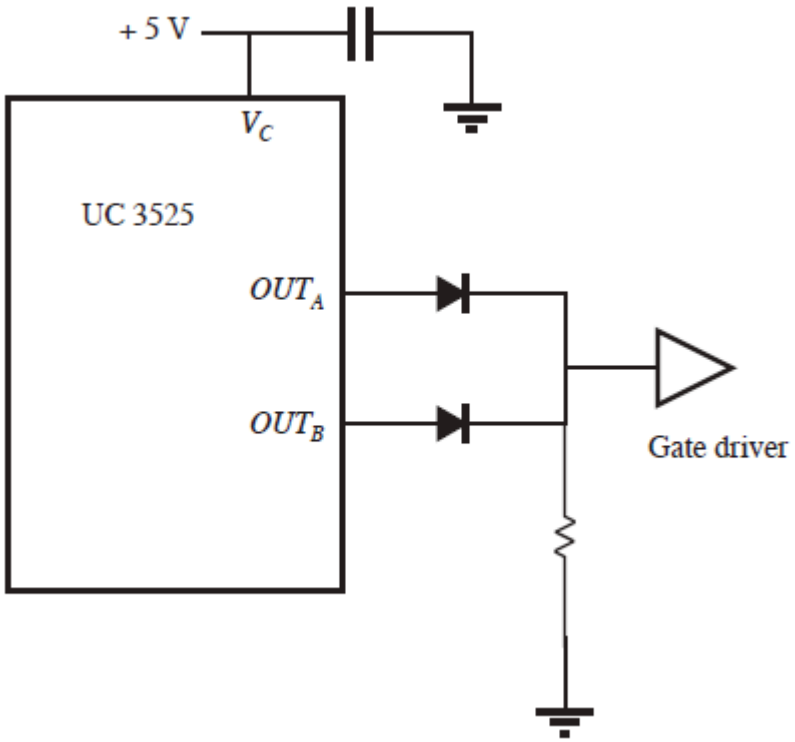
Outputs of UC3525A





Outputs A and B can be OR-ed to restore the PWM pulses at the oscillator frequency.

OR-ing the Outputs of UC3525A



- A simple way to OR the outputs is using two diodes and a resistor

More Tips

The + 5 V *can be obtained from the* 5 V *reference of the* UC3525

Bypass the + 5 V *so that the switching EMI of this circuit does not disrupt the internal control circuitry of the* UC3525, *which also uses the* + 5 V.

Soft Start and Shutdown

Soft Start

- A capacitor can be connected to the soft start pin (8); the voltage on this pin limits the maximum duty ratio
- At turn on, the capacitor will start at 0V, and then will charge from the 50μA current source; this overrides the feedback loop and starts the converter gently

Shutdown

- The shutdown pin (10) turns off the chip outputs; ground this pin to ensure that the outputs are not shut down