EXPERIMENT 4 LAB REPORT

ECEN 5517 (Spring 2017)
Power electronics and Photovoltaic Power Systems Laboratory

4/4/2017

TEAM MUSE
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Objectives

The objectives of this experiment are:

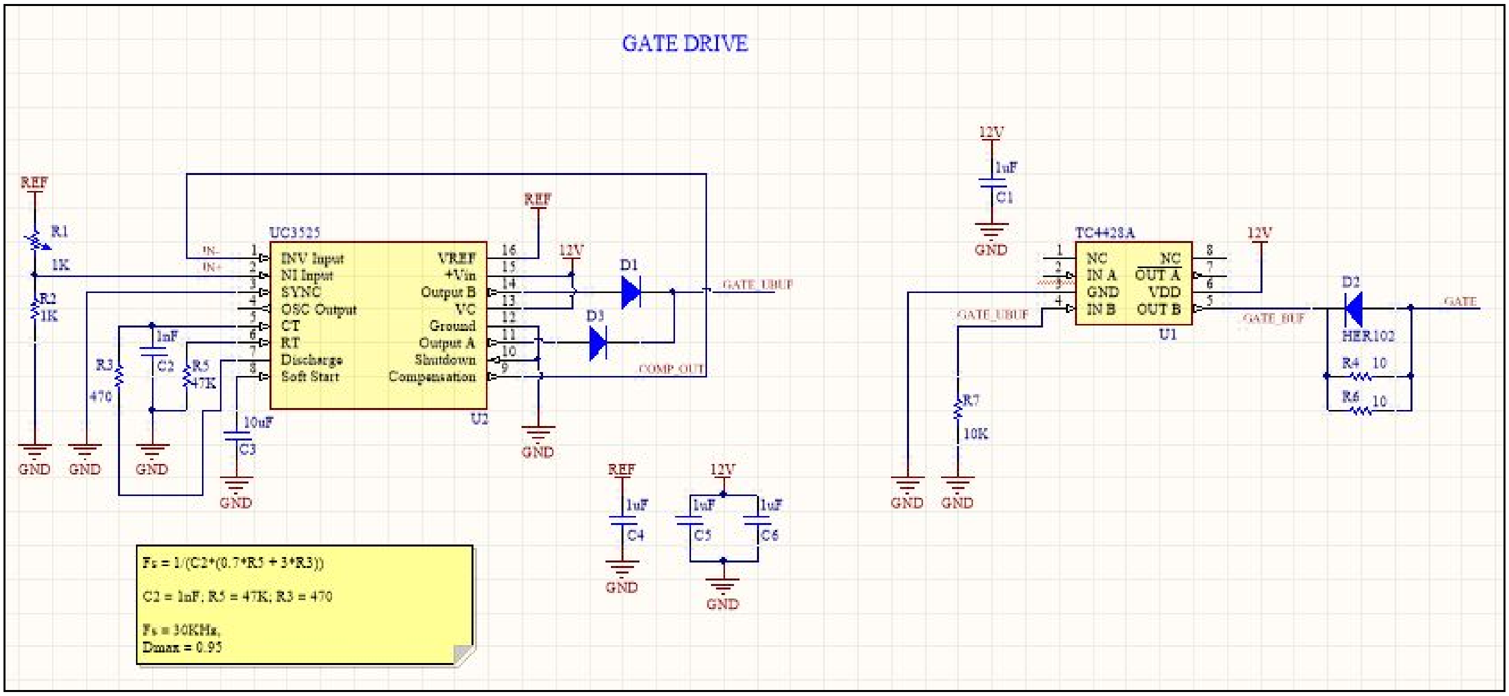
- To design, construct and test a cascaded dc-dc boost converter that converts the low voltage of the battery into a high voltage dc bus (~200V)
- To design, construct and test a closed-loop analog feedback loop that regulates the dc bus output voltage of the converter

Experimental data

Equipments used

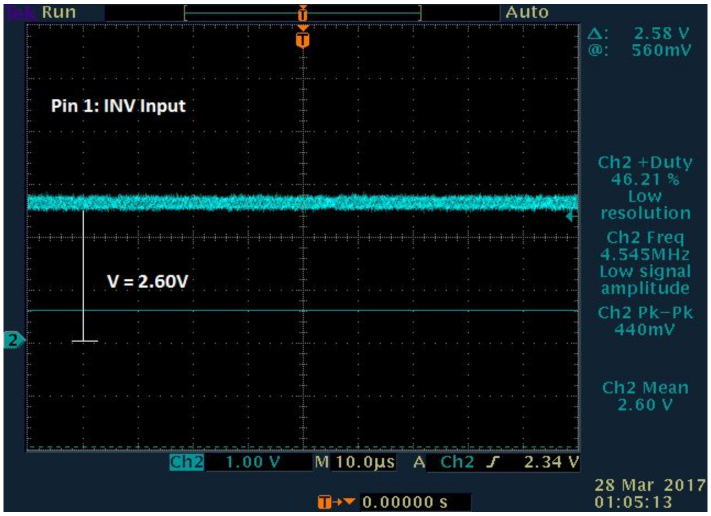
Power	**Measurement**
Power Supply: 30V-5A Dual Power Supply Rheostat: 0 -15.5 Ohms	Meters: FLUKE 45 Oscilloscope: TDS3012C Current Probe: TCP202A

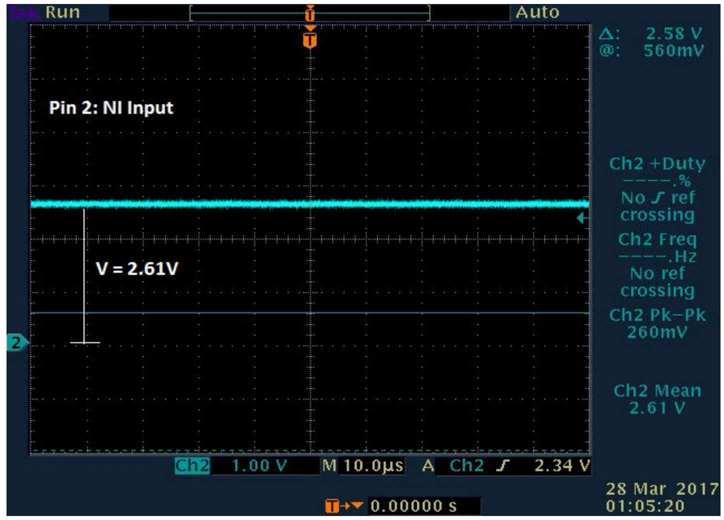
PWM Controller Circuit

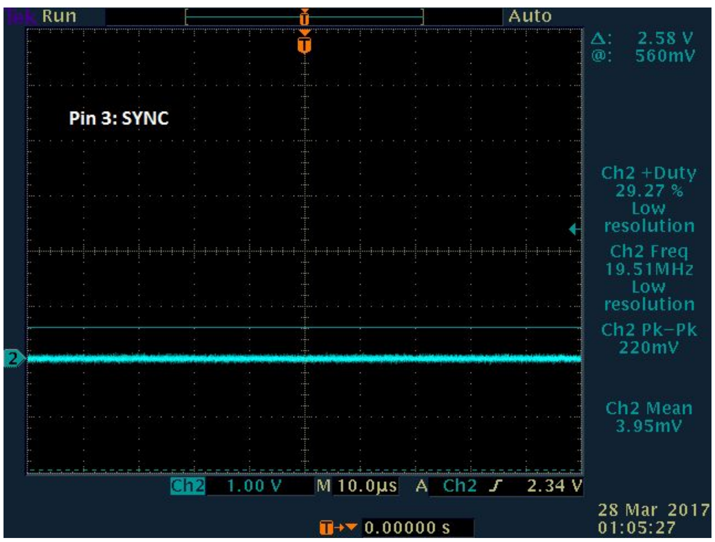


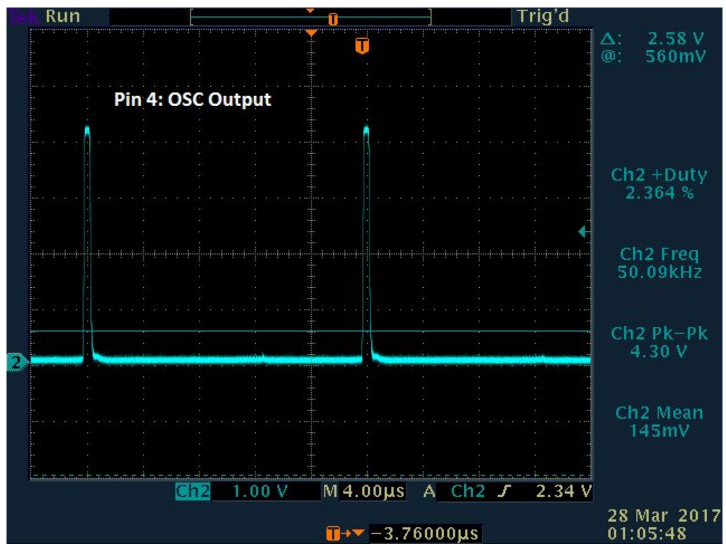
UC3525 PWM Controller waveforms

The important values of the waveforms are indicated by the scope measurement on each image

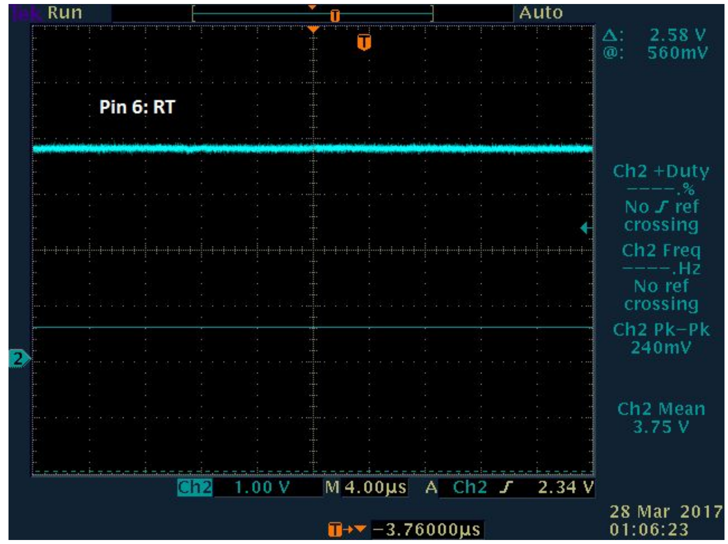


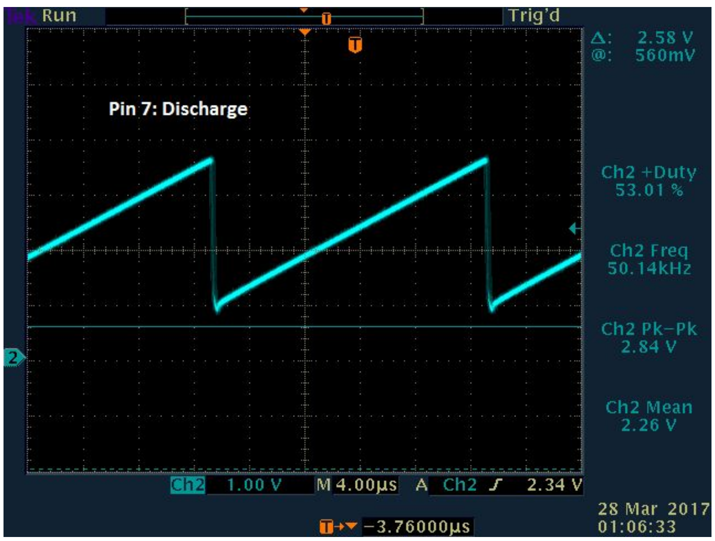


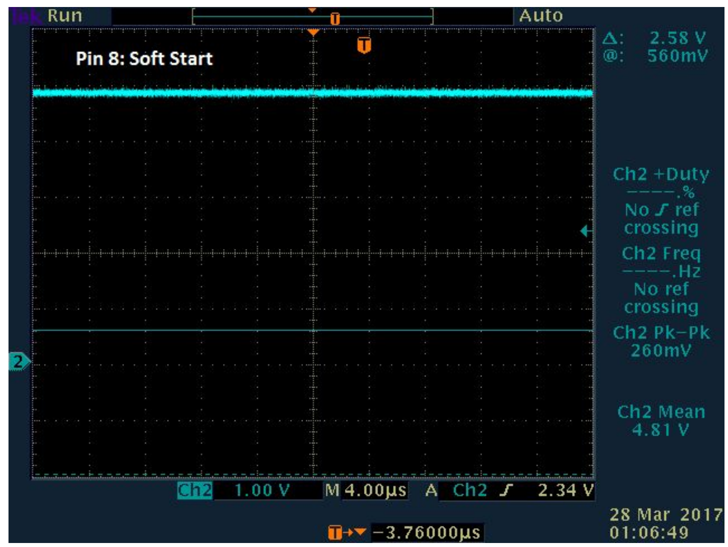


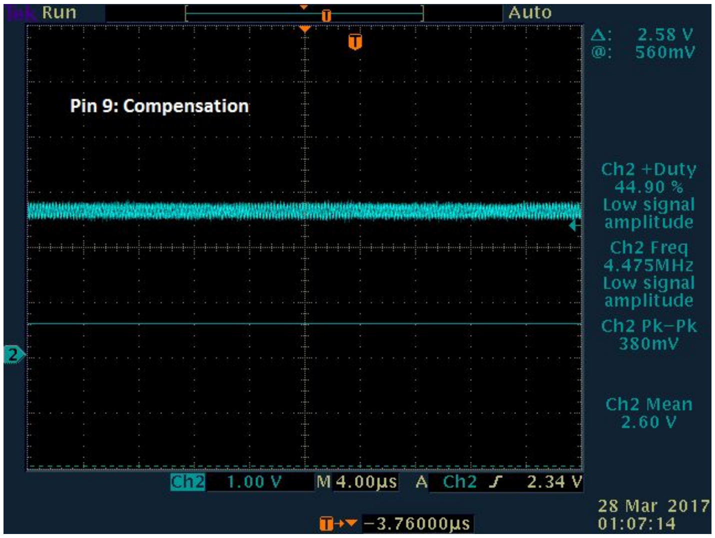


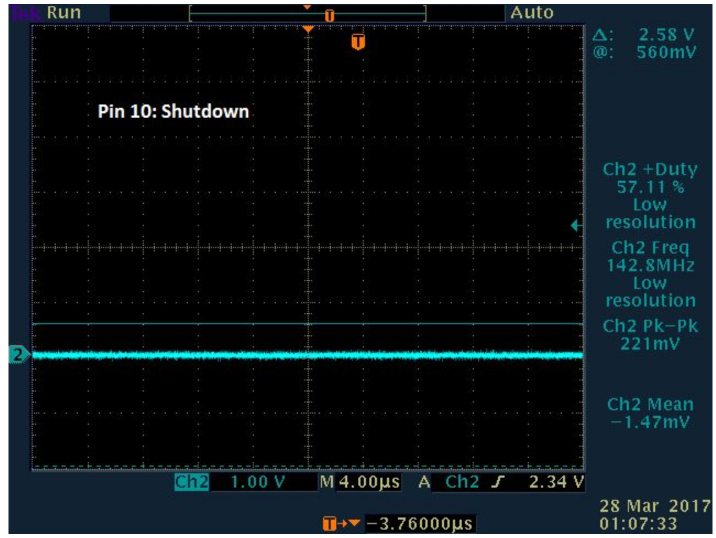

Run
Trig'd
Δ: 2.58 V
@: 560mV
Pin 5: CT
Ch2 +Duty
53.52 %
Ch2 Freq
51.35kHz
Ch2 Pk−Pk
2.78 V
Ch2 Mean
2.28 V
Ch2 1.00 V M 4.00µs A Ch2 2.34 V
−3.76000µs
28 Mar 2017
01:06:05

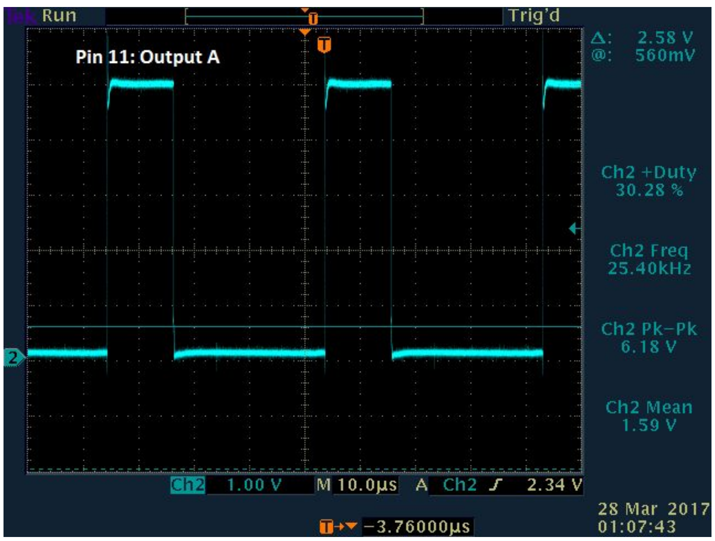

Run
Auto
Δ: 2.58 V
@: 560mV
Pin 6: RT
Ch2 +Duty
−−−−.%
No ref
crossing
Ch2 Freq
−−−−.Hz
No ref
crossing
Ch2 Pk−Pk
240mV
Ch2 Mean
3.75 V
Ch2 1.00 V M 4.00µs A Ch2 2.34 V
−3.76000µs
28 Mar 2017
01:06:23

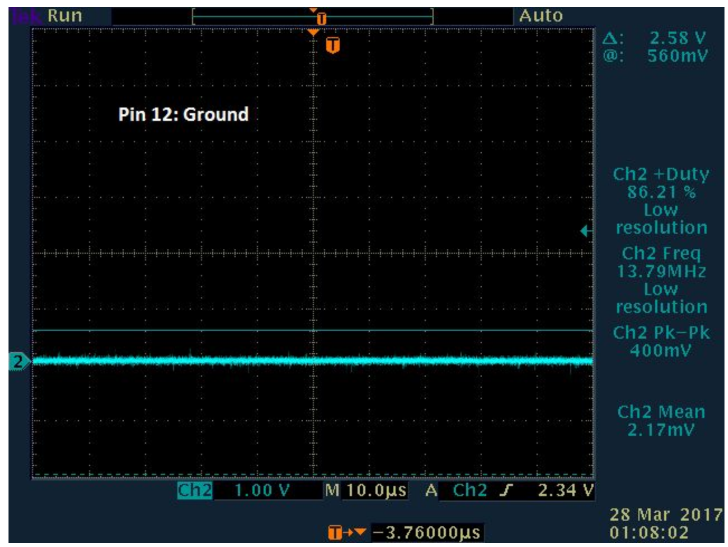

Run
Trig'd
Δ: 2.58 V
@: 560mV
Pin 7: Discharge
Ch2 +Duty
53.01 %
Ch2 Freq
50.14kHz
Ch2 Pk−Pk
2.84 V
Ch2 Mean
2.26 V
Ch2 1.00 V M 4.00µs A Ch2 2.34 V
−3.76000µs
28 Mar 2017
01:06:33

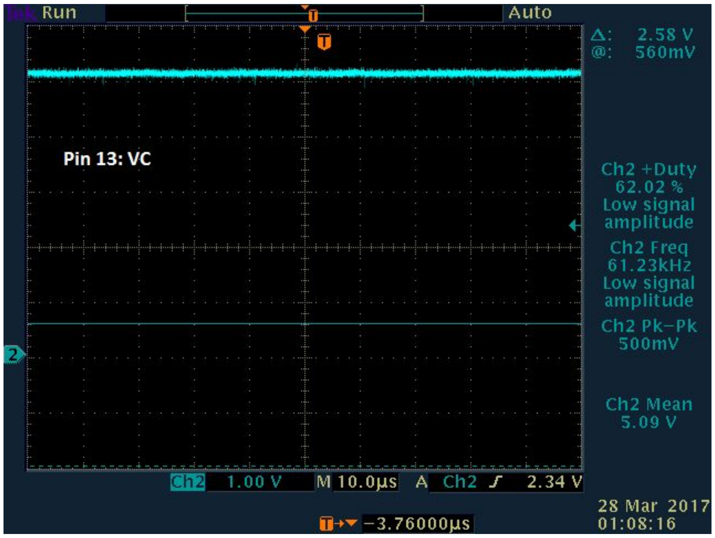

Run
Auto
Δ: 2.58 V
@: 560mV
Pin 8: Soft Start
Ch2 +Duty
−−−−.%
No ref
crossing
Ch2 Freq
−−−−.Hz
No ref
crossing
Ch2 Pk−Pk
260mV
Ch2 Mean
4.81 V
Ch2 1.00 V M 4.00µs A Ch2 2.34 V
−3.76000µs
28 Mar 2017
01:06:49

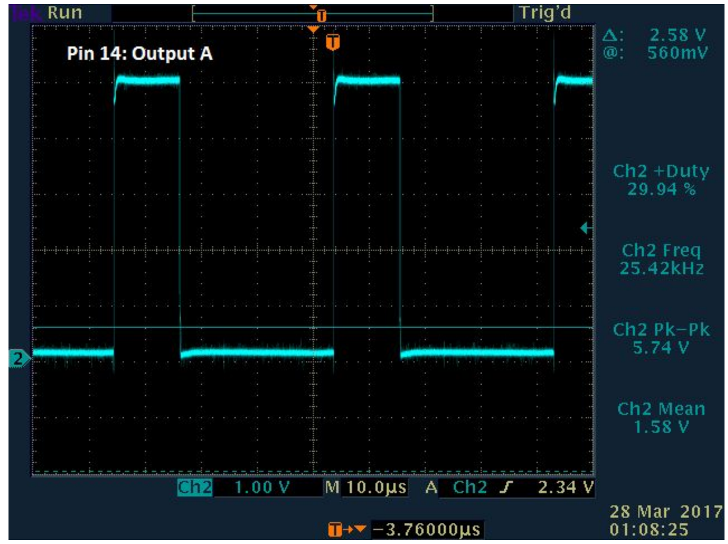

Tek Run
Auto
Δ: 2.58 V
@: 560mV
Pin 9: Compensation
Ch2 +Duty
44.90 %
Low signal
amplitude
Ch2 Freq
4.475MHz
Low signal
amplitude
Ch2 Pk−Pk
380mV
Ch2 Mean
2.60 V
Ch2 1.00 V M 4.00µs A Ch2 2.34 V
−3.76000µs
28 Mar 2017
01:07:14

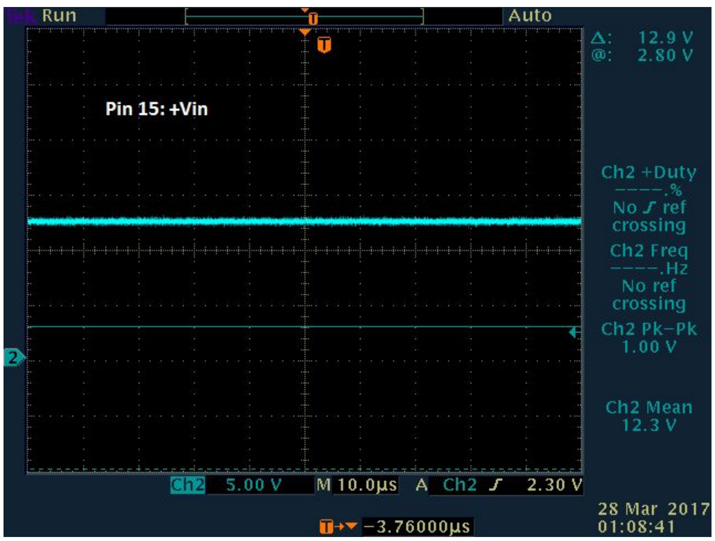

Tek Run
Auto
Δ: 2.58 V
@: 560mV
Pin 10: Shutdown
Ch2 +Duty
57.11 %
Low
resolution
Ch2 Freq
142.8MHz
Low
resolution
Ch2 Pk−Pk
221mV
Ch2 Mean
−1.47mV
Ch2 1.00 V M 4.00µs A Ch2 2.34 V
−3.76000µs
28 Mar 2017
01:07:33

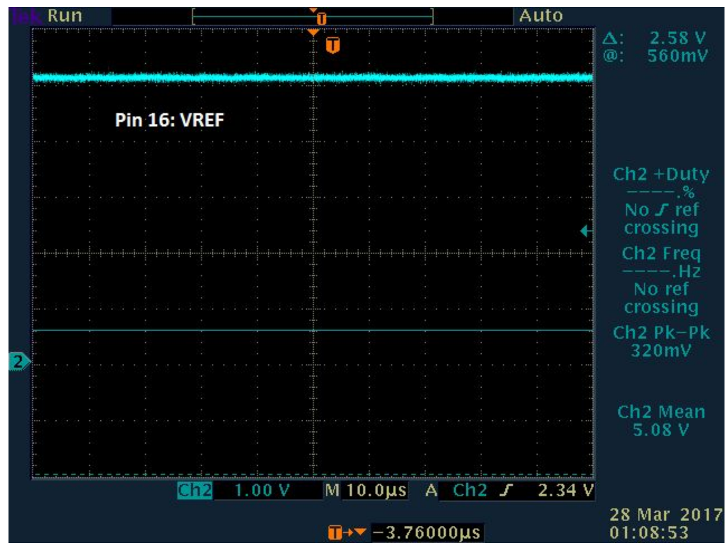

Tek Run
Trig'd
Δ: 2.58 V
@: 560mV
Pin 11: Output A
Ch2 +Duty
30.28 %
Ch2 Freq
25.40kHz
Ch2 Pk−Pk
6.18 V
Ch2 Mean
1.59 V
Ch2 1.00 V M 10.0µs A Ch2 2.34 V
−3.76000µs
28 Mar 2017
01:07:43


Tek Run
Auto
Δ: 2.58 V
@: 560mV
Pin 12: Ground
Ch2 +Duty
86.21 %
Low
resolution
Ch2 Freq
13.79MHz
Low
resolution
Ch2 Pk−Pk
400mV
Ch2 Mean
2.17mV
Ch2 1.00 V M 10.0µs A Ch2 2.34 V
−3.76000µs
28 Mar 2017
01:08:02

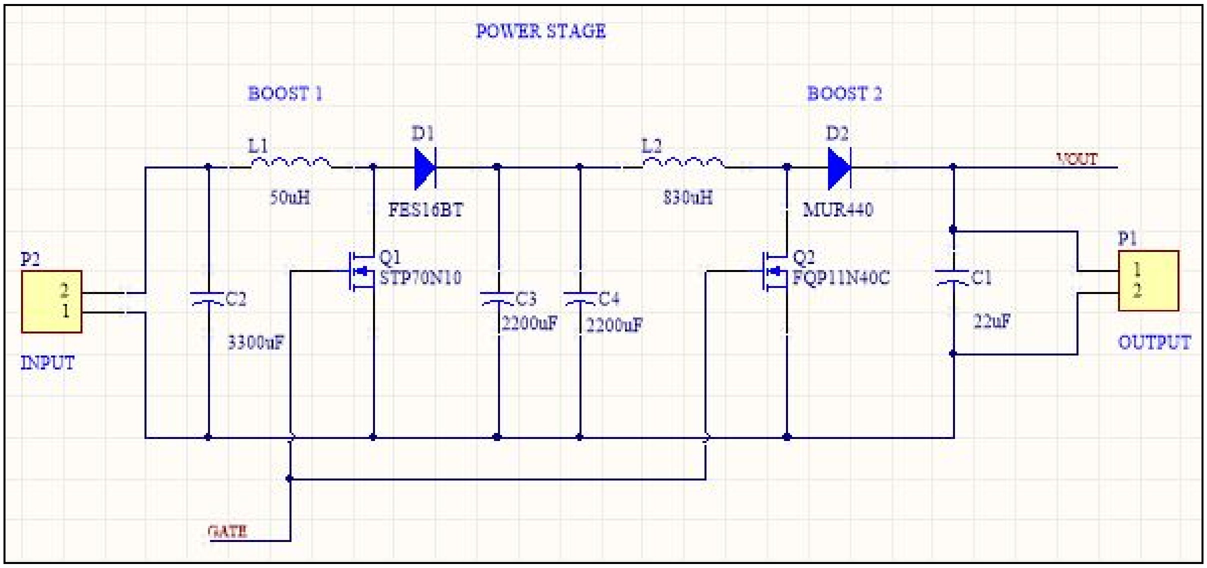

Run
Auto
Δ: 2.58 V
@: 560mV
Pin 13: VC
Ch2 +Duty
62.02 %
Low signal
amplitude
Ch2 Freq
61.23kHz
Low signal
amplitude
Ch2 Pk−Pk
500mV
Ch2 Mean
5.09 V
Ch2 1.00 V M 10.0µs A Ch2 2.34 V
-3.76000µs
28 Mar 2017
01:08:16


Run
Trig'd
Δ: 2.58 V
@: 560mV
Pin 14: Output A
Ch2 +Duty
29.94 %
Ch2 Freq
25.42kHz
Ch2 Pk−Pk
5.74 V
Ch2 Mean
1.58 V
Ch2 1.00 V M 10.0µs A Ch2 2.34 V
-3.76000µs
28 Mar 2017
01:08:25


Run
Auto
Δ: 12.9 V
@: 2.80 V
Pin 15: +Vin
Ch2 +Duty
----.%
No ref
crossing
Ch2 Freq
----.Hz
No ref
crossing
Ch2 Pk−Pk
1.00 V
Ch2 Mean
12.3 V
Ch2 5.00 V M 10.0µs A Ch2 2.30 V
-3.76000µs
28 Mar 2017
01:08:41


Run
Auto
Δ: 2.58 V
@: 560mV
Pin 16: VREF
Ch2 +Duty
----.%
No ref
crossing
Ch2 Freq
----.Hz
No ref
crossing
Ch2 Pk−Pk
320mV
Ch2 Mean
5.08 V
Ch2 1.00 V M 10.0µs A Ch2 2.34 V
-3.76000µs
28 Mar 2017
01:08:53

Power Stage Schematic



Inductance design

	Boost Stage-1	Boost Stage-2
Theoretical	48.6uH	833uH
Measured	50uH	830uH

Open loop Power Stage Testing

EFFICIENCY

The boost stage output capacitor used: **22uF, 200V.** Hence the boost output was limited to 150V. All readings below were taken at 150V and 85W

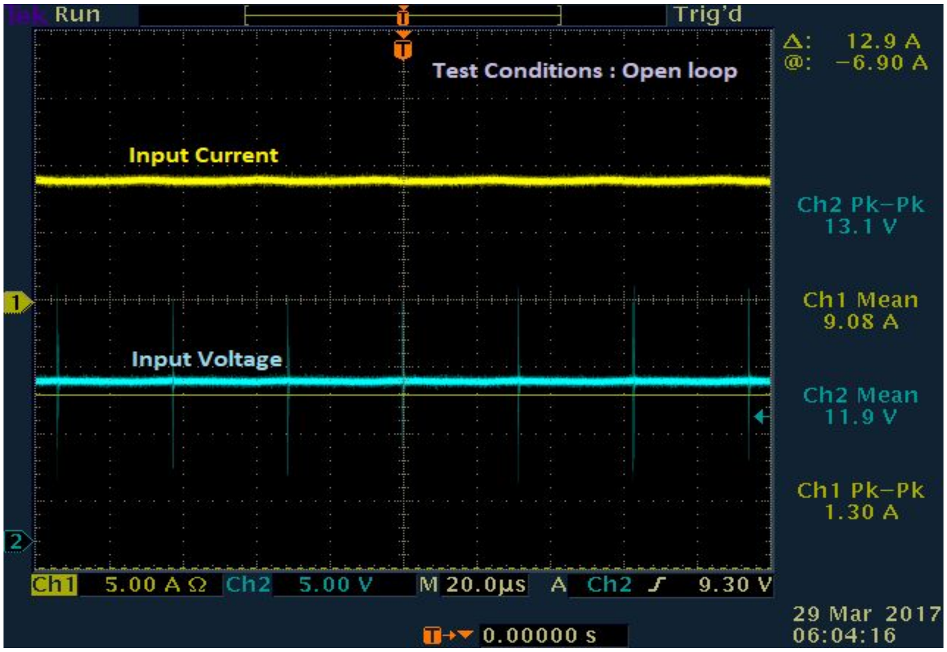
Operating point : 150V , 85W output

Input Voltage (V)	Input Current (A)	Input power (W)	Duty cycle	Output Voltage (V)	Output Current (A)	Output Power (W)	Efficiency (%)
12.05	8.015	96.58	0.717	150.3	0.575	86.42	89.48

INPUT VOLTAGE/CURRENT WAVEFORMS

(Operating point: 150V, 85W)

Vin (average): 11.9V **Iin (average):** 9.08A



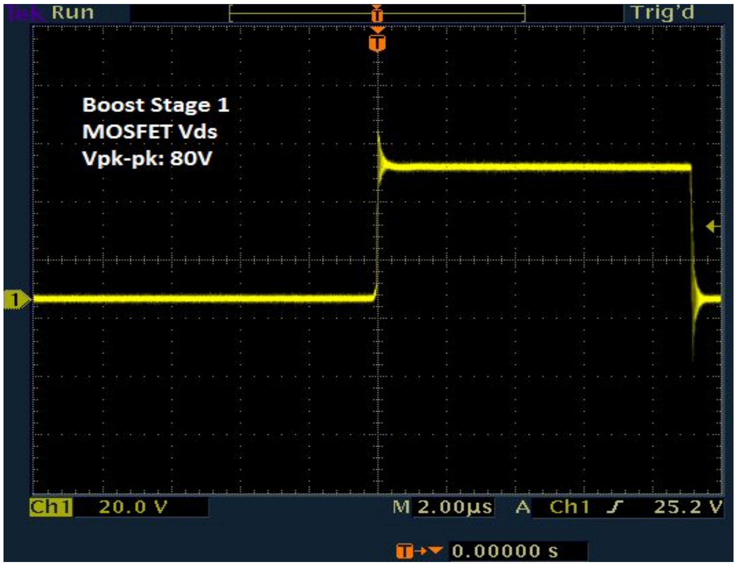
OUTPUT VOLTAGE/CURRENT WAVEFORMS

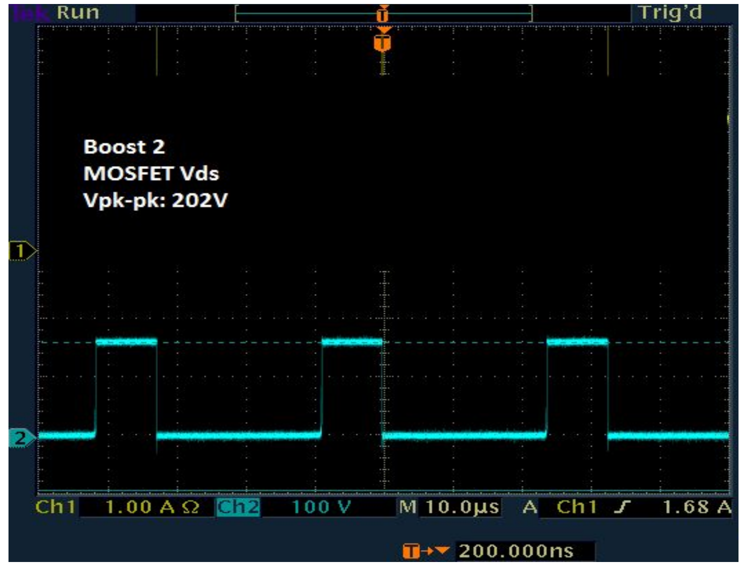
(Operating point: 150V, 85W)

Vout (average): 150V **Iout (average):** 0.542A

MOSFET DRAIN-SOURCE (Vds) WAVEFORMS

BOOST STAGE 1	BOOST STAGE 2





Loss Budget

First Power Stage

MOSFET Conduction Loss

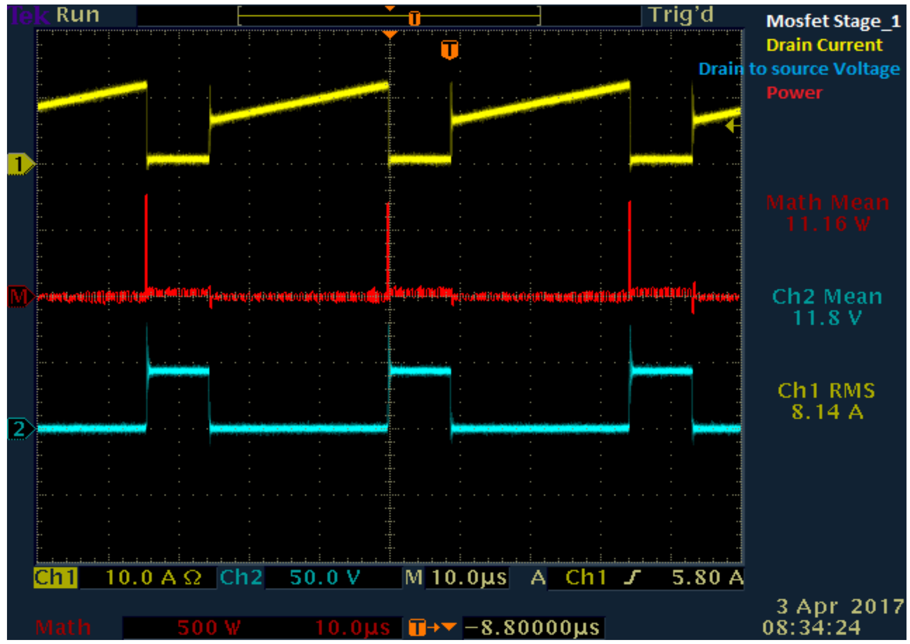
Irms = 8.14 A

R= 19.5 mOhm

D=0.717

$P = Irms^2 * R * D$

= 0.92W



Diode Conduction Loss

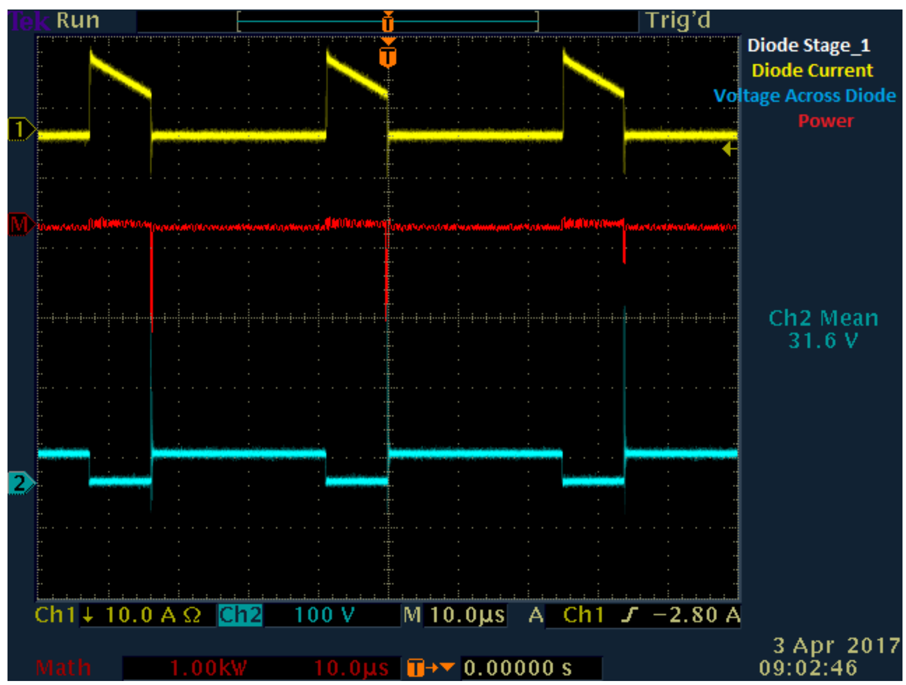
I= 4.43 A

Vf= 1 V

D=0.717

$P = I * Vf * (1 - D)$

= 1.254 W



Switching Loss

Approximating it from Wave Form

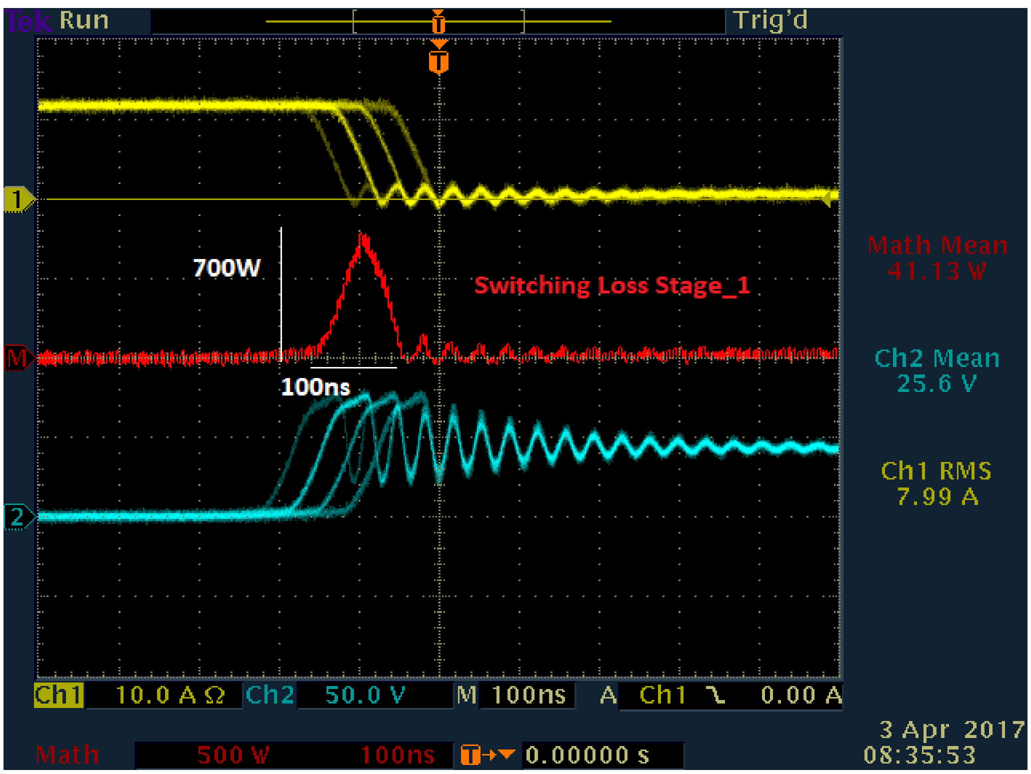
Switching Freq = sw=30kHz

{ approximating power waveform to triangle
base and height values from power waveform}

P= 0.5* Base * height *sw

=0.5*100n*700*30k

= 1.05W



Second Power Stage

MOSFET Conduction Loss

Irms=1.29 A

R= 19.5 mOhm

D= 0.717

$P = Irms^2 * R * D$

=0.023W

Diode Conduction Loss

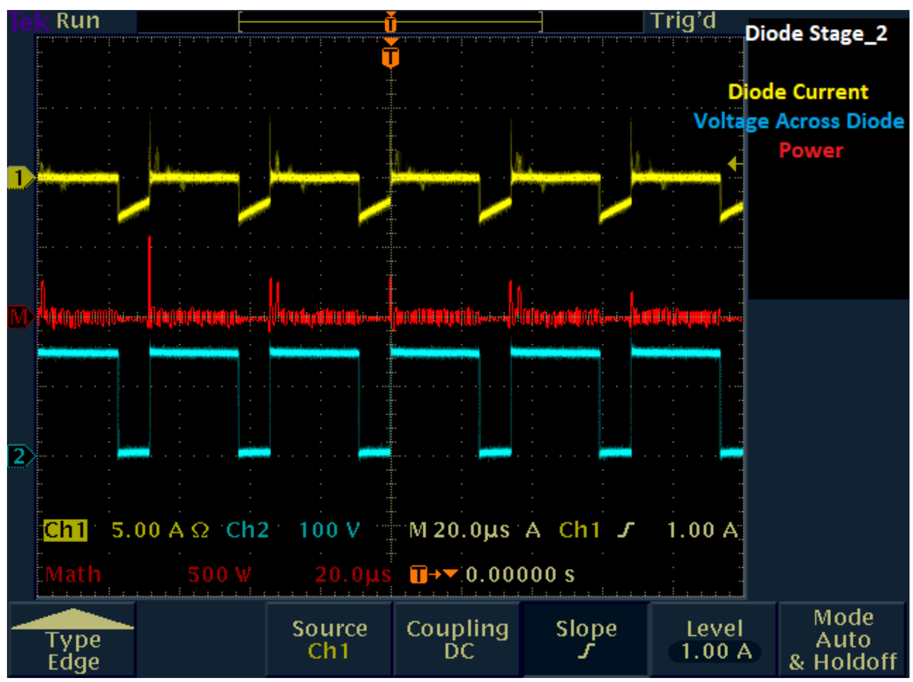
I= 1.12 A

Vf=1 V

D=0.717

$P = I * Vf * (1 - D)$

= 0.317 W



Note: The Diode Stage_2 Current Waveform is inverted

Switching Loss

Approximating it from Wave Form

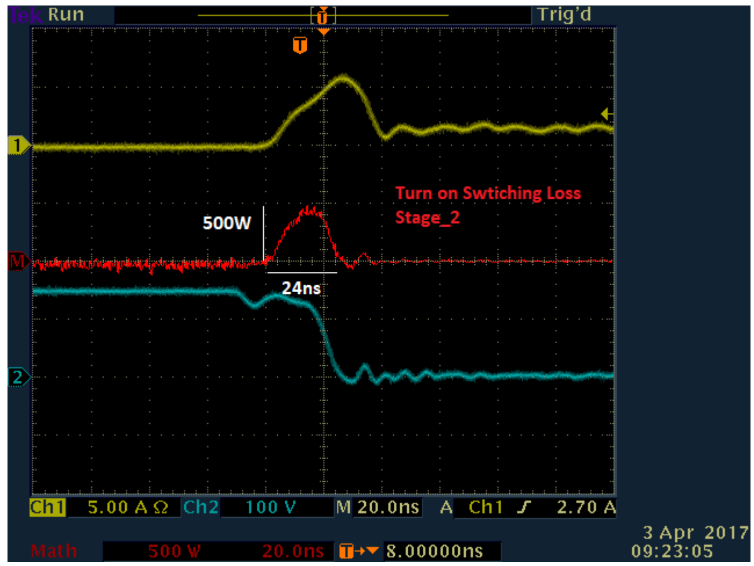
Switching Freq = sw=30kHz

{ approximating power waveform to triangle
base and height values from power waveform}

P_{turn_on}= 0.5* Base * height *sw

=0.5*24n*500*30k

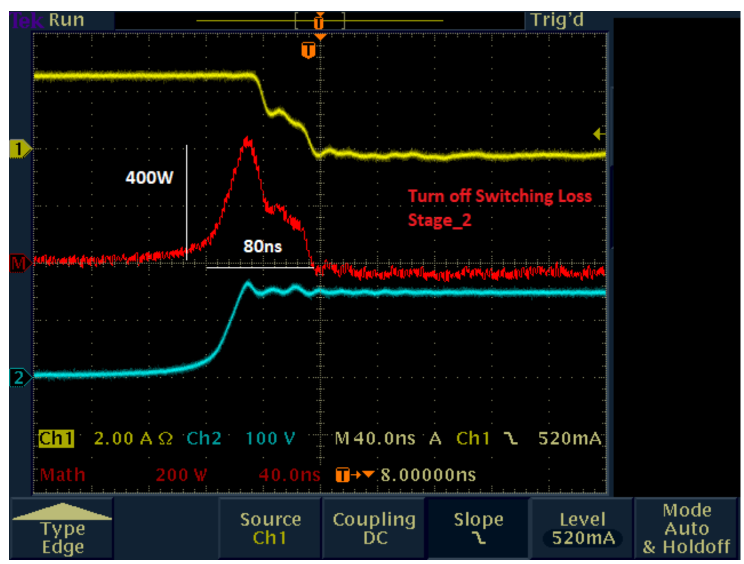
= 0.18 W



P_{turn_off}= 0.5* Base * height *sw

=0.5*80n*400*30k

= 0.48W



Inductor Loss

Copper Loss

Stage_1 Inductor

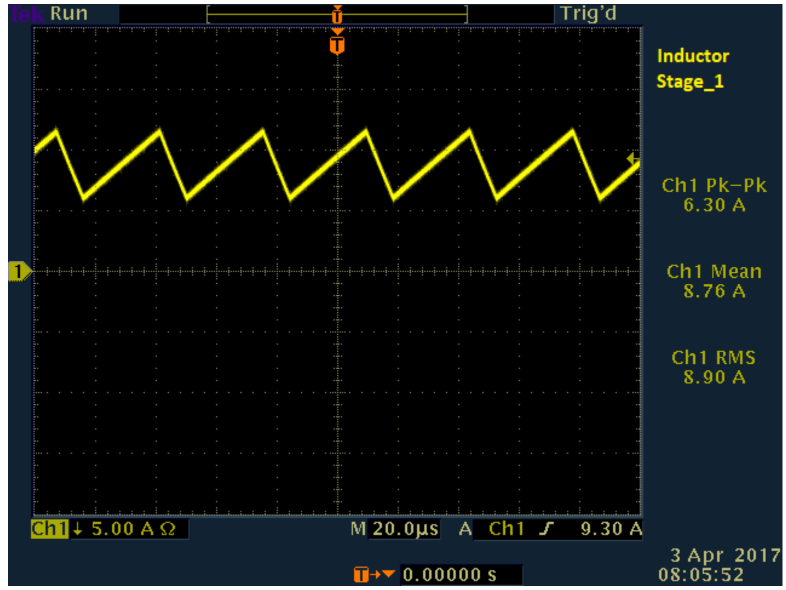
AWG#17

R= 0.013 Ohm

Irms = 8.9 A

$P = Irms^2 * R$

= 1.03 W



Stage_2 Inductor

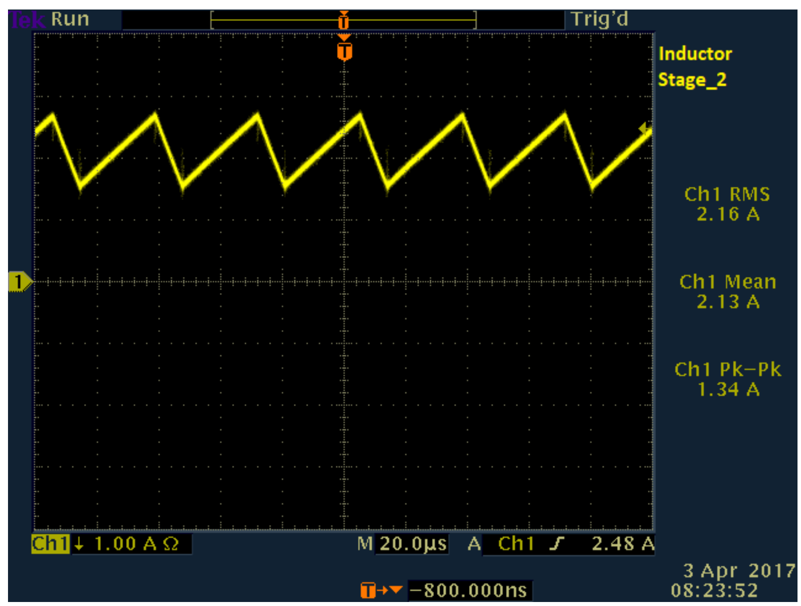
AWG#22

R= 0.152 Ohm

Irms = 2.16 A

$P = Irms^2 * R$

= 0.71 W



Core Loss

Stage_1 Inductor

ΔB=77mT

Switching Frequency = 30kHz

Power Density = 9 (kW/m^3)

Effective Area of Core = 0.000166 m^2

Height = 0.212 m

Volume = 3.52 u*m^3

Power loss= Power density * Volume

= 0.03168 W

Stage_2 Inductor

ΔB=74mT

Switching Frequency = 30kHz

Power Density = 9 (kW/m^3)

Effective Area of Core = 0.000166 m^2

Height = 0.212 m

Volume = 3.52 u*m^3

Power loss= Power density * Volume

= 0.03168 W

Proximity Loss

Stage_1 Inductor

Total Number of Turns = 12

Number of layers=2

Number of turns per layer = 6

Rdc = 0.66 m Ohm

Switching frequency = 30 kHz

H=0.122 cm

δ = 0.378*10^(-3)

$$Rac = \frac{H}{\delta} * Rdc$$

=2.13 m Ohm

ΔIL=3.15

$$Irms = \frac{\Delta IL}{\sqrt{3}}$$

= 1.818

Power Loss_per layer = $Irms^2 * Rac$

= 7.03 mW

Total Loss= 6*Loss_per layer

= 42.23 mW

Stage_2 Inductor

Total Number of Turns = 44

Number of layers=4

Number of turns per layer = 11

Rdc = 39 m Ohm

Switching frequency = 30 kHz

H=0.0701 cm

δ = 0.378*10^(-3)

$$Rac = \frac{H}{\delta} * Rdc$$

=72.3 m

ΔIL=0.67

$$Irms = \frac{\Delta IL}{\sqrt{3}}$$

= 0.38

Power Loss_per layer = $Irms^2 * Rac$

= 10.44 mW

Total Loss= 44*Loss_per layer

= 0.46 W

Loss Budget= Stage_1 (Conduction Loss + Switching Loss) + Stage_2 (Conduction Loss + Switching Loss) + Inductor Loss

=6.529 W

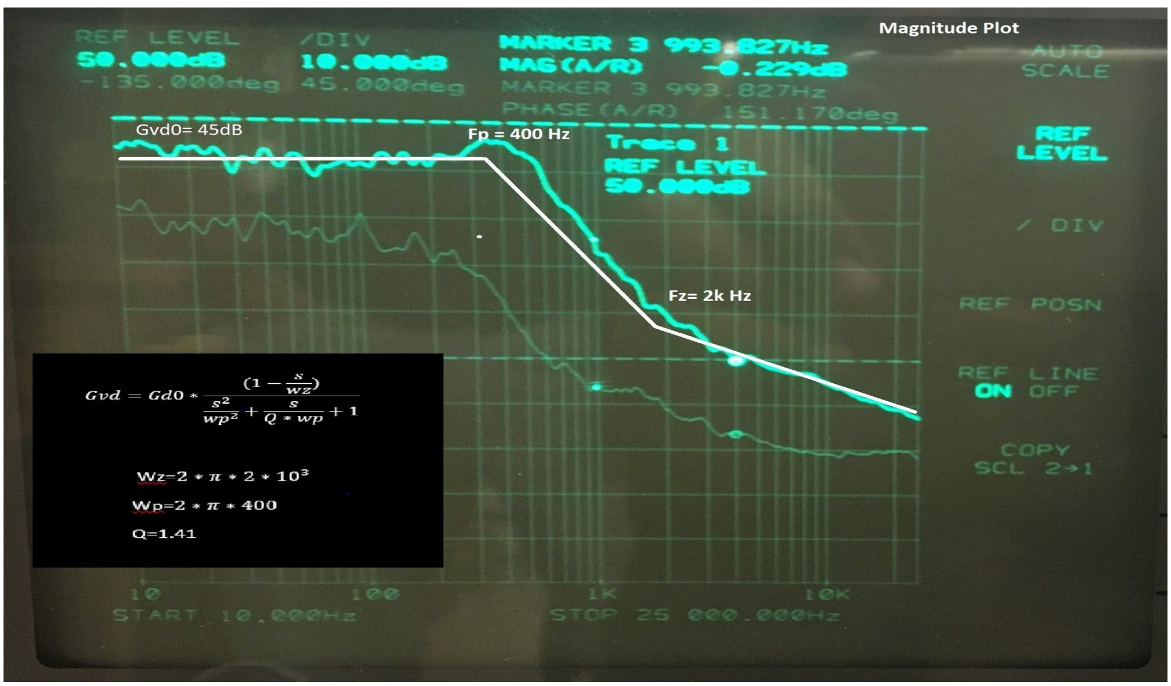
Suggestions for Increasing Efficiency

- The MUR440 diode has a switching loss of 0.18W approximately. A better diode with lower reverse recovery can be used
- The first stage inductor was designed with 16AWG but a 17AWG wire was used for winding
- There is some copper loss on interconnect wires. An 18 AWG wire was used. Reducing the gauge and better layouts can improve efficiency

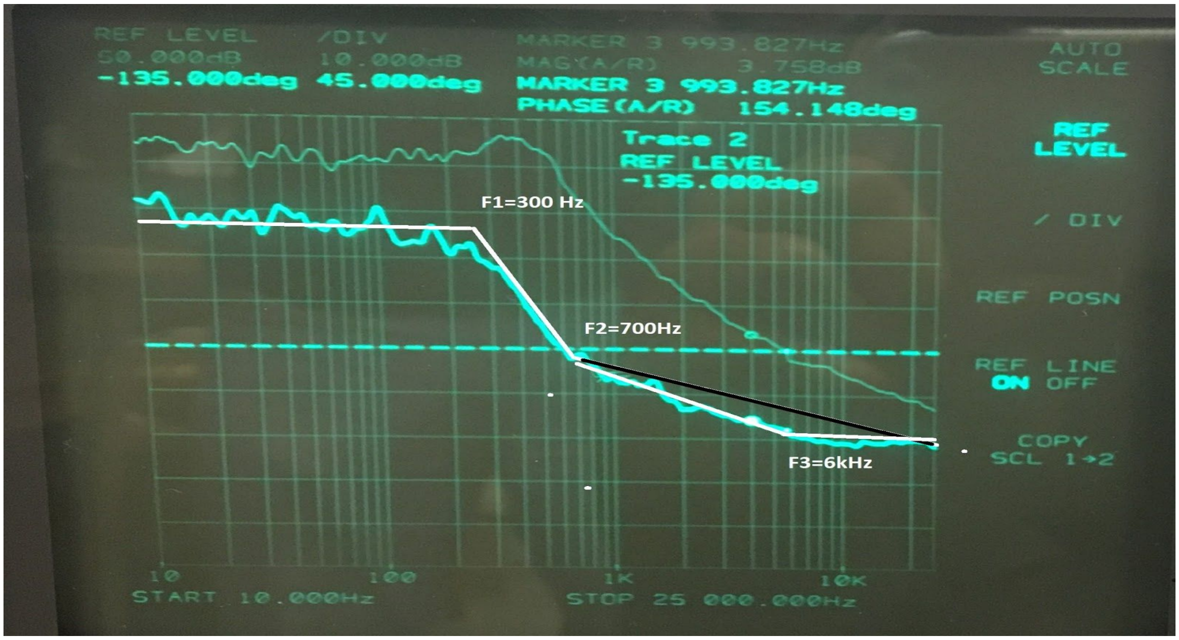
Network Analyzer Measurements

Gvd(s) Magnitude plot:

Operation Conditions: Vin: 11.9V, Vout: 150V, D: 0.717; Output Power: 86W



Gvd(s) Phase Plot



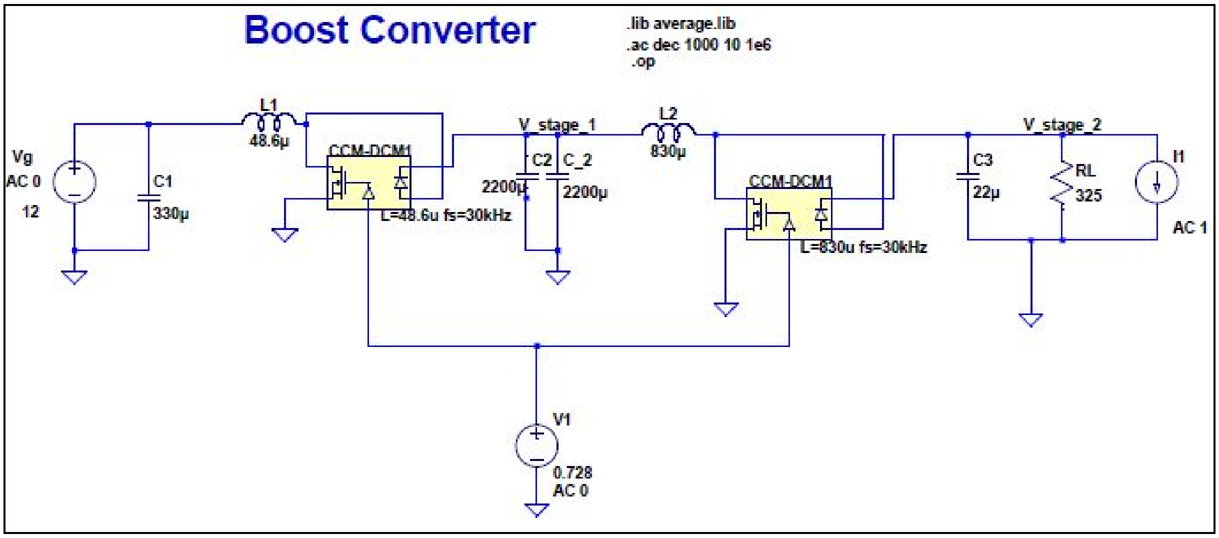
Gvd(s) Expression from measured plot

$$Gvd = Gd0 * \frac{(1 - \frac{s}{wz})}{\frac{s^2}{wp^2} + \frac{s}{Q * wp} + 1}$$

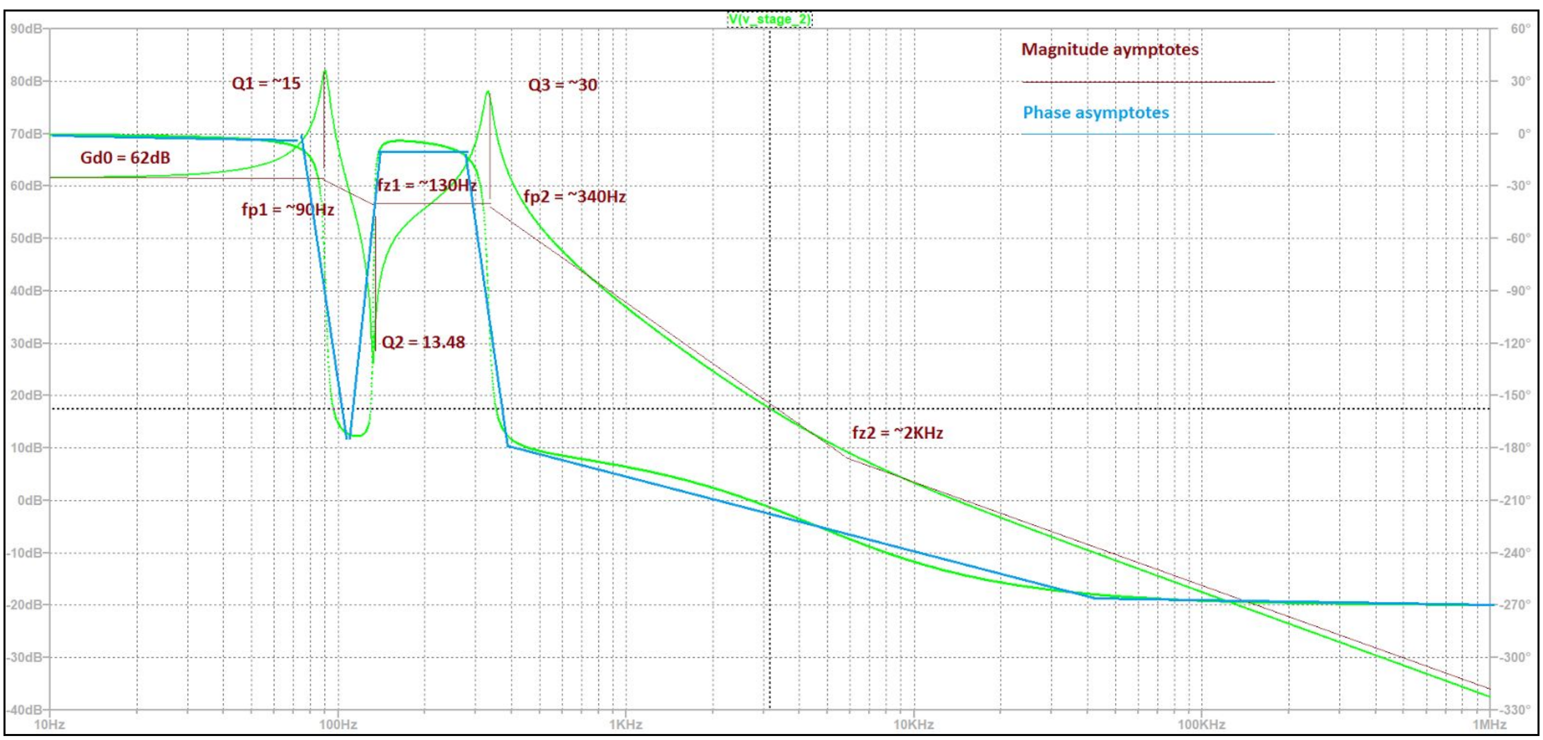
Gd0 = 177.8
fZ = ~2000 Hz
fP = ~400Hz
Q = 2.98dB = 1.41

LT-Spice Simulations

Schematics



Gvd(s) Magnitude Plot



Gvd(s) Expression

From the plot above we can see that the Gvd(s) has following salient features:

- Dc Gain Gdo = ~62dB = 1258.92
- Quadratic pole at fP1 = ~90Hz; QP1 = ~15
- Quadratic zero at fZ1 = ~130Hz, QZ1 = 13.48
- Quadratic pole at fP2 = ~340Hz, QP2 = 30
- Right half plane zero at fZ2 = ~2KHz

The final expression can be therefore written as:

$$G_{vd}(s) = G_{d0} * \frac{\left(1 + \frac{s}{Q_{Z1} * wZ1} + \left(\frac{s}{wZ1}\right)^2\right) * (1 - \frac{s}{wZ2})}{\left(1 + \frac{s}{Q_{P1} * wP1} + (\frac{s}{wP1})^2\right) * (1 + \frac{s}{Q_{P2} * wP2} + (\frac{s}{wP2})^2)}$$

Comparison of simulated and measured Gvd(s)

The measured and simulated Gvd(s) differ in following aspects:

- The measured Gvd(s) shows only a single quadratic pole at ~400Hz. This matches with fP2 at 340Hz of the simulated plot. The first quadratic pole and quadratic zero does not show up in measured plot
- The Q factor at fP2 on measured plot is 1.14 approx. This is much lower than Q at fP2 of simulated plot (30 approx)
- In the measured plot Gvd(s) crosses over at 4KHz with a phase of -150 degrees. The simulated plot crosses over at 15Khz with -240 degrees phase

The differences in plots can be attributed to the following:

- The actual circuit is well damped because of device and interconnect resistances. The model takes into account only inductor resistances
- There is switching loss in the circuit that is not accounted for in the simulation
- Additional loop inductances effect corner and crossover frequencies that the simulation does not account for

Analytical derivation for Gvd(s)

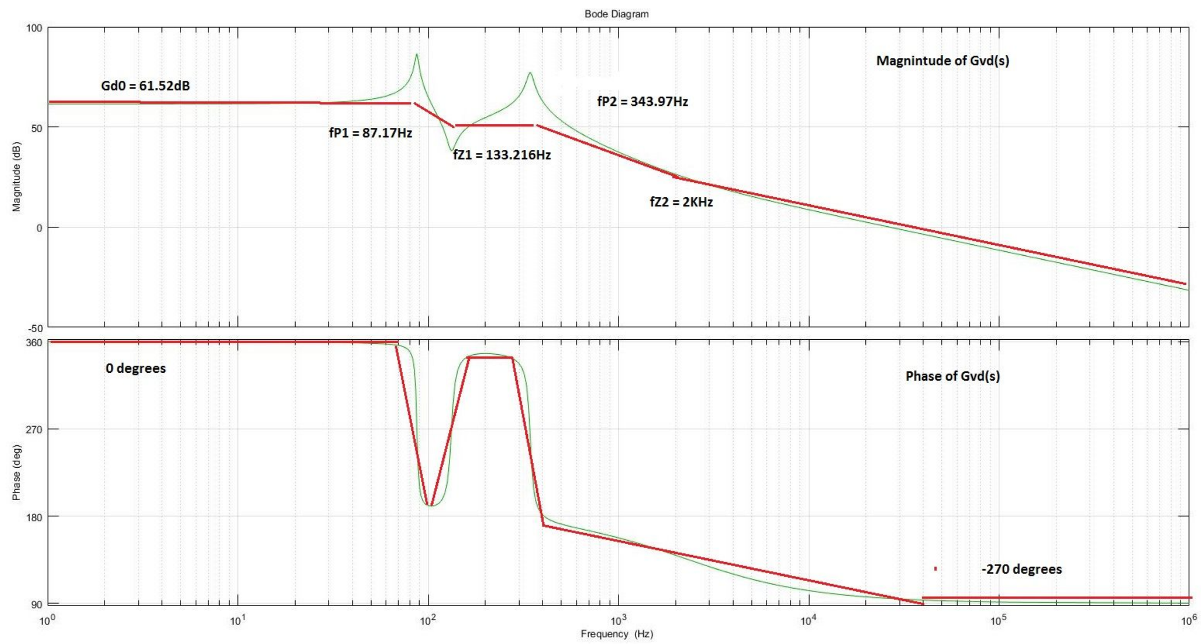
Analytical derivation of the small signal is shown in **Appendix-I**. The final equation is shown here for convenience.

$$G_{vd}(s) = G_{d0} * \frac{\left(1 + \frac{s}{Q_{Z1} * wZ1} + \left(\frac{s}{wZ1}\right)^2\right) * (1 - \frac{s}{wZ2})}{\left(1 + \frac{s}{Q_{P1} * wP1} + (\frac{s}{wP1})^2\right) * (1 + \frac{s}{Q_{P2} * wP2} + (\frac{s}{wP2})^2)}$$

- The derived expressions has same salient features as the simulated expression. It contains following salient features:
- Dc gain Gdo = 61.52dB
- Quadratic pole at fP1 = 87.17Hz; QP1 = 29.52
- Quadratic zero at fZ1 = 133.216HZ; QZ1 = 13.48
- Quadratic pole at fP2 = 343.97Hz; QP2 = 15.45

- Right Half-plane zero fZ2 = 2KHz

The analytical uncompensated MATLAB plot is shown below:



The simulated and analytical plots match quite well.

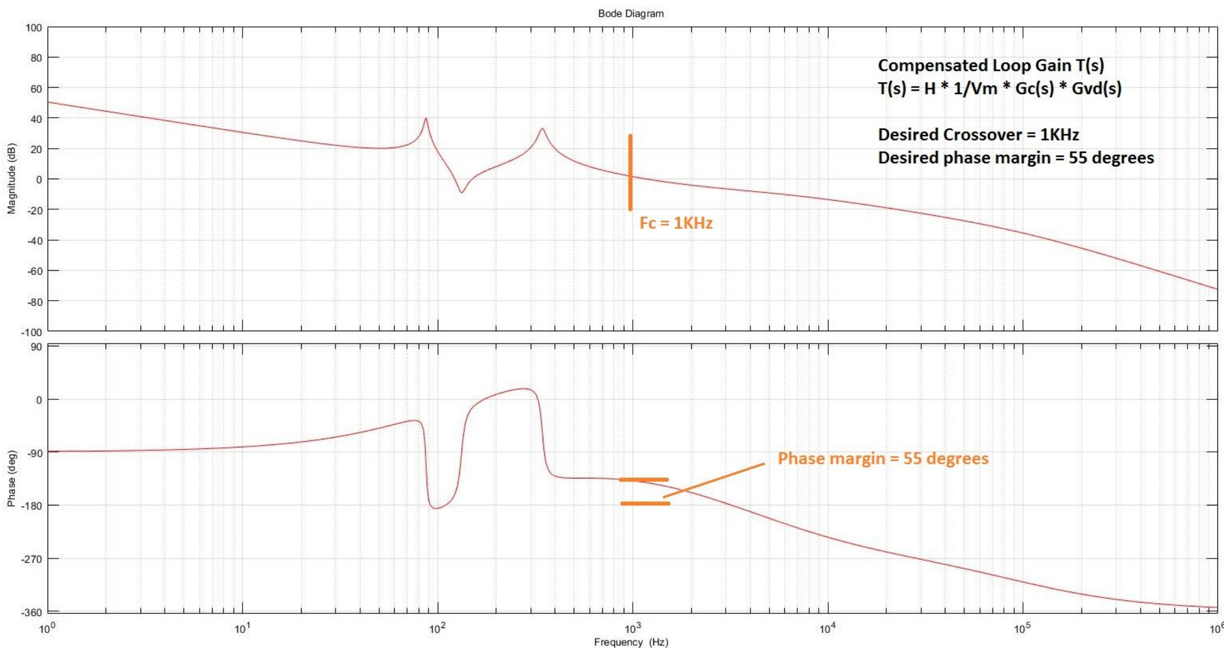
Compensator Design

Proposed Compensator Design

The compensator was designed based on the LT-Spice simulated Gvd(s).

- The crossover frequency was chosen at 1KHz
- The system was designed for a phase margin of 55 degrees

The plot of the compensated loop gain T(s) is shown below:



Compensator calculations

A PID compensator was chosen:

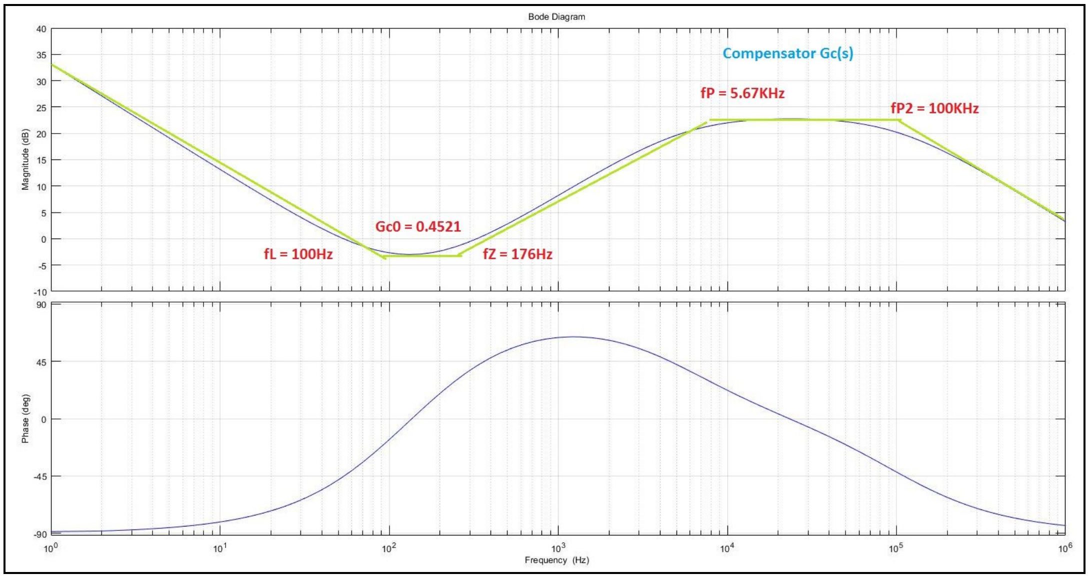
$$Gc(s) = Gc0 * \frac{(1+wL/s) * (1+s/wZ1)}{(1+s/wP1) * (1+s/wP2)}$$

- The uncompensated loop gain has a phase of -203 degrees at crossover. To achieve a PM of 55 degrees compensator needs to provide 70 degrees at 1KHz.
- Thus, the lead zero-pole frequency are found as:

$$fz = fc * \sqrt{\frac{1 - sin\theta}{1 + sin\theta}} = 176.32\text{Hz}$$

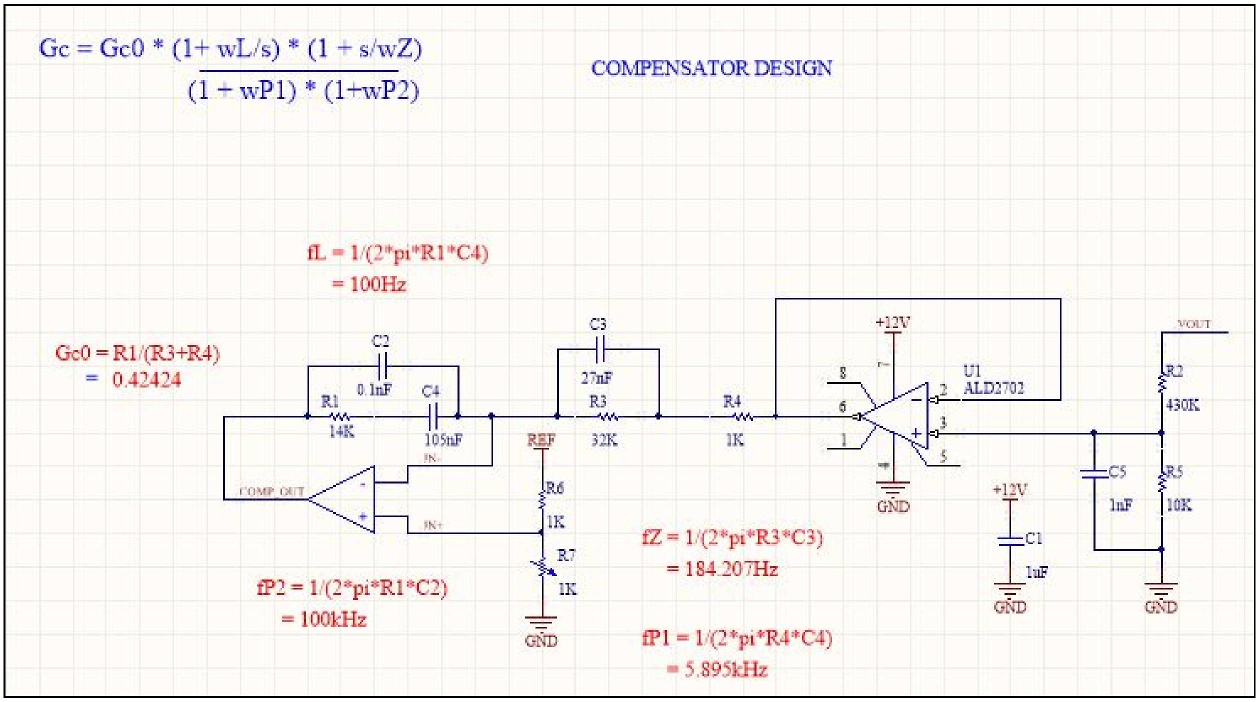
$$fp = fc * \sqrt{\frac{1 + sin\theta}{1 - sin\theta}} = 5.67\text{KHz}$$

- A high frequency pole fp2 is placed at 100KHz for noise immunity
- The PI inverted zero frequncy f_L is placed at 1/10th of crossover frequency:
  f_L = 100Hz
- Mid frequency gain, Gco is calculated at crossover frequncy as:
  $Gc0 = Vm*wZ / (H* |Gd0|_{fc=1KHz} * wC)$
  = 0.4521


Bode Diagram
Compensator Gc(s)
fP = 5.67KHz
fP2 = 100KHz
Gc0 = 0.4521
fL = 100Hz
fZ = 176Hz
Magnitude (dB)
Phase (deg)
Frequency (Hz)

Compensator Circuit

Calculations are shown on the circuit itself:



Load Test

Vin (V)	Iin (A)	Pin (W)	Vout (V)	Iout (A)	Pout (W)	Eff (%)	Duty
12.06	1.662	**20.04**	152.6	0.122	**18.6172**	**92.9**	0.54
12.06	8.71	**98.42**	152.5	0.579	**87.6606**	**89.1**	0.72

Load Regulation (%) = (152.6 - 152.5) * 100 / (152.5) = 0.065%

Line Test

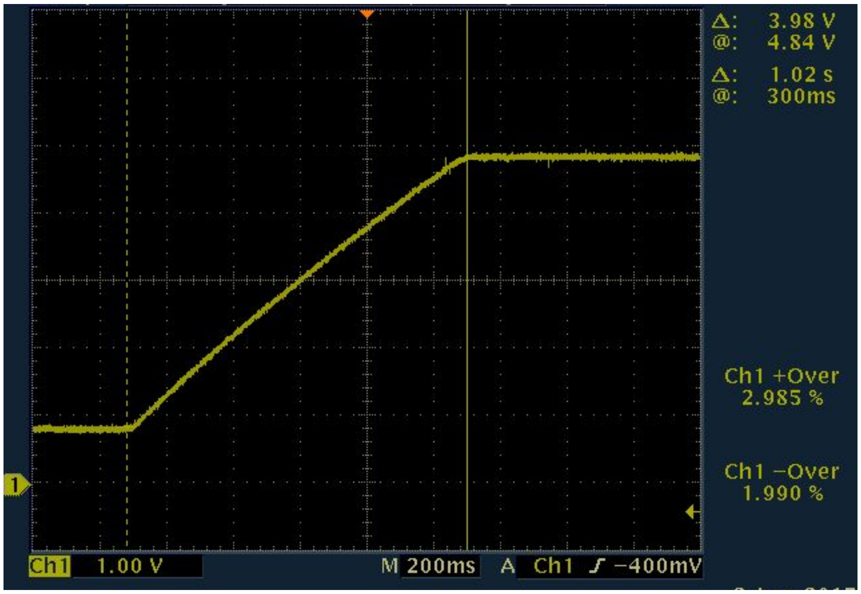
Vin (V)	Iin (A)	Pin (W)	Vout (V)	Iout (A)	Pout (W)	Eff (%)	Duty
11.06	8.785	**97.16**	150.5	0.574	**86.39**	**88.9**	0.75
14.05	6.764	**95.03**	150.6	0.573	**86.29**	**90.8**	0.71

Load Regulation (%) = (150.6 - 150.5) * 100 / (150.5) = 0.066%

Soft Start

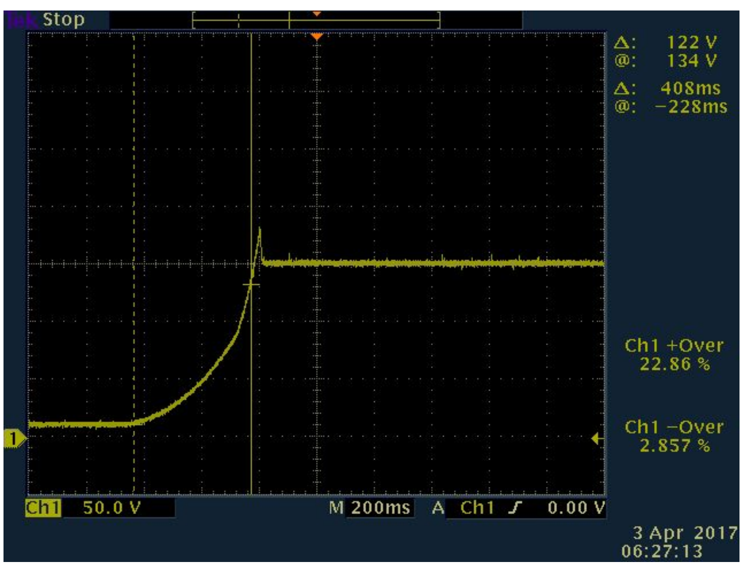
Soft Start capacitor value: 10uF

VRef transient on soft start

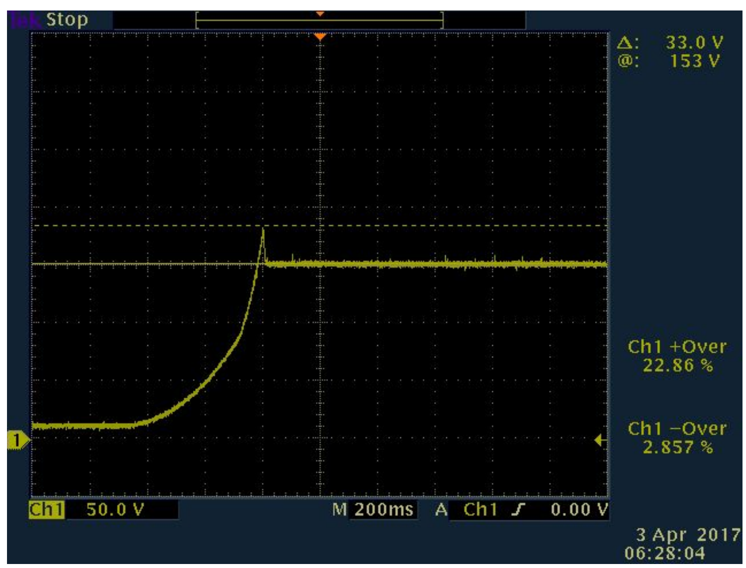


VOUT Transient on Soft Start

Soft Start Transient



Overshoot

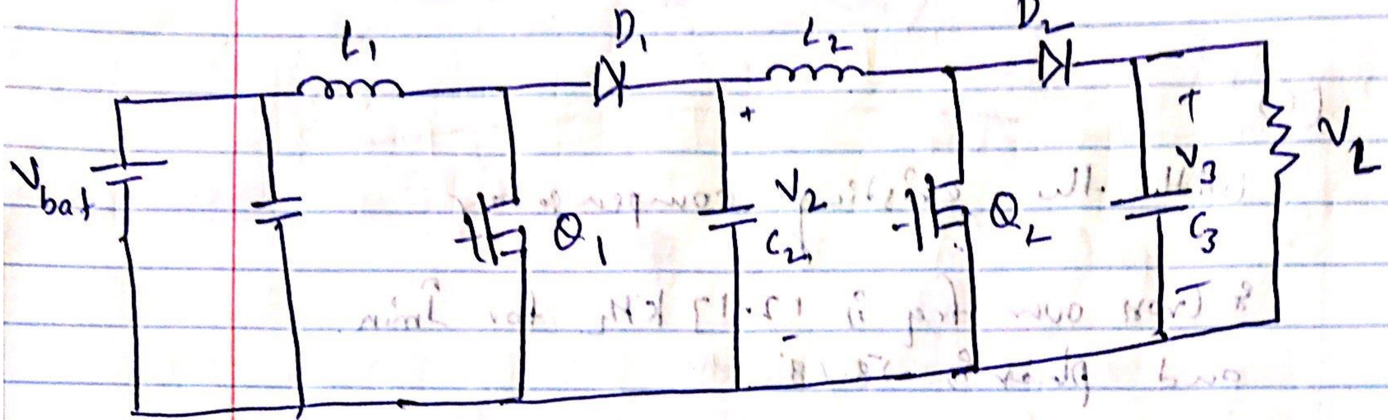


Conclusion

- A cascaded dc-dc boost converter rated for 100W was designed, constructed and tested as per the given specifications. The peak efficiency of 92% was measured
- An analog PID compensator was designed to regulate the output voltage of the boost converter

Appendix-1

Small signal analysis



Q_1, Q_2 - ON:

$V_{L_1} = V_1$ $\quad$ $i_{C_2} = -i_{L_2}$

$V_{L_2} = V_2$ $\quad$ $i_{C_3} = -i_{load}$

Q_1, Q_2 - off

$V_{L_1} = V_1 - V_2$ $\quad$ $i_{C_2} = i_{L_1} - i_{L_2}$

$V_{L_2} = V_2 - V_3$ $\quad$ $i_{C_3} = i_{L_2} - i_{load}$

$$L_1 \frac{di_{L_1}}{dt} = V_1 - D' V_2 \qquad C_2 \frac{dV_2}{dt} = D' i_{L_1} - i_{L_2}$$

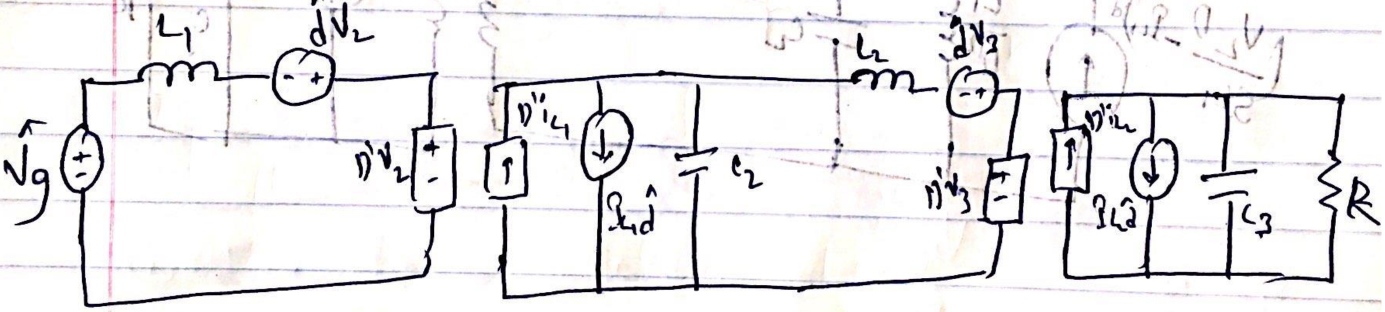
$$L_2 \frac{di_{L_2}}{dt} = V_2 - D' V_3 \qquad C_3 \frac{dV_3}{dt} = D' i_{L_2} - i_{Load}$$

$$L_1 \frac{d\hat{i}_{L_1}}{dt} = \hat{v}_1 - D'\hat{v}_2 + \hat{d}V_2$$

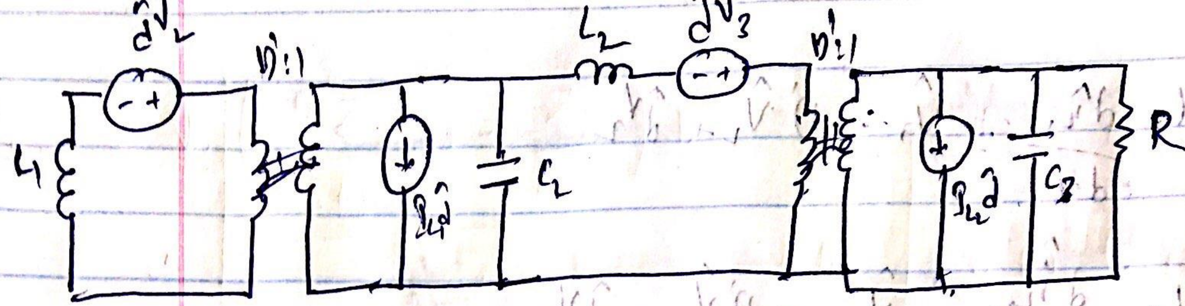
$$L_2 \frac{d\hat{i}_{L_2}}{dt} = \hat{v}_2 - D'\hat{v}_3 + \hat{d}V_3$$

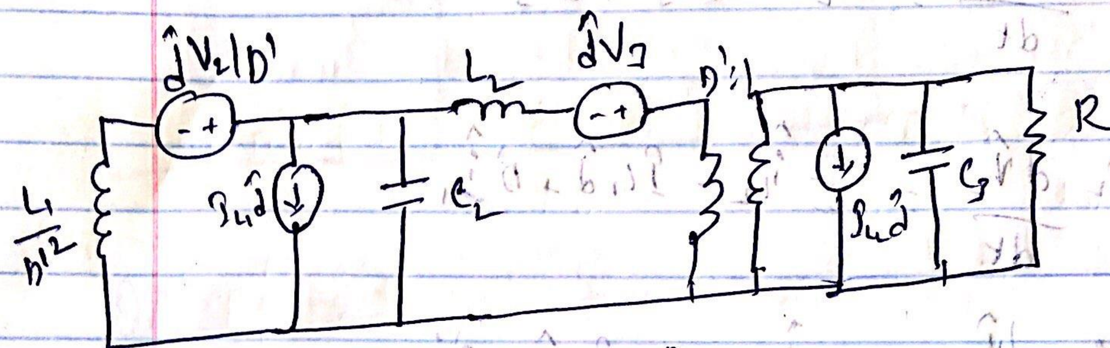
$$C_2 \frac{d\hat{v}_2}{dt} = -\hat{i}_{L_2} - I_{L_1}\hat{d} + D'\hat{i}_{L_1}$$

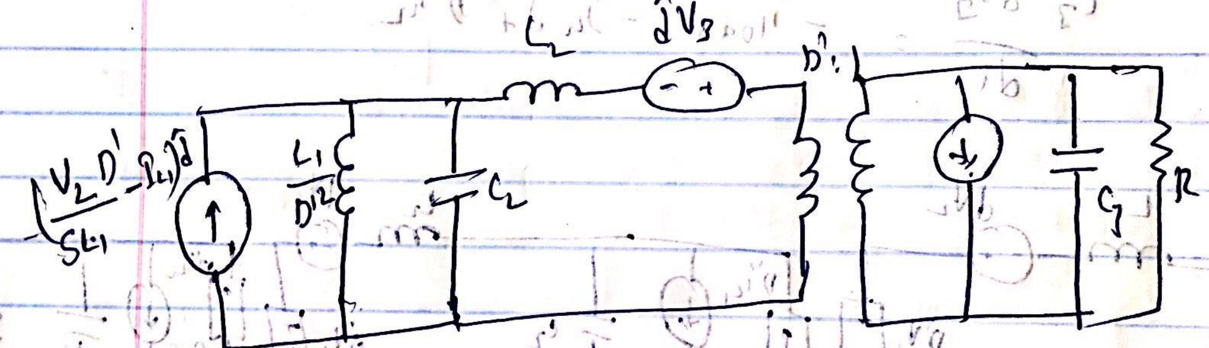
$$C_3 \frac{d\hat{v}_3}{dt} = -\hat{i}_{load} - I_{L_2}\hat{d} + D'\hat{i}_{L_2}.$$



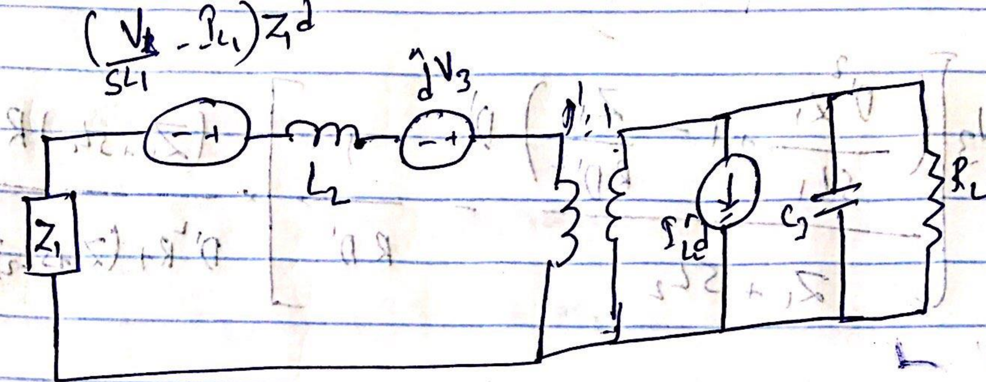
$$G_{vd} = \frac{\hat{v}}{\hat{d}}\bigg|_{\hat{v}_g = 0}$$

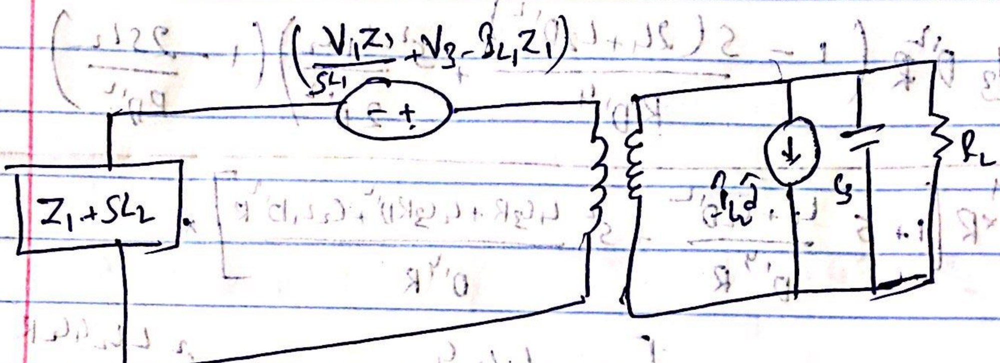






$$Z_1 = \frac{\frac{sL_1}{D'^2} \times \frac{1}{sC_2}}{\frac{sL_1}{D'^2} + \frac{1}{sC_2}} = \frac{sL_1}{s^2 L_1 C_2 + D'^2}$$





$$\left(\frac{\frac{V_1 Z_1}{sL_1} + V_3 - I_{L1} Z_1}{Z_1 + sL_2} \times D' - I_{L2}\right)\left(\frac{Z_1 + sL_2}{D'^2} \,\|\, R_L \,\|\, C_3\right) = \frac{\hat{V}_0}{\hat{d}}$$

$$G_{vd} = \left[\left(\frac{\frac{V_1 Z_1}{sL_1} + V_3 - \frac{V_3}{RD'^2} Z_1}{Z_1 + sL_2}\right) D' - \frac{V_3}{RD'}\right] \frac{(Z_1 + sL_2)R}{D'^2 R + (Z_1 + sL_2)(s C_3 R + 1)}$$

$$G_{vd} = V_3\left[\frac{\left(\frac{D'^2 Z_1}{sL_1}+1-\frac{Z_1}{RD'^2}\right)D'}{Z_1+sL_2} - \frac{1}{RD'}\right] \times \frac{(Z_1+sL_2)R}{D'^2R+(Z_1+sL_2)(sC_3R+1)}$$

$$= \frac{2V_3 D'^2 R\left(1+\frac{s(2L_1+L_2D'^2)}{RD'^4}+s^2\frac{L_1C_2}{2D'^2}\right)\left(1-\frac{2sL_2}{RD'^2}\right)}{D'^3 R\left[1+s\frac{L_1+L_2D'^2}{D'^4R}+s^2\frac{L_1C_3R+L_2C_3RD'^2+C_2L_1D'^2R}{D'^4R}\right] \times \left[1+s\frac{L_1L_2C_2}{L_1C_3R+L_2C_3RD'^2+C_2L_1D'^2R}+s^2\frac{L_1L_2C_3C_2R}{L_1C_3R+L_2C_3RD'^2+C_2L_1D'^2R}\right]}$$

$$\text{Gain} = \frac{2V_3}{D'} = 1191.17 = 61.519\,dB$$

RHP zero $\Rightarrow$ $\omega_z = 14.484$ krad/s

$f_z = 2.3\,kHz$

Quadratic zero

$$\omega_{z_1} = 837.02 \text{ rad/s}$$

$$f_{z_1} = 133.216 \text{ Hz}$$

$$Q = 13.48$$

Poles

$\omega_{p_1} = 2161.25$ rad/s $\omega_{p2} = 547.72$ rad/s

$f_{p_1} = 343.97$ Hz $f_{p_2} = 87.17$ Hz

$Q_1 = 15.45$ $Q_2 = 29.52$