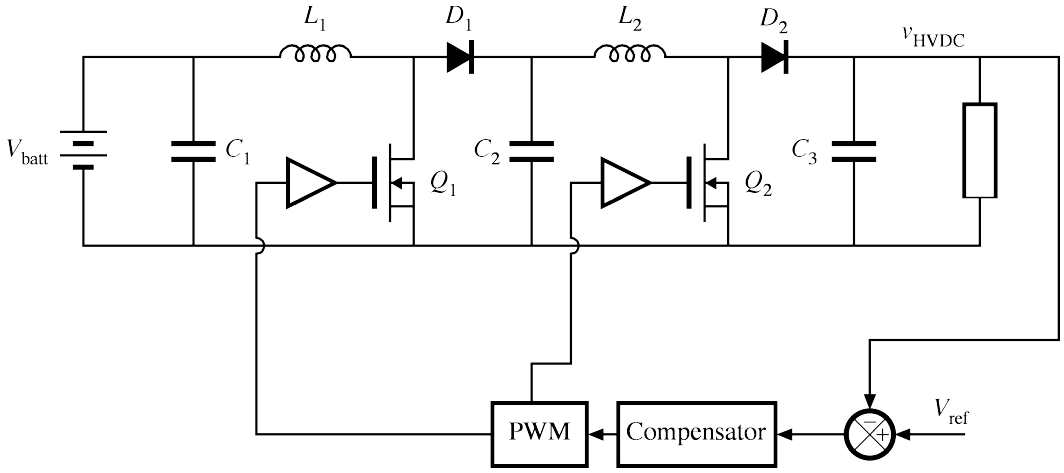
Background

The primary objective of Experiment 4 is to design, construct, test, and demonstrate a step-up dc-dc converter that converts the low-voltage dc produced by the lead-acid battery to a high-voltage dc as needed by the dc-ac inverter of Experiment 5. An additional objective of this experiment is to design, construct, test, and demonstrate a closed-loop analog feedback loop that regulates the dc output voltage of your converter.



In your prelab assignment, you have designed the power stage of the system illustrated in Fig. 1, based on cascaded boost converters, including selection of switching frequencies f_s and duty cycles D_1 and D_2, design of the inductors L_1 and L_2, and selection of the semiconductor components.

Laboratory Procedure

1. Analog Pulse-Width Modulator

Your parts kit includes an analog PWM chip UC3525A, whose operation was described in Lecture 7. Design a circuit around the UC3525A such that the gate drive signal to be applied to the gates of the power MOSFETs have the switching frequency that you chose in your prelab design. Your circuit should include a potentiometer for adjusting the duty cycle, and the maximum duty cycle should be limited to a value greater than your intended operating points but less than 100%. Your circuit should include bypass capacitors on all power supplies.

A dc supply voltage of V_{CC} = 12 V is available. You may use an adjustable trimmer potentiometer for duty cycle adjustment, and as many resistors and capacitors as necessary.

Supply Voltage Decoupling

In all circuits, especially those that produce pulsating waveform, decoupling capacitors are essential to ensure that the dc supply voltage is undisturbed by large current transitions and spikes, and to prevent propagation of noise through the power distribution circuitry. Without decoupling capacitors, current spikes and transitions can cause large voltage transients and oscillations on the power supply wires, because of inductance of the wiring. Such voltage "spikes" and "ringing" can disrupt operation of all devices connected to the power supply.

It is necessary to ensure that adequate capacitors are included in your circuitry for power supply decoupling. Here are some suggestions:

- Between the positive supply and ground terminals of the analog controller circuit board, connect an electrolytic capacitor of at least 10 μF (in the case of a power converter circuit board, a considerably larger capacitance may be required). This capacitor filters low-frequency variations in the power supply. Note that this electrolytic capacitor is polarized; connecting it to a power source with the wrong polarity will cause the capacitor to fail.
- For all integrated circuits on the controller board, a ceramic capacitor of at least 0.1 μF should be connected between each power supply pin and ground pin, as close as possible to the chip. This capacitor filters high-frequency variations in the power supply. Gate driver circuitry often requires additional high-frequency decoupling capacitance, perhaps 1 μF or more.

Constructing and Debugging Test Circuits

Do not forget to power down the circuit before you make any additions or changes to the circuit. This is especially important in later experiments that drive the converter power stage. Turn on the power only after you have checked that your connections are correct. In particular, always check the polarity of the power supply connections to the chips.

If your circuit does not work, it is suggested that you troubleshoot it in a systematic manner. Use the oscilloscope to view the voltage waveforms at every pin of the first chip, beginning with its input. Are they as you expect? If not, then you have localized the problem. When the operation of the first chip is correct, then repeat the process for the next chip.

Controller Circuit Demonstration

Construct the circuit that you designed above. Your output should be a PWM waveform with switching frequency f_s equal to the value you chose in your prelab assignment, and with duty cycle D adjustable between 0 and a suitable maximum limit.

A dc supply voltage of V_{CC} = 15 V is available on the bench, and a 12 V supply is available on the PV cart. You can use a potentiometer for duty ratio adjustment, and as many other resistors and capacitors as needed around the UC3525A chip. If necessary, adjust the component values so that the actual switching frequency and maximum duty cycle are within 5% of the specified values.

In your report, you should include:

- A complete, labeled circuit diagram of the PWM circuit with labeled component names and values.

- Capture the waveforms of all 16 pins of the chip. The waveforms should be aligned in time, and labeled with all important values. Note that some oscilloscopes in the lab can capture bitmapped screen shots over the Ethernet, which can be viewed using a browser on the lab computers. For the other oscilloscopes, these files can be saved onto floppy disk. Use the multimeter to measure the voltages at pins where the voltages are dc. The waveforms and voltage values should be measured at $D = 60\%$.

2. Open-Loop Power Stage

Construct the inductors that you designed in your prelab assignment. Measure the inductances and iterate as necessary. Report the measured values in your report.

Construct the boost converters on your perf board. The following loops should be kept small: Q_1-D_1-C_2, Q_2-D_2-C_3, and the gate drive connections. Heatsinking of the power semiconductors is needed. You will derive the converter input power from the laboratory 0-35V 0-10A bench supply; set this supply initially to zero. Connect an appropriate variable power resistor to the output of your converter. Connect meters to measure the output voltage and current.

Note: When the load is disconnected, the output voltage of the boost converter can tend to a very large value! Be sure that your load is connected. Also be sure that the fuse is not blown in the ammeter you are using to measure the load current.

Note: In this experiment, dangerous voltages in excess of 100 V will be generated! Use caution in testing the circuit, do not touch the power-stage components, and be sure to turn off V_g before making changes to the circuit. Use x10 voltage probes when connecting the oscilloscope to the power stage. Note that, if you don't isolate the case of the power MOSFET and then ground the heatsink, then the heatsink will operate at the high voltage present at the MOSFET drain.

For the initial test, keep the 0-35V bench supply turned off. Power the controller, adjust the duty cycle to the nominal value for your design, and verify that the proper gate drive signals are observed on MOSFETs Q_1 and Q_2.

Next, measure the MOSFET drain-to-source voltages on the oscilloscope. With your load rheostat set to its maximum resistance, turn on the bench power supply, and slowly increase the input voltage to several volts. Observe the MOSFET drain-to-source voltages, especially the voltage spikes that occur during the turn-off transitions of the MOSFETs. These voltage spikes can damage the MOSFETs if they exceed the rated drain-to-source voltages. If the spikes are large, it may be necessary to improve the layouts of the Q_1-D_1-C_2 or Q_2-D_2-C_3 loops. Also check the gate-to-source voltages for increased ringing and spikes; note that the gate ringing increases when the main power is applied. If the ringing approaches the rated

gate-to-source voltage, then it will be necessary to improve the layout of your gate drive circuitry.

Slowly increase the input voltage and the load current, until your converter is able to run at the nominal design point of 85 W output at 200 V, with an input voltage of 12 V. Record the MOSFET voltage waveforms, as well as the converter input and output voltage and current. What is the converter efficiency?

ECEN 5517 Additional Assignment

Revise the converter loss budget that you developed in the prelab assignment, to account for the measured efficiency. Your updated loss budget should include at least the following:

- All transistor and diode conduction losses.
- Switching losses, estimated from measured MOSFET voltage and current waveforms during the switching transitions.
- Inductor losses: dc copper loss based on your final design, core loss based on published core material data, and proximity loss based on calculations with your measured Δi_L and with your final winding geometry.

Document the above measurements and calculations fully in your final report. What steps could you reasonably take to improve your efficiency?

3. Feedback Controller

The goal of this part is to construct a feedback loop to regulate the high voltage dc output to a constant value, regardless of load or input voltage variations. Work on this part only after you have finished the open-loop tests of parts 1 and 2.

Small Signal AC Transfer Functions

For this part, you will operate your dc-dc converter open-loop (as in part 2 above). The objective is to determine the small-signal ac control-to-output transfer function, from pin 2 of the UC3525 to the high-voltage output. You will use a network analyzer to measure this transfer function in the lab, and you will use Spice to simulate the transfer function using the averaged switch model.

There are two HP3577 network analyzers available in the laboratory. These analyzers are required for the first step below. Note that the measurement and simulation steps below are independent, and so can be performed in any order. It is ok to skip ahead to the simulation step while you are waiting for a network analyzer to become available.

Transfer Function Measurement

Connect your converter to operate open-loop, as in Part 2. A potentiometer should be connected to provide an adjustable dc voltage to pin 2 of the UC3525, to set the quiescent duty cycle. Adjust the converter input power supply, load resistance, and duty cycle so that

the converter operates at the nominal dc operating point of 170 V and 85 W. Note the value of the quiescent duty cycle. Also measure the peak-to-peak amplitude of the sawtooth voltage at pin 5 of the UC3525.

Use an HP3577 network analyzer to measure the small-signal transfer function from pin 2 of the UC3525 to the output voltage of your cascaded boost converter, at the quiescent operating point given above. Such measurements are discussed in Section 2.5 of the converter transfer functions tutorial.

Caution: the input amplifiers of the HP 3577 are similar to oscilloscope inputs, and are rated **25V peak**. Do not connect the high voltage output of your converter directly to the network analyzer inputs, or you will destroy this expensive instrument! Use the x10 probes provided with the network analyzer inputs; these will divide the measured voltages by a factor of 10, so that the dc voltage applied to the analyzer input channel is 170/10 = 17 V.

Also note that the injection source and the input channels of the analyzer are connected to the chassis of the analyzer, which is connected through the power plug to earth ground. Therefore, the analyzer cannot make floating measurements, nor can it make floating injections. To avoid disrupting the quiescent operating point, it is necessary to employ a suitable dc blocking capacitor between the injection source and pin 2 of the UC3525, as illustrated in Fig. 2.40 of the tutorial.

A page is taped to the top of the network analyzer, listing the buttons that must be pushed to set it up for a frequency response measurement. This page is also on the course website under the Experiment 4 folder. Follow the steps, and obtain a Bode plot of the magnitude and phase of the transfer function. Obtain a hard copy.

In your report, fit asymptotes to your measured Bode plot magnitude and phase plots. These asymptotes must follow all of the usual rules for Bode plots: the magnitude asymptotes must have slopes that are multiples of 20 dB/decade, and the phase asymptotes must have slopes that follow the rules (multiple of 45°/decade for real poles and zeroes, or slopes of ± 180Q°/decade for complex poles and zeroes). Hence deduce the measured transfer function, along with the numerical values of its dc gain, corner frequencies, Q-factors, and (right half-plane) zeroes.

Simulation

Simulate your dc-dc converter using the averaged switch model discussed in lecture and in Section 2.4 of the tutorial. The PSpice library switch.lib can be downloaded from the course website, and contains many averaged switch models including CCMl, CCM3, and CCM-DCMl. The course website also contains PSpice files for all of the simulation examples in the tutorial. You may use LTspice if you prefer. Perform an ac frequency response simulation of your dc-dc converter, at the operating point of your experimental measurement. Plot the magnitude and phase of the transfer function from pin 2 of the UC3525 to the output voltage of the converter.

Section 2.4.6 of the tutorial contains an ac frequency response analysis of the SEPIC (see Fig. 2.33); this example is a good starting point for your simulation. Note that the transistor and diode are replaced by the averaged switch model CCM-DCMl (CCM-DCMl requires that the inductor value and switching frequency be supplied as parameters). The voltage source v_c contains a dc component that sets the quiescent duty cycle, as well as an ac component that provides that ac modulation of the duty cycle. To get PSpice to perform a frequency response analysis, the ".ac" statement causes the frequency of any ac sources (i.e., v_c) to be swept from 5 Hz to 50 kHz, with 20l points per decade. PROBE is used to plot the magnitude and phase data in Fig. 2.34.

In the report:

- Fit asymptotes to your simulated Bode magnitude and phase plots. These asymptotes must follow all of the usual rules.
- Hence deduce the predicted transfer function, along with numerical values of the dc gain, corner frequencies, Q-factors, and zeroes.
- Compare the measured and simulated results. How well do they agree? If there is a significant disagreement in any of the data, discuss its possible origins.

ECEN 5517 Additional Assignment

Construct a small-signal equivalent circuit model for your converter power stage. Solve this model analytically to find the control-to-output transfer function. Use your numerical values to justify approximations as appropriate, and hence compute the numerical values of the dc gain, corner frequencies, Q-factors, and zeroes.

If you know how, you may wish to add an R-C damping network in parallel with capacitor C_2. This can simplify the dynamics considerably. Extra credit will be assigned to groups that design and demonstrate a damping network that substantially improves the control-to-output transfer function.

Compensator Circuitry Design

Design the best feedback loop that you can, to control the converter with low overshoot and wide bandwidth. Design and construct feedback and compensator circuitry to implement your proposed loop gain. In your report, turn in a Bode plot of your proposed loop gain, including the required compensator gain, the circuit, and identify the crossover frequency and phase margin.

Note: if you use an external op amp for your compensator, then make sure that the op amp cannot drive the UC3525 outside its power supply limits!

Feedback loop testing

Connect your compensator circuitry to the dc-dc converter and PWM circuit. Connect a variable dc reference voltage (derived from either a potentiometer or a DAC output of the MSP430) to the reference input of your circuitry. Set the main power supply current limit to a safe value that is higher than the maximum expected converter input current.

Use multimeters to measure the converter output voltage and current, and connect an oscilloscope to measure the gate drive signal. Set the load resistor to its maximum value (minimum current). Turn on the auxiliary power supply (for the PWM chip and compensator circuit). Verify that the gate drive signal has the correct frequency and maximum duty cycle; include these values in your report.

Monitor the MOSFET voltages using 10:1 voltage probes. Turn on the main dc supply, and slowly increase the converter input voltage V_g. The duty cycle should drop below the maximum value as soon as V_g is high enough that the feedback can regulate the output voltage to the commanded value using a duty cycle less than D_{max}. If the input voltage is unable to supply enough current during the start-up procedure, and the duty cycle does not start decreasing, then stop and consult with a teaching assistant or instructor; it may be necessary to implement a soft start circuit (see below) before proceeding. Once the feedback loop starts working and the duty ratio starts decreasing, adjust V_g, V_{ref}, and the load resistance to make the converter operate at your nominal design point. While you are doing this, observe the input current and make sure that the core does not saturate.

Closed-Loop Voltage Regulation: Load Test

With the closed-loop converter brought to the nominal operating point as above, slowly change the load current from the nominal design point to the minimum value you can obtain with the given load rheostat. Record and include in your report the input voltage, output voltage, input current, output current, duty ratio, and converter efficiency at the two extreme points of the load range. A quantity of interest for a voltage regulator is the closed-loop load regulation, i.e., the percent change in the output voltage over the load range:

$$\frac{\Delta V}{V} = \frac{V_{max} - V_{min}}{V_{nominal}} \text{ x } 100\%$$

If the compensator gain at DC and low frequencies is very large, then the closed-loop regulation should be very good, i.e., very close to 0%. Include the measured value in your report.

Closed-Loop Voltage Regulation: Variations in Input Voltage

With the closed-loop converter operating at the nominal design point, slowly change the input voltage in the range from 11 V to 14 V. Observe the input current to make sure that the inductors do not saturate, and observe the peak MOSFET voltages to make sure that the MOSFET voltage ratings are not exceeded. Record and include in your report the input voltage, output voltage, input current, output current, efficiency, and duty ratio at the extreme values of input voltage. Find the closed-loop output voltage regulation for variations in input voltage.

Soft start circuitry

During start up in closed-loop converters, the switch duty cycle operates at the maximum limit D_{max} as long as the output voltage is less than the regulated value. This typically leads to a large inrush current during the startup transient, which can overload the input power source or damage the converter power components.

In practical designs, this problem can be solved by use of a "soft start" circuit that slowly increases the switch duty cycle from zero to the final regulated value. On the UC3525 chip, the soft-start feature is implemented by a capacitor C_s connected from pin 8 to ground. The output duty cycle is determined by the lower of the pin 8 capacitor voltage and the PWM input voltage at pin 9. When the UC3525 is powered up, capacitor C_s is charged by a current of 50 μA, causing its voltage and the duty cycle to slowly increase.

Find a value of C_s that causes the duty cycle to increase from zero to the nominal value in approximately one second. Test the soft start circuitry as follows:

- Set the converter load resistance to the nominal value.
- Turn off power to the controller board.
- Turn on the converter input power supply and set it to 13 V. Set its current limit to a level somewhat higher than the nominal input current.
- Turn on power to the controller board. The output should reach the regulated value without overloading (current limiting) the converter power supply.

Capture the start-up output voltage transient on the oscilloscope. The oscilloscope should be set to the "single run" mode to capture this one-time event. Measure how long it takes the output voltage to reach the regulated value.