state	HALT	PCwrite	Msrc	Mwrite	IR Write	MDRWrite	LW	LI	RFwd[0]	RFwd[1]	RFwrite
0	0	1	0	0	1	0	0	0	0	0	0
1	0	0	0	0	0	0	0	0	0	0	0
2	0	0	0	0	0	0	0	0	0	0	0
3	0	0	0	0	0	0	0	0	1	1	1
4	0	0	0	0	0	0	0	0	0	0	0
5	0	0	0	0	0	0	0	0	1	1	1
6	0	0	0	0	0	0	0	0	0	0	0
7	0	0	0	0	0	0	0	0	1	1	1
8	0	0	0	0	0	1	0	0	0	0	0
9	0	0	0	0	0	0	0	0	1	1	1
10	0	0	0	0	0	0	0	1	0	0	1
11	0	0	0	0	0	0	0	0	0	0	1
12	0	1	0	0	0	0	0	0	0	0	0
13	0	1	0	0	0	0	0	0	0	0	0
14	0	0	0	0	0	0	1	0	0	0	0
15	0	0	1	0	0	1	0	0	0	0	0
16	0	0	0	0	0	0	0	0	0	1	1
17	0	0	0	0	0	0	0	0	0	0	0
18	0	0	1	1	0	0	0	0	0	0	0
19	0	1	0	0	0	0	0	0	1	0	1
20	1	0	0	0	0	0	0	0	0	0	0

state	SorL	RD1write	RD2write	ALU1[0]	ALU1[1]	ALU2[0]	ALU2[1]	SUB	NOR	BN	BE	JAL
0	0	0	0	0	0	1	0	0	0	0	0	0
1	1	1	1	0	0	0	1	0	0	0	0	0
2	0	0	0	0	1	0	0	0	0	0	0	0
3	0	0	0	0	0	0	0	0	0	0	0	0
4	0	0	0	0	1	0	0	1	0	0	0	0
5	0	0	0	0	0	0	0	0	0	0	0	0
6	0	0	0	0	1	0	0	0	1	0	0	0
7	0	0	0	0	0	0	0	0	0	0	0	0
8	0	0	0	0	1	0	0	1	1	0	0	0
9	0	0	0	0	0	0	0	0	0	0	0	0
10	0	0	0	0	0	0	0	0	0	0	0	0
11	0	0	0	0	0	0	0	0	0	0	0	0
12	0	0	0	1	0	0	0	0	0	0	1	0
13	0	0	0	1	0	0	0	0	0	1	0	0
14	0	0	0	0	1	0	1	0	0	0	0	0
15	0	0	0	0	0	0	0	0	0	0	0	0
16	0	0	0	0	0	0	0	0	0	0	0	0
17	0	0	0	0	1	0	1	0	0	0	0	0
18	0	0	0	0	0	0	0	0	0	0	0	0
19	0	0	0	0	0	0	0	0	0	0	0	1
20	0	0	0	0	0	0	0	0	0	0	0	0