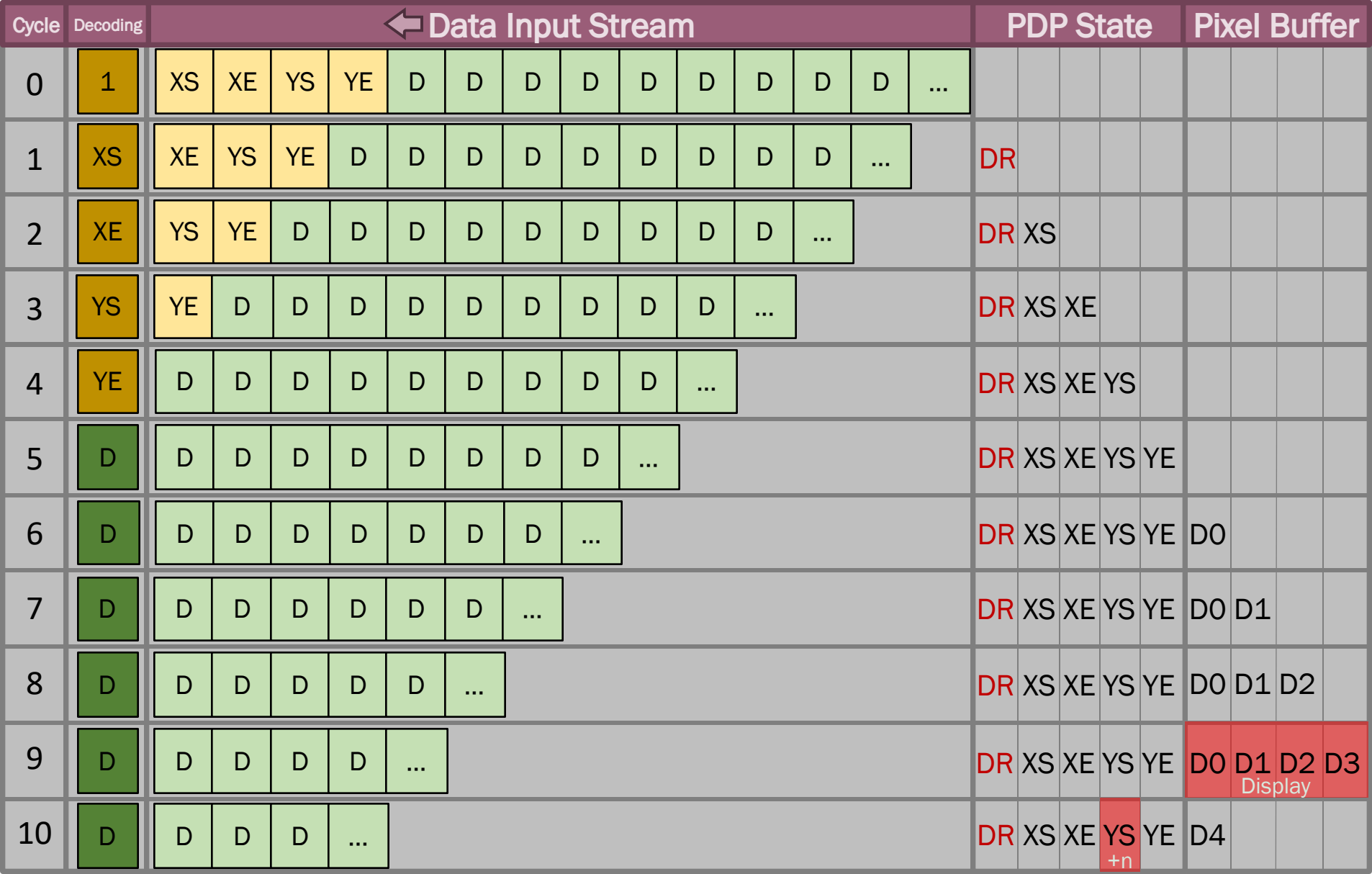
Cycle
Decoding
Data Input Stream
PDP State
Pixel Buffer
0
1
XS XE YS YE D D D D D D D D D ...
1
XS
XE YS YE D D D D D D D D D ...
DR
2
XE
YS YE D D D D D D D D D ...
DR XS
3
YS
YE D D D D D D D D D ...
DR XS XE
4
YE
D D D D D D D D D ...
DR XS XE YS
5
D
D D D D D D D D ...
DR XS XE YS YE
6
D
D D D D D D D ...
DR XS XE YS YE D0
7
D
D D D D D D ...
DR XS XE YS YE D0 D1
8
D
D D D D D ...
DR XS XE YS YE D0 D1 D2
9
D
D D D D ...
DR XS XE YS YE D0 D1 D2 D3
Display
10
D
D D D ...
DR XS XE YS YE D4
+n