SHREYAM NATANI

snatani@ucsd.edu | +1 (858)247-8227 | LinkedIn | Google Scholar

EDUCATION

University of California San Diego
PhD Candidate | Advisor: Prof. Prabhakar Bandaru & Prof. Andrew Kummel — *Exp. Aug 2025*
Master of Science, Mechanical Engineering — *2020*

Indian Institute of Technology, Bombay
Bachelor of Technology (Honors) in Mechanical Engineering — *2018*

RESEARCH EXPERIENCE

Threshold Voltage control of sub - 1nm EOT 2D MoS_2 top gated thin film transistors — *Jan 23 - Present*
Collaboration with TSMC Corporate Research

- Achieved a **sub - 1 nm** EOT on top gated MoS_2 FETs through conformal ALD seed layers and gate oxides
- Improved reliability and performance **~10x** of fabricated devices through an original sacrificial layer process
- Implemented a novel deposition method combining ALD+CVD for ultra-thin conformal films on monolayer MoS_2
- Designed an advanced gate stack engineering process to control threshold voltage for logic applications
- Modeled properties such as mobility, interface trap density and energy distribution, and capture cross-section areas through the combination of advanced **DC-IV and Impedance characterization** measurements

Impedance and DC characterization of top gated CNT thin film transistors — *Sep 21 – Aug 22*
Collaboration with **TSMC Corporate Research**

- Designed a setup capable of accurate measurements of ultra-low capacitances (~10-100 fF) in CNTFETs through careful elimination of parasitic capacitances and resistances resulting in a **20x** improvement in SNR
- Modeled device properties such as mobility and trap density and energy distribution through the combination of **DC-IV and Impedance characterization** measurements

Reduced operation voltages in ferroelectric-based RRAM through graphene interface engineering — *Jan 22 – Jun 23*

- Achieved a **sub-1V** operation – benchmark for **in-memory computing** applications.
- Reduced coercive voltage requirements in ferroelectric tunnel junctions by **~40%** through inserting an interfacial single layer graphene
- Fabricated ultra-thin ferroelectric polymer films (~ 3 nm) utilizing Langmuir Blodgett deposition technique

TCAD study of non-linear electric fields in ferroelectric FinFETs based memory devices — *Aug 21 – Jun 22*

- Invented a new FinFET gate stack structure combining dielectric and ferroelectric materials to enhance electric fields in FE
- Designed an improved performance FE-FET based memory device utilizing non-linear field effects to reduce working voltages by **~ 33%.**

Thermal conductivity characterization of thin films through AC electrical methods — *May 22 – Jan 23*
Collaboration with **Applied Materials**

- Engineered a circuit model and in-house PCB for measurement of thermal conductivity using the 3ω method

Reduced H_2 plasma corrosion of sputtered Al using ALD thin films — *May 22 – Jan 23*
Collaboration with **KLA**

- Designed a scheme to utilize ALD Al_2O_3 thin films as an H_2-plasma corrosion protection film for sputtered Al resulting in **~8x** lower surface roughness compared to unprotected samples.

SKILLS & ABILITIES

- *Thin film deposition :* Atomic Layer Deposition, Chemical Vapor Deposition
- *Device Electrical Characterization* : Impedance (Capacitance-Voltage), DC-IV, Pulse-IV, P-V characterization
- *Device modeling :* TCAD (silvaco)
- *Metrology :* AFM, Raman microscopy, XPS, AES, Ellipsometry, SEM, XRR, XRD
- *Nanofabrication :* Physical Vapor Deposition, Langmuir Blodgett deposition, Photolithography
- *Software :* MATLAB, Python, COMSOL

PUBLICATIONS

- **S. Natani** *et al.*, "Threshold voltage control of sub-1nm EOT top gated MoS_2 transistors using ALD gate oxides" (Manuscript in preparation for **Nature Electronics**)
- **S. Natani** *et al.*, "Spatio-chemical characterization and elimination of localized growth aberrations on monolayer MoS_2 for enhanced performance top gated FETs with scaled ALD oxides" (Submitted to ***Applied Surface Science***)
- **S. Natani** *et al.*, "Low voltage graphene interface engineered organic ferroelectric tunnel junction devices." (Submitted to ***ACS Applied Materials and Interfaces***)
- **S. Natani** *et al.***,** "Low voltage polarization switching in ferroelectric FinFET based memory devices using electric field nonlinearities". (Submitted to ***Journal of Computational Electronics***)
- Z. Zhang, M. Passlack, G. Pitner, **S. Natani** *et al.*, "Complementary carbon nanotube metal–oxide–semiconductor field-effect transistors with localized solid-state extension doping". ***Nature Electronics***
- A. W. Lee, Y. Dong, **S. Natani** *et al.*, "Toward the Ultimate Limit of Analyte Detection in Graphene-Based Field-Effect Transistors". ***Nano Letters***
- D. K. Ban, T. Bodily, A. G. Karkisaval, Y. Dong, **S. Natani** *et al.*, Rapid self-test of unprocessed viruses of SARS-CoV-2 and its variants in saliva by portable wireless graphene biosensor. ***Proceedings of the National Academy of Sciences***
- N. Safron, T.A. Chao, S. Li, **S Natani** *et al.*, High performance transistor of aligned carbon nanotubes in a nanosheet structure, **2024 IEEE Symposium on VLSI Technology and Circuits (VLSI Technology and Circuits)**
- P. Khajanji, **S. Natani**, P. Bandaru, "Investigating pressure and solvent effects in Langmuir–Blodgett deposited ferroelectric thin films". **Journal of Materials Research**
- M. Passlack, N. Safron, A. Oberoi, C. Gilardi, J. Zuo, S.K. Su, T.A. Chao, A. Azizi, **S. Natani** *et al.*, "Statistics Based Modeling and Analysis of Ultra-Low Impedance Carbon Nanotube MOS Capacitors" **2024 IEEE International Electron Devices Meeting**
- K. Eshraghi, **S. Natani**, P. R. Bandaru; Modeling electronic conduction in quantum dot constituted assemblies coupled to metallic electrodes. ***Applied Physics Letters***
- G. Mao, L. Wu, Y. Fu, Z. Chen, **S. Natani** *et al.*, "Design and Characterization of a Soft Dielectric Elastomer Peristaltic Pump Driven by Electromechanical Load," ***IEEE/ASME Transactions on Mechatronics***
- P. Bandaru, **S. Natani**, Topological States for New Modes of Information Storage and Transfer. ***Springer Nature***

CONFERENCES

- IEEE Semiconductor Interface Specialists Conference, SISC 2024
  Talk : Identification of defects on monolayer MoS_2 through infrared photo-induced force microscopy
- IEEE International Symposium on Applications of Ferroelectrics 2023
  Talk : Reduction of Voltage for Low Power Ferroelectric Devices, through Graphene-Based Interfacial Engineering
- IEEE Semiconductor Interface Specialists Conference, SISC 2023
  Poster : Conformal, ultrathin top gate oxides for monolayer MoS_2 – **T.P. Ma award for best student poster**
- IEEE Semiconductor Interface Specialists Conference, SISC 2022
  Poster : Using nonlinear electric fields in non-planar geometries for low-voltage operation of Ferroelectric Field Effect Transistor based memory devices
- International Superconductive Electronics Conference, ISEC 2019