

Low-Voltage Graphene Interface-Engineered Organic Ferroelectric Tunnel Junction Devices

Shreyam Natani, Pranjali Khajanji, Li Cheng, Kassra Eshraghi, Zichen Zhang, Wade Shipley, Andrea R. Tao, and Prabhakar R. Bandaru*



Cite This: ACS Appl. Mater. Interfaces 2025, 17, 32773–32781



Read Online

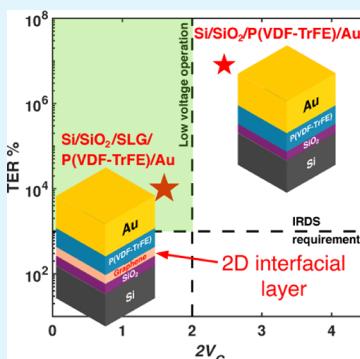
ACCESS |

Metrics & More

Article Recommendations

Supporting Information

ABSTRACT: It has been indicated that the path forward for the widespread usage of ferroelectric (FE) materials may be considerably facilitated through the reduction of programming voltages to on-chip logic-compatible values of <1 V. Obstacles involve issues related to the scaling of the FEs to lower thickness as well as the presence of an interfacial layer (IL) between the high-permittivity FE and the substrate resulting in *wasted* voltage across the IL. Here, we show how lower operating voltages along with a higher tunneling electroresistance (TER) could be achieved through IL engineering. We use piezoresponse force microscopy and fabricated ferroelectric tunnel junctions (FTJs) to show that ultrathin FE films deposited on single-layer graphene/Si can exhibit polarization switching at reduced voltages ~ 0.8 V with significant TER as compared to directly depositing on Si.



KEYWORDS: ferroelectric tunnel junction (FTJ), PVDF-TrFE, low voltage, interface Engineering, memory window, 2D materials

1. INTRODUCTION

FTJs have been mostly constructed using *distinct* metal (*M*) electrodes on either side of the *FE*, i.e., in a $M_1/FE/M_2$ arrangement: Figure 1a – so as to harness the difference in the tunneling currents through the *FE* with respect to polarization direction.^{1–3} The bound charges corresponding to a given *FE* polarization (P_{FE}), are compensated over a screening length (l_{scr}) in the electrodes. The distinction in the respective l_{scr} between the two metals implies directionality dependent barriers to current transmission yielding low(/high) resistance state current/s, termed as I_{LRS} (/ I_{HRS}). The fidelity between the two states is manifested through the magnitude of the tunneling electroresistance: TER (%) = $\frac{I_{LRS} - I_{HRS}}{I_{HRS}}$ × 100.

The *TER* is then typically⁴ proportional to the relative barrier height differences, and would be further enhanced through using a semiconductor (*S*) as one of the electrodes, i.e., in a $M/FE/S$ arrangement: Figure 1b – top, predicated on the possibility of varying the electron density over several orders of magnitude. While Si seems to be an obvious choice for the *S*,⁵ the influence of the related oxides, e.g., SiO_2 on the *Si*, as an IL should be carefully considered. From the continuity of electrical displacement across the *FE-IL* interface, i.e., with $\epsilon_{FE}E_{FE} = \epsilon_{IL}E_{IL}$ and $\epsilon_{FE} > \epsilon_{IL}$, the $E_{FE} < E_{IL}$, implying *wasted* voltage across the IL. The electrical field in the interfacial layer (E_{IL}) is typically considered the “*weakest link*” in *FE* devices,² and has also been implicated in reduced device endurance^{6,7} due to the disparity in charge density—consequent to which charge compensation in the latter occurs through necessary

defect generation, charge trapping, etc. In this context, the consideration of 2D materials is attractive, from the viewpoint of the lack of dangling bonds⁸ which inhibit formation of interfacial compounds and the consequent IL. It was then aimed to alleviate IL-related issues through interfacial engineering by including single layer graphene (SLG) at the interface between the *FE* and the IL in an FTJ.

For the *FE*, traditional materials such as inorganic perovskites, e.g., belonging to the lead or barium titanate families, require epitaxial growth on atypical substrates for ultrathin films⁹ and ultimate scaling. Further, atomic layer deposition (ALD) of $Hf_{1-x}Zr_xO$ (HZO) is nontrivial due to requiring seeding interlayers for deposition.^{10,11} Consequently, P(VDF-TrFE) was selected as the *FE* layer, for this study. A particular advantage of organic ferroelectrics is the possibility of ultimate scaling to atomic dimensions, e.g., through the use of a *FE* such as P(VDF-TrFE): poly(vinylidene difluoride – trifluoroethylene) copolymer, where the ferroelectricity originates at the single atom level, i.e., from the dipole moment between an electro-negative (/positive) F– (/H+) ion.¹² Such atomic layers may be integrated into FTJs—where high(/low)

Received: January 23, 2025

Revised: May 12, 2025

Accepted: May 13, 2025

Published: May 26, 2025



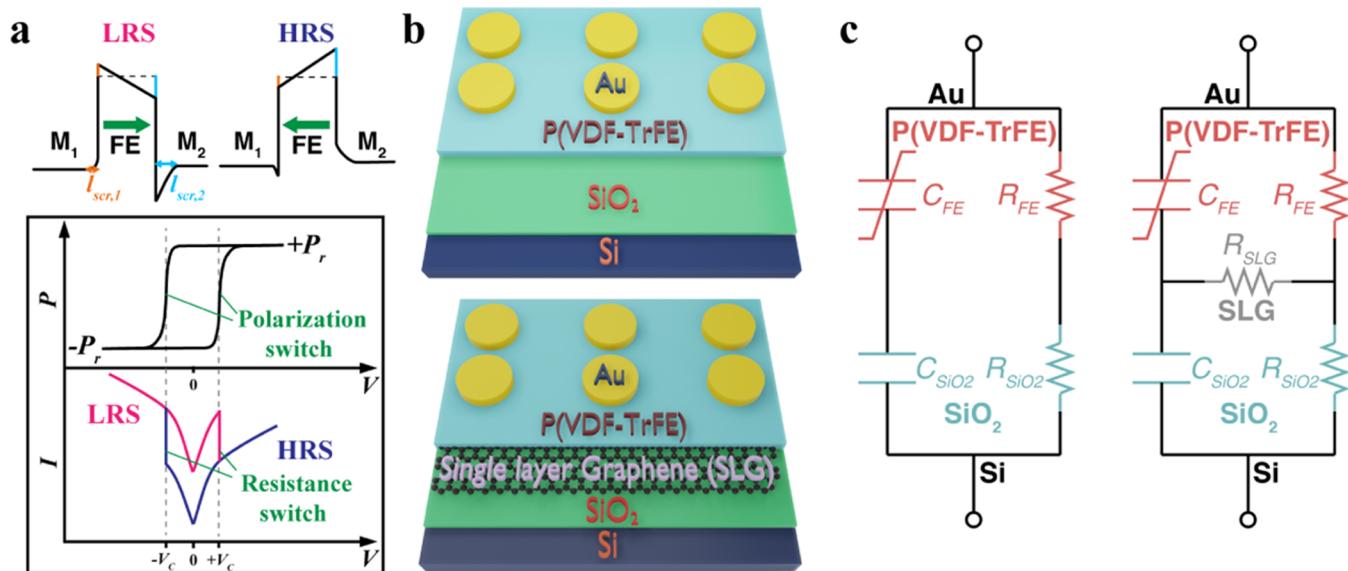


Figure 1. Working principles and device schematic of 2D material-based ferroelectric (FE) tunnel junctions (FTJs). (a) The electrical tunneling current in an FTJ (top) may be modulated to be in a low (/high) resistance state, i.e., LRS (/HRS), depending on the direction of the FE polarization. The differing screening length (l_{scr}) values for the two electrodes, say (1) and (2) are indicated with the assumption that $l_{scr,2} > l_{scr,1}$. The consequently expected polarization (P)–voltage (V) and the current (I , in log scale)– V are indicated (bottom figure). (b) Device structure schematic of the fabricated FTJ on bare Si (top) and interface engineered graphene/Si surface (bottom). (c) Schematic circuit mode for the M/FE/ SiO_2 /Si configuration, (left) where the electric fields in the FE and SiO_2 are determined by their respective capacitance ratio, and for the M/FE/SLG/ SiO_2 /Si configuration (right), where the use of a 2D semiconductor (2D-S), such as single layer graphene acts as a resistor connecting the capacitive and resistive branches of the FE and SiO_2 —here, the electric fields in the FE and SiO_2 are determined by their impedance ratio.

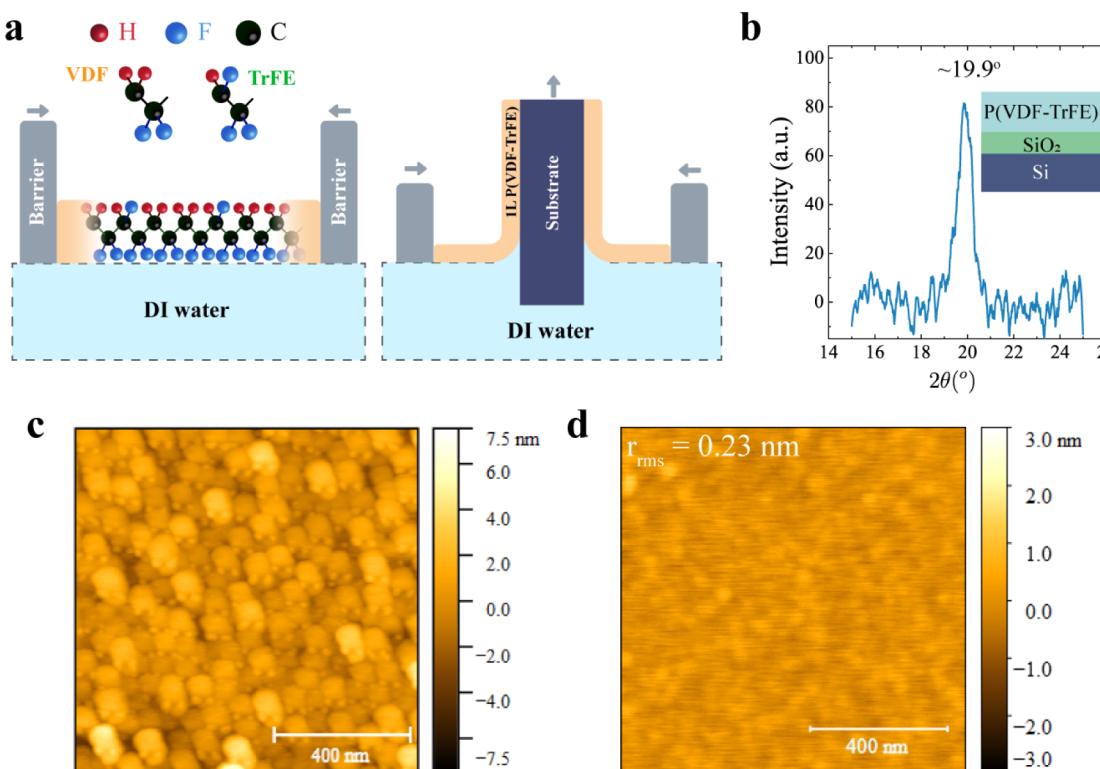


Figure 2. Synthesis and structural characterization of ferroelectric (FE) P(VDF-TrFE) films deposited through the Langmuir–Blodgett (L-B) technique. (a) Sequence of steps related to the L-B deposition of the P(VDF-TrFE) films. (b) X-ray diffraction (XRD) on a thick film (~20 nm) of P(VDF-TrFE) showing a peak at $2\theta = 19.9^\circ$ corresponding to the FE β -phase in the polymer. (c) AFM topography image of thick film showing elliptical nanorods, characteristic of the ferroelectric β -phase. (d) AFM topography image of ultrathin LB film on silicon substrate.

tunneling current through the FE in the junction is utilized to represent high(/low) states, through nondestructive resistive readout. Approaches to date have deployed thin FE P(VDF-

TrFE): placed either between metallic electrodes such as Al, Au, Pt, ITO (indium tin oxide), LSMO (Lanthanum strontium manganese oxide) — yielding reduced TER, or using non

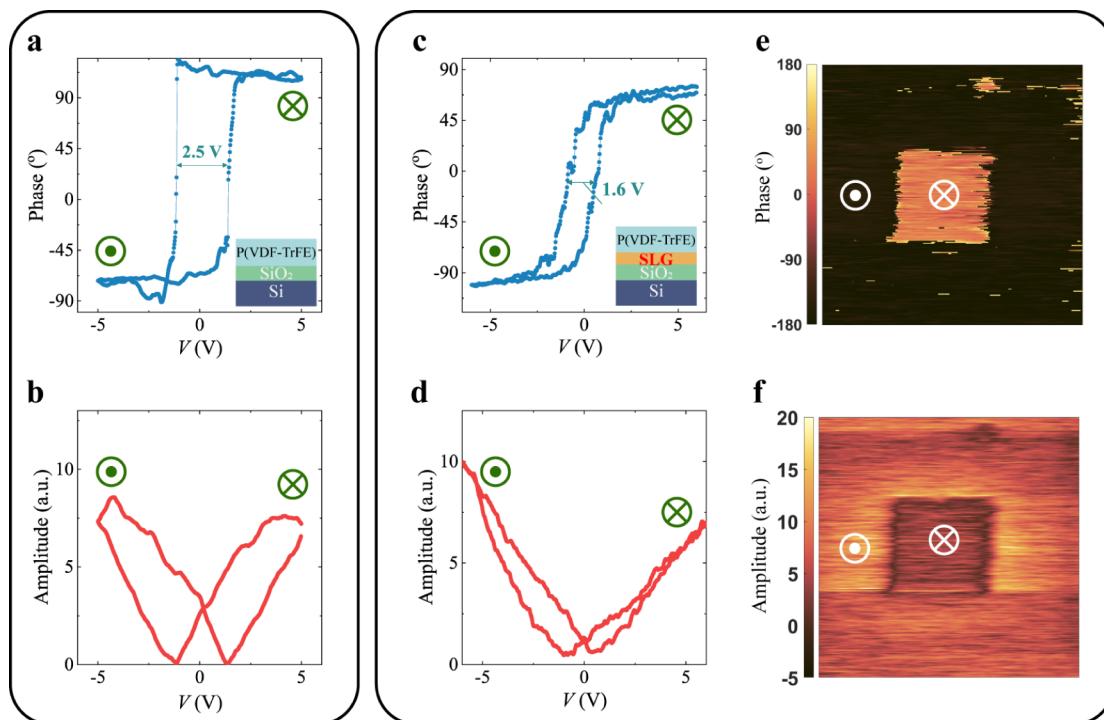


Figure 3. Polarization switching voltage response in P(VDF-TrFE) films deposited on silicon and SLG/silicon substrates, as inferred through piezoresponse force microscopy (PFM). The observed (a) phase and (b) amplitude as a function of voltage on a 1L P(VDF-TrFE) film deposited on a Si substrate. The polarization switching takes place at -1.1 V and $+1.4$ V resulting in a $2V_C \sim 2.5$ V. The observed (c) phase and (d) amplitude as a function of voltage on a 1L P(VDF-TrFE) film deposited on a SLG/Si substrate. The polarization switching occurs at lower voltages, i.e., -0.9 V and $+0.7$ V, resulting in a reduced $2V_C \sim 1.6$ V. The corresponding PFM (e) phase, and (f) amplitude imaging on a 1L-P(VDF-TrFE) film after switching the polarization negative in a $6\text{ }\mu\text{m} \times 6\text{ }\mu\text{m}$ area and switching the polarization positive in the central $2\text{ }\mu\text{m} \times 2\text{ }\mu\text{m}$ area. The \bullet and \otimes symbols indicate up (\uparrow) and down (\downarrow) polarization states, respectively. In (e), the bright (/dark) phase signal is indicative of down (/up) polarization, induced by the AFM tip. In (f), the outside and inside squares have higher amplitude compared to the boundary where the FE switching occurs.

silicon-based semiconductors such as Nb-STO (strontium titanate). However, as indicated earlier, if an ideal FTJ could be posited to be of the *M/FE/2D-S* type, we show here proof of principle toward the necessity of such a device through an intermediate *M/FE/2D-S/Si* structure: Figure 1b - bottom, with the *net* absence of an IL—consequent to which low voltage operation is feasible. This was done, through experimental evaluation of a configuration involving the *FE* placed on graphene/Si substrate electrode. Importantly, sub- -1 V operation was obtained.

Fundamental to such implementation is the consideration of the circuit diagram of the *M/FE/SiO₂/Si* in comparison with the *M/FE/SLG/SiO₂/Si*: Figure 1c. The inclusion of the SLG layer serves to provide an approximate equipotential plane. In the *M/FE/SiO₂/Si* case, the voltage distribution in the *FE* and SiO₂ is dependent on the ratio of the respective capacitances. A large fraction of the applied voltage (V_{app}) is dropped across the lower permittivity SiO₂. The purpose of including the SLG film in between the *FE* and SiO₂ is to induce an equipotential plane—see Figure 1c. Now, the impedance of each film (including the capacitive and resistive components) determines the fraction of V_{app} dropped across the *FE* and SiO₂, respectively.¹³ Thin P(VDF-TrFE) is more resistive than SiO₂ at small thickness.¹⁴ Hence, with the inclusion of the SLG, the impedances of each film are influenced such that a larger fraction of V_{app} is dropped across the *FE* resulting in lower V_C . Such characteristic aspect has been previously considered in other Metal-FE-Metal-Interlayer-Semiconductor(/Metal):

MFMIS(/M)) based configurations, with respect to Metal-FE-Interlayer-Semiconductor(/Metal): *MFIS(/M)*) arrangements.^{15,16}

2. RESULTS AND DISCUSSION

We will next discuss aspects related to the structural and electrical characterization of device configurations, incorporating 2-D material based interface engineering.

2.1. Structural Analysis and Verification of Ferroelectric (FE) Characteristics. With the aim of obtaining lower V_C , a SLG layer¹⁷ — see Section S1, was first transferred onto a Si substrate. An ultrathin (~ 3.2 nm) P(VDF-TrFE) FE film¹⁸ was then deposited onto both Si as well as SLG/Si substrates through the Langmuir–Blodgett (LB) technique, as schematically indicated in Figure 2a — also see Section S2. Deposited L-B P(VDF-TrFE 70:30) copolymer films/substrate were annealed at 135 °C for 30 min in air¹⁹ to yield the β -phase *FE* form²⁰ — inferred through X-ray diffraction on thicker samples: Figure 2b. The subsequent probing of the surface morphology of the P(VDF-TrFE) film through atomic force microscopy (AFM) indicated elliptical nanorods, characteristic²¹ of such a *FE* phase:²² Figure 2c. Further a surface morphology of the ultrathin P(VDF-TrFE) was probed (Figure 2d) which showed a smooth film with rms roughness ~ 0.23 nm. The presence of underlying SLG was found beneficial for smooth monolayer *FE* films, presumably due to reduced interfacial interactions²³ as can be seen in Figure S1c.

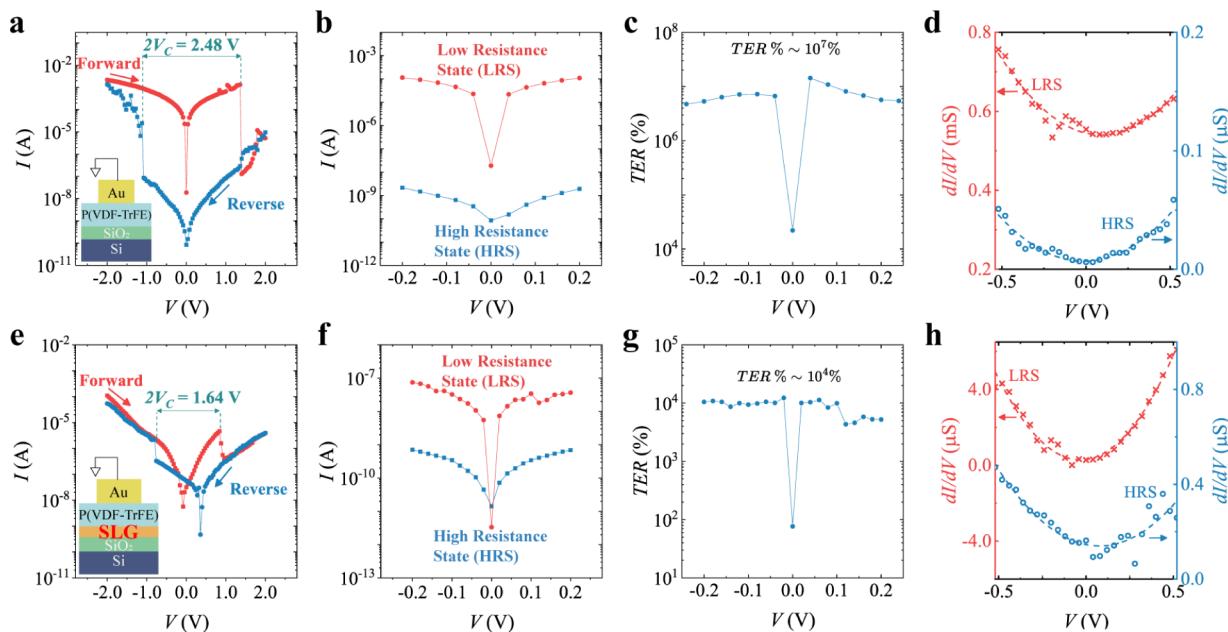


Figure 4. Resistive switching related to polarization modulation in P(VDF-TrFE) tunnel junctions. *Au/FE/SiO₂/Si* devices—top. (a) A change from (/to) a high (/low) current state was observed in the forward (/backward) scans, at similar voltages as observed in PFM, cf., Figure 3(a)—indicating correlation between FE polarization and resistive switching phenomena. The corresponding (b) tunneling current (I) as a function of voltage (V), and the (c) derived TER %. (d) The derived conductance (dI/dV)—voltage (V) characteristics. *Au/FE/SLG/SiO₂/Si* devices—bottom. (e) Modulation from (/to) a high (/low) current state in the forward (/backward) scans. The (f) tunneling current (I) as a function of voltage (V), (g) derived TER %, and (h) conductance characteristics.

PFM spectroscopy was used to indicate close to ideal 180° phase contrast characteristic:²⁴ Figure 3a, as well as minima in the amplitude signal of the “butterfly” attribute: Figure 3b, at a tip voltage of +1.4 V and -1.1 V—which serve as markers of the coercive voltage:²⁵ V_c of the order of 1.25 V (~0.5 |1.4 + 1.1|). Alternately, for the LB FE films deposited on the SLG/Si substrates, the *phase* and the *amplitude* plots, i.e., Figure 3c,d, respectively, also indicate a phase reversal of ~180° and switching at tip voltages of +0.7 V (-0.9 V) in the PFM amplitude scans.

Hence, a V_c of the order of 0.8 V (~0.5 |0.7 + 0.9|) was obtained. Such diminished V_c —to less than 1 V, is significant and marks the considerable reduction of the influence of the underlying *IL* layer. It is to be noted that although the PFM phase loop for the FE/SLG/SiO₂/Si sample does not look as saturated (Figure 3c) as that of the FE/SiO₂/Si sample (Figure 3a), such an aspect is due to measurement resolution rather than the specific influence of the interfacial graphene. Given the local nature of probing the PFM measurement over ~10 nm, insufficient averaging over larger FE grain size could result in such observations.²¹

To illustrate the ferroelectric switching, domains were embossed on the FE film using a conductive AFM tip, the related phase and amplitude plots of which are shown in Figure 3e,f respectively—for SLG/Si substrates. Here, a grounded AFM tip was scanned on a 6 μm × 6 μm area with the substrate voltage (V_{sub}) at +5 V, for defining a up (↑) polarization state in the FE film. Similarly, a smaller 2 μm × 2 μm area was switched to a down (↓) polarization state by scanning the grounded AFM tip with V_{sub} at -5 V. The final polarization state was read by scanning over a 6 μm × 6 μm area with V_{sub} = 0 V. In Figure 3e, the bright (/dark) phase signal is indicative of down (/up) polarization,²¹ induced by the AFM tip. Similarly, in Figure 3f, the outside and inside

square have comparatively high amplitude compared to the boundary where the *FE* switching occurs.

We note that there has been discussion on the validity of PFM measurements, in terms of the influence of the mechanical strain manifested through the observed electrical signals,⁴ and the possibility that *FE*-like hysteresis may be obtained in non-*FE* systems. However, it was indicated²⁵ that the existence of an explicit V_c in the DC scans *alone* could be regarded as strong evidence for intrinsic ferroelectricity and such an aspect was thoroughly verified: see Section S3.

2.2. Ferroelectric Tunnel Junction (FTJ) Devices on Si and Graphene/Si Substrates. Based on the attractive attribute of a lower operational voltage that may be achieved through the *FE/SLG* layer paradigm, the next step was to demonstrate the underlying principles in a device configuration. Au electrodes were patterned using shadow masks and subsequent electron-beam evaporation onto the *FE* film, for this purpose. Related current (I) - voltage (V) measurements, and the derived *TER*, with respect to varying (/ground) voltage on the bottom Si (/top Au) electrodes, are shown in Figure 4—for both the *M/FE/SiO₂/Si* and *M/FE/SLG/SiO₂/Si* configurations. A sudden modulation of the electrical current switching off (/on) at a voltage of ~1.4 V (-1.1 V) during the forward (/reverse) sweep was observed in the *M/FE/SiO₂/Si* case: Figure 4a. The modulation is over 5 orders of magnitude, pointing to the significant influence of the *FE* polarization. For accurate measurements of *TER*, the devices were first set(/reset) to +2 V (-2 V) and then resistance measured in a narrow voltage range (-0.2 to 0.2 V) – Figure 4b. The corresponding variation of the *TER* in Figure 4c was measured to be ~10⁷%, matching previously reported highest values.²⁴ The high *TER* may be ascribed to the influence¹ of both the (i) barrier modulation, as well as (ii) corresponding

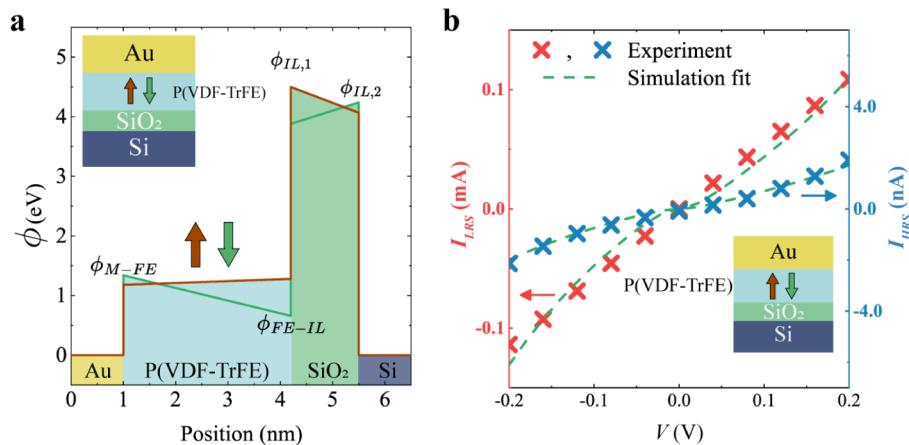


Figure 5. Modeling tunneling current through trapezoidal tunneling barriers, for up (↑) and down (↓) polarization states, through a transfer matrix algorithm (TMA) approach. (a) Using ϕ_{Au-FE} for ↑ (↓) configuration as 1.2 eV (/1.3 eV) and ϕ_{FE-IL} for ↑ (↓) configuration as 1.3 eV (/0.7 eV) related to the high (/low)-resistance states: HRS (/LRS), respectively, yielded (b) an excellent fit to the observed $I-V_b$ characteristics.

change of the Si from an accumulation mode to a depletion mode – affecting carrier states available for tunneling.

Similarly, in the *M/FE/SLG/SiO₂/Si* case, the switching off (/on) events occurred at a voltage of ~0.84 V (/−0.8 V) during the forward (/reverse) sweep: Figure 4e, with an observed decrease (/increase) of the electrical current. An alternative device is shown in Section S4. Additionally, quantitative analysis for the voltage reduction in devices with and without the SLG is further detailed in Section S5.

The obtained switching voltage values, (−1.1 and 1.4 V i.e., $2V_C = 2.5$ V) for *M/FE/SiO₂/Si* case and (−0.80 and 0.84 V i.e., $2V_C = 1.64$ V) for the *M/FE/SLG/SiO₂/Si* case, are well matched to those obtained in the PFM scan: Figure 3 and clearly confirm that the resistance switching is a consequence of the *FE* character²⁶ of the film. The negative (/positive) shifts along the voltage axis in the forward(/backward) scans are likely due to the presence of interface/border traps, i.e., that may have originated from polymer residues used in the graphene transfer process, etc. Similar set/reset measurements as in the *M/FE/SiO₂/Si* samples were carried out: Figure 4f and the TER % was observed to be ~10⁴: Figure 4g – significantly higher than any previously reported device with a $V_c < 1$ V. Corresponding resistance vs voltage hysteresis loops and retention characteristics can be found in Section S6.

While it is remarkable that the inclusion of SLG successfully reduces the operating voltages in our devices by ~40%, there is also indicated a substantial reduction of TER % from 10⁷ to 10⁴. Given that the TER is related to the contrast of l_{scr} between the two electrodes flanking the *FE* film – see Figure 1a, the semimetallic character of SLG, i.e., with $l_{scr,Au} < l_{scr,SLG} < l_{scr,Si}$ implies reduced contrast and leads to the smaller TER.

The transport at low voltages in FTJs is based on direct tunneling with trapezoidal barriers which manifest parabolic conductance-voltage characteristics.²⁷ The related experimental measurements for the *M/FE/SiO₂/Si* and *M/FE/SLG/SiO₂/Si* configurations, i.e., Figure 4d,h, respectively – as derived from Figure 4a,e, indicate such attributes. The presence of tunneling transport, combined with the modulation of the tunneling currents at voltages similar to the polarization switching voltages seen in PFM measurements (Figure 2a,c) provides further evidence for the resistive switching arising from polarization switching in the ferroelectric.

2.3. Remnant Polarization Calculation Using Tunneling Current Simulation. We analyzed the experimental $I-V$ characteristics, considering tunneling barriers and related electrical potential profiles: Figure 5a for the down (↓) and up (↑) polarization states—through a transfer matrix algorithm (TMA) based approach^{28,29} – for estimating the *FE* polarization. Here, the (i) *Au/FE* barrier (of height ϕ_{Au-FE}), (ii) *FE/SiO₂ IL* interface barrier (of height ϕ_{FE-IL}) along with the (iii) *SiO₂ IL/Si* interface barrier (of height $\phi_{IL,1}$ and $\phi_{IL,2}$)³⁰ of ~4.5 eV, are relevant fitting parameters. The interplay among the described potential barriers is modeled as a superposition of contributions from distinct sources. These include the potential arising from spatial variations in the conduction band minimum across the FTJ, the electrostatic potential generated by the spontaneous polarization of the *FE* layer, the polarization induced within the nonpolar dielectric layer (*IL*) due to the *FE*, and the screening charges present in the electrodes.^{31,32}

Here, ϵ_{FE} (=6),³³ t_{FE} (= 3.2 nm); ϵ_{SiO_2} (= 3.9),³⁴ t_{SiO_2} (= 1.3 nm) indicate the respective dielectric permittivity and thickness of the *FE* and *IL*. Under a voltage bias (say, V_b), the TMA yields an energy (E) dependent transmission probability: $T(E, V_b)$, which was used for estimating³⁴ the related tunneling current: $I(V_b)$, through the relation:

$$I(V_b) = A \frac{e}{2\pi\hbar} \int_0^\infty T(E, V_b) [f(E) - f(E')] dE \quad (1)$$

Here, A is the top electrode area, e is the elementary unit of electron charge, \hbar the reduced Planck's constant, $E' = E + eV_b$, and $f(E)$ is the relevant supply function of the top and bottom electrode/s—a measure of the flux of electrons through the barrier, proportional to the *k*-vector dependent carrier velocity (v), the energy dependent density of states: $DOS(E)$, and the state occupation probability (through the Fermi–Dirac distribution function: f_{F-D}), defined by

$$\begin{aligned} f(k) &= \int_0^\infty v \cdot DOS(k) f_{F-D}(E) dk \\ &= \frac{1}{\hbar} \int_0^\infty DOS(E) f_{F-D}(E) dE \\ &\equiv f(E) \end{aligned} \quad (2)$$

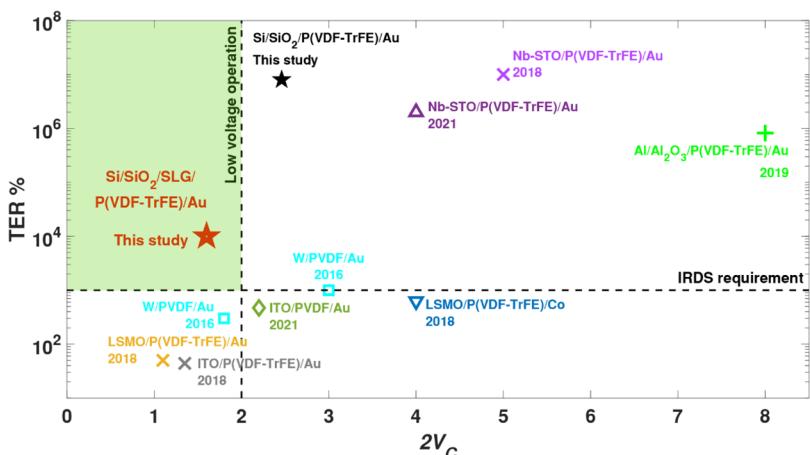


Figure 6. Benchmark of PVDF based ferroelectric tunnel junction device performance, comparing TER% as a function of coercive voltages (V_c) in the literature. The green highlighted region represents the ideal range of device performance, where the lowest acceptable TER% is dictated by IRDS requirements and the highest acceptable coercive voltage is dictated by compatibility requirements with logic for logic-in-memory applications.^{12,24,44–46}

The FE polarization induces in the Si either accumulation or depletion of carriers, varying the $(DOS)_{Si}$ and hence modulating the supply function by $\sim 2 \times 10^4$, as further discussed in **Section S7**. Through experimental knowledge of the left-hand side of **eq 1**, the fits to ϕ_{Au-FE} and ϕ_{FE-IL} along with the $\phi_{IL,1}$ and $\phi_{IL,2}$ were determined, and have been indicated in conduction band (CB) related potential profiles, for both polarization directions in the FE (P(VDF-TrFE)) on Si in **Figure 5a** along with the related modeled $I-V$ characteristics in **Figure 5b**.

The related barrier height modulation, i.e., $|\phi_{M-FE,\uparrow} - \phi_{M-FE,\downarrow}|$ related to the *upper* Au electrode, arising from polarization switching, is ~ 0.1 eV, and on the *bottom* Si electrode is ~ 0.6 eV. The effect of the larger $l_{scr,Si}$ is implicit in the higher modulation of the FE barrier on the Si side. Assuming a screening length of ~ 0.07 nm for Au³⁵ and ~ 0.41 nm for Si³⁶ and combining them with the barrier modulations,³⁷ we estimate a polarization of $6.0\text{--}8.0 \mu\text{C}/\text{cm}^2$ for the P(VDF-TrFE) films, which seems a typical value.³⁸ More details on the calculation can be found in **Section S8**.

2.4. Benchmarking Results. The obtained results, from our work are superior with respect to two crucial key performance indicators, i.e., the TER and the coercive voltage ($2V_c$), in comparison to reports from literature³⁹ – as indicated in **Figure 6**. We have obtained a TER (%) of $\sim 10^4$ along with a V_c of ~ 0.8 V for the Au/FE/SLG/SiO₂/Si devices. As indicated in the introductory sections, an operating voltage of less than 1 V would be crucial in breaking down a barrier for encouraging the adoption of FE technology and this has been achieved in our work. Further, a TER% of at least 10^3 was recommended in the *International Roadmap for Devices and Systems* (IRDS),⁴⁰ and has been demonstrated here.

3. CONCLUSIONS

In summary, we have fabricated high quality ferroelectric tunnel junctions based on ultrathin organic ferroelectric P(VDF-TrFE). Through the inclusion of single layer graphene at the P(VDF-TrFE)/SiO₂ interface, we have successfully bypassed the voltage dropped across the interface layer and hence reduced our operating voltages. The fabricated Au/P(VDF-TrFE)/SLG/SiO₂/Si ferroelectric tunnel junctions demonstrate the lowest operating voltages along with a high

TER% (with reference to IRDS requirements) compared to any other device fabricated using similar ferroelectric materials. Moreover, our work presents a practical and generic approach to integrate 2D materials with ultrathin ferroelectric oxide films (i.e., HZO) for future low voltage operational, CMOS friendly memory devices.

Further, our results constitute the first reported instance of P(VDF-TrFE) based FTJs fabricated on Si based systems through the synergistic incorporation of 2D materials. Our work, based on low temperature synthesis and processing coupled with the lower operating voltage/s, provides further impetus for the integration of FE materials and systems into back-end-of-line (BEOL) implementations. Given recent imperative for the incorporation of 2D materials⁴¹ in FE devices,⁴² our work would further motivate the development of large scale assembly of L-B films.¹⁸

4. EXPERIMENTAL SECTION

4.1. P(VDF-TrFE) Film Deposition. The P(VDF-TrFE) copolymer (from PolyK Technologies), constituted of 70% vinylidene fluoride (VDF) and 30% trifluoroethylene, was dissolved in cyclopentanone with a concentration of 0.1 wt %. The solution was dispersed on the surface of deionized water in a KSV Nima Langmuir trough with an associated dipper mechanism. The surface pressure was continuously monitored, and the surface was compressed to ~ 5.3 mN/m, as measured using a Wilhelmy plate.⁴³ Subsequently, the Silicon and single layer graphene (SLG) coated Silicon substrates – see next section, were raised through the surface polymer film, depositing a single layer of the P(VDF-TrFE), following which the substrate was allowed to dry. The associated deposition technique – termed the Langmuir–Blodgett (L-B) methodology, could be repeated multiple times to yield thicker films.

4.2. Single-Layer Graphene (SLG) Growth and Transfer. Single layer graphene (SLG) was synthesized using chemical vapor deposition (CVD) in a quartz tube reactor on $25 \mu\text{m}$ thick copper foils (MTI Corp) over 2 h, using a mixture of methane (2 sccm) and hydrogen (15 sccm) gas as the precursors for the deposition. To transfer the graphene onto Si substrates, the graphene covered Cu foil was coated with a 3 wt % P(VDF-TrFE) film using spin-coating. Next, Oxygen plasma reactive ion etching (Trion RIE), was used to remove the excess graphene on the other side of the foil. The foil was then floated in an ammonium persulfate (0.1 M) solution to etch off the Cu and subsequently rinsed with DI water. The graphene/polymer composite was then transferred onto the substrate. The P(VDF-

TrFE) was dissolved using acetone for 4 h followed by IPA rinse and N₂ blow dry after which the Langmuir–Blodgett deposition was carried out to deposit the ultrathin ferroelectric film.

4.3. Ferroelectric Tunnel Junction Fabrication. FTJs were fabricated by depositing gold electrodes (~50 nm) patterned via a shadow mask on ultrathin P(VDF-TrFE). Soft evaporation parameters (vacuum ~5 × 10⁻⁷ Torr, deposition time <10 min, distance between gold source and sample ~50 cm) were used to minimize damage to the film.

4.4. Atomic Force Microscopy (AFM) and Piezoresponse Force Microscopy (PFM). AFM and PFM were performed at room temperature in a Park NX 20 AFM system. Topography AFM images were taken using the noncontact mode using commercial silicon tips (MikroMasch NSC15). PFM measurements were performed using silicon tips coated with Cr/Pt (Budget Sensors ElectriMulti75-G). Here, an AC voltage of ~1 V (at ~12 kHz frequency) superimposed on a slower varying (of period ~1 s) triangular sweep voltage (DC) in a range of ±1 V to ±5 V, was applied to the tip scanning the device/s and the resulting measured current, with respect to the phase and amplitude, was monitored as a function of voltage bias.

4.5. Film Thickness. Film thickness was measured using (i)AFM, (ii) nanoindentation, and (iii) ellipsometry. Film thickness was measured across a fabricated step edge by AFM. On the average, the thickness of one P(VDF-TrFE) monolayer was determined to be ~3.2 nm. Alternately, iMicro (from KLA Inc.) equipped with a Berkovich tip (Type TB30524) was used for nanoindentation based measurement of the film thickness, comparing a bare silicon sample and one coated with 1L-P(VDF-TrFE) to give a thickness ~2.9 nm. Further, ellipsometry (J.A. Woollam M-2000D) was also used to fit the film thickness, in the Cauchy mode, to verify that one monolayer of the FE film yielded a thickness of ~3.3 nm and the thickness of the SiO₂ layer to be 1.3 nm. An average thickness of 3.2 nm was assumed for the 1L-P(VDF-TrFE) film.

4.6. Electrical Characterization. Electrical measurements were made in a shielded probe station using an Agilent B1500A semiconductor device parameter analyzer. The top Au electrodes were grounded, and bias voltage was applied to the substrate. The voltage was swept from positive to negative bias and back at a sweep rate of ~120 mV/s in steps of 40 mV. For TER measurements, the device was biased at a large positive(/negative) voltage = +2 V (-2 V) to switch the ferroelectric film into a given polarization state. Then, a small sweep of voltage from -0.2 to 0.2 V in steps of 20 mV was applied and current measured. It was ensured that trapping charges did not shift the *I*–*V* curve minima away from 0 V, through such measurement protocols.

ASSOCIATED CONTENT

Data Availability Statement

The data that support the plots within this paper and other findings of this study are available from the corresponding author upon reasonable request.

Supporting Information

The Supporting Information is available free of charge at <https://pubs.acs.org/doi/10.1021/acsami.Sc01721>.

Single-layer graphene characterization, film thickness measurements, PFM measurement validity, electrical properties for an extra ferroelectric tunnel junction, quantitative analysis of voltage reduction, resistance–voltage hysteresis curves and retention characteristics, electrode supply function, and polarization calculations (PDF)

AUTHOR INFORMATION

Corresponding Author

Prabhakar R. Bandaru — Department of Mechanical Engineering and Program in Materials Science, University of

California, San Diego, La Jolla, California 92093, United States;  orcid.org/0000-0003-4497-9620; Email: pbandaru@ucsd.edu

Authors

Shreyam Natani — Department of Mechanical Engineering, University of California, San Diego, La Jolla, California 92093, United States;  orcid.org/0000-0003-3633-3408

Pranjali Khajanji — Program in Materials Science, University of California, San Diego, La Jolla, California 92093, United States;  orcid.org/0009-0009-0388-9646

Li Cheng — Department of Mechanical Engineering, University of California, San Diego, La Jolla, California 92093, United States;  orcid.org/0000-0003-0818-6236

Kassra Eshraghi — Program in Materials Science, University of California, San Diego, La Jolla, California 92093, United States

Zichen Zhang — Program in Materials Science, University of California, San Diego, La Jolla, California 92093, United States;  orcid.org/0000-0001-8028-3271

Wade Shipley — Program in Materials Science, University of California, San Diego, La Jolla, California 92093, United States

Andrea R. Tao — Program in Materials Science, University of California, San Diego, La Jolla, California 92093, United States;  orcid.org/0000-0003-1857-8743

Complete contact information is available at:

<https://pubs.acs.org/10.1021/acsami.Sc01721>

Author Contributions

S.N. and P.R.B. conceived the ideas and experiments, which were mainly performed by S.N. L.C. contributed to the growth of single-layer graphene. S.N., P.K. and W.S. contributed to the L-B film deposition. K.E. and S.N. contributed to the simulation study. All the authors contributed to the analysis and interpretation of the results and the writing of the manuscript.

Notes

The authors declare no competing financial interest.

ACKNOWLEDGMENTS

The authors are thankful for support from the Army Research Office (W911NF-21-1-0041-(74813-MS)). This work was performed in part at the San Diego Nanotechnology Infrastructure (SDNI) of UCSD, a member of the National Nanotechnology Coordinated Infrastructure, which is supported by the National Science Foundation (Grant ECCS-2025752).

REFERENCES

- (1) Gruverman, A.; Wu, D.; Lu, H.; Wang, Y.; Jang, H. W.; Folkman, C. M.; Zhuravlev, M. Y.; Felker, D.; Rzchowski, M.; Eom, C.-B.; Tsymbal, E. Y. Tunneling Electroresistance Effect in Ferroelectric Tunnel Junctions at the Nanoscale. *Nano Lett.* **2009**, *9*, 3539.
- (2) Khan, A. I.; Keshavarzi, A.; Datta, S. The Future of Ferroelectric Field-Effect Transistor Technology. *Nat. Electron.* **2020**, *3*, 588.
- (3) Kittel, C. *Introduction to Solid State Physics*, 7th ed.; John Wiley & Sons, Inc.: New York, NY, 2003.
- (4) Wen, Z.; Wu, D. Ferroelectric Tunnel Junctions: Modulations on the Potential Barrier. *Adv. Mater.* **2020**, *32*, 1904123.
- (5) Taur, Y.; Ning, T. H. *Fundamentals of Modern VLSI Devices*, 3rd ed.; Cambridge University Press: Cambridge, UK, 2022.

- (6) Gong, N.; Ma, T. P. A Study of Endurance Issues in HfO₂-Based Ferroelectric Field Effect Transistors: Charge Trapping and Trap Generation. *IEEE Electron Device Lett.* **2018**, *39*, 15.
- (7) Toprasertpong, K.; Takenaka, M.; Takagi, S. On the strong coupling of polarization and charge trapping in HfO₂/Si-based ferroelectric field-effect transistors: Overview of device operation and reliability. *Appl. Phys. A* **2022**, *128*, 1114.
- (8) Illarionov, Y.; Knobloch, T.; Jech, M.; Lanza, M.; Akinwande, D.; Vexler, M. I.; Mueller, T.; Lemme, M. C.; Fiori, G.; Schwierz, F.; Grasser, T. Insulators for 2D Nanoelectronics: The Gap to Bridge. *Nat. Commun.* **2020**, *11*, 3385.
- (9) Garcia, V.; Fusil, S.; Bouzehouane, K.; Enouz-Vedrenne, S.; Mathur, N. D.; Barthélémy, A.; Bibes, M. Giant Tunnel Electroresistance for Non-Destructive Readout of Ferroelectric States. *Nature* **2009**, *460* (7251), 81–84.
- (10) Zhang, Z.; Passlack, M.; Pitner, G.; Kuo, C.-H.; Ueda, S. T.; Huang, J.; Kashyap, H.; Wang, V.; Spiegelman, J.; Lam, K.-T.; Liang, Y.-C.; Liew, S. L.; Hsu, C.-F.; Kummel, A. C.; Bandaru, P. Sub-Nanometer Interfacial Oxides on Highly Oriented Pyrolytic Graphite and Carbon Nanotubes Enabled by Lateral Oxide Growth. *ACS Appl. Mater. Interfaces* **2022**, *14* (9), 11873–11882.
- (11) Zhang, Z.; Passlack, M.; Pitner, G.; Natani, S.; Su, S. K.; Chao, T. A.; Liew, S. L.; Hou, V. D. H.; Hsu, C. F.; Shipley, W. E.; Safron, N.; Doornbos, G.; Lee, T. E.; Radu, I.; Kummel, A. C.; Bandaru, P.; Wong, H. S. P. Complementary Carbon Nanotube Metal–Oxide–Semiconductor Field-Effect Transistors with Localized Solid-State Extension Doping. *Nat. Electron.* **2023**, *6* (12), 999–1008.
- (12) Tian, B. B.; Wang, J. L.; Fusil, S.; Liu, Y.; Zhao, X. L.; Sun, S.; Shen, H.; Lin, T.; Sun, J. L.; Duan, C. G.; Bibes, M.; Barthelemy, A.; Dkhil, B.; Garcia, V.; Meng, X. J.; Chu, J. H. Tunnel Electroresistance through Organic Ferroelectrics. *Nat. Commun.* **2016**, *7*, 11502.
- (13) Khan, A. I.; Radhakrishna, U.; Chatterjee, K.; Salahuddin, S.; Antoniadis, D. A. Negative Capacitance Behavior in a Leaky Ferroelectric. *IEEE Trans. Electron Devices* **2016**, *63* (11), 4416–4422.
- (14) Robertson, J. High Dielectric Constant Oxides. *Eur. Phys. J. Appl. Phys.* **2004**, *28* (3), 265–291.
- (15) Park, H. W.; Byun, S.; Kim, K. D.; Ryoo, S. K.; Lee, I. S.; Lee, Y. B.; Lee, S. H.; Nam, H. W.; Lee, J. H.; Song, J. H.; Shin, S. J.; Hwang, C. S. Exploring the Physical Origin of the Negative Capacitance Effect in a Metal–Ferroelectric–Metal–Dielectric Structure. *Adv. Funct. Mater.* **2023**, *33* (51), 2304754.
- (16) Gastaldi, C.; Cavalieri, M.; Saeidi, A.; O'Connor, E.; Bellando, F.; Stolichnov, I.; Ionescu, A. M. Negative Capacitance in HfO₂Gate Stack Structures with and Without Metal Interlayer. *IEEE Trans. Electron Devices* **2022**, *69* (5), 2680–2685.
- (17) Ferrari, A. C.; Basko, D. M. Raman Spectroscopy as a Versatile Tool for Studying the Properties of Graphene. *Nat. Nanotechnol.* **2013**, *8* (4), 235–246.
- (18) Ducharme, S.; Reece, T. J.; Othon, C. M.; Rannow, R. K. Ferroelectric Polymer Langmuir–Blodgett Films for Nonvolatile Memory Applications. *IEEE Trans. Device Mater. Reliab.* **2005**, *5*, 720.
- (19) Zhao, C.; Hong, Y.; Chu, X.; Dong, Y.; Hu, Z.; Sun, X.; Yan, S. Enhanced Ferroelectric Properties of P(VDF-TrFE) Thin Film on Singlayer Graphene Simply Adjusted by Crystallization Condition. *Mater. Today Energy* **2021**, *20*, 100678.
- (20) Yin, Z.; Tian, B.; Zhu, Q.; Duan, C. Characterization and Application of PVDF and Its Copolymer Films Prepared by Spin-Coating and Langmuir–Blodgett Method. *Polymers* **2019**, *11*, 2033.
- (21) Qian, J.; Jiang, S.; Wang, Q.; Yang, C.; Duan, Y.; Wang, H.; Guo, J.; Shi, Y.; Li, Y. Temperature Dependence of Piezo- and Ferroelectricity in Ultrathin P(VDF–TrFE) Films. *RSC Adv.* **2018**, *8*, 29164.
- (22) Feng, T.; Xie, D.; Zang, Y.; Wu, X.; Ren, T.; Pan, W. Temperature Control of P(VDF-TrFE) Copolymer Thin Films. *Integr. Ferroelectr.* **2013**, *141* (1), 187–194.
- (23) Xia, W.; Peter, C.; Weng, J.; Zhang, J.; Kliem, H.; Jiang, Y.; Zhu, G. Epitaxy of Ferroelectric P(VDF-TrFE) Films via Removable PTFE Templates and Its Application in Semiconducting/Ferroelectric Blend Resistive Memory. *ACS Appl. Mater. Interfaces* **2017**, *9*, 12130.
- (24) Majumdar, S.; Chen, B.; Qin, Q. H.; Majumdar, H. S.; van Dijken, S. Electrode Dependence of Tunneling Electroresistance and Switching Stability in Organic Ferroelectric P(VDF-TrFE)-Based Tunnel Junctions. *Adv. Funct. Mater.* **2018**, *28*, 1703273.
- (25) Guan, Z.; Jiang, Z.-Z.; Tian, B.-B.; Zhu, Y.-P.; Xiang, P.-H.; Zhong, N.; Duan, C.-G.; Chu, J.-H. Identifying Intrinsic Ferroelectricity of Thin Film with Piezoresponse Force Microscopy. *AIP Adv.* **2017**, *7*, 095116.
- (26) Garcia, V.; Bibes, M. Ferroelectric Tunnel Junctions for Information Storage and Processing. *Nat. Commun.* **2014**, *5*, 4289.
- (27) Brinkman, W. F.; Dynes, R. C.; Rowell, J. M. Tunneling Conductance of Asymmetrical Barriers. *J. Appl. Phys.* **1970**, *41*, 1915.
- (28) Eshraghi, K.; Bandaru, P. R. Enhancement of Photoelectron Emission Efficiency from Quantum Dot Solids, through Electrical Field Biasing of Interfaces. *Appl. Phys. Lett.* **2021**, *118*, 263104.
- (29) Eshraghi, K.; Natani, S.; Bandaru, P. R. Modeling Electronic Conduction in Quantum Dot Constituted Assemblies Coupled to Metallic Electrodes. *Appl. Phys. Lett.* **2023**, *122* (23), 233104.
- (30) DiStefano, T. H.; Eastman, D. E. Photoemission Measurements of the Valence Levels of Amorphous SiO₂. *Phys. Rev. Lett.* **1971**, *27* (23), 1560–1562.
- (31) Sandu, T.; Tibeica, C.; Plugaru, R.; Nedelcu, O.; Plugaru, N. Insights into Electron Transport in a Ferroelectric Tunnel Junction. *Nanomaterials* **2022**, *12* (10), 1682.
- (32) Zhuravlev, M. Y.; Wang, Y.; Maekawa, S.; Tsymbal, E. Y. Tunneling Electroresistance in Ferroelectric Tunnel Junctions with a Composite Barrier. *Appl. Phys. Lett.* **2009**, *95* (5), 052902.
- (33) Mahdi, R. I.; Gan, W. C.; Majid, W. H. A. Hot Plate Annealing at a Low Temperature of a Thin Ferroelectric P(VDF-TrFE) Film with an Improved Crystalline Structure for Sensors and Actuators. *Sensors* **2014**, *14*, 19115.
- (34) Jensen, K. *Introduction to the Physics of Electron Emission*. Wiley: 2017.
- (35) Gajek, M.; Bibes, M.; Fusil, S.; Bouzehouane, K.; Fontcuberta, J.; Barthélémy, A.; Fert, A. Tunnel Junctions with Multiferroic Barriers. *Nat. Mater.* **2007**, *6* (4), 296–302.
- (36) Slotboom, J. W. The Pn-Product in Silicon. *Solid-State Electron.* **1977**, *20*, 279.
- (37) Pantel, D.; Alexe, M. Electroresistance Effects in Ferroelectric Tunnel Barriers. *Phys. Rev. B* **2010**, *82* (13), 134105.
- (38) Wang, J. L.; Liu, B. L.; Zhao, X. L.; Tian, B. B.; Zou, Y. H.; Sun, S.; Shen, H.; Sun, J. L.; Meng, X. J.; Chu, J. H. Transition of the Polarization Switching from Extrinsic to Intrinsic in the Ultrathin Polyvinylidene Fluoride Homopolymer Films. *Appl. Phys. Lett.* **2014**, *104* (18), 182907.
- (39) Majumdar, S. Back-End CMOS Compatible and Flexible Ferroelectric Memories for Neuromorphic Computing and Adaptive Sensing. *Adv. Intell. Syst.* **2022**, *4*, 2100175.
- (40) Das, S.; Chen, A.; Marinella, M. IRDS 2022: Beyond CMOS and Emerging Materials Integration. In *2021 IEEE International Roadmap for Devices and Systems Outbriefs*; IEEE: 2022.
- (41) Lemme, M. C.; Akinwande, D.; Huyghebaert, C.; Stampfer, C. 2DMaterials for Future Heterogeneous Electronics. *Nat. Commun.* **2022**, *13*, 1392.
- (42) Zhang, Y.; Cui, C.; He, C.; Ouyang, T.; Li, J.; Chen, M.; Tang, C. Vertical Ferroelectricity in van Der Waals Materials: Models and Devices. *Appl. Phys. Lett.* **2023**, *123*, 142901.
- (43) Lindemann, W. R.; Philip, R. L.; Chan, D. W. W.; Ayers, C. T.; Perez, E. M.; Beckman, S. P.; Strzalka, J.; Chaudhary, S.; Vaknin, D. Oriented Polyvinylidene Fluoride–Trifluoroethylene (P(VDF–TrFE)) Films by Langmuir–Blodgett Deposition: A Synchrotron X-Ray Diffraction Study. *Phys. Chem. Chem. Phys.* **2015**, *17*, 29335.
- (44) Kumar, M.; Georgiadou, D. G.; Seitzhan, A.; Loganathan, K.; Yengel, E.; Faber, H.; Naphade, D.; Basu, A.; Anthopoulos, T. D.; Asadi, K. Colossal Tunneling Electroresistance in Co-Planar Polymer Ferroelectric Tunnel Junctions. *Adv. Electron. Mater.* **2020**, *6* (2), 1901091.

- (45) Cheng, L.; Sun, H.; Xu, J.; Yu, C.; Xiao, H.; Wang, R.; Xu, L.; Zeng, Z.; Liang, S. Emulation of Synaptic Behavior by Organic Ferroelectric Tunnel Junctions. *Phys. Lett. A* **2021**, *392*, 127138.
- (46) Majumdar, S. Ultrafast Switching and Linear Conductance Modulation in Ferroelectric Tunnel Junctions via P(VDF-TrFE) Morphology Control. *Nanoscale* **2021**, *13* (25), 11270–11278.



CAS BIOFINDER DISCOVERY PLATFORM™

PRECISION DATA FOR FASTER DRUG DISCOVERY

CAS BioFinder helps you identify targets, biomarkers, and pathways

Unlock insights

CAS 
A division of the
American Chemical Society