CS 2200 - Introduction to Systems

Fall 2016

Homework 7

Rules:

- Please print a copy of the assignment and handwrite your answers. No electronic submissions are allowed. **Please print as one double-sided page.**
- This is an individual assignment. No collaboration is permitted.
- Due Date: 2nd November 2016 – 6:05 PM . Bring your BuzzCard.

Name(print)_____ GT Login:_____ Section_____

1) Given a **direct mapped cache** with the following specifications:

- 16 bit physical addresses
- 16 byte blocks
- 4 KB cache size for data
- Byte addressable

Mark each memory access as a cache hit or miss in the table provided. If it is a miss, specify the type of miss. Assume that the cache is initially empty, and none of these locations have been in the cache before.

ADDRESS	HIT/MISS	TYPE
0x1420	Miss	compulsory
0x1240	Miss	compulsory
0x1428	Hit	X
0x566F	Miss	compulsory
0x266F	Miss	compulsory
0x5664	Miss	conflict
0x5662	Hit	X
0x1242	Hit	X
0x8242	Miss	compulsory
0x1248	Miss	conflict

2) Use the following cache parameters to answer the question:

- 4 way Set Associative
- 2 MB of data cache size
- 64 bit addresses
- 32 byte blocks
- Byte addressable
- LRU Replacement Policy

Draw the layout of how this cache will interpret an address using the figure below as a guide. Label all parts of the address and their respective sizes.

Tag 45 bits	Index 14 bits	Offset 5 bits

3) Given the following processes, use the blanks provided above the diagrams to identify the algorithm used to generate the CPU timeline, as well as if it is preemptive or not. The I/O timeline will always be First Come First Served.

Process	CPU Burst 1	I/O Burst 1	CPU Burst 2	Priority
P1	3	5	1	7
P2	5	1	1	3
P3	2	5	2	5

Algorithm A SRTF_____ Preemptive? Yes_____

Time	0	1	2	3	4	5	6	7	8	9	10	11	12	13
CPU	P3	P3	P1	P1	P1	P2	P2	P3	P3	P2	P2	P2	P1	P2
I/O	-	-	P3	P3	P3	P3	P3	P1	P1	P1	P1	P1	P2	-

Algorithm B_Priority_____ Preemptive? _Yes_____

Time	0	1	2	3	4	5	6	7	8	9	10	11	12	13
CPU	P1	P1	P1	P3	P3	P2	P2	P2	P1	P2	P2	-	-	P3
I/O	-	-	-	P1	P1	P1	P1	P1	P3	P3	P3	P3	P3	P2