CS 2200 - Introduction to Systems

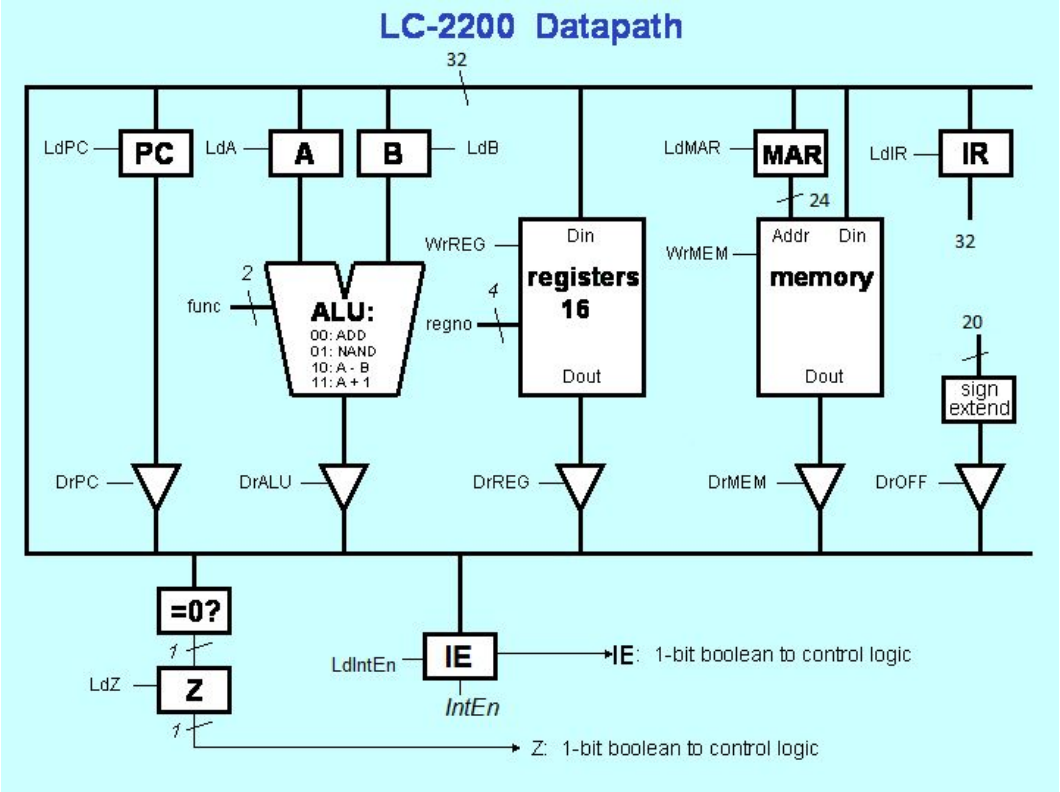
Fall 2016

Homework 3

Rules:

- Please print a copy of the assignment and handwrite your answers. No electronic submissions are allowed. **Please print as one double-sided page.**
- This is an individual assignment. No collaboration is permitted.
- Due Date: 21th September 2016 – 6:05 PM . Bring your BuzzCard.

Name (please print):_____ GTLogin:_____ Section____



The above is the datapath of the LC-2200 with relevant signals labeled. Use this to answer the following questions.

1. Write out the microstates for FETCH. For each microstate, state **both** the **datapath actions** (i.e. A ← Rx) as well as the **control signals.** You will lose points for an inefficient answer. **(15 pts)**
   FETCH1: A<-PC, MAR<-PC |||| DrPC, LdA, LdMAR
   FETCH2: IR<-MEM[PC] |||| DrMEM, LdIR
   FETCH3: PC <- PC+1 |||| DrALU, LdPC, func = 11

[+5 for each correct clock] All or nothing - This answer was given in class, so any errors -> 0 points for that clock cycle.

2. Suppose we wanted to introduce a new instruction to the existing ISA called LW2 which assembles as `LW2 Rx, Ry, Rz` and does the operation listed below. List all of the microstates needed to implement LW2. For each microstate, specify **both** the **datapath actions** as well as the **control signals.** You will lose points for an inefficient answer. (Note: You can simply say regno = RX for example instead of saying on or off) **(40 pts)**

```
LW2:    Rx <- MEM[Ry + Rz]

LW2-1: A <- RY |||| DrREG, regno = RY, LdA
LW2-2: B <- RZ |||| DrREG, regno = RZ, LdB
LW2-3: MAR <- RY + RZ |||| DrALU, func = 00, LdMAR
LW2-4: RX <- MEM[RY + RZ] |||| DrMEM, WrREG, regno = RX
```

3. Normally, every microstate has a static "next state" field which indicates which state it will ALWAYS enter next. However, in the LC-2200, there are two cases where this is not the case, and the "next state" associated with the state is not enough information to determine the next state. Name **both** these cases and what extra information they need to determine the next microstate. **(30 pts)**

End of Fetch/Before Decode. Need OP code
BEQ or branch instructions. Need Z value

4. For the table below, fill out whether or not each program discontinuity is synchronous or asynchronous, whether it is internal or external, and give an example of each. **(15 pts)**

Type	Sync/ Async	Internal/External	Example
Exception	Sync	Internal	Ex: Divide by zero, overflow, etc.
Trap	Sync	Internal	Ex: System calls (page fault, etc)
Interrupt	Async	External	Ex: Hardware devices (mouse, keyboard, etc.)