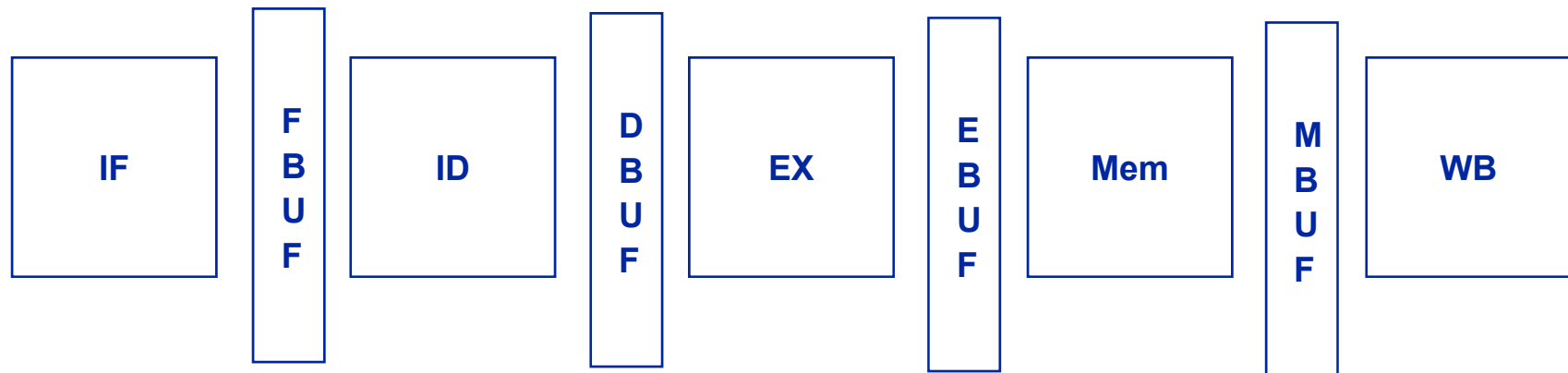
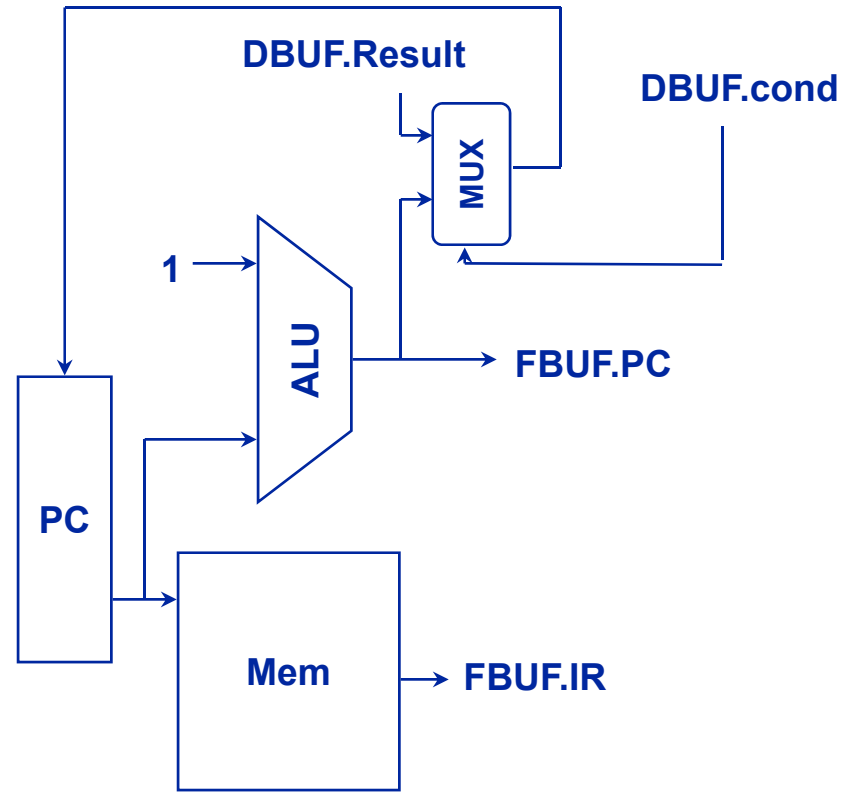

Pipeline top level



How to Execute an Instruction

○ Instruction fetch (“IF”)

- ◆ $\text{FBUF.IR} = \text{Mem}[\text{PC}]$
- ◆ $\text{NPC} = \text{PC} + 1$
- ◆ $\text{FBUF.PC} = \text{NPC}$
- ◆ if (DBUF.cond) $\text{PC} = \text{DBUF.Result}$ else $\text{PC} = \text{NPC}$

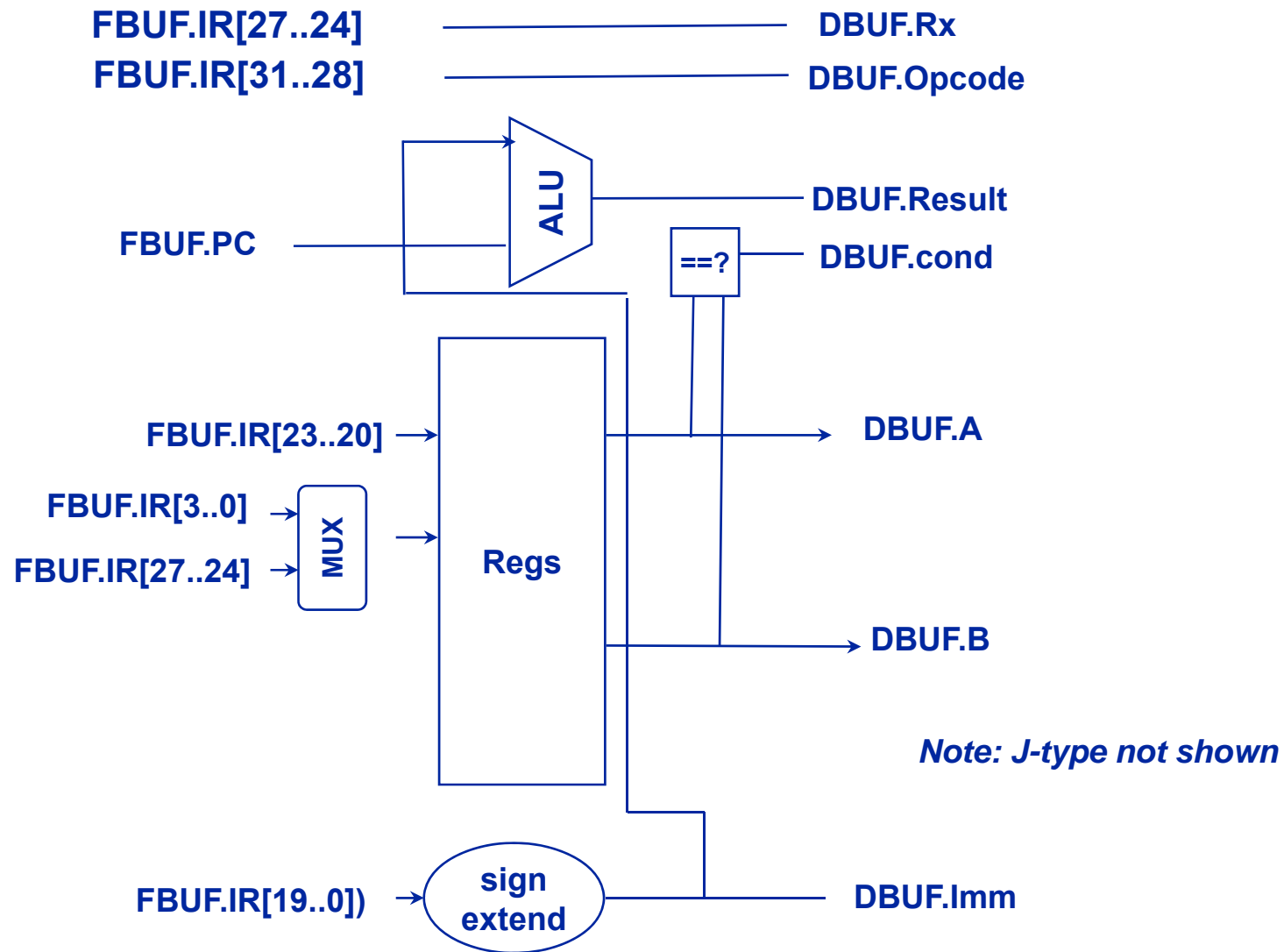


How to Execute an Instruction

○ Instruction decode/Register fetch (“ID”)

- ◆ $\text{DBUF.opcode} = \text{FBUF.IR}[31..28]$
- ◆ $\text{DBUF.A} = \text{Regs}[\text{IR}[23..20]]$
- ◆ if ($\text{DBUF.opcode} == 0100$) // A “sw”
 - ◇ $\text{DUF.B} = \text{Regs}[\text{IR}[27..24]]$
- ◆ Else
 - ◇ $\text{DUF.B} = \text{Regs}[\text{IR}[3..0]]$
- ◆ $\text{DBUF.Imm} = \text{sign-extend}(\text{FBUF.IR}[19..0])$
- ◆ $\text{DBUF.Rx} = \text{FBUF.IR}[27..24]$
- ◆ $\text{DBUF.PC} = \text{FBUF.PC}$
- ◆ $\text{DBUF.Result} = \text{FBUF.PC} + \text{Imm}$
- ◆ $\text{DBUF.Cond} = (\text{A} == \text{B})$
- ◆ If ($\text{DBUF.opcode} == 0110$) // J-type
 - ◇ $\text{Regs}[\text{DBUF.IR}[3..0]] = \text{FBUF.PC}$
 - ◇ $\text{DBUF.Result} = \text{DBUF.A}$
 - ◇ $\text{DBUF.Cond} = 1$

Instruction decode

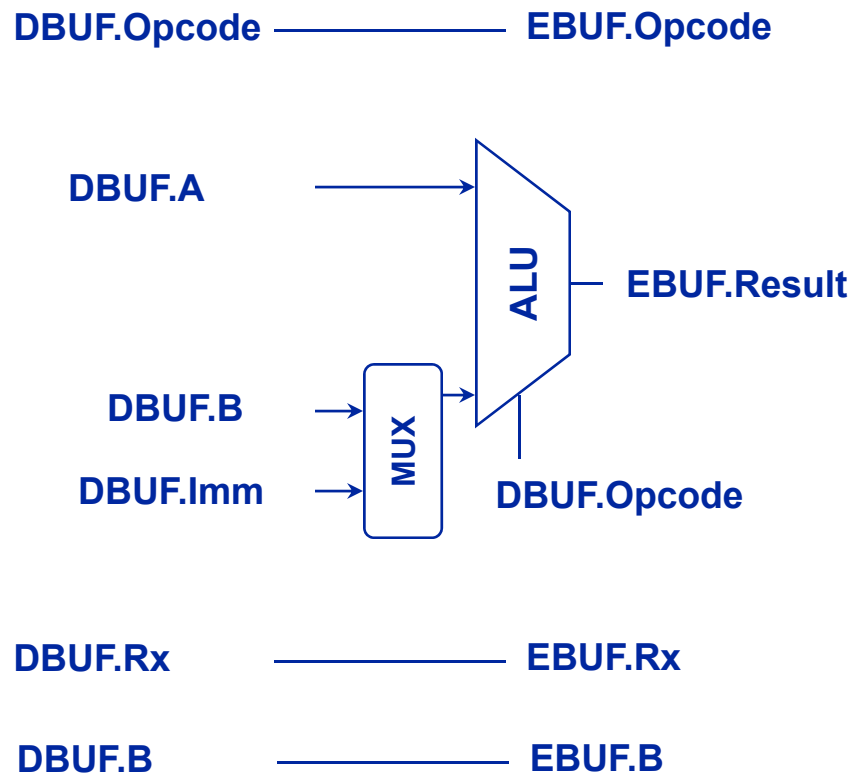


Executing an Instruction (cont.)

○ Execute (“EX”)

- ◆ $\text{EBUF.Rx} = \text{DBUF.Rx}$
- ◆ $\text{EBUF.B} = \text{DBUF.B}$
- ◆ $\text{EBUF.Opcode} = \text{DBUF.Opcode}$
- ◆ I-type ($\text{EBUF.Opcode} == \text{lw, sw, addi, nandi}$):
 - ◇ $\text{EBUF.Result} = \text{DBUF.A op DBUF.Imm}$
- ◆ I-type ($\text{EBUF.Opcode} == \text{BEQ}$)
 - ◇ Do nothing (done in ID) // for BEQ
- ◆ R-type:
 - ◇ $\text{EBUF.Result} = \text{DBUF.A op DBUF.B}$

Execute stage



Executing an Instruction (cont.)

○ Memory Access/Branch completion (“MEM”)

- ◆ MAR = EBUF.Result
- ◆ Din = EBUF.B
- ◆ if (EBUF.opcode = 0100) WtMem=1 // sw
- ◆ else WtMem = 0 // lw
- ◆ MBUF.Rx = EBUF.Rx
- ◆ if (EBUF.opcode = 0011) MBUF.Result = Dout
- ◆ else MBUF.Result = EBUF.Result

○ Write back (“WB”)

- ◆ If (R-type or I-type and != sw, beq)
 - ◇ Regs[MBUF.Rx] = MBUF.Result

