A 7T SRAM Cell using Supply Feedback Technique

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Abstract— **As the CMOS technology is scaled down it creates issues like power dissipation and stability issues in static random access memory (SRAM). Here we are designing an SRAM to address the issue with data stability and power dissipation with the help of Synopsys custom design tool in 28nm technology node.**

Keywords—7T SRAM, NMOS, PMOS, supply feedback.

I. Introduction

Semiconductor devices scaling has been going on for more than the last five decades. High demand in the electronic market for cheaper, enhanced performance, more functionalities portable devices has resulted in rampant scaling of semiconductor devices. In the novel 7T SRAM cell design the read and write operation have been performed separately using read and write port to enhance the data stability. Furthermore, the supply feedback transistor has been used between data storing node and cell power supply in order to increase the write ability of the SRAM cell.

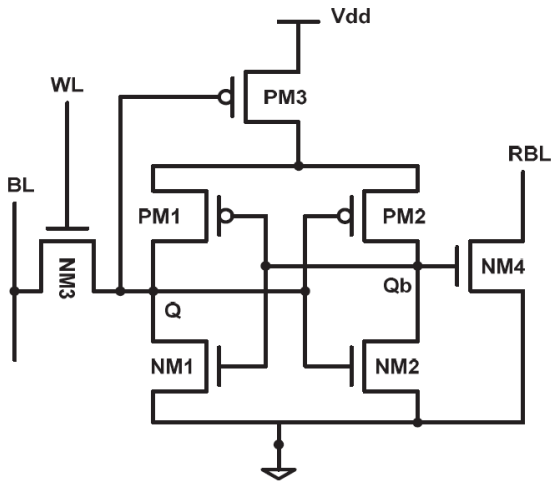

Fig. 1. Schematic diagram of the design.

II. 7T Sram Design

The conventional 6T SRAM cell utilizes a common path for read and write operation. Hence with the lowering of supply voltage, the data stability of Fig. 1 depicts the proposed 7T SRAM cell using supply feedback concept, which comprises of 4 NMOS transistors and three PMOS transistors. Transistor PM1, PM2, NM1, and NM2 forms the latch of SRAM cell where the data has been stored, whereas NM3 acts as an access transistor during the write operation which is activated by word line (WL) signal and NM4 acts as an access transistor during read mode which basically used to separate the RBL from storing nodes Qb and Q of SRAM cell for providing disturb free read operation. The transistor PM3 acts as a feedback transistor which is connected between the power supply and storing node Q. This type of feedback configuration reduces the strength of the pull-up path in write operation which increases the chance of flipping the states of data very fast. When feedback transistor PM3 is ON state, the voltage at the drain of PM3 is slightly lower than the supply voltage. This eventually saves power as the reduced supply voltage is available to the latch. The bitline (BL) is an input line of a cell during write operation whereas RBL is input or output line during the read operation. The cell ratio and pull up ratio of the proposed design are kept as 1.7 and 0.8 respectively.

III. 7T Sram Waveform

The transient waveform during a write operation is presented in Fig. 2. Assume the node Q and BL are initially set to logic ‘0’ and ‘1’ respectively. As shown in Fig. 2, the data retained at storing node Q and Qb when WL is initially at 0 V. Then as WL progresses to Vdd, the data in node Q changing and reached the value of BL at 0.9 V cell supply voltage. When again WL falls down to 0 V then the data stored in node Q has been retained as shown in Fig. 2.

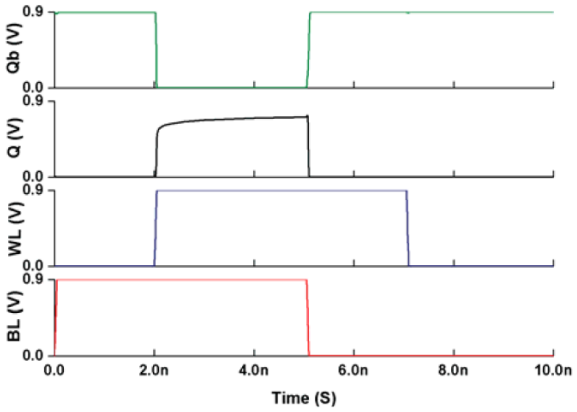

Fig. 2. Transient waveform of 7T SRAM during a write operation

The total area consumed by the proposed 7T SRAM cell is 3.2um^2.

References

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