Sne Samal

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EDUCATION

Imperial College London **London, UK**

Electronic and Information Engineering MEng *Graduation Date: Jun 2026*

- Year 1 Mark: 76.12 (1st Class). Dean's List (top 10% of cohort)
- Year 2 Mark: 72.44 (1st Class).
- Year 1 Modules of Interest: Maths, Digital Electronics & Computer Architecture, Programming in C++
- Year 2 Modules of Interest: Instruction Architecture & Compilers, Software Systems (Networks & Databases), Discrete Math
- Societies: Data Science, Electrical Engineering, Department of Computing.

WORK EXPERIENCE

Imperial College London **London, UK**

Undergraduate Tutor *Oct 2023 – present*

- Tutoring digital electronics and computer architecture to first year electrical and electronic undergraduates
- Arranged hourly 1:1 sessions, going through course content and ensuring that students leave with a stronger understanding.

Embedd.it **London, UK**

Electronics Engineer Intern *Jul 2023 – Sep 2023*

- Led analysis of electronic component databases to identify the most popular digital interfaces and vendors.
- Automated the creation of JSON files, later read by large language models, from datasheets using Python and Pandas,
- Analysed datasheets analysis to extract critical information, enabling faster decision-making in the development process.

PROJECT EXPERIENCE

FPGA Market Making

System Verilog, C++, Python, Vivado, Git, Cocotb, Verilator, Icarus Verilog *Jul 2024 – Sep 2024*

- Wrote HDL for the Avellaneda-Stoikov market making strategy and an order book capable of processing ITCH for 4 stocks.
- Produced an exchange simulation in Python to execute, send and receive orders to and from the module on a PYNQ Z1
- Comprehensively simulated and tested each sub module using both Cocotb testbenches and C++ testbenches using Verilator.

HDL RMII Ethernet Packet Generation and Reception

System Verilog, Python, Icarus Verilog, Cocotb *Sep 2024*

- Wrote System Verilog to generate and receive ethernet packets, supporting UDP/IP communication protocols.
- Created an FSM to handle packet processing, including preamble detection, header parsing and data extraction/generation.
- Simulated RMII signals with Python to send and receive packets.

FPGA Voxel Integer Ray Tracer

C++, System Verilog, Python, Bash, Git, Verilator, Vivado *May 2024 – Jun 2024*

- Developed an integer-based voxel ray tracer that was accelerated via hardware, achieving speeds 1000 times faster than Python and 120 times faster than C++ software equivalents
- Wrote System Verilog logic to perform ray tracing, including the generation of rays from a given camera position and direction and wrote logic for rays to traverse a scene and return a correct pixel colour depending on whether an object was hit.
- Implemented on a PYNQ Z1, used MMIO to pass camera parameters. Generated and outputted frames via VDMA.

C90 to RISC-V Compiler

C++, C, RISC-V Assembly, Make, Bash, Git, GitHub *Feb 2024 – Mar 2024*

- Developed a functional C90 to RISC-V assembly, in C++ with support for integers, floats, pointers, arrays, chars and structs.
- Added support for control-flow including if-else, for and while, enums, nested and recursive functions and the built-in sizeof.
- Used Make for build automation and created Bash scripts to automate testing and validation of outputs.

DotsApp: Real Time FPGA Morse Code Chatting App

C, Python, Verilog, Quartus, AWS, EC2, DynamoDB. Git, GitHub *Mar 2024*

- Produced a real time chat application where users use tilt gestures on a DE10-Lite to talk in Morse code to different rooms.
- Instantiated and programmed a NIOS II soft processor to process gestures and send back to the host computer via UART.
- Tkinter client and a python server running on an EC2 instance used to handle messages, with history stored on DynamoDB.

RISC-V CPU

C++, System Verilog, Python, Verilator, WLS, Git, GitHub *Oct 2023 – Dec 2023*

- Programmed a functional multi-stage pipe-lined processor in a team of 4, compliant with RISC-V specification (RV32I 2.0).
- Involved CPU design, C++ testbenching and debugging, workflow automation and documentation
- Implemented functional and verified pipelining and data cache within the processor for improved performance.

SKILLS & INTERESTS

Skills: C/C++, Python, Assembly, System Verilog, JavaScript, Git, GitHub, SQL, Markdown, LaTeX, Arduino, Django, Flutter
Interests: Computer Architecture, Micro-Architecture, FPGAs, Digital Logic Design, Machine Learning, Digital Electronics, Embedded Systems, Compiler Design.