

Sne Samal

London, UK | +44 7398892448 | sne.samal22@imperial.ac.uk | sne-samal.github.io/portfolio/

EDUCATION

Imperial College London

London, UK

Electronic and Information Engineering MEng

Graduation Date: Jun 2026

- Year 1 Mark: 76.12 (1st Class). Dean's List (top 10% of cohort)
- Year 2 Mark: 72.44 (1st Class).
- Year 1 Modules of Interest: Maths, Digital Electronics & Computer Architecture, Programming in C++
- Year 2 Modules of Interest: Instruction Architecture & Compilers, Software Systems (Networks & Databases), Discrete Math
- Societies: Data Science, Electrical Engineering, Department of Computing.

WORK EXPERIENCE

Imperial College London

London, UK

Undergraduate Tutor

Oct 2023 – present

- Tutoring digital electronics and computer architecture to first year electrical and electronic undergraduates
- Arranged hourly 1:1 sessions, going through course content and ensuring that students leave with a stronger understanding.

Embedd.it

London, UK

Electronics Engineer Intern

Jul 2023 – Sep 2023

- Led analysis of electronic component databases to identify the most popular digital interfaces and vendors.
- Automated the creation of JSON files, later read by large language models, from datasheets using Python and Pandas,
- Analysed datasheets analysis to extract critical information, enabling faster decision-making in the development process.

PROJECT EXPERIENCE

Myelin Health

Flutter, Dart, Supabase

Sep 2024- present

- Built a healthcare booking app with Flutter, Dart, and Supabase for appointments and service listings.
- Created user-friendly interfaces for patients and healthcare providers to streamline bookings.
- Implemented real-time data sync using Supabase for appointments and service details.

NASDAQ Simulator and Market Maker

C++, Python, System Verilog, Vivado, Git, Cocotb, Verilator, Icarus Verilog

Jul 2024 – Sep 2024

- Wrote code to simulate the NASDAQ exchange, randomly generating and executing orders and maintaining an order book.
- Implemented the Avellaneda-Stoikov market making strategy in python to react to changes in the market simulation.
- Both programs used to simulate and verify a hardware equivalent, written in System Verilog.

Python and C++ Ray Tracer

C++, System Verilog, Python, Bash, Git, Verilator, Vivado

May 2024 – Jun 2024

- Developed an integer-based voxel ray tracer that was accelerated via hardware, achieving speeds 1000 times faster than Python and 120 times faster than C++ software equivalents
- Wrote System Verilog logic to perform ray tracing, including the generation of rays from a given camera position and direction and wrote logic for rays to traverse a scene and return a correct pixel colour depending on whether an object was hit.
- Implemented on a PYNQ Z1, used MMIO to pass camera parameters. Generated and outputted frames via VDMA.

C90 to RISC-V Compiler

C++, C, RISC-V Assembly, Make, Bash, Git, GitHub

Feb 2024 – Mar 2024

- Developed a functional C90 to RISC-V assembly, in C++ with support for integers, floats, pointers, arrays, chars and structs.
- Added support for control-flow including if-else, for and while, enums, nested and recursive functions and the built-in sizeof.
- Used Make for build automation and created Bash scripts to automate testing and validation of outputs.

DotsApp: Real Time FPGA Morse Code Chatting App

C, Python, Verilog, Quartus, AWS, EC2, DynamoDB, Git, GitHub

Mar 2024

- Produced a real time chat application where users use tilt gestures on a DE10-Lite to talk in Morse code to different rooms.
- Instantiated and programmed a NIOS II soft processor in C to process gestures and send back to the host computer via UART.
- Tkinter client and a python server running on an EC2 instance used to handle messages, with history stored on DynamoDB.

RISC-V CPU

C++, System Verilog, Python, Verilator, WLS, Git, GitHub

Oct 2023 – Dec 2023

- Programmed a functional multi-stage pipe-lined processor in a team of 4, compliant with RISC-V specification (RV32I 2.0).
- Involved CPU design, C++ testbenching and debugging, workflow automation and documentation
- Implemented functional and verified pipelining and data cache within the processor for improved performance.

SKILLS & INTERESTS

Skills: C/C++, Python, Assembly, System Verilog, JavaScript, Git, GitHub, SQL, Markdown, LaTeX, Arduino, Django, Flutter

Interests: Computer Architecture, Micro-Architecture, FPGAs, Digital Logic Design, Machine Learning, Digital Electronics, Embedded Systems, Compiler Design.