AUTOMATED TELLER MACHINE (ATM) CONTROLLER

Group:51

INTRODUCTION

- This project focuses on building an ATM Controller using a hardware-first approach.

- It implements the ATM controller with pure digital logic.

- The system is implemented using a Finite State Machine (FSM).

- The goal is to create a secure, modular, and efficient ATM design using Verilog HDL.

PROJECT GOALS

- **Finite State Machine (FSM) Design**

1. Broke down ATM operations into distinct states.
2. Designed transitions based on user inputs and system conditions.

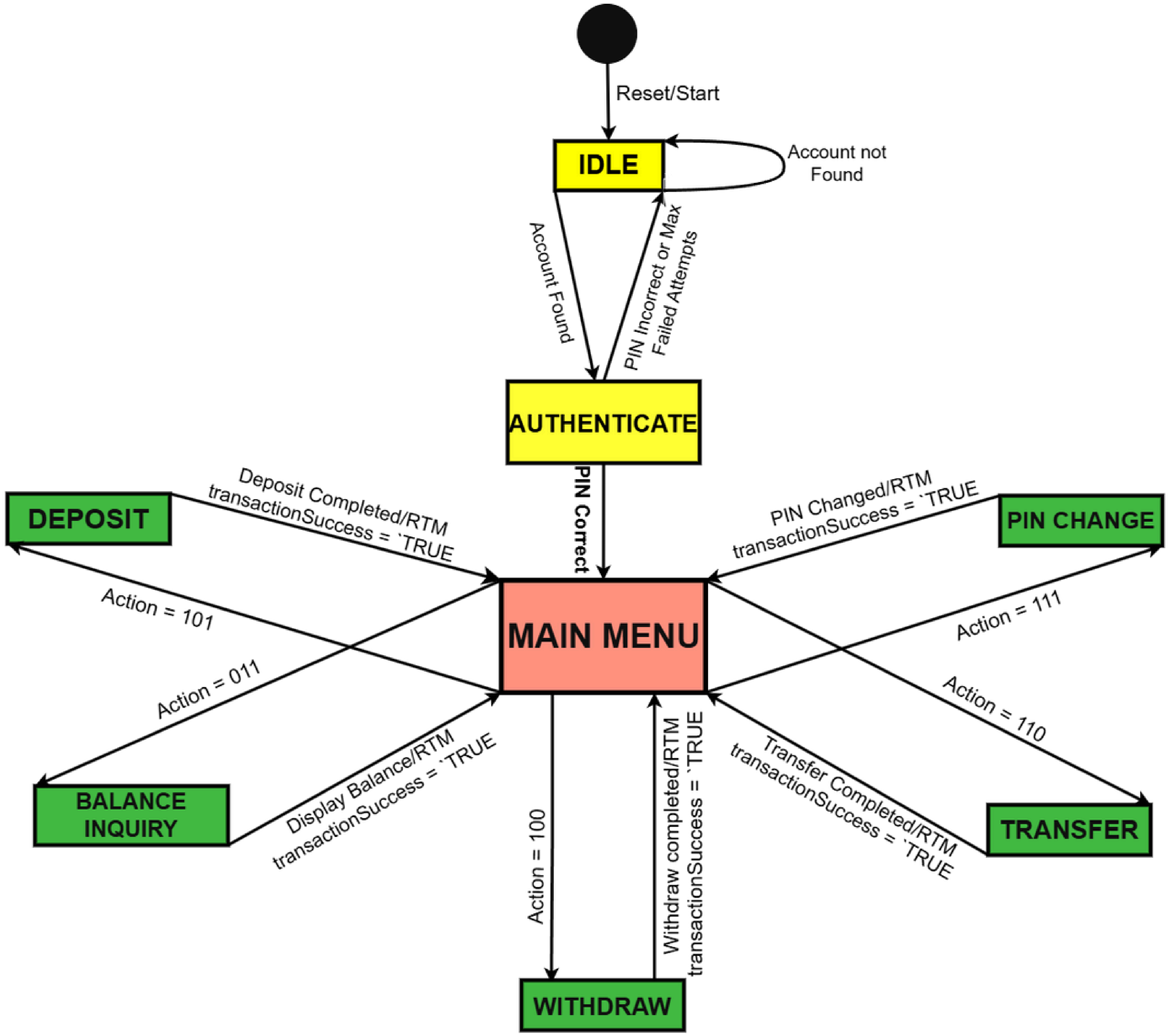
- **RTL Code in Verilog**

1. Implemented the FSM at the Register Transfer Level (RTL).
2. Defined logic for state transitions and control behavior.

- **Physical Layout Generation using Qflow**

1. Used Qflow toolchain to process Verilog code.
2. Completed synthesis, placement, and routing to generate chip layout.

FINITE STATE MACHINE (FSM)


Reset/Start
IDLE
Account not Found
Account Found
PIN Incorrect or Max Failed Attempts
AUTHENTICATE
PIN Correct
MAIN MENU
DEPOSIT
Deposit Completed/RTM transactionSuccess = `TRUE
Action = 101
PIN CHANGE
PIN Changed/RTM transactionSuccess = `TRUE
Action = 111
BALANCE INQUIRY
Action = 011
Display Balance/RTM transactionSuccess = `TRUE
TRANSFER
Action = 110
Transfer Completed/RTM transactionSuccess = `TRUE
WITHDRAW
Action = 100
Withdraw completed/RTM transactionSuccess = `TRUE

1) IDLE

- The ATM is inactive, waiting for userinput.
- No transactions are processed during thistime.

2) AUTHENTICATE (PIN Verification)

- The user enters their PIN for verification.
- If PIN is correct, transition to the Main Menu and if PIN is incorrect, transition to the IDLE State.

3) MAIN MENU

- Based on the Action input, the system branches into specific functional paths.

4) BALANCE INQUIRY

- User checks the account balance.
- After showing the balance, it returns to the Main Menu.

5) WITHDRAW

- Waits for user to enter the amount.
- If sufficient balance, withdraw is successful; otherwise, failure is reported and returns to the Main Menu.

6) DEPOSIT

- Waits for user to enter the amount.
- User deposits money into the account.
- After the transaction, the system returns to the Main Menu.

7) TRANSFER

- Waits for required inputs and Checks if destination account exists and if sufficient balance is available.
- User transfers money to another account. The system then returns to the Main Menu.

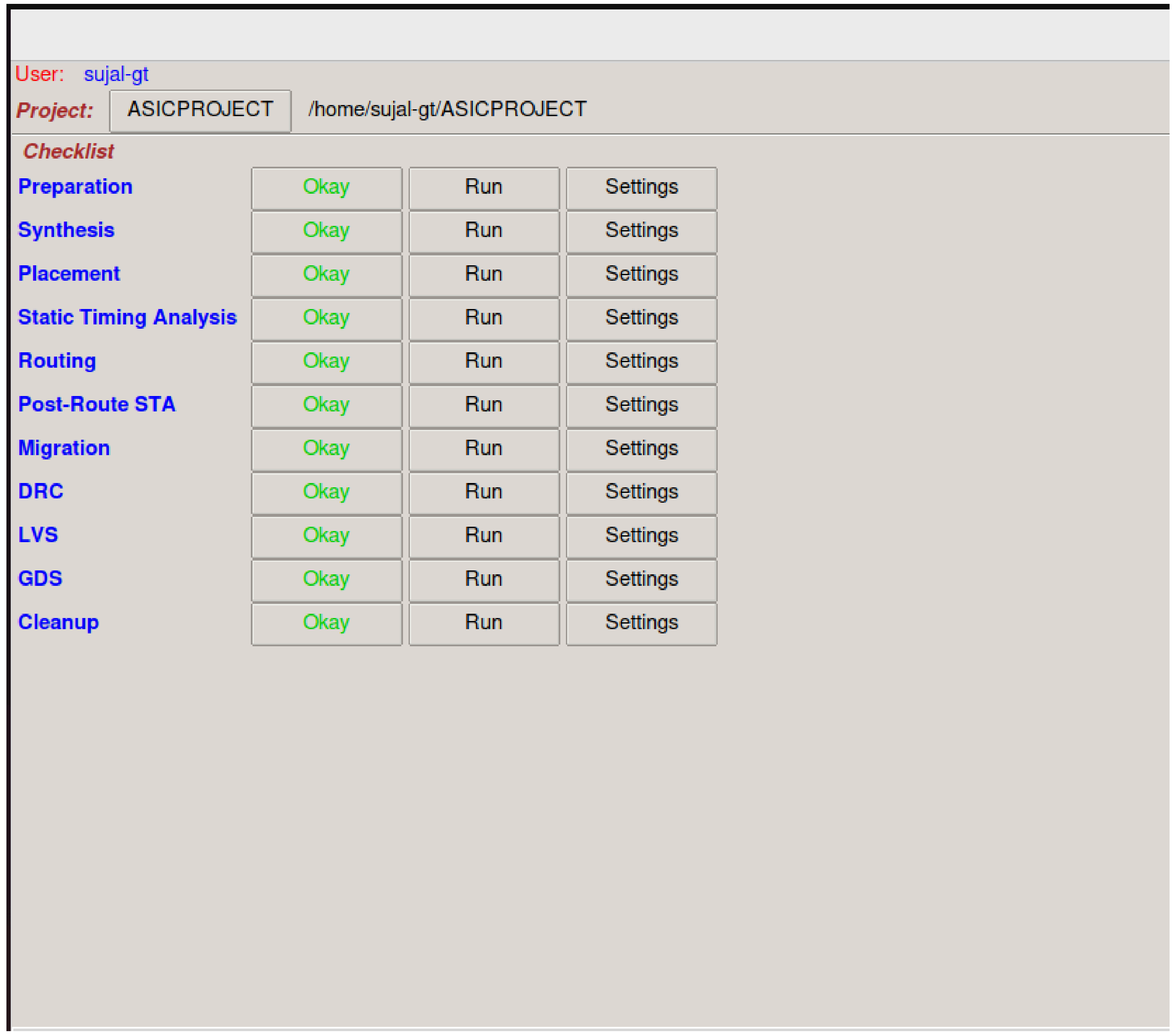
8) PIN CHANGE

- Waits for user to enter new PIN.
- After successful change, return to Main Menu

RTL CODE IN VERILOG & SIMULATION RESULTS

Verilog Code and Testbench code: **LINK**

QFLOW IMPLEMENTATION



User: sujal-gt

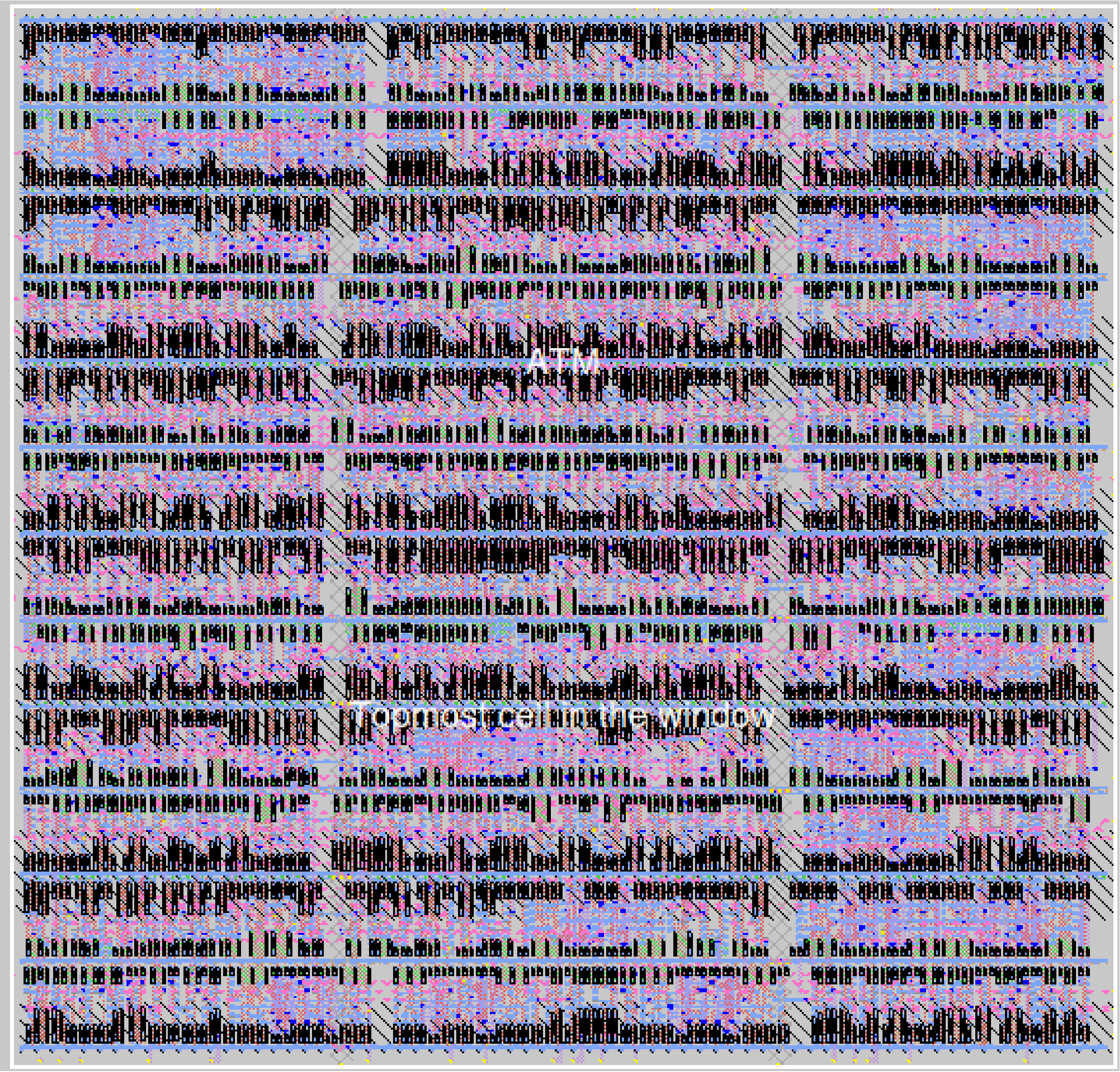
Project: ASICPROJECT /home/sujal-gt/ASICPROJECT

Checklist

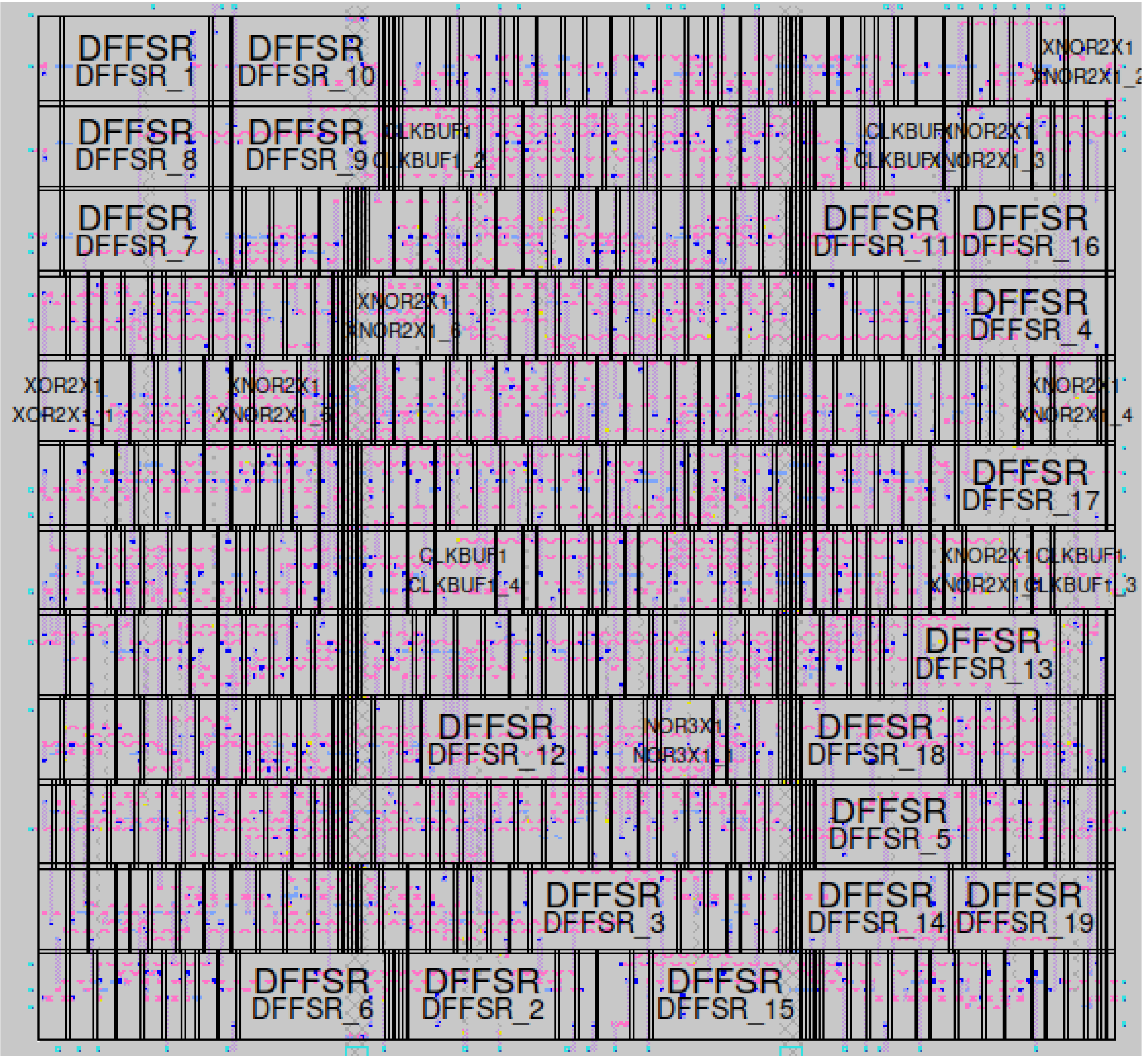
Preparation	Okay	Run	Settings
Synthesis	Okay	Run	Settings
Placement	Okay	Run	Settings
Static Timing Analysis	Okay	Run	Settings
Routing	Okay	Run	Settings
Post-Route STA	Okay	Run	Settings
Migration	Okay	Run	Settings
DRC	Okay	Run	Settings
LVS	Okay	Run	Settings
GDS	Okay	Run	Settings
Cleanup	Okay	Run	Settings

- **Preparation**: Sets up environment and checks necessary files.
- **Synthesis**: Converts RTL to gate-level netlist.
- **Placement**: Arranges gates on chip without wiring.
- **Static Timing Analysis**: Verifies signal timing meets constraints.
- **Routing**: Connects placed gates using metal layers.
- **Post-Route STA**: Checks timing after routing.
- **Migration**: Prepares layout for fabrication format.
- **DRC**: Ensures layout follows design rules.
- **LVS**: Matches layout with original netlist.
- **GDS**: Exports final layout for fabrication.
- **Cleanup**: Deletes temporary files and finalizes project.

QFLOW RESULTS



Final Physical Layout of ATM Controller



Logic-Level Layout of ATM Controller

TEAM MEMBERS

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THANK YOU