RAJIV GANDHI PROUDYOGIKI VISHWAVIDYALAYA, BHOPAL
New Scheme Based On AICTE Flexible Curricula
Electronics & Communication Engineering III-Semester
EC-303 Electronic Devices

Unit-1 Semiconductor Material Properties: Elemental & compound semiconductor materials , Bonding forces and Energy bands in intrinsic and extrinsic silicon, Charge carrier in semiconductors , carrier concentration, Junction properties, Equilibrium condition, biased junction, Steady state condition, breakdown mechanism (Rectifying Diodes, Zener Diodes), Metal Semiconductor Junction.
Special diodes: Tunnel diodes, Varactor diodes, Schottky diode, Photo diodes, Photodetector, LED, solar cell.

Unit-2 Diode circuits: Ideal and Practical diode, Clipper, Clamper.
Power Supply: Rectifiers-Half wave, Full wave, Bridge rectifier, filter circuits, Voltage regulation using shunt & series regulator circuits, Voltage regulation using IC.

Unit-3 Fundamentals of BJT: Construction, basic operation, current components and equations,CB, CE and CC configuration, input and output characteristics, Early effect, Region of operations: active, cut-off and saturation region. BJT as an amplifier. Ebers-Moll model, Power dissipation in transistor (Pd, max rating), Photo transistor. Transistor biasing circuits and analysis: Introduction, various biasing methods: Fixed bias,Self bias, Voltage Divider bias, Collector to base bias, Load-line analysis: DC and AC analysis, Operating Point and Bias Stabilization and Thermal Runaway. Transistor as a switch.

Unit-4 Small Signal analysis: Small signal Amplifier,Amplifier Bandwidth, Hybrid model,

analysis of transistor amplifier using h-parameter, Multistage Amplifier: Cascading amplifier,

Boot-strapping Technique, Darlington amplifier and cas-code amplifier, Coupling methods in **multistage amplifier, Low and high frequency response, Hybrid πmodel, Current Mirror circuits.**

Large Signal analysis and Power Amplifiers: Class A,Class B,Class AB, Class C, Class D, Transformer coupled and Push-Pull amplifier.

Unit-5 FET construction- JFET: Construction, n-channel and p-channel, transfer and drain characteristics, parameters, Equivalent model and voltage gain, analysis of FET in CG, CS and CD configuration. Enhancement and Depletion MOSFET drain and transfer Characteristics. Uni-junction Transistor (UJT) and Thyristors: UJT: Principle of operation, characteristics, UJT relaxation oscillator.

Text/Reference Books:
1. Millman & Halkias, “Electronic Devices And Circuits”, TMH.
2. Salivahanan, Kumar & Vallavaraj, “Electronic Devices And Circuits”, TMH.
3. Boylestad & Neshelsky, “Electronic Devices & Circuits”, PHI.
4. Schilling & Belove, “Electronic Circuits , Discrete & Integrated”, TMH.
5. Chattopadhyay & Rakhshit, “Electronic Fundamentals & Applications”, New Age
6. Adel S. Sedra & Kenneth C. Smith, “Microelectronic Circuits”, OUP.
7. R. A. Gayakwad, “Op-Amps And Linear Integrated Circuits”, PHI
8. Theodore F. Bogart, Jeffrey S. Beasley, “Guillermo Rico Electronic Devices & Circuits”.
9. Allen Mottershead, “Electronic Devices & Circuits”.

ELECTRONIC DEVICES LAB

1. Diode Characteristic
a) pn junction diode Characteristics and Static & Dynamic resistance measurement from graph.

b) To plot Zener diode Characteristics curve.

2. Clipper Clamper
a) To plot the Characteristics curve of various clamper circuits.
b) To plot the Characteristics curve of various clamper circuits.

3. Half wave, full wave & bridge rectifier
a) To measure Vrms, Vdc for half wave, full wave & bridge rectifier.
b) To measure ripple factor, ratio of rectification for full wave & half wave rectifier.

4. Voltage regulation using zener diode shunt regulator and transistor series voltage regulator in the following cases
a) Varying input
b) Varying load

5. Characteristic of BJT
a) To plot the input & output Characteristics curve in CB & CE configuration
b) To find & and Q point from the above curve.
c) To plot the Characteristics curve of various clipper circuits.

6. h- Parameter

7. Multi Stage Amplifier

a) To plot the Characteristics curve for Direct Coupled Amplifier.
b) To plot the Characteristics curve for RC Coupled Amplifier.
c) To plot the Characteristics curve for transformer Coupled Amplifier.

8. FET Characteristic

a) To plot the Characteristics curve for n channel – JFET in CS configuration.
b) To find out pinch off voltage from the above characteristics curve

9 UJT Characteristic

a) To plot the Characteristics curve for UJT.
b) To determine intrinsic stand off ratio.

Electronics & Communication Engineering, III-Semester
EC-303Electronic Device

UNIT-I: Semiconductor Material Properties: Elemental & compound semiconductor materials , Bonding forces and Energy bands in intrinsic and extrinsic silicon, Charge carrier in semiconductors , carrier concentration, Junction properties, Equilibrium condition, biased junction, Steady state condition, breakdown mechanism (Rectifying Diodes, Zener Diodes), Metal Semiconductor Junction. Special diodes: Tunnel diodes, Varactor diodes, Schottky diode, Photo diodes, Photo-detector, LED, solar cell.

1.1. Introduction: Conductors, Insulators, and Semiconductors

Conductors	Materials with many free electrons. These electrons can easily be made to flow through the material. all metals, semi-metals like carbon-graphite, antimony and arsenic
Insulators	Materials that have very few free electrons. plastic, glass and wood
Semiconductors	These materials lie between the extremes of good conductors and good insulators. They are crystalline materials that are insulators when pure, but will conduct when an impurity is added and/or in response to light, heat, voltage, etc. Examples: elements like silicon (Si), germanium (Ge), selenium (Se); compounds like gallium arsenide (GaAs) and indium antimonide (InSb)

1.1.1. Semiconductor Materials

1. Semiconductors are group of materials having electrical conductivities intermediate between metal and insulator.
2. The conductivity of these materials can be varied by changes in temperature, optical excitation and impurity content.
3. This variability of electrical properties makes the semiconductor materials natural choices for electronic device investigation.
4. Semiconductor materials are found in column IV and neighboring column of periodic table. The column IV semiconductor are called elemental semiconductor because they are composed of single species of atom.
5. The elemental semiconductor Ge was widely used in the early days of semiconductor development for transistors and diodes. Silicon is now used majority in transistors, rectifiers and integrated circuits.

In addition to elemental material, compounds of column III and V also can make up compound semiconductor. Most

1.1.2. Compound Semiconductors:

Compound semiconductors are from combinations of elements from Group III and Group V of the Periodic Table of the Elements (GaAs, GaP, InP and others). Other compound semiconductors are made from Groups II and VI (CdTe, ZnSe and others). It is also possible to use different elements from within the same group (IV), to make compound semiconductors such as SiC. Compound semiconductors provide capabilities in optoelectronics that cannot be obtained from silicon or germanium. Compound semiconductors exhibit strong absorption above their band gap energies. Typical wavelengths for band-edge absorption range from the ultraviolet to near-infrared.

1.2. Concept of energy bands:

The electrons in an isolated atom occupy discrete energy levels. When atoms are close to each other these electrons can use the energy levels of their neighbors. When the atoms are all regularly arranged in the crystal lattice of a solid, the energy levels become grouped together in a band. This is a continuous range of allowed energies rather than a single level. There will also be groups of energies that are not allowed, in what is known as a band gap.

An atomic orbital of one atom may overlap with an atomic orbital of another atom forming two molecular orbital. One, called the bonding molecular orbital, is of low energy and the other with higher energy is called the anti-bonding molecular orbital.

When two identical atoms are brought closer together, the quantized energy levels hybridize and split into two

different levels because of the mutual interaction of the two atoms. More generally, when N atoms are moved closer, until they reach the equilibrium inter-atomic distance d, the energy levels split into N levels. These N levels are very close to each other if N is large (which is the case in a crystal) so that they eventually form a continuous energy band.
Let's now consider silicon atoms arranged in a periodic lattice, but with a very large lattice parameter (or inter-atomic distance), in order to first consider each atom as isolated. The two levels with the highest energy are labeled E1 and E2. Now let's shrink the atom lattice: energy levels split and form two continuous bands known as the conduction band CB and the valence band VB, Figure 1.1 shows the formation of these bands as a function of the inter-atomic distance.

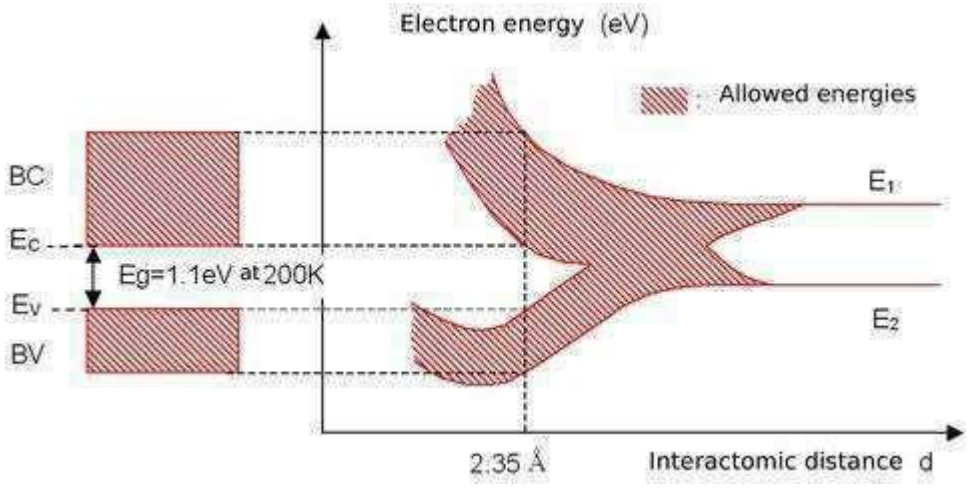


Figure.1.1. Formation of energy bands for electrons in a silicon crystal

In a silicon crystal, two continuous energy bands exist (CB and VB), separated by a forbidden band, which is not accessible for electrons. This forbidden region is called the gap and its width Eg is a characteristic of the material. The lowest energy level of the conduction band is denoted E_C and the highest energy level of the valence band is called E_V so that we have the relationship $E_g=E_C-E_V$. The conduction and valence bands CB and VB represent the energies accessible to electrons, or the energies of the states *potentially* occupied by electrons: they do not provide any information about the *effective* occupation of the energy states by electrons.

Insulators: The valence band of insulators remains full of electrons. The conduction band of those materials remains empty. The forbidden energy gap between the conduction band and the valence band is widest. The difference is more than 10ev. Crossing the forbidden energy gap from valence band to conduction band large amount of energy is needed.

Conductors: In conductors, as shown in figure 1.2(c) shows the energy band of good conductor or metal. The valence band and the conduction band is attached here on overlap each other. There is no forbidden energy gap here so $E_g=0$. At absolute zero temperature large number of electrons remains in the conduction band. The resistance of conductor is very low; large number charge carriers are available here. So, the electricity can pass easily through the conductors.

Semiconductors: Semiconductors are those materials whose electrical conductivity is between conductors and insulators. The forbidden energy gap of a semiconductor is nearly same as insulator. The energy gap is narrower. The value of E_g =1.1eV for silicon crystal and E_g =0.7eV for germanium at 0k temperature. It can easily overcome due to thermal agitation or light. A semiconductor remains partially full valence band and partially full conduction band at the room temperature. The conduction band remains full empty of a semiconductor where the valence band remains full of electrons at absolute zero temperature. So, silicon and germanium are insulators at absolute zero temperature. On the other hand with the increasing of temperature the electrical conductivity of semiconductors increases.

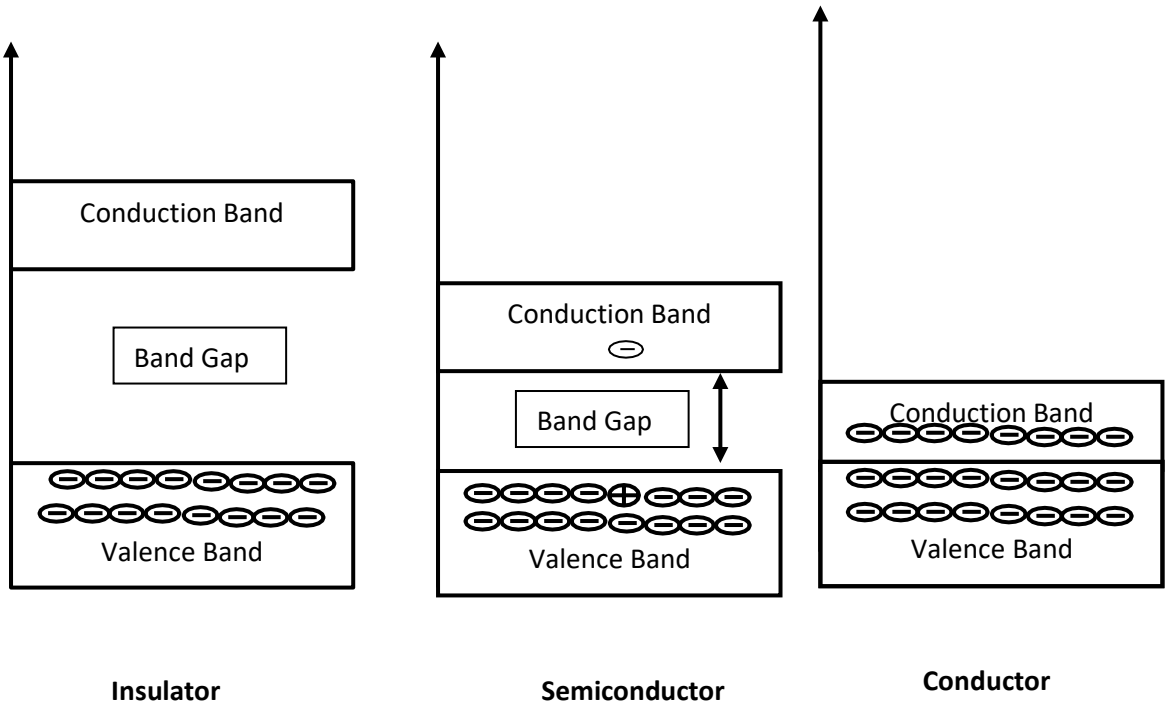


Figure.1.2. Energy band diagram for insulator, semiconductor and conductors

1.3. Concept of Holes

When an electron leaves its position in the crystal lattice, there is a space left behind that is positively charged. This lack of an electron is called a **positive hole**. This hole may be filled by an electron from a neighboring atom, which will in turn leave a hole there. Although it is technically the electron that moves, the effect is the same as if it was the hole that moved through the crystal lattice. The hole can then be thought of as a positive charge carrier.

1.4. Intrinsic Semiconductor: A semiconductor material in its purest form is known as an intrinsic semiconductor. An intrinsic semiconductor behaves as an insulator at 0 K but acts as a conductor at 300 K (room temperature). At room temperatures due to the thermal generation of electron-hole pairs, free electrons & holes are generated in equal numbers, these mobile charges help in the conduction of current in an intrinsic semiconductor. Since electron-hole pairs that are responsible for conduction of current in an intrinsic semiconductor are internal to the semiconductor crystal, the material is known as an intrinsic semiconductor.

1.5. Doping:

At low temperatures, intrinsic semiconductors are insulators since the number of electrons and holes is diminished. At absolute zero, an intrinsic semiconductor would have no electrons in the conduction band. However, the most important semiconductors are of the extrinsic type, where some impurity (another element) has been intentionally added in the solid to increase the conductivity. The conduction in a semiconductor can be changed via doping. Doping is the introduction of foreign atoms such as B or As in Si.

1.6. Extrinsic Semiconductor: An extrinsic semiconductor is obtained by doping an intrinsic Semiconductor with trivalent or pentavalent impurity atoms. Depending upon the valency of the impurity atoms added we obtain either p-type or n-type extrinsic semiconductor. The concentration of dopant ranges from 10^{13} /cm^3 to 10^{17}/cm^3. Since the number of pure atoms is usually about 10^{23}/cm^3, it is clear that the dopant concentrations are about 1 ppm to 0.1 ppb.

1.6.1 N-Type semiconductor:

Doping can produce two types of semiconductors depending upon the element added. If the element used for doping has at least one more valence electron than the host semiconductor i.e. pentavalent, then an **n-type** (negative type) **semiconductor** is created. Silicon is a group IV element on the periodic chart and has four electrons in its outermost shell. When silicon is doped with arsenic (As), a group V element, the arsenic atoms replace silicon atoms at a small number of points on the crystal lattice. Since arsenic has 5 electrons in its outer shell, it adds a loosely-bound "extra" electron to the crystal. This extra electron (often called a "donor" electron) is easily excited into the conduction band

as a freely roaming current carrier. Doping with donors: N_D (donor concentration) gives an n-type semiconductor. Thus the density of free electrons n_n is larger than the density of free holes p_n in an n-type material.

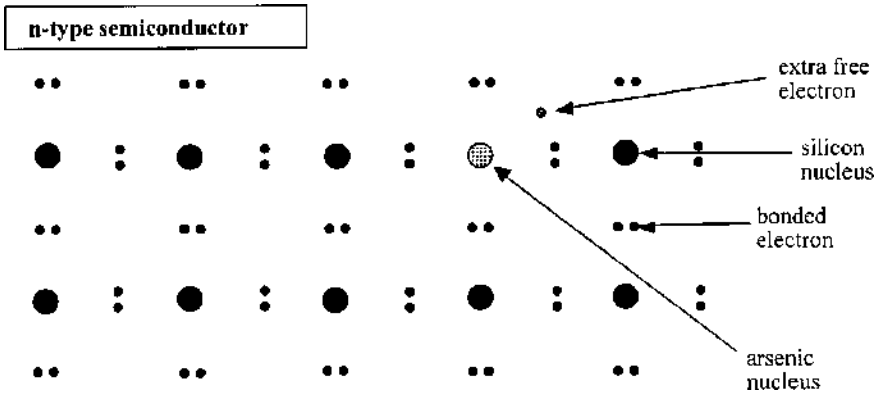


Figure.1.2. N-Type semiconductor

1.6.2 P-Type semiconductor:

If the semiconductor is doped with an element having at least one less electron than the host material i.e. trivalent, then a **p-type** (positive type) **semiconductor** is formed. If Silicon is doped with an element from group III of the periodic table, such as gallium (Ga), the impurity has only three electrons in its outermost shell so there is a deficiency of one electron at every point where a gallium atom replaces a silicon atom. This is called an "acceptor site" since the gallium would very much like to have a fourth electron to complete its bonds. The gallium often "steals" an electron from a neighboring silicon atom leaving a "hole" or empty state in the valence band of the silicon. This "hole" is free to roam around in the valence band and effectively acts as a positive charge carrier. Doping with acceptors: N_A (acceptor concentration) gives a p-type material. The density of free holes p_p is larger than the density of free electrons n_p

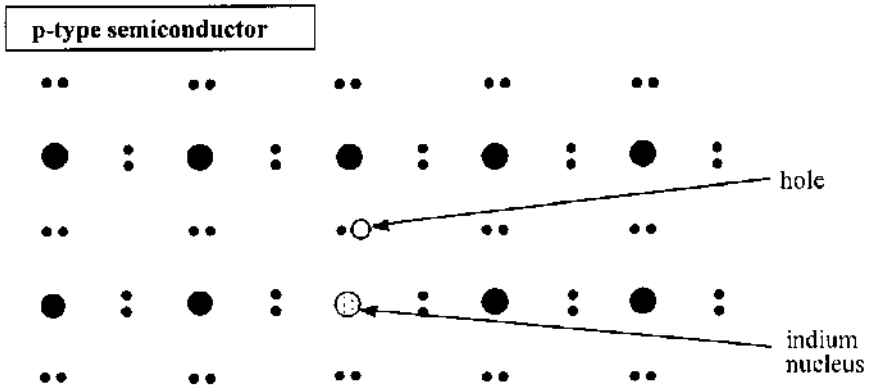


Figure.1.3. P-Type semiconductor

1.7. Charge carriers in semiconductor

For the intrinsic material, since electrons and holes are always created in pairs,

$$n = p = n_i$$

where n_i is the symbol for "intrinsic carrier concentration." (same density of free electrons and holes in an intrinsic semiconductor).

N-Type Semiconductor: As the activation energy is low, at room temperature almost all of the donor atoms included in the crystal will give an electron to the conduction band. So if N_D is the donor concentration, for an n-type material at equilibrium: $n_0 \approx N_D$ [1 /cm^3]

P-Type Semiconductor: The activation energy is low, at room temperature almost all of the acceptor atoms included in the crystal will accept an electron from the valence band. So if NA is the acceptor concentration, for a p-type material at equilibrium: $p_0 \approx N_A$ [1/ cm^3]

1.8. Law of Mass Action:

For both intrinsic and extrinsic materials, at equilibrium:

$$n_0 p_0 = n^2$$

The extrinsic n-type semiconductor: $\begin{cases} n_n = N_D \\ p_n = \dfrac{n_i^2}{N_D} \end{cases}$

The extrinsic p-type semiconductor $\begin{cases} n_p = \dfrac{n_i^2}{N_A} \\ p_p = N_A \end{cases}$

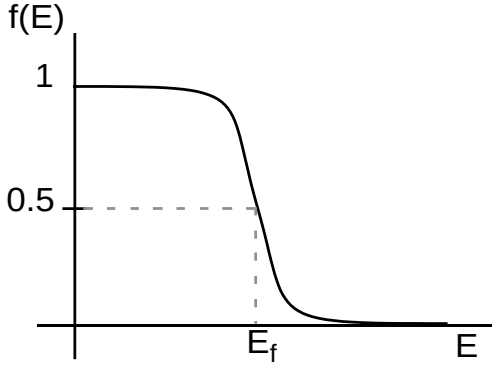
With *n, p* respectively the electron and hole density; $N_{D,A}$ respectively the donor and acceptor doping density (concentration).

1.9. The Fermi-Dirac Distribution Function and Fermi Level

The Fermi-Dirac distribution function, also called Fermi function, provides the probability of occupancy of energy levels by Fermions. Fermions are half-integer spin particles, which obey the Pauli Exclusion Principle.

Mathematically the probability of finding an electron in the energy state E at the temperature T is expressed as

$$f(E) = \frac{1}{1+\left(\frac{E-E_f}{T}\right)}$$



k = 8.62×10^{-5} [eV/K] or 1.38×10^{-23} JK^{-1} is the Boltzmann constant

T is the absolute temperature

E_f is the Fermi level or the Fermi energy

f(E) is the probability that a level with energy E will be filled by an electron

The quantity EF is called the Fermi level, and it represents an important quantity in the analysis of semiconductor behaviour. It is determined as the energy point where the probability of occupancy by an electron is exactly 50%, or 0.5.For an energy E = E_F the occupation probability is

$$f(E_F) = \left[1+\exp\left[(E_F - E_F)/kT\right]\right]^{-1} = \frac{1}{1+1} = \frac{1}{2}$$

1.10. Fermi-Dirac Distribution Function for Intrinsic and Extrinsic Semiconductor

- The F-D distribution function can be used to calculate the electron and hole concentrations in semiconductors, if the densities of available states in the conduction and valence bands are known.
- In equilibrium, the concentration of electrons in the conduction band can be given by

$n_0 = \int_{E_c}^{\infty} f(E)N(E)dE$

where N(E)dE is the density of available states/cm3 in the energy range dE. $N_c = 2\left(\frac{2\pi m^* T}{h^2}\right)^{3/2}$

$$n_0 = N_c f(E_c) = N_c e^{-(Ec-Ef)/T}$$

Where $N_c = 2\left(\frac{2\pi m^* T}{h^2}\right)^{3/2}$

$$p_0 = N_v f(1-E_v) = N_v e^{-(Ef-Ev)/T}$$

where N_v is the effective density of states located at the valence band edge E_v.

- Note: the only terms separating the expressions for N_c and N_v are the effective masses of electrons (m_n^*) and holes (m_h^*) respectively, and since , hence, N_c N_v.
- Thus, as (E_f – Ev)decreases, i.e., the Fermi level moves closer to the valence band edge, and the hole concentration increases.
- These equations for n_0 and P_0 are valid in equilibrium, irrespective of the material being intrinsic or doped.
- For intrinsic material E_f lies at an intrinsic level E_i (very near the middle of the band gap), and the intrinsic electron and hole concentrations are given by

$n_i = N_c e^{-(E_c-E)/T}$ and $p_i = N_v e^{-(E-E_v)/T}$

- Note: At equilibrium, the product n_0p_0 is a constant for a particular material and temperature, even though the doping is varied,

  i.e. $n_0p_0 = n^2 = N_cN_v e^{-E_g/T}$
- This equation gives an expression for the intrinsic carrier concentration n_i as a function of N_c, N_v, and temperature:

$$n = \sqrt{N_cN_v}\ e^{-E_g/2T}$$

These relations are extremely important, and are frequently used for calculations.

- Note: if N_c were to be equal to N_v, then E_i would have been exactly at mid gap

  i.e., $E_c - E_i = E_i - E_v = E_g/2$
- However, since N_c, N_v , E_i is displaced slightly from mid gap (more for GaAs than that for Si).
- Alternate expressions for n_0 and p_0:

  $n_0 = n_i e^{(E_f - E)/T}$ and $p_0 = n_i e^{(E - E_f)/T}$

  Note: the electron concentration is equal to n_i when E_f is at E_i, and n0 increases exponentially as E_f moves away from E_i towards the conduction band.
- Similarly, the hole concentration p_0 varies from n_i to larger values as E_f moves from E_i towards the valence band.

1.11. Energy band for intrinsic and Extrinsic Semiconductors

Free electrons have energies in an allowed energy band higher in energy than the band gap, the conduction band E_c, whilst free holes have energies in an allowed energy band lower in energy than the band gap, the valence band E_v.

The amount of electrons available at each energy value is determined by the density of states *g(E)* and the Fermi-Dirac distribution function *f(E)* as illustrated in Figure 1.4. *g(E)* gives the distribution of energy levels (states) as a function of energy. Note that *g(E)*=0 in the bandgap (no energy levels). *f(E)* gives the probability of finding an electron at energy *E*. Thus 1-*f(E)* gives the probability of finding a hole.

Intrinsic Semiconductor: In an intrinsic semiconductor, n = p. n = p implies that there is an equal chance of finding an electron at the conduction band edge as there is of finding a hole at the valence band edge:

Remember the relationship between the position of the Fermi level E_F and the density of carriers in the semiconductor (given by the Fermi-Dirac or Maxwell-Boltzman distribution functions):

$$p = N_v e^{(E_v - E_F)/kT} \text{ and } p_i = N_v e^{(E_v - E_i)/kT}$$

$$n = N_c e^{(E_F - E_c)/kT} \text{ and } n_i = N_c e^{(E_i - E_c)/kT}$$

with E_i the intrinsic level, N_c the effective density of states in the conduction band and N_v the effective density of states in the valence band. The intrinsic level E_i is an energy position within the forbidden gap that is determined by the intrinsic carrier concentration.

Fermi level for an intrinsic semiconductor E_{Fi}: Since at room temperature kT is significantly lower than the energy gap, this level is located near the middle of the forbidden band :

Electron concentration = Hole concentration

$$N_c \exp\left[\frac{-(E_c - E_{Fi})}{kT}\right] = N_v \exp\left[\frac{-(E_{Fi} - E_v)}{kT}\right]$$

$$E_{Fi} = \frac{1}{2}(E_c + E_v) + \frac{1}{2} kT \ln\left(\frac{N_v}{N_c}\right)$$

$$N_c = 2\left(\frac{2\pi m_n^* kT}{h^2}\right)^{3/2}$$

$$E_{Fi} = \frac{1}{2}(E_c + E_v) + \frac{3}{4} kT \ln\left(\frac{m_p^*}{m_n^*}\right)$$

$$\frac{1}{2}(E_c + E_v) = E_{midgap} \Longrightarrow \boxed{E_{Fi} - E_{midgap} = \frac{3}{4} kT \ln\left(\frac{m_p^*}{m_n^*}\right)}$$

Even in intrinsic semiconductor, Fermi level is not exactly at centre between conduction and valence bands.

The Fermi level for Extrinsic semiconductor

Now let us examine the Fermi energy level of extrinsic semiconductor. If we recall our discussion of Fermi levels, the Fermi energy level in the intrinsic semiconductor lies approximately halfway in between conduction and valance bands ($E_{fi}=(E_V+E_c)/2$).

Let us re-write the expression

$$n = N_C \exp\left\{-\frac{E_c - E_F}{kT}\right\} \text{ as } n = N_C \exp\left\{-\frac{E_c - E_{Fi}}{kT}\right\}\exp\left\{\frac{E_F - E_{Fi}}{kT}\right\}$$

which ultimately can be represented as

$$n = n_i \exp\left\{\frac{E_F - E_{Fi}}{kT}\right\}.....;$$

$$\Rightarrow E_F - E_{Fi} = kT\ln\left(\frac{n}{n_i}\right).$$

$$E_C - E_F = kT\ln\left(\frac{N_C}{N_D}\right)....$$

Where E_F and E_{Fi} stands for Fermi levels of *extrinsic* and *intrinsic* semiconductors respectively.

Fermi level in n type semiconductor $(n = n_0 \approx N_D)$

$$E_F - E_i \cong kT\left(\frac{N_D}{N_i}\right).$$

and for p- type it is

$$E_i - E_F \cong kT\left(\frac{N_A}{N_i}\right).$$

This suggests that in n-type semiconductors, Fermi level (E_F) is higher than E_i and close to the conduction band. Similarly, in p-type it moves down towards the valance band.

Fermi level in n-type semiconductor

In n-type semiconductor pentavalent impurity is added. Each pentavalent impurity donates a free electron. The addition of pentavalent impurity creates large number of free electrons in the conduction band.

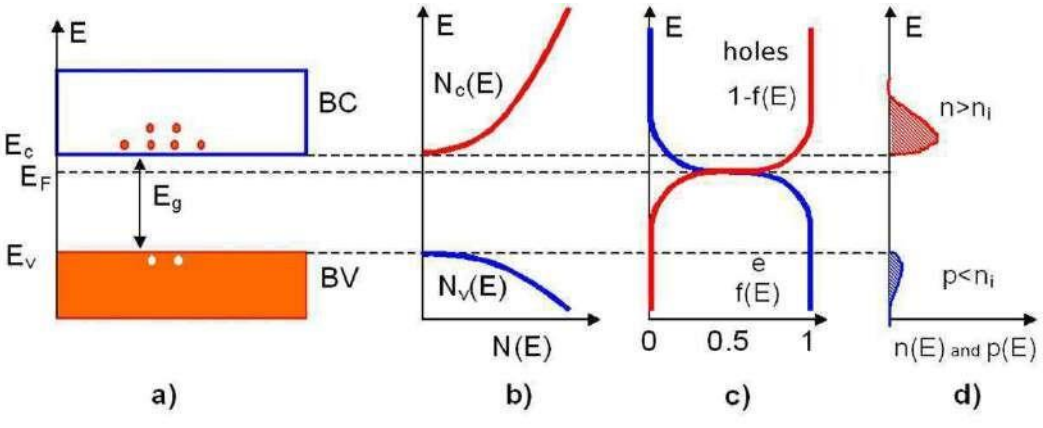


Figure.1.4. Fermi level in N-Type semi conductor

At room temperature, the number of electrons in the conduction band is greater than the number of holes in the valence band. Hence, the probability of occupation of energy levels by the electrons in the conduction band is greater than the probability of occupation of energy levels by the holes in the valence band. This probability of occupation of energy levels is represented in terms of Fermi level. Therefore, the Fermi level in the n-type semiconductor lies close to the conduction band.

The Fermi level for n-type semiconductor is given as

$$E_f = E_c - kT \log \frac{N_c}{N_D}$$

Where E_F is the fermi level.

E_C is the conduction band.

K is the Boltzmann constant.

T is the absolute temperature.

N_C is the effective density of states in the conduction band.

N_D is the concentration of donar atoms.

Fermi level in p-type semiconductor

In p-type semiconductor trivalent impurity is added. Each trivalent impurity creates a hole in the valence band and ready to accept an electron. The addition of trivalent impurity creates large number of holes in the valence band. At room temperature, the number of holes in the valence band is greater than the number of electrons in the conduction band. Hence, the probability of occupation of energy levels by the holes in the valence band is greater than the probability of occupation of energy levels by the electrons in the conduction band. This probability of occupation of energy levels is represented in terms of Fermi level. Therefore, the Fermi level in the p-type semiconductor lies close to the valence band.

The Fermi level for p-type semiconductor is given as

$$E_f = E_v + kT \log \frac{N_v}{N_A}$$ Where N_v is the effective density of states in the valence band.

N_A is the concentration of acceptor atoms

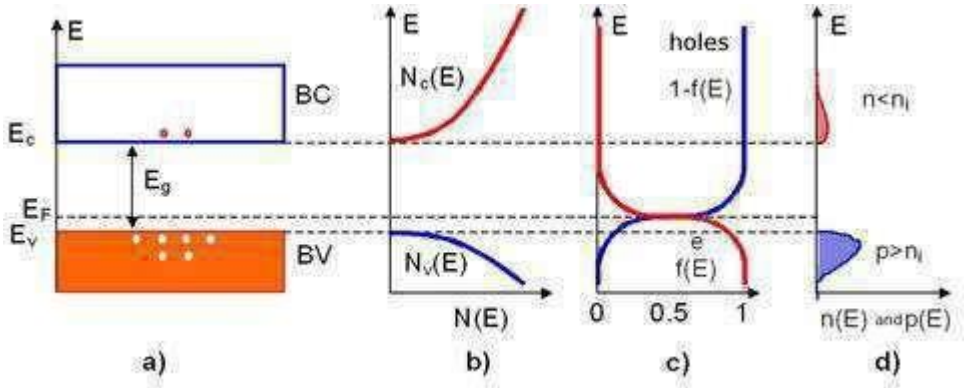


Figure.1.5. Fermi level in P-Type semiconductor

1.9 Drift and diffusion currents:

The flow of charge current through a semiconductor material is of two types namely drift & diffusion. The net current that flows through a (PN junction diode) semiconductor material has two components

Drift current

Diffusion current

1.9.1. Drift current: When an electric field is applied across the semiconductor material, the charge carriers attain a certain drift velocity V_d, which is equal to the product of the mobility of the charge carriers and the applied Electric Field intensity E ;

Drift velocity V_d = mobility of the charge carriers X Applied Electric field intensity.

Holes move towards the negative terminal of the battery and electrons move towards the positive terminal of the battery. This combined effect of movement of the charge carriers constitutes a current known as the drift current. Thus the drift current is defined as the flow of electric current due to the motion of the charge carriers under the influence of an external electric field. Drift current due to the charge carriers such as free electrons and holes are the current passing through a square centimeter perpendicular to the direction of flow.

1. Drift current density J_n , due to free electrons is given by $J_n = q\ n\ \mu_n\ E\ A / cm^2$
2.Drift current density J_P, due to holes is given by $J_P = q\ p\ \mu_p\ E\ A / cm^2$

Where, n - Number of free electrons per cubic centimeter.
P - Number of holes per cubic centimeter
μ_n – Mobility of electrons in cm^2 / Vs
μ_p – Mobility of holes in cm^2 / Vs
E – Applied Electric filed Intensity in V /cm
q – Charge of an electron = 1.6×10^{-19} coulomb.

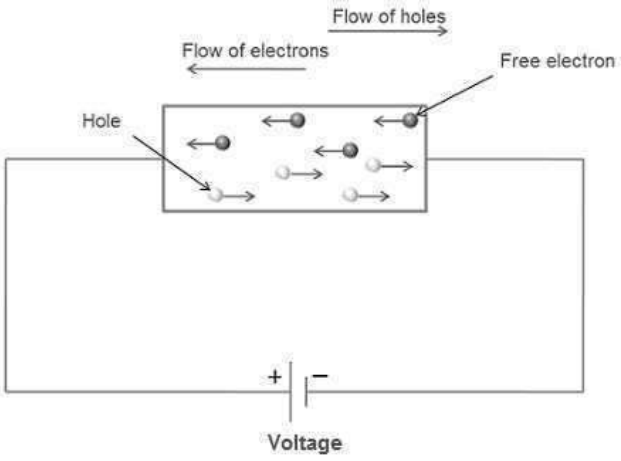


Figure 1.6 Drift mechanism

In a homogeneously doped semiconductor or a semiconductor with a constant carrier density, applying an electric field will cause drift currents to flow. Drift current can be carried by both electrons and holes.

Drift current in a semiconductor is given by:

$$I_{tot} = \sigma_{tot} AE = eA(n\mu_n + p\mu_p)E$$

With A the cross sectional area perpendicular to the current flow, E is the applied electric field.

1.9.2 Diffusion current:

It is possible for an electric current to flow in a semiconductor even in the absence of the applied voltage provided a concentration gradient exists in the material. A concentration gradient exists if the number of either elements or holes is greater in one region of a semiconductor as compared to the rest of the Region. In a semiconductor material the change carriers have the tendency to move from the region of higher concentration to that of lower concentration of the same type of charge carriers. Thus the movement of charge carriers takes place resulting in a current called diffusion current.

Hole density gradients cause hole diffusion currents, electron density gradients cause electron diffusion currents and gradients in both carrier types will cause diffusion of both, creating a total diffusion current of:

$$I_{tot} = eA\left(D_n \frac{dn}{dx} - D_p \frac{dp}{dx}\right)$$

With $D_{n,p}$ the diffusion constant of electrons respectively holes, x is the direction of carrier propagation. The Einstein equation gives the relationship between the diffusion constant and the mobility of the carrier:

$$\frac{D}{\mu} = \frac{kT}{e}$$ with, k the Boltzman constant, T the temperature in Kelvin.

In the general case where both concentration gradients and electric fields are present the total current is the sum of both drift and diffusion currents:

$$I_{tot} = eA\left(n\mu_n E + p\mu_p E + D_n \frac{dn}{dx} - D_p \frac{dp}{dx} \right)$$

This equation is normally referred to as the drift-diffusion equation of carriers and is the basic equation that describes carrier movement in semiconductor devices.

1.10. Hall Effect:

When a magnetic field is applied to a current carrying conductor in a direction perpendicular to that of the flow of current, a potential difference or transverse electric field is created across a conductor. This phenomenon is known as Hall Effect.

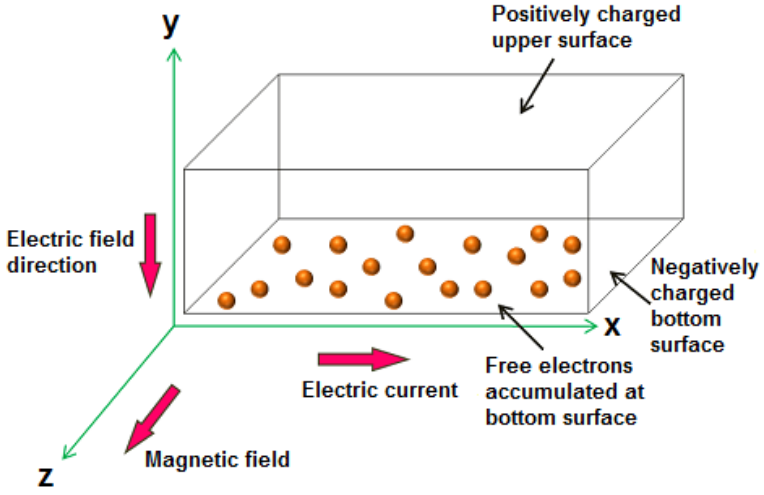


Figure.1.7. Hall effect in conductor

If a magnetic field is applied to this current carrying conductor or semiconductor in a direction perpendicular to that of the flow of current (that is z-direction), an electric field is produced in it that exerts force in the negative y direction (downwards). This phenomenon is known as Hall Effect. Hall Effect was named after American Physicist Edwin Hall, who discovered the phenomenon in 1879.

The electric field produced in the material pushes the charge carriers downwards. If the material is a conductor, the electric field pushes the free electrons downwards (that is in negative y-direction). As a result, a large number of charge carriers (free electrons) are accumulated at the bottom surface of the conductor.

Because of this large accumulation of negative charges (free electrons) at the bottom surface and deficiency of negative charges (free electrons) at the upper surface, the bottom surface is negatively charged and the upper surface is positively charged.

As a result, an electrical difference or potential difference develops between the upper surface and bottom surface of the conductor. This potential difference is known as Hall voltage. In a conductor, the electric field is produced due to the negatively charged free electrons. So the hall voltage produced in the conductor is negative.

1.11. PN junction Diode:

If a junction between P-type and N-type semiconductor material is created within a single crystal, in such a way that the crystalline structure is preserved across the junction, the result is a junction diode. Electrons from the N-region migrate across the junction into the P-region, filling holes as they go. This creates a net charge build-up around the junction positive in the N-region and negative in the P-region leading to an internal electric field as shown. Since the diode is a two-terminal device, the application of a voltage across its terminals leaves three possibilities:

- **No bias** (VD = 0 V),
- **Forward bias** (VD>0 V),
- **Reverse bias** (VD< 0 V).

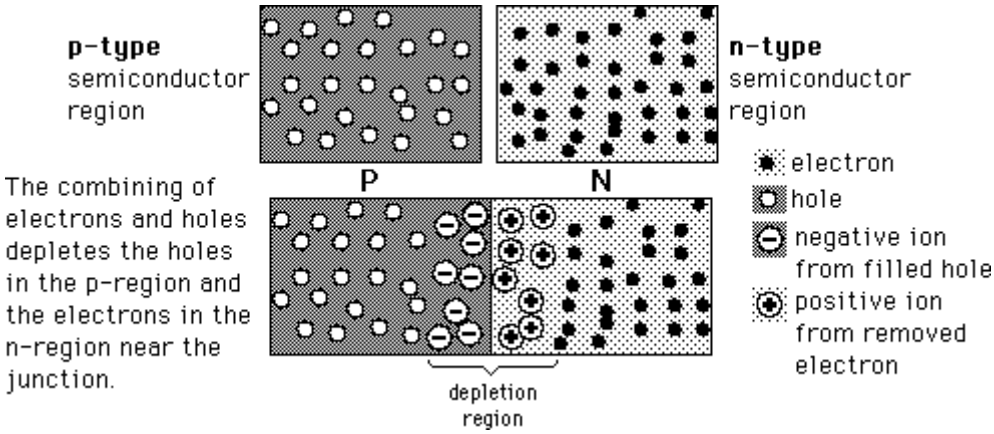


Figure.1.8. Formation of depletion region

1.11.1. Formation of Depletion Region:

At the instant of the PN junction formation free electrons near the junction diffuse across the junction into the P region and combine with holes. Filling a hole makes a negative ion and leaves behind a positive ion on the N side. These two layers of positive and negative charges form the depletion region, as the region near the junction is depleted of charge carriers. As electrons diffuse across the junction a point is reached where the negative charge repels any further diffusion of electrons. The depletion region now acts as a barrier.

1.11.2. Barrier Potential

The electric field formed in the depletion region acts as a barrier. External energy must be applied to get the electrons to move across the barrier of the electric field. The potential difference required to move the electrons through the electric field is called the barrier potential. Barrier potential of a PN junction depends on the type of semiconductor material, amount of doping and temperature. This is approximately 0.7V for silicon and 0.3V for germanium. Once the holes are filled, the junction region becomes devoid of charge carriers and thus acts as an insulator, preventing further current flow.

1.11.3. Energy Diagrams of PN Junction.

The valence band and conduction band in N-Type material are slightly lower than that of P-Type material.

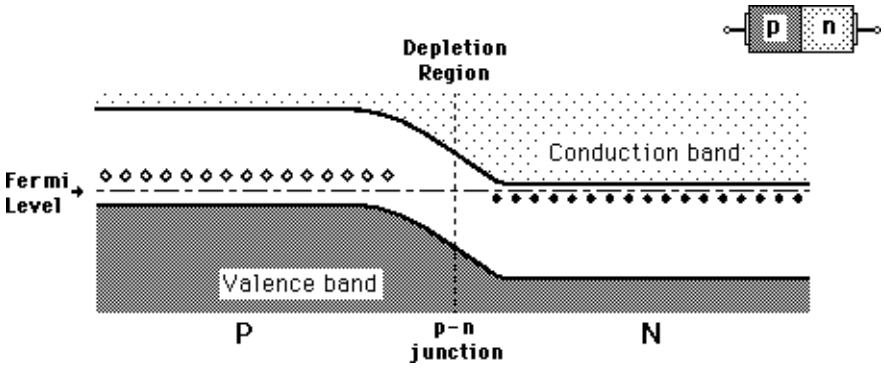


Figure.1.9. Energy diagram of PN junction

As diffusion occur the depletion region forms and the energy level of the N region conduction band drops, causing alignment of the top of the N region conduction band and the bottom of the P region conduction band. At this point the energy bands are at equilibrium as shown in figure 1.9. There is an energy gradient across the depletion region that N region electron must climb to get to the P region.

1.11.4. No Applied Bias (V_D =0 V)

The p-region has negative immobile ions and their corresponding holes as the majority carriers, while the n-region has positive immobile ions and their corresponding free electrons as the majority carriers. Thermally generated electron-hole pairs are also not shown for simplicity. In the equilibrium state no conduction takes place at the PN junction. The conduction of PN junction involves the majority charge carriers diffusion and minority charge carriers drift. Conduction of electrical current in PN junction physically involves in both conduction band and valence band. At zero voltage bias equilibrium condition, the minority concentration of holes and electrons will drift simply under the influence of incorporating electric field E. The diffusion of majority charge carriers have to cross the potential barrier VB of the PN junction formed as the effect of the depletion region.

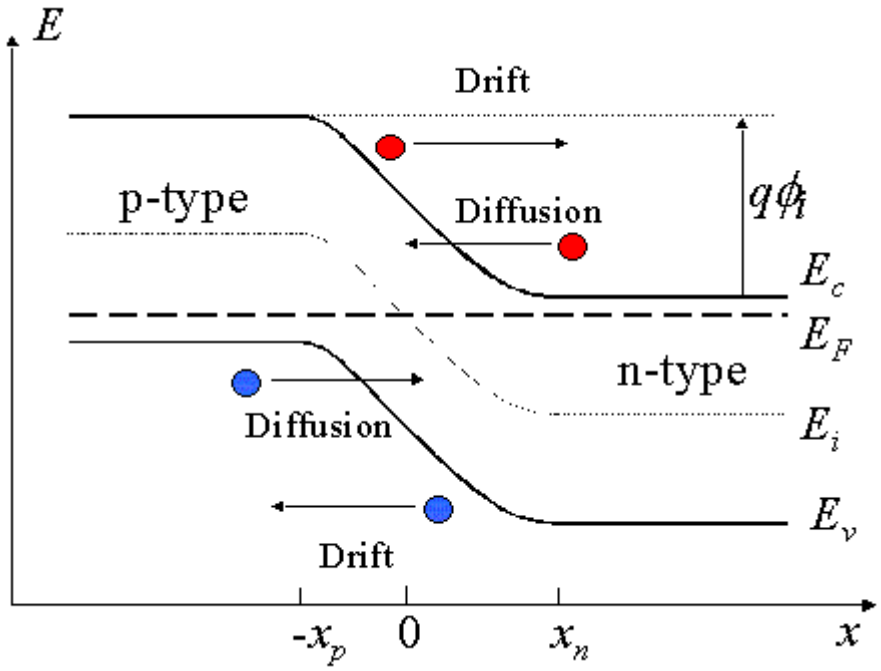


Figure.1.10.PN junction Energy diagram

At the instant of junction formation, the p-material has excess holes and the n- material has excess electrons and the depletion region does not exist. As soon as the p & n regions are formed, electrons on the n-side recombine with holes by crossing onto the p-side of the junction due to diffusion. Soon after recombination both the electrons & the holes disappear and leave behind immobile positive ions on the n-side and immobile negative ions on p-side of the junction as shown in Fig.1.6. This electric field created by the immobile positive & negative ions on either side of the junction prevents further diffusion of charges. Thus a depletion region is formed at the junction even under unbiased conditions as shown in Fig.1.10. Once the electric field and the potential barrier develop to sufficient level, migration of carriers across the junction stops. At this point the **p-n** junction is said to have attained "thermal equilibrium". An approximate idealized plot of the variation of the space charge density, the electric field and the electric potential along the device is shown in Fig 1.9.

1.11.4.1. Built in Potential

The existence of this double layer of charges on either side of the PN junction, potential barrier varies sharply within the depletion zone and the potential difference Vd, called the diffusion potential or built-in potential reach non-negligible values. Electrostatic potential is constant all over the crystal together with the space charge zone, because this potential takes into consideration not only the electric field but also the concentration of charge carriers. The built in potential due to the concentration of charge carriers compensates accurately for the electrostatic potential.

The built-in potential or diffusion potential is proportional to the difference of the Fermi energies of the two unbounded semiconductors:

$$_i = (1/q)*\{E_{Fp} - E_{Fn}\} = (kT/q) \ln \{[N_A N_D]/n_i^2\}$$

- Where E is the zero bias junction voltage
- (kT/q) the thermal voltage of 26mV at room temperature.
- N_A and N_B are the impurity concentrations of acceptor atoms and donor atoms
- n is the intrinsic concentration.

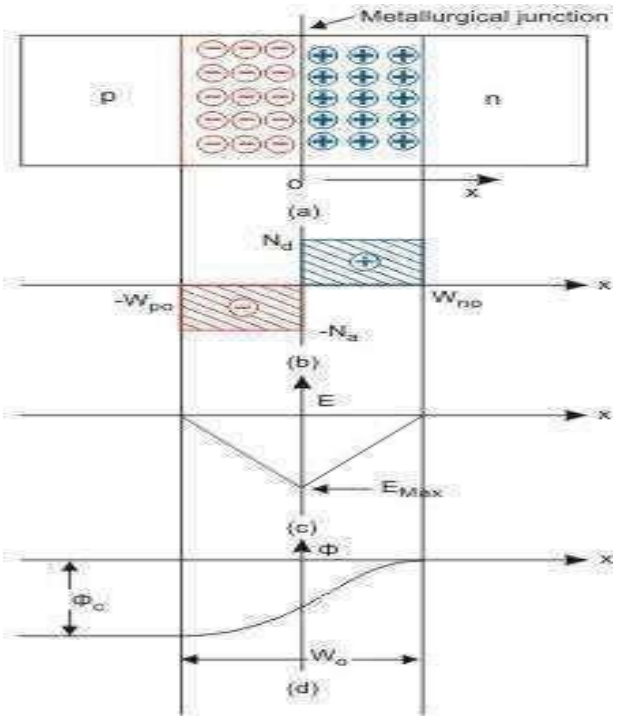


Figure.1.11. Space charge density, electric field and electric potential inside a p-n junction in thermal equilibrium; (a) schematic diagram; (b) space charge density; (c) electric field; (d) electric potential.

1.11.5. Reverse-Bias Condition (V_D< 0 V)

When a p-n junction diode is reverse biased (ie. anode is at a lower potential than the cathode) a very small reverse current flows through the junction due to a small number of temperature dependent minority charge carriers (electrons in p-region & holes in n-region). This minority current or leakage current is also known as the reverse saturation current & is temperature dependent. The leakage current which has a very small value (1 or 2 μA) doubles itself for every 10^0 C rise in temperature. The diode therefore offers very high resistance (1 to 2 Mohm). This means that the diode acts as an open switch under reverse biased conditions. The battery connection is such that majority carriers in both p and n regions are pulled away from the junction. Thus both the depletion width and the potential barrier increase under reverse bias conditions.

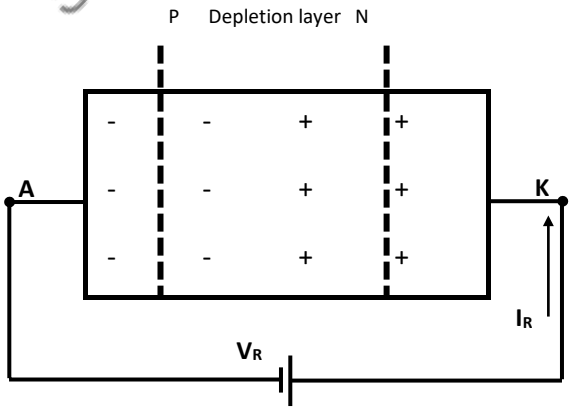


Figure1.12. Reverse-biased p-n junction

This reverse current flow until the reverse voltage is equal to the junction breakdown voltage. Beyond breakdown voltage, there is a drastic increase in the reverse current which is explained using the avalanche breakdown phenomenon. At voltages beyond V_{BD}, minority carriers (electrons) on the p-side gain sufficiently high velocities to knock out valence electrons from the semiconductor atoms. This is a cumulative effect and is known as ionization due to collision. A large number of charges are thus available to constitute a large reverse current. If left uncontrolled, this reverse current can cause physical breakdown of the junction. A p-n junction diode under reverse biased condition is therefore operated well within its breakdown voltage.

1.11.6. Forward-Bias Condition (V_D>0 V)

Figure 1.11 shows a p-n junction diode under forward biased condition (ie. anode is at a higher potential than the cathode). The battery polarity is such that majority carriers in both p & n regions are pushed towards the junction. Since electrons & holes enter the depletion region, it causes a reduction in the depletion width & hence height of

the potential barrier. The reduced potential barrier allows a few high- energy electrons on the n-side to cross the junction on to the p-side and constitute a small forward current. As the magnitude of forward bias voltage is increased the depletion width further reduces & thereby further increases the forward current. The depletion width & the potential barrier reduce to almost zero when the p-n junction is forward biased by a voltage greater than the cut-in voltage V (0.7 V for Silicon diode & 0.3 V for Germanium diode). At voltages greater than V the p-n junction diode acts like a closed switch and a heavy current starts flowing. At voltages greater than$V$, the p-n junction diode acts like a closed switch and a heavy current starts flowing. The thermally generated electron-hole pairs present in both p and n regions & the minority carriers also move in the same direction as majority carriers, i.e. they also add to the forward current.

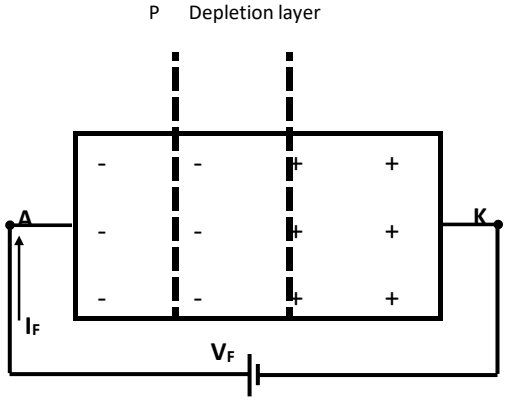


Figure.1.13. Forward-biased p-n junction

When the forward bias voltage $V_f = 0$, the forward current I_f is also equal to 0. When the forward bias voltage is increased, current through the diode gradually increases because some high-energy electrons start crossing the junction. Any further increase in V_f causes an increase in forward current due to reduction in depletion width & potential barrier. When $V_f = V$, the depletion width is zero & potential barrier is also zero. Now a large current starts flowing through the diode. Thus beyond V the diode acts as a closed switch and offers very low resistance resulting in a rapid rise in current.

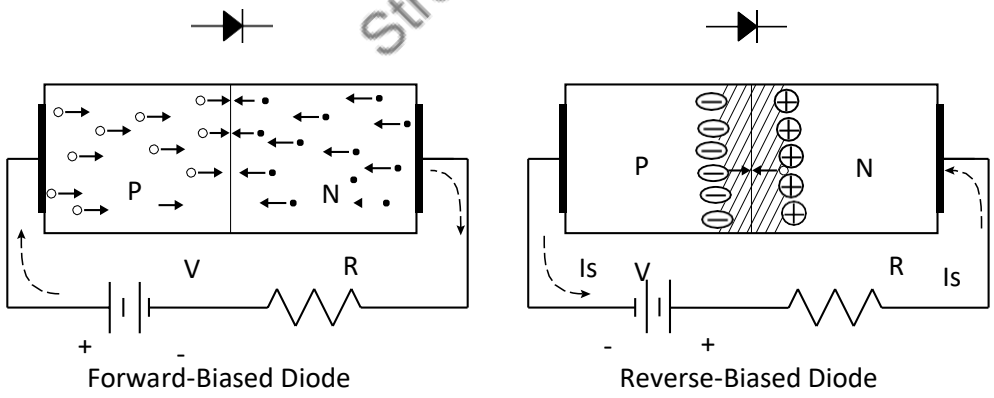


Figure.1.14. Biasing circuit of PN junction diode

1.12. VI Characteristics of PN Diode

When the P-type material is at a more positive voltage than the N-type material, the diode is said to be 'forward-biased'; this corresponds to V > 0 in Fig.1.9 When the P-type material is more negative than the N-type material, the diode is said to be 'reverse-biased'; this corresponds to V < 0 in Fig.1.15.

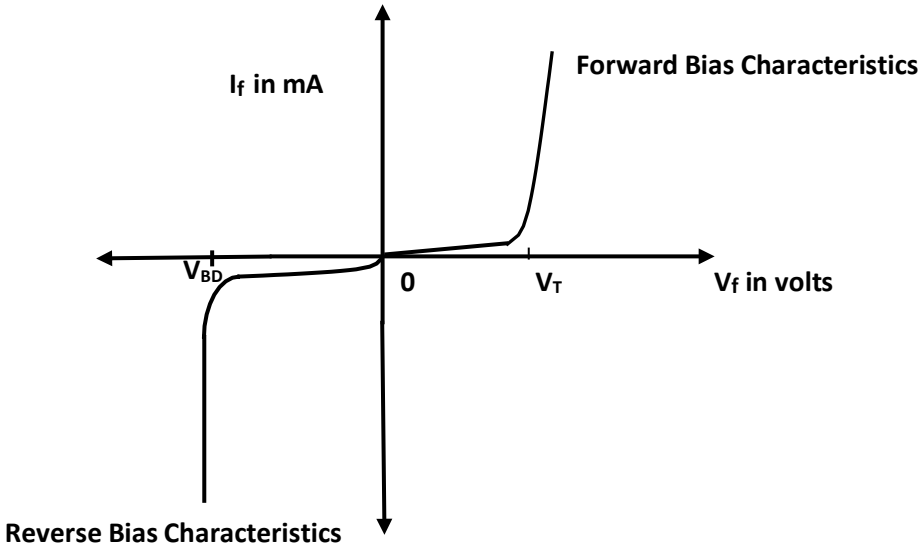


Figure.1.15.V-I Characteristics of PN

Breakdown Mechanism:

1) **Zener effect**: when $V_Z < 5$ V

- As electric field increases, covalent bonds begin to break: new hole-electron pairs are created
- Electrons are swept into n side and holes into p side
- At $\boldsymbol{V=V_Z}$ very large number of carriers are generated and large reverse current appears
- We can control over the value of reverse current
- Voltage is capped at $\boldsymbol{V=V_Z}$

2) **Avalanche effect**: when $Vz > 7$ V

- Ionizing collision: under electric field minority charge carriers (electrons in p side and holes in n side) collide with atoms and break covalent bonds
- Resulting carriers have high energy to cause more carriers to be liberated in further ionizing collision
- Process keeps repeating as avalanche
- We can control over the value of reverse current
- Voltage is capped at $\boldsymbol{V=V_Z}$

1.13. Temperature dependence of V-I characteristics:

PN junction diode parameters like reverse saturation current, bias current, reverse breakdown voltage and barrier voltage are dependent on temperature. Mathematically diode current is given by

$$I = I_S\,(e^{eV/nkT} - 1)$$

where I_S is the 'reverse saturation current', e is the electron charge, V is the voltage across the junction, n is an empirical constant between 1 and 2, k is Boltzmann's constant, and T is the junction temperature in kelvin.

Rise in temperature generates more electron-hole pair thus conductivity increases and thus increases in current Increase in reverse saturation current with temperature offsets the effect of rise in temperature Reverse saturation current (I_S) of diode increases with increase in the temperature the rise is 7%/ºC for both germanium and silicon and approximately doubles for every 10ºC rise in temperature. Thus if we kept the voltage constant, as we increase temperature the current increases. Barrier voltage is also dependent on temperature it decreases by 2mV/ºC for germanium and silicon. Reverse breakdown voltage (V_R) also increases as we increase the temperature.

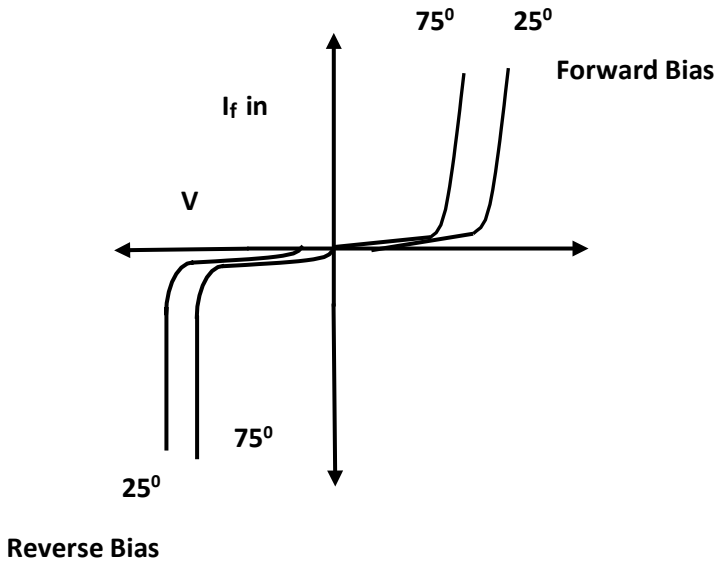


Figure.1.16. Effect of temperature on VI characteristics of Diode

1.14. Diode Resistance:

A p-n junction diode allows electric current in one direction and blocks electric current in another direction. It allows electric current when it is forward biased and blocks electric current when it is reverse biased. However, no diode allows electric current completely even in forward biased condition.

The depletion region present in a diode acts like barrier to electric current. Hence, it offers resistance to the electric current. Also, the atoms present in the diode provide some resistance to the electric current.

When charge carriers (free electrons and holes) flowing through the diode collides with atoms, they lose energy in the form of heat. Thus, depletion region and atoms offer resistance to the electric current.

When forward biased voltage is applied to the p-n junction diode, the width of depletion region decreases. However, the depletion region cannot be completely vanished. There exists a thin depletion region or depletion layer in the forward biased diode. Therefore, a thin depletion region and atoms in the diode offer some resistance to electric current. This resistance is called forward resistance.

When the diode is reversed biased, the width of depletion region increases. As a result, a large number of charge carriers (free electrons and holes) flowing through the diode will be blocked by the depletion region.

In a reverse biased diode, only a small amount of electric current flows. The minority carriers present in the diode carry this electric current. Thus, reverse biased diode offer large resistance to the electric current. This resistance is called reverse resistance.

The two types of resistance takes place in the p-n junction diode are:

1. Forward resistance
2. Reverse resistance

1.14.1. Forward resistance

Forward resistance is a resistance offered by the p-n junction diode when it is forward biased.

In a forward biased p-n junction diode, two type of resistance takes place based on the voltage applied.

The two types of resistance takes place in forward biased diode are

1. Static resistance or DC resistance
2. Dynamic resistance or AC resistance

1.14.2. Static resistance or DC resistance

When forward biased voltage is applied to a diode that is connected to a DC circuit, a DC or direct current flows through the diode. Direct current or electric current is nothing but the flow of charge carriers (free electrons or holes) through a conductor. In DC circuit, the charge carriers flow steadily in single direction or forward direction.

The resistance offered by a p-n junction diode when it is connected to a DC circuit is called static resistance.
Static resistance is also defined as the ratio of DC voltage applied across diode to the DC current or direct current flowing through the diode.
The resistance offered by the p-n junction diode under forward biased condition is denoted as Rf.
The resistance offered by the p-n junction diode under forward biased condition is denoted by Rf.

1.14.3. Dynamic resistance or AC resistance:

The dynamic resistance is the resistance offered by the p-n junction diode when AC voltage is applied.
When forward biased voltage is applied to a diode that is connected to AC circuit, an AC or alternating current flows though the diode.
In AC circuit, charge carriers or electric current does not flow in single direction. It flows in both forward and reverse direction.
Dynamic resistance is also defined as the ratio of change in voltage to the change in current. It is denoted as rf.
Dynamic resistance is also defined as the ratio of change in forward voltage to the change in forward current. It is denoted as rf.

1.14.4. Reverse resistance

Reverse resistance is the resistance offered by the p-n junction diode when it is reverse biased.
When reverse biased voltage is applied to the p-n junction diode, the width of depletion region increases. This depletion region acts as barrier to the electric current. Hence, a large amount of electric current is blocked by the depletion region. Thus, reverse biased diode offer large resistance to the electric current.
The resistance offered by the reverse biased p-n junction diode is very large compared to the forward biased diode. The reverse resistance is in the range of mega ohms (MΩ).

1.15. Diode junction capacitance:

There are two type of capacitance exist in diode: Transition and Diffusion capacitance.

1.15.1. Transition capacitances:

1. When P-N junction is reverse biased the depletion region act as an insulator or as a dielectric medium and the p-type an N-type region have low resistance and act as the plates.
2. Thus this P-N junction can be considered as a parallel plate capacitor.
3. This junction capacitance is called as space charge capacitance or transition capacitance and is denoted as C_T .
4. Since reverse bias causes the majority charge carriers to move away from the junction, so the thickness of the depletion region denoted as W increases with the increase in reverse bias voltage.
5. This incremental capacitance CT may be defined as
CT = dQ/dV,
Where dQ is the increase in charge and dV is the change or increase in voltage.
6. The depletion region increases with the increase in reverse bias potential the resulting transition capacitance decreases.
7. The formula for transition capacitance is given as CT = Aε/W, where A is the cross sectional area of the region, and W is the width.

1.15.2. Diffusion capacitance:

1. When the junction is forward biased, a capacitance comes into play, that is known as diffusion capacitance denoted as C_D. It is much greater than the transition capacitance.
2. During forward biased the potential barrier is reduced. The charge carriers move away from the junction and recombine.
3. The density of the charge carriers is high near the junction and reduces or decays as the distance increases.
4. Thus in this case charge is stored on both side of the junction and varies with the applied potential. So as per definition, change in charge with respect to applied voltage results in capacitance which here is called as diffusion capacitance.

5. The formula for diffusion capacitance is $C_D = \tau I_D / \eta V_T$, where τ is the mean life time of the charge carrier, ID is the diode current and V_T is the applied forward voltage, and η is generation recombination factor.
6. The diffusion capacitance is directly proportional to the diode current.7. In forward biased $C_D >> C_T$. And thus C_T can be neglected.

1.16. Zener Diode:

The Zener diode is also a P-N junction diode (silicon), the difference being that it has a sharp and well-defined break down under reverse biased condition. This breakdown voltage Vz is known as the Zener breakdown voltage. The Zener voltage can be precisely set by controlling doping level of P and N materials of the Zener during the manufacturing process.

Under forward bias condition, the Zener diode behaves like a normal Silicon rectifier diode. The Zener diode is operated only beyond reverse breakdown region. When the junction breaks down, current flows through it. This heavy current may be due to Zener breakdown or Avalanche break down phenomenon or both.

In the breakdown region, the voltage drop across the Zener diode is constant irrespective of current through it. This property of Zener diode makes it useful as a voltage-regulating device.

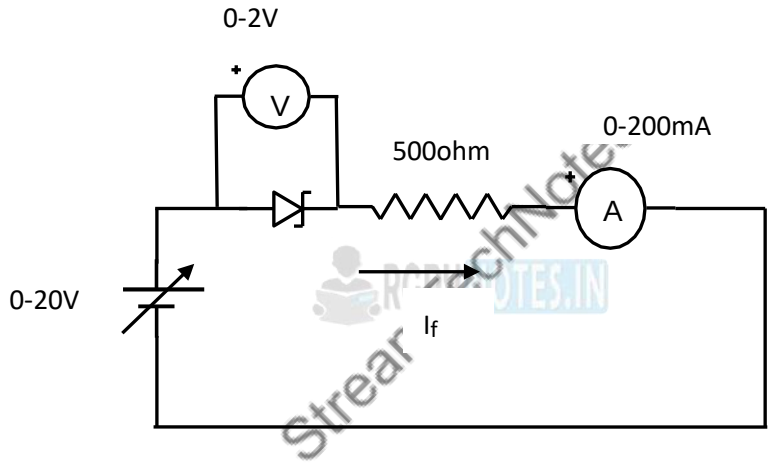


Figure.1.17. Forward biased connection of Zener diode

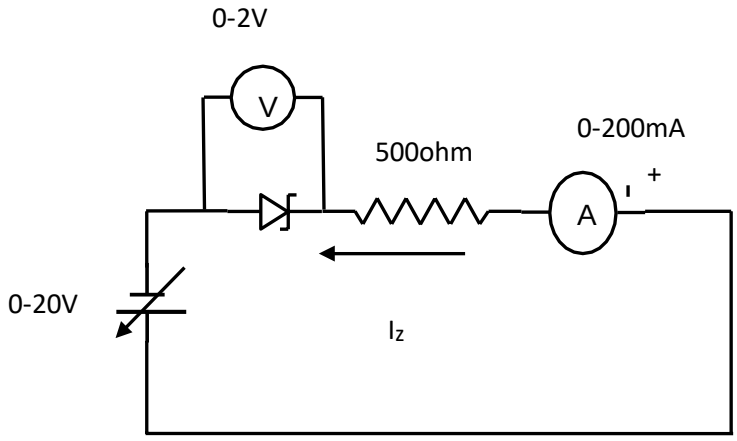


Figure.1.18. Reverse biased connection of Zener diode

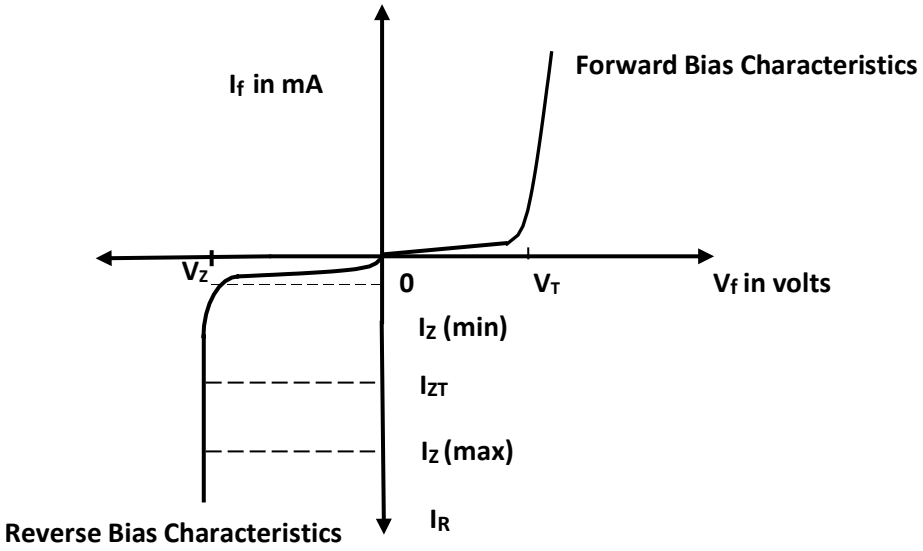


Figure.1.19.V-I Curve of zener

The circuit diagram to plot the VI characteristics of a zener diode is shown. Zener diode is a special diode with increased amounts of doping. This is to compensate for the damage that occurs in the case of a pn junction diode when the reverse bias exceeds the breakdown voltage and thereby current increases at a rapid rate.

Applying a positive potential to the anode and a negative potential to the cathode of the zener diode establishes a forward bias condition. The forward characteristic of the zener diode is same as that of a pn junction diode i.e. as the applied potential increases the current increases exponentially. Applying a negative potential to the anode and positive potential to the cathode reverse biases the zener diode.

As the reverse bias increases, the current increases rapidly in a direction opposite to that of the positive voltage region. Thus under reverse bias condition breakdown occurs. It occurs because there is a strong electric filed in the region of the junction that can disrupt the bonding forces within the atom and generate carriers. The breakdown voltage depends upon the amount of doping. For a heavily doped diode depletion layer will be thin and breakdown occurs at low reverse voltage and the breakdown voltage is sharp. Where as a lightly doped diode has a higher breakdown voltage.

The maximum reverse bias potential that can be applied before entering the zener region is called the Peak Inverse Voltage referred to as PIV rating or the Peak Reverse Voltage Rating (PRV rating).

1.17. Varactor Diode:

Varactor or varicap diodes are used mainly in radio frequency (RF) circuits to be able to provide a capacitance that can be varied by changing a voltage in an electronics circuit. This can be used for tuning circuits including radio frequency oscillators and filters.

Although both names: varactor and varicap diode are used, they are both the same form of diode. The name varactor meaning variable reactor, or reactance, and varicap meaning variable capacitance (vari-cap).

1.17.1. Applications of Varicap:

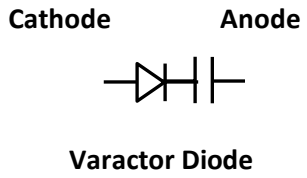
Varactor diodes are widely used within RF circuits. They provide a method of varying the capacitance within a circuit by the application of a control voltage. This gives them an almost unique capability and as a result varactor diodes are widely used within the RF industry. Although varactor diodes or varicap diodes can be used many different circuits, they find uses in two main areas:

- Voltage controlled oscillators, VCOs: Voltage controlled oscillators are used in many different circuits. One major area is for the oscillator within phased locked loops. In turn these can be used as FM demodulators or within frequency synthesizers. The varactor diode is a key component within the voltage controlled oscillator.
- RF filters: Using varactor diodes makes it possible to tune filters. Tracking filters may be needed in receiver front end circuits where they enable the filters to track the incoming received signal frequency. Again this can be controlled using a control voltage. Typically this might be provided under microprocessor control via a digital to analogue converter.

1.17.2. Working: The capacitance of the capacitor is dependent upon the area of the plates - the larger the area the greater the capacitance, and also the distance between them - the greater the distance the smaller the level of capacitance.

A reverse biased diode has no current flowing between the P-type area and the N-type area. The N-type region and the P-type regions can conduct electricity, and can be considered to be the two plates and the region between them - the depletion region is the insulating dielectric. This is exactly the same as the capacitor above.

As with any diode, if the reverse bias is changed so does the size of the depletion region. If the reverse voltage on the varactor or varicap diode is increased, the depletion region of the diode increases and if the reverse voltage on varactor diode is decreased the depletion region narrows. Therefore by changing the reverse bias on the diode it is possible to change the capacitance.



Varactor Diode

The varactor diode or varicap diode is shown in circuit diagrams or schematics using a symbol that combines the diode and capacitor symbols. In this way it is obvious that it is being used as a variable capacitor rather than a rectifier.

When operated in a circuit, it is necessary to ensure the varactor diode remains reverse biased. This means that the cathode will be positive with respect to the anode, i.e. the cathode of the varactor will be more positive than the anode. As a result, one can conclude that the capacitance of the varactor diode can be varied by varying the magnitude of the reverse bias voltage as it varies the width of the depletion region, d. Also it is evident from the capacitance equation that d is inversely proportional to C. This means that the junction capacitance of the varactor diode decreases with an increase in the depletion region width caused to due to an increase in the reverse bias voltage (VR), as shown by the graph in Figure below. Meanwhile it is important to note that although all the diodes exhibit the similar property, varactor diodes are specially manufactured to achieve the objective. In other words varactor diodes are manufactured with an intention to obtain a definite C-V curve which can be accomplished by controlling the level of doping during the process of manufacture. Depending on this, varactor diodes can be classified into two types viz., abrupt varactor diodes and hyper-abrupt varactor diodes, depending on whether the p-n junction diode is linearly or non-linearly doped (respectively).

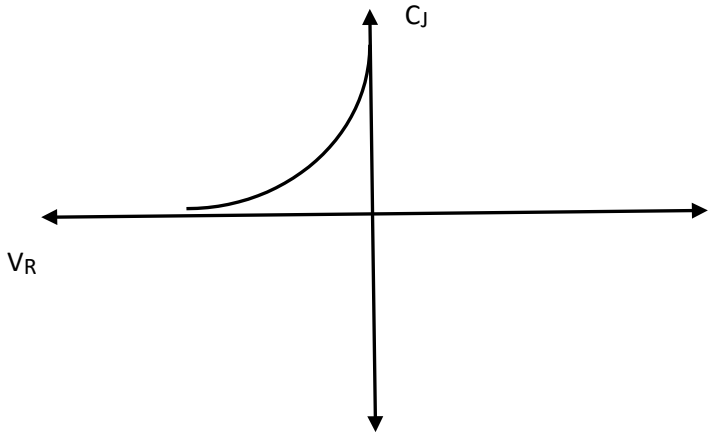


Figure.1.20. Characteristic curves of varactor diode

1.18. Tunnel Diode:

A tunnel diode or Esaki diode is a type of semiconductor diode that is capable of very fast operation, well into the microwave frequency region, by using the quantum mechanical effect called "Tunneling".

A tunnel diode is a high conductivity two terminal P-N Junction diode doped heavily about 1000 times higher than a conventional junction diode. Tunnel diodes are useful in many circuit applications in microwave amplification, microwave oscillation and binary memory.

The tunnel diode exhibits a special characteristic know as negative resistance. This feature makes it useful in oscillator and microwave amplifier applications. Tunnel diodes are constructed with germanium or gallium arsenide by doping the p and n regions much more heavily than in a conventional rectifier diode.

Tunnel Diode

This heavy doping allows conduction for all reverse voltages so that there is no breakdown effect as with the conventional rectifier diode.

Working of Tunnel Diode:

When a small forward bias voltage is applied across a tunnel diode, it begins to conduct current. As the voltage is raised, the current increases and attains a peak value known as peak current. If the current is increased a little more, the current actually begins to decreases until it reaches a low point called the valley current. If the voltage is increased further yet, the current begins to increase again, the time without decreasing into another “valley”. The region on the graph where the current is decreasing while applied voltage is increasing is known as the region of the negative resistance.

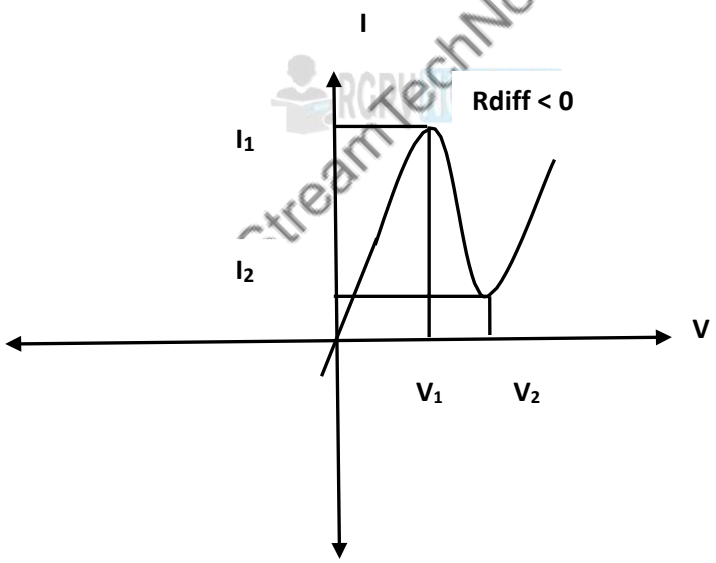


Figure.1.21. Characteristic curves of Tunnel diode

1.18.1. Mechanics behind working:

According to classical mechanics theory, a particle must have an energy at least equal to the the height of a potential-energy barrier if it has to move from one side of the barrier to the other. In other words, energy has to be supplied from some external source so that the electrons on N side of junction climb over the junction barrier to reach the P-side.

However if the barrier is thin such as in tunnel diode, the Schrodinger equation (Quantum Mechanics) indicates that there is a large probability that an electron will penetrate through the barrier. This will happen without any loss of energy on the part of electron. This quantum mechanical behavior is referred to as tunneling and the high-impurity P-N junction devices are called tunnel-diodes. The tunneling phenomenon is a majority carrier effect.

1.18.2. Why tunneling?

It is that the reduced depletion layer can form result in carriers "punching through" the junction with the velocity of light even when they do not possess enough energy to overcome the potential barrier. The result is that large forward current is produced at relatively low forward voltage (less than 100mv) such a mechanism of conduction in which charge carriers (possessing very little energy) punch through a barrier directly instead of climbing over it is called tunneling. That's why such diodes are known as tunnel diodes. Because of heavy doping the tunnel diode can conduct in reverse as well as in formed direction but it is usually used in forward biased mode.

1.18.3. Reverse Bias

In the tunnel diode, the dopant concentration in the p and n layers are increased to the point where the reverse breakdown voltage becomes zero and the diode conducts in the reverse direction.

1.18.4. Applications of Tunnel Diode

The tunnel diode showed great promise as an oscillator and high-frequency threshold (trigger) device since it would operate at frequencies far greater than the tetrode would, well into the microwave bands.

Applications for tunnel diodes included local oscillators for UHF television tuners, trigger circuits in oscilloscopes, high speed counter circuits, and very fast-rise time pulse generator circuits.

The tunnel diode can also be used as low-noise microwave amplifier.

Tunnel diodes are also relatively resistant to nuclear radiation, as compared to other diodes. This makes them well suited to higher radiation environments, such as those found in space applications.

1.19. PIN Diode:

A PIN diode has heavily doped p & n regions separated by an intrinsic semiconductor. PIN diodes are usually fabricated using Silicon or Gallium Arsenide. When reverse biased, it acts like a constant capacitance and when forward biased it behaves like a variable resistor at Radio frequencies. The forward resistance of the intrinsic region decreases with increasing current. A PIN diode is actually a DC controlled high frequency resistor which will act as an open circuit if no DC bias is applied. As the forward resistance of a PIN diode can be changed by changing the forward bias, it can be used as a modulating device for an AC signal. It is widely used in microwave switching applications. Thus we see that a PIN diode acts like a current controlled resistor ie. as the current increases the radio frequency resistance decreases.

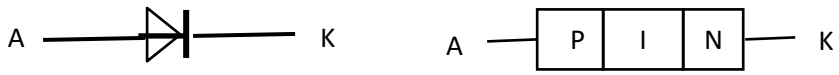


Figure.1.22. Symbol of PIN diode

PIN diode can behave as an open switch at low currents & as a closed switch at high currents PIN diode acts as a rectifier only at low frequencies. The frequency at which it starts behaving as a resistor depends on the thickness of the intrinsic region. One of the most important advantages of a PIN diode is that a very small DC control current can control a very large current at microwave frequencies. PIN diodes are widely used in Radio frequency, Ultra high frequency & micro wave circuits. PIN diodes can be used as switches, attenuators, phase shifters and modulators

1.20. Schottky Diode:

A Schottky barrier diode is a metal semiconductor junction formed by bringing metal in contact with a moderately doped n type semiconductor material. A Schottky barrier diode is also called as known as Schottky or hot carrier diode. It is named after its inventor Walter H. Schottky, barrier stands for the potential energy barrier for electrons at the junction. It is a unilateral device conducting currents in one direction (Conventional current flow from metal to semiconductor) and restricting in the other.

1.20.1. Physical construction:

A Schottky barrier diode is shown in the figure below

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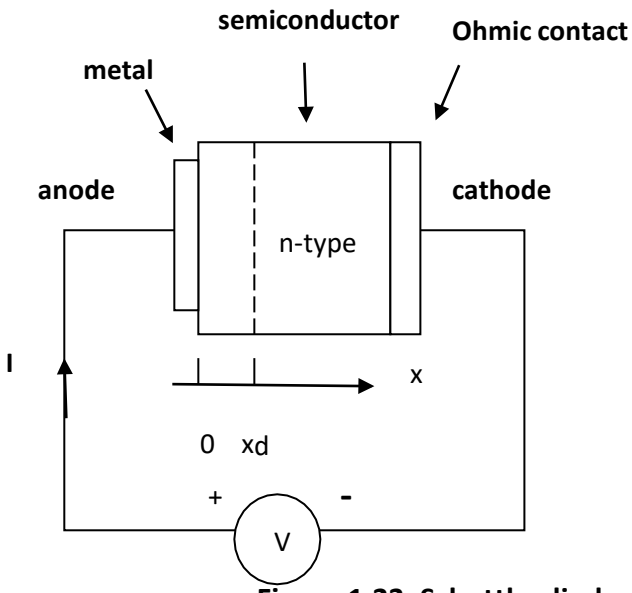
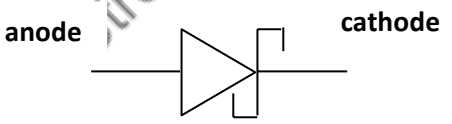


Figure.1.23. Schottky diode

A metal semiconductor junction is formed at one end, it is a unilateral junction. Another metal semiconductor contact is formed at the other end. It is an ideal Ohmic bilateral contact with no potential existing between metal and semiconductor and is non rectifying. The built-in potential across the open circuited Schottky barrier diode characterizes the Schottky barrier diode. It is a function of temperature and doping. It decreases with increasing temperature and doping concentration in N type semiconductor. The typical metals used in the manufacture of Schottky barrier diode are platinum, chromium, tungsten Aluminium, gold etc. and the semiconductor used is N type silicon is used.

1.20.2. Symbol of Schottky Diode:

A Schottky barrier diode is a two terminal device with metal terminal acting as anode and semiconductor terminal acting as anode. The circuit symbol of Schottky barrier diode is shown in the figure.



VI characteristics of Schottky barrier diode:

The VI characteristics of Schottky barrier diode is shown below

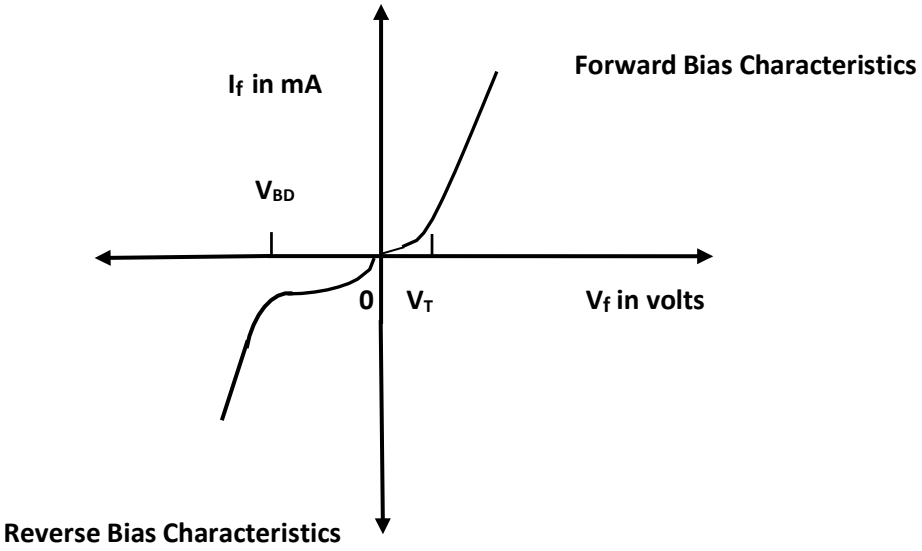


Figure.1.24. V-I Characteristics of Schottky diode

From the VI characteristics it is obvious that the VI characteristics of Schottky barrier diode is similar to normal PN junction diode with the following exceptions

The forward voltage drop of Schottky barrier diode is low compared to normal PN junction diode. The forward voltage drop of Schottky barrier diode made of silicon exhibits a forward voltage drop of 0.3 volts to o.5 volts. The forward voltage drop increases with the increasing doping concentration of n type semiconductor. The VI characteristics of Schottky barrier diode is Steeper compared to VI characteristics of normal PN junction diode due to high concentration of current carriers.

1.21. Light Emitting Diodes LED:

Light Emitting Diodes (LEDs) are the most widely used semiconductor diodes among all the different types of semiconductor diodes available today. Light emitting diodes emit either visible light or invisible infrared light when forward biased. The LEDs which emit invisible infrared light are used for remote controls.A light Emitting Diode (LED) is an optical semiconductor device that emits light when voltage is applied. In other words, LED is an optical semiconductor device that converts electrical energy into light energy.

When Light Emitting Diode (LED) is forward biased, free electrons in the conduction band recombines with the holes in the valence band and releases energy in the form of light. The process of emitting light in response to the strong electric field or flow of electric current is called electroluminescence.

A normal p-n junction diode allows electric current only in one direction. It allows electric current when forward biased and does not allow electric current when reverse biased. Thus, normal p-n junction diode operates only in forward bias condition.

Like the normal p-n junction diodes, LEDs also operates only in forward bias condition. To create an LED, the n-type material should be connected to the negative terminal of the battery and p-type material should be connected to the positive terminal of the battery. In other words, the n-type material should be negatively charged and the p-type material should be positively charged. The construction of LED is similar to the normal p-n junction diode except that gallium, phosphorus and arsenic materials are used for construction instead of silicon or germanium materials.

In normal p-n junction diodes, silicon is most widely used because it is less sensitive to the temperature. Also, it allows electric current efficiently without any damage. In some cases, germanium is used for constructing diodes. However, silicon or germanium diodes do not emit energy in the form of light. Instead, they emit energy in the form of heat. Thus, silicon or germanium is not used for constructing LEDs.

1.21.1. How Light Emitting Diode (LED) works?

Light Emitting Diode (LED) works only in forward bias condition. When Light Emitting Diode (LED) is forward biased, the free electrons from n-side and the holes from p-side are pushed towards the junction.

When free electrons reach the junction or depletion region, some of the free electrons recombine with the holes in the positive ions. We know that positive ions have less number of electrons than protons. Therefore, they are ready to accept electrons. Thus, free electrons recombine with holes in the depletion region. In the similar way, holes from p-side recombine with electrons in the depletion region.

Because of the recombination of free electrons and holes in the depletion region, the width of depletion region decreases. As a result, more charge carriers will cross the p-n junction.Some of the charge carriers from p-side and n-side will cross the p-n junction before they recombine in the depletion region. For example, some free electrons from n-type semiconductor cross the p-n junction and recombines with holes in p-type semiconductor. In the similar way, holes from p-type semiconductor cross the p-n junction and recombines with free electrons in the n-type semiconductor. Thus, recombination takes place in depletion region as well as in p-type and n-type semiconductor.

The free electrons in the conduction band releases energy in the form of light before they recombine with holes in the valence band.In silicon and germanium diodes, most of the energy is released in the form of heat and emitted light is too small.However, in materials like gallium arsenide and gallium phosphide the emitted photons have sufficient energy to produce intense visible light.

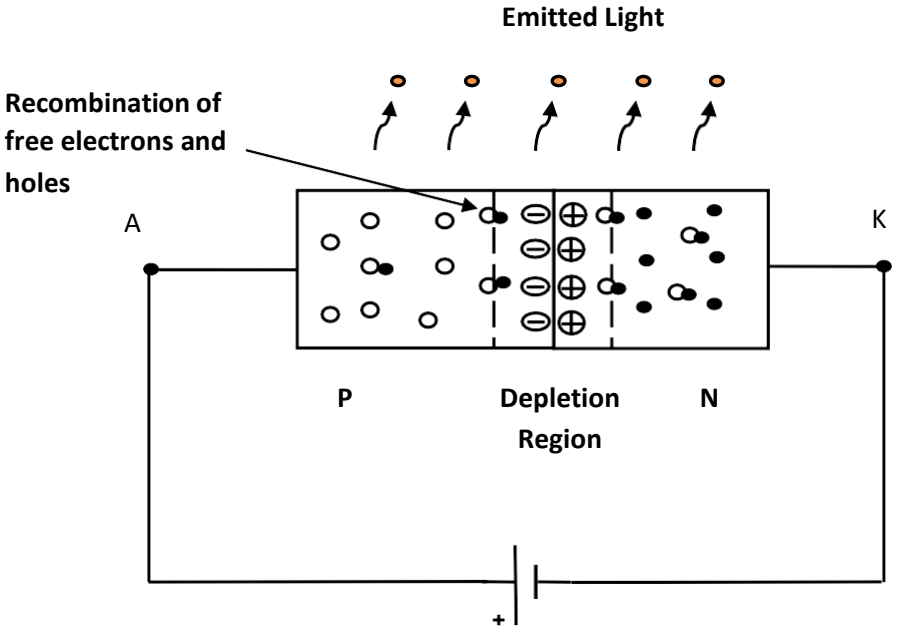
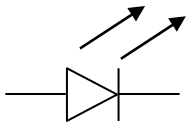


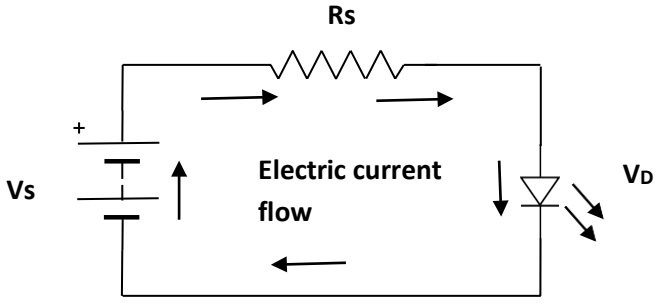
Figure.1.25.LED circuit

Light emitting diode (LED) symbol:



The symbol of LED is similar to the normal p-n junction diode except that it contains arrows pointing away from the diode indicating that light is being emitted by the diode.
LEDs are available in different colors. The most common colors of LEDs are orange, yellow, green and red.
The schematic symbol of LED does not represent the color of light. The schematic symbol is same for all colors of LEDs. Hence, it is not possible to identify the color of LED by seeing its symbol.

1.21.2. Biasing of LED:



The safe forward voltage ratings of most LEDs are from 1V to 3 V and forward current ratings is from 200 mA to 100 mA. If the voltage applied to LED is in between 1V to 3V, LED works perfectly because the current flow for the applied voltage is in the operating range. However, if the voltage applied to LED is increased to a value greater than 3 volts. The depletion region in the LED breaks down and the electric current suddenly rises. This sudden rise in current may destroy the device. To avoid this we need to place a resistor (Rs) in series with the LED. The resistor (Rs) must be placed in between voltage source (Vs) and LED.
The resistor placed between LED and voltage source is called current limiting resistor. This resistor restricts extra current which may destroy the LED. Thus, current limiting resistor protects LED from damage. The current flowing through the LED is mathematically written as
Forward current in LED is

Where, $If = (Vs - Vd)/Rs$

If = Forward current
Vs = Source voltage or supply voltage
Vd = Voltage drop across LED
Rs = Resistor or current limiting resistor

Voltage drop is the amount of voltage wasted to overcome the depletion region barrier (which leads to electric current flow). The voltage drop of LED is 2 to 3V whereas silicon or germanium diode is 0.3 or 0.7 V. Therefore, to operate LED we need to apply greater voltage than silicon or germanium diodes. Light emitting diodes consume more energy than silicon or germanium diodes to operate.

1.22. Photo Diode:

Photo means light and diode means a device consisting of two electrodes. A photo diode is a light sensitive electronic device capable of converting light into a voltage or current signal. It works on the principle of photo generation.
Symbol of Photo diode

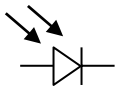


Photo diode has two terminals anode and cathode with the arrows indicating that the light rays falling on photo diode reflecting its significance as a photo detector.

1.22.1. Types of photo diodes

There are mainly three types of photo diodes

- PN junction photo diode
- Avalanche photo diode
- PIN photo diode

Normal PN junction photo diode is used in low frequency and low sensitive applications. When high frequency of operation and high sensitivity is needed avalanche photo diode or PIN photo diodes are used.

1.22.2. Physical Structure of photo diode

A normal PN junction photo diode is made by sandwiching a P type semiconductor into N type semiconductor. All the sides of PN junction diode is enclosed in metallic case or painted black except for one side on which radiation is allowed to fall.

1.22.3. Modes of operation of Photo diode

A photo sensitive diode can be operated mainly in two modes

- Photo conductive mode
- Photo voltaic mode

The photo diodes used as photo detectors are optimized (in the physical construction of the device itself) to have fast response times whereas the photo diodes used in electrical energy generation are optimized to have high efficiency of energy conversion. The photo detectors are operated in photo conductive mode. Solar cells are operated in Photo voltaic mode.

1.22.4. Principle of operation

When a PN junction is illuminated with light, it ionizes covalent bonds and new hole, electron pairs are generated in excess of thermally generated pairs. If the photo generation occurs at a distance of the diffusion length order or less depletion layer the photo generated electron hole pairs are swept across by the applied reverse bias field. This mode of operation of photo diode is called photo conductive mode. The photo current varies almost linearly with incident light flux or optical power. The mode of operation of photo diode is called photo conductive diode.

1.22.5. V-I characteristics of photo diode

A photo diode is always operated in reverse bias mode. From the photo diode characteristics it is seen clearly that the photo current is almost independent of applied reverse bias voltage. For zero luminance the photo current is almost zero except for small dark current. It is of the order of nano amperes. As optical power increases the photo current also increases linearly. The maximum photo current is limited by the power dissipation of the photo diode**.**

1.22.6. Applications of photo diodes:

Photo diodes are used as photo detectors

Photo diodes are used in providing electric isolation using a special circuitry called as Opto-couplers. Opto-coupler is an electronic component which is used in coupling optically the two isolated circuits by using light. The two circuits are optically coupled but electrically isolated. It is a combination of light emitting diode and photo diode (or) avalanche diode (or) photo transistor. Opto-couplers are faster than the conventional devices.

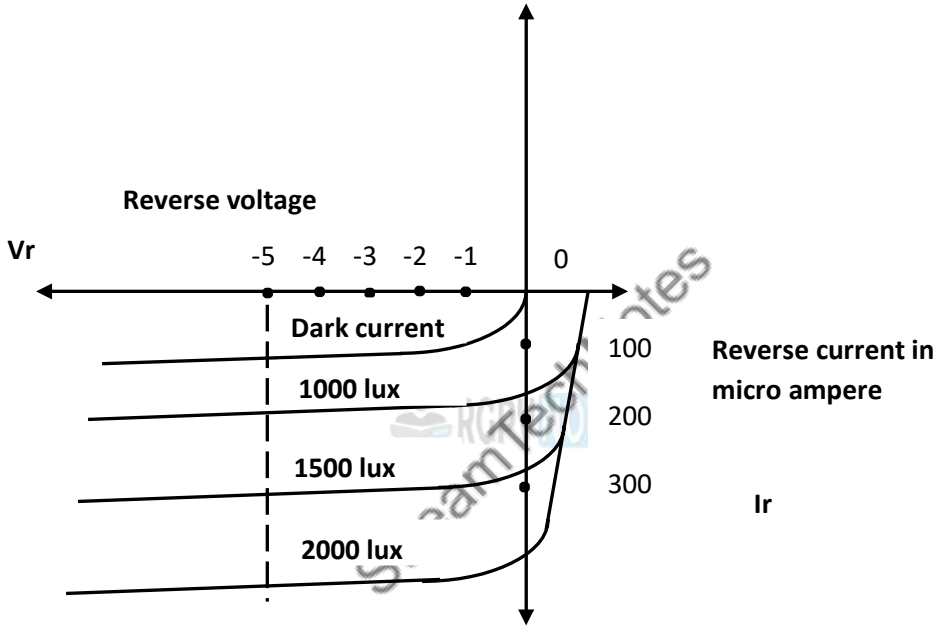


Figure.1.26. The V-I characteristics of a photo diode

1.23. Switching characteristics of diode:

When diode is switched from forward biased to the reverse biased state or vice versa, it takes finite time to attain a steady state.

This time consists of a transient and an interval of time before the diode attains a steady state. The behavior of the diode during this time is called switching characteristics of the diode. In the forward-bias state, there are a large number of electrons from the n side diffusing into p side and a large number of holes diffusing into n side from p side. This diffusion process establishes a large number of minority carriers in each material.

When forward biased, let n is concentration of electrons on p side at thermal equilibrium and p is concentration of holes on n side thermal equilibrium. This is concentration level far away from the junction. It increases towards the junction and becomes n and Pn on p and n side respectively in steady state. These minority charge carriers are supplied from other side of the junction, where those carriers are majority in number.

When the diode is reverse biased, again far from the junction the minority charge concentration is n on p side and Pno on n side. In reverse biased condition, as they approach the junction, they quickly cross the junction. Hence minority carrier concentration decreases to zero at the junction in steady state.

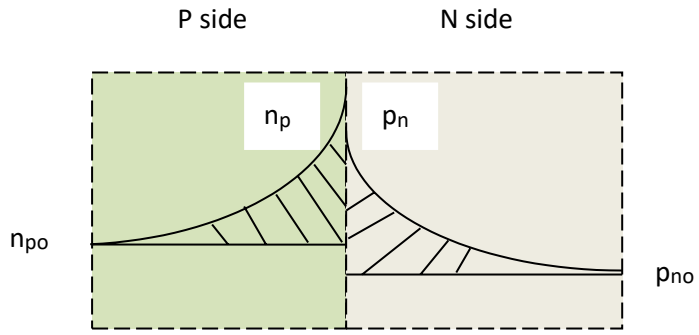


Figure.1.27. Carrier profile for switching in diode

Now when a forward biased diode is suddenly reverse biased, it takes finite time to change the minority charge carrier concentration and to attain new steady state value. The diode cannot attain steady state till the minority charge carrier concentration changes from that corresponding to the forward biased to that corresponding to the reverse biased. Till the excess charge carrier concentration pn-pno and np-npo reduces to zero, the diode continues to conduct. This current is decided by the current limiting external resistance connected in the circuit. Hence in switching applications, the time required by the diode to attain new steady state, plays an important role.

1.23.1.Diode switching time: In AC applications, when diode is instantaneously switched from a conduction state to a non conduction state it needs some time to return to non conduction state and behaves short circuited for a little time period in reverse direction. This occurs because when the diode biasing is suddenly changed, the majority charge carriers migrated to other region is the minority charge carriers in the region. Specifically, holes are the minority carriers migrated from p-type to n-type in reverse bias. . These holes require some time to return back to state of non conduction which is called as the 'Reverse recovery time'. Reverse recovery time is the sum of storage time and the transition time.

· **Storage time:** The time period for which diode remains in conduction state even in the reverse direction.

· **Transition time:** The time elapsed in returning back to state of non conduction.

It is desirable those diodes has minimum switching or reverse recovery time t_{rr}. Switching time of diodes is of the order of few nanoseconds to 1 microsecond. Now fast switching diodes with switching time up to few picoseconds are also available.

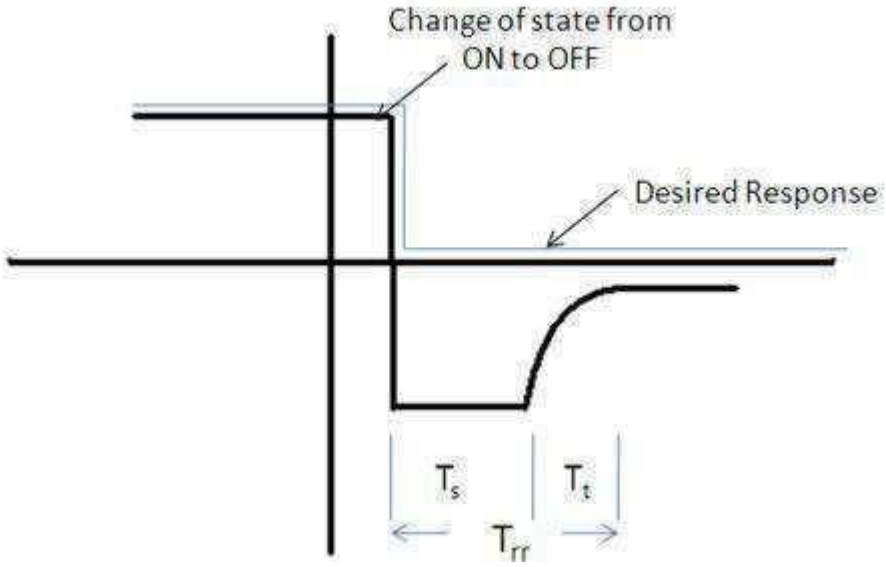
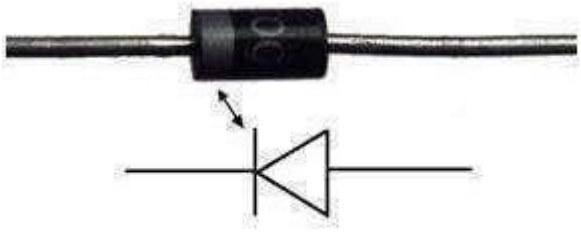


Figure.1.28. Characteristics of diode witching time

Identification of diode:

A diode is marked with a bar which indicates the cathode terminal of a diode which is as shown in the figure below:

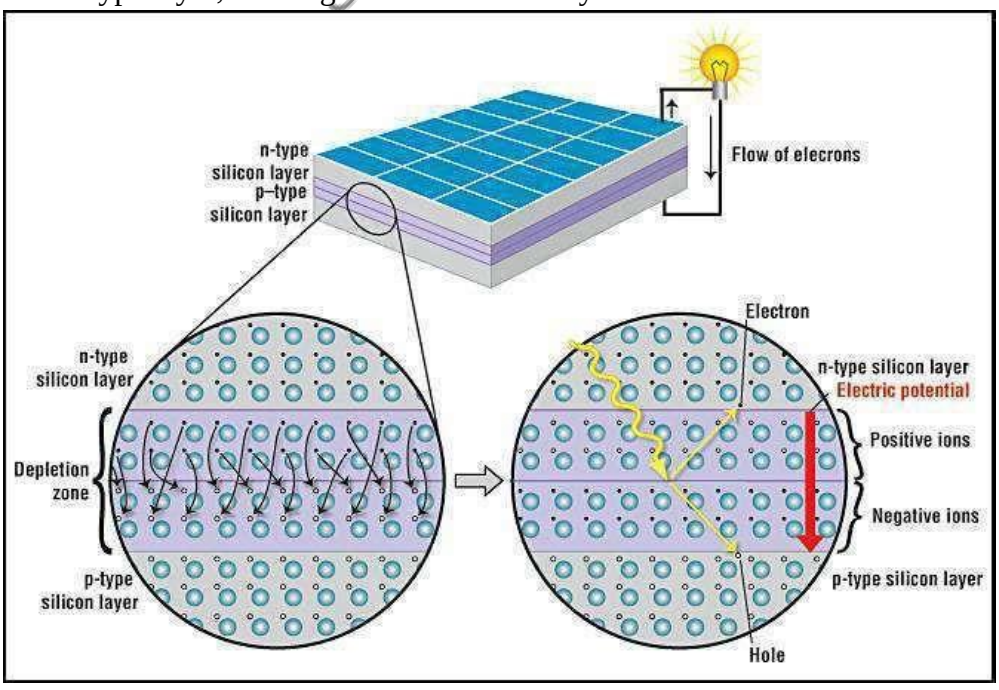


Solar Cell:

A solar cell consists of a layer of p-type silicon placed next to a layer of n-type silicon (Fig. 1). In the n-type layer, there is an excess of electrons, and in the p-type layer, there is an excess of positively charged holes (which are vacancies due to the lack of valence electrons). Near the junction of the two layers, the electrons on one side of the junction (n-type layer) move into the holes on the other side of the junction (p-type layer). This creates an area around the junction, called the depletion zone, in which the electrons fill the holes

When all the holes are filled with electrons in the depletion zone, the p-type side of the depletion zone (where holes were initially present) now contains negatively charged ions, and the n-type side of the depletion zone (where electrons were present) now contains positively charged ions. The presence of these oppositely charged ions creates an internal electric field that prevents electrons in the n-type layer to fill holes in the p-type layer.

When sunlight strikes a solar cell, electrons in the silicon are ejected, which results in the formation of "holes"—the vacancies left behind by the escaping electrons. If this happens in the electric field, the field will move electrons to the n-type layer and holes to the p-type layer. If you connect the n-type and p-type layers with a metallic wire, the electrons will travel from the n-type layer to the p-type layer by crossing the depletion zone and then go through the external wire back of the n-type layer, creating a flow of electricity.



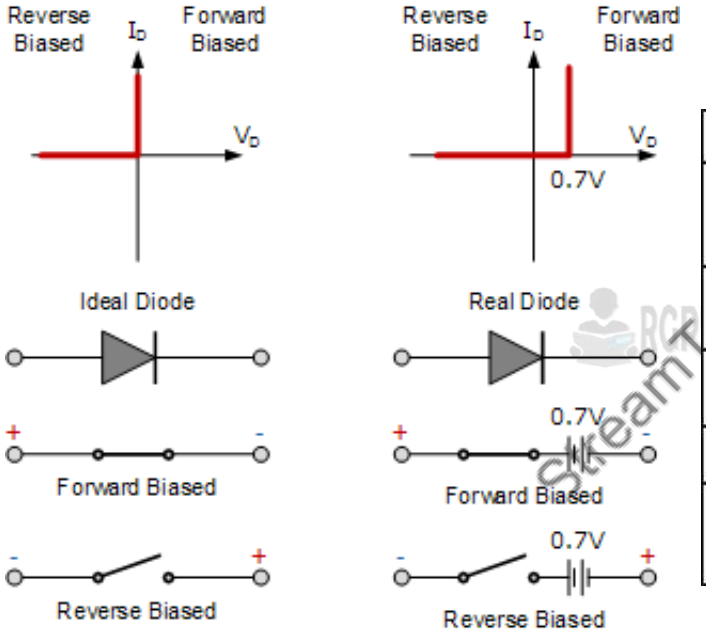
UNIT-II: Diode circuits: Ideal and Practical diode, Clipper, Clamper.
Power Supply: Rectifiers-Half wave, Full wave, Bridge rectifier, filter circuits, Voltage regulation using shunt & series regulator circuits, Voltage regulation using IC.

2.1. Ideal and Practical Diode: An ideal diode is a non linear device. It performs like an ideal conductor when voltage is applied in forward bias and like an ideal insulator when the voltage is applied in reverse bias. So when +ve voltage is applied across the anode toward the cathode, the diode performs forward current immediately. When a voltage is applied in reverse bias, then there is no current at all. Also the current will flow only when voltage applied will be greater than it's threshold value.

A **Real diode** contains barrier potential V_0 (0.7 V for silicon and 0.3 V for Germanium) and a forward resistance R_F of about 25 ohms. When a diode is forward biased and conducts a forward current I_F flows through it which causes a voltage drop $I_F R_F$ in the forward resistance. Hence, the forward voltage V_F applied across the real diode for conduction, has to overcome the following.

- Potential barrier
- Drop in forward resistance

The **V-I characteristics** of the Ideal and real diode are shown in the figure below.



IDEAL DIODE	PRACTICAL DIODE	REFERENCE
No reverse leakage current	Finite reverse leakage current (increases with temperature & reverse voltage)	I_R
No limit to reverse reverse blocking	Maximum reverse surge voltage Reverse breakdown voltage	V_{RSM} V_{BR}
Zero forward voltage drop when conducting	Finite forward voltage drop (Approx 0.7V for silicon rectifier)	V_F
Zero forward resistance	Finite forwrd dynamic resistance	See figure
Unlimited forward current capacity	Maximum average onstate current Maximum RMS on-state current Peak 1-cycle surge current	I_{TAV} I_{TRMS} I_{TSM}

Figure.2.1. Ideal and Real diode characteristics

2.2. Clipper:

Clipping circuits (also known as limiters, amplitude selectors, or slicers), are used to remove the part of a signal that is above or below some defined reference level. The basic components required for a clipping circuit are – an ideal diode and a resistor. In order to fix the clipping level to the desired amount, a dc battery must also be included. When the diode is forward biased, it acts as a closed switch, and when it is reverse biased, it acts as an open switch. Different levels of clipping can be obtained by varying the amount of voltage of the battery and also interchanging the positions of the diode and resistor.

Depending on the features of the diode, the positive or negative region of the input signal is "clipped" off and accordingly the diode clippers are classified as:

- positive clipper
- Negative clippers.

Depending on the diode connection there are two types of clipper circuits:

- Series clipper
- Parallel Clipper

2.2.1. Positive Series Clipper:

In series Diode Clipping Circuit, the diode is connected between the input and output voltage terminals. In a positive clipper, the positive half cycles of the input voltage will be removed. Although the input voltage to diode clipping circuits can have any waveform shape, we will assume here that the input voltage is sinusoidal.

The series positive clipper circuit is connected as shown in the figure. During the positive half cycle, diode becomes reverse biased, and no output is generated across the resistor, and during the negative half cycle, the diode conducts and the entire input appears as output across the resistor.

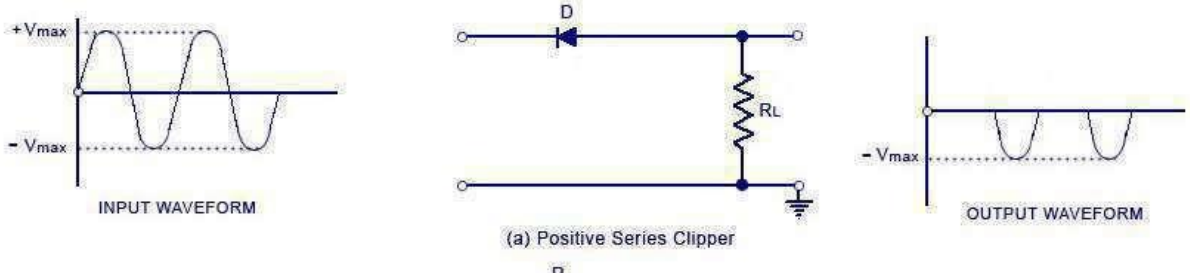


Figure.2.2. Series Positive Clipper

2.2.2. Positive Shunt Clipper:

In this diode clipping circuit, the diode is forward biased (anode more positive than cathode) during the positive half cycle of the sinusoidal input waveform. For the diode to become forward biased, it must have the input voltage magnitude greater than +0.7 volts (0.3 volts for a germanium diode).

When this happens the diodes begins to conduct and holds the voltage across itself constant at 0.7V until the sinusoidal waveform falls below this value. Thus the output voltage which is taken across the diode can never exceed 0.7 volts during the positive half cycle.

During the negative half cycle, the diode is reverse biased (cathode more positive than anode) blocking current flow through itself and as a result has no effect on the negative half of the sinusoidal voltage which passes to the load unaltered. Thus the diode limits the positive half of the input waveform and is known as a positive clipper circuit.

Figure.2.3. Shunt Positive Clipper

2.2.3. Negative Series Clipper:

The figure 2.4 shows a series negative clipper with its output waveforms. During the positive half cycle the diode (considered as ideal diode) appears in the forward biased and conducts such that the entire positive half cycle of input appears across the resistor connected in parallel as output waveform. During the negative half cycle the diode is in reverse biased. No output appears across the resistor. Thus, it clips the negative half cycle of the input waveform, and therefore, it is called as a series negative clipper.

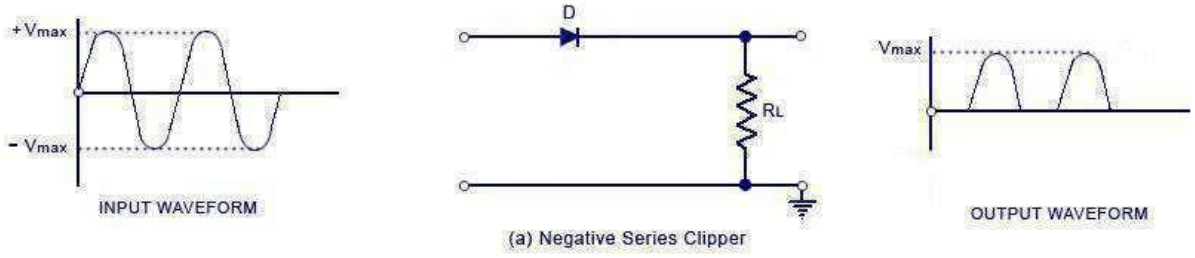


Figure.2.4.Series Negative Clipper

2.2.4. Negative Shunt Clipper: Shunt negative clipper is connected as shown in the above figure. During the positive half cycle, the entire input is the output, and during the negative half cycle, the diode conducts causing no output to be generated from the input. The diode is forward biased during the negative half cycle of the sinusoidal waveform and limits or clips it to –0.7 volts while allowing the positive half cycle to pass unaltered when reverse biased. As the diode limits the negative half cycle of the input voltage it is therefore called a negative clipper circuit.

Figure.2.5. Shunt Negative clipper

2.2.5. Biased Clippers:

To produce diode clipping circuits for voltage waveforms at different levels, a bias voltage, V_{BIAS} is added in series with the diode to produce a combination clipper as shown. The voltage across the series combination must be greater than V_{BIAS} + 0.7V before the diode becomes sufficiently forward biased to conduct.

2.2.5.1. Positive Biased Clipping

Working: During the positive half cycle, the negative reference voltage connected in series with the diode appears as output; and during the negative half cycle, the diode conducts until the input voltage value becomes greater than the negative reference voltage and output will be generated as shown in the figure.

Figure.2.6.Positive Shunt biased clipper

2.2.5.2. Negative Bias Diode Clipping:

Working: Instead of positive reference voltage, a negative reference voltage is connected in series with the diode to form a shunt negative clipper with a negative reference voltage. During the positive half cycle, the entire input appears as output, and during the negative half cycle, a reference voltage appears as output as shown in the above figure.

Figure.2.7.Negative Shunt Biased Clipper

2.2.5.3. Combinational Clipper:

Working: The action of the circuit is summarized below. For positive input voltage signal when input voltage exceeds battery voltage '+ V_1' diode D_1 conducts heavily while diode 'D_2' is reversed biased and so voltage '+ V_1' appears across the output. This output voltage '+ V_1' stays as long as. the input signal voltage exceeds '+ V_1'. On the other hand for the negative input voltage signal, the diode 'D_1' remains reverse biased and diode 'D_2' conducts heavily only when input voltage exceeds battery voltage 'V_2' in magnitude. Thus during the negative half cycle the output stays at '- V_2' so long as the input signal voltage is greater than '-V_2'.

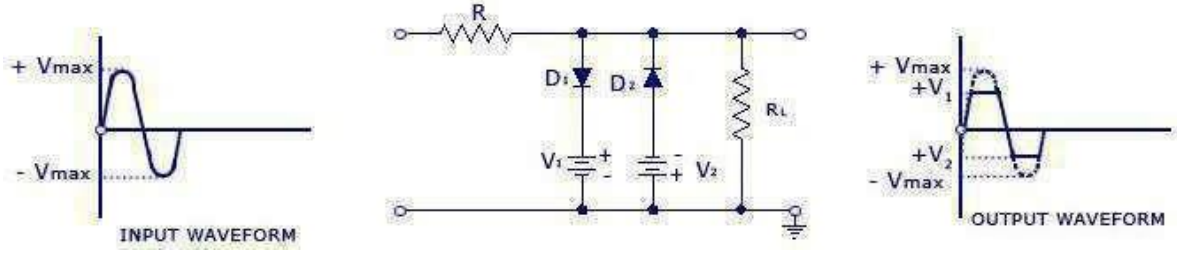


Figure.2.8.Combinational Clipper

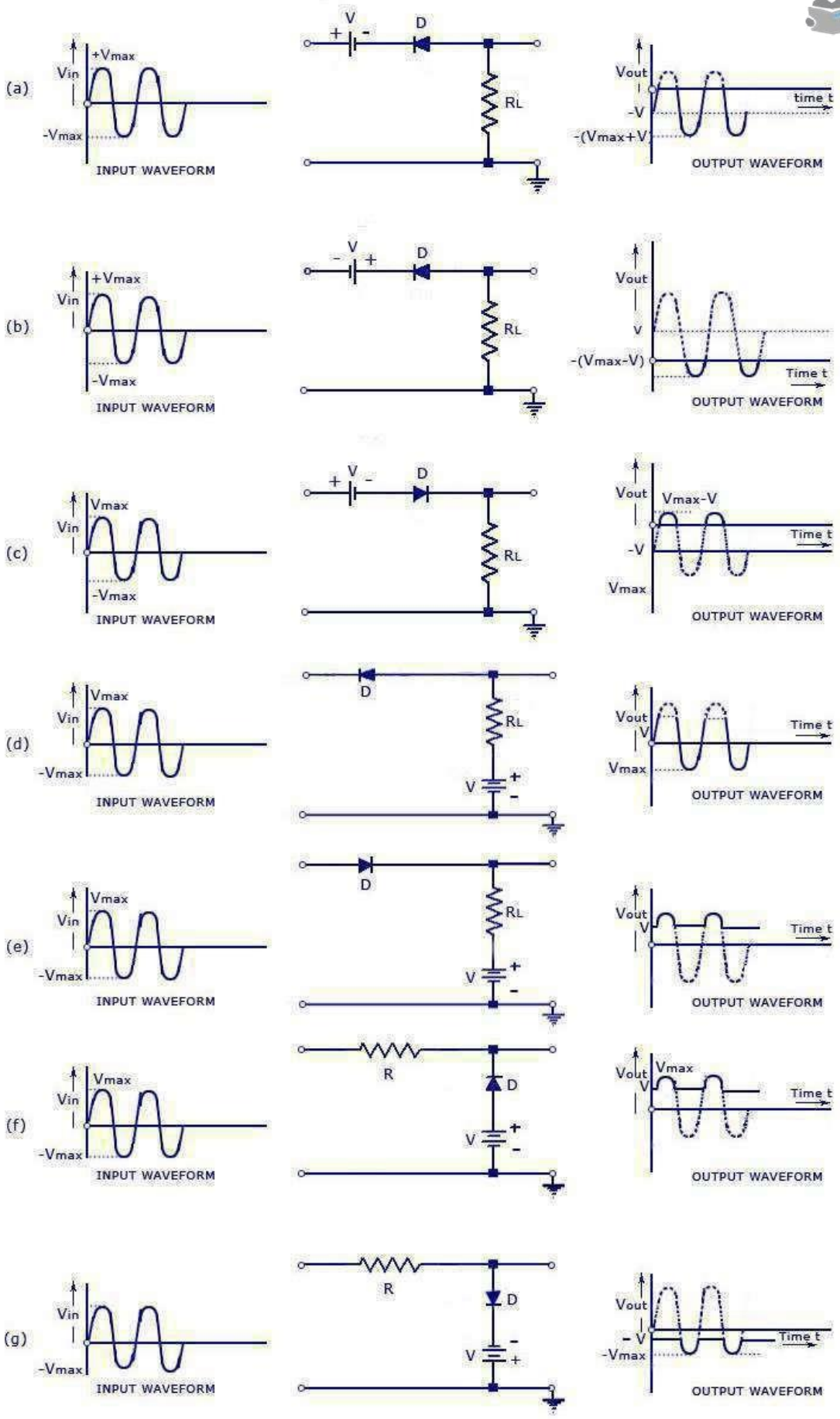


Figure.2.9. Different Clipping circuits

2.2.6. Drawbacks of Series and Shunt Diode Clippers

- In series clippers, when the diode is in 'OFF' position, there will be no transmission of input signal to output. But in case of high frequency signals transmission occurs through diode

capacitance which is undesirable. This is the drawback of using diode as a series element in such clippers.

- In shunt clippers, when diode is in the 'off condition, transmission of input signal should take place to output. But in case of high frequency input signals, diode capacitance affects the circuit operation adversely and the signal gets attenuated (that is, it passes through diode capacitance to ground).

2.3. Clampers:

A Clamper circuit can be defined as the circuit that consists of a diode, a resistor and a capacitor that shifts the waveform to a desired DC level without changing the actual appearance of the applied signal.

In order to maintain the time period of the wave form, the **tau** must be greater than, half the time period (discharging time of the capacitor should be slow.)

$$\tau=RC$$

Where

- R is the resistance of the resistor employed
- C is the capacitance of the capacitor used

The time constant of charge and discharge of the capacitor determines the output of a clamper circuit.

- In a clamper circuit, a vertical shift of upward or downward takes place in the output waveform with respect to the input signal.
- The load resistor and the capacitor affect the waveform. So, the discharging time of the capacitor should be large enough.

The DC component present in the input is rejected when a capacitor coupled network is used (as a capacitor blocks dc). Hence when dc needs to be restored, clamping circuit is used.

2.3.1. Positive Clamper:

When a negative peak of the signal is raised above to the zero level, then the signal is said to be positively clamped. It shifts the output signal to the positive portion of the input signal. The figure below explains the construction of a positive clamper circuit.

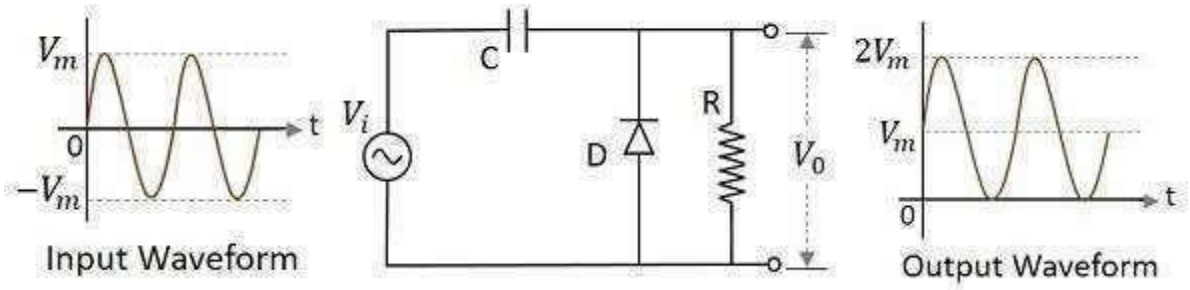


Figure.2.10. Positive Clamper

Initially when the input is given, the capacitor is not yet charged and the diode is reverse biased. The output is not considered at this point of time. During the negative half cycle, at the peak value, the capacitor gets charged with negative on one plate and positive on the other. The capacitor is now charged to its peak value V_m. The diode is forward biased and conducts heavily.

During the next positive half cycle, the capacitor is charged to positive Vm while the diode gets reverse biased and gets open circuited. The output of the circuit at this moment will be

$$V_0=V_i+V_m$$

Hence the signal is positively clamped as shown in the above figure. The output signal changes according to the changes in the input, but shifts the level according to the charge on the capacitor, as it adds the input voltage.

2.3.2. Positive Clamper with reference voltage V_r

A Positive clamper circuit if biased with some positive reference voltage, that voltage will be added to the output to raise the clamped level. Using this, the circuit of the positive clamper with positive reference voltage is constructed as below.

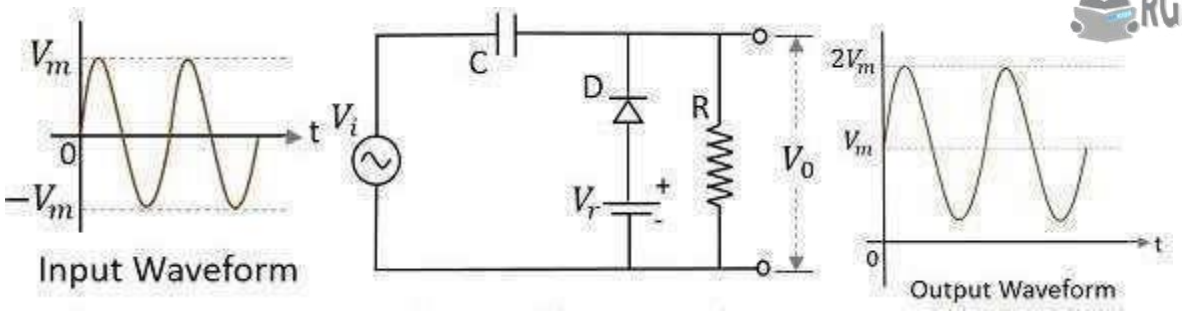


Figure.2.11.Positive Biased clamper with ($+V_{r+}$)

During the positive half cycle, the reference voltage is applied through the diode at the output and as the input voltage increases, the cathode voltage of the diode increase with respect to the anode voltage and hence it stops conducting. During the negative half cycle, the diode gets forward biased and starts conducting. The voltage across the capacitor and the reference voltage together maintain the output voltage level.

A Positive clamper circuit if biased with some negative reference voltage is designed.

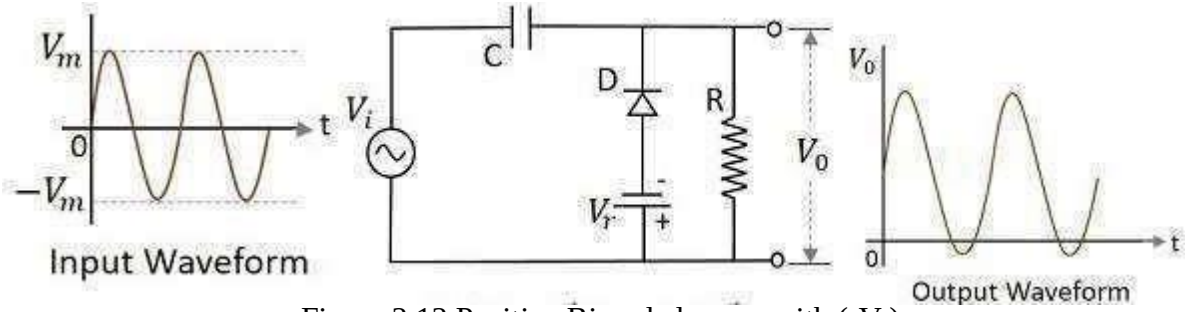


Figure.2.12.Positive Biased clamper with ($-V_r$)

2.3.3. Negative Clamper:

A Negative Clamper circuit is one that consists of a diode, a resistor and a capacitor and that shifts the output signal to the negative portion of the input signal. The figure below explains the construction of a negative clamper circuit.

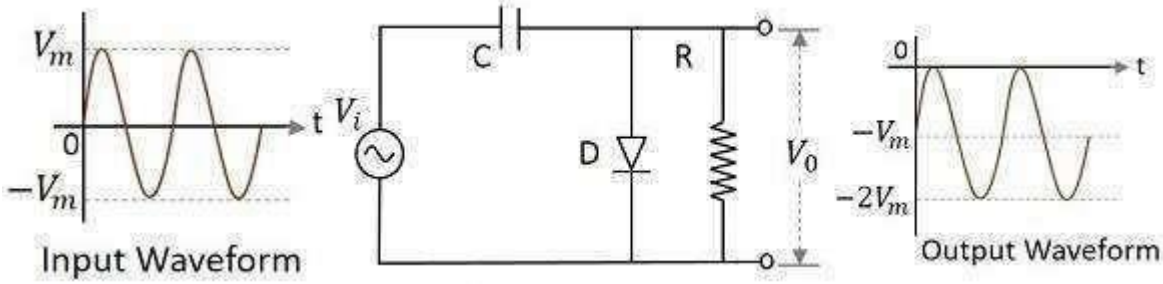


Figure.2.13.Negative clamper

During the positive half cycle, the capacitor gets charged to its peak value v_m. The diode is forward biased and conducts. During the negative half cycle, the diode gets reverse biased and gets open circuited. The output of the circuit at this moment will be

$$V_0=V_i+V_m$$

Hence the signal is negatively clamped as shown in the above figure. The output signal changes according to the changes in the input, but shifts the level according to the charge on the capacitor, as it adds the input voltage.

2.3.4. Negative clamper with reference voltage V_r

A Negative clamper circuit if biased with some positive reference voltage, that voltage will be added to the output to raise the clamped level. Using this, the circuit of the negative clamper with positive reference voltage is constructed as below.

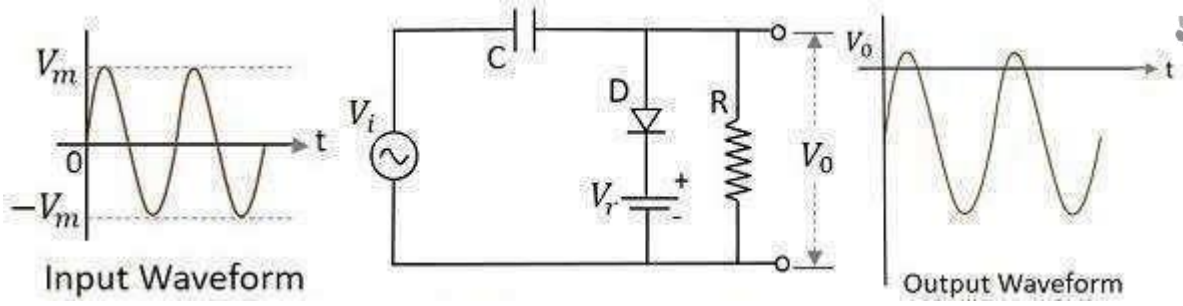


Figure.2.14.Negative Biased clamper with ($+V_r$)

Though the output voltage is negatively clamped, a portion of the output waveform is raised to the positive level, as the applied reference voltage is positive. During the positive half-cycle, the diode conducts, but the output equals the positive reference voltage applied. During the negative half cycle, the diode acts as open circuited and the voltage across the capacitor forms the output.

A Negative clamper circuit if biased with some negative reference voltage, that voltage will be added to the output to raise the clamped level. Using this, the circuit of the negative clamper with negative reference voltage is constructed as below.

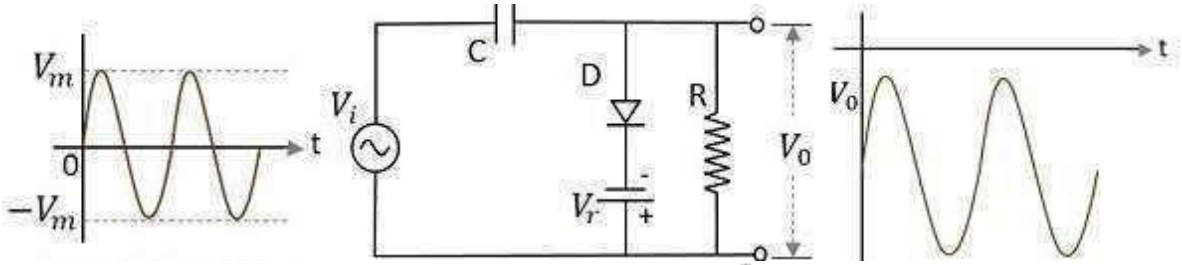


Figure.2.14.Negative Biased clamper with ($-V_r$)

2.4. Applications of Clippers and clampers:

Clippers

- Used for the generation and shaping of waveforms
- Used for the protection of circuits from spikes
- Used for amplitude restorers
- Used as voltage limiters
- Used in television circuits
- Used in FM transmitters

Clampers

- Used as direct current restorers
- Used to remove distortions
- Used as voltage multipliers
- Used for the protection of amplifiers
- Used as test equipment
- Used as base-line stabilizer

2.5. Rectifiers:

Rectification is the conversion of alternating current (AC) to direct current (DC). This involves a device that only allows one-way flow of electrons. The main application of p-n junction diode is in rectification circuits. Diode rectifier gives an alternating voltage which pulsates in accordance with time. The filter smoothes the pulsation in the voltage and to produce d.c voltage, a regulator is used which removes the ripples. There are two primary methods of diode rectification:

- Half Wave Rectifier
- Full Wave Rectifier

2.5.1. Half Wave Rectifier:

In a half-wave rectifier, one half of each a.c input cycle is rectified. When the p-n junction diode is forward biased, it gives little resistance and when it is reversing biased it provides high resistance.

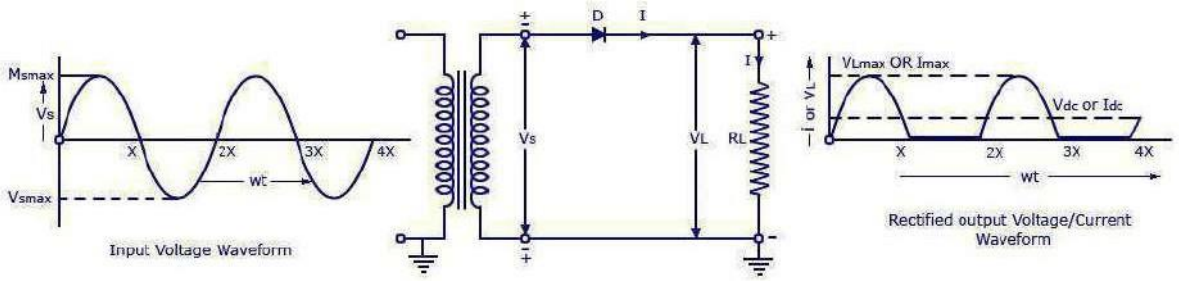


Figure.2.15. Half wave Rectifier

Working: The half wave rectifier has both positive and negative cycles. During positive half of the input, the current will flow from positive to negative which will generate only positive half cycle of the a.c supply. When a.c supply is applied to the transformer, the voltage will be decreasing at the secondary winding of the diode. All the variations in the a.c supply will reduce and we will get the pulsating d.c voltage to the load resistor.

In the second half cycle, current will flow from negative to positive and the diode will be reverse biased. Thus, at the output side, there will be no current generated and we cannot get power at the load resistance. A small amount of reverse current will flow during reverse bias due to minority carriers.

2.5.2. Centre Tapped Full Wave Rectifier

A centre tapped full wave rectifier is a type of rectifier which uses a centre tapped transformer and two diodes to convert the complete AC signal into DC signal.

The centre tapped full wave rectifier is made up of an AC source, a centre tapped transformer, two diodes, and a load resistor.

Full wave rectifier utilizes both halves of each a.c input. When the p-n junction is forward biased, the diode offers low resistance and when it is reversing biased it gives high resistance. The AC source is connected to the primary winding of the centre tapped transformer. A centre tap (additional wire) connected at the exact middle of the the secondary winding divides the input voltage into two parts.

The upper part of the secondary winding is connected to the diode D_1 and the lower part of the secondary winding is connected to the diode D_2. Both diode D_1 and diode D_2 are connected to a common load R_L with the help of a center tap transformer. The center tap is generally considered as the ground point or the zero voltage reference point.

Working:

When input AC voltage is applied, the secondary winding of the center tapped transformer divides this input AC voltage into two parts: positive and negative.

During the positive half cycle of the input AC signal, terminal A become positive, terminal B become negative and centre tap is grounded (zero volts). The positive terminal A is connected to the p-side of the diode D_1 and the negative terminal B is connected to the n-side of the diode D_1. So the diode D_1 is forward biased during the positive half cycle and allows electric current through it.

On the other hand, the negative terminal B is connected to the p-side of the diode D_2 and the positive terminal A is connected to the n-side of the diode D_2. So the diode D_2 is reversed biased during the positive half cycle and does not allow electric current through it.

The diode D_1 supplies DC current to the load R_L. The DC current produced at the load R_L will return to the secondary winding through a centre tap. Thus, during the positive half cycle of the input AC signal, only diode D_1 allows electric current while diode D_2 does not allow electric current.

During the negative half cycle of the input AC signal, terminal A become negative, terminal B become positive and centre tap is grounded (zero volts). The negative terminal A is connected to

the p-side of the diode D_1 and the positive terminal B is connected to the n-side of the diode D_1. So the diode D_1 is reversed biased during the negative half cycle and does not allow electric current through it. On the other hand, the positive terminal B is connected to the p-side of the diode D_2 and the negative terminal A is connected to the n-side of the diode D_2. So the diode D_2 is forward biased during the negative half cycle and allows electric current through it.

The diode D_2 supplies DC current to the load R_L. The DC current produced at the load R_L will return to the secondary winding through a centre tap.

Thus, the diode D_1 allows electric current during the positive half cycle and diode D_2 allows electric current during the negative half cycle of the input AC signal. As a result, both half cycles (positive and negative) of the input AC signal are allowed. So the output DC voltage is almost equal to the input AC voltage.

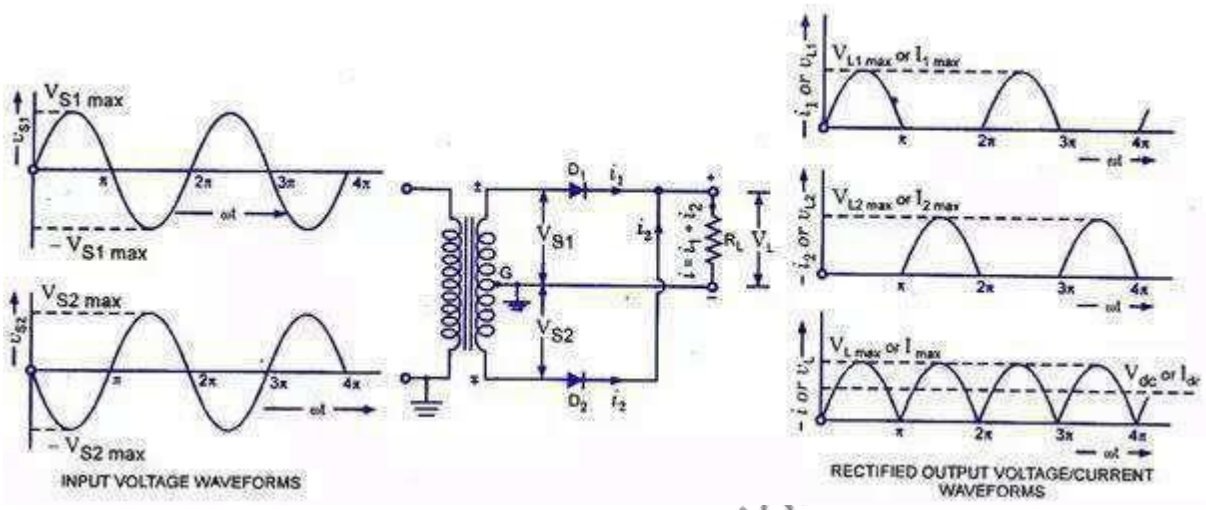


Figure.2.16. Centre Tapped Full Wave Rectifier

2.5.3. The bridge rectifier:

The Bridge rectifier is a circuit, which converts an ac voltage to dc voltage using both half cycles of the input ac voltage. The Bridge rectifier circuit is shown in the following figure. The circuit has four diodes connected to form a bridge. The ac input voltage is applied to the diagonally opposite ends of the bridge. The load resistance is connected between the other two ends of the bridge. For the positive half cycle of the input ac voltage, diodes D1 and D2 conduct, whereas diodes D3 and D4 remain in the OFF state. The conducting diodes will be in series with the load resistance RL and hence the load current flows through RL. For the negative half cycle of the input ac voltage, diodes D3 and D4 conduct whereas, D1 and D2 remain OFF. The conducting diodes D3 and D4 will be in series with the load resistance RL and hence the current flows through RL in the same direction as in the previous half cycle. Thus a bi-directional wave is converted into a unidirectional wave.

Figure.2.17. Bridge Rectifier

2.5.4. Ripple factor

The effectiveness of a rectifier depends upon the magnitude of ac component in the output; smaller the ac component, the more effective is the rectifier. Ripple factor is a measure of effectiveness of a rectifier circuit and defined as a ratio of RMS value of ac component to the dc component in the rectifier output. The output DC signal with very fewer ripples is considered as the smooth DC signal while the output DC signal with high ripples is considered as the high pulsating DC signal.

Ripple factor is mathematically defined as the ratio of ripple voltage to the pure DC voltage. The ripple factor for a bridge rectifier is given by

$$\gamma = \sqrt{\left(\frac{V_{rms}}{V_{DC}}\right)^2 - 1}$$

$$Ripple factor = \frac{I_{ac}}{I_{dc}} \qquad I_{rms} = \sqrt{I_{dc}^2 + I_{ac}^2} \qquad \frac{I_{ac}}{I_{dc}} = \sqrt{\frac{I_{rms}^2}{I_{dc}^2} - 1}$$

For half wave rectifier: $I_{rms} = \frac{I_m}{2}$ $I_{dc} = \frac{I_m}{\Pi}$ Ripple factor = 1.21

For full wave rectifier: $I_{rms} = \frac{I_m}{\sqrt{2}}$ $I_{dc} = \frac{2I_m}{\Pi}$ Ripple factor = 0.48

- Efficiency in rectifiers is equal to the ratio of output DC power (i.e V_{dc}*I_{dc}) to the input power from the AC supply (I_{rms}^2.R)
- Efficiency of half wave rectifier is very low its approx 40.5 percent, because there is presence of very high magnitudes of ripples.
- For full wave rectifier ripple factor is very less and that's why efficiency is quite high i.e approx 81.2 percent.

2.5.5. Filters:

The output Direct Current (DC) produced by the half wave rectifier contains large ripples. This ripple voltage fluctuates with respect to time. So it is not suitable for practical applications. To overcome these problems, we use filters at the output. Even though we use filters at the output, the DC signal obtained at the output is not a pure DC. Furthermore, the power loss is high in half wave rectifier. The filter is an electronic device that converts the pulsating Direct Current into pure Direct Current.

The filter is made up of a combination of electronic components such as resistors, capacitors, and inductors. The property of inductor is that it allows the DC components and blocks the AC components. The property of a capacitor is that it allows the AC components and blocks the DC components.

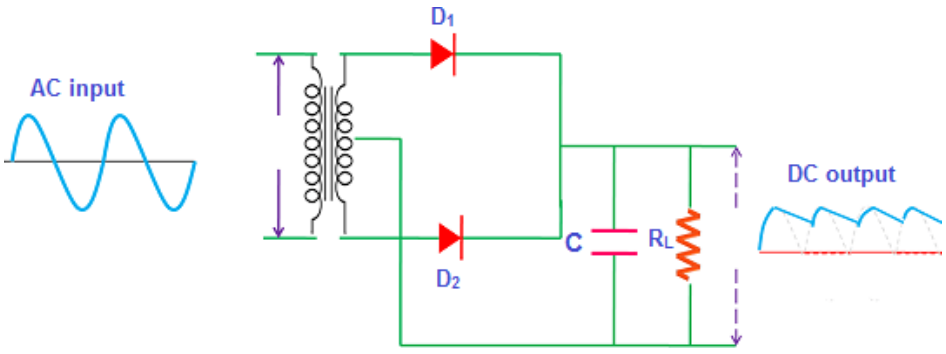


Figure.2.18. Full wave Rectifier with Capacitor filter

Working:

The main duty of the capacitor filter is to short the ripples to the ground and blocks the pure DC (DC components), so that it flows through the alternate path and reaches output load resistor R_L. When input AC voltage is applied, during the positive half cycle, the diode D_1 is forward biased and allows electric current whereas the diode D_2 is reverse biased and blocks electric current. On the other hand, during the negative half cycle the diode D_2 is forward biased (allows electric current) and the diode D_1 is reverse biased (blocks electric current).

The charging of the capacitor happens only when the applied AC voltage is greater than the capacitor voltage.

Initially, the capacitor is uncharged. That means no voltage exists between the plates of the capacitor. So when the voltage is turned on, the charging of the capacitor happens immediately.

During this conduction period, the capacitor charges to the maximum value of the input supply voltage. The capacitor stores a maximum charge exactly at the quarter positive half cycle in the waveform. At this point, the supply voltage is equal to the capacitor voltage.

When the AC voltage starts decreasing and becomes less than the capacitor voltage, then the capacitor starts slowly discharging.

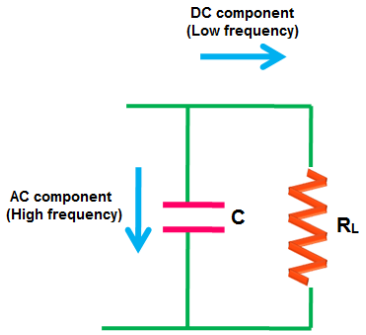
The discharging of the capacitor is very slow as compared to the charging of the capacitor. So the capacitor does not get enough time to completely discharge. Before the complete discharge of the capacitor happens, the charging again takes place. So only half or more than half of the capacitor charge get discharged.

2.5.6. How the capacitor filter removes the ripples in the signal

The pulsating Direct Current (DC) produced by the full wave rectifier contains both AC and DC components.

We know that the capacitor allows the AC components and blocks the DC components of the current. When the DC current that contains both DC components and AC components reaches the filter, the DC components experience a high resistance from the capacitor whereas the AC components experience a low resistance from the capacitor.

Electric current always prefers to flow through a low resistance path. So the AC components will flow through the capacitor whereas the DC components are blocked by the capacitor. Therefore, they find an alternate path and reach the output load resistor R_L. The flow of AC components through the capacitor is nothing but the charging of a capacitor. Thus, the filter converts the pulsating DC into pure DC.



2.6. Voltage Regulation:

Voltage regulation is "the ratio of voltage drop from no load to the full load to the no load voltage".

There are two ways to express the voltage regulation. One is voltage regulation up and another is voltage regulation down.

Consider formula for voltage regulation :

$$\%VR = \frac{V_{nl} - V_{fl}}{V_{nl}} \times 100$$

Here V_{nl} is the no load voltage and V_{fl} is the full load voltage.

2.6.1. Series voltage regulator

The series voltage regulator operates by using a variable element in series with the load. By changing the resistance of the series element, the voltage dropped across it can be varied to ensure that the voltage across the load remains constant.

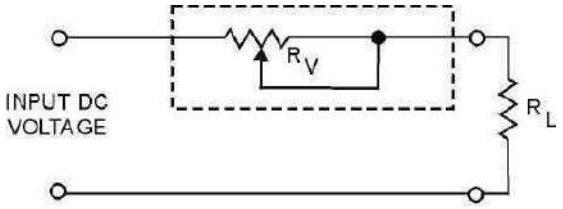


Figure.2.19.Series Regulator

The advantage of the series voltage regulator is that the amount of current drawn is effectively that used by the load, although some will be consumed by any circuitry associated with the regulator.

Unlike the shunt regulator, the series regulator does not draw the full current even when the load does not require any current. As a result the series regulator is considerably more efficient.

2.6.2. Shunt voltage regulator

The load is operated with a resistor in series with the voltage source and the shunt regulator then in parallel with the load.

In order to keep the voltage across the load constant, a level of current must be drawn through the series resistor to maintain the required voltage across the load. The load will take some and the remaining current is drawn by the shunt voltage regulator.

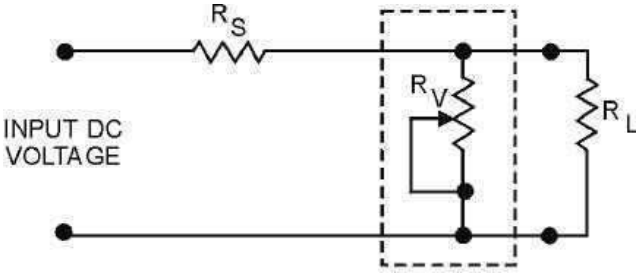


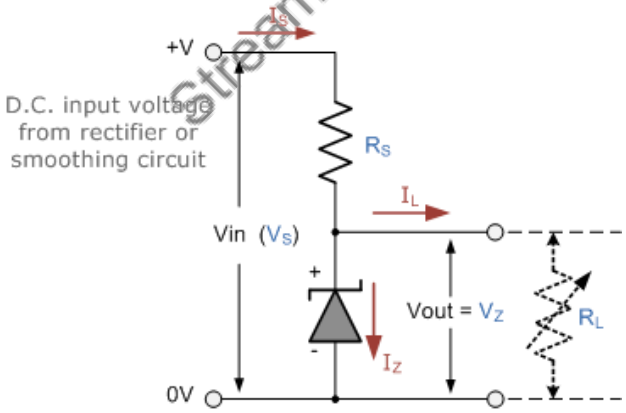
Figure.2.20. Shunt Regulator

The circuit is designed so that at maximum load current the shunt regulator draws virtually no current and at minimum load current, the shunt voltage regulator passes the full current.

As a result, it can be seen that shunt regulators are inefficient because maximum current is drawn from the source regardless of the load current, i.e. even when there is no load current.

2.6.2.1. Zener diode shunt regulator

The resistor, R_S is connected in series with the zener diode to limit the current flow through the diode with the voltage source, V_S being connected across the combination. The stabilised output voltage V_{out} is taken from across the zener diode. The zener diode is connected with its cathode terminal connected to the positive rail of the DC supply so it is reverse biased and will be operating in its breakdown condition. Resistor R_S is selected so to limit the maximum current flowing in the circuit.



Working:

With no load connected to the circuit, the load current will be zero, ($I_L = 0$), and all the circuit current passes through the zener diode which in turn dissipates its maximum power. Also a small value of the series resistor R_S will result in a greater diode current when the load resistance R_L is connected and large as this will increase the power dissipation requirement of the diode so care must be taken when selecting the appropriate value of series resistance so that the Zener maximum power rating is not exceeded under this no-load or high-impedance condition.

The load is connected in parallel with the zener diode, so the voltage across R_L is always the same as the zener voltage, ($V_R = V_Z$). There is a minimum zener current for which the stabilization of the voltage is effective and the zener current must stay above this value operating under load within

its breakdown region at all times. The upper limit of current is of course dependent upon the power rating of the device. The supply voltage V_S must be greater than V_Z.

Comparison of Series and Shunt regulators

Shunt voltages regulator	Series voltages regulator
Shunt voltage regulator has good voltage regulation even at high load currents.	Series voltage regulator has not so good voltage regulation at high load currents.
In the shunt voltage regulator the output DC voltage is constant.	In the series voltage regulator the output DC voltages is not constant.
Shunt voltage regulator is connected in shunt with the load.	Series voltages regulator is connected in series with the load.
Shunt voltages regulator has good efficiency for low load current.	It has good efficiency for higher load currents.
It is appropriate for light loads.	It is appropriate for heavy loads.
Shunt voltage regulator has poor voltage is constant.	Series voltages regulator has better voltage regulation.
The control element has to bear the load voltage across it. So, it is a high voltage low current device.	The control element has to carry the load current. So, it is a high current low voltage device.

2.7. Voltage Regulation using IC:

It is an integrated circuit whose basic purpose is to regulate the unregulated input voltage (definitely over a predefined range) and provide with a constant, regulated output voltage**.**

An IC based voltage regulator can be classified in different ways.

1. Three terminal voltage regulator and five or multi terminal voltage regulator.
2. Linear voltage regulator & switching voltage regulator.
3. Fixed voltage regulators (positive & negative) and adjustable voltage regulators (positive & negative)

2.7.1. Fixed Voltage Regulators

These regulators provide a constant output voltage. A popular example is the 7805 IC which provides a constant 5 volts output. A fixed voltage regulator can be a positive voltage regulator or a negative voltage regulator. A positive voltage regulator provides with constant positive output voltage. All those IC's in the 78XX series are fixed positive voltage regulators.

A negative fixed voltage regulator is same as the positive fixed voltage regulator in design, construction & operation. The only difference is in the polarity of output voltages. These IC's are designed to provide a negative output voltage. Example-7905, 7906 and all those IC's in the 79XX series.

2.7.2. Adjustable Voltage Regulator

An adjustable voltage regulator is a kind of regulator whose regulated output voltage can be varied over a range. There are two variations of the same; known as positive adjustable voltage regulator and negative adjustable regulator. LM317 is a classic example of positive adjustable voltage regulator, whose output voltage can be varied over a range of 1.2 volts to 57 volts. LM337 is an example of negative adjustable voltage regulator.

Subject Name- Electronics Device **Subject Code**: EC303

Unit III

Fundamentals of BJT: Construction, basic operation, current components and equations,CB, CE and CC configuration, input and output characteristics, Early effect, Region of operations: active, cut-off and saturation region. BJT as an amplifier.

Ebers-Moll model, Power dissipation in transistor (Pd, max rating), Photo transistor. Transistor biasing circuits and analysis: Introduction, various biasing methods: Fixed bias, Self bias, Voltage Divider bias, Collector to base bias, Load-line analysis: DC and AC analysis, Operating Point and Bias Stabilization and Thermal Runaway, Transistor as a switch.

3.1. Bipolar Junction Transistor (BJT)

The BJT is a device which has three ohmic contacts to the three different semiconductor layers that are connected together. Basically, the BJT structure consists of a series connection of a pn and np or np and pn diode where the n-regions, respectively p-regions, of both diodes overlap. This makes a pnp and npn BJT. The fusion of the two diodes produces a three layer, two junctions, and three terminal device forming the basis of a Bipolar Junction Transistor**,** or BJT for short.

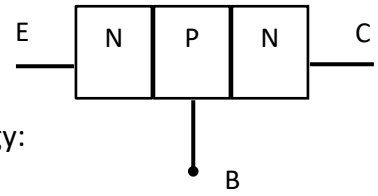
Transistors are three terminal active devices made from different semiconductor materials that can act as either an insulator or a conductor by the application of a small signal voltage. The transistor's ability to change between these two states enables it to have two basic functions: "switching" (digital electronics) or "amplification" (analogue electronics).

The word Transistor is a combination of the two words Transfer resistor which describes their mode of operation way back in their early days of electronics development. There are two basic types of bipolar transistor construction, PNP and NPN, which basically describes the physical arrangement of the P-type and N-type semiconductor materials from which they are made.

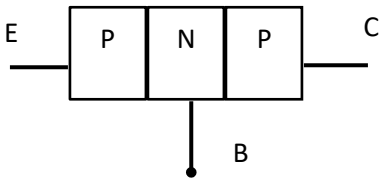
Construction: The Bipolar Transistor basic construction consists of two PN-junctions producing three connecting terminals with each terminal being given a name to identify it from the other two. These three terminals are known and labelled as the Emitter (E), the Base (B) and the Collector (C) respectively. Bipolar Transistors are current regulating devices that control the amount of current flowing through them in proportion to the amount of biasing voltage applied to their base terminal acting like a current-controlled switch. The principle of operation of the two transistor types PNP and NPN, is exactly the same the only difference being in their biasing and the polarity of the power supply for each type.

3.2. Bipolar Transistor Construction

Physical construction:

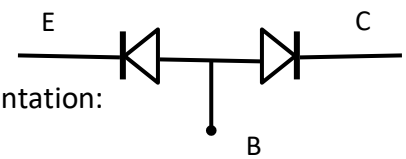


NPN

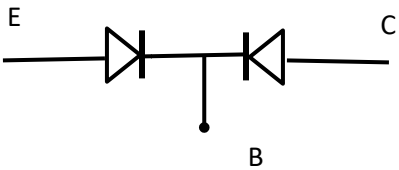


PNP

Two diode analogy:

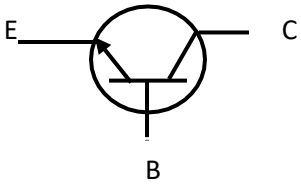


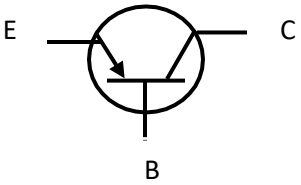
NPN



PNP

Symbol representation:





The construction and circuit symbols for both the PNP and NPN bipolar transistor are given above with the arrow in the circuit symbol always showing the direction of "conventional current flow" between the base terminal and its emitter terminal. The direction of the arrow always points from the positive P-type region to the negative N-type region for both transistor types, exactly the same as for the standar l.

3.3. Transistor biasing

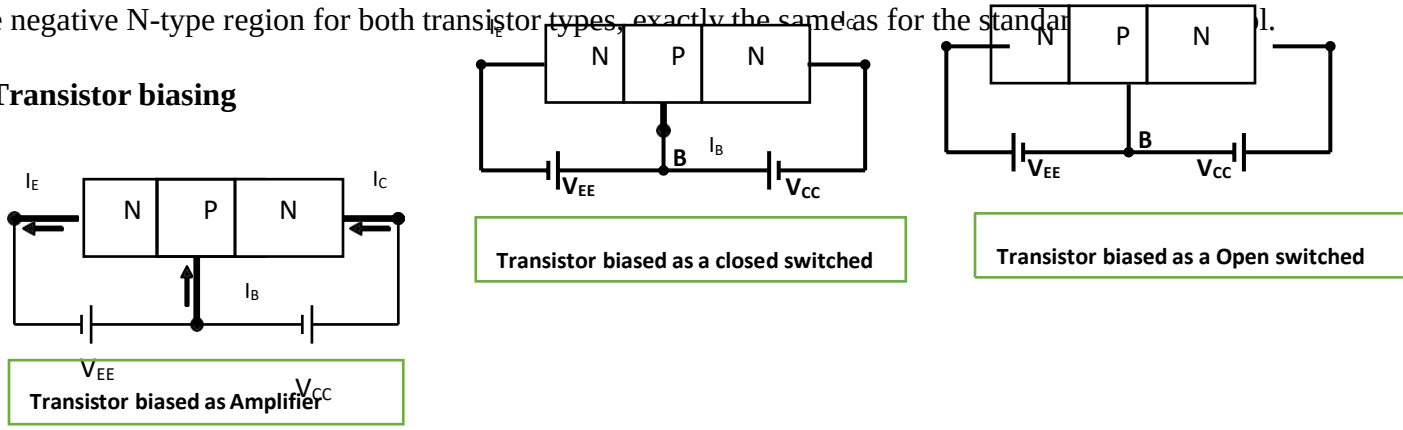


Figure.3.1. Transistor biasing in different modes

If a transistor has to work as an amplifier, the base-emitter junction J_1 must be forward biased and the collector-base junction J_2 must be reverse biased. Transistor biasing is a process of creating an appropriate potential difference across the base-emitter and the collector-base junctions. The base-emitter junction should always be forward biased by a voltage greater than its cut-in voltage (V_λ), while the collector-base junction should be sufficiently reverse biased for efficient collection of charges. If these two conditions are satisfied, the transistor provides faithful amplification while operating in the active region (linear region).

A transistor can also operate as a switch (in the non-linear regions). If both the emitter-base & collector-base junctions are forward biased then the transistor will behave as a closed switch offering almost zero resistance (saturation region). If both the emitter-base & collector-base junctions are reverse biased then the transistor behaves as an open switch offering very high resistance (cut-off region).

3.4. Calculating the currents in a BJT

In case of forward active mode, the currents in the emitter base diode determine all the BJT currents completely. The holes that are diffusing through the base will be collected by the collector and thus make the collector current. The electrons that are escaping from the base into the emitter have to be re-supplied by the base current, thus the electron current of the E-B diode defines the base current. The emitter current is the total current in the E-B diode. This gives the well known result:

$$\boldsymbol{I_E = I_B + I_C}$$

Figure.3.2. Left: A PNP BJT symbol with the directions of the different currents. Right: An NPN BJT symbol with the direction of current.

Apply nodal analysis (sum of current into node = sum of currents out of node) in the base node of fig.5:

For PNP BJT: $I_E = I_C + I_B$

For NPN BJT: $I_C + I_B = I_E$

The bipolar transistors have the ability to operate within three different regions:

- Active Region – the transistor operates as an amplifier and Ic = β.Ib
- Saturation – the transistor is "Fully-ON" operating as a switch and Ic = I(saturation)
- Cut-off – the transistor is "Fully-OFF" operating as a switch and Ic = 0

3.5. Transistor configurations:

A transistor has only 3 leads hence any one of the 3 leads has to be common to the input & output circuits if the transistor is to be considered as a 2-port linear network. Depending on the lead that is common to both the input & output circuits there are three transistor configurations:

1. Common-base configuration or Grounded-base configuration
2. Common-emitter configuration or Grounded-emitter configuration
3. Common-collector configuration or Grounded-collector configuration

The behavior of a transistor varies greatly with each configuration & can be understood by studying the input & output characteristics in all the 3 configurations.

3.5.1. Common base configuration

Figure shows the circuit arrangement for obtaining the input and output characteristics of a NPN transistor in common-base configuration. V_{EE} is the emitter battery on the input side and R_E is the emitter current limiting resistor. The milliammeter is used to measure the emitter current (input current) while the voltmeter is used to measure the input voltage V_{BE}. V_{CC} is the collector battery on the output side and R_C is the collector resistance.

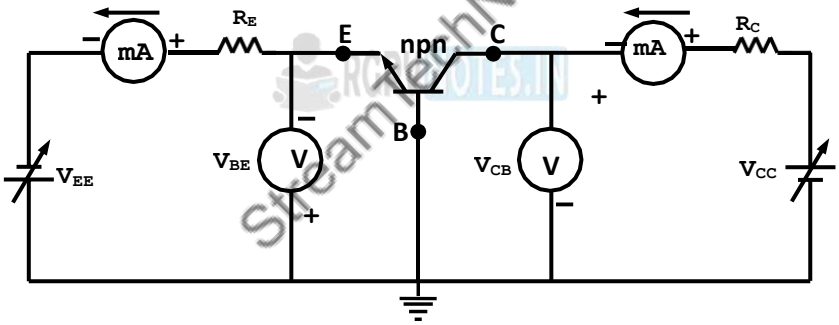


Figure.3.3. Common base configuration

The milliammeter measures the collector current (output current) while the voltmeter measures the collector-base voltage, V_{CB} (output voltage). Here the base lead is common to both the input and output circuits, hence it is known as the common-base configuration (has Voltage Gain but no Current Gain).

The behaviour of the NPN-transistor in CB configuration:

- The forward biased base-emitter (BE) PN-junction allows the free electrons in emitter to go through the PN-junction to arrive at the base, forming the emitter current I_E.
- As the P-type base is thin and lightly doped, only a small number of the electrons from the emitter are combined with the holes in base to form the base current I_B.
- Most of the electrons coming from the emitter become minority carriers in the P-type base, and they go through the reverse biased collector-base PN junction to arrive at the collector.
- The percentage of those electrons that arrive at the collector out of the electrons from the emitter is defined as α, depending on the doping and geometry of the material. The total collector current I_C is therefore $I_C = \alpha I_E$.

The *current gain* or *current transfer ratio* is defined as the ratio between the emitter (input) current and the collector (output) current : $I_C = \alpha I_E$

The base current I_B is given as:

$$I_B = I_E - I_C \approx I_E - \alpha I_E = (1-\alpha) I_E, \quad \text{i.e.} \quad I_E = \frac{1}{1-\alpha} I_B$$

The CB configuration can be considered as a 2-port circuit. The input port is formed by the emitter and base, the output port is formed by the collector and base. The relationships between the current and voltage of both the input and output ports are described by the following input and output characteristics.

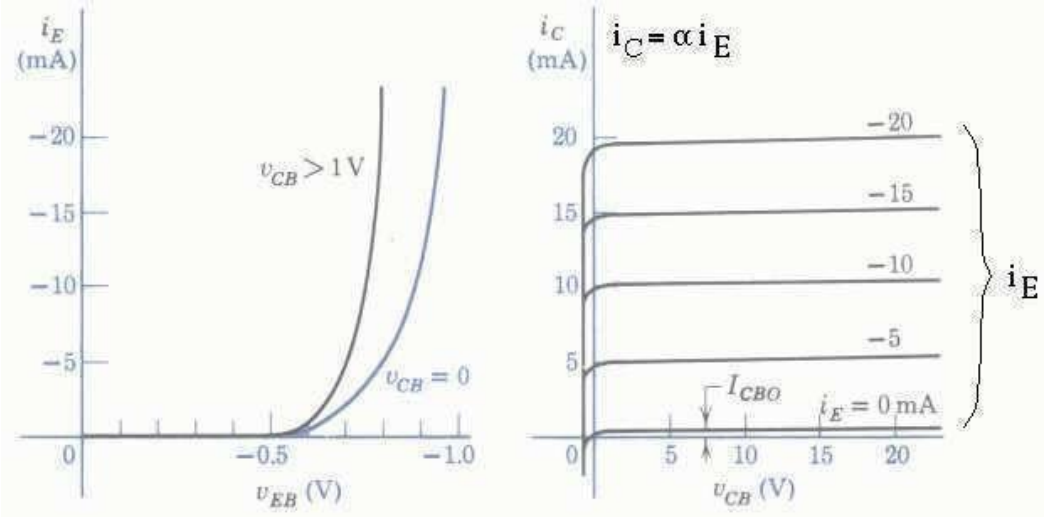


Figure.3.4. Input and Output characteristics of CB configured BJT

3.5.2. Common emitter configuration

Figure 1.19 shows the circuit diagram for a transistor in common emitter configuration. Battery V_{BB} is used to forward bias the base-emitter junction. The microammeter measures the input current I_B and the voltmeter measures the input voltage V_{BE}. Battery V_{CC} is used to reverse bias the collector- base junction (V_{CC}>V_{BB}).

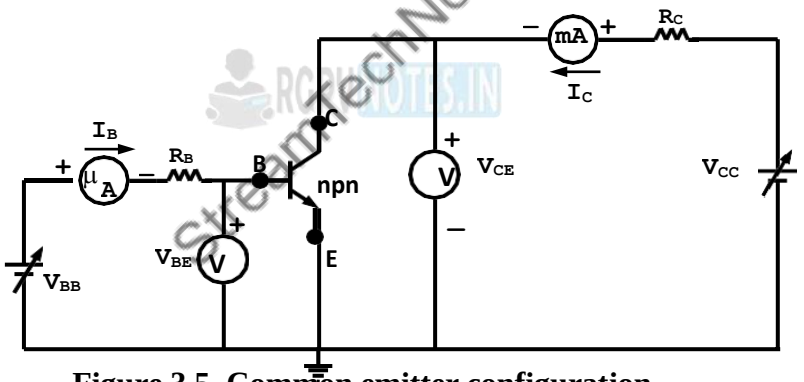


Figure.3.5. Common emitter configuration

The milliammeter is used to measure the output current I_C while the voltmeter measures the output voltage V_{CE}. R_B is the base resistor and R_C is the collector resistor. Here the emitter lead is common to both the input and output circuits, hence it is known as common emitter configuration (has both Current and Voltage Gain). A transistor in common-emitter configuration is used as a voltage amplifier, power amplifier and multi-stage amplifier.

Analysis of circuit:

The base current I_B is treated as the input current, and the collector current I_C is treated as the output current: $I_C = \alpha I_E = \alpha(I_C + I_B)$

Solving this equation for I_C, we get the relationship between the output I_C and the input current I_B:

$$I_C = \frac{\alpha}{1-\alpha} I_B = \beta I_B$$

Where we have defined the CE *current gain*, the ratio of the output current I_C and the input current I_B:

$$\beta = \frac{\alpha}{1-\alpha} \approx \frac{I_C}{I_B}$$

The two parameters α and β are related by any of the following:

$$\beta = \frac{\alpha}{1-\alpha}, \qquad \alpha = \frac{\beta}{1+\beta}, \qquad 1+\beta = \frac{1}{1-\alpha}, \qquad 1-\alpha = \frac{1}{1+\beta}$$

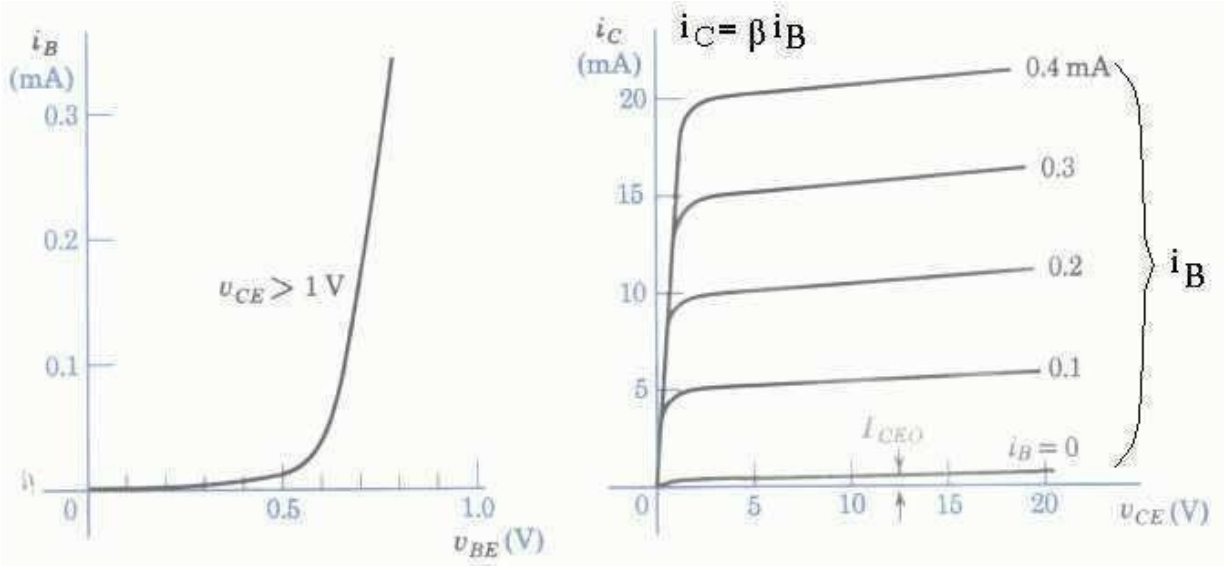


Figure.3.6. Input and Output characteristics of CE configured BJT

3.5.3. Common collector configuration

Figure 1.21 shows the circuit diagram for a NPN transistor in common collector configuration. Battery V_{BB} is used to reverse bias the collector base junction. The microammeter measures input current I_B and the voltmeter measures input voltage V_{CB}. Battery V_{EE} along with V_{BB} is used to forward bias the base- emitter junction (V_{EE} is at lower potential than V_{BB}).

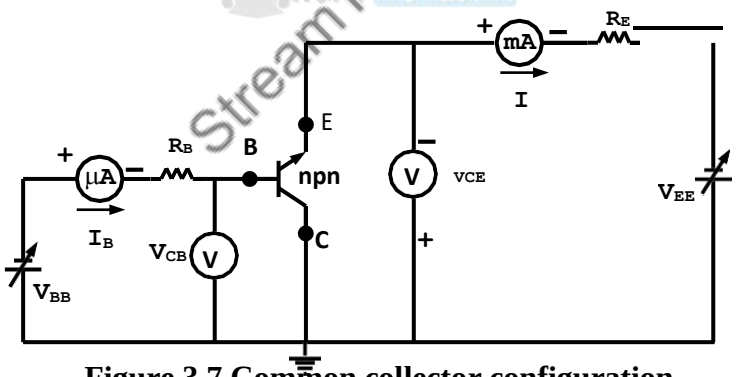


Figure.3.7.Common collector configuration

The milliammeter is used to measure output current I_E , while the voltmeter measures the output voltage V_{CE}. (I_E is the output current and V_{CE} is the output voltage).R_B is the base resistor and R_E is the emitter resistor. Here the collector lead is common to both the input and output circuits, hence it is known as common-collector configuration (has Current Gain but no Voltage Gain). It is used as a buffer amplifier to provide excellent impedance matching between two stages. The circuit is commonly known as an Emitter follower.

Bipolar Transistor Characteristics: The static characteristics for a **Bipolar Transistor** can be divided into the following three main groups.

Input Characteristics:-	Common Base -	$\Delta V_{EB} / \Delta I_E$
	Common Emitter -	$\Delta V_{BE} / \Delta I_B$
Output Characteristics:-	Common Base -	$\Delta V_C / \Delta I_C$
	Common Emitter -	$\Delta V_C / \Delta I_C$
Transfer Characteristics:-	Common Base -	$\Delta I_C / \Delta I_E$
	Common Emitter -	$\Delta I_C / \Delta I_B$

Table.3.1.BJT Characteristic Summary

Characteristic	Common Base	Common Emitter	Common Collector
Input Impedance	Low	Medium	High
Output Impedance	Very High	High	Low
Phase Angle	0^o	180^o	0^o
Voltage Gain	High	Medium	Low
Current Gain	Low	Medium	High
Power Gain	Low	Very High	Medium

3.6. Load line biasing method

In the above figure, the output characteristics are drawn between collector current I_C and collector voltage V_{CE} for different values of base current I_B. These are considered here for different input values to obtain different output curves.

3.6.1. Operating point

When a value for the maximum possible collector current is considered, that point will be present on the Y-axis, which is nothing but the saturation point. As well, when a value for the maximum possible collector emitter voltage is considered, that point will be present on the X-axis, which is the cutoff point.
When a line is drawn joining these two points, such a line can be called as Load line. This is called so as it symbolizes the output at the load. This line, when drawn over the output characteristic curve, makes contact at a point called as Operating point.
This operating point is also called as quiescent point or simply Q-point. There can be many such intersecting points, but the Q-point is selected in such a way that irrespective of AC signal swing, the transistor remains in active region.
AC load Line: The load line has to be drawn in order to obtain the Q-point. A transistor acts as a good amplifier when it is in active region and when it is made to operate at Q-point, faithful amplification is achieved. Faithful amplification is the process of obtaining complete portions of input signal by increasing the signal strength. This is done when AC signal is applied at its input. The AC load line gives the peak-to-peak voltage, or the maximum possible output swing for a given amplifier.

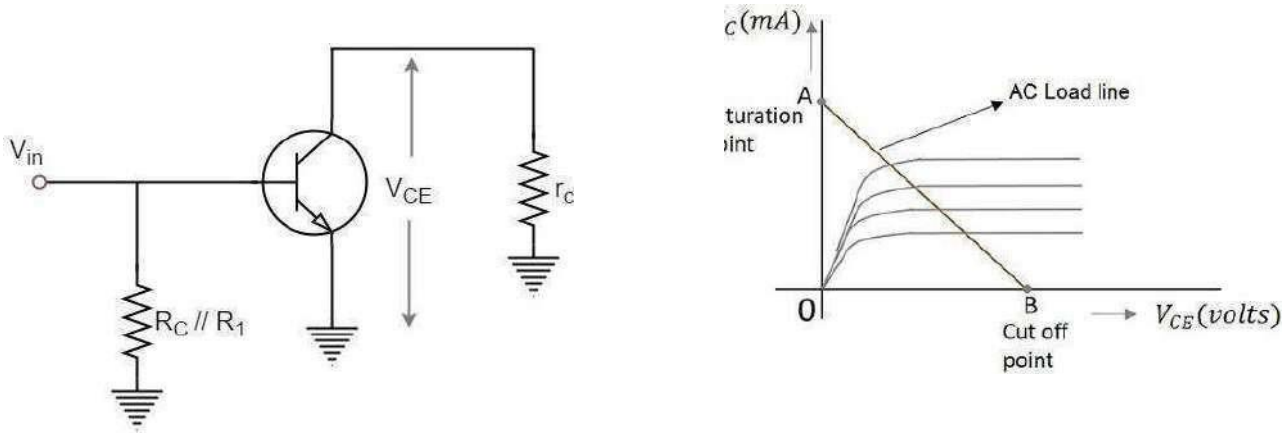


Figure.3.8. AC equivalent circuit of a CE amplifier and AC Load line

From the above figure,

$V_{CE}=(R_C \text{ ll } R_1)\times I_C$

$r_C=R_C \text{ ll } R_1$

For a transistor to operate as an amplifier, it should stay in active region. The quiescent point is so chosen in such a way that the maximum input signal excursion is symmetrical on both negative and positive half cycles.

Hence,

$V_{max}=V_{CEQ}$ and $V_{min}=-V_{CEQ}$

Where V_{CEQ} is the emitter-collector voltage at quiescent point

The following graph represents the AC load line which is drawn between saturation and cut off points.

The end points of AC load line are

$I_{C(sat)}=I_{CQ}+V_{CEQ}/(R_C \text{ ll } R_1)$

$V_{CE(off)}=V_{CEQ}+I_{CQ}*(R_C \text{ ll } R_1)$

3.6.2. DC Load line

When the transistor is given the bias and no signal is applied at its input, the load line drawn at such condition can be understood as DC condition. Here there will be no amplification as the signal is absent. The circuit will be as shown below.

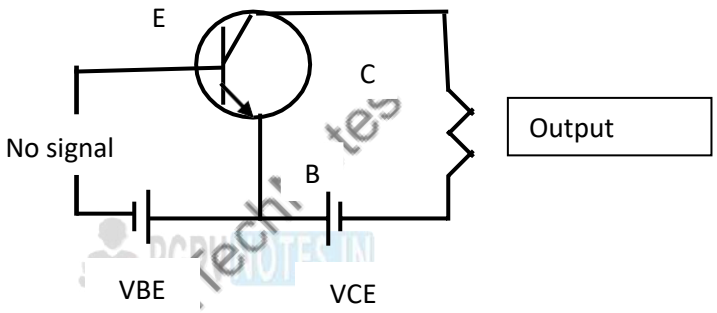


Figure.3.9. DC load line circuit

The value of collector emitter voltage at any given time will be

$V_{CE}=V_{CC}-I_cR_C$

As V_{CC} and R_C are fixed values, the above one is a first degree equation and hence will be a straight line on the output characteristics. This line is called as D.C. Load line. The figure below shows the DC load line.

To obtain the load line, the two end points of the straight line are to be determined. Let those two points be A and B.

To obtain A

When collector emitter voltage V_{CE} = 0, the collector current is maximum and is equal to V_{CC}/R_C. This gives the maximum value of V_{CE}. This is shown as

$V_{CE}=V_{CC}-IcR_C$

$0=V_{CC}-Ic\ R_C$

$I_C=V_{CC}/R_C$

This gives the point A (OA = V_{CC}/R_C) on collector current axis, shown in the figure.

To obtain B: When the collector current IC = 0, then collector emitter voltage is maximum and will be equal to the V_{CC}. This gives the maximum value of IC. This is shown as

$V_{CE}=V_{CC}-I_CR_C$

$V_{CE}=V_{CC}$ (As I_C = 0)

This gives the point B, which means (OB = V_{CC}) on the collector emitter voltage axis shown in the above figure. Hence we got both the saturation and cutoff point determined and learnt that the load line is a straight line. So, a DC load line can be drawn. The importance of this operating point is further understood when an AC signal is given at the input.

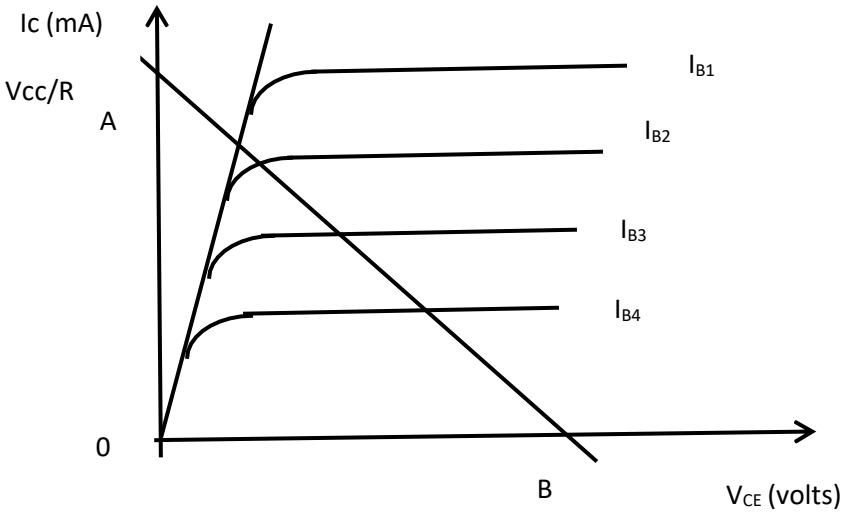


Figure.3.10. Load line analysis

3.6.3. Early Effect

This effect occurring in bipolar transistors is named after its discoverer J.M. Early. In a BJT, Early effect corresponds to the modulation of the emitter & collector currents by the collector-base voltage $V_{CB.}$ Early effect arises from the variation of the base width 'w' with the reverse voltage V_{CB} across the collector-base junction & exists in both static & high frequency characteristics. Early effect is more prominent in BJTs with narrow base widths.

Early effect or base width modulation is the variation in the actual width of the base region in a BJT due to a variation in the applied base-collector voltage. With an increase in the collector-base voltage the collector- base depletion width increases thereby decreasing the effective base width. The base-emitter depletion width is unchanged because there is no change in the base-emitter voltage. The narrowing of the base region results in reduced recombination & an increase in minority carrier injection into the collector region. This causes an increase in the current amplification factor α & hence an increase in the output or collector current due to an increase in collector-base voltage. Another damaging effect due to an increase in collector-base reverse voltage is the phenomenon of 'Punch-Through' or 'Reach-Through' which causes voltage breakdown of the transistor depending on the circuit configuration.

3.6.4. Relationship between α and β

α is the current gain of a transistor in common-base configuration and is given by the relation,

$\alpha = \Delta I_C / \Delta I_E$

β is the current gain of a transistor in common-emitter configuration and is given by the relation,

$\beta = \Delta I_C / \Delta I_B$

α in terms of β

The basic transistor equation is given by:

$I_E = I_B + I_C$ .....(a)

Considering the incremental values, we have

$\Delta I_E = \Delta I_B + \Delta I_C$ .....(b)

Divide equation (b) throughout by ΔI_C,

ie. $(\Delta I_E / \Delta I_C) = (\Delta I_B / \Delta I_C) + (\Delta I_C / \Delta I_C)$ ..... (c)

But $(\Delta I_C / \Delta I_E) = \alpha \Rightarrow (\Delta I_E / \Delta I_C) = (1 / \alpha)$

$(\Delta I_C / \Delta I_B) = \beta \Rightarrow (\Delta I_B / \Delta I_C) = (1 / \beta)$

ie. $(1/\alpha) = (1 / \beta) + 1$ ..... (d)

ie. $(1 / \alpha) = (1+ \beta) / \beta$

Taking the reciprocal we have: $\alpha = [\beta / (\beta + 1)]$

β in terms of α

From equation **(d)**, we have

$1 / \alpha = 1 + (1 / \beta) \Rightarrow 1/\beta = (1/\alpha) - 1$. ie. $(1/\beta) = (1-\alpha)/\alpha$

$\Rightarrow \therefore \beta = [\alpha / (1-\alpha)]$

3.7. Transistor as an amplifier:

The most common amplifier configuration for an NPN transistor is that of the Common Emitter Amplifier circuit. Transistor amplifiers operate using AC signal inputs which alternate between a positive value and a negative value so some way of "presetting" the amplifier circuit to operate between these two maximum or peak values is required. This is achieved using a process known as **Biasing**. Biasing is very important in amplifier design as it establishes the correct operating point of the transistor amplifier ready to receive signals, thereby reducing any distortion to the output signal. We saw that a static or DC load line can be drawn onto the output characteristics curves to show all the possible operating points of the transistor from fully "ON" to fully "OFF", and to which the quiescent operating point or **Q-point** of the amplifier can be found.

The aim of any small signal amplifier is to amplify all of the input signal with the minimum amount of distortion possible to the output signal, in other words, the output signal must be an exact reproduction of the input signal but only bigger (amplified). To obtain low distortion when used as an amplifier the operating quiescent point needs to be correctly selected. This is in fact the DC operating point of the amplifier and its position may be established at any point along the load line by a suitable biasing arrangement.

The best possible position for this Q-point is as close to the centre position of the load line as reasonably possible, thereby producing Vce = 1/2Vcc. Consider the **Common Emitter Amplifier** circuit shown below.

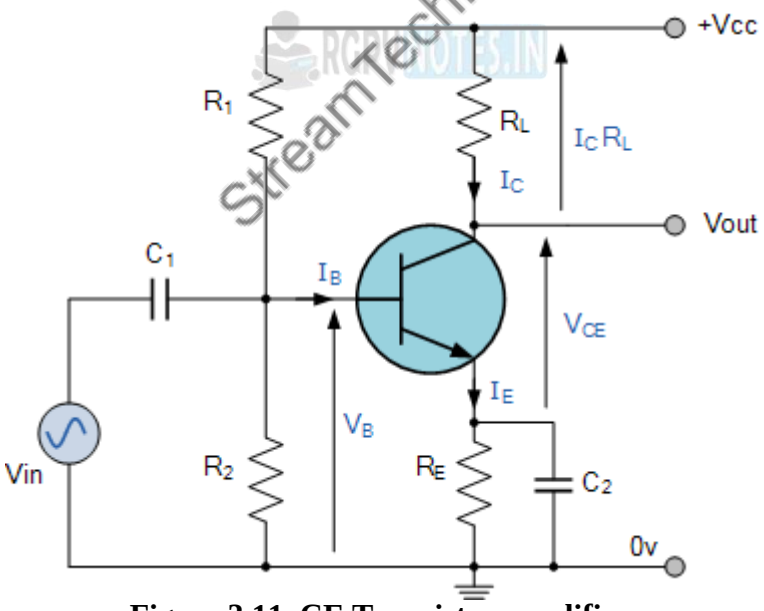


Figure.3.11. CE Transistor amplifier

3.7.1. Amplifier Analysis:

The single stage common emitter amplifier circuit shown above uses what is commonly called "Voltage Divider Biasing". This type of biasing arrangement uses two resistors as a potential divider network across the supply with their centre point supplying the required Base bias voltage to the transistor. Voltage divider biasing is commonly used in the design of bipolar transistor amplifier circuits.

This method of biasing the transistor greatly reduces the effects of varying Beta, (β) by holding the Base bias at a constant steady voltage level allowing for best stability. The quiescent Base voltage (V_b) is determined by the potential divider network formed by the two resistors, R_1, R_2 and the power supply voltage Vcc as shown with the current flowing through both resistors.

Figure.3.12. Voltage division part of amplifier

Then the total resistance R_T will be equal to $R_1 + R_2$ giving the current as $i = Vcc/R_T$. The voltage level generated at the junction of resistors R_1 and R_2 holds the Base voltage (V_b) constant at a value below the supply voltage. Then the potential divider network used in the common emitter amplifier circuit divides the supply voltage in proportion to the resistance. This bias reference voltage can be easily calculated using the simple voltage divider formula below:

Transistor Bias Voltage

$$\mathbf{V_B} = \frac{V_{cc}R_2}{R_1+R_2}$$

The same supply voltage, (V_{cc}) also determines the maximum Collector current, Ic when the transistor is switched fully "ON" (saturation), $V_{ce} = 0$. The Base current I_b for the transistor is found from the Collector current, Ic and the DC current gain Beta, β of the transistor.

Waveform: The sinusoidal voltage at the base produces a base current that varies above and below the Q-point on the ac load line, as shown by the arrows.

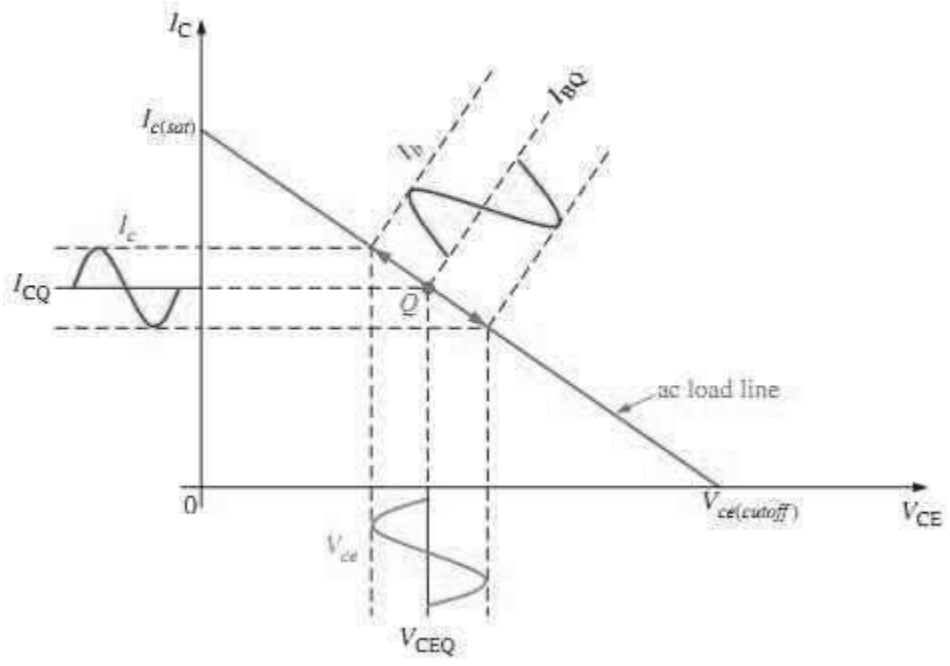


Figure.3.13. Graphical picture of CE amplifier characteristics

3.8. Amplifier Parameters:

3.8.1. Gain

The gain of an amplifier is a measure of the "Amplification" of an amplifier, i.e. how much it increases the amplitude of a signal. More precisely it is the ratio of the output signal amplitude to the input signal amplitude, and is given the symbol "A". It can be calculated for voltage (A_v), current (A_i) or power (A_p).

- Voltage gain A_v = Amplitude of output voltage /Amplitude of input voltage= V_o/Vi
- Current gain A_i = Amplitude of output current / Amplitude of input current = I_o/I_i
- Power gain A_p = Signal power out /Signal power in = P_o/ P_i

3.8.2. Frequency Response

Amplifiers do not have the same gain at all frequencies. For example, an amplifier designed for audio frequency amplification will amplify signals with a frequency of less than about 20kHz but will not amplify signals having higher frequencies. An amplifier designed for radio frequencies will amplify a band of frequencies above about 100kHz but will not amplify the lower frequency audio signals.
In each case the amplifier has a particular frequency response, being a band of frequencies where it provides adequate amplification, and excluding frequencies above and below this band, where the amplification is less than adequate.

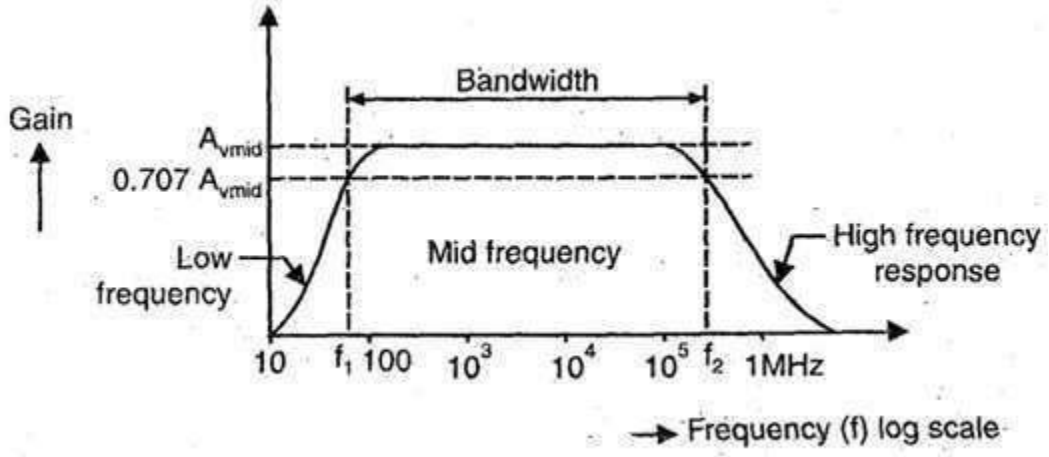


Figure.3.14. Frequency response of amplifier

To show how the gain of an amplifier varies with frequency, a graph, showing the frequency response of the amplifier is used. Fig. 1.33 shows the typical frequency response curve of an audio amplifier. In such graphs, it is common that very large values may be encountered for both gain and frequency. For this reason it is usual for both the frequency and gain axes of the graph to use logarithmic scales. It can be seen from Figure that scales on the (horizontal) x-axis do not increase in a linear manner; each equal division represents a tenfold increase in the frequency plotted. This ensures that a very wide range of frequency can be plotted on a single graph. The (vertical) y-axis uses linear divisions but logarithmic units (deciBels dB). The curve of the graph shows how gain, measured in deciBels, varies with frequency.

3.8.3. Bandwidth

An important piece of information that can be obtained from a frequency response curve is the Bandwidth of the amplifier. This refers to the 'band' of frequencies for which the amplifier has a useful gain. Outside this useful band the gain of the amplifier is considered to be insufficient compared with the gain at the centre of the bandwidth. Bandwidth specified for voltage amplifiers is the range of frequencies for which the amplifier's gain is greater than 0.707 of the maximum gain. The useful bandwidth in Fig. 1.33 would be described as extending to those frequencies at which the voltage gain is −3dB down compared to the gain at the mid band frequency.

3.9. Transistor Biasing Circuits:

3.9.1. Need for transistor biasing:

If the o/p signal must be a faithful reproduction of the i/p signal, the transistor must be operated in active region. That means an operating point has to be established in this region . To establish an operating point (proper values of collector current I_c and collector to emitter voltage V_{CE}) appropriate supply voltages and resistances must be suitably chosen in the ckt. This process of selecting proper supply voltages and resistance for obtaining desired operating point or Q point is called as biasing and the ckt used for transistor biasing is called as biasing ckt.

There are four conditions to be met by a transistor so that it acts as a faithful ampr:

1) Emitter base junction must be forward biased (V_{BE}=0.7Vfor Si, 0.2V for Ge) and collector base junction must be reverse biased for all levels of i/p signal.
2) V_{ce} voltage should not fall below $V_{CE\,(sat)}$ (0.3V for Si, 0.1V for Ge) for any part of the i/p signal. For V_{CE} less than $V_{CE\,(sat)}$ the collector base junction is not probably reverse biased.

3) The value of the signal I_c when no signal is applied should be at least equal to the max. collector current t due to signal alone.
4) Max. rating of the transistor $I_{c(max)}$, $V_{CE\,(max)}$ and $P_{D(max)}$ should not be exceeded at any value of i/p signal.

The Q point is fixed properly, to ensure that the operating point remains stable where it is originally fixed. If the Q point shifts, the output voltage and current get clipped, thereby o/p signal is distorted.

In practice, the Q-point tends to shift its position due to any or all of the following three main factors.

1) Reverse saturation current, Ico, which doubles for every 10°C raise in temperature
2) Base emitter Voltage ,VBE, which decreases by 2.5 mV per °C
3) Transistor current gain, h_{FE} or β which increases with temperature.

3.9.2. Stability Factor (S):

The rise of temperature results in increase in the value of transistor gain β and the leakage current Ico. So, I_C also increases which results in a shift in operating point. Therefore, The biasing network should be provided with thermal stability. Maintenance of the operating point is specified by S, which indicates the degree of change in operating point due to change in temperature.

The extent to which I_C is stabilized with varying I_C is measured by a stability factor S

$$S = \frac{I_c}{I_{co}} \approx \frac{dI_c}{dI_{co}} \approx \frac{\Delta I_c}{\Delta I_{co}}, \beta \text{ and } I_B \text{ constant}$$

For CE configuration $I_C = \beta I_B + (1+\beta) I_C$

Differentiate the above equation w.r.t I_C , We get

$$1 = \beta \frac{dI_B}{dI_C} + (1+\beta)\frac{dI_c}{dI_c}$$

$$\therefore \quad (1 - \beta \frac{dI_B}{dI_C}) = \frac{(\beta+1)}{S}$$

$$\therefore \quad S = \frac{1+\beta}{1-\beta\frac{dI_B}{dI_C}}$$

S should be small to have better thermal stability.

Stability factor S' and S'':

S' is defined as the rate of change of I_C with V_{BE}, keeping I_C and V_{BE} constant.

$$S' = \frac{I_c}{V_{BE}}$$

S'' is defined as the rate of change of I_C with β, keeping I_{CO} and V_{BE} constant.

$$S'' = \frac{I_c}{\beta}$$

3.9.3. Methods of Transistor Biasing:

3.9.3.1. Fixed bias (base bias): As shown in figure 3.15 is also called *base bias*. In the fig 3.15 shown, the single power source (for example, a battery) is used for both collector and base of a transistor, although separate batteries can also be used.

In the given circuit,

$V_{cc} = I_B R_B + V_{be}$

Therefore, $I_B = (V_{cc} - V_{be})/R_B$

Since the equation is independent of current $I_C R$, $dI_B/dI_C R = 0$ and the stability factor is given by the equation….. reduces to

$$S = 1 + \beta$$

Since β is a large quantity, this is very poor biasing circuit. Therefore in practice the circuit is not used for biasing.

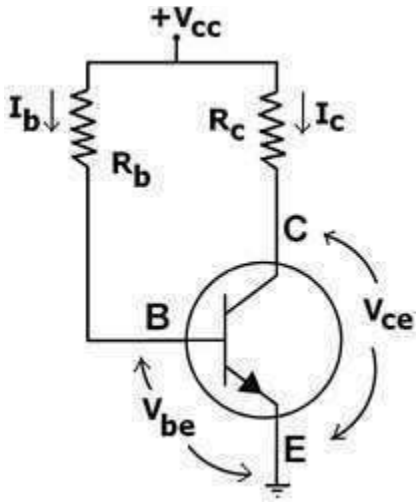


Figure.3.15. Fixed Bias Circuit

For a given transistor, V_{be} does not vary significantly during use. As V_{cc} is of fixed value, on selection of R_B, the base current I_B is fixed. Therefore this type is called *fixed bias* type of circuit.

Also for given circuit, $V_{cc} = I_C R_C + V_{ce}$

Therefore, $V_{ce} = V_{cc} - I_C R_C$

Merits:

- It is simple to shift the operating point anywhere in the active region by merely changing the base resistor (R_B).
- A very small number of components are required.

Demerits:

- The collector current does not remain constant with variation in temperature or power supply voltage. Therefore the operating point is unstable.
- Changes in V_{be} will change I_B and thus cause R_E to change. This in turn will alter the gain of the stage.
- When the transistor is replaced with another one, considerable change in the value of β can be expected. Due to this change the operating point will shift.

3.9.3.2. Emitter-Feedback Bias:

The emitter feedback bias circuit is shown in the fig 3.16. The fixed bias circuit is modified by attaching an external resistor to the emitter. This resistor introduces negative feedback that stabilizes the Q-point. From Kirchhoff's voltage law, the voltage across the base resistor is

$V_{Rb} = V_{CC} - I_e R_e - V_{be}$.

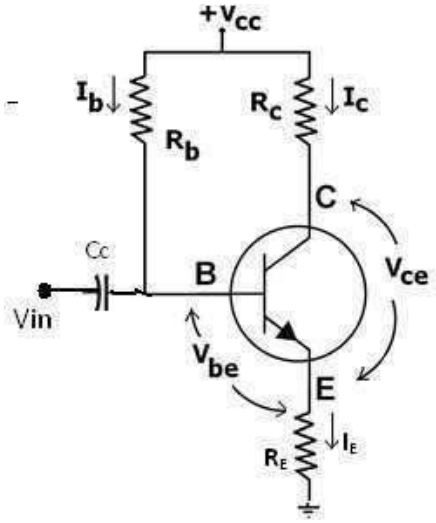


Figure.3.16. Emitter feedback Bias

From Ohm's law, the base current is

$I_b = V_{Rb} / R_b$.

The way feedback controls the bias point is as follows. If V_{be} is held constant and temperature increases, emitter current increases. However, a larger I_e increases the emitter voltage $V_e = I_eR_e$, which in turn reduces the voltage V_{Rb} across the base resistor. A lower base-resistor voltage drop reduces the base current, which results in less collector current because $I_c = ß\ I_B$. Collector current and emitter current are related by $I_c = \alpha\ I_e$ with $\alpha \approx 1$, so increase in emitter current with temperature is opposed, and operating point is kept stable.

Similarly, if the transistor is replaced by another, there may be a change in I_C (corresponding to change in β-value, for example). By similar process as above, the change is negated and operating point kept stable.

For the given circuit,

$I_B = (V_{CC} - V_{be})/(R_B + (\beta+1)R_E)$.

Merits:

The circuit has the tendency to stabilize operating point against changes in temperature and β-value.

Demerits:

- In this circuit, to keep I_C independent of β the following condition must be met:

$$I_C = \beta I_B = \frac{\beta(V_{CC} - V_{be})}{R_B + (\beta + 1)R_E} \approx \frac{(V_{CC} - V_{be})}{R_E}$$

which is approximately the case if $(\beta + 1)R_E >> R_B$.

- As β-value is fixed for a given transistor, this relation can be satisfied either by keeping R_E very large, or making R_B very low.
- If R_E is of large value, high V_{CC} is necessary. This increases cost as well as precautions necessary while handling.
- If R_B is low, a separate low voltage supply should be used in the base circuit. Using two supplies of different voltages is impractical.
- In addition to the above, R_E causes ac feedback which reduces the voltage gain of the amplifier.

3.9.3.3. Collector to Base Bias or Collector Feed-Back Bias:

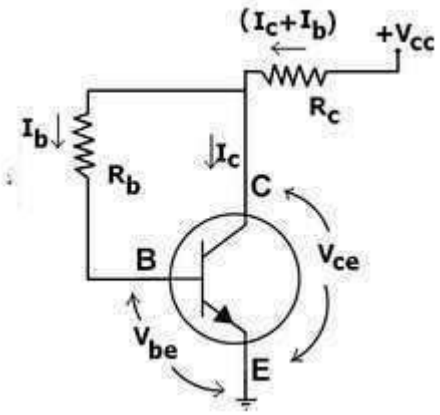


Figure.3.17. Collector feedback bias

This configuration shown in fig 3.17 employs negative feedback to prevent thermal runaway and stabilize the operating point. In this form of biasing, the base resistor R_B is connected to the collector instead of connecting it to the DC source V_{cc}. So any thermal runaway will induce a voltage drop across the R_C resistor that will throttle the transistor's base current.

From Kirchhoff's voltage law, the voltage V_{R_b}across the base resistor R_b is

$$V_{R_b} = V_{cc} - \overbrace{(I_c + I_b)R_c}^{\text{Voltage drop across } R_c} - \overbrace{V_{be}}^{\text{Voltage at base}}.$$

By the Ebers–Moll model, $I_c = \beta I_b$, and so

$$V_{R_b} = V_{cc} - (\overbrace{\beta I_b}^{I_c} + I_b)R_c - V_{be} = V_{cc} - I_b(\beta + 1)R_c - V_{be}.$$

From Ohm's law, the base current $I_b = V_{R_b}/R_b$, and so

$\overbrace{I_b R_b}^{V_{R_b}} = V_{cc} - I_b(\beta + 1)R_c - V_{be}$.

Hence, the base current I_b is

$$I_b = \frac{V_{cc} - V_b}{R_b + (\beta + 1)R_c}$$

If V_{be} is held constant and temperature increases, then the collector current I_c increases. However, a larger I_c causes the voltage drop across resistor R_c to increase, which in turn reduces the voltage V_{R_b} across the base resistor R_b. A lower base-resistor voltage drop reduces the base current I_b, which results in less collector current I_c. Because an increase in collector current with temperature is opposed, the operating point is kept stable.

Merits:

- Circuit stabilizes the operating point against variations in temperature and β (i.e. replacement of transistor)

Demerits:

In this circuit, to keep I_c independent of β, the following condition must be met:

$$I_c = \beta I_b = \frac{\beta(V_{cc} - V_b)}{R_b + R_c + \beta R_c} \sim \frac{(V_{cc} - V_b)}{R_c}$$

which is the case when $\beta R_c >> R_b$

- As β-value is fixed (and generally unknown) for a given transistor, this relation can be satisfied either by keeping R_c fairly large or making R_b very low.
- If R_c is large, a high V_{cc} is necessary, which increases cost as well as precautions necessary while handling.
- If R_b is low, the reverse bias of the collector–base region is small, which limits the range of collector voltage swing that leaves the transistor in active mode.
- The resistor R_b causes an AC feedback, reducing the voltage gain of the amplifier. This undesirable effect is a trade-off for greater Q-point stability.

Usage: The feedback also decreases the input impedance of the amplifier as seen from the base, which can be advantageous. Due to the gain reduction from feedback, this biasing form is used only when the trade-off for stability is warranted.

3.9.3.4. Collector –Emitter Feedback Bias:

The below fig 3.18 shows the collector –emitter feedback bias circuit that can be obtained by applying both the collector feedback and emitter feedback. Here the collector feedback is provided by connecting a resistance RB from the collector to the base and emitter feedback is provided by connecting an emitter Re from emitter to ground. Both feed backs are used to control collector current and base current IB in the opposite direction to increase the stability as compared to the previous biasing circuits.

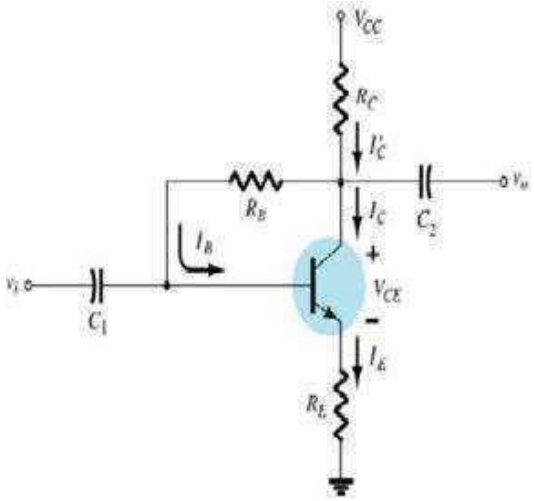


Figure.3.18. Collector –Emitter Feedback Bias

3.9.3.5. Voltage Divider Bias or Self Bias Or Emitter Bias

The voltage divider as shown in the fig 4.7 is formed using external resistors R_1 and R_2. The voltage across R_2 forward biases the emitter junction. By proper selection of resistors R_1 and R_2, the operating point of the transistor can be made independent of β. In this circuit, the voltage divider holds the base voltage fixed independent of base current provided the divider current is large compared to the base current. However, even with a fixed base voltage, collector current varies with temperature (for example) so an emitter resistor is added to stabilize the Q-point, similar to the above circuits with emitter resistor.

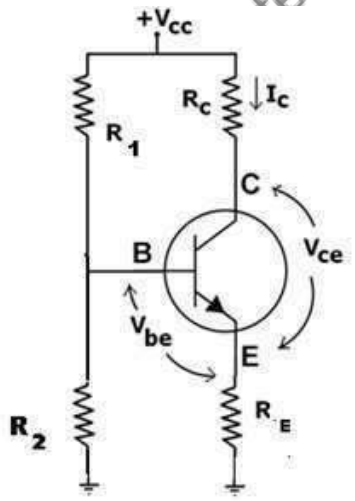


Figure.3.19.Voltage divider bias

In this circuit the base voltage is given by:

V_B= voltage across $R_2 = V_{cc}\frac{R_2}{(R_1+R_2)} - I_B\frac{R_1R_2}{(R_1+R_2)}$

$\sim V_{cc}=\frac{R_2}{(R_1+R_2)}$ provided $I_B << I_2 = V_B/ R_2$

Also $V_B = V_{be} + I_E R_E$

For the given circuit,

$$I_B = \frac{\frac{V_{CC}}{1+R_1/R_2} - V_{be}}{(\beta+1)R_E + R_1 \parallel R_2}.$$

Let the current in resistor R1 is I1 and this is divided into two parts – current through base and resistor R2. Since the base current is very small so for all practical purpose it is assumed that I1 also flows through R2, so we have

$I_1 = \frac{V_{cc}}{R_1+R_2}$

$V_2 = \frac{R_1+R_2}{V_{cc}} R_2$

Applying KVL in the circuit, we have

$V_2 = V_{BE} + V_E$

$V_2 = V_{BE} + I_E R_E$

$I_E = \frac{V_2 - V_{BE}}{R_E}$

$I_C = \frac{V_2 - V_{BE}}{R_E}$ (since $I_c \sim I_E$)

$I_C = \frac{\frac{cc}{R_1+R_2} R_2 - V_{BE}}{R_E}$

It is apparent from above expression that the collector current is independent of β thus the stability is excellent. In all practical cases the value of V_{BE} is quite small in comparison to the V_2, so it can be ignored in the above expression so the collector current is almost independent of the transistor parameters thus this arrangement provides excellent stability.

Again applying KVL in collector circuit, we have

$V_{cc} = I_c R_c + V_{CE} + I_E R_E$

$I_c \sim = I_E$

$V_{cc} = I_c R_c + V_{CE} + I_c R_E$

$V_{CE} = Vcc - Ic(Rc+R_E)$

The resistor RE provides stability to the circuit. If the current through the collector rises, the voltage across the resistor RE also rises. This will cause VCE to increase as the voltage V2 is independent of collector current. This decreases the base current, thus collector current increases to its former value.

Merits:

- Unlike above circuits, only one dc supply is necessary.
- Operating point is almost independent of β variation.
- Operating point stabilized against shift in temperature.

Demerits:

- In this circuit, to keep I_C independent of β the following condition must be met:

$$I_C = \beta I_B = \beta \frac{\frac{V_{CC}}{1+R_1/R_2} - V_{be}}{(\beta+1)R_E + R_1 \parallel R_2} \approx \frac{\frac{V_{CC}}{1+R_1/R_2} - V_{be}}{R_E},$$

which is approximately the case if $(\beta+1)R_E >> R_1 \parallel R_2$

where $R_1 \parallel R_2$ denotes the equivalent resistance of R_1 and R_2 connected in parallel.

- As β-value is fixed for a given transistor, this relation can be satisfied either by keeping R_E fairly large, or making $R_1 \| R_2$ very low.
- If R_E is of large value, high V_{CC} is necessary. This increases cost as well as precautions necessary while handling.
- If $R_1 \parallel R_2$ is low, either R_1 is low, or R_2 is low, or both are low. A low R_1 raises V_B closer to V_C, reducing the available swing in collector voltage, and limiting how large R_C can be made without driving the transistor out of active mode. A low R_2 lowers V_{be}, reducing the allowed collector current. Lowering both resistor values draws more current from the power supply and lowers the input resistance of the amplifier as seen from the base.
- AC as well as DC feedback is caused by R_E, which reduces the AC voltage gain of the amplifier. A method to avoid AC feedback while retaining DC feedback is discussed below.

Usage: The circuit's stability and merits as above make it widely used for linear circuits.

3.10. Thermal Runaway:

The collector current for the CE circuit is given by $I_C = \beta I_B + (1 + \beta) I_C$. The three variables in the equation, β, I_B, and I_C increases with rise in temperature. In particular, the reverse saturation current or leakage current I_C changes greatly with temperature. Specifically it doubles for every 10°C rise in temperature. The collector current $I_C$causes the collector base junction temperature to rise which in turn, increase I_C , as a result I_C will increase still further, which will further rise the temperature at the collector base junction. This process will become cumulative leading at the collector base junction. This process will become cumulative leading to *"thermal runaway"*. Consequently, the ratings of the transistor are exceeded which may destroy the transistor itself.

The collector is made larger in size than the emitter in order to help the heat developed at the collector junction. However if the circuit is designed such that the base current I_B is made to decrease automatically with rise in temperature, then the decrease in βI_B will compensate for increase in the $(1 + \beta) I_C$, keeping I_C almost constant.

3.11. Ebers Moll Model:

The bipolar junction transistor can be considered essentially as two pn junctions placed back-to-back, with the base p-type region being common to both diodes. This can be viewed as two diodes having a common third terminal as shown in Fig.3.20.

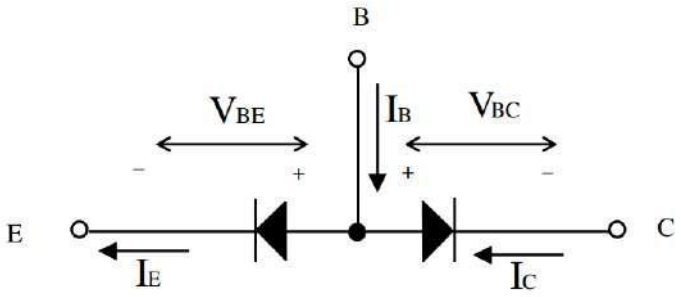


Figure.3.20.BJT as two back-to-back PN junction diode

The Ebers-Moll transistor model is an attempt to create an electrical model of the device as two diodes whose currents are determined by the normal diode law but with additional transfer ratios to quantify the interdependency of the junctions as shown in Fig. 3.21. Two dependent current sources are used to indicate the interaction of the junctions. The interdependency is quantified by the forward and reverse transfer ratios, αF and αR. The diode currents are given as:

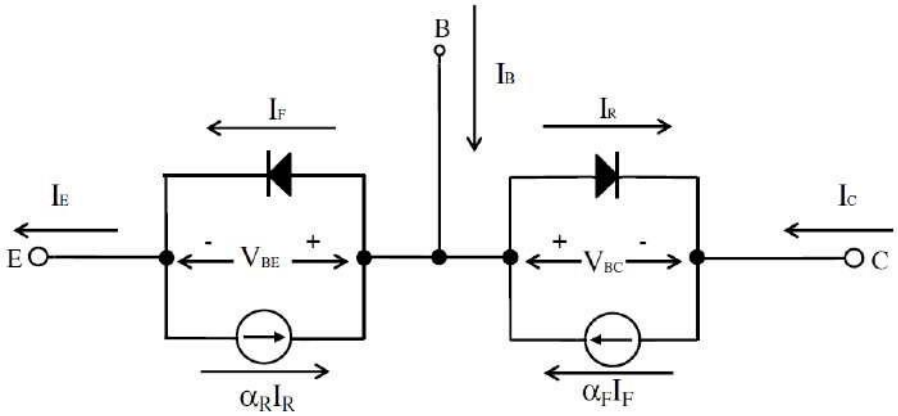


Figure.3.21. Ebers moll Model

$I_F = I_{ES} (e^{V_{BE}/V_T} - 1)$

$I_R = I_{CS} (e^{V_{BC}/V_T} - 1)$

Applying Kirchoff's laws to the model gives the terminal currents as:

$I_E = I_F - \alpha_R I_R$

$I_C = \alpha_F I_F - I_R$

$I_B = I_E - I_C$

This Gives:

$I_E = I_{ES} (e^{V_{BE}/V_T} - 1) - \alpha_R I_{CS} (e^{V_{BC}/V_T} - 1)$

$I_C = \alpha_F I_{ES} (e^{V_{BE}/V_T} - 1) - I_{CS} (e^{V_{BC}/V_T} - 1)$

$I_B = (1- \alpha_F) I_{ES} (e^{V_{BE}/V_T} - 1) + (1 -\alpha_R) I_{CS} (e^{V_{BC}/V_T} - 1)$

These are called the Ebers-Moll Equations for the bipolar transistor.

3.12. Phototransistors:

The phototransistor is a device that is able to sense light levels and alter the current flowing between emitter and collector according to the level of light it receives.

Phototransistors and photodiodes can both be used for sensing light, but the phototransistor is more sensitive in view of the gain provided by the transistor. This makes phototransistors more suitable in a number of applications.

Phototransistor operation

The phototransistor uses the basic transistor concept as the basis of its operation. In fact a phototransistor can be made by exposing the semiconductor of an ordinary transistor to light. The photo transistor operates because light striking the semiconductor frees electronics / holes and causes current to flow in the base region.

Photo transistors are operated in their active regime, although the base connection is generally left open circuit or disconnected because it is often not required. The base of the photo transistor would only be used to bias the transistor so that additional collector current was flowing and this would mask any current flowing as a result of the photo-action. For operation the bias conditions are quite simple. The collector of an n-p-n transistor is made positive with respect to the emitter or negative for a p-n-p transistor.

The light enters the base region where it causes hole electron pairs to be generated. This generation mainly occurs in the reverse biased base-collector junction. The hole-electron pairs move under the influence of the electric field and provide the base current, causing electrons to be injected into the emitter. As a result the photodiode current is multiplied by the current gain β of the transistor.

One of the drawbacks of the phototransistor is that is particularly slow and its high frequency response is very poor

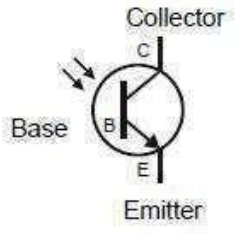


Figure.3.22. Symbol of phototransistor

Subject Name- Electronics Device **Subject Code**: EC303

Unit IV

Small Signal analysis: Small signal Amplifier, Amplifier Bandwidth, Hybrid model, analysis of transistor amplifier using h-parameter, Multistage Amplifier: Cascading amplifier, Boot-strapping Technique, Darlington amplifier and cascode amplifier, coupling methods in multistage amplifier, Low and high frequency response, Hybrid π model, Current Mirror circuits.

Large Signal analysis and Power Amplifiers: Class A, Class B, Class AB, Class C, Class D, Transformer coupled and Push-Pull amplifier.

4.1. Small Signal Amplifier:

Small signal condition: When the input signal (v_{in} and i_{in}) is small so that output signal (v_{out} and i_{out}) is confined in the active region of the output characteristics of the device, the device is operating in a condition of small signal. More specifically, the condition of small signal are verified when the variations in output are so small that the parameter values of the device can be regarded as constant. In these conditions, the amplifiers can be analyzed using the small-signal models of the BJT. The small signal conditions occur for the first stages constituting an amplification system.

In conditions of the small signal, the amplifier can be considered linear. The output signal is proportional to the input signal. This property derives from the fact that the components of the circuit are described by linear equations.

4.2. Amplifier Consideration

For an amplifier circuit, the overall gain of the amplifier is an important consideration. CE Amplifier has voltage gain greater than unity and its voltage gain is further increased by cascading. The characteristics of CE amplifier are such that, this configuration is very suitable for cascading in amplifier circuits. Hence most of the amplifier circuits use CE configuration. It is shown in figure 4.1.

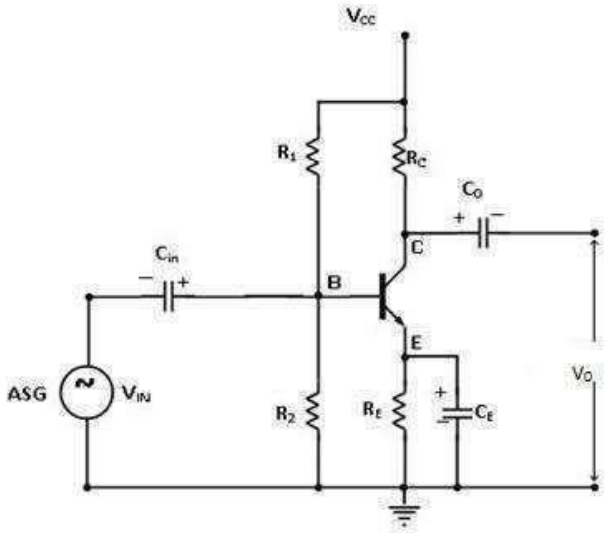


Figure.4.1. CE Amplifier

4.3. Role of Capacitors in Amplifiers

Other than the coupling purpose, there are other purposes for which few capacitors are especially employed in amplifiers.

4.3.1. Input Capacitor C_{in} : The input capacitor C_{in} present at the initial stage of the amplifier, couples AC signal to the base of the transistor. This capacitor C_{in} if not present, the signal source will be in parallel to resistor R_2 and the bias voltage of the transistor base will be change. Hence C_{in} allows, the AC signal from source to flow into input circuit, without affecting the bias conditions.

4.3.2. Emitter By-pass Capacitor C_e: The emitter by-pass capacitor C_e is connected in parallel to the emitter resistor. It offers a low reactance path to the amplified AC signal. In the absence of this capacitor, the voltage developed across RE will feedback to the input side thereby reducing the output voltage. Thus in the presence of C_e the amplified AC will pass through this.

4.3.3. Coupling Capacitor C_C: The capacitor CC is the coupling capacitor that connects two stages and prevents DC interference between the stages and controls the operating point from shifting. This is also called as blocking capacitor because it does not allow the DC voltage to pass through it. In the absence of this capacitor, RC will come in parallel with the resistance R1 of the biasing network of the next stage and thereby changing the biasing conditions of the next stage.

4.4. Amplifier Parameter:

- **Gain variation with frequency**: Because of the introduced reactive elements and the parasitic reactive elements the response of the amplifier is function of frequency.
- **Cut-off frequencies** The mid-band is delimited by two frequencies, the lower cut-off frequency f l (determined by coupling and by-pass capacitors) and the upper cut-off frequency fu (determined by the junction capacitance and the parasitic effects).
- **Amplifier bandwidth:**

The gain of an amplifier is affected by the capacitance associated with its circuit. This capacitance reduces the gain in both the low and high frequency ranges of operation.

- The reduction of gain in the low frequency band is due to the coupling and bypass capacitors selected. They are essentially short circuits in the mid and high bands.
- The reduction of gain in the high frequency band is due to the internal capacitance of the amplifying device, e.g., BJT, FET, etc.. This capacitance is represented by capacitors in the small signal equivalent circuit for these devices. They are essentially open circuits in the low and mid bands.

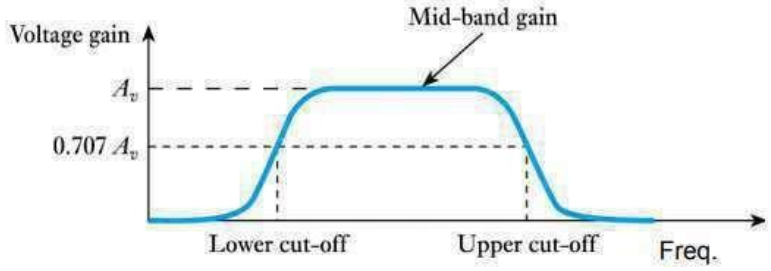


Figure.4.2.Frequency Response of CE amplifier

4.5. Hybrid (h) Parameter model:

The equivalent circuit of a transistor can be dram using simple approximation by retaining its essential features. These equivalent circuits will aid in analyzing transistor circuits easily and rapidly. If the input current i_1 and output Voltage V_2 are takes as independent variables, the input voltage V_1 and output current i_2 can be written as

$$v_1 = h_{11} i_1 + h_{12} v_2$$
$$i_2 = h_{21} i_1 + h_{22} v_2$$

Figure.4.3. Hybrid parameter model

The four hybrid parameters h_{11}, h_{12}, $h_{21}$and h_{22} are defined as follows:
h_{11}= [V_1/ i_1] with V_2= 0 Input Impedance with output port short circuited.
h_{22}= [i_2/ V_2] with i_1= 0 Output admittance with input port open circuited.
h_{12}= [V_1/ V_2] with i_1= 0 reverse voltage transfer ratio with input port open circuited.
h_{21}= [i_2/ i_1] with V_2= 0 Forward current gain with output port short circuited
The dimensions of h–parameters are as follows:
h_{11}-Ω
h_{22}–mhos
h_{12}, h_{21}–dimension less.
As the dimensions are not alike, they are hybrid in nature, and these parameters are called as hybrid parameters.

h_{11} = input; h_{22} = output; h_{21}= forward transfer; h_{22} = Reverse transfer.

The Hybrid Model for Two-port Network:

V_1= h_{11} i_1+ $h_{12}V_2$
I_2= $h_{21}i_1$+ $h_{22}V_2$

V_1= $h_i i_1$+ $h_r V_2$
I_2 = $h_f i_1$+ $h_0 V_2$

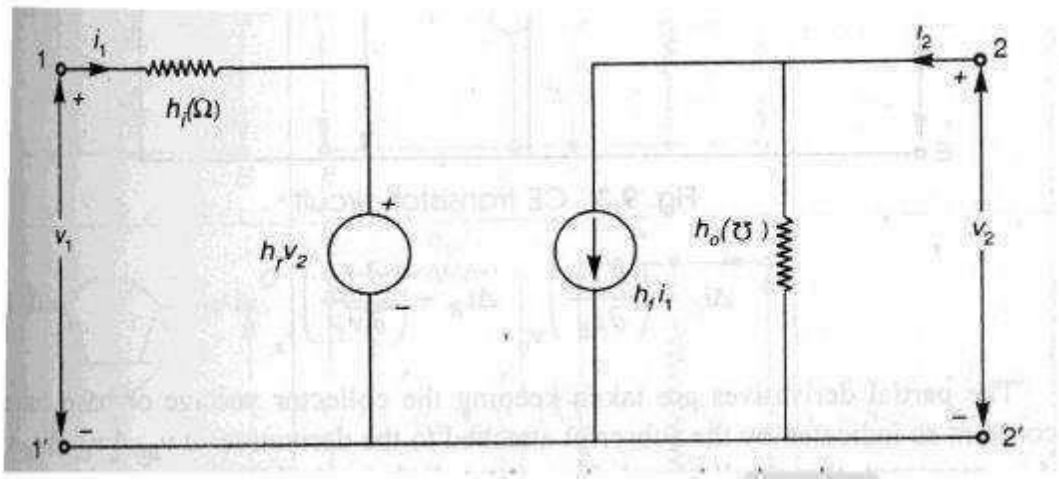


Figure.4.4.Hybrid model for two port network

4.6. Hybrid-Parameter Model for the CommonEmitter BJT

Notations used in transistor circuits:
h_{ie}= h11e= Short circuit input impedance
h_{oe}= h22e= Open circuit output admittance
h_{re} = h12e= Open circuit reverse voltage transfer ratio
h_{fe}= h21e= Short circuit forward current Gain.

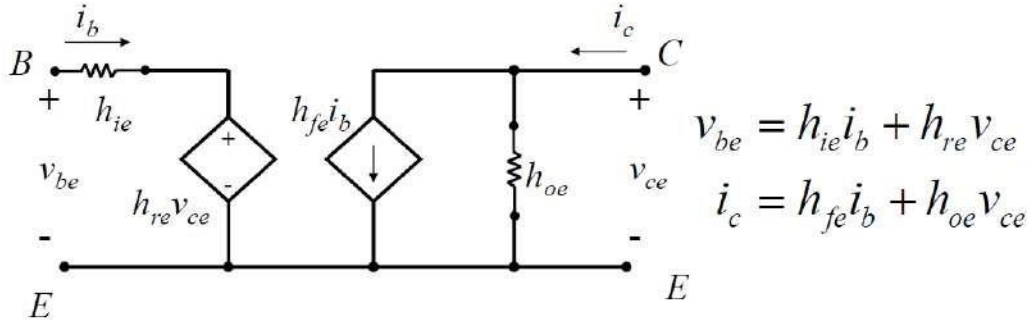


Figure.4.5. Hybrid model for CE amplifier

4.5. Multistage Amplifier:

In practical applications, the output of a single stage amplifier is usually insufficient, though it is a voltage or power amplifier. Hence they are replaced by Multi-stage transistor amplifiers. In Multi-stage amplifiers, the output of first stage is coupled to the input of next stage using a coupling device. These coupling devices can usually be a capacitor or a transformer. This process of joining two amplifier stages using a coupling device can be called as Cascading.

The following figure shows a two-stage amplifier connected in cascade.

4.3.1. Coupling in Multistage amplifiers:

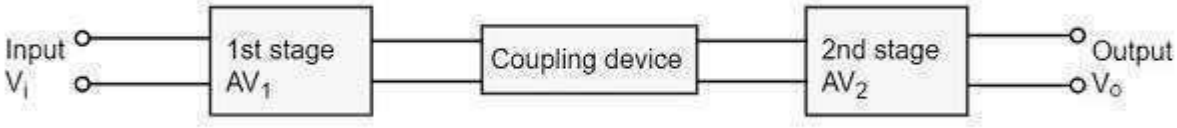


Figure.4.6. Multistage amplifier

The overall gain is the product of voltage gain of individual stages:

$A_V=A_{V1}\times A_{V2}=V_2/V_1\times V_0/V_2=V_0/V_1 A_V=A_{V1}\times A_{V2}$

Where A_V = Overall gain, A_{V1} = Voltage gain of 1st stage, and A_{V2} = Voltage gain of 2nd stage.

If there is n number of stages, the product of voltage gains of those **n** stages will be the overall gain of that multistage amplifier circuit.

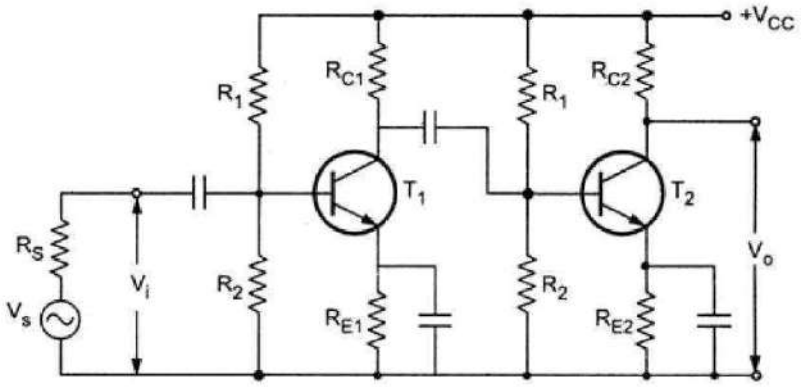


Figure.4.7. Two stage CE-CE cascade amplifier

4.3.2. Purpose and Types of coupling device:

The basic purposes of a coupling device are:

- To transfer the AC from the output of one stage to the input of next stage.
- To block the DC to pass from the output of one stage to the input of next stage, this means to isolate the DC conditions.

Joining one amplifier stage with the other in cascade; using coupling devices form a **Multi-stage amplifier circuit**. There are **four** basic methods of coupling, using these coupling devices such as resistors, capacitors, transformers etc. Let us have an idea about them.

4.3.2.1. Resistance-Capacitance Coupling

This is the mostly used method of coupling, formed using simple resistor-capacitor combination. The capacitor which allows AC and blocks DC is the main coupling element used here. The coupling capacitor passes the AC from the output of one stage to the input of its next stage. While blocking the DC components from DC bias voltages to affect the next stage

4.3.2.2. Impedance Coupling

The coupling network that uses inductance and capacitance as coupling elements can be called as Impedance coupling network. In this impedance coupling method, the impedance of coupling coil depends on its inductance and signal frequency which is $j\omega L$.

4.3.2.3. Transformer Coupling

The coupling method that uses a transformer as the coupling device can be called as Transformer coupling. There is no capacitor used in this method of coupling because the transformer itself conveys the AC component directly to the base of second stage. The secondary winding of the transformer provides a base return path and hence there is no need of base resistance. This coupling is mostly used because of its efficiency and its impedance matching and hence it is mostly used.

4.3.2.4. Direct Coupling

If the previous amplifier stage is connected to the next amplifier stage directly, it is called as direct coupling. The individual amplifier stage bias conditions are so designed that the stages can be directly connected without DC isolation. The direct coupling method is mostly used when the load is connected in series, with the output terminal of the active circuit element. For example, head-phones, loud speakers etc.

4.4. Boot-strapping Technique:

Bootstrapping (Using positive feedback to feed part of the output back to the input, but without causing oscillation) is a method of apparently increasing the value of a fixed resistor as it appears to A.C. signals, and thereby increasing input impedance. A basic bootstrap amplifier is shown in Fig. 4.4 where capacitor C_B is the 'Bootstrap Capacitor', which provides A.C. feedback to a resistor in series with the base. The value of C_B will be large, about 10 x the lowest frequency handled x the value of the series resistor ($10f_{min}R3$).

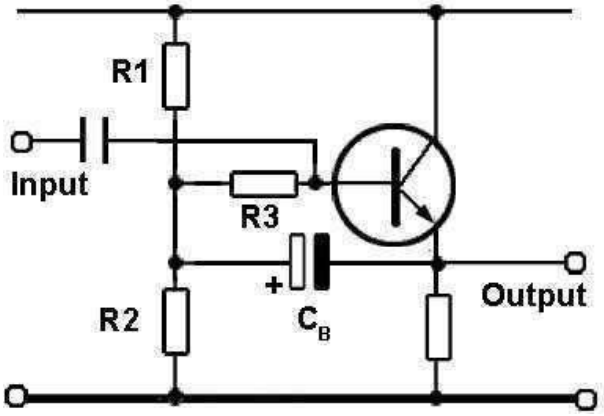


Figure.4.8 Bootstrapping applied to an Emitter Follower

Although positive feedback is being used, which would normally cause an amplifier to oscillate, the voltage gain of the emitter follower is less than 1, which prevents oscillation.

In Fig. 4.8 the base of the emitter follower is biased from a potential divider via R3. By feeding the output waveform back to the left hand side of R3 the voltage at this end of R3 is made to rise and fall in phase with the input signal at the base end of R3.

Because the output waveform of the emitter follower is a slightly less amplitude than the base waveform (due to the less than 1 gain of the transistor) there will be a very small signal current waveform across R3. Such a small current waveform suggests a very small current is flowing; therefore the resistance of R3 must be very high, much higher than in fact it is. The input impedance of the amplifier has therefore been increased.

The effective A.C. value of '3 is increased by '3 ÷ (1 −A_o) where A_o is the open loop gain of the amplifier.

The main drawback of this method of increasing input impedance compared with other methods is that the use of positive feedback is likely to increase noise and distortion.

4.5. Darlington amplifier

This transistor is also called as a Darlington pair, contains of two BJTs that are connected to deliver a high current gain from a low base current. In this transistor, the emitter of the input transistor is connected to the o/p of the base of the transistor and the collectors of the transistor are wired together. So, the input transistor amplifies the current even further amplifies by the o/p transistor. A Darlington transistor acts as a single transistor with high current gain, it means that a small amount of current is used from a microcontroller or a sensor to run a larger load.

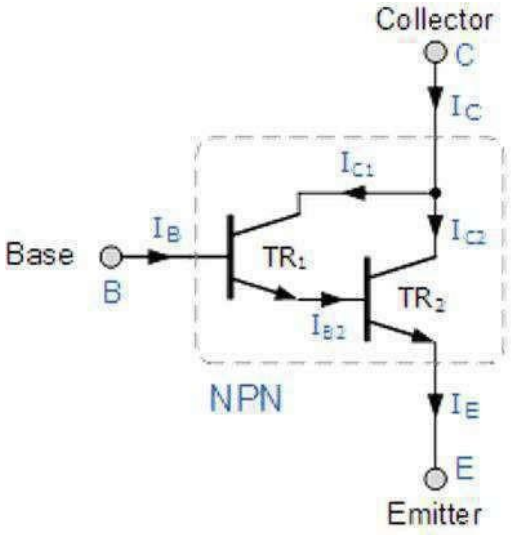


Figure.4.9.Darlington amplifier

Current gain is the most important characteristic of a transistor and it is indicated with h_{FE}. When the Darlington transistor is switched ON, then the current supplies through the load to the circuit

Load current=i/p current X transistor gain

A Darlington transistor contains two transistors, but it acts as a single transistor with a current gain that equals the total current gain is equal to current gains of the transistor1 and transistor 2.

Total current gain (h_{FE})= current gain of transisotr1 (h_{FE1}) X current gain of transistor2 (h_{FE2})

4.5.1. Structure of Darlington Transistor:

The collectors of the two transistors are connected together, and the emitter of the transistor TR1 energies the base terminal of the TR2 transistor. This structure attains β multiplication because for a base and collector current (i_b and β. i_b), where the current gain is greater than unity that is defined as

$I_c=I_{c1}+I_{c2}$

$I_c= \beta_1.I_B+ \beta_2.I_{B2}$

But the base current of the transistor TR1 is equal to I_{E1}(emitter current), and emitter of the TR1 transistor is connected to the base terminal of the transistor TR2

$I_{B2} = I_{E1}$

$=I_{c1}+ I_B$

$=\beta_1.I_B +I_B$

$= I_B(\beta_1 + 1)$

Substitute this I_{B2} value in the above equation

$I_c= \beta_1.I_B+ \beta_2. I_B(\beta_1 + 1)$

$I_c= \beta_1.I_B+ \beta_2. I_B\beta_1 + \beta_2. I_B$

$= (\beta1+ (\beta2.\beta1) + \beta2). I_B$

In the above equation, β1 and β2 are gains of individual transistors.

Here, the overall current gain of the first transistor is multiplied by the second transistor that is specified by β, & a couple of bipolar transistors are combined to form a single Darlington transistor with a very high i/p resistance and value of β.

4.6. Cascode amplifier

While the CB amplifier is known for wider bandwidth than the CE configuration, the low input impedance of CB is a limitation for many applications. The solution is to precede the CB stage by a low gain CE stage which has moderately high input impedance. The cascode amplifier is combined common-emitter and common-base. This circuit have a lot of advantages over the single stage amplifier like, better input output isolation, better gain, improved bandwidth, higher input impedance, higher output impedance, better stability, higher slew rate etc. The reason behind the increase in bandwidth is the reduction of Miller effect.

Analysis:

Figure 4.10 shows CE stage feeding a CB stage. This arrangement is designed to provide high input impedance with low voltage gain to ensure that the input Miller capacitance is at a minimum with the CB stage providing good high frequency operation. There are two transistors, a bottom transistor and a top transistor, called Q1 and Q2 respectively. Assuming both transistors are operating in the active region, an increase in V_{in} causes an increase in the current through the transistors as they are in series. As long as Q2 (top) is biased active, it will change its V_{be} with the current flowing. As current changes through R_L, the voltage dropped across R_L changes, and thus the voltage V_{out} changes. So it's similar to a normal common emitter amplifier, as long as everything is biased properly.

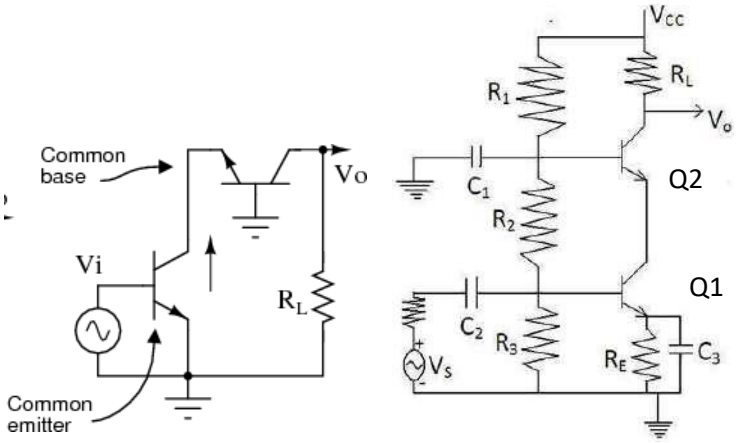


Figure.4.10. Cascode amplifier

4.7. Miller's theorem:

The Miller's theorem establishes that in a linear circuit, if there exists a branch with impedance Z, connecting two nodes with nodal voltages V1 and V2, we can replace this branch by two branches connecting corresponding nodes to ground by impedances Z/(1-K) and K*Z/(K-1) where K = V2/V1. It is shown in the figure below:

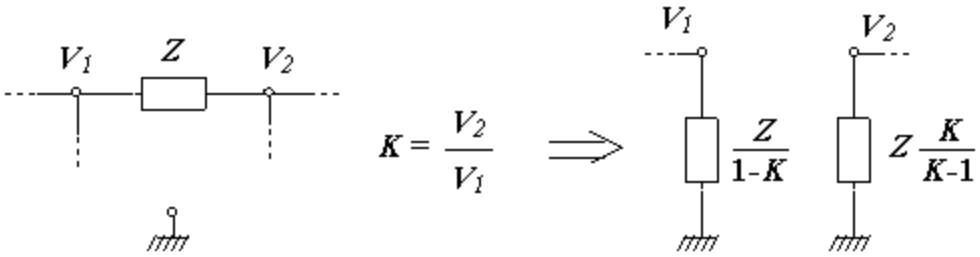


Figure.4.11. Miller Effect

Miller Effect Capacitance

In a BJT amplifier this capacitance becomes noticeable between: the Base-Collector junction at high frequencies in CE BJT amplifier configurations. It is called the Miller Capacitance. It effects the input and output circuits.

$I_i = I_1 + I_2$.....eqn(1)

Using Ohm's law yields

$$I_1 = V_i / Z_i,$$

$$I_1 = V_i / R_1$$

and $$I_2 = (V_i - V_o) / X_{cf}$$

$$= (V_i - A_v V_i) / X_{cf}$$

$$I_2 = V_i(1 - A_v) / X_{cf}$$

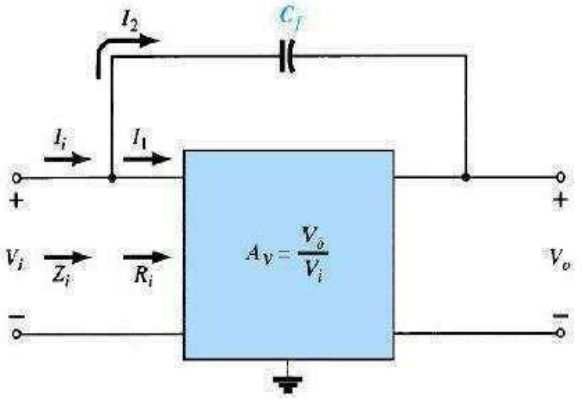


Figure.4.12. Miller effect

Substituting for I_i, I_1 and I_2 in eqn(1),

$$V_i / Z_i = V_i / R_i + [(1 - A_v)V_i] / X_{cf}$$

$$1/ Z_i = 1/R_i + [(1 - A_v)] / X_{cf}$$

$$1/ Z_i = 1/R_i + 1/ [X_{cf} / (1 - A_v)]$$

$$1/ Z_i = 1/R_i + 1/ X_{CM}$$

Where, $X_{CM} = [X_{cf} / (1 - A_v)]$

$$= 1/[\omega (1 - A_v) C_f]$$

$$C_{Mi} = (1 - A_v) C_f$$

C_{Mi} is the Miller effect capacitance.

4.8. Low and high frequency response:

Frequency Response of an amplifier shows how the gain of the output responds to input signals at different frequencies. Graphical representations of frequency response curves are called **Bode Plots** and as such Bode plots are generally said to be a semi-logarithmic graphs because one scale (x-axis) is logarithmic and the other (y-axis) is linear as shown in Fig.4.13. At low frequencies the coupling and bypass capacitors can no longer be replaced by the short circuit approximation because of the increase in reactance of these elements. The frequency dependent parameters of the small signal equivalent circuits and the stray capacitive elements associated with the active device and the network will limit the high frequency response of the system.

Analysis: The frequency response of circuit is the variation in its behavior with changes in the input signal frequency as it shows the band of frequencies over which the output (and the gain) remains fairly constant. The range of frequencies either big or small between f_L and f_H is called the circuit's bandwidth. We determine the voltage gain (in dB) for any sinusoidal input within a given frequency range. Frequency points f_L and f_H relate to the lower corner or cut-off frequency and the upper corner or cut-off frequency points respectively were the circuits gain falls off at high and low frequencies. These points on a frequency response curve are known commonly as the -3dB (decibel) points. So the bandwidth is simply given as:

Bandwidth(BW) = $f_H - f_L$

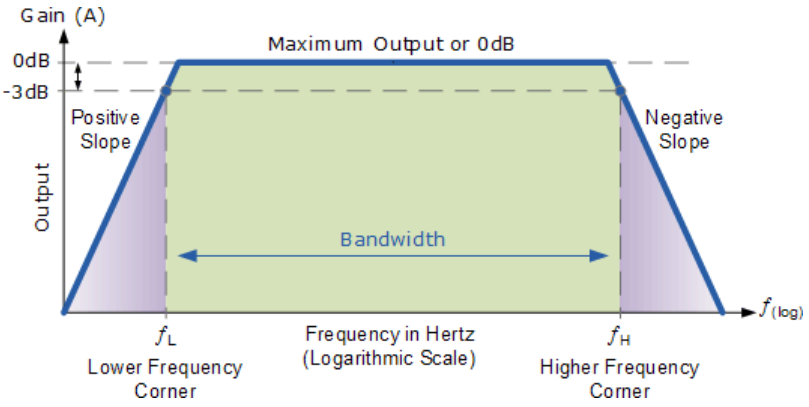


Figure.4.13.Frequency Response of BJT amplifier

The decibel, (dB) which is $1/10^{th}$ of a bel (B), is a common non-linear unit for measuring gain and is defined as $20\log_{10}(A)$ where A is the decimal gain, being plotted on the y-axis. Zero decibels, (0dB) correspond to a magnitude function of unity giving the maximum output. The -3dB point is also known as

the half-power points since the output power at this corner frequencies will be half that of its maximum 0dB value as shown.

$P = \frac{V^2}{R} = I^2 \times R$

V or I = 70.71 % of maximum or 0.7071 max at f_l or f_h

If R=1, then $P = \frac{(0.07071 \times V)^2}{1}$ 0r $(o.o7071 \text{ X } I)^2$

Therefore P = 0.5 V or 0.5 I

BJT Amplifier Low-Frequency Response:

In the low-frequency region of the single-stage BJT amplifier, it is the RC combinations formed by the network capacitors C_C, C_E and the network resistive parameters that determine the cutoff frequencies.

High-Frequency Response of BJT Amplifiers:

- The gain decreases at high frequencies due to internal feedback capacitance. The highest frequency of operation of BJT will be limited by internal capacitance's of BJT.
- The on and off switching times of BJT will be high and speed will be limited due to internal charge storage effects.

4.8. Hybrid π model:

The hybrid-pi model is a linearized two-port network approximation to the BJT using the small-signal base-emitter voltage, V_{BE}, and collector-emitter voltage, V_{CE}, as independent variables, and the small-signal base current, I_B, and collector current, I_C, as dependent variables.

A basic, low-frequency hybrid-pi model for the bipolar transistor is shown in figure 4.9. The various parameters are as follows.

$g_m = \frac{I_c}{V_{BE}}$ at $V_{CE} = 0$

is the transconductance, evaluated in a simple model, where:

- I_c is the quiescent collector current (also called the collector bias or DC collector current)
- $V_T = kT/e$ is the *thermal voltage*, calculated from Boltzmann's constant, k, the charge of an electron, e and the transistor temperature T in kelvins. At approximately room temperature (295 K, 22 °C or 71 °F), V_T is about 25 mV.

$r_\pi = \frac{V_{BE}}{I_B}$ at $V_{CE} = 0 \frac{V_T}{I_B} = \frac{\beta_0}{m}$

where:

- I_B is the DC (bias) base current.
- β_0 is the current gain at low frequencies (generally quoted as h_{fe} from the h-parameter model).

- $R_0=\frac{V_{CE}}{I_C}$ at $V_{BE} = 0$ is the output resistance due to the Early effect (is the Early voltage).

Related terms

The *output conductance*, g_{ce}, is the reciprocal of the output resistance, r_o:

$g_{ce}= 1/r_0$

The *transresistance*, r_m, is the reciprocal of the transconductance g_m:

$r_m= 1/g_m$

Full Hybrid Pi model: The full model introduces the virtual terminal, B', so that the base spreading resistance, r_{bb}, (the bulk resistance between the base contact and the active region of the base under the emitter) and $r_{b'e}$ (representing the base current required to make up for recombination of minority carriers in the base region) can be represented separately. C_e is the diffusion capacitance representing minority carrier storage in the base. The feedback components, $r_{b'c}$ and C_c, are introduced to represent the Early effect.

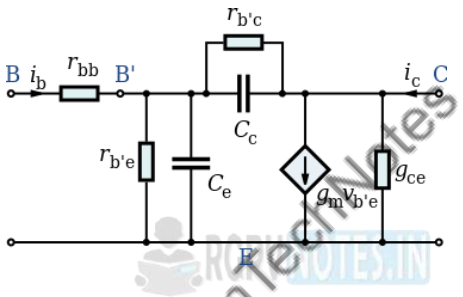


Figure.4.14.Hybrid Pi model

Physical explanation of parameters of high frequency model of BJT

- $R_{bb'}$ is the base spreading resistance of BJT which represents the bulk resistance of the material between the base terminal and the physical inaccessible internal node of BJT.
- $R_{b'e}$ is the internal base node to emitter resistance. It accounts for the increase recombination base current as emitter current increases. It is in parallel with the collector circuit and hence reduces the collector current value from emitter current. This resistance will be high order of kilo ohms as the decrease in the collector current due to base recombination currents will be very less.
- $R_{b'c}$ is the Feedback resistance from internal base node to collector node. It is included in the model to take in to account early effect. As collector to base reverse bias is increased(action) the effective width increases and collector current increases(feedback response).This feedback effect(early effect) is accounted for by $R_{b'c}$.
- R_{ce} represents the bulk resistance of the material between collector to emitter.
- C_e is the Diffusion capacitance of emitter base junction. Diffusion capacitance of emitter base junction is directly proportional to emitter bias current and forward base transit time. Forward transit time is defined as the average time the minority carrier spends in base. The Diffusion capacitance of emitter base junction accounts for the minority charge stored in base.
- C_C represents the transition or space charge capacitance of base collector junction.

4.9. Current mirror:

Current mirror serves as a simple current regulator, supplying nearly constant current to a load over a wide range of load resistances.

We know that in a transistor operating in its active mode,
$I_c = \beta I_B$
$\alpha = I_c / I_B$.
$\alpha = \beta/(\beta+1)$ for any transistor.
Maintaining a constant base current through an active transistor results in the regulation of collector current. The α ratio works similarly: if emitter current is held constant, collector current will remain at a stable, regulated value so long as the transistor has enough collector-to-emitter voltage drop to maintain it in its active mode. Therefore, if we have a way of holding emitter current constant through a transistor, the transistor will work to regulate collector current at a constant value.
Remember that the base-emitter junction of a BJT is nothing more than a PN junction, just like a diode, and that the "diode equation" specifies how much current will go through a PN junction given forward voltage drop and junction temperature:
$I_D = I_s (\exp(qV_D/NK_T)-1)$
If both junction voltage and temperature are held constant, then the PN junction current will be constant. Following this rationale, if we were to hold the base-emitter voltage of a transistor constant, then its emitter current will be constant, given a constant temperature. Consider the figure 4.15.

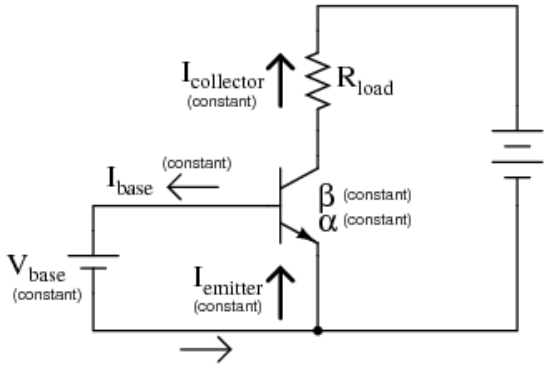


Figure.4.15.Constant V_{BE} gives constant I_B, constant I_E, and constant I_C.

The transistor's collector current is almost equal to its emitter current, as the α ratio of a typical transistor is almost unity. If we have control over the transistor's emitter current by setting diode current with a simple resistor adjustment, then we have control over the transistor's collector current. In other words, collector current mimics, or mirrors the diode current.
Current through resistor R_{load} is therefore a function of current set by the bias resistor, the two being nearly equal. This is the function of the current mirror circuit: to regulate current through the load resistor by conveniently adjusting the value of R_{bias}. Current through the diode is described by a simple equation: power supply voltage minus diode voltage (almost a constant value), divided by the resistance of R_{bias}.
Because temperature is a factor in the "diode equation," and we want the two PN junctions to behave identically under all operating conditions, we should maintain the two transistors at exactly the same temperature. The current mirror circuit shown with two NPN transistors in Figure 4.16 is sometimes called a current-sinking type, because the regulating transistor conducts current to the load from ground ("sinking" current), rather than from the positive side of the battery ("sourcing" current).

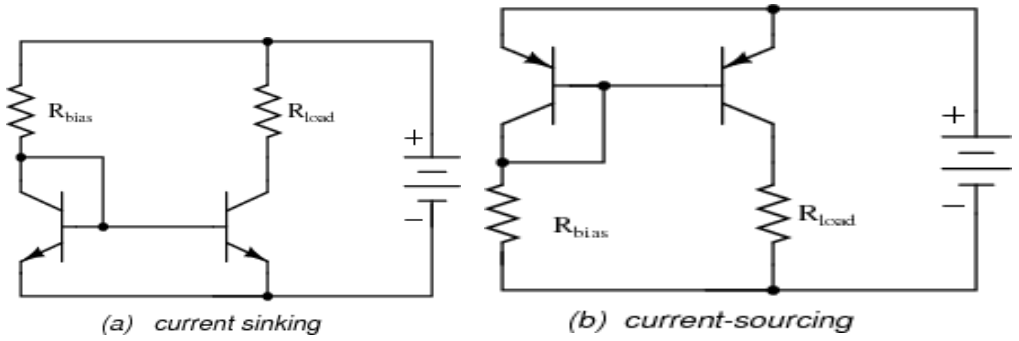


Figure.4.16.Current mirror circuits.

A current mirror is a transistor circuit that regulates current through a load resistance, the regulation point being set by a simple resistor adjustment.

- Transistors in a current mirror circuit must be maintained at the same temperature for precise operation. When using discrete transistors, you may glue their cases together to do this.
- Current mirror circuits may be found in two basic varieties: the current sinking configuration, where the regulating transistor connects the load to ground; and the current sourcing configuration, where the regulating transistor connects the load to the positive terminal of the DC power supply.

4.11. Power Amplifier:

A power amplifier is an electronic amplifier designed to increase the magnitude of power of a given input signal. The power of the input signal is increased to a level high enough to drive loads of output devices like speakers, headphones, RF transmitters etc. Unlike voltage/current amplifiers, a power amplifier is designed to drive loads directly and is used as a final block in an amplifier chain. The input signal to a power amplifier needs to be above a certain threshold. So instead of directly passing the raw audio/RF signal to the power amplifier, it is first pre-amplified using current/voltage amplifiers and is sent as input to the power amp after making necessary modifications.

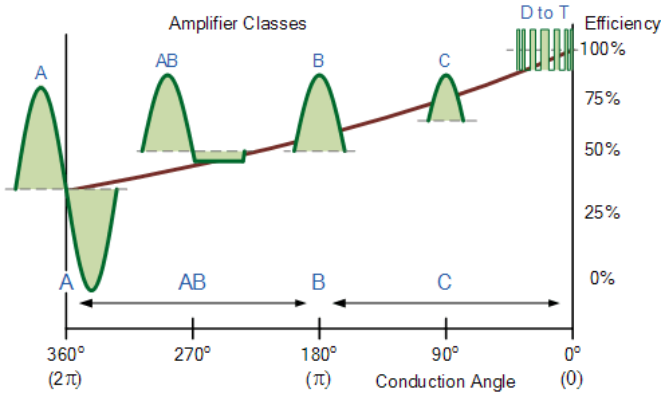


Figure.4.17. Power amplifiers efficiency and output

A Power amplifier is large signal amplifier and this is generally a last stage of a multistage amplifier. The function of a practical power amplifier is to amplify a weak signal until sufficient power is achieved to operate a loudspeaker or output device. Typical output power rating of a power amplifier will be 1W or higher.

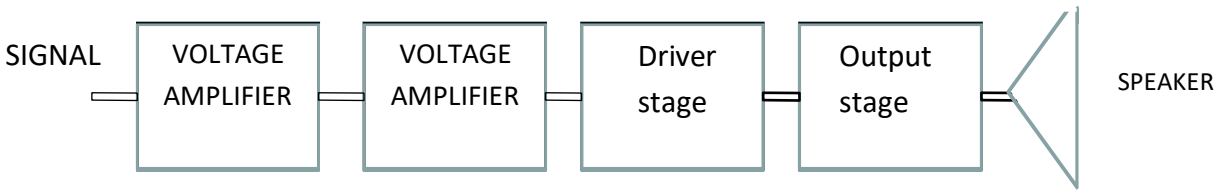


Figure.4.18.Stages of Power amplifier

The driver stage operates as a class A power amplifier and supplies the drive for the output stage. The last output stage is essentially a power amplifier and its purpose is to transfer maximum power to the output device. The output stage generally employ class B amplifiers in push-pull arrangement. A large signal amplifier means much larger portion of load line is used during signal operation compared to small signal amplifier. A small signal amplifier operate over a linear portion of load line. In case of power amplifier, we cannot use small signal approximation directly to calculate voltage gain, current gain and input/output impedance. Ideal power amplifier will deliver 100% of the power it draws from the supply to load.

Classification of power amplifier:

- **Class A,**
- **Class B,**
- **Class A B,**
- **C amplifiers**

Class A amplifier

The power amplifiers are classified according the conduction angle they produced. Conduction angle measures the portion of the input cycle that is reproduced at the output of a power amplifier. Class A amplifier as long as the output signal is not clipped. With this kind of amplifier, collector current flows throughout the cycle. Stated another way, no clipping of the output signal occurs at any time during the cycle. Now, we discuss a few equations that are useful in the analysis of class A amplifiers.

Besides voltage gain, any amplifier has a **power gain,** defined as

$$A = \frac{P_{0UT}}{P_{IN}}$$

In words, the power gain equals the ac output power divided by the ac input power.

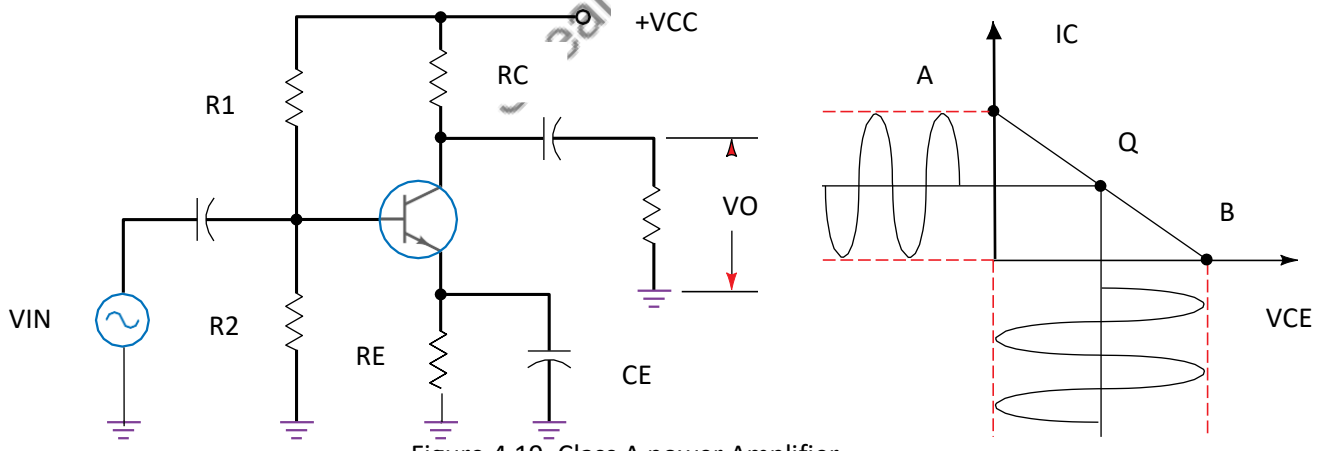


Figure.4.19. Class A power Amplifier

Figure 4.19 shows the output characteristics with operating point Q. here at point A (I_{CQ}) and point B (V_{CEQ}) Represent no signal collector current and collector –emitter voltage respectively. It may be observed that when an a.c input signal is applied, the operating point Q shifts up and down causing output current and voltage to vary about it. The output current is increased to I_{Cmax} and I_{Cmin}. In the same fashion, the collector emitter voltage increases to V_{ce} max and falls to V_{ce} min.

The Class A amplifier is the simplest form of power amplifier that uses a single switching transistor in the standard common emitter circuit configuration as seen previously to produce an inverted output. The transistor is always biased "ON" so that it conducts during one complete cycle of the input signal waveform producing minimum distortion and maximum amplitude of the output signal.

Efficiency

The efficiency of an amplifier represents the amount of ac power delivered (transferred) from the dc source. The efficiency of the amplifier is calculated using

$$\% = \frac{p_{ac}}{p_{dc}} x100\%$$

Maximum efficiency:

For the class A series-fed amplifier, the maximum efficiency can be determined using the maximum voltage and current swings. For the voltage swing it is maximum $V_{CE(}$p-p) =V_{CC}

For the current swing it is

Maximum I_C (p-p)= $\frac{V_{cc}}{R_c}$

Using the maximum voltage swing $p_{ac} = \frac{V_{cc}(\frac{cc}{R_c})}{8}$

$$V^2_{cc/8R_c}$$

The maximum power input can be calculated using the dc bias current set to one-half the maximum value:

Maximum p_{dc} $= \text{VCC (maximum Ic)} = \text{VCC}\frac{(\frac{cc}{Rc})}{2}$

$$V^2_{cc/2R_c}$$

But we know that:

$$\% = \frac{p_{ac}}{p_{dc}} x100\%$$

$\frac{V^2_{cc/8Rc}}{V^2_{cc/2R_c}}$x100% =25%

The maximum efficiency of a class A series-fed amplifier is thus seen to be 25%.Since this maximum efficiency will occur only for ideal conditions of both voltage swing and current swing, most series-fed circuits will provide efficiencies of much less than 25%.

Class B amplifier:

Class A is the common way to run a transistor in linear circuits because it leads to the simplest and most stable biasing circuits. But class A is not the most efficient way to operate a transistor. In some applications, like battery-powered systems, current drain and stage efficiency become important considerations in the design. Figure.4.14. shows a basic class B amplifier. When a transistor operates as class B, it clips off half a cycle. To avoid the resulting distortion, we can use two transistors in a push-pull arrangement like that of Figure 4.14.Push-pullmeans that one transistor conducts for half a cycle while the other is off, and vice versa. Here is how the circuit works: On the positive half cycle of input voltage, the secondary winding of T_1 has voltage V_1 and V_2, as shown. Therefore, the upper transistor conducts and the lower one cuts off. The collector current through Q1 flows through the upper half of the output primary winding. This produces an amplified and inverted voltage, which is transformer-coupled to the loudspeaker. On the next half cycle of input voltage, the polarities reverse. Now, the lower transistor turns on and the upper transistor turns off. The lower transistor amplifies the signal, and the alternate half cycle appears across the loudspeaker. Since each transistor amplifies one-half of the input cycle, the loudspeaker receives a complete cycle of the amplified signal.

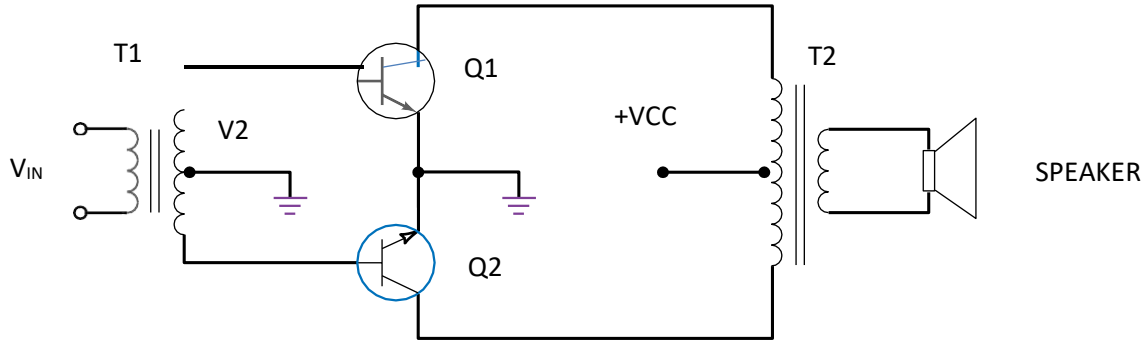


Figure.4.20. Class B push Pull amplfier

Maximum efficiency:
The efficiency of the class B amplifier can be calculated using the basic equation

$$\% = \frac{p_{ac}}{p_{dc}} x100\% \quad = \frac{V_L^2(P)/2R_l}{\frac{2}{Vcc\ [(\pi)\ I\ p\ ]}} x100\% = \frac{\pi\ V_l(p)}{4\ V_{cc}} x100\%$$

Using $I(p) = V_l(p)/Rl$shows that the larger the peak voltage, the higher the circuit efficiency, up to a maximum value when *VL*(p) = *VCC*, this maximum efficiency then being

$$maxmum\ \text{eff}cency\ () = \frac{\pi}{4}\ x100\%=78.5\%$$

Power Dissipation:
The power dissipated (as heat) by the output power transistors is the difference between the input power delivered by the supplies and the output power delivered to the load.

$$P_{2Q} = P_{dc} - P_{ac}$$

Where*P*2*Q* is the power dissipated by the two output power transistors. The dissipated power handled by each transistor is then

$$P_Q = \frac{P_{2Q}}{2}$$

Advantage and Disadvantages class B amplifier: Since there is no bias in Fig. class B amplifier, each transistor is at cutoff when there is no input signal, an advantage because there is no current drain when the signal is zero. Another advantage is improved efficiency where there is an input signal. The maximum efficiency of a class B push-pull amplifier is 78.5 percent, so a class B push-pull power amplifier is more commonly used for an output stage than a class A power amplifier. The main disadvantage is the use of transformers.Audiotransformersarebulkyandexpensive.Althoughwidelyused at one time, a transformer-coupled amplifier like Fig. class B amplifier is no longer popular.

Crossover Distortion
In the push-pull configuration, the two identical transistors get into conduction, one after the other and the output produced will be the combination of both. When the signal changes or crosses over from one transistor to the other at the zero voltage point, it produces an amount of distortion to the output wave shape. For a transistor in order to conduct, the base emitter junction should cross 0.7v, the cut off voltage. The time taken for a transistor to get ON from OFF or to get OFF from ON state is called the **transition period**. At the zero voltage point, the transition period of switching over the transistors from one to the other, has its effect which leads to the instances where both the transistors are OFF at a time. Such instances can be called as **Flat spot** or **Dead band** on the output wave shape.

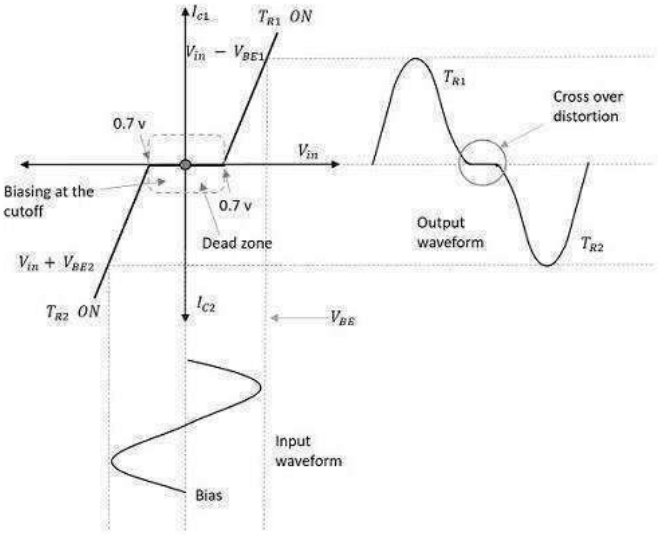


Figure.4.21. Crossover distortion

Class C amplifier:

A class C amplifier can produce more power than a class B amplifier. Consider the case of a radio transmitter in which the audio signals are raised in their frequency to the medium or short wave band to that they can be easily transmitted. The high frequency introduced is in radio frequency range and it serves as the carrier of the audio signal. The process of raising the audio signal to radio frequency called modulation.

The modulated wave has a relatively narrow band of frequencies centered on the carrier frequencies. At any instant, there are several transmitters transmitting simultaneously. The radio receiver selects the signals of desired frequencies to which it is tuned, amplifies it and converts it back to audio range. Therefore, tuned voltage amplifiers are used. In short, the tuned voltage amplifiers selects the desired radio frequency signal out of a number of RF signals present at that instant and then amplifies the selected RF signal to the desired level as shown in fig.4.22.

Class C operation means that the collector current flows for less than 180° of the ac cycle. This implies that the collector current of a class C amplifier is highly non-sinusoidal because current flows in pulses. To avoid distortion, class C amplifier makes use of a resonant tank circuit. This results in a sinusoidal output voltage. The resonant tank circuit is tuned to the frequency of the input signal.

When the circuit has a high quality factor (Q) parallel resonance occurs at approximately

$$F = \frac{1}{2\pi LC}$$

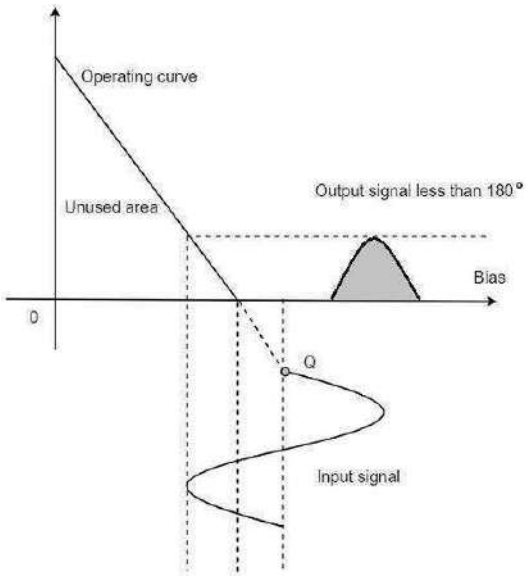


Figure.4.22. Class C Amplifier Output

At the resonance frequency, the impedance of the parallel resonant circuit is very high and is purely resistive. When the circuit is tuned to the resonant frequency, the voltage across R_L is maximum and sinusoidal. The higher the Q of the circuit, the faster the gain drops off on either side of resonance.

Class AB amplifier:

Class AB is another type of push pull amplifier which is almost similar to that of a Class A push pull amplifier and the only difference is that the value of biasing resistors R1 and R2 are so selected that the transistors are biased just at the cut in voltage (0.7V). This reduces the time for which both transistors are simultaneously OFF (the time for which input signal is between (-0.7V and +0.7V) and so the cross over distortion gets reduced. Of the above said classes Class A has least distortion, then Class AB and then Class B. Any way Class AB configuration has reduced efficiency and wastes a reasonable amount of power during zero input condition. Class B has the highest efficiency (78.5%), then Class B (between 78.5 to 50%) and then Class A (50%).

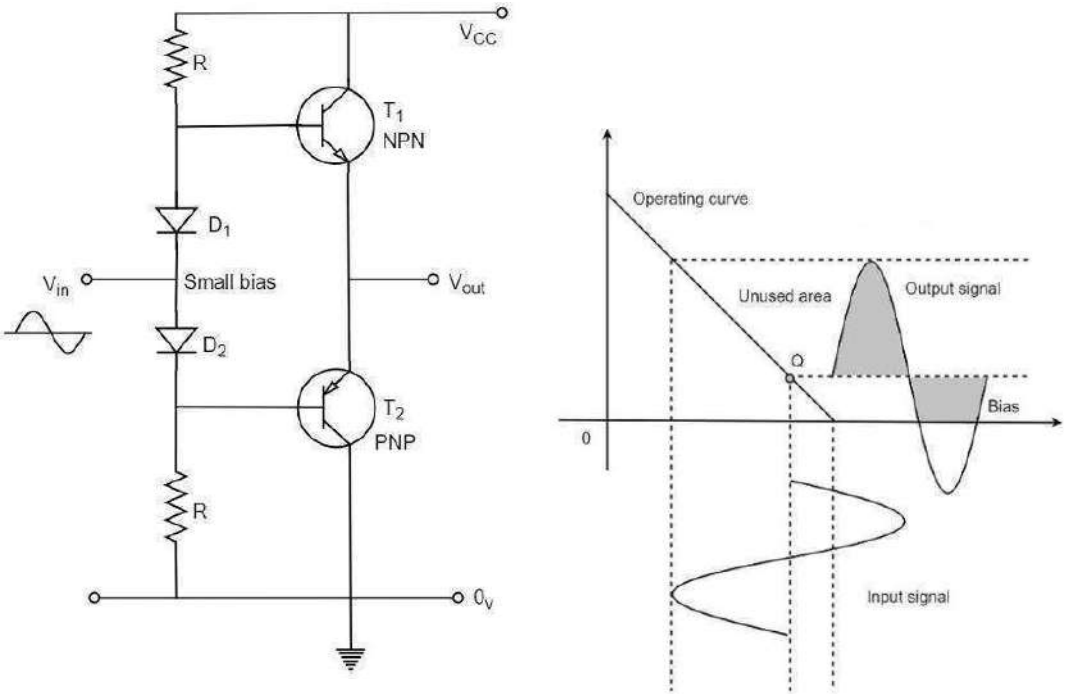


Figure.4.23. Class AB amplifier

During the first half-cycle of operation, transistor *Q*1 is driven into conduction whereas transistor *Q*2 is driven off. The current I_1 through the transformer results in the first half-cycle of signal to the load. During the second half-cycle of the input signal, *Q*2 conducts whereas *Q*1 stays off, the current I_2 through the transformer resulting in the second half-cycle to the load. The overall signal developed across the load then varies over the full cycle of signal operation. The small bias voltage given using diodes D1 and D2, as shown in the above figure, helps the operating point to be above the cut off point. Hence the output waveform of class AB results as seen in the above figure. The crossover distortion created by class B is overcome by this class AB, as well the inefficiencies of class A and B don't affect the circuit.

Class D Power Amplifier:

A Class D audio amplifier is basically a non-linear switching amplifier or PWM amplifier. Class-D amplifiers theoretically can reach 100% efficiency, as there is no period during a cycle were the voltage and current waveforms overlap as current is drawn only through the transistor that is on.

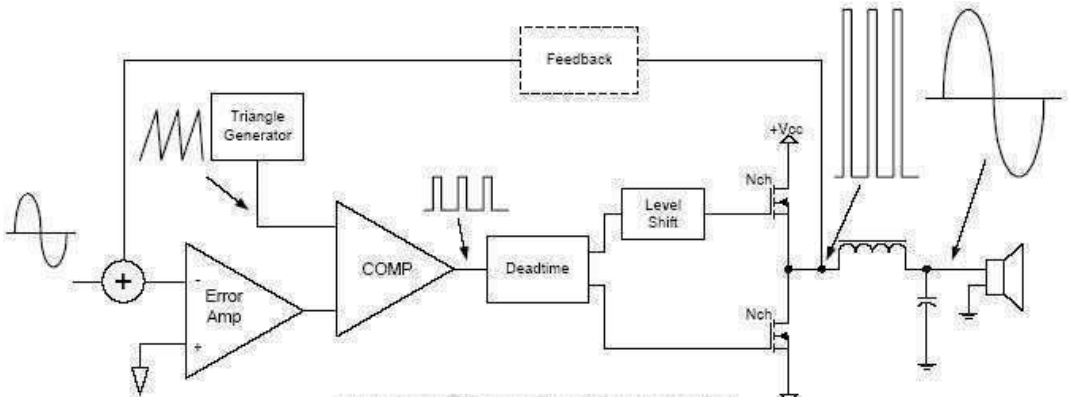


Figure.4.24Class D power Amplifier

Subject Name- Electronics Device **Subject Code**: EC303

Unit V

FET construction- JFET: Construction, n-channel and p-channel, transfer and drain characteristics, parameters, Equivalent model and voltage gain, analysis of FET in CG, CS and CD configuration. Enhancement and Depletion MOSFET drain and transfer Characteristics. Unijunction Transistor (UJT) and Thyristors: UJT: Principle of operation, characteristics, UJT relaxation oscillator.

5.1. Field Effect Transistor (FET):

A bipolar junction transistor (BJT) is a current controlled device i.e., output characteristics of the device are controlled by base current and not by base voltage. However, in a field effect transistor (FET), the output characteristics are controlled by input voltage (i.e., electric field) and not by input current. This is probably the biggest difference between BJT and FET.

There are two basic types of field effect transistors:

- **(i)** Junction field effect transistor (JFET)
- **(ii)** Metal oxide semiconductor field effect transistor (MOSFET)

The FET is a three terminal device like the BJT, but operates by a different principle. The three terminals are called the source, drain, and gate. The voltage applied to the gate controls the current flowing in the source-drain channel. No current flows through the gate electrode, thus the gate is essentially insulated from the source-drain channel. Because no current flows through the gate, the input impedance of the FET is extremely large (in the range of 10^{10}–10^{15} Ω). The large input impedance of the FET makes them an excellent choice for amplifier inputs. The two common families of FETs, the junction FET (JFET) and the metal oxide semiconductor FET (MOSFET) differ in the way the gate contact is made on the source-drain channel.

5.2. JFET

In the JFET the gate-channel contact is a reverse biased pn junction. The gate-channel junction of the JFET must always be reverse biased otherwise it may behave as a diode. All JFETs are depletion mode devices—they are on when the gate bias is zero ($V_{GS} = 0$). Two versions of the symbols are in common use. The symbols in the top row depict the source and drain as being symmetric. This is not generally true. Slight asymmetries are built into the channel during manufacturing which optimize the performance of the FET. Thus it is necessary to distinguish the source from the drain. In this class we will use the asymmetric symbols found on the bottom row, which depict the gate nearly opposite the source. The designation n-channel means that the channel is n doped and the gate is p doped. The p-channel is complement of n- channel.

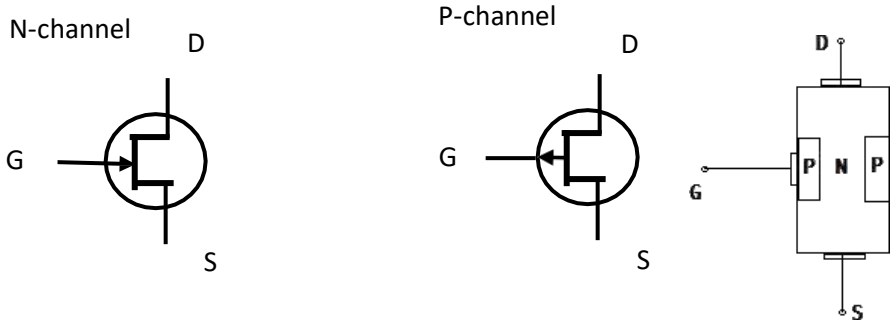


Figure.5.1. Symbol and schematic of JFET

5.2.1. Basic Operation of JFET:

Figure 5.2 shows dc bias voltages applied to an n-channel JFET. V_{DS} provides a drain-to-source voltage and supplies current from drain to source. VGG sets the reverse-bias voltage between the gate and the source. The JFET is always operated with the gate-source pn junction reverse-biased. Reverse-biasing of the gate-source junction with a negative gate voltage produces a depletion region along the pn junction, which extends into the n channel and thus increases its resistance by decreasing the channel width. The channel width and the channel resistance can be controlled by varying the gate voltage, there by controlling the amount of drain current I_D Figure 5.2, illustrates this concept when $V_{GG} = V_{GS}$.

The JFET has two distinct modes of operation: the variable-resistance mode, and the *pinch-off* mode. In the variable-resistance mode the JFET behaves like a resistor whose value is controlled by $\mathbf{V_{GS}}$. In the pinch-off mode, the channel has been heavily constricted with most of the drain-source voltage drop occurring along the narrow and therefore high-resistance part of the channel near the depletion regions.

At small values of V_{DS} (in the range of a few tenths of a volt), the curves of constant $\mathbf{V_{GS}}$ show a linear relationship between V_{DS} and I_D. This is the variable-resistance region of the graph. As V_{DS} increases, each of the curves of constant $\mathbf{V_{GS}}$ enters a region of nearly constant I_D. This is the pinch-off region, where the JFET can be used as a linear voltage and current amplifier.

At $\mathbf{V_{GS}=0}$, the current through the JFET reaches a maximum known as I_{DSS} , the current from Drain to Source with the gate Shorted to the source. If $\mathbf{V_{GS}}$ goes positive for this N-channel JFET, the PN junction becomes conducting and the JFET becomes just a forward-biased diode.

5.2.2. Drain characteristics of JFET: The curve drawn between drain current I_D and drain-source voltage V_{DS} with gate-to source voltage V_{GS} as the parameter is called the *drain* or *output characteristic.* This characteristic is analogous to collector characteristic of a BJT.

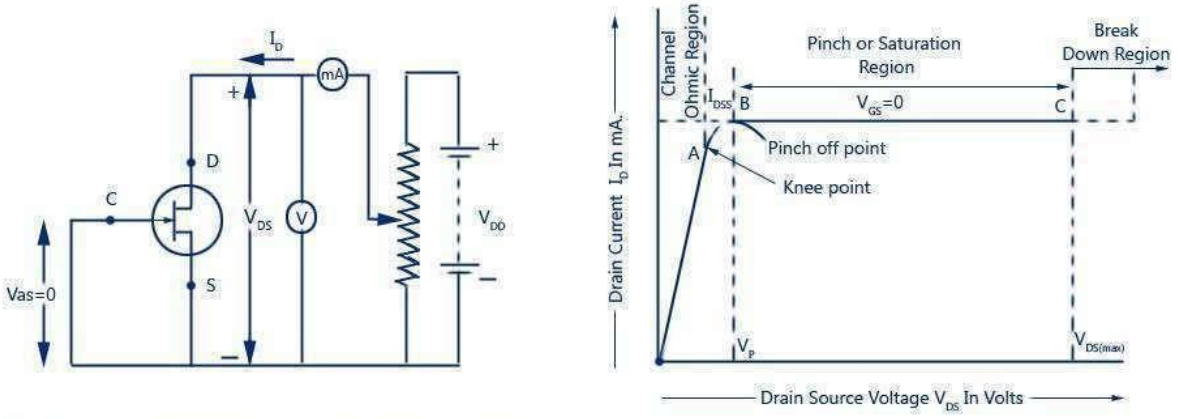


Figure.5.2. JFET drain characteristics with shorted Gate

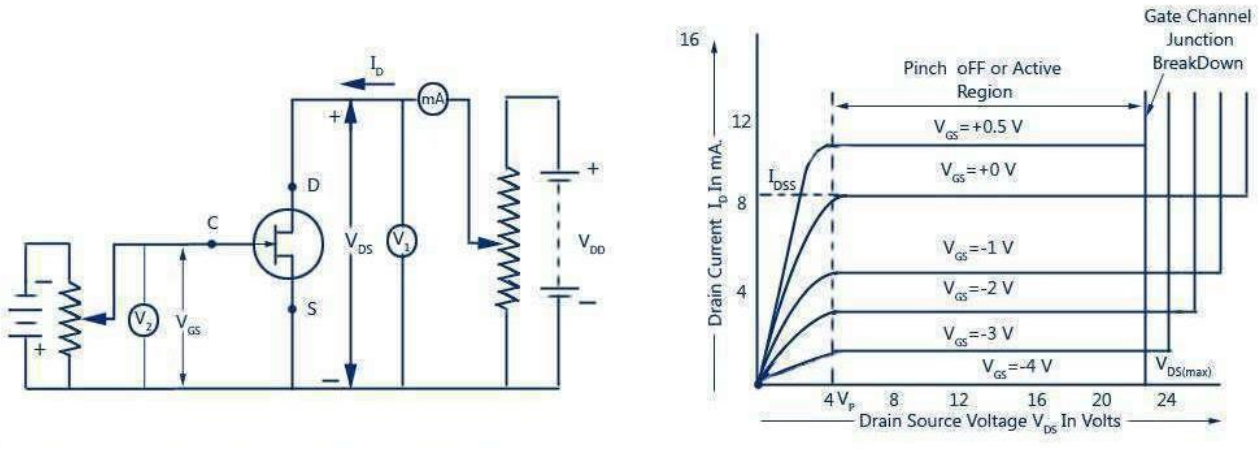


Figure.5.3. JFET drain characteristics at different values of V_{GS}

It is observed that as the negative gate bias voltage is increased

(1) The maximum saturation drain current becomes smaller because the conducting channel now becomes narrower.
The equation that relates the current I_D with the voltage V_{GS} is known as the Schockley equation that is given by:

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_p}\right)^2$$

$$V_{GS} > V_p$$

$$V_{DS} \geq V_{GS} - V_p$$

where V_p is the pinch-off voltage and I_{DSS} is the saturation current.

This current (I_{DSS}) is defined as the value of the current I_D when $V_{GS} = 0$, and this feature is often used to obtain a constant value current source (I_{DSS}). This equation at the I_D and V_{GS} plane represent a parabola displaced in V_p.

(2) Pinch-off voltage is reached at a lower value of drain current I_D than when $V_{GS} = 0$. When an external bias of, say – 1 V is applied between the gate and the source, the gate-channel junctions are reverse-biased even when drain current, I_D is zero. Hence the depletion regions are already penetrating the channel to a certain extent when drain-| source voltage, V_{DS} is zero. Due to this reason, a smaller voltage drop along the channel (i.e. smaller than that for $V_{GS} = 0$) will increase the depletion regions to the point where 1 they pinch-off the current. Consequently, the pinch-off voltage V_P is reached at a lower 1 drain current, I_D when $V_{GS} = 0$.
(3) The ohmic region portion decreases.
(4) Value of drain-source voltage V_{DS} for the avalanche breakdown of the gate junction is reduced.
Value of drain-source voltage, V_{DS} for breakdown with the increase in negative bias voltage is reduced simply due to the fact that gate-source voltage, V_{GS} keeps adding to the I reverse bias at the junction produced by current flow.

5.2.3. Transfer Characteristic of JFET

The transfer characteristic for a JFET can be determined experimentally, keeping drain-source voltage, V_{DS} constant and determining drain current, I_D for various values of gate-source voltage, V_{GS}. The curve is plotted between gate-source voltage, V_{GS} and drain current, I_D, as illustrated in fig. 5.*4*. It is similar to the transconductance characteristic of a vacuum tube or a transistor. It is observed that
(i) Drain current decreases with the increase in negative gate-source bias
(ii) Drain current, $I_D = I_{DSS}$ when $V_{GS} = 0$
(iii) Drain current, $I_D = 0$ when $V_{GS} = V_D$

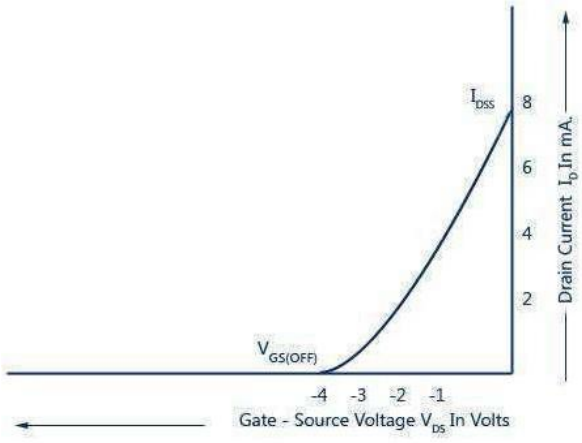


Figure.5.4. transfer characteristics

5.3. FET configurations:

There are three basic configurations for a single stage FET amplifier:

- Common source (CS) configuration: The common source circuit provides a medium input and output impedance levels. Both current and voltage gain can be described as medium, but the output is the inverse of the input, i.e. 180° phase change. This provides a good overall performance and as such it is often thought of as the most widely used configuration.
- Common gate (CG) configuration: This transistor configuration provides low input impedance while offering a high output impedance. Although the voltage is high, the current gain is low and the overall power gain is also low when compared to the other FET circuit configurations available. The other salient feature of this configuration is that the input and output are in phase.
- Source follower (SF) or common Drain configuration: This FET configuration is also known as the source follower. The reason for this is that the source voltage follows that of the gate. Offering high input impedance and low output impedance it is widely used as a buffer. The voltage gain is unity, although current gain is high. The input and output signals are in phase.

5.4. JFET Biasing: The purpose of biasing is to select the proper dc gate-to-source voltage to establish a desired value of drain current and, thus, a proper Q-point. Three types of bias are self-bias, voltage-divider bias, and Fixed bias.

5.4.1. Self-Bias: Self-bias is the most common type of JFET bias. JFET must be operated such that the gate source junction is always reverse-biased. This condition requires a negative V_{GS} for an n-channel JFET. This can be achieved using the self-bias arrangements shown in figure here. The gate resistor, R_G, does not affect the bias because it has essentially no voltage drop across it; and therefore the gate remains at 0 V. R_G is necessary only to force the gate to be at 0 V and to isolate an ac signal from ground in amplifier applications. For the n-channel JFET as shown in the figure, I_s produces a voltage drop across R_s and makes the source positive with respect to ground. Since $I_s = I_D$ and V_G=0V, then $V_S = I_D R_S$. The gate-to-source voltage is then given by

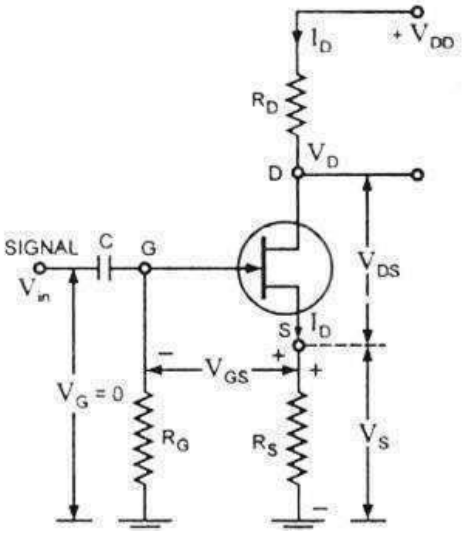


Figure.5.5. Self Bias circuit of JFET

$V_{GS} = V_G - V_S = 0 - I_D R_S$

$= - I_D R_S$

the drain-to-source voltage is

$V_{DS} = V_D - V_S = V_{DD} - I_D(R_D + R_S)$

Thus dc conditions of JFET amplifier are fully specified. Self biasing of a JFET stabilizes its quiescent operating point against any change in its parameters like transconductance. Let the given JFET be

replaced by another JFET having the double conductance then drain current will also try to be double but since any increase in voltage drop across R_s, therefore, gate-source voltage, V_{GS} becomes more negative and thus increase in drain current is reduced.

5.4.2. Voltage Divider Bias:

The JFET gate voltage Vg is biased through the potential divider network set up by resistors R1 and R2and is biased to operate within its saturation region which is equivalent to the active region of the bipolar junction transistor. Since the N-Channel JFET is a depletion mode device and is normally "ON", a negative gate voltage with respect to the source is required to modulate or control the drain current. This negative voltage can be provided by biasing from a separate power supply voltage or by a self biasing arrangement as long as a steady current flows through the JFET even when there is no input signal present and Vg maintains a reverse bias of the gate-source PN junction.

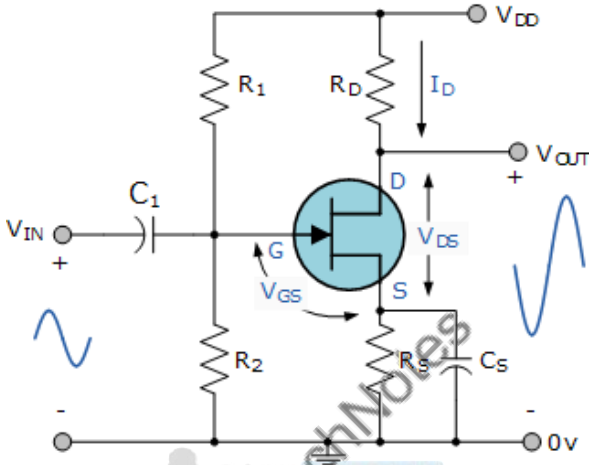


Figure.5.6. Voltage Divider Bias

$$V_G = \frac{V_{DD}\,R_2}{R_1 + R_2} = V_{DD}\left(\frac{R_2}{R_1 + R_2}\right)$$

$$V_{GS} = V_G - V_S = V_G - I_D R_S$$

The circuit is so designed that $I_D R_s$ is greater than V_G so that V_{GS} is negative. This provides correct bias voltage.

The operating point can be determined as

$I_D = (V_G - V_{GS})/ R_S$

$V_{DS} = V_{DD} - I_D (R_D + R_S)$

When the JFET is switched fully "ON" a voltage drop equal to Rs*Id is developed across this resistor raising the potential of the source terminal above 0v or ground level. This voltage drop across Rs due to the drain current provides the necessary reverse biasing condition across the gate resistor, R2 effectively generating negative feedback.

So in order to keep the gate-source junction reverse biased, the source voltage, Vs needs to be higher than the gate voltage, Vg. This source voltage is therefore given as:

$$V_S = I_D \times R_S = V_G - V_{GS}$$

Then the Drain current, Id is also equal to the Source current, Is as "No Current" enters the Gate terminal and this can be given as:

$$I_D = \frac{V_S}{R_S} = \frac{V_{DD}}{R_D + R_S}$$

5.4.3. Fixed Bias:

DC bias of a FET device needs setting of gate-source voltage V_{GS} to give desired drain current I_D. For a JFET drain current is limited by the saturation current I_{DS}. Since the FET has such a high input impedance that no gate current flows and the dc voltage of the gate set by a voltage divider or a fixed battery voltage is not affected or loaded by the FET.

Fixed dc bias is obtained using a battery V_{QG}. This battery ensures that the gate is always negative with respect to source and no current flows through resistor R_G and gate terminal that is I_G =0. The battery provides a voltage V_{GS} to bias the N-channel JFET, but no resulting current is drawn from the battery V_{GG}. Resistor R_G is included to allow any ac signal applied through capacitor C to develop across R_G. While any ac signal will develop across R_G, the dc voltage drop across R_G is equal to $I_G R_G$ *i.e.* 0 volt.

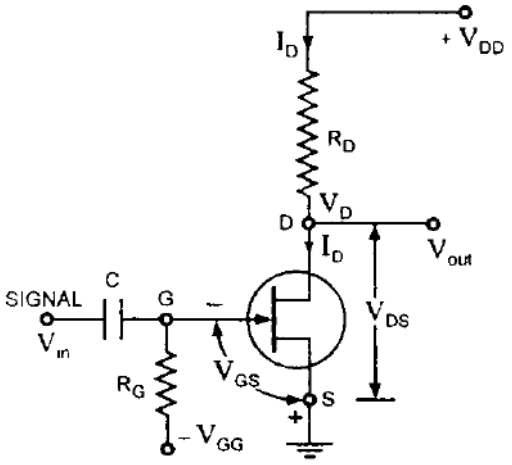


Figure.5.7.Fixed Bias Circuit

The gate-source voltage V_{GS} is then

$V_{GS} = – V_G – V_s = – V_{GG} – 0 = – V_{GG}$

The drain -source current I_D is then fixed by the gate-source voltage as determined by equation.

This current then causes a voltage drop across the drain resistor R_D and is given as $V_{RD} = I_D R_D$ and output voltage, $V_{out} = V_{DD} – I_D R_D$

5.5. Metal-oxide semiconductor field effect transistor (MOSFET):

In the MOSFET the gate-channel contact is a metal electrode separated from the channel by a thin layer of insulating oxide. MOSFETs have very good isolation between the gate and the channel, but the thin oxide is easily damaged (punctured!) by static discharge through careless handling A depletion-type device is a device that uses an input voltage to reduce the size of the channel to control the amount of current. An enhancement-type device is a device that uses an input voltage to increase the size of the channel to control the amount of current. JFETs can operate only in depletion mode. There are two types of MOSFETS: depletion-type MOSFETs or D-MOSFETs, and enhancement-type MOSFETs, or E-MOSFETs. There are two types of channel: n-channel and p-channel.

In the MOSFET, the current is controlled by an electric field applied perpendicular to both the semiconductor surface and to the direction of current. The phenomenon used to modulate the conductance of a semiconductor, or control the current in a semiconductor, by applying an electric field perpendicular to the surface is called the field effect. Again, the basic transistor principle is that the voltage between two terminals controls the current through the third terminal.

5.5.1. Types of MOSFETs: There are two basic types of MOSFETs viz.

- Depletion-type MOSFET or D-MOSFET. The D-MOSFET can be operated in both the depletion mode and the enhancement-mode. For this reason, a D-MOSFET is sometimes called depletion/enhancement MOSFET.
- Enhancement-type MOSFET or E-MOSFET. The E-MOSFET can be operated only in enhancement-mode.

5.5.2. N-Channel Enhancement mode MOSFET:

When the gate voltage is negative with respect to source, the depletion type MOSFET (metal oxide semiconductor field effect transistor) operates with an enhancement mode. Figure 5.3 shows a simplified cross section of a MOS field-effect transistor. The gate, oxide, and p-type substrate regions are the same as those of a MOS capacitor. In addition, we now have two n-regions, called the source terminal and drain terminal. The current in a MOSFET is the result of the flow of charge in the inversion layer, also called the channel region, adjacent to the oxide− semiconductor interface.

The channel length L and channel width E are defined on the figure. The channel length of a typical integrated circuit MOSFET is less than 1 µm (10—6 m), which means that MOSFETs are small devices. The oxide thickness t_{ox} is typically on the order of 400 angstroms, or less. The diagram in Figure1.27 is a simplified sketch of the basic structure of the transistor.

5.5.4. N-Channel MOSFET

- The n-channel D-MOSFET is a piece of n-type material with a p-type region (called substrate) on the right and an insulated gate on the left as shown in Fig.5.9. The free electrons (Q it is n-channel) flowing from source to drain must pass through the narrow channel between the gate and the p-type region.
- Note carefully the gate construction of D-MOSFET. A thin layer of metal oxide (usually silicon dioxide, SiO2) is deposited over a small portion of the channel. A metallic gate is deposited over the oxide layer. As SiO2 is an insulator, therefore, gate is insulated from the channel. Note that the arrangement forms a capacitor. One plate of this capacitor is the gate and the other plate is the channel with SiO2 as the dielectric.
- It is a usual practice to connect the substrate to the source (S) internally so that a MOSFET has three terminals that is source (S), gate (G) and drain (D).Since the gate is insulated from the channel; we can apply either negative or positive voltage to the gate. Therefore, D-MOSFET can be operated in both depletion-mode and enhancement-mode. However, JFET can be operated only in depletion-mode.

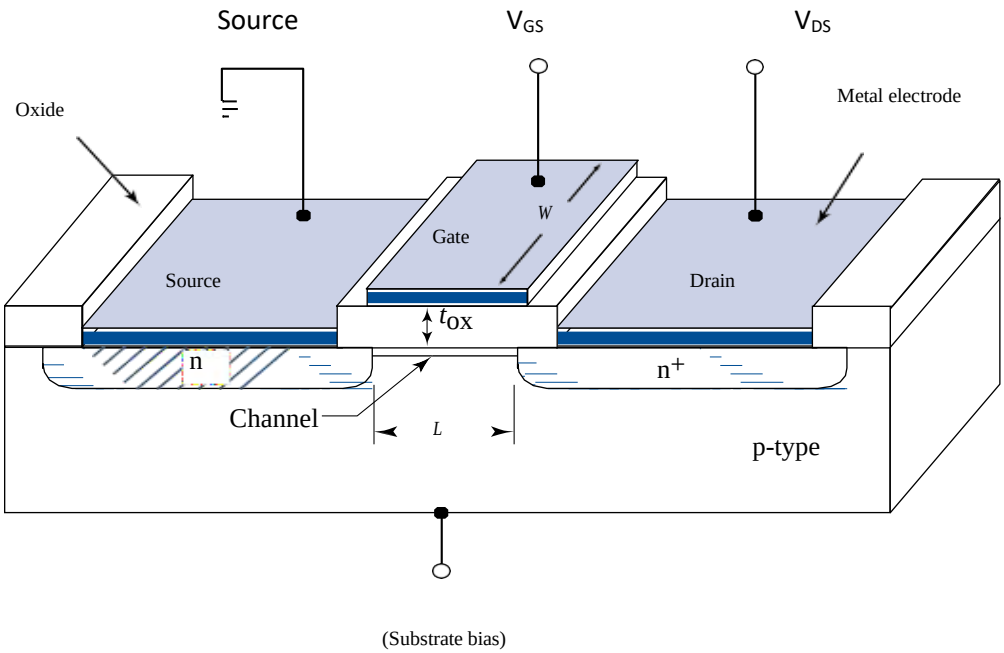


Figure.5.8. Schematic diagram of an n-channel enhancement mode MOSFET

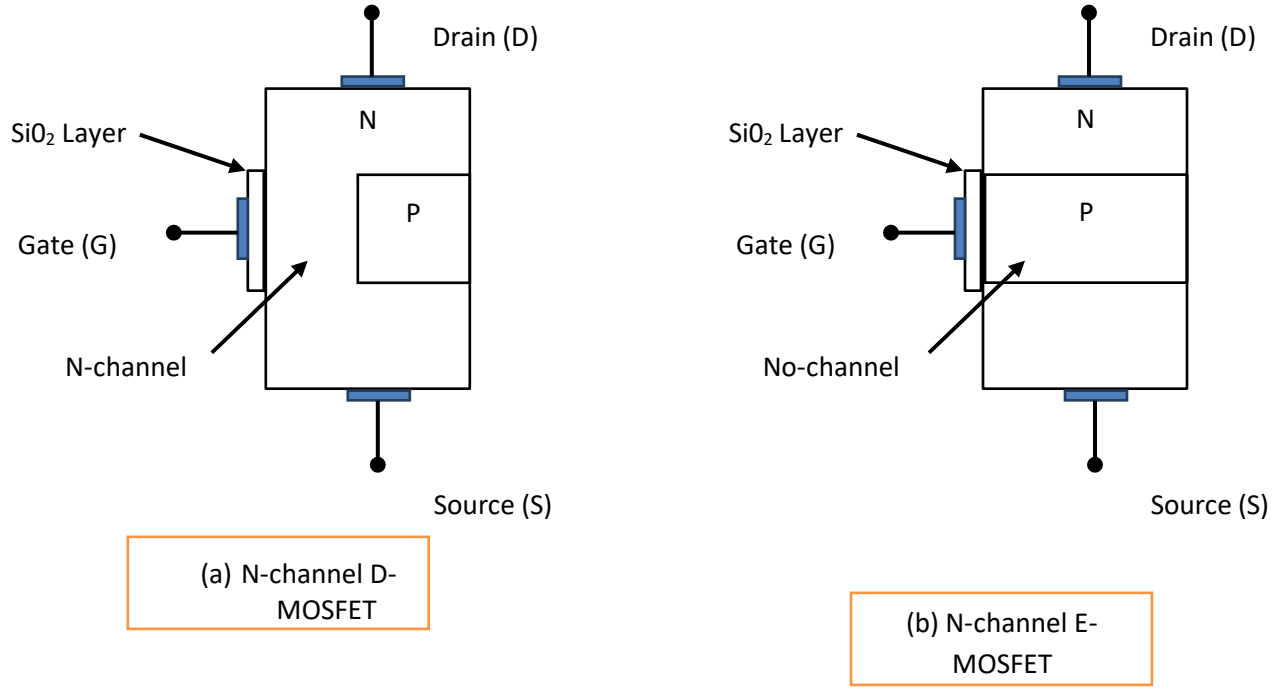


Figure.5.9. MOSFET construction

5.5.5. D-MOSFET

Fig.5.4 (a) shows the circuit of n-channel D-MOSFET. The gate forms a small capacitor. One plate of this capacitor is the gate and the other plate is the channel with metal oxide layer as the dielectric. When gate voltage is changed, the electric field of the capacitor changes, which in turn changes the resistance of the n-channel. Since the gate is insulated from the channel, we can apply either negative or positive voltage to the gate. The negative-gate operation is called depletion mode whereas positive gate operation is known as enhancement mode.

5.5.6. E-MOSFET

Fig. 5.4(b) shows the constructional details of n-channel E-MOSFET. Its gate construction is similar to that of D-MOSFET. The E-MOSFET has no channel between source and drain unlike the D-MOSFET. Note that the substrate extends completely to the SiO2 layer so that no channel exists. The E-MOSFET requires a proper gate voltage to form a channel (called induced channel). It is reminded that E-MOSFET can be operated only in enhancement mode. In short, the construction of E-MOSFET is quite similar to that of the D-MOSFET except for the absence of a channel between the drain and source terminals.

5.5.7. Depletion mode

Fig. 5.10 shows depletion-mode operation of n-channel D-MOSFET. Since gate is negative, it means electrons are on the gate as shown is Fig.1.26. These electrons repel the free electrons in the n-channel, leaving a layer of positive ions in a part of the channel. In other words, we have depleted (i.e. emptied) the n-channel of some of its free electrons. Therefore, lesser number of free electrons is made available for current conduction through the n-channel. This is the same thing as if the resistance of the channel is increased. The greater the negative voltage on the gate, the lesser is the current from source to drain.

Thus by changing the negative voltage on the gate, we can vary the resistance of the n-channel and hence the current from source to drain. Note that with negative voltage to the gate, the action of D-MOSFET is similar to JFET. Because the action with negative gate depends upon depleting (i.e. emptying) the channel of free electrons, the negative-gate operation is called depletion mode.

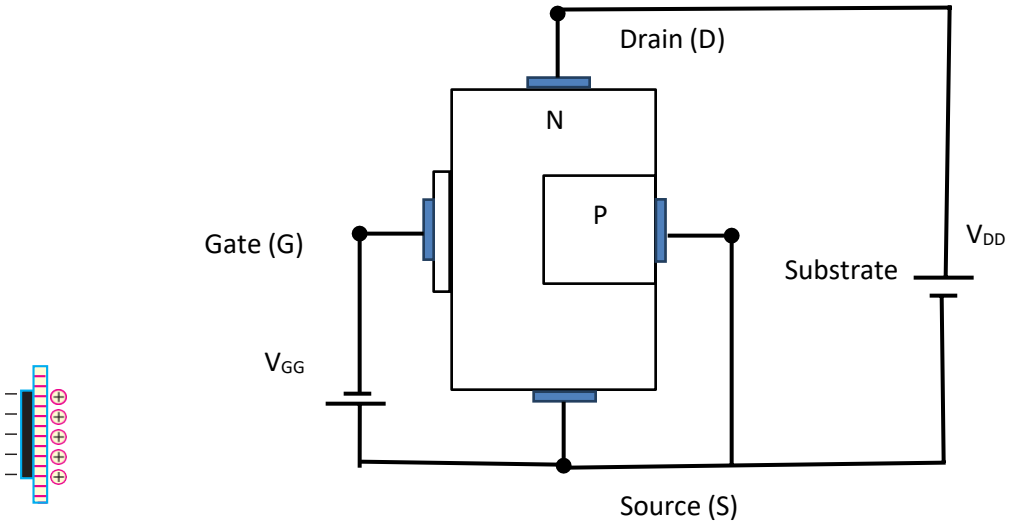


Figure.5.10. Depletion mode MOSFET

5.5.7. Enhancement mode:

Fig. 5.11 shows enhancement-mode operation of n-channel D- MOSFET. Again, the gate acts like a capacitor. Since the gate is positive, it induces negative charges in the n-channel. These negative charges are the free electrons drawn into the channel. Because these free electrons are added to those already in the channel, the total number of free electrons in the channel is increased. Thus a positive gate voltage enhances or increases the conductivity of the channel. Greater the positive voltage on the gate, greater the conduction from source to drain. Thus by changing the positive voltage on the gate, we can change the conductivity of the channel. The main difference between D-MOSFET and JFET is that we can apply positive gate voltage to D-MOSFET and still have essentially zero current. Because the action with a positive gate depends upon enhancing the conductivity of the channel, the positive gate operation is called enhancement mode.

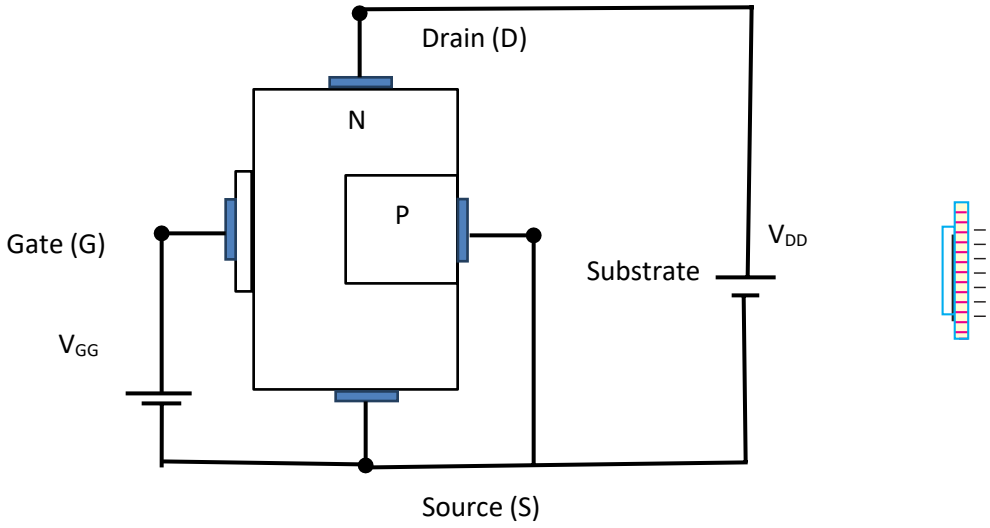


Figure.5.11. Enhancement mode MOSFET

The following points may be noted about D-MOSFET operation:

- In a D-MOSFET, the source to drain current is controlled by the electric field of capacitor formed at the gate.
- The gate of JFET behaves as a reverse-biased diode whereas the gate of a D-MOSFET acts like a capacitor. For this reason, it is possible to operate D-MOSFET with positive or negative gate voltage.

- As the gate of D-MOSFET forms a capacitor, therefore, negligible gate current flows whether positive or negative voltage is applied to the gate. For this reason, the input impedance of D-MOSFET is very high, ranging from 10,000 MΩ to 10,000,00 MΩ.
- The extremely small dimensions of the oxide layer under the gate terminal result in a very low capacitance and the D-MOSFET has, therefore, a very low input capacitance. This characteristic makes the D-MOSFET useful in high-frequency applications.

5.6. Drain and Transfer Characteristics of MOSFET:

DE-MOSFETs are classified as the depletion-mode devices because their conductivity depends on the action of depletion layers. E-MOSFET is classified as an enhancement-mode device because its conductivity depends on the action of the inversion layer. Depletion-mode devices are normally ON when the gate-source voltage $V_{GS} = 0$, whereas the enhancement-mode devices are normally OFF when $V_{GS} = 0$. In general, any MOSFET characteristics is seen to exhibit three operating regions viz.,

1. **Cut-Off Region:** Cut-off region is a region in which the MOSFET will be OFF as there will be no current flow through it. In this region, MOSFET behaves like an open switch and is thus used when they are required to function as electronic switches.
2. **Ohmic or Linear Region** Ohmic or linear region is a region where in the current I_{DS} increases with an increase in the value of V_{DS}. When MOSFETs are made to operate in this region, they can be used as amplifiers.
3. **Saturation Region** In saturation region, the MOSFETs have their I_{DS} constant inspite of an increase in V_{DS} and occur once V_{DS} exceeds the value of pinch-off voltage V_P. Under this condition, the device will act like a closed switch through which a saturated value of I_{DS} flows. As a result, this operating region is chosen whenever MOSFETs are required to perform switching operations.

5.6.1. N-Channel EMOSFET characteristics: Drain characteristics of an N-channel E-MOSFET are shown in figure. The lowest curve is the V_{GST} curve. When V_{GS} is lesser than V_{GST}, I_D is approximately zero. When V_{GS} is greater than V_{GST}, the device turns- on and the drain current I_D is controlled by the gate voltage and the current through the device increases with an increase in I_{DS} initially (Ohmic region) and then saturates to a value as determined by the V_{GS} (saturation region of operation) i.e. as V_{GS} increases, even the saturation current flowing through the device also increases. The characteristic curves have almost vertical and almost horizontal parts. The almost vertical components of the curves correspond to the ohmic region, and the horizontal components correspond to the constant current region. Thus E-MOSFET can be operated in either of these regions *i.e.* it can be used as a variable-voltage resistor (VVR) or as a constant current source.

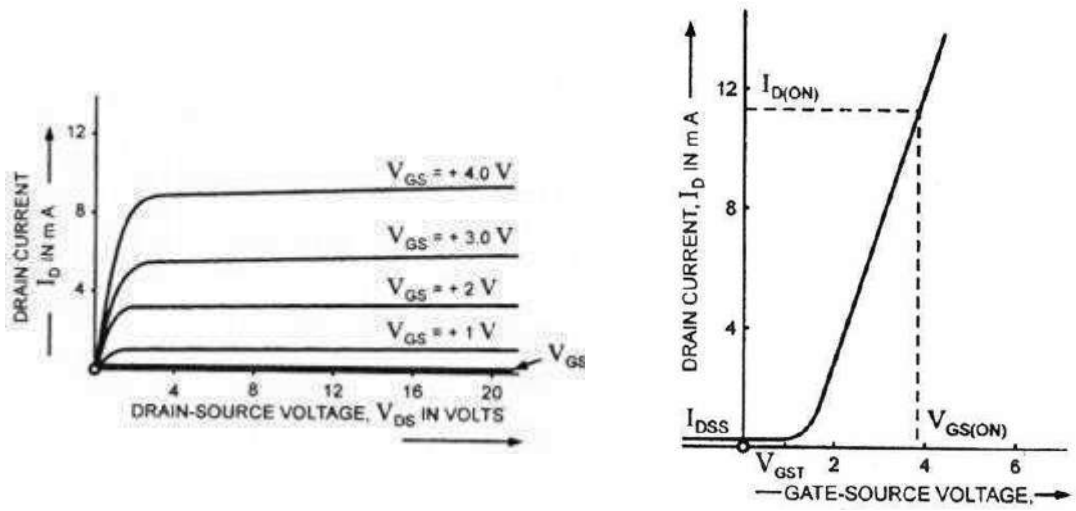


Figure.5.12. Drain and transfer Characteristics of EMOSFET

Transfer characteristics: The transconductance curve is shown in figure 5.12. The current I_{DSS} at V_{GS} <=0 is very small, being of the order of a few nano-amperes. When the V_{GS} is made positive, the drain current I_D increases slowly at first, and then much more rapidly with an increase in V_{GS}.

The equation for the transfer characteristic of E-MOSFETs is given as:

$$I_D=K(V_{GS}-V_{GST})^2$$

5.6.2. N-Channel DMOSFET characteristics:

The transfer characteristics of n-channel depletion MOSFET shown by Figure 5.13 indicate that the device has a current flowing through it even when V_{GS} is 0V. This indicates that these devices conduct even when the gate terminal is left unbiased, which is further emphasized by the V_{GS0} curve of Figure 5.13(b). Under this condition, the current through the MOSFET is seen to increase with an increase in the value of V_{DS} (Ohmic region) until V_{DS} becomes equal to pinch-off voltage V_P. After this, I_{DS} will get saturated to a particular level I_{DSS} (saturation region of operation) which increases with an increase in V_{GS} i.e. I_{DSS3} > I_{DSS2} > I_{DSS1}, as V_{GS3} > V_{GS2} > V_{GS1}. Further, the locus of the pinch-off voltage also shows that V_P increases with an increase in V_{GS}. However it is to be noted that, if one needs to operate these devices in cut-off state, then it is required to make V_{GS} negative and once it becomes equal to $-V_T$, the conduction through the device stops (I_{DS} = 0) as it gets deprived of its n-type channel (Figure 5.13(a)).

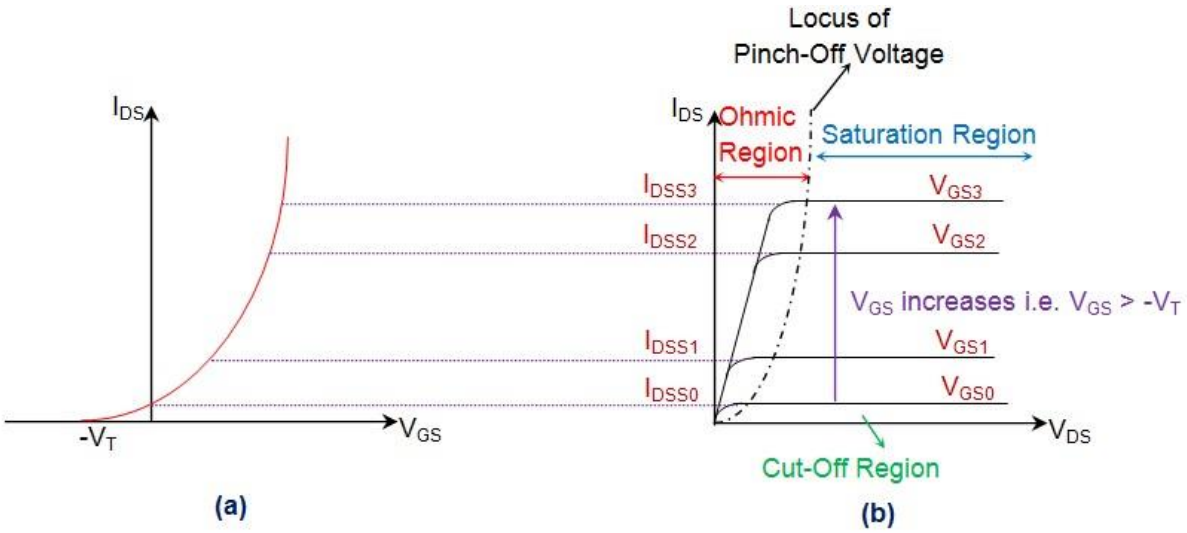


Figure.5.13.N-Channel D-MOSFET characteristics

5.7. Unijunction Transistor (UJT):

The Unijunction transistor (UJT) is a three terminal device having one emitter and two base contacts. It is also known as double-base diode because it is a 2-layered, 3-terminal solid-state switching device. It has only one junction so it is called as a uni-junction device. This device has a unique characteristics that when it is triggered, the emitter current increases regeneratively until it is limited by emitter power supply. Due to this characteristics, the uni-junction transistor can be employed in a variety of applications e.g., switching, pulse generator, saw-tooth generator etc.

5.7.1. Construction of UJT

Fig.5.14 shows the basic structure of a uni-junction transistor. It consists of an n-type silicon bar with an electrical connection on each end. The leads to those connections are called base leads base-one B_1 and base two B_2. Part way along the bar between the two bases, nearer to B_2 than B_1.a PN junction is formed between a p-type emitter and the bar. The lead to this junction is called the emitter lead E. The emitter is heavily doped having many holes. The n-region, however, is lightly doped. For this reason, the resistance between the base terminals is very high when emitter lead is open.

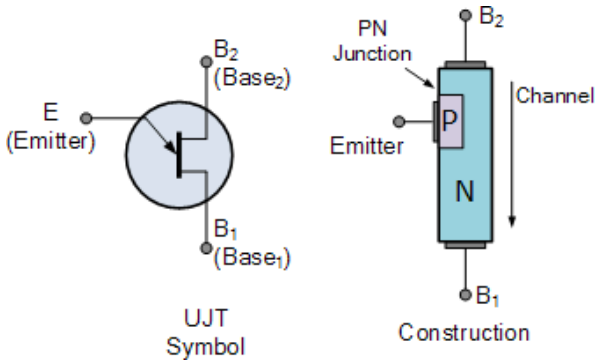


Figure.5.14. UJT construction

5.7.2. Equivalent circuit of UJT:

The voltage applied at the emitter is indicated as V_E and the internal resistances are indicated as R_{B1} and R_{B2} at bases 1 and 2 respectively. Both resistances present internally are together called as intrinsic resistance, indicated as R_{BB}. The voltage across RB1 can be denoted as V_1. The dc voltage applied for the circuit to function is V_{BB}. The UJT equivalent circuit is as given below in figure 5.15.

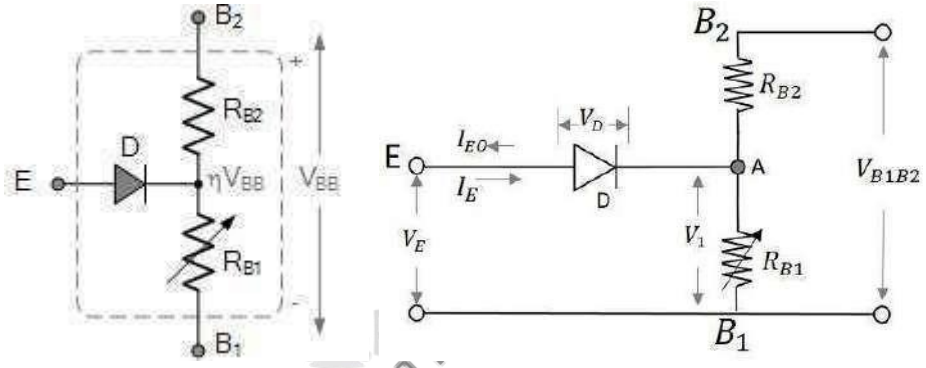


Figure.5.15. Equivalent Circuit of UJT

(i) With no voltage applied to the UJT, the inter-base resistance is given by ;

$$R_{BB} = R_{B1} + R_{B2}$$

(ii) If a voltage V_{BB} is applied between the bases with emitter open, the voltage will divide up across R_{B1} and R_{B2}.

Voltage across R_{B1},

$$V_1 = \frac{R_{B1}}{R_{B1} + R_{B2}} V_{BB}$$

The ratio V1/ V_{BB} is called intrinsic stand-off ratio and is represented by η.
Hence,

$$\eta = \frac{R_{B1}}{R_{B1} + R_{B2}}$$

The value of η lies between 0.51 and 0.82.

So voltage across $R_{B1} = \eta V_{BB}$

The voltage ηV_{BB} appearing across R_{B1} reverse biases the diode. Therefore, the emitter current is zero.

(iii) If now a progressively rising voltage is applied to the emitter, the diode will become forward biased when input voltage exceeds ηV_{BB} by V_D, the forward voltage drop across the silicon diode

i.e.

$$V_P = \eta V_{BB} + V_D$$

5.7.2. Principle of operation and characteristics:

The device has normally B_2 positive with respect to B_1.

(i) If voltage V_{BB} is applied between B_2 and $B_1$with emitter open, a voltage gradient is established along the n-type bar. Since the emitter is located nearer to B_2, more than half of V_{BB} appears between the emitter and B_1. The voltage V_1 between emitter and B_1 establishes a reverse bias on the PN junction and the emitter current is cut off. A small leakage current flows from B_2 to emitter due to minority carriers.

(ii) This transistor operation starts by making the emitter supply voltage to zero, and its emitter diode is reverse biased with the intrinsic stand-off voltage. If V_B is the voltage of the emitter diode, then the total reverse bias voltage is $V_1 + V_B = \eta V_{BB} + V_D$. For silicon $V_D = 0.7$ V.

(iii) If a positive voltage is applied at the emitter, the PN junction will remain reverse biased so long as the input voltage is less than V_1.If the input voltage to the emitter exceeds V_1, the PN junction becomes forward biased. Under these conditions, holes are injected from p-type material into the n-type bar. These holes are repelled by positive B_2 terminal and they are attracted towards B_1 terminal of the bar. This accumulation of the holes in the emitter to B_1 region results in the decrease of resistance in this section of the bar. The result is that internal voltage drop from emitter to B_1 is decreased and hence the emitter current I_E increases.

(iv) As more holes are injected, a condition of saturation will eventually be reached. At this point, the emitter current is limited by emitter power supply only. The device is now in the ON sate.

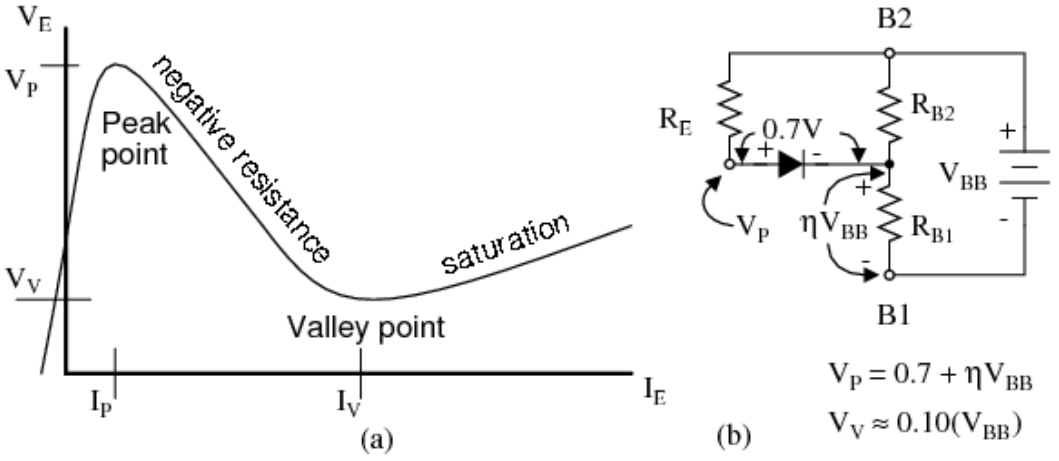


Figure.5.16 (a) Characteristics of UJT;(b)UJT model for V_p

(v) The Unijunction emitter current vs voltage characteristic curve (Figure.5.16) shows that as V_E increases, current I_E increases up I_P at the peak point. Beyond the peak point, current increases as voltage decreases in the negative resistance region. The voltage reaches a minimum at the valley point. The resistance of R_{B1}, the saturation resistance is lowest at the valley point.

5.8. UJT relaxation oscillator:

The relaxation oscillator in Figure 5.17 is an application of the UJT oscillator.

Operation of UJT Oscillator:

(i) When a voltage (V_s) is firstly applied, the UJT is "OFF" and the capacitor C1 is fully discharged but begins to charge up exponentially through resistor R3.

(ii) As the Emitter of the UJT is connected to the capacitor, when the charging voltage V_c across the capacitor becomes greater than the diode volt drop value, the p-n junction behaves as a normal diode and becomes forward biased triggering the UJT into conduction. The UJT is "ON". At this point the Emitter to B1 impedance collapses as the Emitter goes into a low impedance saturated state with the flow of Emitter current through R1 taking place.

(iii) As the ohmic value of resistor R1 is very low, the capacitor discharges rapidly through the UJT and a fast rising voltage pulse appears across R1. Also, because the capacitor discharges more quickly through the UJT than it does charging up through resistor R3, the discharging time is a lot less than the charging time as the capacitor discharges through the low resistance UJT.

(iv) When the voltage across the capacitor decreases below the holding point of the p-n junction (V_{OFF}), the UJT turns "OFF" and no current flows into the Emitter junction so once again the capacitor charges up through resistor R3 and this charging and discharging process between V_{ON} and V_{OFF} is constantly repeated while there is a supply voltage, V_s applied.

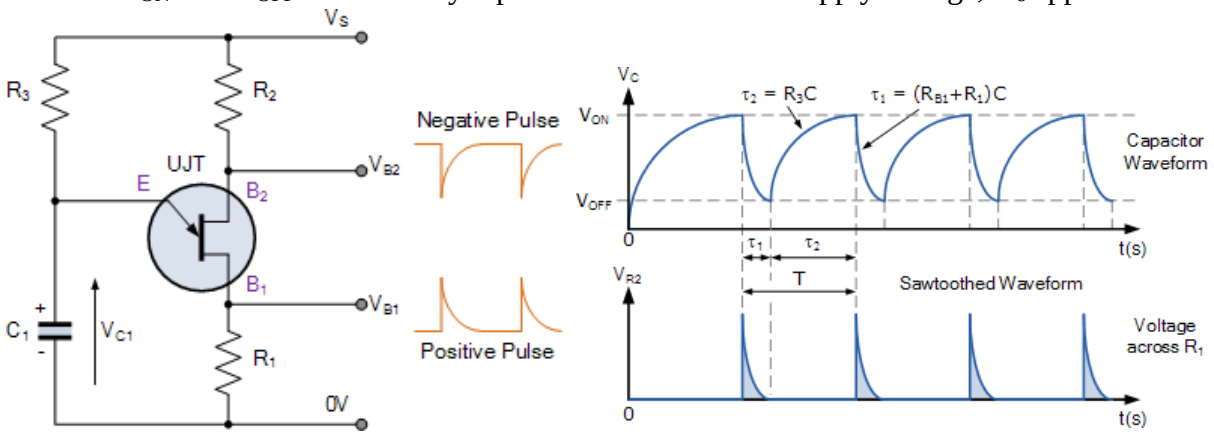


Figure.5.17. UJT relaxation Oscillator and waveforms

5.9. Thyristor:

It is a multi-layer semiconductor device, requires a gate signal to turn it "ON", and once "ON" it behaves like a rectifying diode. The Thyristor is a four layer (P-N-P-N) semiconductor device that contains three PN junctions in series, and is represented by the symbol as shown. It is a unidirectional device that is it will only conduct current in one direction and only in the switching mode and cannot be used for amplification. The thyristor is a three-terminal device labeled as "Anode", "Cathode" and "Gate" and consisting of three PN junctions which can be switched "ON" and "OFF" at an extremely fast rate.

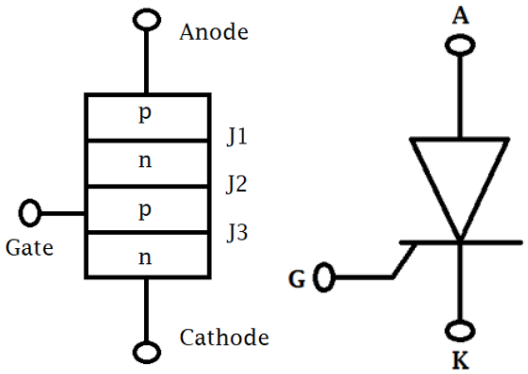


Figure.5.18.Thyristor and its symbol

5.9.1. V-I Characteristics of Thyristor or SCR:

The basic circuit for obtaining Thyristor V-I characteristics is given below, the anode and cathode of the Thyristor are connected to main supply through the load. The gate and cathode of the Thyristor are fed from a source Es, used to provide gate current from gate to cathode.

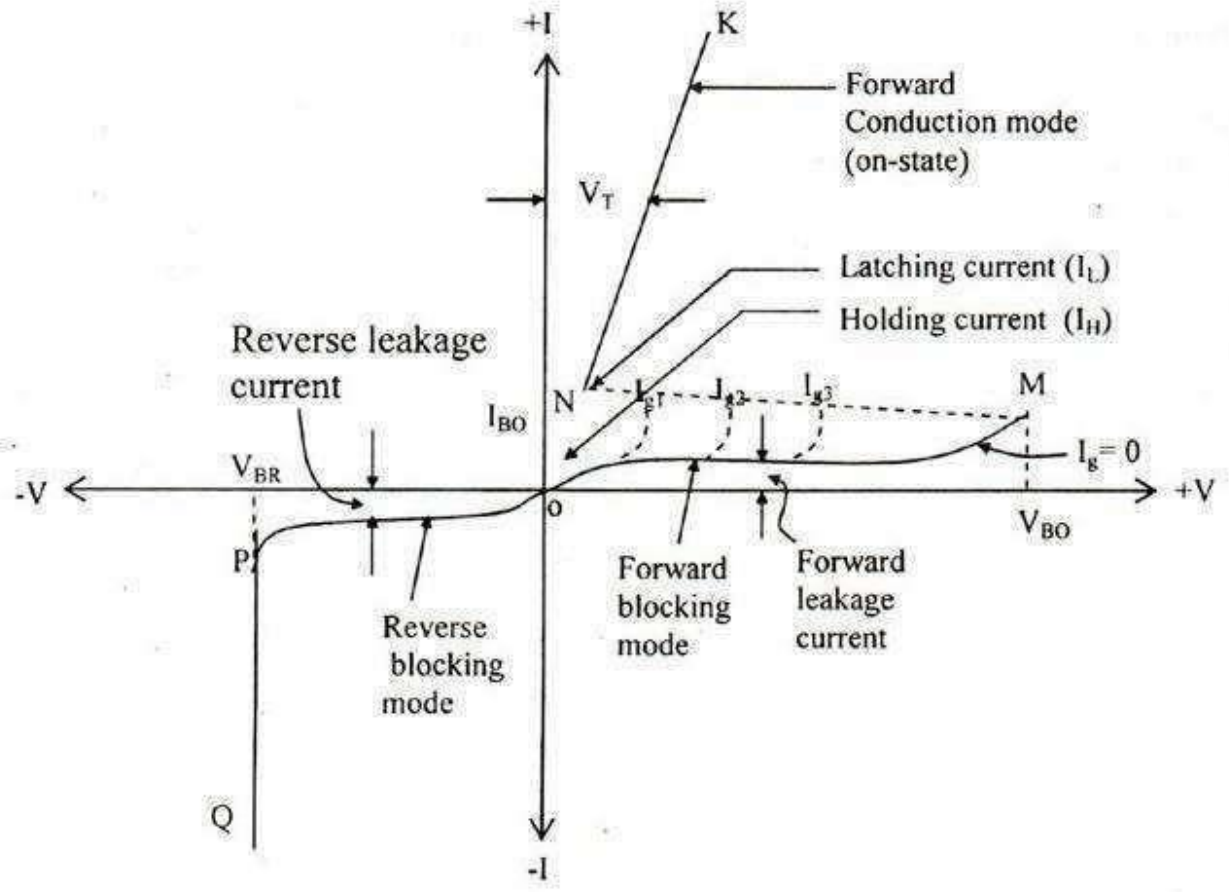


Figure.5.19.VI characteristics of Thyristor

As per the characteristic diagram, there are three basic modes of SCR: reverse blocking mode, forward blocking mode, and forward conduction mode.

Reverse Blocking Mode: In this mode the cathode is made positive with respect to anode with switch S open. Junction J1 and J3 are reversed biased and J2 is forward biased. When reverse voltage applied across Thyristor (should be less than V_{BR}), the device offers a high impedance in the reverse direction. Therefore, Thyristor treated as open switch in the reverse blocking mode. V_{BR} is the reverse breakdown voltage where the avalanche occurs, if voltage exceeds V_{BR} may cause to Thyristor damage.

Forward Blocking Mode: When anode is made positive with respect to cathode, with gate switch open. Thyristor is said to be forward biased, junction J1 and J3 are forward biased and J2 is reversed biased as you can see in figure. In this mode, small current flows called forward leakage current, as the forward leakage current is small and not enough to trigger the SCR. Therefore, SCR is treated as open switch even in forward blocking mode.

Forward Conduction Mode: As the forward voltage is increased with gate circuit remain open, an avalanche occurs at junction J2 and SCR comes into conduction mode. We can turn ON the SCR at any moment by giving a positive gate pulse between gate and cathode or by a forward break over voltage across anode and cathode of the Thyristor.