RAJIV GANDHI PROUDYOGIKI VISHWAVIDYALAYA, BHOPAL

New Scheme Based On AICTE Flexible Curricula

Electronics & Communication Engineering IV-Semester

EC405 Analog Circuits

COURSE CONTENTS:

Feedback Amplifier and Oscillators: Concept of feedback and their types, Amplifier with negative feedback and its advantages. Feedback Topologies.

Oscillators: Concept of Positive feedback, Classification of Oscillators, Barkhausen criterion, Types of oscillators: RC oscillator, RC Phase Shift, Wien Bridge Oscillators. LC Oscillator: Hartley, Colpitt's, Clapp and Crystal oscillator.

Introduction to integrated circuits: Advantages and characteristic parameters of IC's, basic building components, data sheets

Operational Amplifier: Differential amplifier and analysis, Configurations- Dual input balanced output differential amplifier, Dual input Unbalanced output differential amplifier, Single input balanced output differential amplifier, Single input Unbalanced output differential amplifier Introduction of op-amp, Block diagram, characteristics and equivalent circuits of an ideal opamp, Power supply configurations for OP-AMP.

Characteristics of op-amp: Ideal and Practical, Input offset voltage, offset current, Input bias current, Output offset voltage, thermal drift, Effect of variation in power supply voltage, common-mode rejection ratio (CMRR), Slew rate and its Effect, PSRR and gain bandwidth product, frequency limitations and compensations, transient response, analysis of TL082 datasheet.

OP-AMP applications: Inverting and non-inverting amplifier configurations, Summing amplifier, Integrators and differentiators, Instrumentation amplifier, Differential input and differential output amplifier, Voltage-series feedback amplifier, Voltage-shunt feedback amplifier, Log/ Antilog amplifier, Triangular/rectangular wave generator, phase-shift oscillators, Wein bridge oscillator, analog multiplier-MPY634, VCO, Comparator, Zero Crossing Detector. OP-AMP AS FILTERS: Characteristics of filters, Classification of filters, Magnitude and frequency response, Butterworth 1st and 2nd order Low pass, High pass and band pass filters, Chebyshev filter characteristics, Band reject filters, Notch filter; all pass filters, self-tuned filters, AGC,AVC using op-AMP.

TIMER:IC-555 Timer concept, Block pin configuration of timer. Monostable, Bistable and AstableMultivibrator using timer 555-IC, Schmitt Trigger, Voltage limiters, Clipper and

clampers circuits, Absolute value output circuit, Peak detector, Sample and hold Circuit, Precision rectifiers, Voltage-to-current converter, Current-to-voltage converter.

Voltage Regulator: simple OP-AMP Voltage regulator, Fixed and Adjustable Voltage Regulators, Dual Power supply, Basic Switching Regulator and characteristics of standard regulator ICs such as linear regulator, Switching regulator andlow-drop out regulator. Study of LM317, TPS40200 and TPS7250

TEXT BOOKS:

1. RamakantA.Gaikward,"OP- Amp and linear Integrated circuits" Third edition 2006, Pearson.
2. B. Visvesvara Rao Linear Integrated Circuits Pearson.
3. http://www.nptelvideos.in/2012/11/analog-ics.html
4. http://nptel.ac.in/courses/117108107/

REFERENCES:

1. David A. Bell: Operational Amplifiers & Linear ICs, Oxford University Press, 2nd edition,2010.
2. D. Roy Choudhury:Linear Integrated Circuits New Age Publication.
3. B. Somanathan Nair: Linear Integrated Circuits analysis design and application Wiley India Pvt. Ltd.
4. Maheshwary and Anand: Analog Electronics, PHI.
5. S.Salivahanan,V S KanchanaBhaaskaran: Linear Integrated Circuits",second edition, McGraw Hill.
6. Gray Hurst Lewis Meyer Analysis and design of analog Integrated Circuits fifth edition Wiley India.
7. RobertF.Coughlin, Frederick,F.Driscoll: Operational Amplifiers and Linear Integrated Circuits, sixth edition, Pearson.
8. Millman and Halkias: Integrated electronics, TMH.
9. Boylestad and Nashelsky: Electronic Devices and Circuit Theory, Pearson Education.
10. Sedra and Smith: Microelectronics, Oxford Press.

List of Experiments :

Apparatus Required –Dual Channel Cathode Ray Oscilloscope (0-20 MHz), Function Generator (10MHz and above), Dual Power Supply, LM741, TL082, MPY634,TPS7250, Probes, digital multimeter.

1. To measure and compare the op-amp characteristics: offset voltages, bias currents, CMRR, Slew Rate of OPAMP LM741 and TL082.
2. To determine voltage gain and frequency response of inverting and non-inverting amplifiers using TL082.
3. To design an instrumentation amplifier and determine its voltage gain using TL082.
4. To design op-amp integrator (low pass filter) and determine its frequency response.
5. To design op-amp differentiator (high pass filter) and determine its frequency response.

6. Design 2nd order Butterworth filter using universal active filter topology with LM741
7. To design Astable, Monostable and Bistablemultivibrator using 555 and analyse its characteristics.
8. Automatic Gain Control (AGC) Automatic Volume Control (AVC)using multiplier MPY634
9. To design a PLL using opampwith MPY634 anddetermine the free running frequency, the capture range and the lock in range of PLL
10. Design and test a Low Dropout regulator using op-amps for a given voltage regulation characteristic and compare the characteristics with TPS7250 IC.

RGPV University

Department of Electronics and Communication Engineering

Subject Name: Analog Circuits **Subject Code**: EC405

Subject Notes

Operational Amplifier: Differential amplifier and analysis, Configurations- Dual input balanced output differential amplifier, Dual input Unbalanced output differential amplifier, Single input balanced output differential amplifier, Single input Unbalanced output differential amplifier . Introduction of op-amp, Block diagram, characteristics and equivalent circuits of an ideal op-amp, Power supply configurations for OP-AMP.

Differential Amplifier: An amplifier which amplifies the difference between the two input signals is differential amplifier. It is the basic building block of operational amplifier.

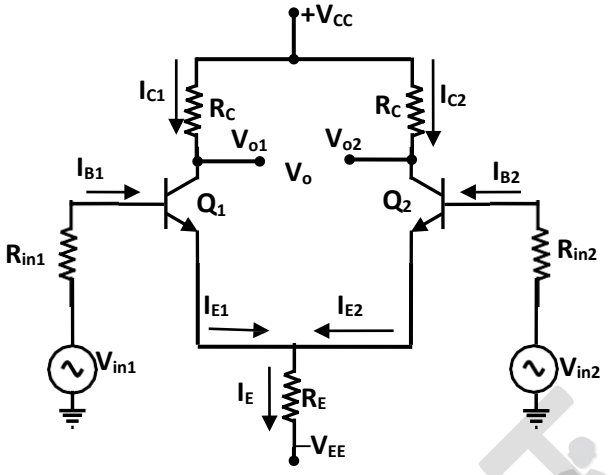


Figure 3.1: Emitter coupled Differential Amplifier

Figure 3.1 shows the circuit diagram of emitter coupled differential amplifier. Emitters of transistor Q_1 and Q_2 are connected to a single resistor R_E. It has two input terminals, inverting and non-inverting inputs. Amplifier output is a function of the difference of the two input signals. Differential amplifier is capable of handling very low frequency signals and DC signals also because no coupling capacitors are used. A few basic assumptions have to be made to understand the analysis and operation of a differential amplifier. It is assumed that Q_1 and Q_2 are matched on the basis of their transconductance curve and current gain β. It is also assumed that transistors are operating at same temperature and the supply voltages V_{CC} and V_{EE} are equal in magnitudes. Also assumed that the value of resistors are same if their subscript are same.

Operation of transistor differential amplifier: The operation of a transistorised differential amplifier can be understood by considering different operating conditions existing in the circuit. Figure shows the circuit diagram of an emitter coupled differential amplifier. It consists of two identical NPN transistors biased by $+V_{CC}$ and $-V_{EE}$ supply voltages of equal magnitudes and common to both. Both the collector resistors are identical and the emitter resistance is common to both the transistors. The value of R_E is quite large to ensure that in conjunction with $-V_{EE}$. It behave like a constant current source. The current through R_E is almost constant and is given by the relation: $I_E = [V_{EE}/R_E]$. As the two transistors are identical their emitter currents $I_{E1}=I_{E2}$ and $I_{E1}+I_{E2}=I_E$. V_{in1} and V_{in2} are the two input signal sources with R_{in1} and R_{in2} as the source resistances. The input signals are applied at the base of the two transistors Q_1 and Q_2. The output voltage can be taken either between the two collectors or between any one of the two collectors and the ground. In this circuit the output voltage is proportional to the difference of the two input voltages, ie. the output voltage will be zero if the two input voltages are equal.

When $V_{in1} = V_{in2}$, $I_{B1} = I_{B2}$ and $I_{C1} = I_{C2}$, since both the collector resistances are equal the collector voltages of both the transistors will be equal ie. $V_{O1} = V_{O2}$. This results in an output voltage $V_O = 0$.

When $V_{in1} > V_{in2}$, $I_{B1} > I_{B2}$ and $I_{C1} > I_{C2}$, as both the collector resistances have equal values the output voltage V_O will be proportional to the difference of the two input voltages.

When the input voltage V_{in1} is applied at the base of Q_1 with the base of Q_2 grounded, transistor Q_1 acts like a common-emitter amplifier and an amplified , inverted output voltage V_{O1} is obtained at the collector of Q_1 ie $V_{O1} = A_D(V_{in1})$. Thus the input voltage V_{in1} produces output voltages of equal amplitudes but with opposite polarities because the base-emitter voltages of both the transistors are equal in magnitude with opposite polarities. In a similar way, an input voltage V_{in2} applied independently at the base of transistor Q_2 with the base of Q_1 grounded produces an output voltage $V_{O2} = A_D.(V_{in2})$.

When both the input voltages are simultaneously applied, the output voltage can be determined using the super position theorem and is given by the expression: $V_O=A_D.(V_{in1}-V_{in2})$, where A_D is the differential voltage gain of the

in1

amplifier. It is observed in a differential amplifier that when a positive input voltage V is independently applied

at the base of Q_1, it produces a negative output voltage at V_{O1} and this input terminal is known as the Inverting input terminal. When a positive input voltage V_{in2} is independently applied at the base of Q_2, it produces a positive output voltage at V_{O1} and this input terminal is known as the Non-Inverting Input terminal. This is known as Differential Input. When the same input signal (same phase) is applied at both the inputs, then the amplifier is said to have a Common Mode Input. In this case the differential amplifier produces a zero output and is said to be perfectly balanced.

h-PARAMETER ANALYSIS OF EMITTER COUPLED DIFFERENTIAL AMPLIFIER:

The performance of the differential amplifier is evaluated by knowing the values of the differential mode gain, Common mode gain and the common mode rejection ratio.

Differential mode gain (A_{DM}):

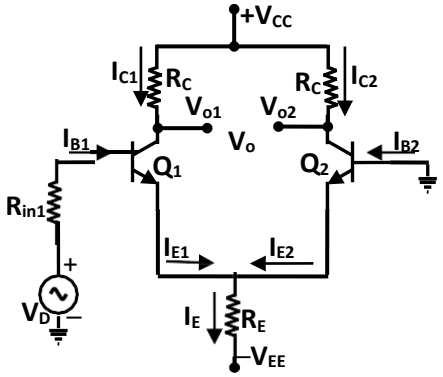


Figure 3.2: Differential Mode Gain

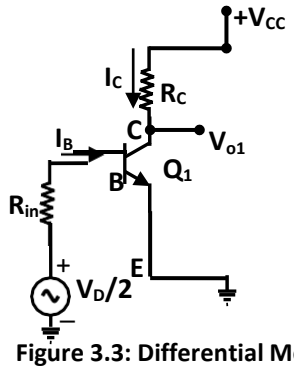


Figure 3.3: Differential Mode Half Circuit

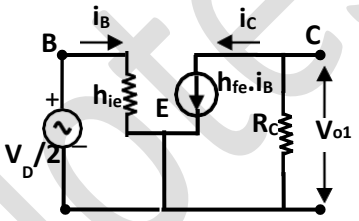


Figure 3.4: h-parameter model

When a differential mode input is applied as shown in figure 3.2, the input signals appearing at the base of the two transistors are out of phase with one another (ie. Input signal is applied at one input while the other input is grounded), hence transistor Q_1 gets a positive going signal while Q_2 gets a negative going signal. This means that the forward bias on the base-emitter junction increases to produce an increase in base current i_{B1} and thereby an increase in collector current i_{C1} and emitter current i_{E1}. At the same time the forward bias on the base-emitter junction decreases to produce a decrease in base current i_{B2} and thereby a decrease in its collector current i_{C2} and emitter current i_{E2}. An increase in transistor currents i_{B1} and i_{C1} (also i_{E1}) of Q_1 is exactly equal to the decrease in transistor currents i_{B2} and i_{C2}(also i_{E2}) of Q_2 because the sum of the two transistor currents is always a constant & equal to the emitter current i_E. The value of emitter current i_E through R_E remains unchanged irrespective of increase or decrease in the two transistor currents. This results in a constant emitter voltage. Thus for small signal h-parameter analysis we consider only the half circuit of the differential mode as shown in Figure 3.3 and assume that the emitter is at ground potential without any emitter resistance (ie. $R_E = 0$). The approximate small signal equivalent circuit or the approximate h-parameter model of the differential mode half circuit is as shown in Figure 3.4.

From the base-emitter input circuit we have: $V_D/2 = i_B.h_{ie}$

From the collector-emitter output circuit we have: $V_{O1} = -i_C.R_C = -h_{fe}.i_B.R_C$ ie. $V_{O1} = -h_{fe}.i_B.R_C$

The differential mode gain, A_{DM} for unbalanced or single ended output (Q1) is given by:

$$A_{DM} = \frac{V_{O1}}{V_D} \quad \text{ie.}\, A_{DM} = \frac{-h_{fe} i_B R_C}{2 i_B h_{ie}} \quad \text{ie.}\, A_{DM} = \frac{-h_{fe} R_C}{2 h_{ie}}$$

Similarly the differential mode gain for the other unbalanced or single ended output (Q2) is given by:

$$A_{DM} = \frac{V_{O2}}{V_D} \quad \text{ie.}\, A_{DM} = \frac{h_{fe} i_B R_C}{2 i_B h_{ie}} \quad \text{ie.}\, A_{DM} = \frac{h_{fe} R_C}{2 h_{ie}}$$

The differential mode gain for balanced or double ended output is given by:

$$A_{DM} = \frac{V_{O1} - V_{O2}}{V_D} \quad \text{ie.}\, A_{DM} = \frac{-h_{fe} i_B R_C - h_{fe} i_B R_C}{2 i_B h_{ie}} \quad \text{ie.}\, A_{DM} = \frac{-h_{fe} R_C}{h_{ie}}$$

Common Mode Gain (A_{CM}): When a common mode input is applied as shown in Figure 3.5 (Input signal V_C is applied simultaneously at base of transistor Q_1 as well as the base of transistor Q_2) the input signals appearing at the base of the two transistors are in phase with one another. With this type of input both transistors Q_1 and Q_2 simultaneously get either a positive going signal or a negative going signal. This means that the forward bias on

the base-emitter junction of transistors Q_1 and Q_2 increases or decreases simultaneously thereby causing a simultaneous increase or decrease in collector currents i_{C1} and i_{C2} (also emitter currents i_{E1} and i_{E2}). The value of emitter current i_E through R_E will be equal to the sum of the two emitter currents i_{E1} and i_{E2} ie. $i_E = [i_{E1} + i_{E2}]$, since $i_{E1} = i_{E2} = i$ the net emitter current $i_E = (2.i)$. Thus the emitter current gets doubled and results in a doubled emitter voltage .

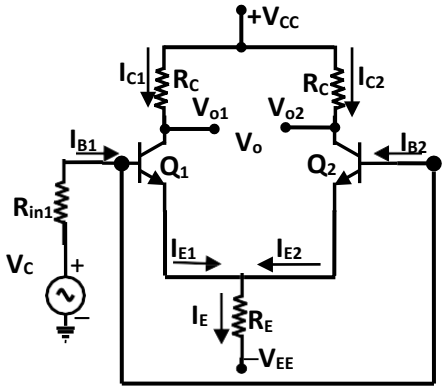


Figure 3.5: Common Mode Gain

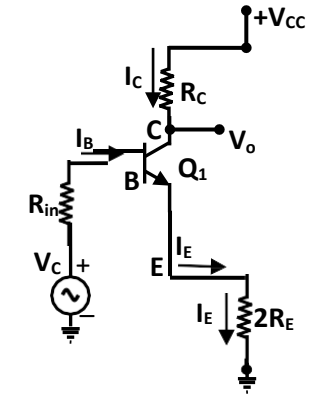


Figure 3.6: Common Mode Half Circuit

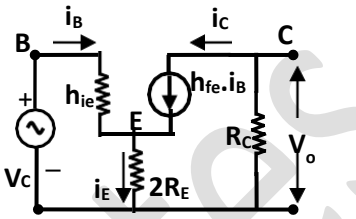


Figure 3.7: h-parameter model

In order to carry out the small signal h-parameter analysis we consider only the half circuit of the common mode configuration as shown in Figure 3.6 and also consider that the emitter resistance is doubled ($2.R_E$) to take care of the doubled emitter current and voltage. The approximate small signal equivalent circuit or the approximate h-parameter model of the common mode half circuit is as shown in Figure 3.7.

From Figure 3.7 , we have : $i_E = (i_B + i_C) = (i_B + i_B.h_{fe}) = i_B(1 + h_{fe})$

ie. : $\mathbf{i_E = [i_B(1 + h_{fe})]}$

From the base-emitter input circuit we have: $V_C = [i_B.h_{ie} + i_E.(2.R_E)] = [i_B.h_{ie} + i_B(1 + h_{fe}).(2.R_E)]$

ie. $V_C = i_B.[h_{ie} + (1 + h_{fe}).(2.R_E)]$

From the collector-emitter output circuit we have :$V_{O1} = - i_C.R_C = - h_{fe}.i_B.R_C$ ie. **$V_{O1} = [- h_{fe}.i_B.R_C]$**

The common mode gain , A_{CM} for unbalanced or single ended output (Q1) is given by the expression:

$$A_{CM} = \frac{V_{o1}}{V_C} \quad \text{ie.} \quad A_{CM} = \frac{-h_{fe} i_B R_C}{i_B[h_{ie} + (1 + h_{fe})(2R_E)]} \quad \text{ie.} \quad A_{CM} = \frac{-h_{fe} R_c}{[h_{ie} + (1 + h_{fe})2R_E]}$$

Similarly the common mode gain for the other unbalanced or single ended output (Q2) is given by:

$$A_{CM} = \frac{V_{o2}}{V_C} \quad \text{ie.} \quad A_{CM} = \frac{-h_{fe} i_B R_C}{i_B[h_{ie} + (1 + h_{fe})(2R_E)]} \quad \text{ie.} \quad A_{CM} = \frac{-h_{fe} R_c}{[h_{ie} + (1 + h_{fe})2R_E]}$$

Common Mode Rejection Ratio (CMRR): CMRR represents the performance factor of an op-amp. An op-amp should not amplify noise signals appearing at its input terminals. A measure of this noise rejecting capability of an op-amp is known as the Common Mode Rejection and a numerical value assigned to this capability is known as the CMRR. The CMRR of an op-amp gives an idea about how well a differential mode signal is amplified and how well a common-mode signal is rejected. Thus for an ideal op-amp the CMRR should be infinite. CMRR is a frequency dependent parameter and its value reduces with an increase in frequency, which means that the noise rejecting capability of an op-amp is poor at higher operating frequencies.

CMRR is also defined as the ratio of the Differential Mode Gain (A_{DM}) to the Common Mode Gain (A_{CM}),

ie. **$\mathbf{CMRR = [A_{DM}/A_{CM}]}$.**

Expressed in dB, CMRR is given by the expression: **$\mathbf{CMRR = [20.\ log_{10}\ .(A_{DM}/A_{CM})]}$.**

CMRR = **$\mathbf{[A_{DM}/A_{CM}]}$.** On substituting the expression of A_{DM} and A_{CM} we get,

$$\text{CMRR} = \frac{-h_{fe}R_C}{h_{ie}} \div \frac{-h_{fe}R_c}{[h_{ie} + (1 + h_{fe})2R_E]} \quad \text{ie. CMRR} = \frac{[h_{ie} + (1 + h_{fe})2R_E]}{h_{ie}}$$

But $(1 + h_{fe})$ is approximately equal to (h_{fe}) because ($h_{fe} >> 1$), hence,

$$\text{CMRR} = \frac{[h_{ie} + (h_{fe})2R_E]}{h_{ie}} \quad \text{ie. CMRR} = 1 + \frac{(h_{fe})2R_E}{h_{ie}} \approx \frac{(h_{fe})2R_E}{h_{ie}}$$

$$\therefore CMRR \approx \frac{(h_{fe})2R_E}{h_{ie}}$$

DIFFERENTIAL AMPLIFIER CONFIGURATIONS : Differential amplifiers can be used in different configurations to suit different requirements. Variation in differential amplifier configurations is based on the number of input signals used and the way in which output voltage is measured. When one input signal is used, it is known as a single input or single ended configuration and when two inputs are used it is known as a dual input or double ended configuration. When the output voltage is taken across any one of the collectors and the ground, it is known as unbalanced output and when the output voltage is taken across the two collectors, it is known as the balanced output configuration. Based on these conditions, there are four important differential amplifier configurations, they are : a) Single input balance output differential amplifier. b) Single input unbalance output differential amplifier c) Dual input balance output differential amplifier d) Dual input unbalance output differential amplifier.

A) Single Input Balance Output Differential Amplifier: In this amplifier as shown in figure 3.8, input is applied to one of the base of transistor, say Q_1 and base of Q_2 is grounded. The output is measured between two collectors, which are at the same DC potential. Therefore the output is said to be balanced output.

AC analysis of amplifier: AC equivalent circuit of the Single Input Balance Output differential amplifier with a small signal T-equivalent model is shown in figure 3.9 below.

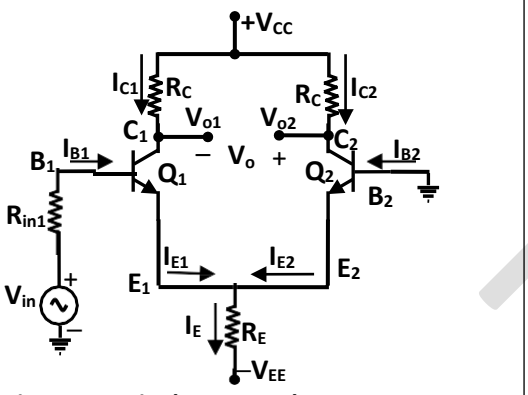


Figure 3.8: Single Input Balance Output

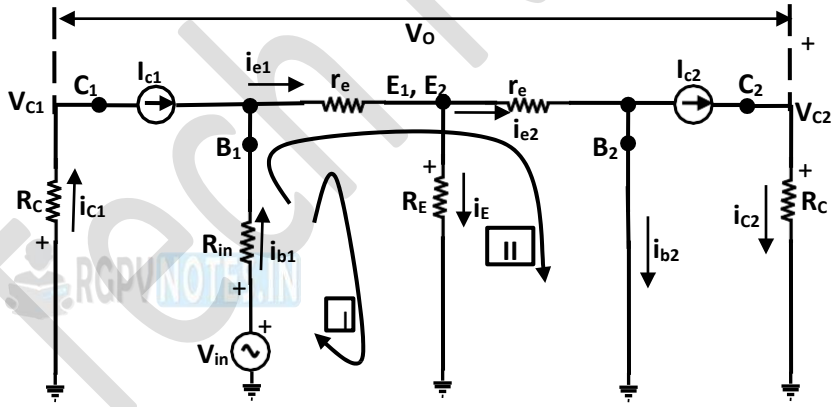


Figure 3.9: AC Equivalent Circuit of Single Input Balance Output

Voltage gain: Kirchhoff's voltage equation for loop I & II gives-

$$V_{in} - R_{in}i_{b1} - r_e i_{e1} - R_E i_E = 0 \quad ----------3.1$$

$$V_{in} - R_{in}i_{b1} - r_e i_{e1} - r_e i_{e2} = 0 \quad ----------3.2$$

Substituting current relations $i_E = (i_{e1} - i_{e2})$, $i_{b1} \cong \frac{i_{e1}}{\beta_{ac}}$, and $i_{b2} \cong \frac{i_{e2}}{\beta_{ac}}$ and neglecting $\frac{R_{in}}{\beta_{ac}}$ very small we get

$$(r_e + R_E)i_{e1} - (R_E)i_{e2} = V_{in} \quad ----------3.3$$

$$(r_e)i_{e1} + (r_e)i_{e2} = V_{in} \quad ----------3.4$$

Equation 3.3 and 3.4 solved simultaneously for i_{e1} and i_{e2} by using cramer's rule-

$$i_{e1} = \frac{\begin{vmatrix} V_{in} & -R_E \\ V_{in} & r_e \end{vmatrix}}{\begin{vmatrix} r_e + R_E & -R_E \\ r_e & r_e \end{vmatrix}} = \frac{(r_e + R_E)V_{in}}{r_e(r_e + 2R_E)} \quad ----------3.5$$

Similarly,

$$i_{e2} = \frac{\begin{vmatrix} r_e + R_E & V_{in} \\ r_e & V_{in} \end{vmatrix}}{\begin{vmatrix} r_e + R_E & -R_E \\ r_e & r_e \end{vmatrix}} = \frac{(R_E)V_{in}}{r_e(r_e + 2R_E)} \quad ----------3.6$$

The output voltage is, $V_o = V_{C2} - V_{C1} = R_C.i_{C2} - (-R_C.i_{C1}) = R_C(i_{C1} + i_{C2})$

since $i_e = i_c$ hence, $V_o = R_C(i_{e1} + i_{e2})$ ----------3.7

Substituting the i_{e1} and i_{e2} in equation 3.7, we get

$$V_o = \frac{R_C}{r_e} V_{in} \quad \text{----------3.8}$$

Therefore,

$$A_d = \frac{V_O}{V_{in}} = \frac{R_C}{e} \quad \text{----------3.}$$

Equation 3.9 is the voltage gain equation and is independent of R_E and this equation is identical to the voltage gain equation of common emitter amplifier.

b) Differential input resistance: Input resistance R_i seen from the input signal source is determined as follows-

$$R_i = \frac{V_{in}}{i_{b1}} = \frac{V_{in}}{i_{e1}/\beta_{ac}} = \frac{\beta_{ac} V_{in}}{i_{e1}}$$

Substituting the value of $\mathbf{i_{e1}}$ from equation 3.5, we get

$$R_i = 2\beta_{ace} \qquad \text{if } R_E \gg {}_e \quad \text{------3.10}$$

c) Output Resistance: Output resistance R_O is the equivalent resistance , measured at collector of either transistor Q_1 or Q_2 with respect to ground and is given by the equation $\mathbf{R_{O1} = R_{O2} = R_C}$

B) Single Input Unbalance Output Differential Amplifier: In this amplifier shown in figure 3.10, input is applied to one of the base of transistor, say Q_1 and base of Q_2 is grounded. The output is measured at either collector with respect to ground, say output is measured at collector of Q_2 with respect to ground.

AC analysis of amplifier: AC equivalent circuit of the amplifier with a small signal T-equivalent model is shown in figure 3.11 below.

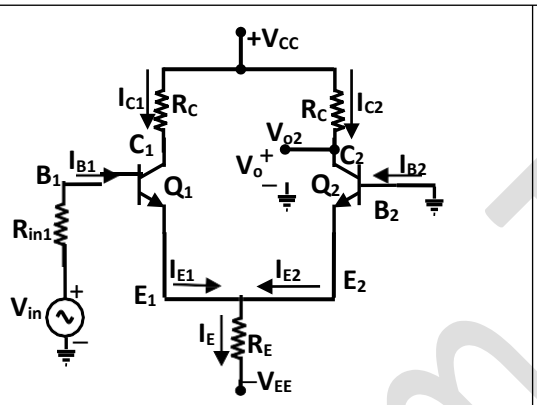


Figure 3.10: Single Input Unbalance Output

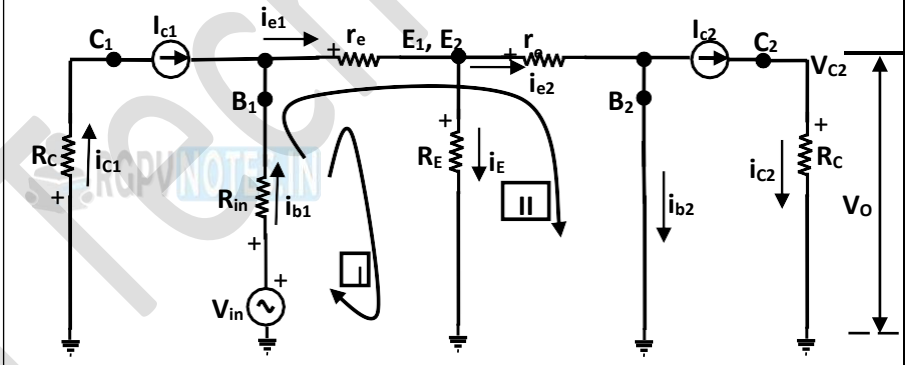


Figure 3.11: AC Equivalent Circuit of Singe Input Unbalance Output Differential Amplifier

The output voltage is, $V_o = V_{C2} = R_C.i_{C2}$

since $i_e = i_c$ hence, $V_o = R_C\, i_{e2}$ ----------3.11

Substituting the i_{e2} from equation 3.6 in equation 3.11, and if $R_E >> r_e$ we get,

$$V_o = \frac{R_C}{2r_e} V_{in} \quad \text{----------3.12}$$

Therefore,

$$A_d = \frac{V_O}{V_{in}} = \frac{R_C}{2 \quad e} \quad \text{----------3.13}$$

b) Differential input resistance: Input resistance R_i seen from the input signal source is determined as follows-

$$R_i = \frac{V_{in}}{i_{b1}} = \frac{V_{in}}{i_{e1}/\beta_{ac}} = \frac{\beta_{ac} V_{in}}{i_{e1}}$$

Substituting the value of $\mathbf{i_{e1}}$ from equation 3.5, we get

$$R_i = 2\beta_{ace} \qquad \text{if } R_E \gg {}_e \quad \text{------3.14}$$

c) Output Resistance: Output resistance R_O is the equivalent resistance , measured at collector $\mathbf{C_2}$ of transistor Q_2 with respect to ground and is given by the equation $\mathbf{R_O = R_C}$

C) Dual Input Balance Output Differential Amplifier: In this amplifier as shown in figure 3.12, input signals (V_{in1} and V_{in2}) are applied to the base of transistors Q_1 and base of Q_2. The output (V_o) is measured between two collectors, which are at the same DC potential. Therefore the output is said to be balanced output.

AC analysis of amplifier: AC equivalent circuit of the Dual Input Balance Output differential amplifier with a small signal T-equivalent model is shown in figure 3.13 below.

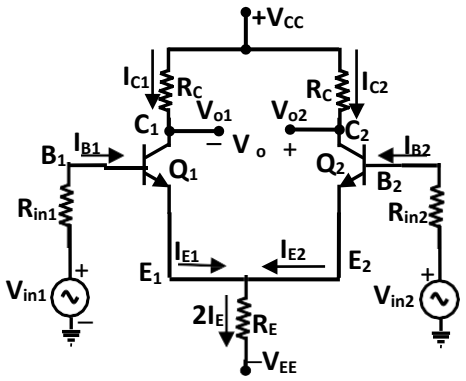


Figure 3.12: Dual Input Balance output Differential Amplifier

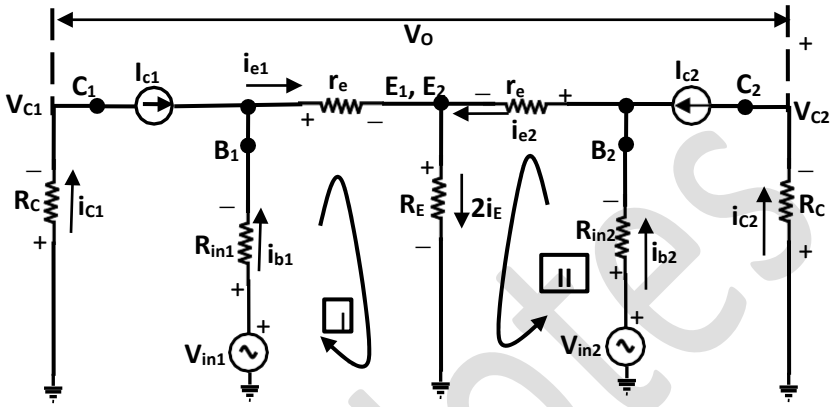


Figure 3.13: AC Equivalent Circuit of Dual Input Balance output Differential Amplifier

Voltage gain: Kirchoff's voltage equation for loop I & II gives-

$$V_{in1} - R_{in1}i_{b1} - r_e i_{e1} - R_E(i_{e1} + i_{e2}) = 0 \quad \text{----------3.15}$$

$$V_{in2} - R_{in2}i_{b2} - r_e i_{e2} - R_E(i_{e1} + i_{e2}) = 0 \quad \text{----------3.16}$$

Substituting current relations $i_{b1} \cong \frac{i_{e1}}{\beta_{ac}}$, and $i_{b2} \cong \frac{i_{e2}}{\beta_{ac}}$ and neglecting $\frac{R_{in1}}{\beta_{ac}}$ and $\frac{R_{in2}}{\beta_{ac}}$ very small we get

$$(r_e + R_E)i_{e1} + (R_E)i_{e2} = V_{in1} \quad \text{----------3.17}$$

$$(R_E)i_{e1} + (r_e + R_E)i_{e2} = V_{in2} \quad \text{----------3.18}$$

Equation 3.17 and 3.18 solved simultaneously for i_{e1} and i_{e2} by using cramer's rule-

$$i_{e1} = \frac{\begin{vmatrix} V_{in1} & R_E \\ V_{in2} & r_e + R_E \end{vmatrix}}{\begin{vmatrix} r_e + R_E & R_E \\ R_E & r_e + R_E \end{vmatrix}} = \frac{(r_e + R_E)V_{in1} - (R_E)V_{in2}}{(r_e + R_E)^2 - R_E^2} \quad \text{----------3.19}$$

Similarly,

$$i_{e2} = \frac{\begin{vmatrix} r_e + R_E & V_{in1} \\ R_E & V_{in2} \end{vmatrix}}{\begin{vmatrix} r_e + R_E & R_E \\ R_E & r_e + R_E \end{vmatrix}} = \frac{(r_e + R_E)V_{in2} - (R_E)V_{in1}}{(r_e + R_E)^2 - R_E^2} \quad \text{----------3.20}$$

The output voltage is, $V_o = V_{C2} - V_{C1} = -R_C.i_{C2} - (-R_C.i_{C1}) = R_C(i_{C1} - i_{C2})$

since $i_e = i_c$ hence, $V_o = R_C(i_{e1} - i_{e2})$ ---------- 3.21

Substituting the i_{e1} and i_{e2} in equation 3.21, we get

$$V_o = \frac{R_C}{r_e}(V_{in1} - V_{in2}) \quad \text{----------3.22}$$

Therefore,

$$A_d = \frac{V_O}{V_{id}} = \frac{R_C}{r_e} \quad \text{----------3.23}$$

Equation 3.23 is the voltage gain equation and is independent of R_E since R_E and this equation is identical to the voltage gain equation of common emitter amplifier.

b) Differential input resistance: Differential Input resistance R_{i1} and R_{i2} is defined as the equivalent resistance that would be measured at either input terminal with the other input terminal grounded. Means that R_{i1} seen from input signal source V_{in1} is determined and other source V_{in2} is set at zero. Usually source resistance R_{in1} and R_{in2} are very small and be ignored. In equation form-

$$R_{i1} = \frac{V_{in1}}{i_{b1}} = \frac{V_{in1}}{i_{e1}/\beta_{ac}} = \frac{\beta_{ac}V_{in1}}{i_{e1}}$$

Substituting the value of i_{e1} from equation 3.5, we get

$$R_{i1} = 2\beta_{ace} \text{ if } R_E \gg r_e, \text{then } (r_e + 2R_E \cong 2R_E) \text{and } (r_e + R_E) \cong R_E \quad \text{------3.24}$$

Similarly, $R_{i2} = 2\beta_{ace}$ ---------- 3.25

c) Output Resistance: Output resistance is defined as the equivalent resistance that would be measured at either output terminal with respect to ground**.** Output resistance R_O is the equivalent resistance, measured between collector C_1 and ground is equal to that of collector resistance and is given by the equation **$R_{O1} = R_{O2} = R_C$**

D) <u>Dual Input Unbalance Output Differential Amplifier:</u> In this amplifier as shown in figure 3.14, input signals (V_{in1} and V_{in2}) are applied to of the base of transistorsQ_1 and base of Q_2. The output (V_o) is measured at either of the two collectors C_1 or C_2, with respect to ground.

AC analysis of amplifier: AC equivalent circuit of the Dual Input Unbalance Output differential amplifier with a small signal T-equivalent model is shown in figure 3.15 below.

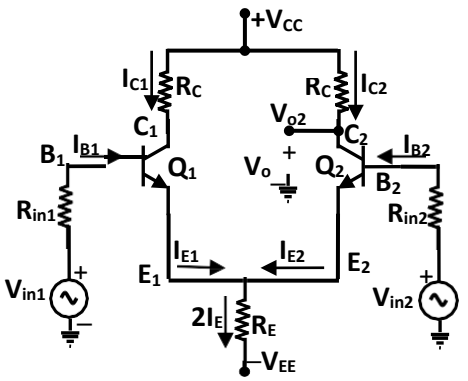


Figure 3.14: Dual Input Unbalance Output Differential Amplifier

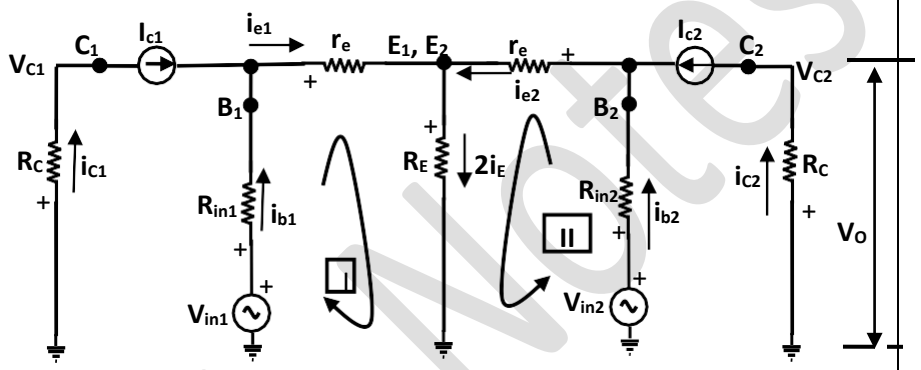


Figure 3.15: AC Equivalent Circuit Of Dual Input Unbalance Output Differential Amplifier

Voltage gain: Kirchoff's voltage equation for loop I & II gives-

$$V_{in1} - R_{in1}i_{b1} - r_e i_{e1} - R_E(i_{e1} + i_{e2}) = 0 \text{ ----------} 3.26$$

$$V_{in2} - R_{in2}i_{b2} - r_e i_{e2} - R_E(i_{e1} + i_{e2}) = 0 \text{ ----------} 3.27$$

Substituting current relations $i_{b1} \cong \frac{i_{e1}}{\beta_{ac}}$, and $i_{b2} \cong \frac{i_{e2}}{\beta_{ac}}$ and neglecting $\frac{R_{in1}}{\beta_{ac}}$ and $\frac{R_{in2}}{\beta_{ac}}$ very small we get

$$(r_e + R_E)i_{e1} + (R_E)i_{e2} = V_{in1} \text{ ----------} 3.28$$

$$(R_E)i_{e1} + (r_e + R_E)i_{e2} = V_{in2} \text{ ----------} 3.29$$

Equation 3.28 and 3.29 solved simultaneously for i_{e1} and i_{e2} by using cramer's rule-

$$i_{e1} = \frac{\begin{vmatrix} V_{in1} & R_E \\ V_{in2} & r_e + R_E \end{vmatrix}}{\begin{vmatrix} r_e + R_E & R_E \\ R_E & r_e + R_E \end{vmatrix}} = \frac{(r_e + R_E)V_{in1} - (R_E)V_{in2}}{(r_e + R_E)^2 - R_E^2} \text{ ----------} 3.30$$

Similarly,

$$i_{e2} = \frac{\begin{vmatrix} r_e + R_E & V_{in1} \\ R_E & V_{in2} \end{vmatrix}}{\begin{vmatrix} r_e + R_E & R_E \\ R_E & r_e + R_E \end{vmatrix}} = \frac{(r_e + R_E)V_{in2} - (R_E)V_{in1}}{(r_e + R_E)^2 - R_E^2} \text{ ----------} 3.31$$

The output voltage is, $V_o = V_{C2} = V_{o2} = -R_C.i_{C2}$

since $i_e \approx i_c$ hence, $V_o = -R_C\,(i_{e2})$ ---------- 3.32

Substituting the i_{e2} in equation 3.32, and generally $R_E \gg r_e$, then $(r_e + 2R_E \cong 2R_E)$and $(r_e + R_E) \cong R_E$we get

$$V_o = \frac{R_C}{2r_e}(V_{in1} - V_{in2}) \text{ ----------} 3.33$$

Therefore,

$$A_d = \frac{V_O}{V_{id}} = \frac{R_C}{2_{\ e}} \text{ ----------} 3.34$$

Thus the voltage gain is half the gain of the dual input balanced output differential amplifier.

b) Differential input resistance: Differential Input resistance R_{i1} and R_{i2} is

$$R_{i1} = R_{i1} = 2\beta_{ace} \text{ ----------} 3.35$$

c) Output Resistance: Output resistance is defined as the equivalent resistance that would be measured at either output terminal with respect to ground**.** Output resistance R_O is the equivalent resistance, measured at collector C_2 and ground is equal to that of collector resistance and is given by the equation **$R_O = R_C$**

INTRODUCTION TO OP-AMP: An op-amp is a direct coupled high-gain amplifier. It consists of one or more differential amplifiers and followed by a level translator and output stage. It can amplify DC as well as AC signals. By addition of suitable external feedback components, op-amp is designed to perform mathematical operations such as addition, subtraction, multiplication, integration, differentiation, active filters, oscillators, comparators, regulators and others. Figure 3.16 shows the schematic symbol of Op-amp.

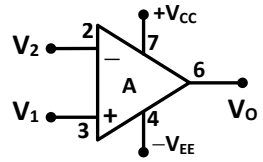


Figure 3.16: Schematic Symbol of OP-AMP

V_1 = Voltage at non-inverting input (volts)
V_2 = Voltage at inverting input (volts)
V_o = Output Voltage (volts)
All these voltages are measured with respect to ground.
A = large-signal voltage gain.

Block diagram representation of op-amp:

The block diagram of a typical op-amp is as shown in figure 3.17. It has four important stages which are as listed below.

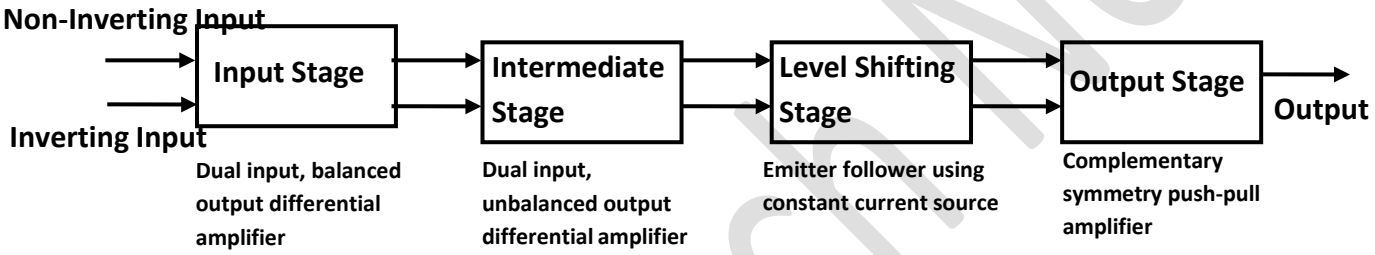


Figure 3.17: Block Diagram Representation of OP-AMP

The first stage is the input stage which is a dual input, balanced output differential amplifier. This stage generally provides most of the voltage gain of the amplifier and also establishes the input resistance of the op-amp.

The second stage is the intermediate stage which is usually another differential amplifier which is driven by the output of the first stage. In most of the op-amps the intermediate stage is a dual input, unbalanced (single ended) output.

Cascaded differential amplifier are used to provide a required voltage gain. The net gain is the product of the voltage gains of individual differential amplifier. Thus a very high voltage gains with a very low noise levels are obtained.

In op-amps the amplifier stages are directly coupled (coupling capacitors are not used) to make them handle all frequencies from 0 to several MHz, hence there is no DC isolation. This direct coupling results in a high level of DC voltage at the output of the amplifiers. Thus a level shifter or level translator is used to shift the DC level to zero volts with respect to ground. The level shifter circuit is basically an emitter follower circuit.

The final stage ie. the output stage is usually a complementary symmetry push-pull power amplifier. This stage is mainly used to increase the output voltage swing and also to increase the current supplying capability of the op-amp. A well designed output stage also provides a low output resistance.

Ideal Op-Amp characteristics:

Ideal op-amp characteristics:
1) Infinite voltage gain A_V.
2) Infinite input resistance R_i.
3) Zero output resistance Ro.
4) Zero output voltage when input voltage is zero.
5) Infinite bandwidth.
6) Infinite common-mode rejection ratio.
7) Infinite slew rate.

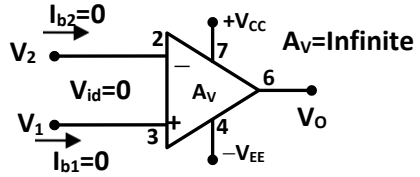


Figure3.18: Equivalent circuit of an ideal OP-AMP

Equivalent circuit of op-amp:

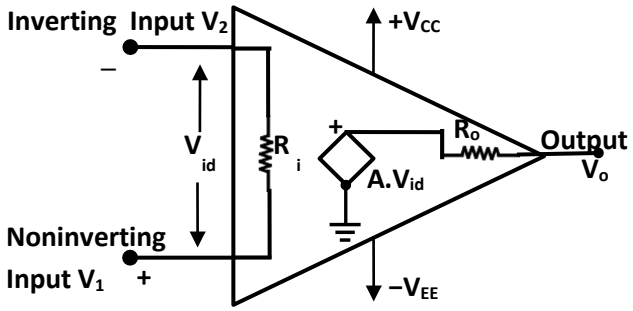


Figure3.19: Equivalent circuit of OP-AMP

Equivalent Circuit of op-amp is shown in figure 3.19. The voltage V_{id} is the differential input voltage $V_{id} = (V_1 - V_2)$. R_i is the input resistance of the device. The gain parameter A is called the open loop gain. The output voltage is $V_o = AV_{id} = A(V_1 - V_2)$ Which indicates that the output voltage Vo is a function of the difference between the input voltages V_1 and V_2. Note that the AV_{id} is an equivalent thevenin voltage source and Ro is the thevenin equivalent resistance looking back into the output terminal of an OpAmp. The equivalent circuit is useful in analyzing the basic operating principles of op-amps and in observing the effects of feedback arrangements.

Power Supply Configurations of Op-Amp:

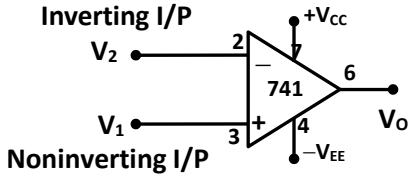


Figure3.20: OP-AMP Power Supply Connections

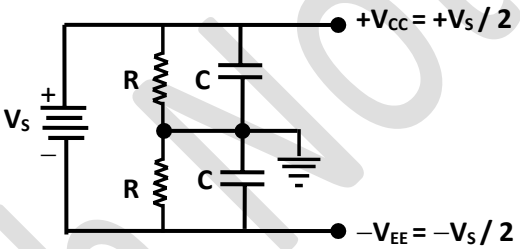


Figure3.21(a) : Arrangement for obtaining positive and negative Supply voltages for an Opamp

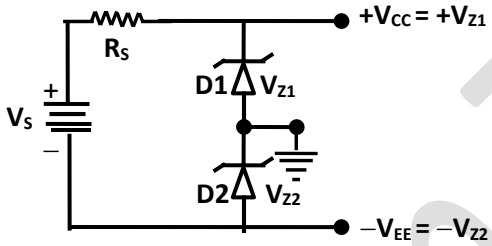


Figure3.21(b) : Arrangement for obtaining positive and negative Supply voltages for an Opamp

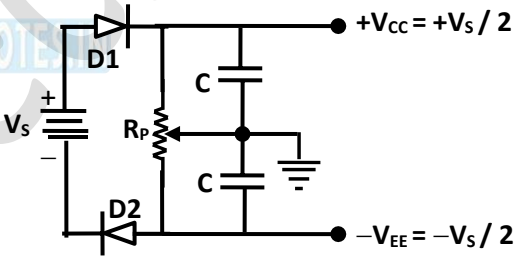


Figure3.21(C) : Arrangement for obtaining positive and negative Supply voltages for an Opamp

As opamp uses one or more differential amplifier stages and differential amplifier requires both positive and negative power supply for proper operation of the circuit. The two power supplies required for a linear IC are usually equal in magnitudes, +15V and −15V respectively. These power supply voltages must be reference to a common point or ground. Figure 3.20 shows power supply connections for the 741 opamp. Pin 7 is a positive supply and pin 4 is a negative supply pin. Instead of using two separate power supplies, we can use a single power supply to obtain +V_{CC} and −V_{EE} as shown in figure 3.21 (a), (b) and (C). In figure 3.21 (a) the value of total resistance (2R) should be ≥ 10kΩ for not to draw much current from the supply V_S. The two capacitors (range from 0.01μF to 10μF) provides for decoupling (bypass) of the power supply. In figure 3.21 (b) zener diodes are used for obtaining symmetrical power supply voltages. The value of R_S is chosen such that it supplies sufficient current for the diodes to operate in avalanche mode. In figure 3.21 (C) the potentiometer R_P is used to assure equality between +V_{CC} and −V_{EE} values. Diodes D1 and D2 are used to protect the IC, if the negative and positive terminals of V_S are accidentally reversed.

Characteristics of op-amp: Ideal and Practical, Input offset voltage, offset current, Input bias current, Output offset voltage, thermal drift, Effect of variation in power supply voltage, common-mode rejection ratio (CMRR), Slew rate and its Effect, PSRR and gain bandwidth product, frequency limitations and compensations, transient response, analysis of TL082 datasheet.

CHARACTERISTICS OF A PRACTICAL OP-AMP:

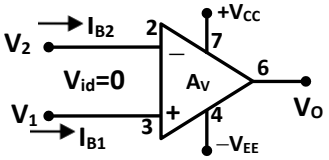


Figure 4.1: OP-AMP

a) Input Offset Voltage (V_{io}): The voltage that must be applied between two input terminals of op-amp to nullify the output ie. V_o =0V is input offset voltage. This voltage could be positive or negative. The smaller the values of V_{io}, better the input terminals are matched**.** For IC741C, V_{io} = 6mV maximum.

b) Input Offset Current (I_{io}): The difference between the separate input currents entering into the two input terminals is referred as input bias current and given by equation $I_{io} = [I_{B1} - I_{B2}]$ with $V_o = 0$. For IC741C, I_{io} = 200nA maximum.

c) Input Bias Current (I_B): The average of the separate input currents entering into the two input terminals is referred to as input bias current and is given by equation: $I_B = [(I_{B1} + I_{B2})/2]$. For IC741C, I_B = 500nA maximum.

d) Output Offset Voltage (V_{OO}): The output offset voltage is the DC voltage between the output terminal and ground of an amplifier, when the two inputs are grounded ie. $V_1 = V_2 = 0$ V. For IC741C, V_{OO} = ±15V maximum.

e) Thermal Drift : The average rate of change of input offset voltage (ΔV_{IO}) or change of input offset current (ΔI_{IO}) or change in input bias current (ΔI_B) per unit change in temperature (ΔT) is called thermal drift.

$\Delta V_{IO} / \Delta T$ = thermal voltage drift (µV/°C); $\Delta I_{IO} / \Delta T$ = thermal current drift (pA/°C)

f) Common-Mode Rejection Ratio (CMRR): It is defined as the ratio of differential voltage gain(A_{DM}) to the common mode voltage gain(A_{CM}) ie. CMRR = A_{DM}/ A_{CM}. The higher the value of CMRR, the better is the matching between two input terminals and the smaller is the output common-mode voltage. For the 741C, CMRR is 90dB typically.

g) Power Supply Rejection Ratio (PSRR): The change in an op-amps input offset voltage ΔV_{io} caused by variation in supply voltages ΔV is called power supply sensitivity (PSS). The reciprocal of the PSS is PSRR or supply voltage rejection ratio (SVRR)

PSRR = $\Delta V / \Delta V_{io}$. Expressed in V/µV or in decibels (dB). For the 741C, SVRR = 150µV/V. Lower the value of SVRR, the better for op-amp performance.

h) Slew Rate (SR): Slew rate is defined as the maximum rate of change of output voltage with respect to time. Expressed in V/µS. In equation form: **SR =** $\frac{dV_O}{d}$**.** The Opamp 741 has a slew rate of 0.5 V/µs. This means that the output cannot rise or fall at a rate of 0.5 V in 1 µs ie. distortion will occur at voltages greater than 0.5 V when operating at an unity gain with an output frequency of 1 MHz.

Slew rate indicates how rapidly the output of an op-amp can change in response to the changes in the input frequency. Also known as output voltage swing, as a function of frequency or as a voltage follower large-signal pulse response. For 741C, slew rate is 0.5V/µs. The slew rate of an op-amp is fixed, therefore if the slope requirements of the output signal are greater than the slew rate, then distortion occurs. One of the drawback of IC741C is its low slew rate (0.5V/µs), which limits its use in high frequency applications, such as oscillators, comparators and filters.

i) Gain-Bandwidth product: Gain-Bandwidth product is the bandwidth of the op-amp when the voltage gain is 1. From the open loop voltage gain versus frequency graph it can be found to be approximately 1MHz.

Causes of Slew Rate limitation : Slew rate is caused by current limiting and the saturation of internal stages of an op-amp when a large amplitude signal of high frequency is applied. Thus the slew rate is a large signal phenomenon. The resulting maximum current is available to charge the capacitance compensation network. As the capacitor requires a finite amount of time to charge and discharge, hence the internal capacitors prevent the output voltage from responding immediately to a fast changing input. Thus the slew rate limiting is caused by this capacitor charging rate, in which the voltage across the capacitor is the output voltage.

The slew rate equation is given by the expression: **SR =** $2fV_P$ V/Sec **=** $2fV_P/10^6$ V/Sec
Where, f = input signal frequency in Hz, V_P = peak value of the output sine wave in volts.
Slew rate determines the maximum frequency f_{max} of operation for a desired output swing. If the right hand side value of the slew rate equation is less than the slew rate of the op-amp, the output waveform will always be undistorted. If the value exceeded, the output waveform will be distorted.

Effect of Slew Rate in Applications: Slew rate has effect on both open and closed loop configurations. In open loop configuration, using IC741C, open loop gain is very large. Output will swing between +14V to -14V each time the input sine wave crosses zero volts as shown in figure 4.2 (a).

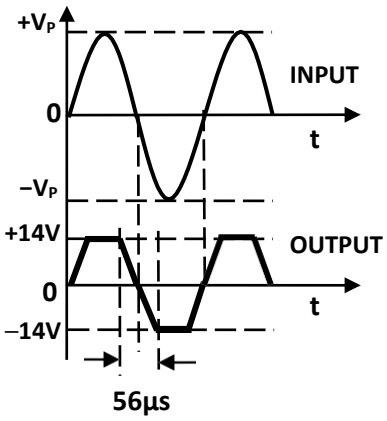


Figure 4.2 (a): Input and output Waveforms

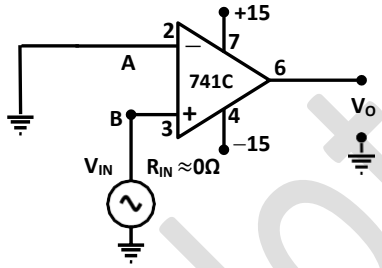


Figure 4.2 (b): Open loop configuration

The time taken by the output to go from +14V to -14V can be determined by slew rate value of 741C. Slew rate can be calculated from the slope of the output waveform. The 741C has a typical slew rate of 0.5V/µs. Therefore we have (28V / 0.5V/µs) = 56µs. This means that 56µs is the minimum time between the two zero crossings. Hence the maximum input frequency **f_{max}** at which the output will be distorted is given by
f_{max} = (1/(2x 56µs) = 8.93kHz.
Therefore at **f_{max},** the output will be triangular wave instead of a square wave. Thus, to get a square wave output, input frequency should keep below **f_{max}** or choose an opamp with a faster slew rate.
Figure 4.2 (c), shows closed loop configuration where the opamp used as an inverting amplifier with a gain of 10.

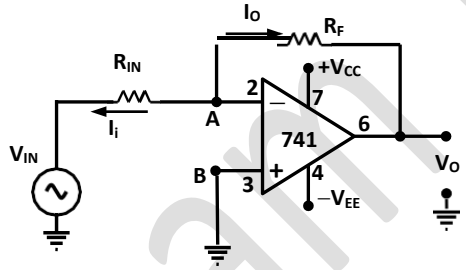


Figure 4.2 (C): Close loop configuration

R_F = 10 kΩ, R_{IN} = 1 kΩ;
So, Gain of Inverting amplifier is equal to:
(R_F / R_{IN}) = (10 k / 1 k) = 10.
The amplifier will operate with a gain of 10 up to about 91 kHz.
BW with feedback, f_F = [Unity Gain Bandwidth x K] / A_F
where, UGB = 1 MHz, K = R_F / (R_{IN} + R_F) and
A_F, Amplifier gain = 10.

On substituting we get, BW with feedback, $f_F \approx$ 91kHz.
Since, **SR =** $2fV_P$ V/Sec **=** $2fV_P/10^6$ V/Sec
Substituting the value of f_F and 0.5 V/µS (SR of opamp 741C) in the above equation
We get, **V_P = 0.874 V_{peak} (Undistorted) Or V_O = 2 x 0.874 V_{peak} = 1.75 $V_{peak\text{-}peak}$ (Sinewave).**
Hence, for the output to be a sinewave, the maximum input signal V_{INMAX} should be less than- 1.75/10 = 175m$V_{p\text{-}p}$

Effect of variation in power supply voltages on offset voltage: Due to poor regulation and filtering, the supply voltages (+V_{CC} and –V_{EE}) changes. This change results in a change in the input offset voltage, which in turn causes change in output offset voltage. This change in input offset voltage is specified in datasheet by variety of terms as input offset voltage sensitivity, power supply voltage rejection ratio, power supply sensitivity and supply voltage rejection ratio. Terms are expressed in µV/V or in decibels (dB). Example: For the 741C, SVRR = 150µV/V maximum and typically 20 log ($\Delta V/\Delta V_{io}$) = 76.48dB
20 log(1/SVRR) = 20 log (1/($\Delta V_{io}/\Delta V$) = 20 log (1/150µV/V) = 20 log (10^6 / 150) = 76.48dB.
Lower the value of SVRR, the better the op-amp performance.
Relationship between the change in output offset voltage and SVRR is express as-

$$\Delta V_{OO} = [1+ (R_F/R_{IN})] (\Delta V/\Delta V_{io}) \Delta V$$

Where, ΔV_{OO} = change in output offset voltage (volts); ΔV = change in supply voltages ($+V_{CC}$ and $-V_{EE}$);
($\Delta V/\Delta V_{io}$) = Supply voltage rejection ratio (V/µV)

FREQUENCY LIMITATIONS AND COMPENSATIONS:

Frequency Response plot: Manner in which the gain of the op-amp responds to the different frequencies is frequency response. A graph of magnitude of gain versus frequency is called frequency response plot.

Limitation: Some of the characteristics of op-amp such as voltage gain, input resistance, output resistance, output voltage swing, input noise voltage and noise current and CMRR are frequency dependent parameters. Most important voltage gain A decreases as the operating frequency increases. This variation in gain as a function of frequency imposes a limitation on performance of op-amp and also when op-amp used in AC applications.

Compensating networks:

Change in gain and phase shift between input and output as a function of frequency is credited to the internally integrated capacitors as well as stray capacitances. These capacitances are due to the physical characteristics of semiconductor devices (BJTs or FETs) and internal construction of the op-amp.

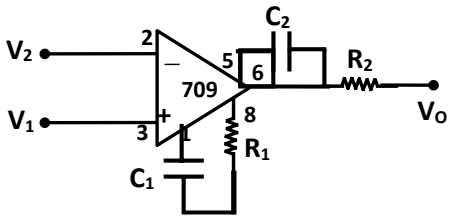


Figure 4.3(c): Frequency compensation circuit of op-amp 709

To modify the rate of change of gain as well as phase shift by using a specific component network (components are resistors and capacitors) with op-amp is called a compensating network. The phase lead (contributes a positive phase angle) and phase lag (contributes a negative phase angle) are the most compensating networks in op-amp. Two types of compensating networks : internal compensating network and external compensating network.

IC741C is an internally compensated op-amp and op-amp 709 is a noncompensated op-amp (ie. External discrete components are added at the designated terminals of op-amp. The open-loop frequency response curves and the connection diagram of IC709 for the external compensating components is shown in figure 4.3(a,b and c).

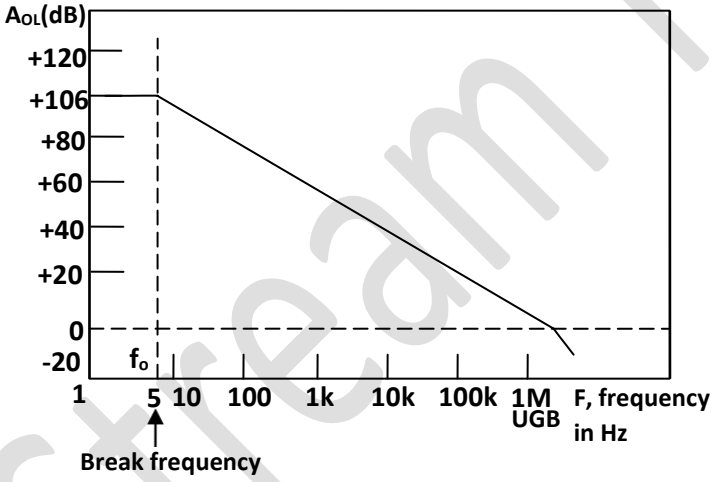


Figure 4.3(a): Frequency Response of internally compensated op-amp 741

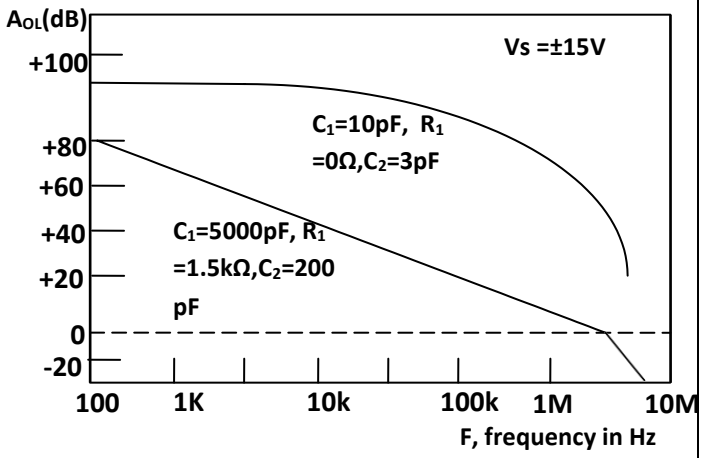
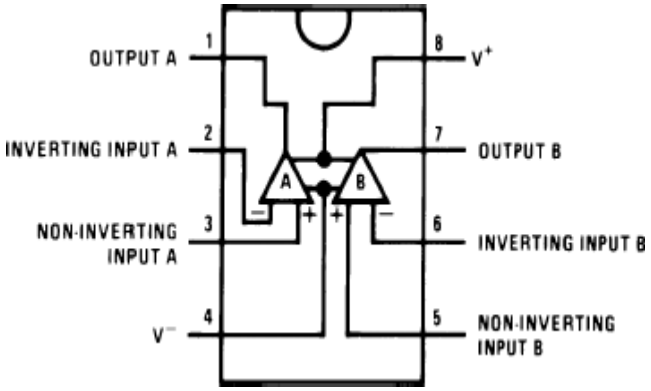


Figure 4.3(b): Frequency Response of external compensated op-amp 709 for various values of C_1, R_1 and C_2

Transient Response: The response of any practically useful network to a given input is composed of two parts: the transient and steady state response. The transient response is that portion of the complete response before the output attains some fixed value (steady state value). Transient response is time variant. Rise time and the percent of overshoot are the characteristics of transient response. The time required by the output to go from 10 % to 90% of its final value is called rise time. Overshoot is the maximum amount by which the output deviates from the steady state value. The transient response test circuit for the 741C for V_{in} = 20mV, rise time is 0.3µs and overshoot is 5%. Transient response is one of the important considerations in selecting op-amp in ac applications. Rise time is inversely proportional to the unity gain bandwidth of op-amp. This means that the smaller the value of rise time the higher is the bandwidth.

Thermal Drift: The average rate of change of some of the characteristics of op-amp such as input offset voltage (V_{io}), input offset current (I_{io}) and input bias current (I_b) due to the change in temperature is thermal drift.
$\Delta I_{io}/\Delta T$ = thermal drift in the input offset current (pA/°C) [Thermal Current Drift]
$\Delta I_b/\Delta T$ = thermal drift in the input bias current (pA/°C) [Thermal Current Drift]
$\Delta V_{io}/\Delta T$ = thermal drift in the input offset voltage (µV/°C) [Thermal Voltage Drift]

ANALYSIS OF TL082 DATASHEET:



IC TL082 is a wide bandwidth dual JFET input operational amplifier manufactured by Texas instruments. It is low cost, high speed with an internally compensated input offset voltage. It maintains a large gain-bandwidth product and fast slew rate. JFET input devices provide very high input impedance and very low input bias and input offset currents. It has very low noise level and offset voltage drift hence not sensitive to temperature variations.

Features of TL082C:

: Low Power Consumption.
: Wide Common-Mode and Differential Voltage ranges.
: Low Input Bias Current: 30 pA Typical.
: High Input Impedance: JFET Input Stage.
: Low Input Offset Current: 5 pA Typical.
: Output Short-Circuit Protection.
: Low Total Harmonic Distortion: 0.003% Typical.
: High Slew Rate: 13 V/µs Typical.
: Common-Mode Input Voltage Range Includes V_{CC+}

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TEXAS INSTRUMENTS

TL081, TL081A, TL081B, TL082, TL082A
TL082B, TL084, TL084A, TL084B

SLOS081I – FEBRUARY 1977 – REVISED MAY 2015

TL08xx JFET-Input Operational Amplifiers

1 Features

- Low Power Consumption: 1.4 mA/ch Typical
- Wide Common-Mode and Differential Voltage Ranges
- Low Input Bias Current: 30 pA Typical
- Low Input Offset Current: 5 pA Typical
- Output Short-Circuit Protection
- Low Total Harmonic Distortion: 0.003% Typical
- High Input Impedance: JFET Input Stage
- Latch-Up-Free Operation
- High Slew Rate: 13 V/µs Typical
- Common-Mode Input Voltage Range Includes V_{CC+}

2 Applications

- Tablets
- White goods
- Personal electronics
- Computers

3 Description

The TL08xx JFET-input operational amplifier family is designed to offer a wider selection than any previously developed operational amplifier family. Each of these JFET-input operational amplifiers incorporates well-matched, high-voltage JFET and bipolar transistors in a monolithic integrated circuit. The devices feature high slew rates, low input bias and offset currents, and low offset-voltage temperature coefficient.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TL084xD	SOIC (14)	8.65 mm × 3.91 mm
TL08xxFK	LCCC (20)	8.89 mm × 8.89 mm
TL084xJ	CDIP (14)	19.56 mm × 6.92 mm
TL084xN	PDIP (14)	19.3 mm × 6.35 mm
TL084xNS	SO (14)	10.3 mm × 5.3 mm
TL084xPW	TSSOP (14)	5.0 mm × 4.4 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Schematic Symbol

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

				MIN	MAX	UNIT
V_{CC+}	Supply voltage(2)				18	V
V_{CC-}					–18	
V_{ID}	Differential input voltage(3)				±30	V
V_I	Input voltage(2)(4)				±15	V
	Duration of output short circuit(5)			Unlimited		
	Continuous total power dissipation			See *Dissipation Rating Table*		
T_A	Operating free-air temperature		TL08_C TL08_AC TL08_BC	0	70	°C
			TL08_I	–40	85	
			TL084Q	–40	125	
			TL08_M	–55	125	
	Operating virtual junction temperature				150	°C
T_C	Case temperature for 60 seconds	FK package	TL08_M		260	°C
	Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	J or JG package	TL08_M		300	°C
T_{stg}	Storage temperature			–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values, except differential voltages, are with respect to the midpoint between V_{CC+} and V_{CC-}.
(3) Differential voltages are at IN+, with respect to IN−.
(4) The magnitude of the input voltage must never exceed the magnitude of the supply voltage or 15 V, whichever is less.
(5) The output may be shorted to ground or to either supply. Temperature and/or supply voltages must be limited to ensure that the dissipation rating is not exceeded.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{CC+}	Supply voltage		5	15	V
V_{CC-}	Supply voltage		–5	–15	V
V_{CM}	Common-mode voltage		V_{CC-} + 4	V_{CC+} – 4	V
T_A	Ambient temperature	TL08xM	–55	125	°C
		TL08xQ	–40	125	
		TL08xI	–40	85	
		TL08xC	0	70	

6.5 Electrical Characteristics for TL08xC, TL08xxC, and TL08xI

$V_{CC\pm}$ = ±15 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A[1]	TL081C, TL082C, TL084C			TL081AC, TL082AC, TL084AC			TL081BC, TL082BC, TL084BC			TL081I, TL082I, TL084I			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_O = 0, R_S = 50 Ω	25°C		3	15		3	6		2	3		3	6	mV
			Full range			20			7.5			5			9	
α_{VIO}	Temperature coefficient of input offset voltage	V_O = 0, R_S = 50 Ω	Full range		18			18			18			18		µV/°C
I_{IO}	Input offset current[2]	V_O = 0	25°C		5	200		5	100		5	100		5	100	pA
			Full range			2			2			2			10	nA
I_{IB}	Input bias current[2]	V_O = 0	25°C		30	400		30	200		30	200		30	200	pA
			Full range			10			7			7			20	nA
V_{ICR}	Common-mode input voltage range		25°C	±11	−12 to 15		±11	−12 to 15		±11	−12 to 15		±11	−12 to 15		V
V_{OM}	Maximum peak output voltage swing	R_L = 10 kΩ	25°C	±12	±13.5		±12	±13.5		±12	±13.5		±12	±13.5		V
		R_L ≥ 10 kΩ	Full range	±12			±12			±12			±12			
		R_L ≥ 2 kΩ		±10	±12		±10	±12		±10	±12		±10	±12		
A_{VD}	Large-signal differential voltage amplification	V_O = ±10 V, R_L ≥ 2 kΩ	25°C	25	200		50	200		50	200		50	200		V/mV
			Full range	15			15			25			25			
B_1	Unity-gain bandwidth		25°C		3			3			3			3		MHz
r_i	Input resistance		25°C		10^{12}			10^{12}			10^{12}			10^{12}		Ω
CMRR	Common-mode rejection ratio	V_{IC} = V_{ICR}min, V_O = 0, R_S = 50 Ω	25°C	70	86		75	86		75	86		75	86		dB
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC}/\Delta V_{IO}$)	V_{CC} = ±15 V to ±9 V, V_O = 0, R_S = 50 Ω	25°C	70	86		80	86		80	86		80	86		dB

(1) All characteristics are measured under open-loop conditions with zero common-mode voltage, unless otherwise specified. Full range for T_A is 0°C to 70°C for TL08_C, TL08_AC, TL08_BC and –40°C to 85°C for TL08_I.

6.7 Operating Characteristics

$V_{CC\pm}$ = ±15 V, T_A= 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	V_I = 10 V, R_L = 2 kΩ, C_L = 100 pF, See Figure 19	8[1]	13		V/µs
		V_I = 10 V, R_L = 2 kΩ, C_L = 100 pF, T_A = − 55°C to 125°C, See Figure 19	5[1]			

Operating Characteristics (continued)

$V_{CC\pm}$ = ±15 V, T_A= 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_r	Rise-time	V_I = 20 V, R_L = 2 kΩ, C_L = 100 pF, See Figure 19			0.05		µs
	overshoot factor				20%		
V_n	Equivalent input noise voltage	R_S = 20 Ω	f = 1 kHz		18		nV/√Hz
			f = 10 Hz to 10 kHz		4		µV
I_n	Equivalent input noise current	R_S = 20 Ω,	f = 1 kHz		0.01		pA/√Hz
THD	Total harmonic distortion	$V_I$rms = 6 V, A_{VD} = 1, R_S ≤ 1 kΩ, R_L ≥ 2 kΩ, f = 1 kHz,			0.003%		

6.8 Dissipation Rating Table

PACKAGE	T_A ≤ 25°C POWER RATING	DERATING FACTOR	DERATE ABOVE T_A	T_A = 70°C POWER RATING	T_A = 85°C POWER RATING	T_A = 125°C POWER RATING
D (14 pin)	680 mW	7.6 mW/°C	60°C	604 m/W	490 mW	186 mW
FK	680 mW	11.0 mW/°C	88°C	680 m/W	680 mW	273 mW
J	680 mW	11.0 mW/°C	88°C	680 m/W	680 mW	273 mW
JG	680 mW	8.4 mW/°C	69°C	672 m/W	546 mW	210 mW

IC-741C

1) BJT input operational amplifier.
2) Not compensated internally the input offset voltage.
3) CMRR- 90 dB Typical.
4) Differential input voltage, V_{ID} : ±15V (max.)
5) Input resistance: 2 MΩ (BJT Input Stage).
6) Input Offset Current: 1 mA Typical.
7) Output Short-Circuit Protection.
8) Rise Time overshoot factor: 0.3µS Typical.
9) Slew Rate at unity: 0.5 V/µs Typical. (V_I = 10 V, C_L = 100 pF, R_L = 2 kΩ)
10) Unity gain bandwidth- 1MHz

IC-TL082

1) JFET input operational amplifier.
2) Internally compensated input offset voltage.
3) CMRR- 86 dB Typical.
4) Differential input voltage, V_{ID} : ±30V (max.)
5) Input resistance: 10^{12} Ω (JFET Input Stage).
6) Offset Current: 5 pA Typical.
7) Output Short-Circuit Protection.
8) Rise Time overshoot factor: 0.05µS Typical
9) Slew Rate at unity: 13 V/µs Typical. (V_I = 10 V, C_L = 100 pF, R_L = 2 kΩ)
10) Unity gain bandwidth- 3MHz

OP-AMP applications: **Inverting and non-inverting amplifier configurations, Summing amplifier, Integrators and differentiators, Instrumentation amplifier, Differential input and differential output amplifier, Voltage-series feedback amplifier, Voltage-shunt feedback amplifier, Log/ Antilog amplifier, Triangular/rectangular wave generator, phase-shift oscillators, Wein bridge oscillator, analog multiplier-MPY634, VCO, Comparator, Zero Crossing Detector.**

OP-AMP AS INVERTING-AMPLIFIER:

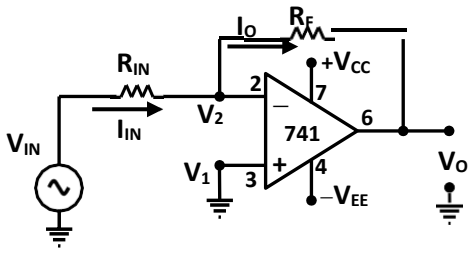


Figure 5.1: Inverting Amplifier with feedback

Circuit diagram of Inverting amplifier with feedback is shown in Figure 5.1. Input voltage V_{IN} in series with input resistance R_{IN} is connected to input inverting terminal (pin2) of op-amp. Non-inverting terminal (pin3) is grounded. Feedback resistor R_F is connected in between inverting terminal and output terminal (pin6) V_O of op-amp.

Due to high input impedance, the op-amp input current is zero, means that point V_1 and V_2 are at the same potential. Point V_1 is at ground potential means that point V_2 is also at ground potential. Thus point V_2 is said to be at virtual ground.

From the circuit; $I_{IN} \approx I_O$ ---------- 5.1

That is,

$$\frac{V_{IN} - V_2}{R_{IN}} = \frac{V_2 - V_O}{R_F} \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots \quad 5.2$$

Due to virtual ground concept, $V_1 = V_2 = 0V$

Therefore, equation 5.2 becomes,

$$\frac{V_{IN}}{R_{IN}} = \frac{-V_O}{R_F} \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots \quad 5.3$$

Ie.

$$\frac{V_O}{V_{IN}} = \frac{-R_F}{R_{IN}} \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots 5.4$$

Hence from equation 5.4, $\mathbf{V_O / V_{IN}}$ is the **Voltage gain $\mathbf{A_V}$**, by definition.

Therefore

$$A_V = \frac{V_O}{V_{IN}} = \frac{-R_F}{R_{IN}}$$

The output voltage V_O for inverting amplifier is given by:

$$V_O = \left(\frac{-R_F}{R_{IN}}\right) V_{IN}$$

The negative sign indicates that the input and output signals are out of phase by 180°. Gain of the amplifier is set by selecting the ratio of feedback resistance R_F to the input resistance R_{IN}.

OP-AMP AS NON-INVERTING AMPLIFIER:

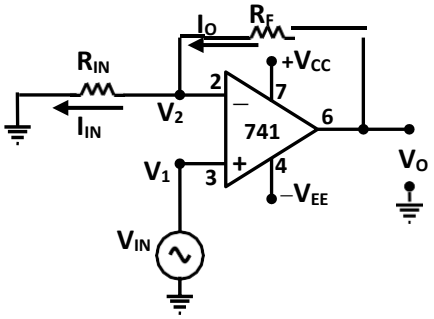


Figure 5.2: Non-Inverting Amplifier with feedback

Circuit diagram of non- Inverting amplifier with feedback is shown in Figure 5.2. Input voltage V_{IN} is applied to non-inverting terminal of op-amp. Input resistance R_{IN} is connected to inverting terminal of op-amp and it is grounded. Feedback resistor R_F is connected in between inverting terminal and output terminal V_O of op-amp.

Due to high input impedance, the op-amp input current is zero, means that point V_1 and V_2 are at the same potential. Point V_1 is at ground potential means that point V_2 is also at ground potential. Thus point V_2 is said to be at virtual ground ie. $V_1 = V_2 = V_{IN}$

From the circuit, the entire current passes through R_{IN} as the input current of op-amp is zero.

From the circuit; **$I_{IN} \approx I_O$** ---------- 5.5

That is, $\frac{V_2-0}{R_{IN}} = \frac{V_0-V_2}{R_F}$ 5.6

Due to virtual ground concept, $V_1 = V_2 = V_{IN}$

Therefore, equation 5.6 becomes,

$$\frac{V_{IN}}{R_{IN}} = \frac{V_O - V_{IN}}{R_F} \quad \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots 5.7$$

Ie.

$$\frac{V_O}{V_{IN}} = 1 + \frac{R_F}{R_{IN}} \quad \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots 5.8$$

V_O / V_{IN} is the **Voltage gain A_V**, by definition.

Hence from equation 5.8,

$$A_V = \frac{V_O}{V_{IN}} = 1 + \frac{R_F}{R_{IN}}$$

The output voltage V_O for non- inverting amplifier is given by:

$$V_O = (1 + \frac{R_F}{R_{IN}})\, V_{IN}$$

The positive sign indicates that the input and output signals are in phase.

OP-AMP AS SUMMING AMPLIFIER (ADDER CIRCUIT):

Inverting Summing Amplifier :

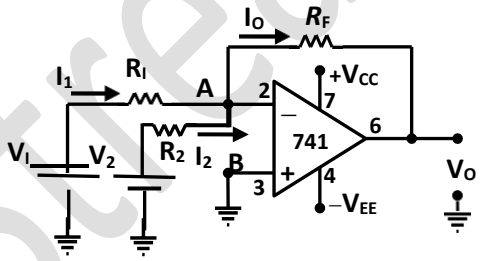


Figure 5.3: Op-amp as an Adder (Inverting)

Figure 5.3 shows the op-amp as an adder (Inverting Summing Amplifier). It is used to add voltages V_1 and V_2 which are connected to inverting terminal through resistor R_1 and R_2. Current I_1 and I_2 are the input currents and I_0 is the output current. Non-inverting terminal is grounded.

Total input current **, $I_i = I_1 + I_2$** **5.9**

Output current**, $I_O = V_O / R_F$** **5.10**

For op-amp in inverting mode**, $I_i = -I_O$** **5.11**

Therefore, equation 5.11 becomes

$$\frac{V_1}{R_1} + \frac{V_2}{R_2} = \frac{-V_O}{R_F}$$

If $R_1 = R_2 = R$ then; $\frac{V_1+V_2}{R} = \frac{-V_O}{R_F}$

Therefore, output voltage of an adder is : $V_0 = (\frac{-R_F}{R})\, V_1 + V_2$ 5. 12

If **$(R_F/R) = 1$** then, the output voltage, **$V_O = -(V_1 + V_2)$.**

The output voltage is equal to sum of the input voltages with a negative sign.

Non-inverting Summing Amplifier :

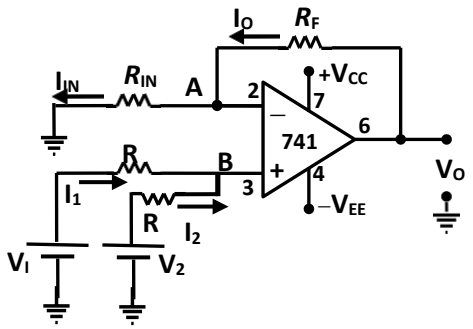


Figure 5.4: Op-amp as an Adder (Non-Inverting)

Figure 5.4 shows the op-amp as an non-inverting adder (non-Inverting Summing Amplifier). It is used to add voltages V_1 and V_2 which are connected to non-inverting terminal through resistors R and also by selecting of appropriate values of resistors R_{IN} and R_F. Current I_1 and I_2 are the input currents and I_0 is the output current.

Recall that the input impedance of non-inverting amplifier is very large. Therefore by using superposition theorem, the voltage at point B at the non-inverting terminal is

Voltage at point B = $\frac{R}{R+R} V_1 + \frac{R}{R+R} V_2$ 5. 13

Voltage at point B = $\frac{1}{2} V_1 + \frac{1}{2} V_2 = \frac{V_1+V_2}{2}$ 5. 14

Therefore, output voltage of an adder is : $V_0 = (1 + \frac{R_F}{R})(\frac{V_1+V_2}{2})$ 5. 15

If **[1+ (R_F / R)] = 2** then, the output voltage, **$V_O = (V_1 + V_2)$.**

Hence, the output voltage is equal to sum of the input voltages, the circuit is called as non-inverting summing amplifier.

OPAMP AS AN INTEGRATOR:

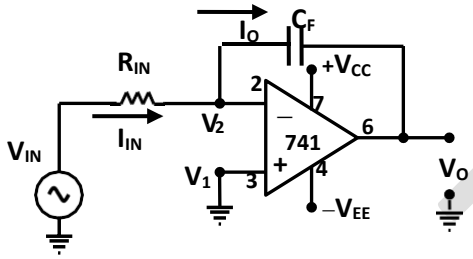


Figure 5.5: Basic Integrator

Circuit diagram of basic integrator is shown in Figure 5.5. A circuit in which output is the integral of input is the integrator or the integration amplifier. Integrator circuit is obtained by using a basic inverting amplifier configuration if the feedback resistor is replaced by a capacitor C_F. V_{IN} is the input voltage applied to the inverting terminal and non inverting terminal is grounded. I_O is the output current and V_O is the output voltage.

When the V_{IN} is applied, a current I_{IN} flows through R_{IN} and is given by equation: **$I_{IN} = V_{IN} / R_{IN}$** ---------- **5.16**

For the op-amp in inverting mode**: $I_{IN} = - I_O$** ---------- **5.17**

Output voltage V_O is the voltage across the capacitor C_F and is given by the relation:

$$V_O = V_C = \frac{1}{F} \int_O dt \quad \text{.....5.18}$$

Since, **$I_{IN} = - I_O$;** we have**:**

$$V_O = V_C = \frac{1}{F} \int -_{IN} dt \quad \text{.....5.19}$$

From the equation 5.16 we have:

$$V_O = \frac{1}{F} \int -\frac{V_{IN}}{R_{IN}} dt \quad \text{..... 5.20}$$

Therefore, $V_O = \frac{1}{-R_{IN}C_F} \int V_{IN}\ d$ 5. 21

Here, R_{IN} and C_F are constant. Hence, $V_O \propto \int V_{IN}\ d$

In Integrator, if input is sine wave then cosine wave output or if input is square wave then triangular wave output.

FREQUENCY RESPONSE OF INTEGRATOR: Frequency response of basic integrator is shown in figure 5.6, here f_b is the frequency at which the gain is 0dB and is given by, $f_b = (\frac{1}{2R\ C_{IN}\ F})$

Bothe the stability and the low-frequency roll-off problems can be corrected by the addition of the resistor R_F as shown in the practical integrator circuit of figure 5.7.

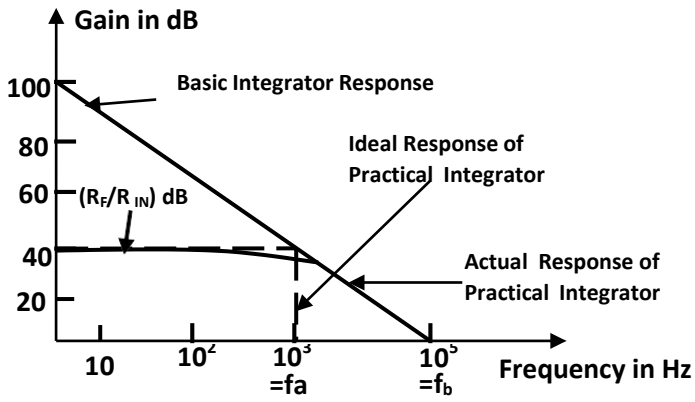


Figure 5.6: Frequency response of Practical Integrator

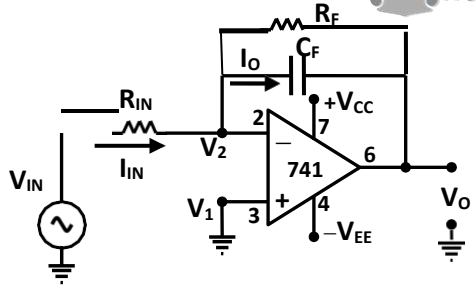


Figure 5.7: Practical Integrator

The frequency response of an ideal practical integrator is shown by broken lines in figure 5.6. In this case , f is some relative operating frequency, and for frequencies f to f_a the gain $\mathbf{R_F / R_{IN}}$ is constant. After f_a the gain decreases at a rate of 20 dB/decade. This means that between f_a and f_b, the practical integrator behaves as an integrator. The gain limiting frequency fa is given by $f_a = \left(\frac{1}{2R\ C_F}\right)_F$

Usually the value of f_a and in turn ($R_{IN}.C_F$) and ($R_F.C_F$) values should be selected such that $f_a < f_b$. The input signal will be integrated properly, if the time period T of the signal $T \geq (R_F.C_F)$ where $R_F.C_F = 1/ 2\pi.f_a$

Integrator is most commonly used in analog computers and analog to digital converters and signal-wave shaping circuits.

OP-AMP AS DIFFERENTIATOR:

Figure 5.8 shows the basic differentiator or differentiation amplifier. The circuit which performs the mathematical operation of differentiation ie. the output waveform is the derivative of the input is the differentiator. Circuit may be constructed from a basic inverting amplifier if an input resistor R_{IN} is replaced by capacitor C_{IN}.

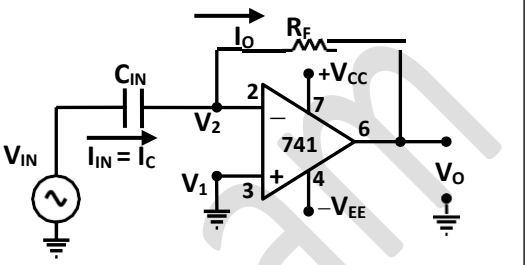


Figure 5.8: Basic Differentiator

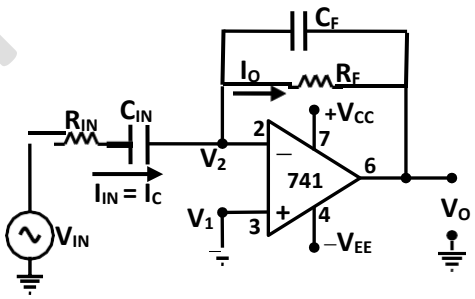


Figure 5.9: Practical Differentiator

When V_{IN} is applied, a current I_C flows through C_{IN} and is given by equation: $\mathbf{I_{IN} = I_C = C_{IN}\ d/dt\ (V_{IN})}$-------- **5.22**

For the op-amp in inverting mode: $\mathbf{I_{IN} = - I_O}$ ----------**5.23** and output current, $\mathbf{I_O = V_O/R_F}$ ----------**5.24**

Using equations 5.23 and 5.24 in equation 5.22, we have:

$$\frac{-V_O}{R_F} = {}_{IN}\cdot\frac{d}{dt}\cdot(V_{IN}) \qquad \textbf{ie.} \quad V_O = -(C_{IN}.R_F)\frac{d}{d}(V_{IN})$$

Since R_F and C_{IN} are constant, therefore $V_O \propto \frac{d}{d}(V_{IN})$

This relationship indicates that the output voltage V_O of an op-amp differentiator circuit is proportional to the derivative of the input voltage. If the constant of proportionality is made equal to 1, then V_O will be equal to the derivative of the input voltage V_{IN}. In differentiator, if input is cosine wave then sine wave is the output or a triangular wave input will produce a square wave output.

The differentiator is most commonly used in wave shaping circuit to detect the high-frequency components in an input signal and also as a rate-of-change detector in FM modulators.

FREQUENCY RESPONSE OF DIFFERENTIATOR:

However the differentiator in figure 5.8 will not perform the differentiation because of certain instability in the circuit. Here the gain of the circuit (R_F / X_{CIN}) increases with increase in frequency at a rate of 20dB/decade. Also,

input impedance X_{CIN} decreases with increase in frequency, which makes the circuit susceptible to high frequency noise. When amplified, this noise completely override the differentiated output signal.

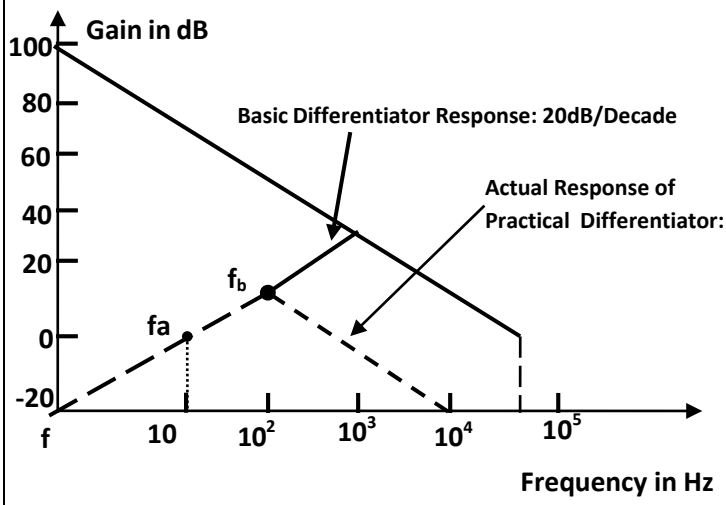


Figure 5.10: Frequency response of Practical Differentiator

Frequency response of basic and practical differentiator is shown in figure 5.10. Here, fa is the frequency at which the gain is 0dB and is given by:

$$f_a = \left(\frac{1}{2R\ C_{F\ IN}}\right)$$

Also, fc is the unity gain-bandwidth of the op-amp. Both the stability and high frequency noise problems can be corrected by the addition of two components: R_{IN} and C_F as shown in figure 5.9 and the frequency response is shown by dashed lines in figure 5.10. From frequency f to f_b, the gain increases at 20dB/decade, after f_b, gain decreases by the same rate. This 40db/decade change in gain is caused by the ($R_{IN}.C_{IN}$) and ($R_F.C_F$) combinations.

This gain limiting frequency f_b is given by: $f_b = \left(\frac{1}{2R_{IN}C_{IN}}\right)$ **where** ($R_{IN}.C_{IN}$) = ($R_F.C_F$). Thus ($R_{IN}.C_{IN}$) and ($R_F.C_F$) help to reduce the effect of high-frequency input, amplifier noise and offsets. It makes circuit more stable by preventing the increase in gain with frequency. Generally the value of fb and in turn ($R_{IN}.C_{IN}$) and ($R_F.C_F$) should be selected such that $f_a < f_b < f_c$

Where $f_a = \left(\frac{1}{2R\ C_{F\ IN}}\right)$; $f_b = \left(\frac{1}{2R\ C_{IN\ IN}}\right) = \left(\frac{1}{2R\ C_{F\ F}}\right)$; fc = unity gin-bandwidth

The input signal will be differentiated properly if the time period, $T \geq (R_F.\ C_{IN})$

OP-AMP AS AN INSTRUMENTATION AMPLIFIER:

Instrumentation amplifier is intended for precise, low level signal amplification where low noise, low thermal and time drifts, high input resistance and accurate closed loop gain are required.

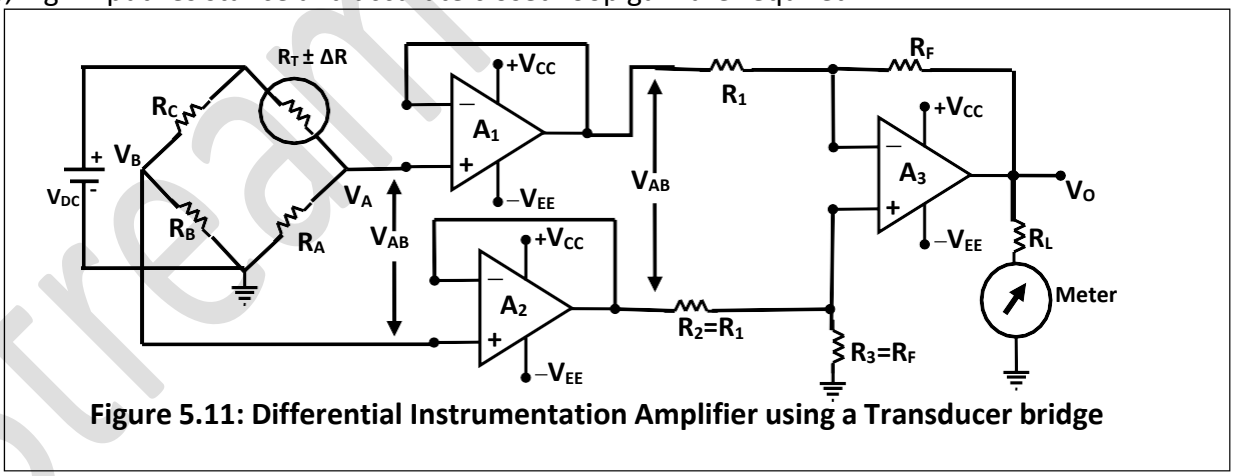


Figure 5.11: Differential Instrumentation Amplifier using a Transducer bridge

Besides, low power consumption, high CMRR and high slew rate are desirable for performance. Figure 5.11 shows the differential instrumentation amplifier using transducer bridge. A resistive transducer is connected in one arm of the bridge ($R_T \pm \Delta R$) whose resistance changes as a function of some physical energy, where R_T is the transducer resistance and ΔR is the change in resistance. The bridge is DC excited but can also be AC excited. For the bridge to be balanced the condition is that: $V_A = V_B$ ie. $\frac{R_B.V_{DC}}{R_C+R_B} = \frac{R_A.V_{DC}}{R_T+R_A}$ on solving the equation we have: $\frac{R_C}{R_B} = \frac{R_T}{R_A}$

Generally $R_A = R_B = R_C = R_T$ when the bridge is balanced. When the physical quantity to be measured changes, the transducer resistance also changes and the bridge is unbalanced ie. $V_A \neq V_B$. The output voltage of the bridge can be expressed as a function of the change in transducer resistance.

Therefore by voltage divider rule, we have: $V_A = \frac{R_A.V_{DC}}{R_A+(R_T+\Delta R)}$ and $V_B = \frac{R_B.V_{DC}}{R_B+R_C}$

Therefore the voltage V_{AB} across the output terminal of the bridge is, $V_{AB} = V_A - V_B$

If $R_A = R_B = R_C = R_T$ then we have the expression for the output voltage as: $V_{AB} = \frac{-\Delta R.(V_{DC})}{2.(2R+\Delta R)}$

The negative sign indicates that $V_B > V_A$ due to increase in value of R_T.

The output voltage of the bridge is applied to the differential instrumentation amplifier consisting of three op-amp as shown in figure 5.11. Two voltage followers help to avoid loading of the bridge circuit. The gain of the basic differential amplifier is: $(-R_F / R_1)$. Therefore the output voltage $V_O = V_{AB} (-R_F / R_1)$ ie $V_O = \frac{-\Delta R.(V_{DC})(-R_F)}{2.(2R+\Delta R).R_1}$

Since ΔR is very small (2R+ΔR)≈ (2R), therefore, $V_O = \frac{\Delta R.(V_{DC})(R_F)}{(4R).R_1}$

From this equation it is observed that V_O is directly proportional to change in resistance ΔR, hence a change in physical energy can be easily measured.

Applications of Instrumentation Amplifier:

1. Temperature Indicator.
2. Temperature controller.
3. Light intensity meter.
4. Measurement of flow and thermal conductivity.
5. Analog weight scale.

DIFFERENTIAL INPUT AND DIFFERENTIAL OUTPUT AMPLIFIER:

This amplifier is most commonly used as a preamplifier and in driving push-pull arrangements. Figure 5.12 shows the circuit diagram of differential input and differential output amplifier.

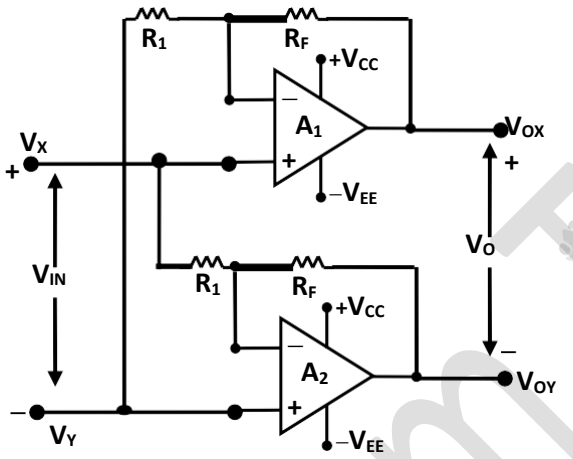


Figure 5.12: Differential input and Differential output amplifier

Circuit consist of two identical op-amps. The analysis of circuit can be accomplished by determining the output of each op-amp due to differential input.

Using superposition theorem, output V_{OX} due to inputs V_X and V_Y is given as- $V_{0X} = (1 + \frac{R_F}{R_1}) V_X - (\frac{R_F}{R_1}) V_Y$

Similarly, the output V_{OY} is- $V_{0Y} = (1 + \frac{R_F}{R_1}) V_Y - (\frac{R_F}{R_1}) V_X$

However, the differential output V_O is-

$V_O = V_{OX} - V_{OY}$

Therefore substituting V_{OX} and V_{OY} in above equation we get-

$V_O = (1 + \frac{2R_F}{R_1}) (V_X - V_Y) = (1 + \frac{2R_F}{R_1}) (V_{IN})$

This means that the differential input and output are in phase. This amplifier is useful in noisy environment, especially if the input is relatively smaller, because it rejects the common mode noise voltages.

VOLTAGE SERIES FEEDBACK AMPLIFIER:

This is basically a practical non inverting amplifier with feedback also called as closed loop non inverting amplifier.

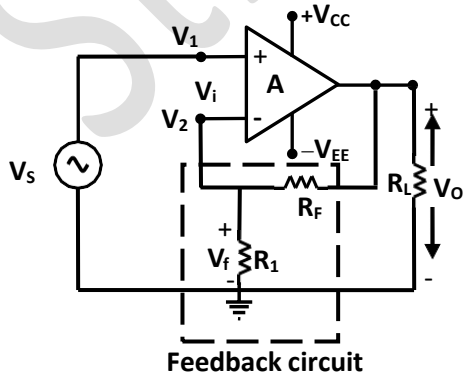


Figure 5.13: Voltage Series feedback amplifier

Op-amp is in forward path while the feedback circuit consists of the resistances R_1 and R_F. Input is applied to non-inverting terminal. Voltage across R_1 is the feedback voltage V_f. V_f is given to inverting terminal which opposes the input voltage by 180° which ensures that feedback is negative.

Closed loop voltage gain, $A_f = V_O / V_S$

Open loop voltage gain, $A = V_O / V_i$

where V_i (Difference of input voltage) $= V_1 - V_2$

Feedback factor, $\beta = V_f / V_O$

Closed Loop Voltage gain of voltage series feedback amplifier:

As defined, $A_f = V_O / V_S$

The output voltage $V_o = A.V_i = A (V_1 - V_2)$ 5.25

From figure 5.13, $V_1 = V_S$ and $V_2 = V_f = \frac{R_1.V_O}{R_1+R_F}$ 5.26

Substituting the value of V_1 and V_2 in equation 5.25 and rearranging, we get

$$V_0 = \frac{A.V_S(R_1 + R_F)}{R_1 + R_F + AR_1}$$

Thus,

$$A = \frac{V_0}{V_S} = \frac{A.(R_1 + R_F)}{R_1 + R_F + AR_1} \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots 5.27$$

Generally, A is very large (typically 10^5). Therefore $(A.R_1) >> (R_1+R_F)$ and $(R_1+R_F+A.R_1) \approx A.R_1$

Thus,

$$= \frac{V_0}{V_S} = 1 + \frac{R_1}{R_F} \quad \text{(Ideal)} \ldots\ldots 5.28$$

Since the feedback factor, $\beta = V_f / V_O$

Thus from equation 5.26, $\beta = \frac{V_F}{V_O} = \frac{R_1}{R_1+R_F}$ 5.29

Comparing equation 5.27 and 5.28, we can conclude that: $A = \frac{1}{\beta}$ (Ideal) 5.30

Closed loop voltage gain in terms of open loop gain A and feedback factor, β as follows:

Rearranging the equation 5.27 we get:

$$= \frac{V_0}{V_S} = \frac{(\frac{R_1 + R_F}{R_1 + R_F})}{\frac{R_1 + R_F}{R_1 + R_F} + \frac{R_1}{R_1 + R_F}}$$

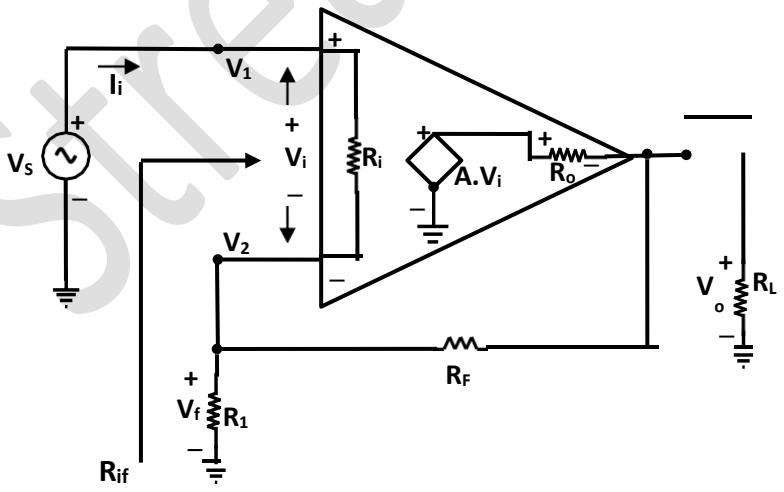
Using equation 5.29, we get:

$$A_f = \frac{V_O}{V_S} = \frac{A}{1 + (A.\beta)} \ldots\ldots 5.31$$

Where, A = open loop voltage gain; A_f = closed loop voltage gain; β= gain of feedback circuit; (A.β)= loop gain

Input Resistance with feedback(R_{if}) of voltage series feedback amplifier:

Figure shows the voltage series feedback amplifier with the op-amp equivalent circuit.



R_i= Open loop input resistance of op-amp

R_{iF}= input resistance with feedback

Figure 5.14: Voltage Series Feedback with op-amp equivalent circuit (Input Resistance)

The input resistance with feedback is defined as- $R_{if} = \frac{V_S}{I_i} = \frac{V_S}{(V_i/R_i)}$

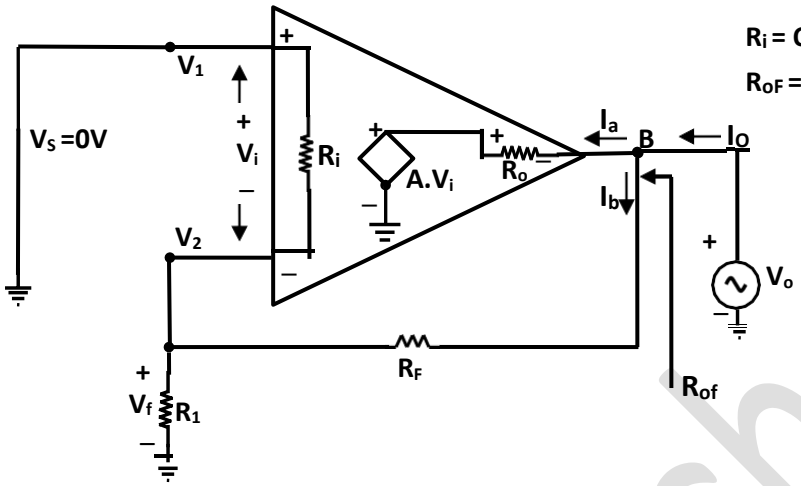
However, $V_i = \frac{V_O}{A}$ and $V_O = \frac{A}{1+A\beta} V_S$

Therefore, **$R_{if} = R_i (1+A\beta)$**.....**5.32**

From equation 5.32 we conclude that the input resistance of op-amp with feedback is (1+Aβ) times that without feedback.

Output Resistance with feedback (R_{of}) of voltage series feedback amplifier:

Output resistance is the resistance determined looking back into the feedback amplifier from the output terminal as shown in figure 5.15.



R_i = Open loop input resistance of op-amp

R_{oF} = Output resistance with feedback

Figure 5.15: Voltage Series Feedback with op-amp equivalent circuit (Output Resistance)

Output resistance is obtained by using Thevenin's theorem, by making $V_S = 0V$, and by applying external voltage V_o.

R_{of} is defined as; **$R_{of} = V_O / I_O$**.....**5.33**

Applying KCL at output node B, we get $I_O = I_a + I_b$

Since, $I_a >> I_b$. Therefore, $I_O \approx I_a$

Applying KVL for the output loop- we get, $V_O - R_O.I_O - A.V_i = 0$

Therefore,

$$o = \frac{V_0 - .V_i}{R_o}$$

However, $V_i = V_1 - V_2 = 0 - V_f$ (since, $V_S = V_1 = 0V$ and $V_2 = V_f$)

Therefore,

$$V_i = -\frac{R_1.V_O}{R_1 + R_F} = -\beta V_O$$

Therefore,

$$o = \frac{V_0 + \beta.V_0}{R_o}$$

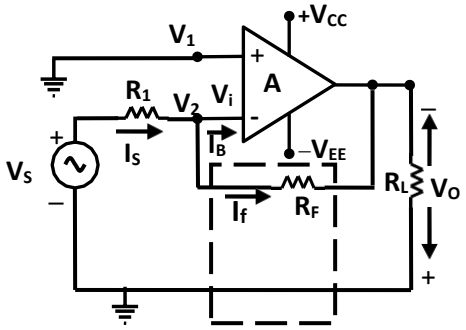
Substituting the value of I_O in equation 5.33, we get

$$R_{of} = \frac{R_O}{1 + A.\beta} \quad \text{.....} \quad 5.34$$

Equation 5.34 shows that the output resistance with feedback is [1/(1+Aβ)] times the output resistance R_O of the op-amp ie. the output resistance with feedback is much smaller than the output resistance without feedback.

VOLTAGE SHUNT FEEDBACK AMPLIFIER:

It is also called as inverting amplifier with feedback. Figure 5.16 shows the voltage shunt feedback amplifier. Input voltage is applied to inverting terminal and amplified as well as inverted output signal is applied to inverting input via feedback resistor R_F and this arrangement forms a negative feedback. Non inverting terminal is grounded.



Feedback circuit

Figure 5.16: Voltage Shunt feedback amplifier

Closed Loop Voltage gain of voltage shunt feedback amplifier:

From figure 5.13, writing KCL at input node V_2,

$I_S = I_B + I_f$ 5.35

Input bias current is very small because very high input impedance (R_i).

Therefore , $I_S \approx I_f$

$\frac{V_S - V_2}{R_1} = \frac{V_2 - V_0}{R_F}$ 5.36

Since, the output voltage $V_o = A.V_i = A\,(V_1 - V_2)$ 5.37

$(V_1 - V_2) = V_o / A$ Since, $V_1 = 0V$

Therefore , $(V_2) = -(V_o / A)$ 5.38

Substituting the equation 5.38 in equation 5.36, we get

$$A = \frac{V_0}{V_S} = -\frac{AR_F}{R_1 + R_F + AR_1}(exact) \quad \text{..... 5.39}$$

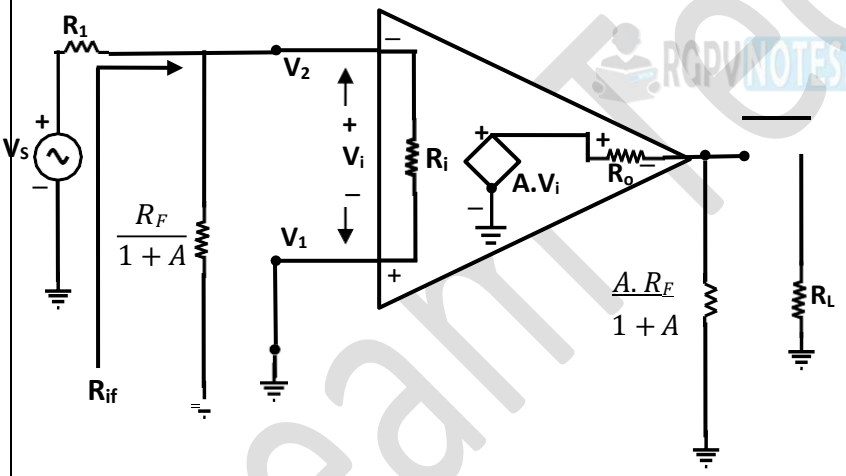
Since, the internal gain A of op-amp is very large, $A.R_1 >> R_1 + R_F$

Hence, equation 5.39 can be rewritten as-

$$A = \frac{V_0}{V_S} = -\frac{R_F}{R_1}\ (ideal) \quad \text{.....5.40}$$

This equation shows that gain of inverting amplifier is set by values of feedback and input resistors. The negative sign indicates that input and output is out of phase by 180°.

Input resistance with feedback of voltage shunt feedback amplifier:



Ri= Open loop input resistance of op-amp

RiF= input resistance with feedback

Figure 5.17: Inverting amplifier with Millerized feedback resistor

Millerize the feedback resistor R_F; ie. splitting the R_F into two miller components as shown in figure 5.17 to find the input resistance.

From the circuit, the input resistance with feedback R_{if} is then , $R_{if} = R_1 + \frac{R_F}{1+A} // (R_i)$

Output resistance with feedback of voltage shunt feedback amplifier:

The equivalent circuit for output resistance with feedback R_{of} of inverting amplifier is same as that for non inverting amplifier because the output resistance of inverting amplifier must be same to that of the non inverting amplifier.

$$R_{of} = \frac{R_O}{1 + A.\beta} \quad \text{..... } 5.41$$

LOGARITHMIC AMPLIFIER:

Figure 5.18 shows the circuit diagram of logarithmic amplifier. The output voltage is always proportional to the natural logarithm of the input voltage, hence called as logarithmic amplifier. Basically circuit is an inverting amplifier in which feedback resistor R_F is replaced by a p-n junction diode D. For satisfactorily operation of this amplifier, diode has to be forward biased, so the input signal must have positive values only.

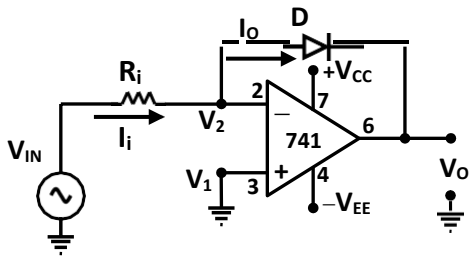


Figure 5.18: Logarithmic Amplifier

Mathematically, diode current equation is given as:

$$= _R.[(e^{(V_D/V_T)}) - 1]$$

Where, I is diode current, I_R is diode reverse saturation current, V_D is the applied voltage and V_T is the volt equivalent of temperature.

When diode is forward biased, $V_D >>> V_T$, hence

$(e^{(V_D/V_T)}) \gg 1$

Therefore,

$$= _R.[(e^{(V_D/V_T)})] \quad \ldots\ldots 5.42$$

From the circuit diagram, using the virtual ground concept, we have: $I_i = -I_O$

So, $\frac{V_{IN}}{R} = -\ _R.[(e^{(V_D/V_T)})] \quad \ldots\ldots 5.43$

But, voltage across diode D is equal to output voltage V_O. Hence, equation 5.43 becomes

$\frac{V_{IN}}{R_i} = -\ _R.[(e^{(V_O/V_T)})] \quad \ldots\ldots 5.44$

Taking natural logarithm on both sides, we have

$$\ln[\frac{V_{IN}}{R\ _i R}] = -[\frac{V_O}{V_T}] \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots 5.45$$

Hence,

$$V_0 = -V_T.n[\ \frac{V_{IN}}{R_i I_R}] \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots 5.46$$

From equation 5.46, since V_T, I_R and R_i are constants, then V_O is directly proportional to natural logarithm of V_{IN}.

ANTILOGARITHMIC AMPLIFIER or EXPONENTIAL AMPLIFIER:

Antilogarithmic amplifier is obtained by changing the position of diode D and resistor R_i in a logarithmic amplifier, as shown in figure 5.19. The output voltage of this amplifier is always proportional to the antilogarithmic of the input voltage. For satisfactorily operation of this amplifier, diode has to be forward biased, so the input signal must have positive values only.

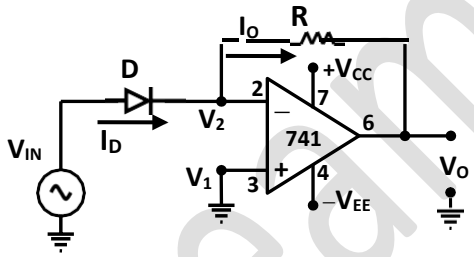


Figure 5.18: Antilogarithmic Amplifier

Mathematically, diode current equation is given as:

$$= _R.[(e^{(V_D/V_T)}) - 1]$$

Where, I is diode current, I_R is diode reverse saturation current, V_D is the applied voltage and V_T is the volt equivalent of temperature.

When diode is forward biased, $V_D >>> V_T$, hence

$(e^{(V_D/V_T)}) \gg 1$

Therefore,

$$= _R.[(e^{(V_D/V_T)})] \quad \ldots\ldots 5.47$$

Therefore,

$$_{IN} = _D = _R.[(e^{(V_D/V_T)})] \quad \ldots\ldots 5.48$$

But the diode voltage V_D is equal to the input voltage V_{IN}, therefore

$$_{IN} = _D = _R.[(e^{(V_{IN}/V_T)})]$$

From the circuit diagram, using the virtual ground concept, we have: $I_{IN} = -I_O$

Therefore, $_R.[(e^{(V_{IN}/V_T)})] = -(\frac{V_O}{R})$ ie. $V_O = -(I_R.R)(e^{(V_{IN}/V_T)}) \quad \ldots\ldots 5.4$

From equation 5.49, Since V_T, I_R and R are constants, we have output voltage V_O is directly proportional to antilog of V_{IN}.

TRIANGULAR WAVE GENERATOR:

Triangular wave generator, as shown in figure 5.19 can be formed by connecting the output of square wave generator to an integrator. The frequencies of the square wave and triangular wave are the same.

The frequency of triangular wave will increase or decrease as resistor R increases or decreases. Although the amplitude of the square wave is constant ($\pm V_{sat}$); the amplitude of the triangular wave decreases with an increase in its frequency and vice versa as shown in figure 5.21. The input to the integrator is a square wave, while its

output is a triangular wave. For a perfect triangular wave output the circuit time constant ($5.R_3.C_2$) > T/2, where T is the time period of the square wave input. The output frequency is limited by the slew rate of the op-amp. Therefore, for generation of relatively higher frequencies, high slew rate op-amp are used.

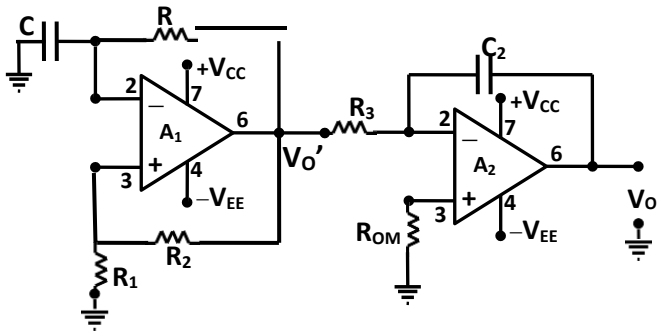


Figure 5.19

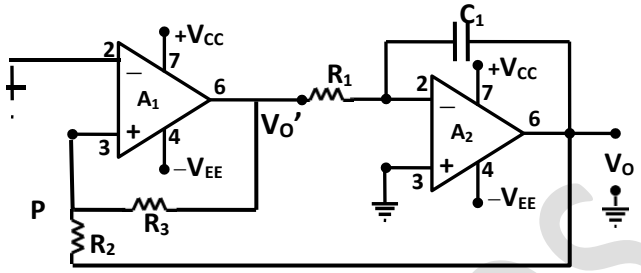


Figure 5.20

Another triangular wave generator, with fewer components is shown in figure 5.20. Op-amp A_1 operates as a comparator and A_2 as an integrator. The voltage drop across R_2 appears at the point P which is the actual input appearing at the non-inverting terminal of op-amp A_1. This voltage at point P continuously compared with the voltage at inverting terminal of op-amp A_1, which is at ground potential. When the potential at point P is positive and greater than the potential at inverting terminal, the output voltage swings to positive saturation, where as potential P is negative the output voltage swings to negative saturation.

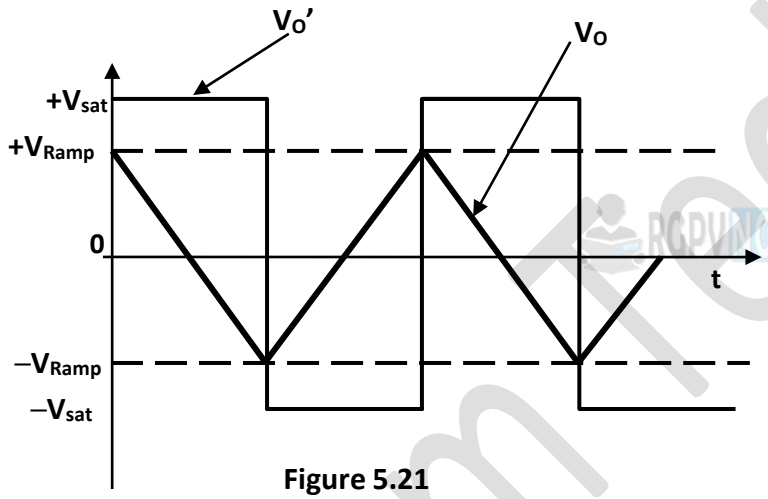


Figure 5.21

Circuit operation: Let the output of op-amp A_1 is at $+V_{SAT}$ ($+V_{CC}$). This $+V_{SAT}$ is an input to integrator A_2. The output of A_2, therefore will be negative going ramp. This means that the one end of the voltage divider R_2-R_3 is at $+V_{SAT}$ of A_1 and the other end is the negative going ramp of A_2. When negative going ramp attains a certain value $-V_{Ramp}$, point P potential becomes negative and the output amplifier A_1 swings from positive saturation to negative saturation. The output of op-amp A_2 will now start increasing until it reaches a voltage level equal to $+V_{Ramp}$. At this value of the output, the potential at point P becomes positive forcing the output of op-amp A_1 from $-V_{SAT}$ to $+V_{SAT}$.

This process repeats and the triangular wave output gets generated as shown in figure 5.21. The triangular and square wave output frequencies are same and the amplitudes of square wave is proportional to the saturation voltages $-V_{SAT}$ and $+V_{SAT}$. The amplitude of triangular wave is given as: $-V_{Ramp} = -(R_2/R_3)(+V_{SAT})$ and similarly, $+V_{Ramp} = -(R_2/R_3)(-V_{SAT})$.

Hence the peak to peak (PP) output amplitude of triangular wave is:

$V_O(PP) = +V_{Ramp} - (-V_{Ramp}) = 2(R_2/R_3)(V_{SAT})$ where $V_{SAT} = |+V_{ST}| = |-V_{ST}|$

Above equation indicates that amplitude of triangular wave decreases with an increase in resistor R_3.

The time period T of the triangular wave is given by the expression: **$T = [(4.R_1.R_2.C_1) / (R_3)]$**

The frequency of oscillation of the triangular wave is given by: **$f = 1/T = [(R_3) / (4.R_1.R_2.C_1)]$**

PHASE SHIFT OSCILLATOR: Figure 5.22 shows the phase shift oscillator, which consists of op-amp as the amplifying stage and three RC cascaded networks as the feedback circuit. Phase shift of 180° is provided by op-amp which is used in inverting mode whereas additional 180° phase shift is provided by the cascaded RC networks. Thus the total phase shift around the loop is 360°.

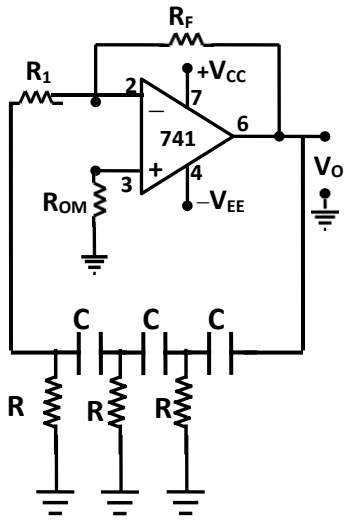


Figure 5.22: Phase shift Oscillator

At some specific frequency, when phase shift of RC network is exactly 180° and gain of amplifier is sufficiently large, oscillation occurs at that frequency. The frequency of oscillation is given as:

$$f_o = \frac{1}{2RC\sqrt{6}} =$$

At this frequency, the gain of amplifier must be 29. ie. $|\frac{R_F}{R_1}| = 29.$

Means, the circuit will produce a sinusoidal waveform of frequency f_o if the gain is 29 and the total phase shift around the loop is 360°.

WEIN BRIDGE OSCILLATOR:

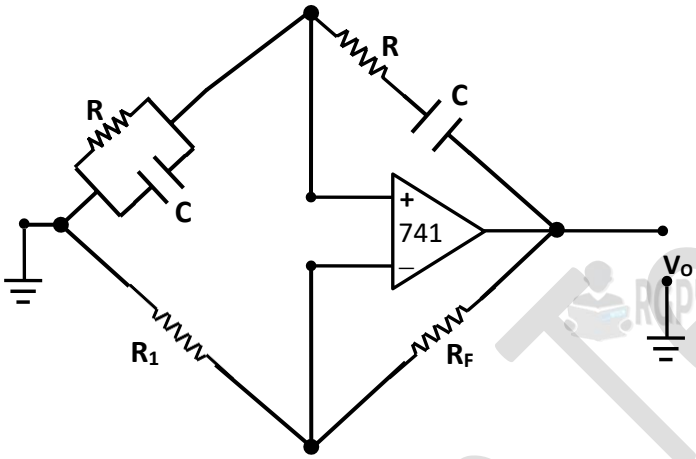


Figure 5.23: Wein Bridge Oscillator

Oscillator used to generate audio frequency is the wein bridge oscillator as shown in figure 5.23. It provides frequency stability. Wein bridge is connected between the amplifier input terminals and the output terminals. Bridge has RC series and RC parallel network in two arms and in remaining arms R_1 and R_F resistors are connected as shown in figure.

Total phase shift of 360° around the circuit occurs only when the bridge is balanced ie. at resonance.

The frequency of oscillation is given by:

$$f_o = \frac{1}{2RC}$$

At this frequency the gain required for sustained oscillation is given by $A = 1/\beta = 3$

Ie. $1+ (R_F/R_1) = 3$ or $R_F = 2R_1$.

ANALOG MULTIPLIER-MPY634:

Analog multiplier IC is commonly used to perform various mathematical operations such as voltage divider, frequency doubling squaring, square rooting etc.

Basic multiplier and its characteristics:

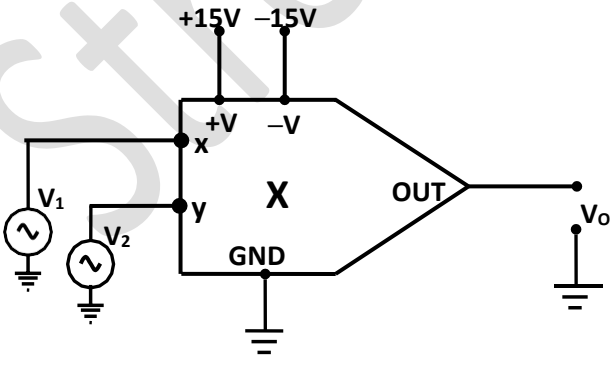


Figure 5.24: Multiplier IC Symbol

Basic multiplier is an active circuit in which output voltage is proportional to the product of input signals.

Output of multiplier is : $V_O = K.V_1.V_2$ where, $K = 1/(V_{ref})$

Usually V_{ref} is set to 10V internally, hence,

$V_O = (V_1.V_2) / 10$ 5.50

If, $(V_1.V_2) < V_{ref}$, the output of multiplier will not saturate.

Depending upon the polarity restriction of the inputs, the IC operation is called as-

a)One Quadrant multiplier: In such operation, polarity of inputs must always be positive.

b) Two quadrant Multiplier: This multiplier functions properly, if one input is held positive and the other is allowed to swing in both positive and negative.

c) Four Quadrant Multiplier: This multiplier functions properly, if both the inputs are allowed to swing in both positive and negative directions.

Applications of Multiplier:

1) In communication, it is used in amplitude modulation, frequency modulation, phase modulation etc.
2) In instrumentation and control, to measure velocity, acceleration, automatic gain control etc.
3) For voltage controlled applications.
4) It is used for voltage divider, true RMS calculation etc.
5) Used for frequency converters, frequency doubling etc.
6) It is used for squaring, square root calculations and solving non-linear equations.
7) It is used in oscillators.

Voltage Divider using Multiplier:

Figure 5.25 shows the voltage divider circuit using multiplier. Voltage divider is the circuit in which the output is the division of two input signals. As shown in figure the multiplier is used in feedback loop. Denominator is applied to X input of multiplier and denominator at inverting input of op-amp.

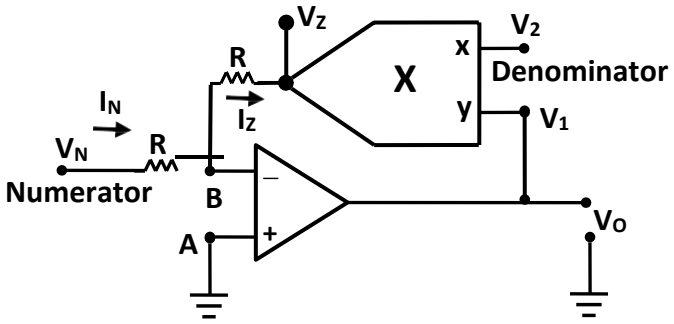


Figure 5.25: Voltage Divider Circuit using Multiplier

Node A and B is at same potential, due to virtual ground concept ie $V_A = V_B = 0V$. As input is applied to inverting terminal, so, $I_N = -I_Z$.
Therefore, $(V_N/R) = -(V_Z/R)$
Since , $V_Z = K.V_1.V_2$ and $V_1 = V_O$
Hence, $(V_N/R) = -[K.V_O.V_2/R]$
Therefore, $\mathbf{V_O = -[V_N / (K.V_2)]}$
Thus the output is proportional to the division of two input voltages V_N and V_2. Input voltage V_2 is negative, hence divider circuit are two quadrant circuits.

Squaring Circuit using Multiplier:

Figure 5.26 shows the circuit diagram of squaring circuit using multiplier.

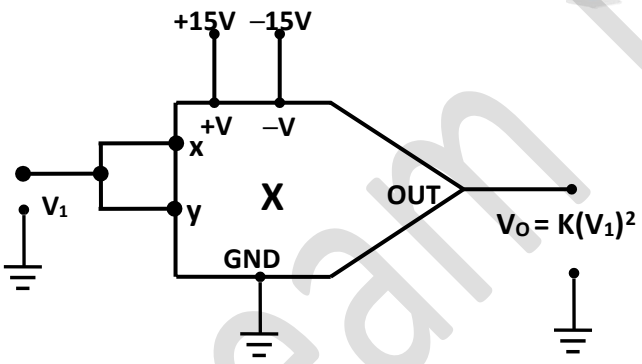
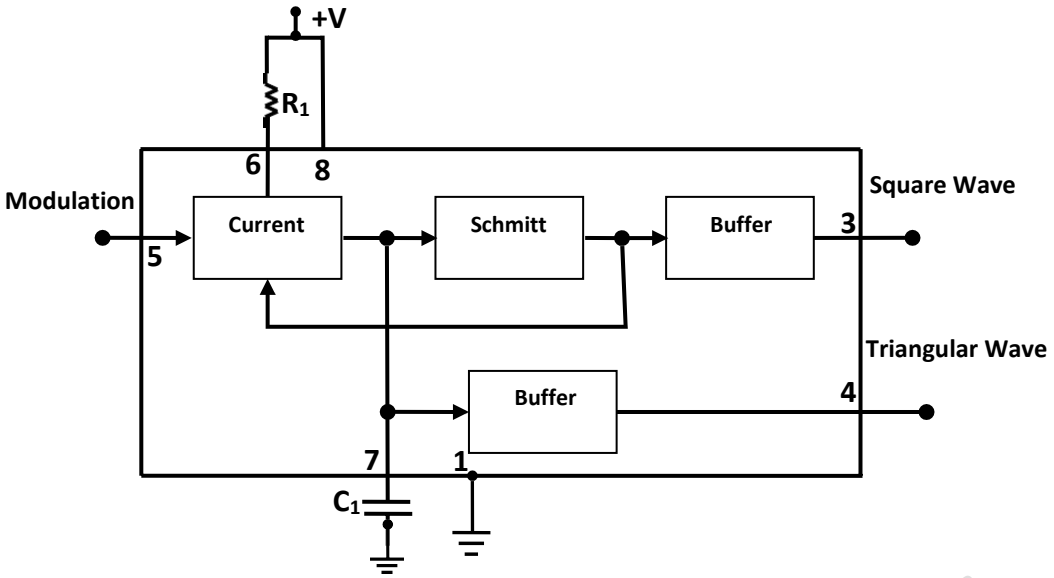


Figure 5.26: Squaring Circuit using Multiplier

Squaring circuit gives the square of the input voltage applied.
From figure, same input voltage (V_1) is applied to both the input terminals of multiplier. Hence the output voltage is given as, $\mathbf{V_O = K.(V_1)^2}$
Thus the output is proportional to the square of the input.

VOLTAGE CONTROLLED OSCILLATOR (VCO):

In some applications such as frequency modulation, frequency shift keying, where the frequency is controlled by an input voltage (also called control voltage). Such type of frequency control is achieved in voltage controlled oscillator (also called voltage to frequency converter).



1: Ground
2: NC
3: Square Wave Output
4: Triangular Wave Output
5: Modulation input
6: R_1
7: C_1
8: +V

Figure 5.27: Block diagram of 566 VCO

Figure 5.27 shows the block diagram of 566 VCO. Triangular wave output is generated by charging and discharging of capacitor C1 ,by current sources. A charge and discharge level are determined by Schmitt trigger and also provides square wave output. Both the output waveforms are buffered so that the output impedance of each will be equal.

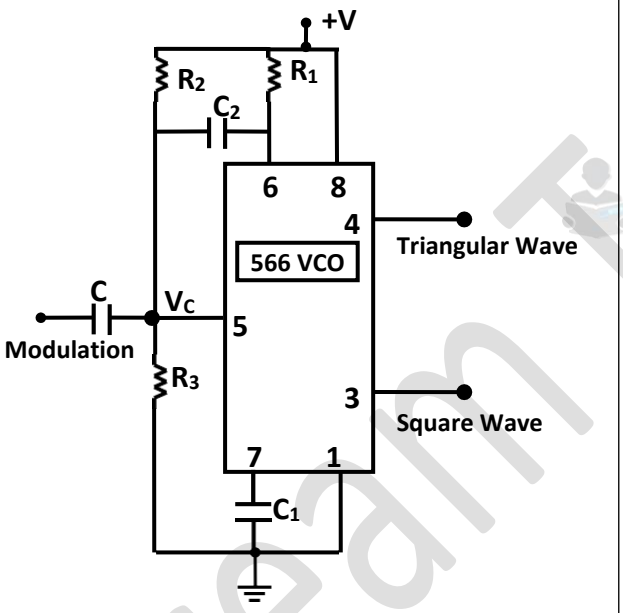


Figure 5.28: Connection diagram of 566 VCO

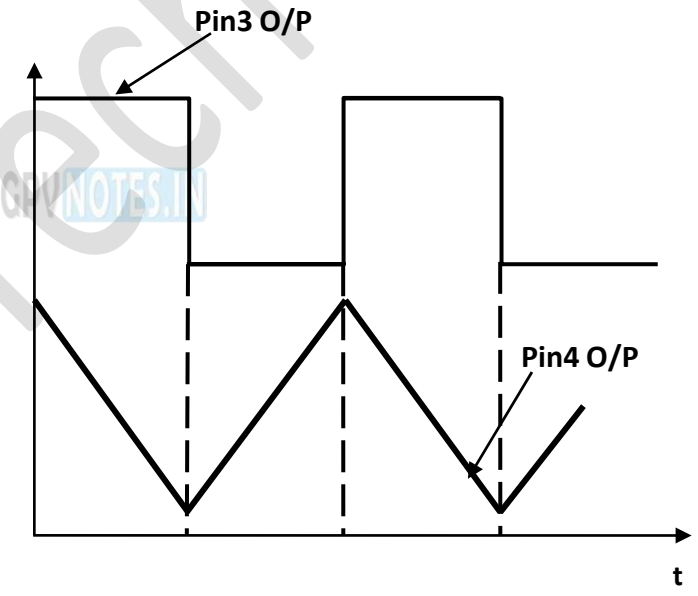


Figure 5.29: Output Waveforms of 566 VCO

Figure 5.28 is the connection diagram. R_1C_1 combination provides the free running frequency. Control voltage V_C is set by voltage divider formed by R_2 and R_3. The modulating signal is ac coupled with capacitor C and must be less than $3V_{P\text{-}P}$. The frequency of oscillation of output waveforms is given by:

$$f_O = \{ [\, 2\,(+V - V_C)] \,/\, [R_1C_1(+V)] \,\}$$

where, $2k\Omega < R_1 < 20k\Omega$ and $[\,(¾)(+V_C)] \le V_C \le +V$. For the fixed value of V_C and constant C_1, f_O can be carried over a 10:1 frequency range by choosing R1 between 2kΩ and 20kΩ. Similarly, for constant R_1C_1 product, f_O can be modulated over a 10:1 range by the control voltage V_C.

If VCO has to drive standard logic circuitry, dual supply of ±5V is used, so that square wave output has a proper DC level.

Applications of VCO:

1) FM modulation. 2) Frequency Shift Keying. 3) Signal generation (Square and Triangular) 4) Function Generation. 5) Converting low frequency signals such as electroencephalograms (EEG) or electrocardiograms (EKG) into a audio frequency range. 6) In frequency multipliers.

COMPARATOR:

An open loop op-amp, which compares a signal voltage on one input with the known voltage (reference voltage) on other input of op-amp is called a comparator. Output of comparator may be $+V_{SAT}$ and $-V_{SAT}$, depending on which input is largest. Comparators are used in circuits such as Schmitt triggers, voltage level detectors, oscillators and digital interfacing.

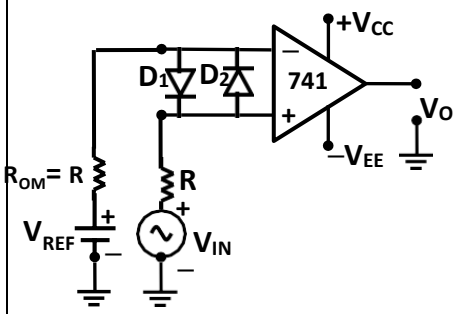


Figure 5.30: Non-Inverting Comparator

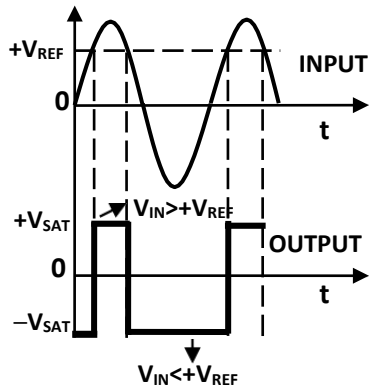


Figure 5.31: Output for $+V_{REF}$

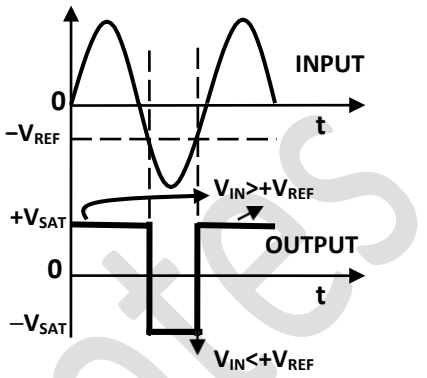


Figure 5.32: Output for $-V_{REF}$

Figure 5.30 shows the circuit diagram of non-inverting comparator. From the circuit diagram, a fixed reference voltage is applied to inverting terminal of op-amp and a time-varying sinusoidal signal is applied to non-inverting input, hence the circuit is called as non-inverting comparator. Here the reference voltage V_{REF} is positive. When the $V_{IN} < V_{REF}$ (ie. voltage at inverting input is higher than non-inverting input), the output V_O is at $-V_{SAT}$ ($\approx -V_{EE}$). On the other hand, when the $V_{IN} > V_{REF}$ (ie. voltage at non- inverting input is higher than inverting input), the output V_O is at $+V_{SAT}$ ($\approx +V_{CC}$). Thus the output voltage V_O changes from one saturation level to another whenever $V_{IN} \approx V_{REF}$, as shown in figure 5.31. Hence, we can say that the comparator is a type of ADC converter. Diodes D_1 and D_2 are called clamping diodes because the difference input voltage, V_i of op-amp is clamped to either +0.7V and –0.7V. These diodes also protect the op-amp from damage due to excessive input voltage V_{IN}. Resistance R is used to limit the current through diodes. To minimize the offset problems, $R_{OM} \approx R$ is connected in between V_{REF} and inverting input of op-amp. Figure 5.32 shows the input and output waveforms when the reference voltage (V_{REF}) is negative.

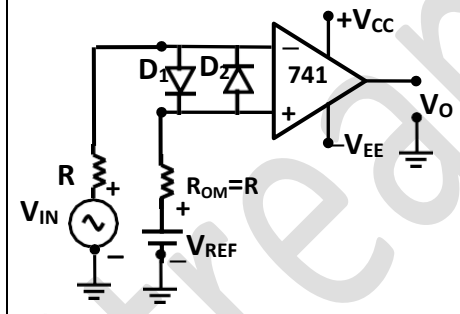


Figure 5.33: Inverting Comparator

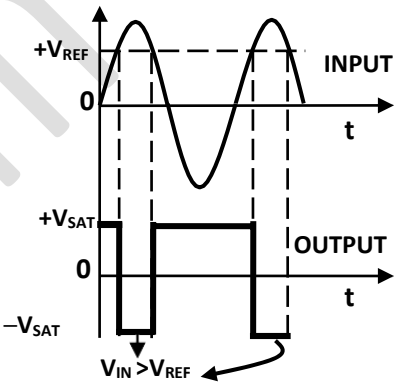


Figure 5.34: Output for $+V_{REF}$

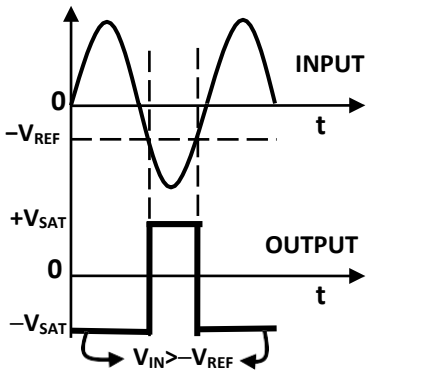


Figure 5.35: Output for $-V_{REF}$

Figure 5.33 shows the inverting comparator. Here V_{IN} is applied to inverting terminal of op-amp and V_{ref} is applied to non-inverting terminal of op-amp. With sinusoidal input waveform, the output waveform for negative reference and positive reference voltage is shown in figure 5.34 and 5.35.

ZERO CROSSING DETECTOR:

Inverting or non-inverting comparator can be used as a zero crossing detector provided that reference voltage ,V_{ref} is set to zero volts ($V_{ref} = 0V$) as shown in figure 5.36. The output voltage V_O switches and saturates positively and negatively, whenever input signal V_{IN} crosses zero volts. Output voltage V_O is driven into negative saturation when the input signal V_{IN} passes through zero volts in positive direction and V_O is driven into positive saturation when the input signal V_{IN} passes through zero volts in negative direction as shown in figure 5.37. The output waveform is a square wave. Hence the zero crossing detector is also called as sine wave-to-square wave converter.

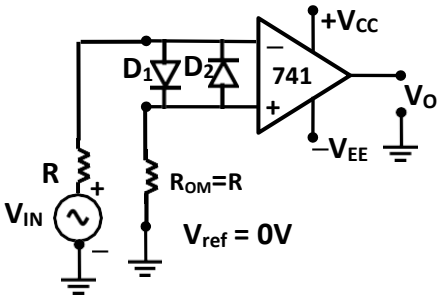


Figure 5.36: Zero Crossing Detector

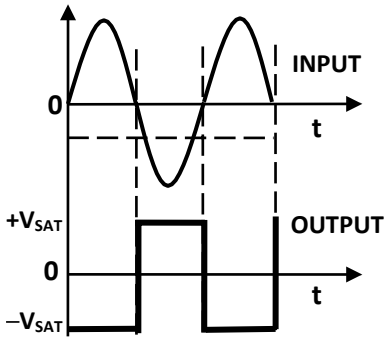


Figure 5.37: Input and output Waveforms

For low frequency input signal (slowly changing waveform), V_{IN} take more time to cross 0V, hence switching at the output will also take time. On the other hand, because of noise at the op-amps input terminals, output fluctuates between $+V_{SAT}$ and $-V_{SAT}$, detecting zero reference crossing for noise as well as input V_{IN}. These problems can be cured by the use of positive feedback or regenerative feedback, that causes the output to change faster and eliminate any false output transitions due to noise at the input.

OP-AMP AS FILTERS: Characteristics of filters, Classification of filters, Magnitude and frequency response, Butterworth 1st and 2nd order Low pass, High pass and band pass filters, Chebyshev filter characteristics, Band reject filters, Notch filter; all pass filters, self-tuned filters, AGC, AVC using OP-AMP.

TIMER: IC-555 Timer concept, Block pin configuration of timer. Monostable, Bistable and astable Multivibrator using timer 555-IC, Schmitt Trigger, Voltage limiters, Clipper and clampers circuits, Absolute value output circuit, Peak detector, Sample and hold Circuit, Precision rectifiers, Voltage-to-current converter, Current-to-voltage converter.

Voltage Regulator: Simple OP-AMP Voltage regulator, Fixed and Adjustable Voltage Regulators, Dual Power supply, Basic Switching Regulator and characteristics of standard regulator ICs.

OP-AMP AS FILTERS (ACTIVE FILTERS):

Filter is a frequency selective circuit that passes a specific band of frequencies and blocks the frequencies outside this band. Depending on the type of elements used in their construction, filters are classified as active or passive. Passive filters used passive components such as resistors, capacitors and inductors whereas active filters used active components such as transistors or op-amps in addition to resistors and capacitors. The type of elements used dictates the operating frequency of the filter. RC filters are used for low or audio frequency operation, whereas LC filters are used for RF or high frequency operation. In audio frequencies, inductors are not used because they are very large, costly and dissipate more power. Inductors also produce magnetic fields.

Advantage of active filter over passive filter:

1. Gain and frequency adjustment flexibility: Active filter containing active components such as op-amp, is capable of providing a gain, hence the input signal is not attenuated as in passive filter. In addition, active filter is easier to tune or adjust.

2. No loading problems: Because of high input impedance and low output impedance of op-amp, active filter does not cause loading of source or load.

3. Cost: Because of absence of inductors and use of cheaper op-amp in filter circuit, active filters are more economical than passive filters.

TYPES OF FILTERS:

Most commonly type of active filter used are:

(1) Low-pass filter (2) High-pass filter (3) Band-pass filter (4) Band-reject filter (5) All-pass filter

MAGNITUDE AND FREQUENCY RESPONSE OF FILTERS:

All these filters use op-amp as the active element and resistors and capacitors as passive elements. Active element improves the filter performance through their increased slew rates and higher unity gain-bandwidths.

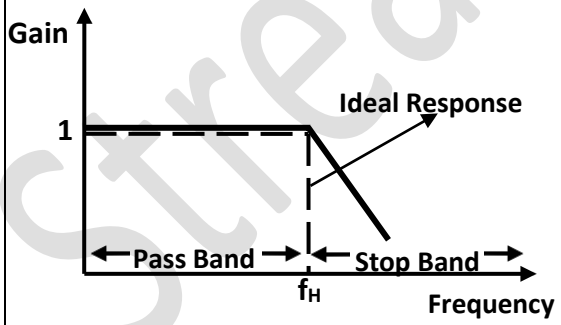


Figure 6.01: Low pass filter frequency response

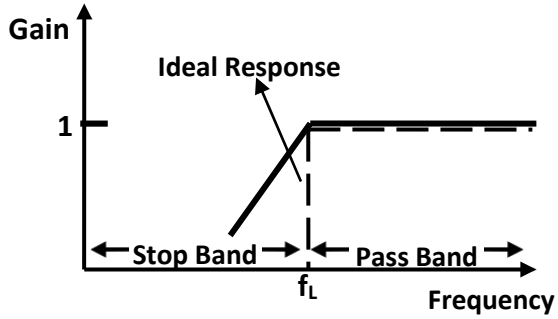


Figure 6.02: High pass filter frequency response

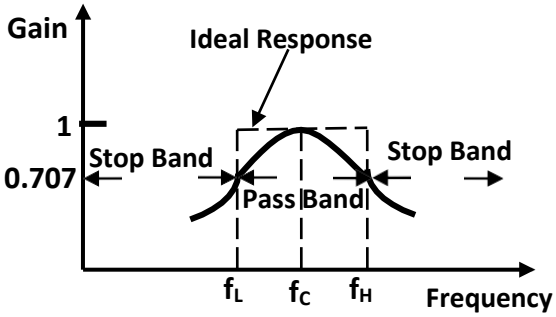


Figure 6.03: Band pass filter frequency response

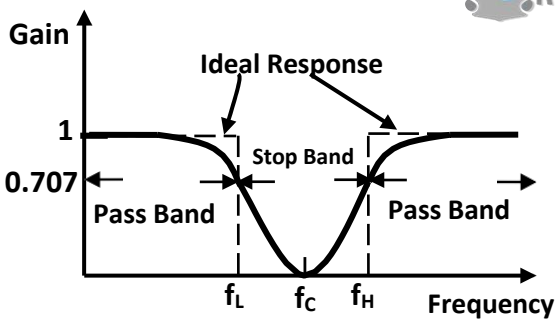


Figure 6.04: Band reject filter frequency response

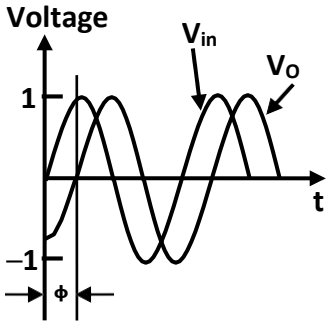


Figure 6.05: All Pass Filter

All type of filter frequency responses are shown from figure 6.01 to 6.04 except all pass filters. A dashed curve indicates the response of ideal filter whereas solid lines indicate practical filter response. Figure 6.01 shows the frequency response of low pass filter. A low pass filter has a constant gain from 0Hz to f_H (high cutoff frequency). Therefore bandwidth is also f_H. After f_H the gain decreases by 3dB ie. $f > f_H$ the gain decreases with increase in input frequency. Hence, frequencies between 0Hz and f_H are known as pass band frequencies, whereas beyond f_H includes stop band frequencies. An ideal filter has zero attenuation in pass band and infinite attenuation in stop band. Practical circuits cannot produce the ideal response, but a close ideal response can be obtained by using special design techniques, precise component values and high speed op-amps.

Some of the commonly used practical filters that approximate the ideal filter response are: (i) Butterworth filter (ii) Chebyshev filter (iii) Cauer filter

Butterworth filter also called as flat-flat filter because it has flat stop and pass band. Chebyshev filter has a ripple pass band and flat stop band, while the cauer filter has ripple pass and stop band.

Figure 6.02 shows a high pass filter with stop band is from frequency ($f > 0$) to frequency ($f < f_L$) while pass band is for frequencies ($f > f_L$) where, f_L is low cut off frequency and f is the operating frequency.

Figure 6.03 shows a band pass filter with pass band is between the two cut off frequencies f_H and f_L here ($f_H > f_L$). The two stop bands are for frequencies ($f > 0$) to ($f < f_L$) and ($f > f_H$). The bandwidth of the band pass filter, therefore, is equal to $(f_H - f_L)$. f_C is the center frequency.

Figure 6.04 shows a band reject or band-stop or band-elimination filter with stop band is between the two cut off frequencies f_H and f_L here ($f_H < f_L$). The two pass bands are from frequencies ($f > 0$) to ($f < f_H$) and ($f > f_L$). f_C is the center frequency.

Figure 6.05 shows the input (V_{in}) and output (V_O) signals of all pass filter where there is a phase shift (ϕ) between input and output signals as a function of frequency. This filter passes all frequencies keeping input and output voltages amplitude equal for all frequencies. The highest frequency up to which the input and output amplitudes remain equal is dependent on the unity gain-bandwidth of the op-amp. At this frequency, the phase shift between input and output is maximum.

The rate at which the gain of the filter changes in the stop band is determined by the order of the filter. For example, for first order filter, the roll-off rate in stop band is 20dB/decade, on the other hand, for second order filter, the roll-off rate in stop band is 40dB/decade.

FIRST ORDER LOW PASS BUTTERWORTH FILTER:

Figure 6.06 (a) and (b) shows the circuit diagram of first order low pass butterworth filter and frequency response plot. Here op-amp is used in non-inverting mode and RC network for filtering. Resistance R_{IN} and R_F determine the gain of the filter.

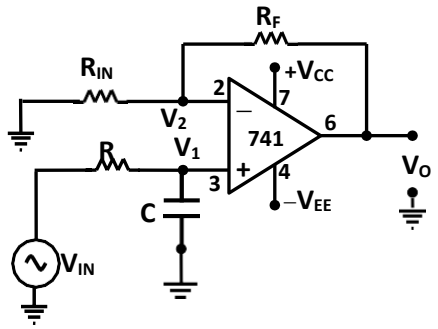


Figure 6.06(a): First order low pass filter

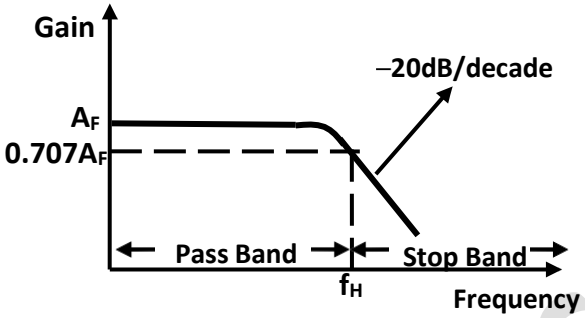


Figure 6.06(b): Frequency response

According to the voltage divider rule, the voltage at the non-inverting terminal (across the capacitor C) is

$V_1 = \frac{-jX_C}{R-jX_C} V_{IN}$ Where, j = √-1 and $-jC = \frac{1}{j2\pi C}$ therefore $V_1 = \frac{V_{IN}}{1+j2\pi RC}$

And the output voltage, $V_O = [1 + (R_F/R_{IN})] V_1$ ie. $V_O = [1 + (R_F/R_{IN})] [V_{IN} / (1+j2\pi.f.R.C)]$ OR

$V_O/V_{IN} = A_F / (1+j2\pi.f.R.C) = A_F / [(1+j(f/f_H)]$ where, (V_O/V_{IN}) is the gain of the filter as a function of frequency.

$A_F = [1 + (R_F/R_{IN})]$ = pass band gain of the filter, f is the frequency of input signal.

$f_H = 1/(2\pi.R.C)$ = high cutoff frequency of the filter.

The gain magnitude and phase angle equation is obtained by converting equation (V_O/V_{IN}) into its equivalent polar form, as follows-

$$\left|\frac{V_O}{V_{IN}}\right| = \frac{A_F}{\sqrt{1+(f/f_H)^2}}$$

and $\phi = -\tan^{-1}\left(\frac{f}{f_H}\right)$ where ϕ is the phase angle in degrees.

The low pass filter operation can be varied from the gain magnitude equation as shown:

(i) At very low frequencies, ie, $f < f_H$, $\left|\frac{V_O}{V_{IN}}\right| \cong A_F$

(ii) At $f = f_H$, $\left|\frac{V_O}{V_{IN}}\right| = \frac{A_F}{\sqrt{2}} = 0.707 A_F$

(iii) At $f > f_H$, $\left|\frac{V_O}{V_{IN}}\right| < \frac{A_F}{\sqrt{2}}$

A low pass filter has a constant gain A_F from 0Hz to the cutoff frequency f_H. At f_H the gain is $0.707A_F$, and after f_H it decreases at a constant rate with an increase in frequency ie, when the frequency is increased tenfold (one decade), the voltage gain is divided by 10 ie the gain decreases 20 dB (= 20 log 10) each time the frequency is increased by 10. Frequency f_H is known as high cutoff frequency or –3dB frequency or break frequency or corner frequency.

FIRST ORDER LOW PASS FILTER DESIGN STEPS:

(i) Choose a value of high cutoff frequency f_H.

(ii) Select the value of C less than or equal to 1µF. Mylar or tantalum capacitors are used for better performance.

(iii) Calculate the value of R using : $R = 1 / (2\pi. f_H. C)$

(iv) Select the values of R_{IN} and R_F depend on the desired pass band gain A_F using $A_F = [1 + (R_F/R_{IN})]$

Example: Design a low pass filter at a cutoff frequency of 1 kHz with a pass band gain of 2.

Solution: f_H = 1 kHz. Assume C = 0.01µF. Then, $R = 1 / (2\pi. f_H. C) = 1 / (2\pi)(10^3)(0.01\mu F) = 15.9k\Omega$

Since the pass band gain is 2, resistors R_{IN} and R_F must have equal values. Let R_{IN} and R_F is 10 kΩ.

FREQUENCY SCALING: Frequency scaling is the procedure used to convert an original cutoff frequency f_H to a new cutoff frequency f_H'. Scaling is done by multiplying R or C, but not both, by the ratio of the original cutoff frequency to the new cutoff frequency.

For example, to change a cutoff frequency from 1kHz to 1.6kHz, multiply 15.9 kΩ resistor by

$\frac{\text{Original cutoff frequency}}{\text{new cutoff frequency}} = \frac{1\text{ kHz}}{1.6\text{ kHz}} = 0.625$. Therefore, new resistor R = (15.9 kΩ)(0.625) = 9.94 kΩ.

Thus the new cutoff frequency is $f_H' = 1 / (2\pi. R. C) = 1 / (2\pi)(9.94x10^3)(0.01\mu F) = 1.6$ kHz.

SECOND-ORDER LOW PASS BUTTERWORTH FILTER:

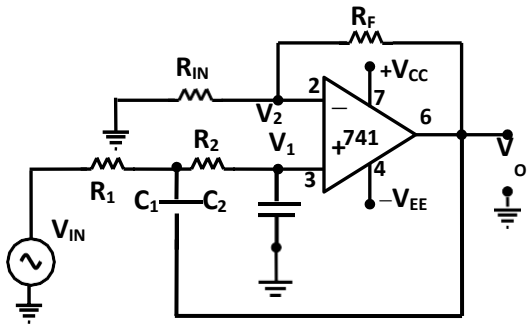


Figure 6.07(a): Second order low pass filter

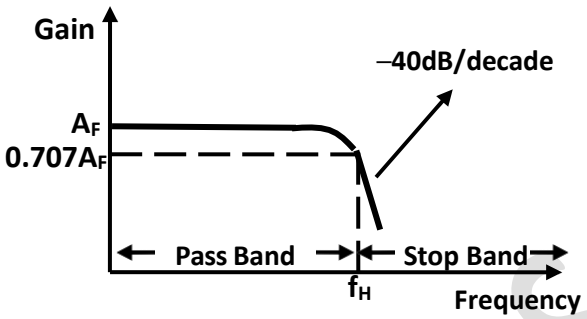


Figure 6.07(b): Frequency response

Figure 6.07 (a) and (b) shows the circuit diagram of second order butterworth low pass filter and frequency response plot. It consists of two RC networks for filtering and op-amp used in non-inverting mode. Resistance R_{IN} and R_F determine the gain of the filter. Roll off of 40dB/decade is obtained in frequency response of second order low pass filter. The high cut off frequency f_H is determined by R_1, C_1, R_2, C_2, as follows-

$f_H = 1 / 2\pi.\sqrt{(R_1. C_1. R_2. C_2)}$ If $R_1 = R_2 = R$ and $C_1 = C_2 = C$, then **$f_H = 1 / (2\pi.R.C)$**

For a second-order low pass butterworth filter response, the voltage gain magnitude equation is

$\left|\frac{V_O}{V_{IN}}\right| = \frac{A_F}{\sqrt{1+(f/f_H)^4}}$ where $A_F = [1 + (R_F/R_{IN})]$ = pass band gain of the filter and f is the frequency of input signal.

SECOND ORDER LOW PASS FILTER DESIGN STEPS:

Design steps of second order low pass filter is same as first order low pass filter, except having twice RC network.

(i) Choose a value of high cutoff frequency f_H.

(ii) Select the value of C ≤ 1μF. Mylar or tantalum capacitors are used for better performance. To simply design calculations, set $R_1 = R_2 = R$ and $C_1 = C_2 = C$

(iii) Calculate the value of R using : $R = 1 / (2\pi. f_H. C)$

(iv)Because of the equal resistor and capacitor values, the pass band gain A_F using $A_F = [1 + (R_F/R_{IN})]$ of second order low pass filter has to be equal to 1.586 ie. $R_F = 0.586\ R_{IN}$. This pass band gain is necessary for butterworth response. Hence select the value of $R_{IN} \leq 100k\Omega$ and calculate the value of R_F.

Example: Design a second order low pass filter at $f_H = 1kHz$.

Solution: $f_H = 1$ kHz. Assume $C_1 = C_2 = C = 0.0047\mu F$.Then, $R_1 = R_2 = R = 1/(2\pi.f_H.C) = 1/(2\pi)(10^3)(0.0047\mu F) = 33.86k\Omega$

Since the pass band gain is 1.586, hence $R_F = 0.586\ R_{IN}$ and let $R_{IN} = 27\ k\Omega$. Therefore $R_F = 15.82\ k\Omega$. Hence, the required components are **$R_F = 15.82\ k\Omega$, $R_{IN} = 27\ k\Omega$, $C_1 = C_2 = C = 0.0047\mu F$ and $R_1 = R_2 = R = 33.86k\Omega$.**

FREQUENCY SCALING: Frequency scaling method of second order low pass filter is same as of first order low pass filter.

FIRST ORDER HIGH PASS BUTTERWORTH FILTER:

Figure 6.08 (a) and (b) shows the circuit diagram of first order high pass butterworth filter and frequency response plot. High pass filter is formed by interchanging frequency determining resistors and capacitors in low pass filter. Here op-amp is used in non-inverting mode and RC network for filtering. Resistance R_{IN} and R_F determine the gain of the filter.

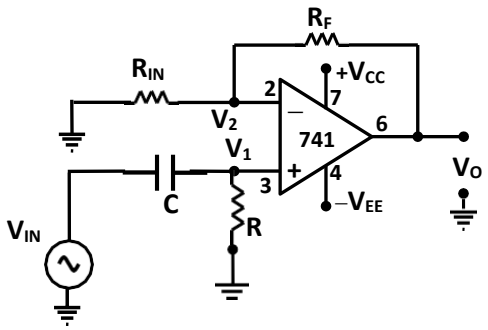


Figure 6.08(a): First order high pass filter

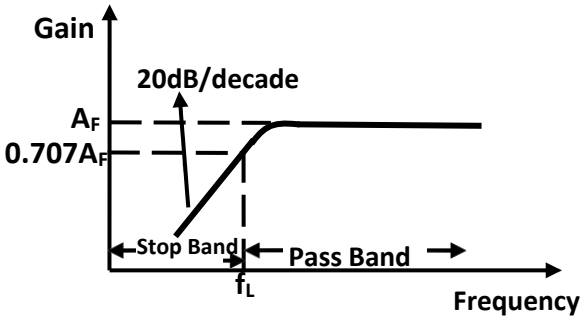


Figure 6.08(b): Frequency response

Figure 6.08(b) shows a frequency response of first order butterworth high pass filter with a low cutoff frequency of f_L. At f_L the magnitude of gain is $0.707A_F$. All frequencies higher than f_L are pass band frequencies with the highest frequency determined by the close loop bandwidth of the op-amp. The gain increases at a rate of 20db/decade.

Output voltage V_O is given by expression: $V_O = [1 + (R_F/R_{IN})] [(j2\pi.f.R.C .V_{IN}) / (1+j2\pi.f.R.C)]$ OR

$$\mathbf{V_O/V_{IN} = A_F / (1+j2\pi.f.R.C) = A_F \{ j(f/f_L) / [(1 + j(f/f_L)]}$$

where, (V_O/V_{IN}) is the gain of the filter as a function of frequency.

$A_F = [1 + (R_F/R_{IN})]$ = pass band gain of the filter, f is the frequency of input signal (Hz).

$f_L = 1/(2\pi.R.C)$ = low cutoff frequency of the filter (Hz).

The gain magnitude equation is obtained by converting equation (V_O/V_{IN}) into its equivalent polar form, as follows-

$$\left|\frac{V_O}{V_{IN}}\right| = \frac{A_F\ (f/f_L)}{\sqrt{1 + (f/f_L)^2}}$$

Designing and frequency scaling procedure of first order high pass filter is same as of first order low pass filter.

SECOND ORDER HIGH PASS BUTTERWORTH FILTER:

Figure 6.09 (a) and (b) shows the circuit diagram of second order high pass butterworth filter and frequency response plot. Here two RC networks are used for filtering and op-amp is used in non-inverting mode . Resistance R_{IN} and R_F determine the gain of the filter.

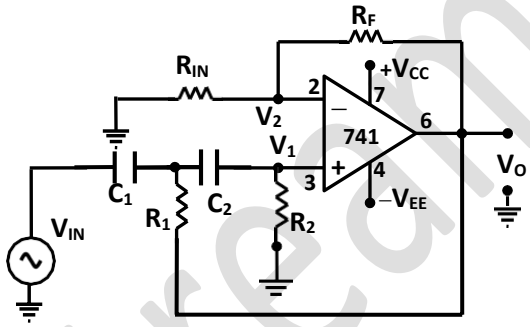


Figure 6.09(a): Second order low pass filter

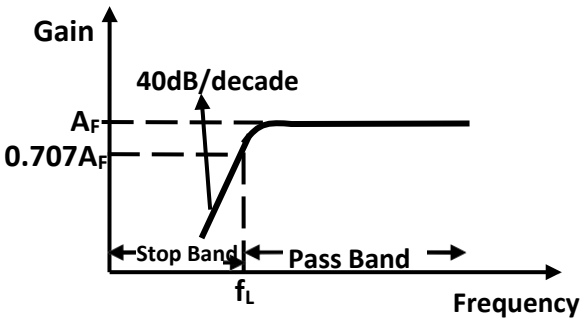


Figure 6.09(b): Frequency response

Figure 6.09(b) shows a frequency response of second order butterworth high pass filter with a low cutoff frequency of f_L. At f_L the magnitude of gain is $0.707A_F$. All frequencies higher than f_L are pass band frequencies with the highest frequency determined by the close loop bandwidth of the op-amp. The gain increases at a rate of 40db/decade.

$A_F = [1 + (R_F/R_{IN})]$ = pass band gain of the filter, f is the frequency of input signal (Hz).

$f_L = 1/(2\pi.R.C)$ = low cutoff frequency of the filter (Hz).

The gain magnitude equation is obtained by converting equation (V_O/V_{IN}) into its equivalent polar form, as follows-

$$\left|\frac{V_O}{V_{IN}}\right| = \frac{A_F}{\sqrt{1 + (f_L/f)^4}}$$

Where, $A_F = 1.586$ = pass band gain for the second order butterworth response.

Designing and frequency scaling procedure of high pass filter is same as of low pass filter because the circuits of both the filters are same except that the position of resistors and capacitors are interchanged.

HIGHER ORDER FILTERS:

Since the gain of filter in the stop band of first and second order filters, changes at a rate of 20 db/decade and 40 db/decade, means that, as the order of filter is increased, the actual stop band response of the filter approaches its ideal stop band characteristic. Higher order filters, such as third, fourth and so on are formed by using first and second order filters.

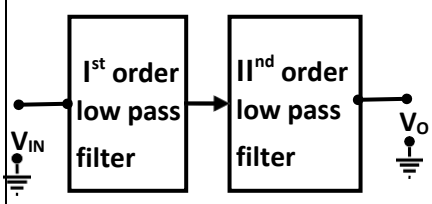


Figure6.10: Third order Filter

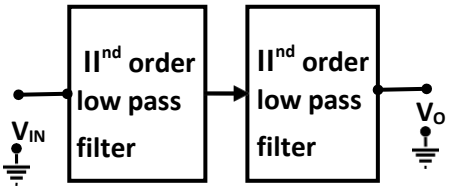


Figure6.11: Fourth order Filter

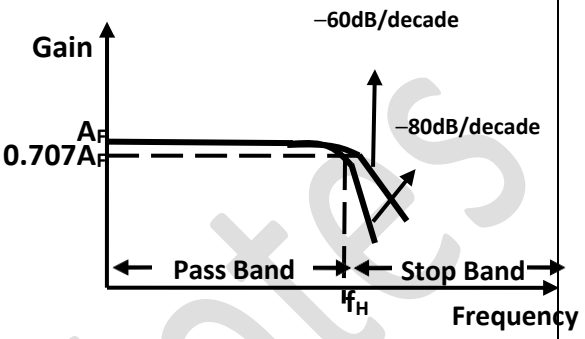


Figure 6.12: Frequency response

Figure 6.10 shows the block diagram of third order low pass filter, formed by cascading first order filter with second order filter whereas figure 6.11 shows the block diagram of fourth order low pass filter, formed by cascading two second order filters. Although there is no limit to the order of the filter, as the order increases, size of filter increases and its accuracy turns down. Also as the order of the filter increases, the difference between the actual and the theoretical stop band response increases. The overall gain of the higher order filter is equal to the product of the individual voltage gains of the filter sections. Since the value of resistors and capacitors used in higher order filter are equal, the high cutoff frequency of higher order filter is given as: $\mathbf{f_H = 1 / (2\pi.R.C)}$

BAND PASS FILTERS:

A filter that passes only a band of frequencies lying in between lower cut off frequency (f_L) and upper cutoff frequency (f_H) and block frequencies above f_H and below f_L is known as band pass filter. There are two types of band pass filter: wide band pass and narrow band pass.

Wide band pass filter has a figure of merit or quality factor Q <10 whereas, Q>10 for a narrow band pass filter. Quality factor Q is a measure of selectivity, means that higher the value of Q, the more selective is the filter or narrower its bandwidth (BW). The relationship between Q, BW and center frequency f_C is given as:

$\mathbf{Q = (f_C / BW)=[f_C/(f_H - f_L).}$

For wide band pass filter, $\mathbf{f_C = \sqrt{(f_H . f_L)}}$ where, f_H and f_L are the high and low cutoff frequencies (Hz).

Important is that upper cutoff frequency f_H should always be greater than lower cutoff frequency f_L ie. $\mathbf{f_H > f_L}$

Wide Band Pass Filter:

Wide band pass filter is formed by cascading high pass and low pass filter as shown in figure 6.13(a), and (b) shows its frequency response. To obtain a ±20db/decade roll off, first order high pass filter is cascaded with first order low pass filter ie. the order of band pass filter depends on the order of the high and low pass filter.

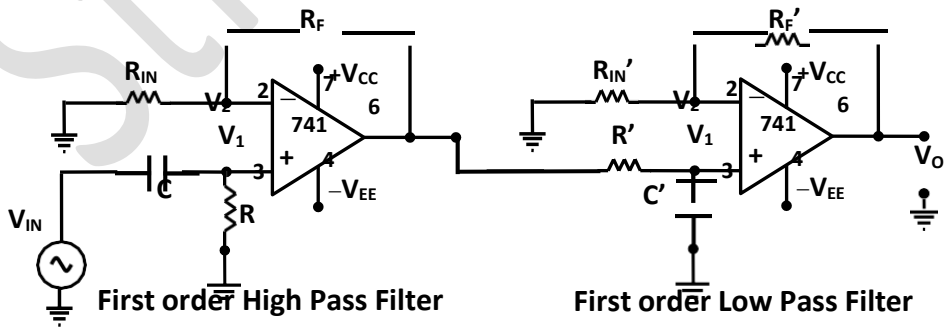


Figure 6.13(a): Wide Band Pass Filter

The voltage gain magnitude of the band filter is equal to the product of the voltage gain magnitudes of the high pass and low pass. Therefore,

$$\left|\frac{V_O}{V_{IN}}\right| = \frac{A_{FT}\,(f/f_L)}{\sqrt{[(1+(f/f_L)^2)][1+(f/f_H)^2]}}$$

Where, A_{FT} = total pass band gain

f = frequency of the input signal (Hz)

f_L = low cutoff frequency (Hz)

f_H = high cutoff frequency (Hz)

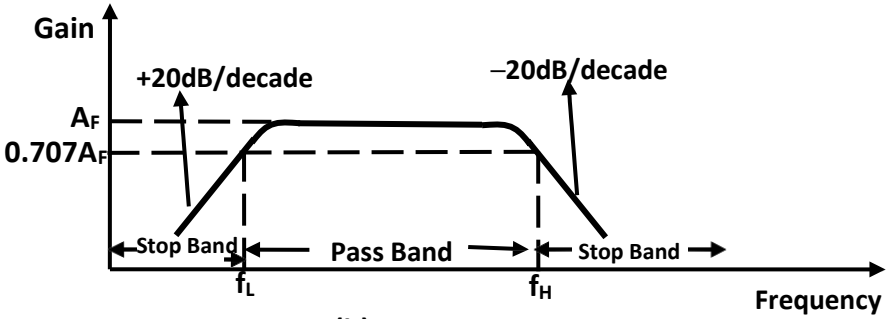


Figure 6.13(b): Frequency Response

Narrow Band Pass Filter:

Figure 6.13(a) and (b) shows the circuit diagram and frequency response of narrow band pass filter.

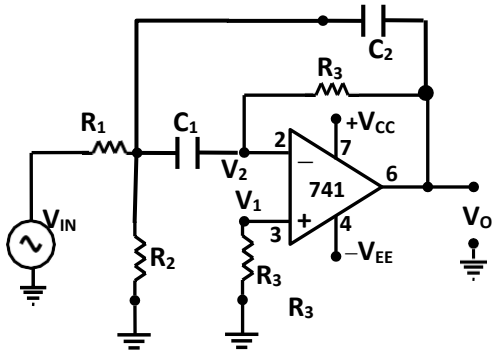


Figure 6.14(a): Narrow Band Pass Filter

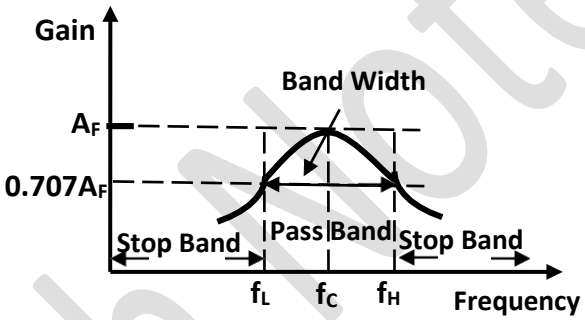


Figure 6.14(b): Frequency Response

Narrow band pass filter using multiple feedback as shown hence the name multiple feedback filter. Op-amp used is in inverting mode. This filter is designed for specific values of center frequency f_C and quality factor Q or f_C and bandwidth.

Design of narrow band pass filter:

(i) Choose $C_1 = C_2 = C$.

(ii) Determine the value of R_1, R_2 and R_3 by the following expressions:

$R_1 = Q / (2\pi.f_C.C.A_F)$; $R_2 = Q / [2\pi.f_C.C.(2Q^2 – A_F]$; and $R_3 = Q / (\pi.f_C.C)$ where Q is the quality factor, fc is the center frequency (Hz), A_F is the gain at fc , is given by : $A_F = (R_3)/(2R_1)$

(iii) Important is that, the gain must satisfy the condition: $A_F < 2Q^2$

Advantages of narrow band pass filter:

(1) Only single op-amp is used.

(2) Center frequency f_C can be changed to new frequency f_C' without changing the gain or bandwidth. This can be done by changing resistor R_2 to R_2' so that $R_2' = R_2 (fc/fc')^2$

BAND REJECT FILTERS :

In band reject filters, band of frequencies from f_H to f_L is attenuated ie. stop band whereas frequencies are passed outside this band ie. pass band. Band reject filters are also called as band stop or band elimination filters. This filters are classified as (i) Wide band reject filter (ii) Narrow band reject filter.

Wide band reject filter:

Figure 6.15(a) and (b) shows the circuit diagram and frequency response of wide band reject filter. This filter has a high pass filter, a low pass filter and a summing amplifier. Condition to realize the band reject filter response is that the low cutoff frequency f_L, of high pass filter must be larger than the high cutoff frequency f_H, of low pass filter. Also the pass band gain of high and low pass filters must be same. Center frequency $fc = \sqrt{(f_H . f_L)}$

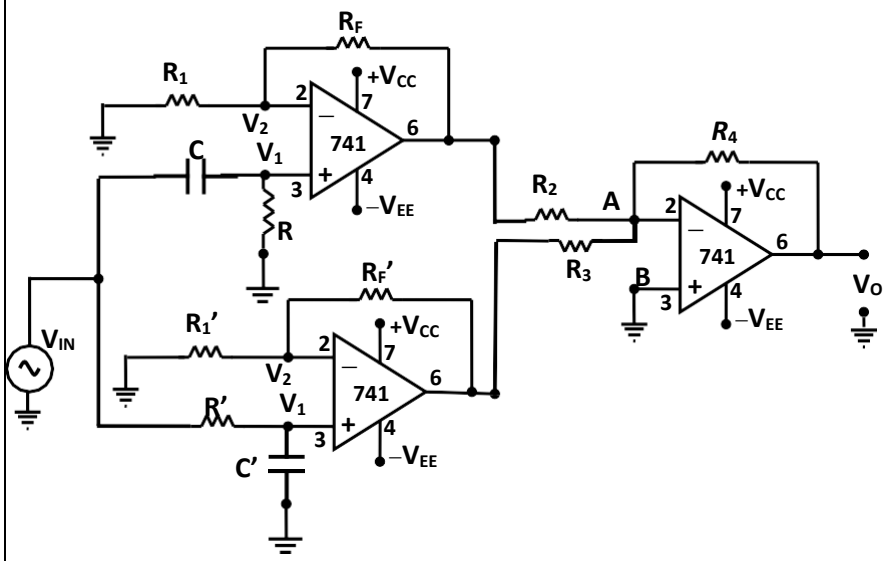


Figure 6.15(a): Wide Band Reject Filter

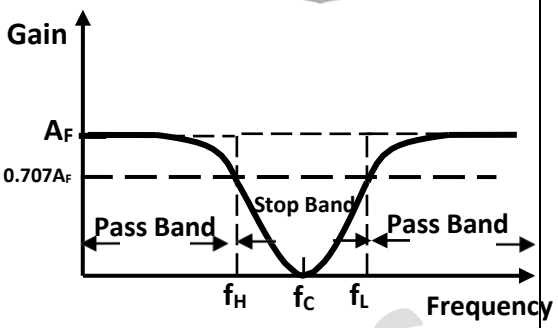


Figure 6.15(b): Frequency Response

From figure 6.15(b), the voltage gain changes at the rate of 20dB/decade above f_H and below f_L, with a maximum attenuation occurring at fc.

Narrow Band Reject Filter (Notch Filter):

For rejection of only a single frequency, the notch filter is used. Active notch filter commonly uses a twin-T network and a op-amp as voltage follower. One T network has two resistors and a capacitor while the other uses two capacitors and a resistor. The quality factor Q of T network is low and can be increased, if it is used with voltage follower as shown in figure 6.16(a) and figure 6.16(b) shows the frequency response of filter.

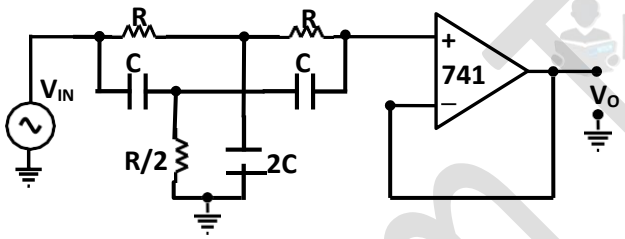


Figure 6.16(a): Narrow Band Pass Filter

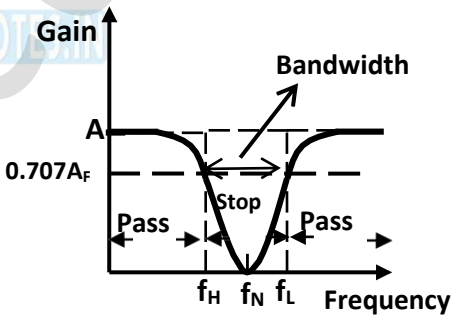


Figure 6.16(b): Frequency Response

To design a notch filter for a desired notch out frequency f_N, choose the value of capacitor C ≤ 1μF and then calculate the value of resistor using the expression: $R = 1/ (2\pi.f_N.C)$. Notch filters are used in communications and biomedical instruments to eliminate undesired frequency.

ALL PASS FILTER:

A filter which passes all frequency components of input signal without attenuation is known as all pass filter. All pass filters is also called as delay equalizers or phase correctors. Figure 6.17(a) and (b) shows the circuit diagram and input and output waveforms. In this filter, the pass band covers the entire frequency, hence has a flat amplitude response characteristics. All pass filter produces an output that is phase shifted relative to the input signal.

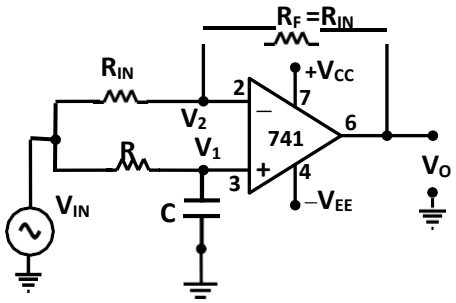


Figure 6.17(a): All Pass Filter

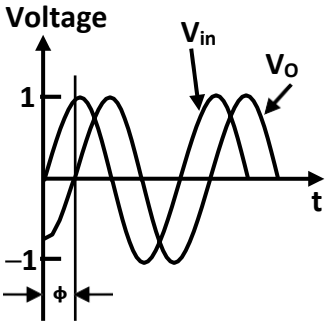


Figure 6.17(b): Input and Output Waveforms

The output voltage Vo is given by the expression- $\mathbf{Vo = [(1-j2\pi.f.R.C)/ (1+j2\pi.f.R.C)].V_{IN}}$

Where, f is the input signal frequency (Hz). From the above equation, amplitude of (Vo/V_{IN}) is unity ie. $Vo = V_{IN}$ throughout the useful frequency range and the phase shift between input and output is a function of input frequency f. From figure 6.17(b), the output signal lags the input signal by 90° ie. there is a phase shift of 90° between input and output. The circuit causes a change in phase angle ϕ from 0° to (–180°) for a frequency variation from 0 Hz to ∞.

The phase lag introduced by the circuit is given by the expression: $\mathbf{\phi = [-2.\tan^{-1}(2\pi.f.R.C)]}$ where ϕ is in degrees, f is in hertz, R in ohms and C in farads. If the position of R and C are interchanged, then the output signal leads the input signal and the phase angle introduced by the circuit is given by: $\mathbf{\phi = [2.\tan^{-1}\{1/(2\pi.f.R.C)\}]}$

IC-555 TIMER:

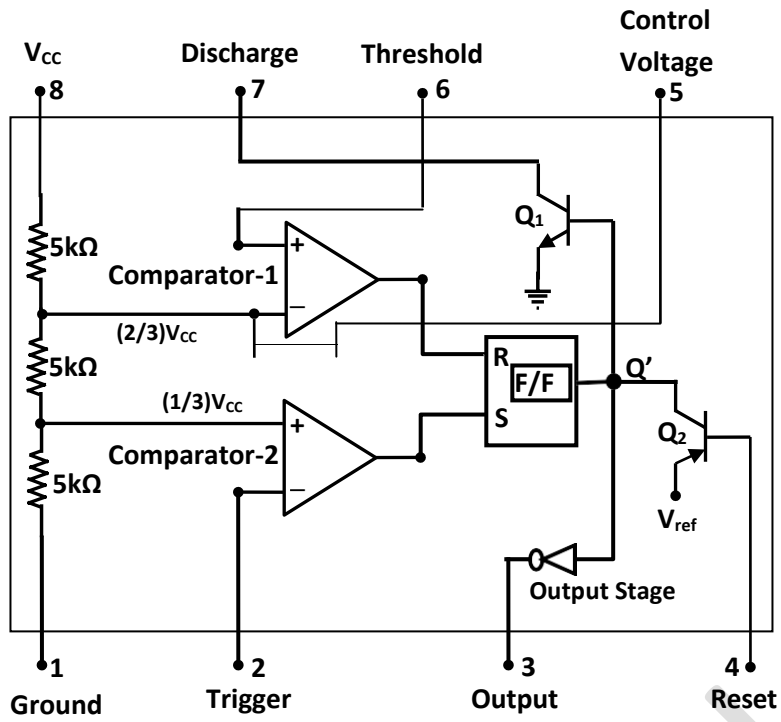


Figure 7.01: Functional block diagram of IC-555 Timer

Figure 7.01 shows the functional block diagram of IC-555 timer. It consists of a voltage divider network, which provides bias voltage of (2/3)Vcc to the inverting input of the comparator-1 and (1/3)Vcc to the non-inverting input of the comparator-2. These two voltages fix the comparator threshold voltage and also determine the timing interval. Electronically, possible to vary time by applying a modulation voltage to the control voltage input (pin-5). If no such modulation is proposed, a 0.01µF capacitor is connected between control voltage and ground to bypass noise and ripple from supply. The other two inputs to the comparator are threshold and trigger inputs. The output of these two comparators, SET or RESET the flip flop, whose Q'output is fed to base of transistor Q_1. When Q' = high, Q_1 is ON and capacitor (externally connected between pin 7 and ground) will discharge.

The output stage is basically an inverting buffer stage used to provide a low output resistance and also to invert the flip flop output. Output stage has a capability of sourcing and sinking 200mA current. Q_2 (PNP transistor) whose emitter is connected to an internal reference voltage which is less than Vcc. When V_{ref} > Vcc (Pin-4 potential is less than Vcc), Q_2 is ON, which causes Q_1 to turn ON and output at pin-3 is brought to ground level.

Applications include oscillator, pulse generator, ramp and square wave generator, voltage monitor and may more applications.

IC-555 AS MONOSTABLE MULTIVIBRATOR:

Figure 7.02 (a) shows the circuit diagram of IC-555 as monostable multivibrator and (b) shows the waveform of trigger pulse, capacitor voltage and output pulse. Since it has only one stable state (output low), hence name monostable.

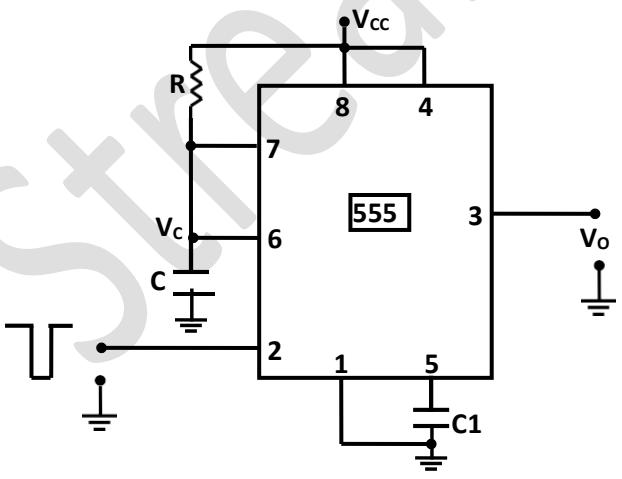


Figure 7.02(a): Monostable Multivibrator

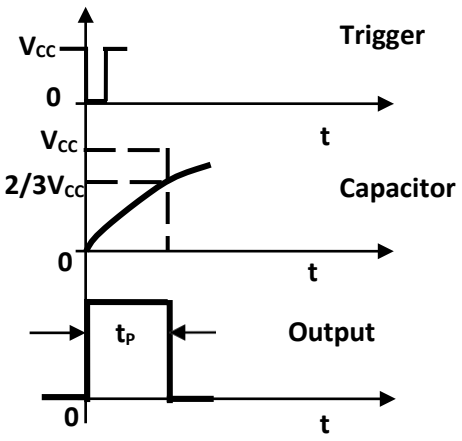


Figure 7.02(a): Waveforms

It is also called as one-shot multivibrator. From the circuit diagram, Pin-8 is connected to Vcc and pin-4 (reset pin) also connected to Vcc so that reset condition is disabled. The time interval for which the output remains high (t_P, pulse width) is decided by the external RC network. The capacitor C is connected between pin 7 and 1 so that it charges through the resistance R when the transistor Q_1 is OFF.

Operation: Initially, trigger pulse is high (Vcc), this drives the output of comparator-2 to low condition. As the capacitor C is in discharged state, pin-6 and 7 are at ground potential. The inputs to the flip flop will be S=R=0, hence Q' = high, so, Q_1 is ON, and C discharges to 0V ie. Vc = 0V. Since Q' = 1, output pin-3 = 0 is actually the stable state of multivibrator.

When the trigger input (negative trigger pulse) goes low (from Vcc to 0), comparator-2 output = high ie. S = 1. The comparator-1 output continue to be 0 ie. R=0, hence the flip flop is in set condition ie. Q' = 0, pin-3 = 1(High state). Since Q' = 0, transistor Q_1 is OFF and the capacitor C starts charging exponentially towards Vcc through the resistor R. When Vc becomes greater than ((2/3) Vcc), comparator-1 output changes form low to high ie. R = 1. Since the trigger input has returned back to Vcc from 0, comparator-2 output is equal to zero ie. S =0. So, S = 0 and R= 1, RS flip flop get RESET and Q' = 1. AS Q' = 1, transistor Q_1 = ON and capacitor C starts discharging towards zero through the transistor Q_1 and capacitor voltage Vc becomes zero. While discharging, when Vc < ((2/3) Vcc), the comparator-1 output goes to zero ie. R=0. Since the trigger input = Vcc, the comparator-2 output will be = 0 ie. S=0. Hence, S=0 and R=0, so no change in the Q' output condition and hence continuous to be High. Thus, pin-3 output = LOW (0-state).

The monostable multivibrator, thus goes from stable state into quasistable state and then returns back to the stable state after a time, $\mathbf{t_P = (1.1)R.C}$

The output remains to be in LOW state until the next trigger pulse is applied to change the state.

IC-555 AS ASTABLE MULTIVIBRATOR:

Figure 7.03 (a) shows the circuit diagram of IC-555 as astable multivibrator and (b) shows the waveform of capacitor voltage and output pulse. Since no stable state, hence name astable.

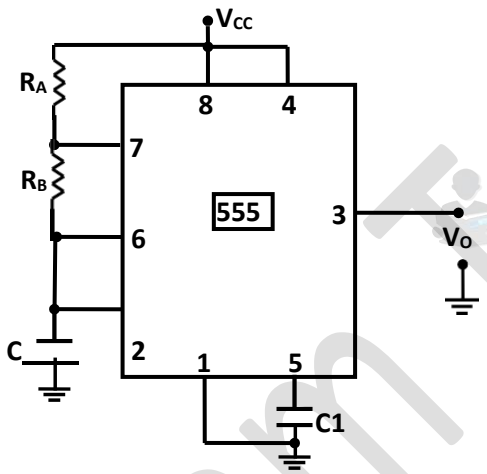


Figure 7.03(a): Astable Multivibrator

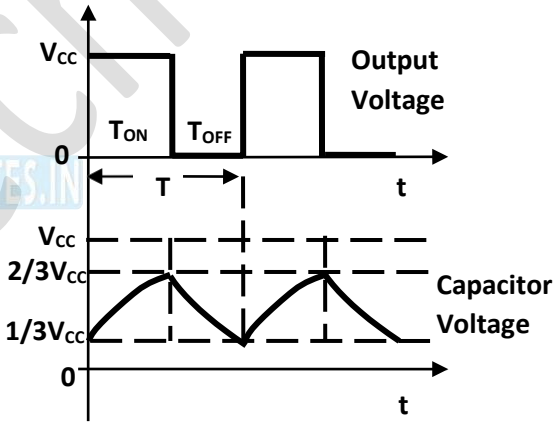


Figure 7.03(a): Waveforms

Astable multivibrator does not requires an external trigger pluse to change the output state, hence called as free-running multivibrator. The time duration for which the output will remain high or low is decided by the externally connected two resistors (R_A and R_B) and a capacitor (C).

Operation: Initially, when output is high (pin-3 = High), Flip flop output Q' = 0, hence transistor Q_1 is OFF. Now the capacitor C starts charging towards Vcc through R_A and R_B. As soon as the voltage across the capacitor Vc, becomes equal to[(2/3)Vcc], the comparator-1 output is high and will RESET the flip flop ie. Q' = 1. Hence the output = 0. As, Q' =1 , transistor Q_1 = ON and the capacitor C starts discharging through resistor R_B and transistor Q_1. During discharging mode of capacitor C, as soon as the voltage across the capacitor C becomes equal to [(1/3)Vcc], comparator-2 output will SET the flip flop, Q' = 0, and output = high. Then the cycle repeats.

Charging time duration of the capacitor C, is equal to the time the output is high is given by the expression:
$\mathbf{t_C = T_{ON} = 0.69(R_A + R_B)C}$

Discharging time duration of the capacitor C, is equal to the time the output is low is given by the expression:
$\mathbf{t_d = T_{OFF} = 0.69(R_B)C}$

Hence the total time period of output waveform: $\mathbf{T = t_C + t_d = T_{ON} + T_{OFF} = 0.69(R_A + 2R_B)C}$

Hence, the frequency of oscillation is, $\mathbf{f_O = 1/T} = \frac{1.45}{(R_A+2R_B)C}$

From the equation of frequency of oscillation fo, frequency is independent of the supply voltage Vcc.

Duty Cycle: Duty cycle is the ratio of the time during which the output is high (T_{ON}) to the total time period T.

% duty cycle = [T_{ON} / T] x 100 = $\frac{R_A+R_B}{R_A+2R_B} \times 100$

Applications: Astable multivibrator can be used to produce a square wave output. It can be used as a free running ramp generator.

OP-AMP AS SCHMITT TRIGGER:

Figure 7.05(a) shows the circuit diagram and 7.05(b) input and output waveforms of op-amp as Schmitt trigger. This circuit converts an irregular-shaped waveform to a square wave output.

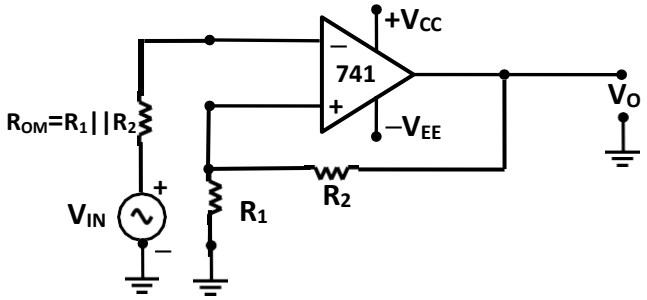


Figure 7.05(a): Op-Amp as Schmitt Trigger

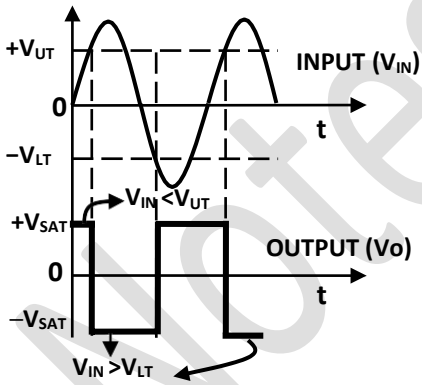


Figure 7.05(b): Waveforms

Circuit diagram shows an inverting comparator with positive feedback as a Schmitt trigger. Upper threshold voltage (V_{UT}) and lower threshold voltage (V_{LT}) are obtained by using voltage divider network R_1 and R_2. The voltage drop across R_1 is fed back to the non-inverting input. This voltage drop across R_1 is the V_{UT} and V_{LT} threshold voltages that depend on the value and polarity of output voltage Vo. The output voltage Vo, switches between positive saturation voltage ($+V_{SAT}$) and negative saturation voltage ($-V_{SAT}$), each time the input voltage exceeds the threshold voltage levels, V_{UT} and V_{LT}, as shown in figure 7.05(b). R_{OM} is the offset minimizing resistance, used to minimize offset problems.

As long as $V_{IN} < V_{UT}$, the output voltage Vo = $+V_{SAT}$. When $V_{IN} > V_{LT}$, the output voltage Vo = $-V_{SAT}$. Using the voltage divider rule, the values of V_{UT} and V_{LT} can be obtained as:

$$V_{UT} = \frac{R_1}{R_1 + R_2}[+V_{SAT}] \; and \; V_{LT} = \frac{R_1}{R_1 + R_2}[-V_{SAT}]$$

To remove the false output transitions, the threshold voltages (V_{UT} and V_{LT}) are made slightly larger than the input noise voltages. Also, the positive feedback, because of its regenerative action, switching of output voltage Vo, between positive saturation voltage ($+V_{SAT}$) and negative saturation voltage ($-V_{SAT}$) will be fast.

This inverting comparator with positive feedback exhibits hysterisis, a dead band condition ie. the output switches from $+V_{SAT}$ to $-V_{SAT}$, when the $V_{IN} > V_{UT}$ and output comes back to its original state ie. $+V_{SAT}$ when the $V_{IN} < V_{LT}$.

COMPARATOR CHARACTERISTICS:

(1) Speed of operation: As the comparator switches rapidly between $+V_{SAT}$ to $-V_{SAT}$, implies that the bandwidth is wider and hence the higher is the speed of operation.

(2) Accuracy: Comparator accuracy depends on its voltage gain, CMRR, input offsets, and thermal drifts.

(3)Compatibility of output: Comparator is aform of ADC converter, whose output swings between two logic levels suitable for logic family (TTL logic family)

LIMITATIONS OF OP-AMP AS COMPARATORS:

Generally, output of a comparator is not well matched with a particular logic family (TTL logic family). This is the limitation of comparator. Hence to matched the output, op-amps are used with external components such as zeners or diodes. Hence, the resulting circuits, in which the outputs are limited to predetermined values, are called limiters.

OP-AMP AS VOLTAGE LIMITERS:

Figure 7.06 (a) to (f) shows the circuit diagram and input/output waveforms of voltage limiters.

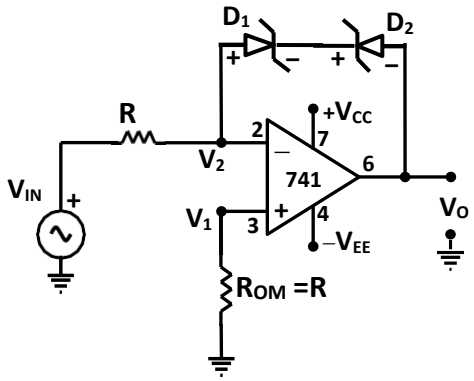


Figure 7.06(a): Op-amp as Comparator with positive and negative voltage limiting

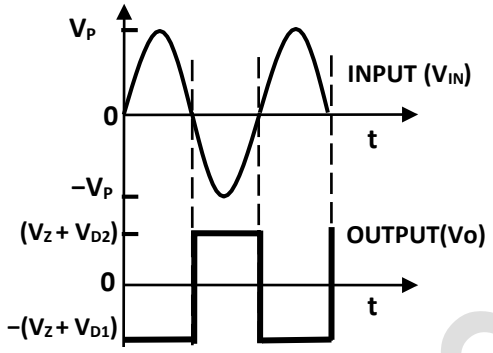


Figure 7.06(b): Input and output Waveforms

Figure 7.06 (a) shows the circuit diagram of comparator with positive and negative voltage limiting circuit and (b) shows the input and output waveforms. From figure, Point V_1 and V_2 are at virtual ground, so input voltage V_{IN}, appears across input resistor R, and output voltage Vo, across zener diodes D_1 and D_2, which are connected in the feedback path. Resistance R_{OM}, is used to minimize the offset problems.

This arrangement limits the output voltage. When the input voltage V_{IN}, crosses zero and increases in positive direction, as shown in figure 7.06(b), diode D_1 is forward biased and diode D_2 goes into avalanche conduction, the output voltage (Vo) increases in negative direction. Therefore, the maximum negative value of output voltage Vo, is equal to $-(V_Z + V_{D1})$ where V_Z is the zener voltage and V_{D1} is the voltage drop across the forward biased zener diode D_1 (= 0.7V). On the other hand, when input crosses zero and increases in the negative direction, output voltage Vo, starts increasing positively until diode D2 is forward biased and D1 goes into avalanche conduction. Thus the maximum positive voltage is equal to $+(V_Z + V_{D2})$, where V_{D2} is the voltage drop across the forward biased zener diode D_2 (= 0.7V). Thus the output voltage Vo swing is limited to $+(V_Z + V_{D2})$ and $-(V_Z + V_{D1})$.

If there is a need of output voltage to limit the swing in positive direction only, then the circuit diagram in figure 7.06(c) is used. Figure 7.06(d) shows the input and output waveforms of figure 7.06(c).

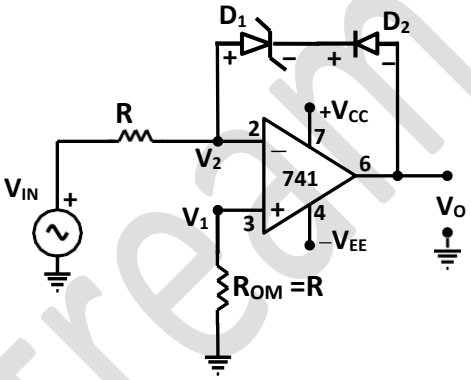


Figure 7.06(c): Op-amp as Comparator with positive voltage limiting

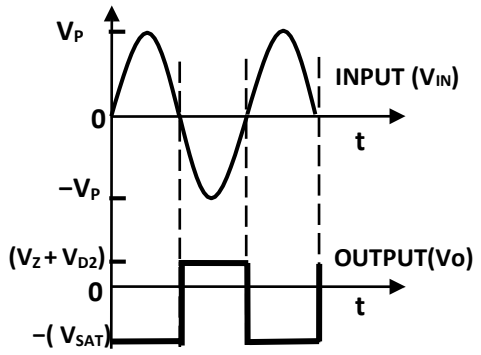


Figure 7.06(d): Input and output Waveforms

If only one zener diode is used in feedback path, as shown in figure 7.06(e), the output voltage is limited to $+V_Z$ and $-V_D$, as shown in figure 7.06(f). If the direction of diode D in the feedback path is changed in figure 7.06(e), then exact opposite result can be obtained ie. output voltage Vo, is limited to $-V_Z$ and $+V_D$, where V_Z is the zener voltage and V_D is the voltage drop across the forward biased zener diode.

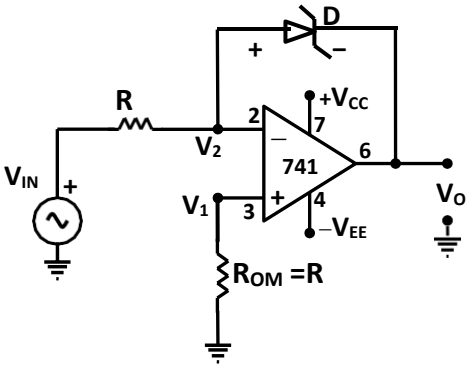


Figure 7.06(e): Op-amp as Comparator with positive and negative voltage limiting

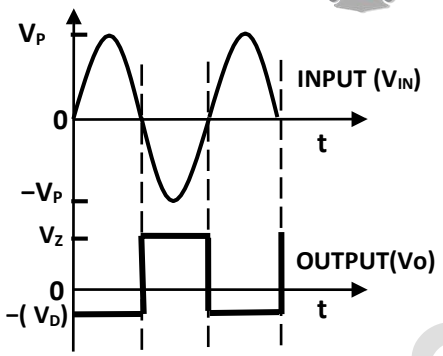


Figure 7.06(f): Input and output Waveforms

Voltage limiters are commonly used in communication devices such as Television and frequency modulation receivers.

OP-AMP AS CLIPPERS AND CLAMPERS:

CLIPPERS:

The circuits which are used to clip off the unwanted portions of the input voltage above or below certain levels to produce output are called as clipping circuits.

POSITIVE CLIPPER CIRCUIT:

Figure 7.07(a) shows the circuit diagram of positive clipper using op-amp with a rectifier diode and figure 7.07(b) shows the input and output waveforms.

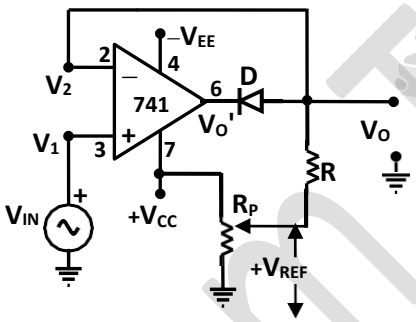


Figure 7.07(a): Positive Clipper Circuit

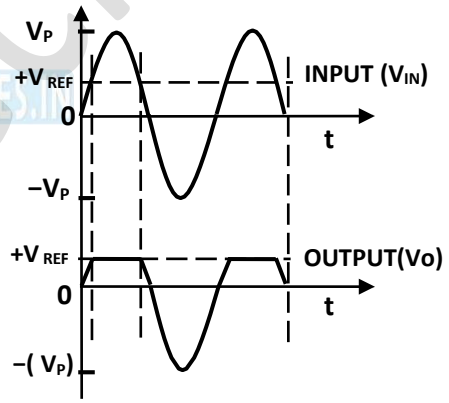


Figure 7.07(b): Input and output Waveforms

Here the op-amp is basically used as a voltage follower with a diode D in the feedback path. Clipping level is determined by reference voltage $+V_{REF}$. The $+V_{REF}$ should always be less than the input voltage range of op-amp. Resistance R_P is used as a potentiometer (variable resistor) to vary the reference voltage. Diode D is assumed as an ideal diode.

Operation: During positive half cycle of input voltage, when $V_{IN} \le V_{REF}$, the V_{REF} voltage at inverting input terminal is higher than the input voltage V_{IN} applied at the non-inverting terminal of op-amp. Hence, op-amp output V_O'(pin 6), is sufficiently negative to turn ON diode D, so, the output Vo, follows the input V_{IN}, because the op-amp is used as a voltage follower. when $V_{IN} > V_{REF}$, the V_{REF} voltage at inverting input terminal is lower than the input voltage V_{IN} applied at the non-inverting terminal of op-amp. Hence, op-amp output V_O'(pin 6), is sufficiently positive to turn OFF diode D, the op-amp operates open-loop; therefore it further drives its output voltage V_O'(pin 6) towards positive saturation ($+V_{CC}$). Thus, when $V_{IN} > V_{REF}$, $V_O' = +Vcc$ and $Vo = +V_{REF}$.

During negative half cycle, $V_{IN} \le V_{REF}$, the output of op-amp V_O'(pin 6), is sufficiently negative to turn ON diode D, so, the output Vo, follows the input V_{IN}. Thus from the output waveform, it is seen that the output portion of the positive half cycle above reference voltage is clipped off, hence it is called as positive clipper circuit.

The op-amp alternates between closed loop and open loop as the diode D is ON and OFF respectively, so the op-amp must be a high speed and preferably compensated for unity gain. HA2500, LM310 and µA318 are examples of high speed op-amps.

NEGATIVE CLIPPER CIRCUIT:

If POT R_P of figure 7.07(a) is connected to negative power supply $-V_{EE}$, then the reference voltage V_{REF} becomes negative. This will cause the entire output waveform, above $-V_{REF}$, to be clipped off. The output follows the input only when $V_{in} < -V_{REF}$. By changing the position of diode D and the polarity of reference voltage V_{REF}, the positive clipper can be converted into negative clipper.

SMALL SIGNAL HALF-WAVE RECTIFIERS (POSITIVE):

Figure 7.08(a) shows the circuit diagram of a positive small signal half wave rectifier with zero reference voltage and figure 7.08(a) shows the input and output waveforms.

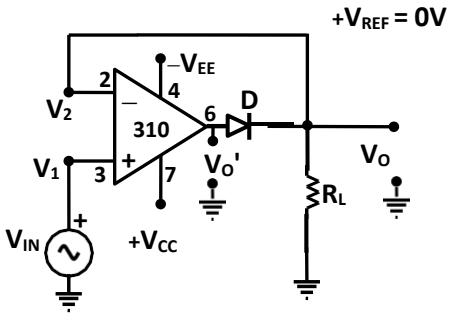


Figure 7.08(a): Positive Small Signal Half Wave Rectifier

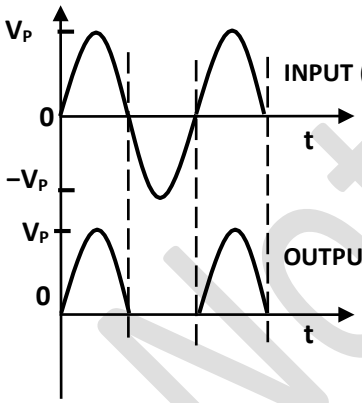


Figure 7.08(b): Input and output Waveforms

This circuit can rectify the signal of peak values of few millivolts. This is possible because the high open loop gain of op-amp automatically adjusts the voltage drive to the diode D so that rectified output peak is the same as the input. Diode D acts as an ideal diode.

Operation: When input voltage V_{IN} increases in positive direction, output of op-amp V_O', also increases in positive direction and diode D is forward biased and act as closed switch, and closes a feedback loop. Hence the op-amp act as a voltage follower, and output voltage Vo, is same as input voltage, as shown in figure 7.08(b).

When input voltage V_{IN} increases in negative direction, output of op-amp V_O', also increases in negative direction and diode D is reverse biased and act as an open switch, and opens a feedback loop. Hence output voltage Vo, is zero volt, and output does not follow the input as shown in figure 7.08(b).

Here the op-amp should be high speed op-amp, since it alternates between closed and open loop operations. Examples of high speed op-amps are HA2500, LM310 and µA318.

SMALL SIGNAL HALF-WAVE RECTIFIERS (NEGATIVE):

This small signal positive half wave rectifier can be converted into negative small-signal half wave rectifier by reversing diode D.

NEGATIVE HALF-WAVE RECTIFIER:

Figure 7.09(a) shows the circuit diagram of a negative half wave rectifier with zero reference voltage and figure 7.09(a) shows the input and output waveforms.

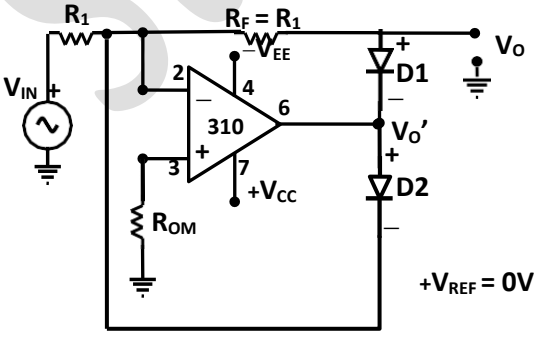


Figure 7.09(a): Negative Half Wave Rectifier

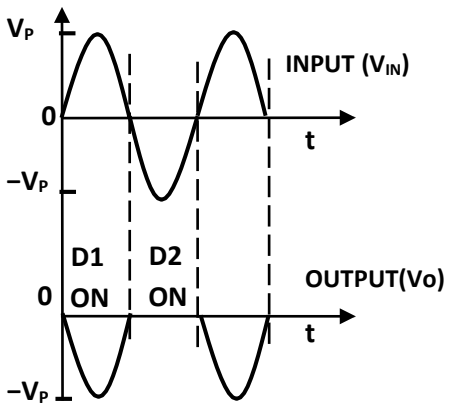


Figure 7.09(b): Input and output Waveforms

In this circuit, op-amp is used in inverting configuration. The two diodes D1 and D2 are used in such a way that the output Vo' does not saturate which in turn minimizes the response time increases the operating frequency of op-amp. The output voltage Vo is measured at the anode of D1.

Operation: During positive half cycle of input voltage V_{IN}, output Vo' is negative, hence diode D1 is forward biased and closes the feedback loop through R_F. Since $R_1 = R_F$, $Vo = V_{IN}$. During negative half cycle of input voltage V_{IN}, output Vo' is positive, hence diode D2 is forward biased and prevents the op-amp from going into positive saturation. Since diode D1 is OFF, Vo = 0V.

In order to obtained positive half-wave rectified outputs, diodes D1 and D2 must be reverse biased.

POSITIVE AND NEGATIVE CLAMPERS:

The circuit in which the output signal is clamped to a predetermined DC level (Positive or Negative), without changing the shape and amplitude of the input signal is called clamper. Clamper is also called as DC inserter or restorer. Condition to keep the output waveform undistorted is that the (RC) time constant should be very large compared to the time period of the input waveform.

Figure 7.10(a) shows the circuit diagram of peak clamper and figure 7.10(b) shows the input and output waveforms with $+V_{REF}$.

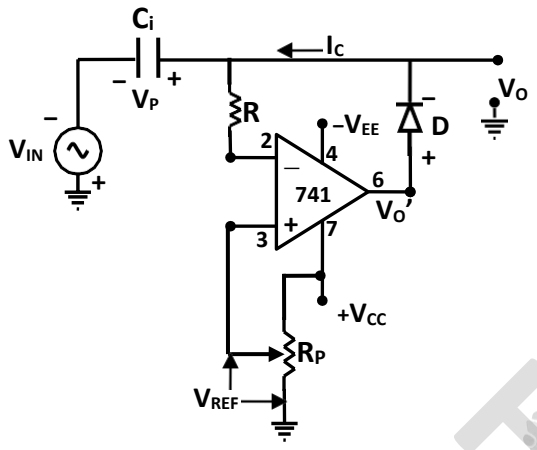


Figure 7.10(a): Op-amp as peak clamper

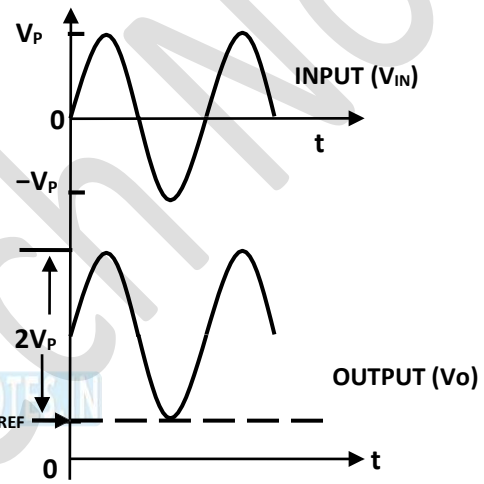


Figure 7.10(b): Input and output Waveforms with $+V_{REF}$

Figure 7.10(c) shows the input and output waveforms with $-V_{REF}$.

Figure 7.10(a) consists of a variable positive DC level. Output Vo, is the net result of AC and DC, applied to inverting terminal and non-inverting terminal of op-amp.

Circuit Operation: Diode D is assumed as an ideal diode. To understand the operation, we will consider each input separately. Considering V_{REF} input first, connected to non-inverting terminal of op-amp. Since reference voltage V_{REF} is positive, output at pin 6 (Vo') is also positive, which forward bias the diode D. Thus diode act as a closed switch, and closes the feedback loop and op-amp operates as a voltage follower. This is possible because capacitor C_i is an open circuit for DC voltage. Therefore, $Vo = +V_{REF}$.

Now considering AC input voltage VIN, which is connected to inverting terminal of op-amp.

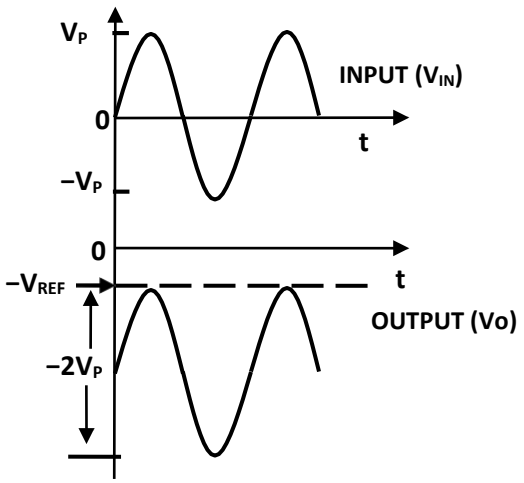


Figure 7.10(C): Input and output Waveforms with $-V_{REF}$

During negative half cycle of input voltage V_{IN}, diode D conducts and capacitor starts charging to the negative peak value of V_P. During positive half cycle, diode D is reverse biased, hence V_P across capacitor will remain same. Since the positive half cycle V_P, is in series with the capacitor voltage V_P, hence the output voltage $V_O = 2V_P$. Thus the net output is V_{REF} plus $2V_P$, so the negative peak of $2V_P$ is at V_{REF} as shown in figure 7.10(b). For precision clamping, $C_i.R_d << T/2$ where R_d is the resistance of diode D when forward biased (100Ω typically) and T = time period of the

input waveform. Resistor R is used to protect the op-amp from excessive discharge current from capacitor Ci, when DC supply voltages are switched OFF. A positive peak clamped to negative reference level clamper circuit is made by reversing the diode D and using negative reference voltage. Its input and output waveform is shown in figure 7.10(c).

Clipping and clamping are used in wave shaping circuits. These circuits are used in digital computers and communications such as TV and FM receivers.

ABSOLUTE VALUE OUTPUT CIRCUIT:

Figure 7.11 (a) shows the circuit diagram of absolute value output circuit, figure 7.11 (b) shows the circuit diagram of absolute value output circuit during positive half cycle, figure 7.11 (c) shows the circuit diagram of absolute value output circuit during negative half cycle, and figure 7.11 (d) shows the input and output waveforms.

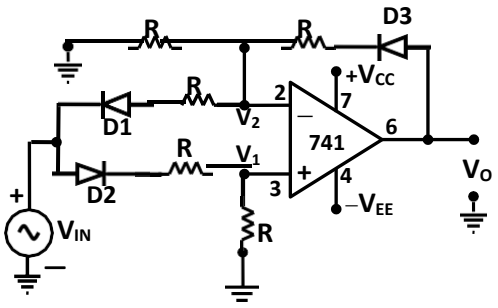


Figure 7.11(a): Absolute value output circuit

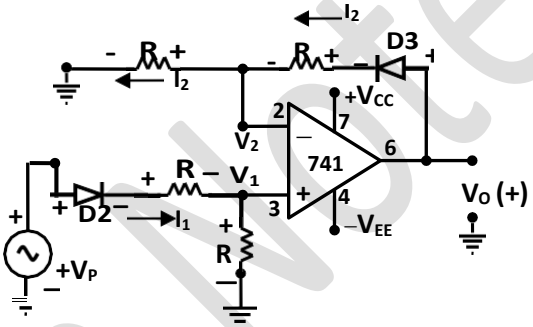


Figure 7.11(b): Absolute value output circuit during positive half cycle

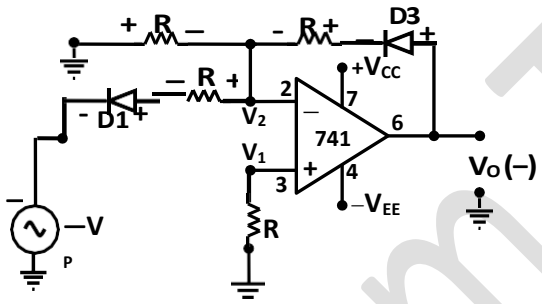


Figure 7.11(c): Absolute value output circuit during negative half cycle

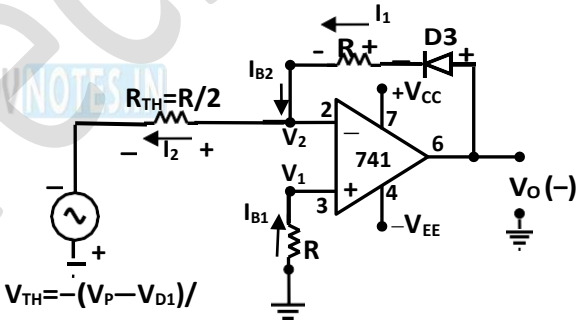


Figure 7.11(c): Thevenin's Equivalent

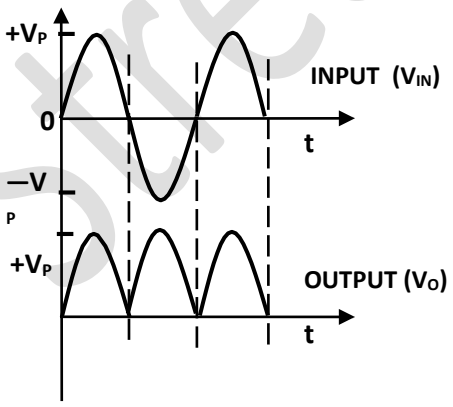


Figure 7.11(d): Input and output Waveforms

Circuit Operation: During positive half cycle of input voltage (V_P), diode D2 is forward biased and D1 is reverse biased. Hence the Diode D2 is connected in the circuit as shown in figure 7.11 (b). Thus the voltage at node V_1 (+ input of op-amp) is:

$$V_1 = \frac{V_P - V_{D2}}{2}$$

Where, V_{D2} is the voltage drop across diode D2 = 0.7V

Similarly, the voltage at node V_2 (− input of op-amp) is:

$$V_2 = \frac{V_{O(+)} - V_{D3}}{2}$$

Where, $V_O(+)$ is the output voltage during positive half cycle and V_{D3} is the voltage drop across diode D3 = 0.7V

Since, difference input voltage, $V_{id} \approx 0V$, so $V_1 = V_2$.

Therefore,

$$\frac{V_P - V_{D2}}{2} = \frac{V_{O(+)} - V_{D3}}{2}$$

Hence, we get the output voltage, $\mathbf{V_O(+) = V_P}$ (ie. the output voltage is equal to the peak of positive half cycle of the input as shown in figure 7.11(d)).

During negative half cycle of input voltage ($-V_P$), diode D1 is forward biased and D2 is reverse biased. Hence the Diode D1 is connected in the circuit as shown in figure 7.11 (c). This circuit is further simplified by applying thevenin's theorem to the left of the (−) input of op-amp. Hence, its Thevenin's equivalent voltage and resistance are:

$$V_{TH} = -\left(\frac{V_P - V_{D1}}{2}\right) \quad \text{and} \quad R_{TH} \cong \frac{R}{2}$$

Where, V_{D1} is the voltage drop across diode D1 , V_{TH} and R_{TH} are Thevenin's equivalent voltage and resistance.

Now, applying Kirchoff's current law at node V_2, we get:

$$\mathbf{I_1 = I_2 + I_{B2};} \qquad \mathbf{Since,\ I_{B2} \approx 0A;} \qquad \mathbf{Hence,\ I_1 = I_2}$$

Where, I_1 and I_2 are the currents flowing through resistor R and R_{TH} and I_{B2} is the bias current that flows into the inverting terminal of op-amp as shown in the figure 7.11(c).

Since,

$$I_1 = \frac{[V_O(-) - V_{D3}] - V_2}{R} \quad \text{and} \quad I_2 = \frac{V_2 - (V_{TH})}{R/2}$$

Hence, on equating currents, I_1 and I_2, we get,

$$\frac{[V_O(-) - V_{D3}] - V_2}{R} = \frac{V_2 - (V_{TH})}{R/2}$$

Since, Voltage at Node V_1 = 0V, so, V_2 is also zero, due to virtual ground concept. Therefore, substituting the node voltage V_2 = 0V and also V_{TH} in the above equation, we get:

$$\mathbf{V_O\,(-) - V_{D3} = V_P - V_{D1}}$$

Hence, **the output voltage, V_O (−) = V_P,** where, $V_{D1} = V_{D3} = 0.7V$ (ie. the output voltage is equal to the peak of negative half cycle of the input as shown in figure 7.11(d)).

Hence, from the output equations of **V_O (−) and V_O (+),** it is concluded that the regardless of the polarity of the input signal, the output is always positive going; hence the name given absolute value output circuit.

Note that the gain of the circuit is 1, therefore the positive peak amplitudes are the same as the input peak amplitudes. Diode D3 compensates for the voltage drop across diodes D1 or D2.

This circuit is used in wave shaping circuits.

PEAK DETECTOR:

Peak detector is a circuit which is used to measure the peak value of any non sinusoidal waveforms. Figure 7.12(a) shows the circuit diagram of peak detector (positive) and 7.12(b) shows the input and output waveforms.

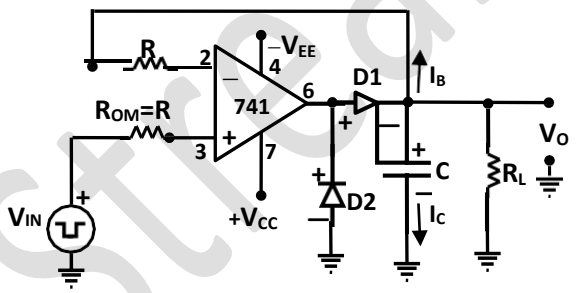


Figure 7.12(a): Peak Detector Circuit

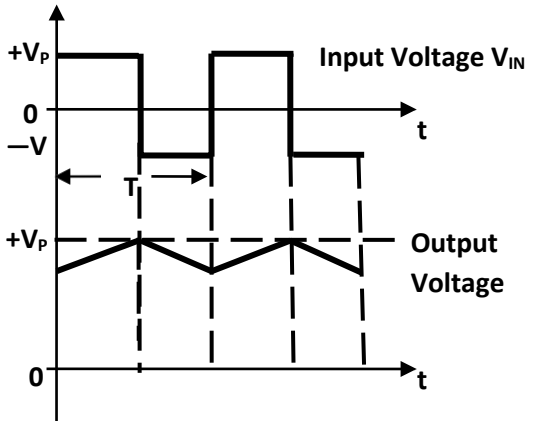


Figure 7.12(b): Input and Output Waveforms

Operation: During the application positive half cycle of input voltage V_{IN}, diode D1 is forward biased and D2 is reverse biased. Due to diode D1 forward biased, the op-amp operates as a voltage follower. As diode D1 is forward biased, capacitor C starts charging towards positive peak $+V_P$ of input voltage as the polarity shown in figure 7.12(a).

During the application of negative half cycle, diode D1 is reverse biased, and voltage across capacitor C remains unchanged. The only discharge path for C is through load resistor R_L. For proper operation of the circuit the charging time constant ($C.R_d$) and discharging time constant ($C.R_L$) must satisfy the following conditions:

(i)(C. R_d) ≤ (T/10); where R_d is the resistance of forward biased diode (100Ω typically) and T is the time period of input waveform.

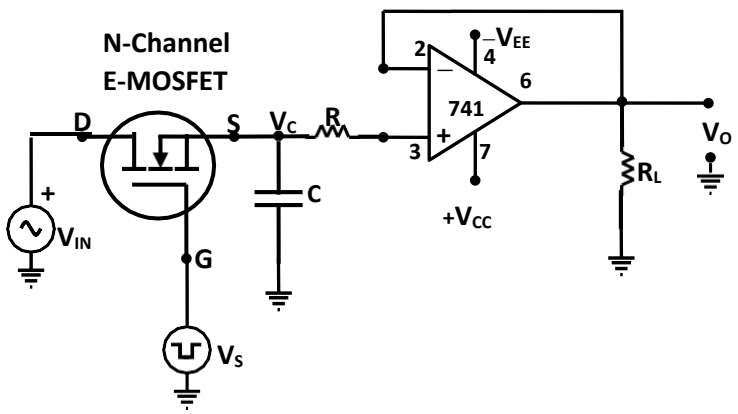
(ii) (C.R_L) ≥ (10T); where R_L is the load resistor.

A high speed, precision type op-amp such as µA741 is used. The resistor R is used to protect the op-amp against the excessive discharge currents, especially when the power supply is switched off. The resistor R_{OM} = R minimizes the offsets problems. Diode D2 conducts during negative half cycle of V_{IN} voltage to prevent the op-amp from going into negative saturation, which in turn reduces the reverse recovery time of op-amp.

Negative peak detector can be detected by reversing diodes D1 and D2 of figure 7.12(a)

SAMPLE AND HOLD CIRCUIT:

Figure 7.13(a) shows the circuit diagram of sample and hold circuit and figure 7.13 (b) shows the input and output waveforms.



V_{IN} : Input signal to be sampled

V_S : Sample and Hold Control Voltage

V_C : Voltage across capacitor

G : Gate; D : Drain and S : Source

Figure 7.13(a): Sample and Hold Circuit

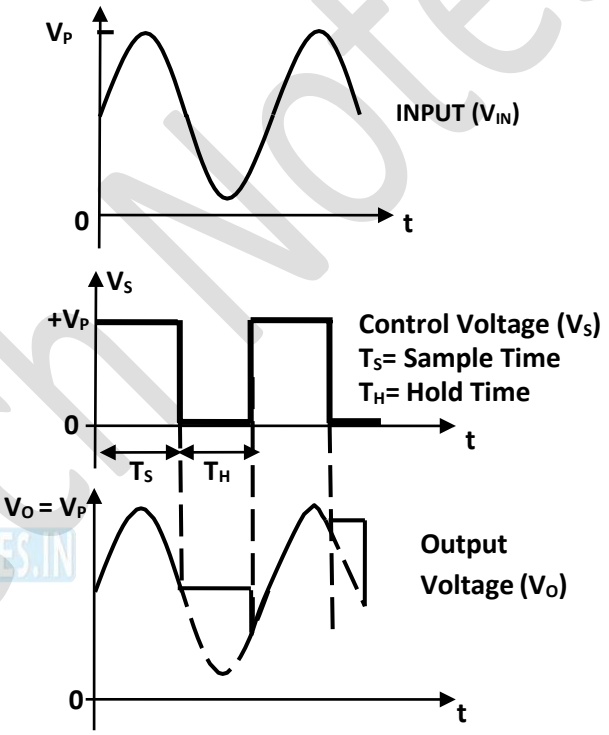


Figure 7.13(b): Input and output Waveforms

Sample and hold circuit is the circuit which samples the applied input signal and holds on to its last sampled value until the input is sampled again. From the circuit, enhancement MOSFET (E-MOSFET) works as a switch ie. when gate (G) terminal is positive E-MOSFET conducts (ON) and when zero, E-MOSFET is OFF. This ON and OFF of E-MOSFET is controlled by sample and hold control voltage (V_S). The analog input signal (V_{IN}) to be sampled is connected to drain (D) terminal and source (S) terminal is connected to capacitor C, where capacitor C, acts as a storage element. Here op-amp acts as a voltage follower.

Operation: When control voltage V_S, is positive, E-MOSFET is ON, and capacitor starts charging towards input voltage V_{IN}. This input voltage V_{IN}, appears across capacitor C and in turn at the output of op-amp V_O, as shown in figure 7.13(b). This is the sample period time.

When control voltage V_S, is zero, E-MOSFET is OFF, and act as a open switch. The only discharge path for capacitor C is through op-amp. However the input resistance of op-amp as voltage follower is very high; hence the voltage across capacitor V_C, is retained. This is the hold period time. The output of op-amp is observed during hold periods.

Note that, for obtaining the close approximation of the input waveform, the frequency of control voltage V_S must be higher than that of the input signal V_{IN}. Also precise and high speed op-amp is used. Choose a low-leakage capacitor such as Teflon or polyethylene.

Sample Periods: The time periods **T_S** of the control voltage V_S, during which the voltage across the capacitor is equal to the input voltage V_{IN} are called sample periods.

Hold Periods: The time periods **T_H** of the control voltage V_S, during which the voltage across the capacitor is constant are called sample periods.

The sample and hold circuit is commonly used in digital interfacing and communications such as analog-to-digital and pulse modulation systems.

VOLTAGE TO CURRENT CONVERTER WITH GROUNDED LOAD:

Figure 7.14 shows the circuit diagram of an op-amp voltage to current converter operating with a grounded load.

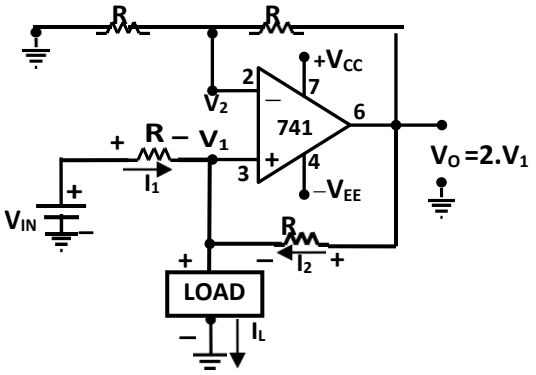


Figure 7.14: Voltage to current converter with grounded load

The input voltage source is connected to the non-inverting terminal of the op-amp; hence it does not get loaded due to the very high input resistance of the circuit. The circuit is capable of converting an input voltage into its equivalent load current that flows through a load in which one end is grounded as shown in figure. It can be shown mathematically that the load current I_L is directly proportional to the input voltage V_{IN}. The circuit analysis is carried out by determining the voltage V_1 that appears at the non-inverting input (pin-3). We then establish a relationship V_1 and load current I_L.

Applying Kirchhoff's current equation at node V_1,

$$\mathbf{I_1 + I_2 = I_L} \quad \text{.....(6.1)}$$

Since, $I_1 = \frac{V_{IN}-V_1}{R}$ and $I_2 = \frac{V_O-V_1}{R}$

Substituting, I_1 and I_2 in equation no. 6.1, we get,

$\frac{V_{IN}-V_1}{R} + \frac{V_O-V_1}{R} = I_L$; On solving, we get, $V_1 = \frac{V_{IN}+V_O-R.I_L}{2}$ .....(6. 2)

Since the gain of the circuit connected in non-inverting amplifier is given as (1+R/R) = 2. Hence the output voltage

$$\mathbf{V_O = 2.V_1} \quad \text{.....(6.3)}$$

On substituting equation 6.2 in equation 6.3, we get,

$\mathbf{V_O = V_{IN} + V_O – R.I_L}$; **OR** $\mathbf{V_{IN} = R.I_L}$; **OR** $\mathbf{I_L = V_{IN} / R}$ ..... **(6.4)**

ie. $\mathbf{I_L \alpha V_{IN}}$; this relationship shows that the load current I_L is directly proportional to the input voltage V_{IN}.

The load current I_L depends on the input voltage V_{IN} and the resistance R. In this circuit it is very important that all resistors must have equal values for satisfactory operation.

Voltage to current converter circuits is used to test Zener diodes and LEDs. They are also used for low voltage Voltmeters. The load size ≤ R value will give satisfactorily performance of the circuit.

VOLTAGE TO CURRENT CONVERTER WITH FLOATING LOAD:

Figure 7.15 shows the circuit diagram of an op-amp voltage to current converter operating with a floating load ie. the load terminals are not connected to ground.

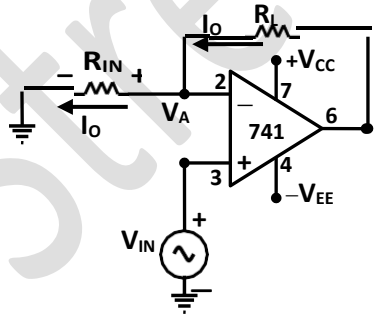


Figure 7.15: Voltage to current converter with floating load

The input voltage source is connected to the non-inverting terminal of the op-amp; hence it does not get loaded due to the very high input resistance of the circuit. The voltage drop across resistance R_{IN} is equal to ($I_O.R_{IN}$) where I_O is the output current. (V_A) is the input at the inverting input terminal. The circuit is capable of converting an input voltage into its equivalent load current that flows through the floating load as shown in figure 7.15. This circuit is also called as current series negative feedback amplifier because the feedback voltage across resistor R_{IN} depends upon output current I_O and is in series with input difference voltage V_{id}.

Applying Kirchhoff's voltage law to the input circuit, we get, $\mathbf{V_{IN} = V_A}$

But $\mathbf{V_A = (I_O . R_{IN})}$; but $\mathbf{V_A = V_{IN}}$; therefore $\mathbf{V_{IN} = (I_O . R_{IN})}$; or $\mathbf{I_O = [V_{IN} / R_{IN}]}$ **ie.** $\mathbf{I_O \alpha V_{IN}}$. The relationship of the output current I_O and the input voltage V_{IN} clearly shows that the output current I_O is directly proportional to the input voltage V_{IN}. For satisfactory operation of the circuit, the resistor R_{IN} must be a precision resistor. Voltage to

current converters with floating loads is used for testing Zener diodes, LEDs, for matching diodes and also in low range (AC and DC) voltmeters.

CURRENT TO VOLTAGE CONVERTER:

Figure 7.16 shows the circuit diagram of current to voltage converter in which the input current is directly proportional to output voltage. Basically the circuit is an op-amp inverting amplifier.

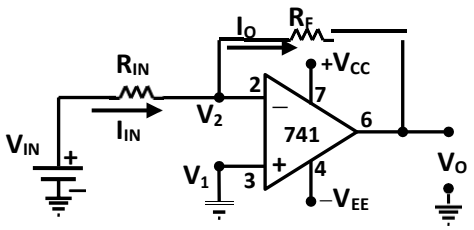


Figure 7.16: Current to voltage converter

Input voltage source V_{IN} in series with input resistor R_{IN} is connected to inverting terminal of op-amp. This series combination will form a constant current source of magnitude I_{IN}.

The voltage gain of inverting amplifier is given by:

$(V_O / V_{IN}) = -(R_F / R_{IN})$; ie. $V_O = \frac{-R_F}{R_{IN}} . V_{IN}$ 0 V $_O = \frac{-V_{IN}}{R_{IN}} . R_F$

Since, $I_{IN} = (V_{IN} / R_{IN})$.

Hence, $V_O = -[(I_{IN}).R_F]$ ie. $V_O \alpha (I_{IN})$.

From the above relationship it is clear that the output voltage V_O is directly proportional to the input current I_{IN} which means that the circuit is capable of converting an input current into a proportional output voltage. The lower limit on current measurement is set by the bias current I_B of an op-amp, this means that op-amps with smaller I_B values such as µA714 which has an I_B = 3 nA can be used to detect lower currents.

Current to voltage converters are used to sense currents from photo detectors and are also used in digital to analog converters.

PRECISION FULL WAVE RECTIFIER : [ABSOLUTE VALUE OUTPUT CIRCUIT]

Refer to figure 7.11 for circuit diagram and operation.

PRECISION HALF WAVE RECTIFIER : [SMALL SIGNAL HALF-WAVE RECTIFIERS]

Refer to figure 7.08 for circuit diagram and operation.

VOLTAGE REGULATORS: A voltage regulator is a circuit that provides a constant voltage regardless of any changes in the load currents. Performance parameters of voltage regulators are:

Line regulation or input regulation: The change in output voltage for a change in input voltage. Expressed in millivolts.

Load regulation: The change in output voltage for a change in load current. Expressed in millivolts.

Temperature stability or average temperature coefficient of output voltage: The change in output voltage per unit change in temperature. Expressed in either millivolts/°C or parts per million (ppm)/°C.

Ripple rejection: It is the measure of the regulator's ability to reject ripple voltages. Expressed in decibels.

The smaller the values of line regulation, load regulation, and temperature stability, the better the regulator.

IC voltage regulators are multipurpose and have features as programmable output, current/voltage boosting, internal short-circuit current limiting, thermal shutdown and floating operations for high-voltage applications.

Types of IC voltage regulators are:

(1) Fixed output voltage regulators: Positive and negative output voltage

(2) Adjustable output voltage regulators: Positive or negative output voltage

(3) Switching regulators

(4) Special regulators

SERIES VOLTAGE REGULATOR USING OP-AMP:

Figure 8.01 shows the circuit diagram of series voltage regulator using op-amp.

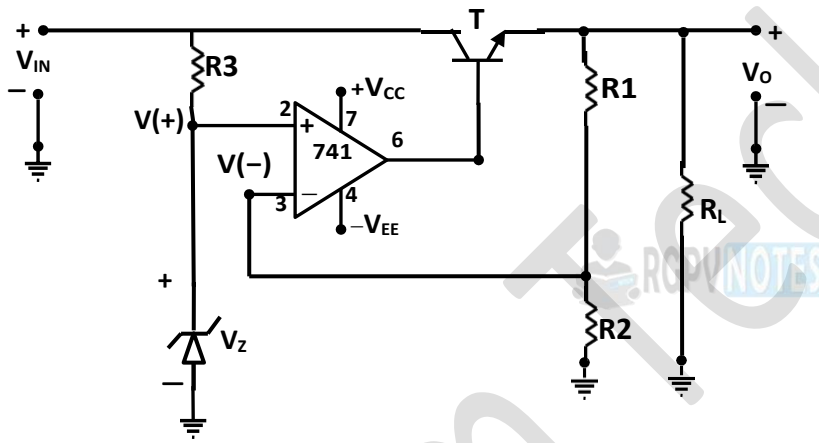


Figure 8.01: Series voltage regulator using op-amp

The op-amp is used as a comparator. It compares the part of the output voltage Vo obtained from potential divider circuit as a feedback with the reference voltage generated by the zener diode Vz.

The output of the op-amp drives the series pass transistor T.

If there is any change in output voltage the control signal from op-amp control the conduction of the transistor T. Thus the output voltage is maintained at a constant level.

From virtual ground concept

V (−) = V(+)

V (−) = V(+)= [Vo/(R1+R2)] R2

The voltage at non-inverting terminal V+ is nothing but the zener voltage Vz as shown in figure 8.01.

V(+) = Vz

The output voltage can be expressed as: Vo = [(R1+R2)/R2] V(+); Vo=[(R1+R2)/R2] Vz

Hence, **Vo=[1+R1/R2] Vz**

FIXED VOLTAGE REGULATORS:

Positive fixed voltage regulator: 78XX series is a positive voltage regulator ICs. It is 3-terminal IC. First terminal is input , second terminal is ground and third terminal is output, as shown in figure 8.02.

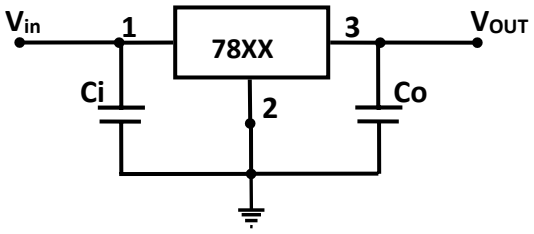


Figure 8.02: Positive voltage regulator IC

These ICs are fixed voltage regulators and can deliver output current of 1Amp. These ICs has internal thermal over load protection and short-circuit protection. Capacitor Ci, is required if the regulator is located at considerable distance from a power supply filter. Capacitor Co, is used to improve the transient response of the regulator. Ground pin no.2, should be common for both input and output pins, for proper operation. The dropout voltage, (V_{in} − V_{OUT}), must be typically 2.0V even during the low point on the input ripple voltage.

Table 1.1 shows the 7800 series voltage regulators with seven voltage options:

Device type	Output Voltage (Vo)	Maximum Input Voltage (Vin)
7805	5.0	35
7806	6.0	35
7808	8.0	35
7812	12.0	35
7815	15.0	35
7818	18.0	35
7824	24.0	40

TABLE 1.1

Negative fixed voltage regulator: 79XX series is a negative voltage regulator ICs. It is 3-terminal IC as ground, input and output.

Table 1.2 shows the 7800 series voltage regulators with seven voltage options:

Device type	Output Voltage (Vo)	Maximum Input Voltage (Vin)
7902	−2.0	−35
7905	−5.0	−35
7905.2	−5.2	−35
7906	−6.0	−35
7908	−8.0	−35
7912	−12.0	−35
7915	−15.0	−35
7918	−18.0	−35
7924	−24.0	−40

TABLE 1.2

ADJUSTABLE VOLTAGE REGULATORS:

A single IC which satisfies the voltage requirement from 1.2V to 57 V, is adjustable voltage regulator. LM317 series is the most commonly used adjustable voltage regulators.

Advantages of adjustable over fixed voltage regulators:

1) Improved system performance by having line and load regulation of a factor of 10 or better.
2) Improved overload protection allows greater output current over operating temperature range.
3) Improved system reliability with each device being subjected to 100% thermal limit burn-in.

Adjustable positive voltage regulators:

Figure 8.03 shows the typical connection diagram of LM317 series adjustable 3-terminal positive voltage regulator.

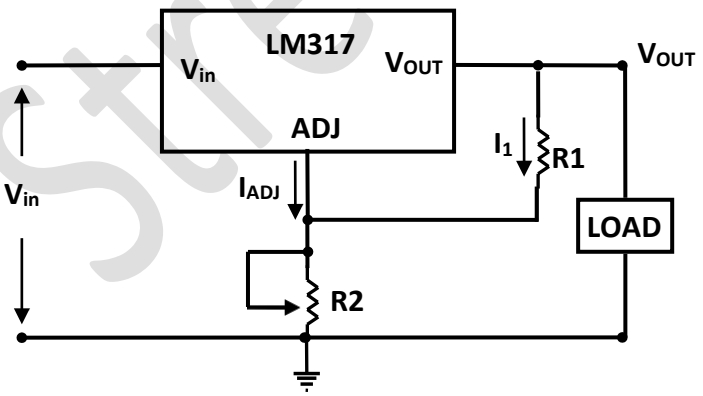


Figure 8.03: Connection diagram of Positive adjustable voltage regulator

The 3-terminals are: V_{in}, V_{OUT} and ADJUSTMENT (ADJ). From figure 8.03, LM317 requires only two resistors (R1= 240Ω and R2= 3kΩ) to set the output voltage. When configured, LM317 produces a 1.25 V, referred as reference voltage (V_{REF}), between the output and adjustment terminal. Since this reference voltage is constant, current I_1 is also constant for a given value of R1. Resistor R1 is called as current set or program resistor. Current ($I_1 + I_{ADJ}$), flows through the output set resistor R2.

Referring to the connection diagram, we will determine the output voltage expression as:

The output voltage, $\mathbf{V_{OUT} = R1.I_1 + R2(I_1 + I_{ADJ})}$ **(6.5)**

Where, $\mathbf{I_1 = (Drop\ across\ R1)/\ R1 = (V_{REF})/R1}$

R1 = Current (I1) set resistor

R2= Output (Vo) set resistor

I_{ADJ} = Adjustment pin current (100µA max. Value)

Substituting the value of I_1 in equation 6.5, we get:

$$V_O = V_{REF}(1 + \frac{R_2}{R_1}) + I_{ADJ} R_2 \text{ ---------- (6.6)}$$

Where, V_{REF} = 1.25V and however I_{ADJ} is very small (100µA) and constant. Therefore, drop across resistor R2 is very small and can be neglected.

Hence, $V_O = V_{REF}(1 + \frac{R_2}{R_1})$ ---------- **(6.7)**

Equation 6.7 indicated that the output voltage Vo is a function of resistor R2 for a given value of resistor R1 and can be varied by adjusting the value of resistor R2. To achieve good regulation, resistor R1 shoud be tied directly to the output of the regulator, as shown in figure 8.03.

Table 1.3 shows the different grade LM317 regulators.

Device	Vo (V)	Io (A)	V_{in} (max) in volts	Ripple rejection (dB)
LM317	1.2 to 37	1.5	40	80
LM317H	1.2 to 37	0.5	40	80
LM317HV	1.2 to 57	1.5	60	80
LM317HVH	1.2 to 37	0.50	40	80
LM317L	1.2 to 37	0.10	40	65
LM317M	1.2 to 37	0.50	40	80

Table 1.3

The different grades of regulators in the series are available with output voltage of 1.2 to 57V and output current from 0.10 to 1.5A. These ICs are available in standard transistor packages that are easily mounted and handled.

Adjustable negative voltage regulator:

LM337 series is adjustable negative voltage regulators devices. These are available in same voltage and current options as LM317 devices. Table 1.4 shows the different grades of regulators in the series.

Device	Vo (V)	Io (A)	V_{in} (max) in volts	Ripple rejection (dB)
LM337	−1.2 to −37	1.5	40	77
LM337H	−1.2 to −37	0.5	40	77
LM337HV	−1.2 to −47	1.5	50	77
LM337HVH	−1.2 to −47	0.50	50	77
LM337LZ	−1.2 to −37	0.10	40	65
LM337M	−1.2 to −37	0.50	40	77

TABLE 1.4

Disadvantage: Fixed and adjustable voltage regulators such as 78XX, 79XX and LM317 and LM337 are called as series dissipative regulators because these regulators creates a variable resistance between the input voltage and the load, and hence function in a linear mode. Thus linear regulator maintains a constant output voltage by dissipating the excess power as heat. Conversion efficiency of series dissipative regulator decreases as the input/output voltage increases or vice versa. Hence, for this reason the linear series regulator is matched with medium current applications, where power dissipation can be handled with heat sinks.

SWITCHING REGULATORS:

To improve the conversion efficiency of regulator, the series-pass transistor is used as a switch, rather than as a variable resistor as in linear series regulator. A regulator constructed in this manner is called as switching regulator. In switching regulators, a series pass transistor is used to switch between cut off and saturation at a high frequency, which produces a pulse width modulated square wave output. This PWM output is then filtered through a Low Pass LC filter to produce an average DC output voltage. The conversion efficiency of this regulator is independent of input/output differential and can approach up to 95%.

Switching regulators comes in various configurations such as: Fly back, feed forward, push pull, and non-isolated single ended or single polarity types.

The way, in which the components (switch and filter) are connected, the switching regulators can operates in any of the three modes: Step down, step up, or polarity inverting.

Basic Switching regulator:

Basic switching regulator has 4-major components: (i) Voltage source V_{IN} (ii) Switch S1 (iii) Pulse generator V_{Pulse} and (iv) Filter F1. Figure 8.04 shows the interconnection between the components of basic switching regulator.

(i)Voltage Source, V_{IN} : Supply Voltage source V_{IN} may be any DC supply ie. a battery or an unregulated or a regulated voltage. Following requirements must satisfy by the voltage source are:

1) The losses associated with voltage source and the required output power must be supplied by voltage source.
2) It must be large enough to supply satisfactory dynamic range for line and load variations.
3) It must be sufficiently high to meet the minimum requirement of the regulator system to be designed.
4) During power failure, voltage source should store energy for specified amount of time, for a back up.

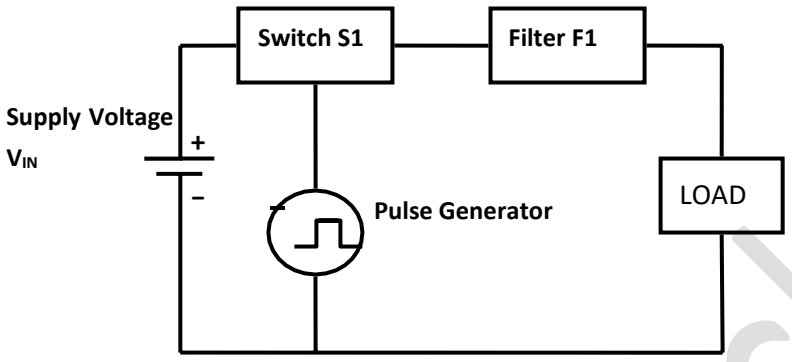


Figure 8.04: Connection diagram of basic switching regulator

(ii) Switch S1: Transistor or thyristor is used as power switch. Switch is operated in saturated mode. Generally output of pulse generator used to turn the switch ON and OFF.

(iii) Pulse Generator V_{Pulse}: It produces an asymmetrical square wave varying in either frequency or pulse width called frequency modulation or pulse width modulation. Effective frequency range of pulse generator is around 20kHz and is well within the switching speeds of transistors and diodes.

The duty cycle of pulse waveform is given as :

duty cycle = $\frac{t_{ON}}{t_{ON}+t_{OFF}} = \frac{t_{ON}}{T} = (t_{ON} \cdot f)$; Where, t_{ON} = on-time of the pulse waveform

t_{OFF} = off-time of the pulse waveform; T = time period.

Typical operating frequencies of switching regulators range from 10 to 50 kHz.

(iv) Filter F1: Filter is one of the major components in filter designing. The basic filter types are RC,RL and RLC, which are used in switching regulators. The RLC filter is most commonly used filter. Filter F1 converts the pulse into a DC voltage.

Output Voltage V_O, is a function of duty cycle and input voltage V_{IN}, and is expressed as : $V_O = (\frac{t_{ON}}{T}) \times V_{IN}$

Expression of output Voltage V_O, indicates that when time period T is held constant, V_O is directly proportional to the on-time, t_{ON} for a given value of V_{IN}. This method of changing the output voltage by varying t_{ON} is referred to as pulse width modulation (PWM). Similarly, if t_{ON} is held constant, output voltage is inversely proportional to time period, T or directly proportional to frequency f of pulse waveform. This method of changing the output voltage by varying frequency f, is referred to as frequency modulation (FM).

Switching regulators are used in commercial switching supplies with multiple outputs. µA78S40 is an example of switching regulator.

DUAL POWER SUPPLY:

Figure 8.05 shows the circuit diagram of dual DC power supply.

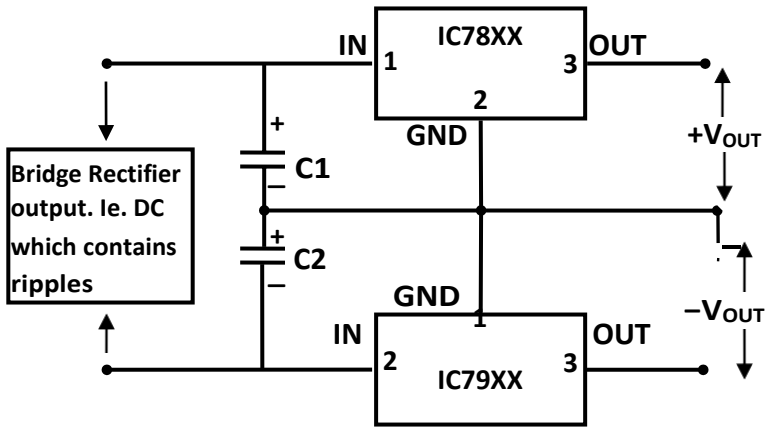


Figure 8.05: Dual DC power supply

Bridge rectifier circuit, which will convert the ac supply into dc supply. The output of the rectifier circuit ie. DC, contains the ripples in the output voltage. To filter out these ripples, capacitors C1 and C2 are used. The output of the capacitor that is pure DC is given to voltage regulator IC78XX and IC79XX which will regulate the output voltage at +XX Volt and –XX Volt DC, despite the change in input voltage.