KLE Technological University

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School

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Electronics and Communication Engineering

Minor Project Report
on

RRAM Based In-Memory Computation

By:

1. **Harsha S Hiregoudar** 01FE20BEC183
2. **Kiran Hanamagoudar** 01FE20BEC214
3. **Sneha Kumari** 01FE20BEC272
4. **Sneha S Anchekar** 01FE20BEC291

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Under the Guidance of

Dr. Vijay H M

K.L.E SOCIETY'S
KLE Technological University,
HUBBALLI-580031
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SCHOOL OF ELECTRONICS AND COMMUNICATION ENGINEERING

CERTIFICATE

This is to certify that project entitled " **RRAM Based In-Memory Computation**" is a bonafide work carried out by the student team of **Harsha S Hiregoudar (01FE20BEC183), Kiran Hanamagoudar(01FE20BEC214), Sneha Kumari (01FE20BEC272), Sneha S Anchekar(01FE20BEC291).The project report has been approved as it satisfies the requirements with respect to the minor project work prescribed by the university curriculum for BE (VI Semester) in School of Electronics and Communication Engineering of KLE Technological University for the academic year 2022-2023.**

Dr. Vijay H M	**Dr. Nalini C. Iyer**	**Dr. Basavaraj S Anami**
Guide	**Head of School**	**Registrar**

External Viva:

Name of Examiners	**Signature with date**
1.	
2.	

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-Harsha S Hiregoudar
Kiran Hanamagoudar
Sneha Kumari
Sneha S Anchekar

ABSTRACT

RRAM-based 1T1R (one transistor one resistor) in-memory computation is a novel approach for achieving high-performance and energy-efficient computing. In this approach, the RRAM device is integrated with a transistor to form a 1T1R structure, which enables both data storage and computation in the same memory cell. The 1T1R structure can perform various arithmetic and logical operations, such as addition, subtraction, multiplication, and comparison, directly in the memory array, without the need for data transfer to the processing unit. This approach can significantly reduce the energy consumption and latency compared to conventional computing architectures. This paper provides an overview of the RRAM-based 1T1R in-memory computing approach and discusses the recent developments, challenges, and opportunities in the field.

Contents

Chapter 1

Introduction

Prof. Leon Chua is known for formulating the theory of nonlinear circuit elements, which are capable of exhibiting memory and other complex behaviors. Memristors are basic circuit components that relate the charge q and flux linkage φ as a function of time t, and he presented the idea of them in his theory [1]. These memristors can be connected with other basiccircuit components, including resistors, capacitors, and inductors, to create circuits that are more sophisticated and capable of displaying a variety of behaviours.The relationship between basic circuit components is depicted in fig. 1.1.

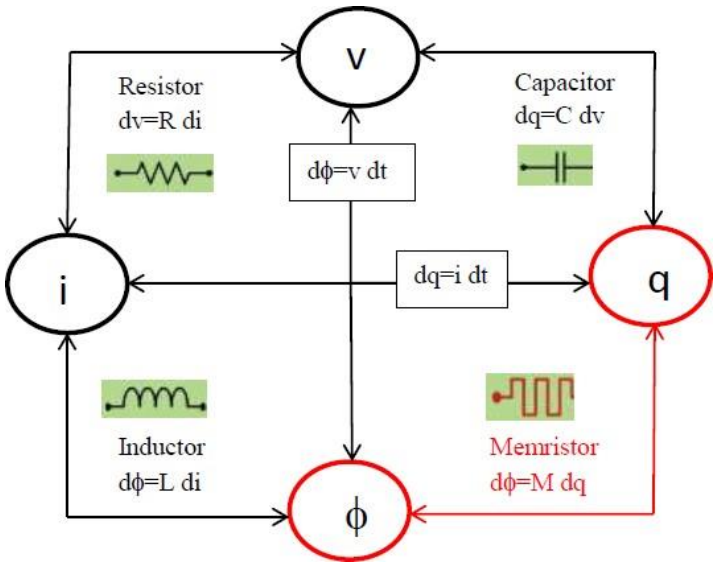


Figure 1.1:Relation between fundamental circuit elements

Resistive Random Access Memory (RRAM) devices are used in RRAM-based in-memory computation, a novel computing paradigm, for both data storage and processing. In this method, the memory arrays are employed for both data storage and processing, and the RRAM devices serve as computational

units. In comparison to conventional computing designs that need data transfer between the memory and processor units, the RRAM-based in-memory computing technique can dramatically lower the energy consumption and latency. RRAM-based in-memory computing has become a reality because to recent improvements in nanoscale RRAM devices and in the circuit and microarchitecture layers.

1.1 Motivation

The charge-based memory systems face serious hurdles at the nanoscale, resulting in a loss of reliability, performance, and noise margin.

The advantages of non-charge based memory are

- They have minimum operating voltage
- Perform fast write or read speed
- More retention time
- Excellent scalability
- Low-power consumption
- Long read/write endurance and perform fast write or read speed.

Characteristics of non-charge based memory are

- They have cell area of 4-12 F^2.
- Read and write time are less than 10 ns
- Have retention period of more than 10 years
- Operating voltage is less than 3 V
- Endurance is of the range 1e6-1e12.
- Moreover, the RRAM technology is compatible with the CMOS technology and easily scalable.

RRAM has a wide range of applications, namely logic applications, non-volatile memory applications, hardware-based security applications and neuromorphic applications.
Device Characteristics of various memory technology shown in Table 1.1

Table 1.1 : Device Characteristics of various memory technology

Device characteristics	Main stream memories			Emerging memories		
	SRAM	DRAM	NAND FLASH	STT-MRAM	PC-RAM	**RRAM**
Cell area (F^2)	100	6	4	6 ~ 50	4 ~ 30	**4 ~ 12**
Operating voltage	1V	1V	>10V	<1.5V	<3V	**<3V**
Read time	1 ns	10 ns	10 µs	10 ns	10 ns	**10 ns**
Write time	1 ns	10 ns	100µ-1ms	10 ns	50 ns	**10 ns**
Endurance (cycles)	1E16	1E16	1E4	1E15	1E9	**1E6-1E12**
Retention	NA	64 ms	10 years	10 years	10 years	**10 years**

1.2 Objectives

To increase the effectiveness and speed of data processing, resistive random access memory (RRAM) is used for in-memory computation. When computation can be done entirely within the memory, there is no longer a need to send information from the processor's memory.More elaborate and procedural objectives in order are as followed:

1.To create the RRAM Symbol in cadence using Verilog-A model.

2.To realise the Basic Gates using RRAM.

3.Simulation of Basic Gates.

4.To construct the RRAM array(crossbar and 1T1R).

5.Simulation of RRAM arrays.

6.Perform in-memory Computation.

1.3 Literature survey

1. RRAM Conductive Filament Geometrical Variations And Its Impact On Single-event Upset

In the von Neumann computer design, the central processor unit (CPU) and the storage device are independent components [13]. Through a proper interface, data is transferred from the memory to the CPU during processing. The latency rises along with the volume of data, which reduces the efficiency of the system as a whole. This results in the von Neumann architecture's bottleneck [14]. To get over the aforementioned congestion, numerous methods have been put forth. One approach is to use several processing cores [14], another is to design specialised accelerators [15], and a third is to do computation in memory [16]. Data is moved less often between memory and processing units in newer computers.

2. Logic Synthesis for RRAM-based In-Memory Computing

The three stated data structures—BDDs, AIGs, and MIGs—are used in this study's comprehensive strategy for the logic synthesis of in-memory computing circuits based on RRAM for effective representation [17]. The Majority-Inverter Graph (MIG), a brand-new homogeneous logic representation structure, only employs the majority function and negation as logic operations [17]. Faster design times for logic circuits and FPGA implementations are made possible by MIGs. In experiments, MIGs outperformed the well-known data structures BDDs and AIGs in terms of logic optimisation, especially in terms of propagating delay.

3. Memristor-Based Analog Computation and Neural Network Classification with a Dot Product Engine

By leveraging Kirchhoff's current law for summing and Ohm's law for resistance, dense crossbar architectures may naturally perform vector matrix multiplication (VMM), a crucial computing function of interest with memristors [18]. The dense memristor crossbar approach for VMM is one instance of the "computing by physics" paradigm among other freshly proposed and realised analogue systems [18]. One of the key matrix-intensive applications that could be impacted by speeding up VMM computations at lower power with memristor crossbars is speech recognition. Other notable matrix-intensive applications include photo and video classification, neuromorphic engineering, and signal processing. Even more of an impact will result from using memristors' nonvolatility to significantly reduce data

retrieval and communication costs—the well-known von Neumann bottleneck that fundamentally limits practically all system performance. Deep neural networks' inference and training periods are when this bottleneck is most obvious.

4. In-memory computing on resistive RAM systems using majority operation

majority operation-based in-memory computation on resistive RAM systems The objective of this work is to design a memristor-based system with 3-variable majority (MAJ) operations.The 1T1R VTEAM memristor model, which operates in two modes, and the Predictive Technology Model (PTM) for 45 nm transistors created by Arizona State University (ASU) as access devices .

1. The standard memory mode, which performs read and write operations.
2. In the in-memory computing mode, MAJ operations are performed on the memory cells [19].

1.4 Problem statement

The aim of the project is to design,implement and simulate 1T1R array using RRAM which performs In-memory computation.

1.5 Organization of the report

• Chapter 1: Introduction
It includes motivation towards the project, objectives of project, litera ture survey done towards the problem statement, defining the problem statement

• Chapter 2: System design
This chapter includes the High level functional block diagram and descrip tion of the functional blocks.

• Chapter 3: Implementation details
This chapter contains detailed information about implementation. It also includes specifications used to design and propose the final system ar chitecture. The algorithm and flowchart give the birds-eye view of the functionalities achieved.

- Chapter 4: Results and Analysis This chapter includes the conclusion and results of implementation.

- Chapter 5: Conclusion

This is the concluding chapter that includes project closure and epilogue along with the future scope of our project and application to societal context.

Chapter 2

System design

In this Chapter, we infer the High level functional block diagram,description of the functional block diagram.

One type of memory technologies is resistive RAM. It is a passive electrical device with a pair of terminals that merely expresses the ability of an electric component to remember its previous resistance it encountered prior shutting down.Resistive RAM is a type of non-volatile random access memory.

Device structure and its operation:
According to figure 2.1, it is a two terminal passive device with an insulating switching layer sandwiched between two electrodes that carry electricity.

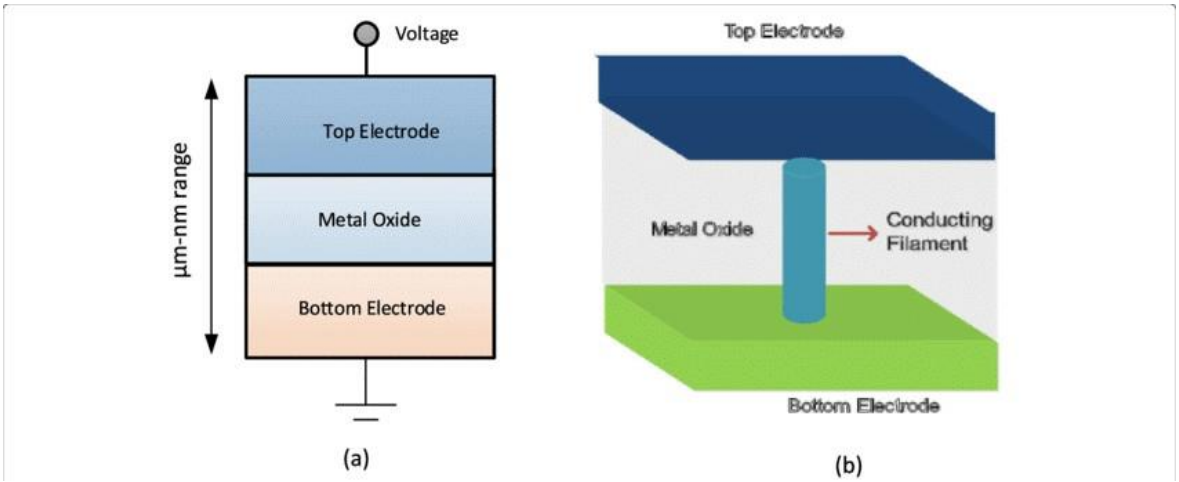


Figure 2.1: RRAM Structure

Applying external bias across a metal-insulator-metal (MIM) stack helps reduce the RRAM device's resistance. The electrode to which current or voltage is applied is referred to as the top electrode, and any other electrode that is electrically grounded is referred to as the bottom electrode.
Here is a summary of the electrodes and the material for the resistive switching oxide layer. The materials utilised to make electrodes are TiN and

TaN. CuOx and WOx are more compatible than other oxides. Materials to choose HfOx, AlOx, NiOx, TiOx, and TaOx since they have received more attention and have been the subject of much research in the past.

Operations of RRAM

The switching process can be used to describe how RRAM operates. Instead of employing electrons to store data, RRAM uses variations in electric resistance caused by ions. Ions in resistive switching memory cells operate similarly to batteries at the nanomaterial scale. The ions dissolve and then precipitate at two electrodes in the cells. As a result, the electrical resistance changes, which can be used to store data. Oxygen vacancies, defects created by RRAM that can charge and drift in an electric field, are found in a thin oxide layer. Similar to how electrons and holes move in semiconductors, oxygen ions and vacancies move in oxide. Through a filament or conduction route created when a high enough voltage has been applied, dielectric can be made to conduct. The migration of metal defects or vacancies may increase conduction. Once produced, the filament can be reset or set. Measurement of the area dependence can distinguish lower resistance that is either homogeneous or localised.

The switching behaviour in RRAM can be divided into two categories based on the shape of their current-voltage (IV) characteristics: Unipolar and Bipolar .

Unipolar: the polarity of the applied voltage has no bearing on the direction of the switching.

When a sufficiently high voltage is provided, unipolar switching causes the resistance of the RRAM cell to vary while only allowing one direction of current to flow. On the IV curve of a unipolar RRAM cell, the forming procedure required to create a conductive filament in the oxide layer is displayed. The IV curve demonstrates a set process, where the resistance drops, and a reset process, where the resistance increases, after the filament has been produced. The applied voltage pulse's amplitude and length can regulate the set and reset procedures.

Bipolar: Set and reset occur in opposite polarities and are sensitive to polarity. Only negative voltage can reset a memory device if it can be set by providing positive voltage to the top electrode.

Bipolar switching causes current to flow in both directions and the resistance of the RRAM cell to alter when a voltage of either polarity is applied. The bipolar RRAM cell's IV curve exhibits a similar development and is followed by a continuous decrease in resistance during set and a gradual increase in resistance during reset. The switching behaviour of bipolar RRAM cells is controlled by the polarity and amplitude of the applied voltage pulse.The IV Characteristics of Unipolar and Bipolar Modes are depicted in Figure 2.2.

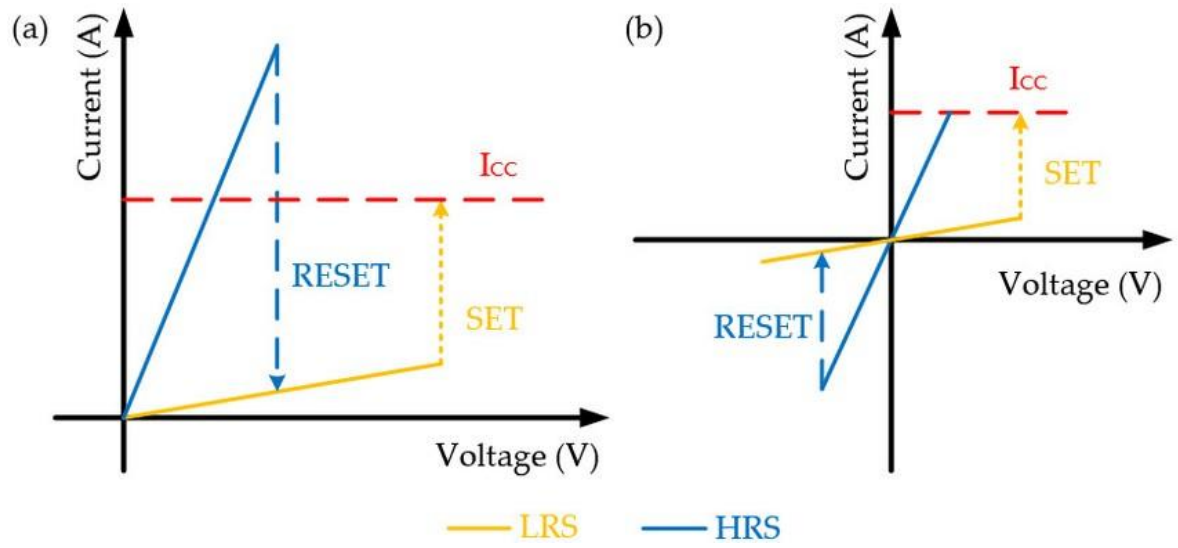


Figure 2.2: (a) Unipolar and (b) Bipolar Modes for RRAM devices

Set refers to moving RRAM from low resistance state (LRS) to high resistance state (HRS), while reset refers to switching RRAM from low resistance state (LRS) to high resistance state (HRS).

In conclusion, the voltage pulse given to the cell can regulate the switching behaviour in RRAM, and the type of switching behavior—unipolar or bipolar—depends on the material and cell structure.

Types of RRAM

It is categorised into two types

1. Oxygen vacancy based RRAM
2. Metal ion based RRAM or conductive bridge RRAM

1. Oxygen vacancy based RRAM

It is a two-terminal device with two electrodes at the top and bottom, which are usually metallic electrodes, and a metal oxide in the middle. The RRAM device state depends on the development of this oxygen-vacancy filament. So,

while we have the filament, we store state ”1”, and when we don’t, we store state ”0”. Creation of oxygen filament is showed in fig 2.3 .

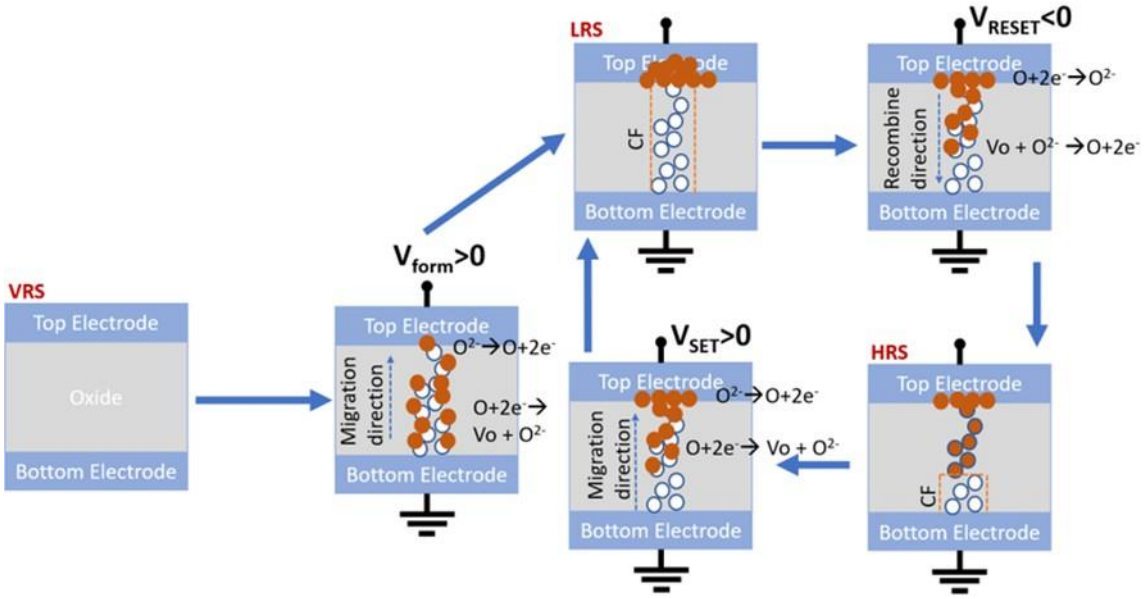


Figure 2.3: Representation of redox activity in bipolar-switching RRAM devices that causes the formation and dissolution of oxygen vacancies filaments

2. Metal ion based RRAM or Conductive bridge RRAM

This kind of RRAM is predicated on the movement of metal ions. into solid electrolyte material, which can be either oxide or chalcogenide. Therefore, the filament still forms the basis of the physical mechanism here. Here, the top and bottom electrodes are active and are often constructed of copper or silver. In other words, if we apply positive voltage, the atoms of copper and silver can easily be ionised. They will transform into copper and silver ions, which will then diffuse into the insulating layer and create this metallic filament to conduct the current. Creation of ion filament is showed in fig 2.4

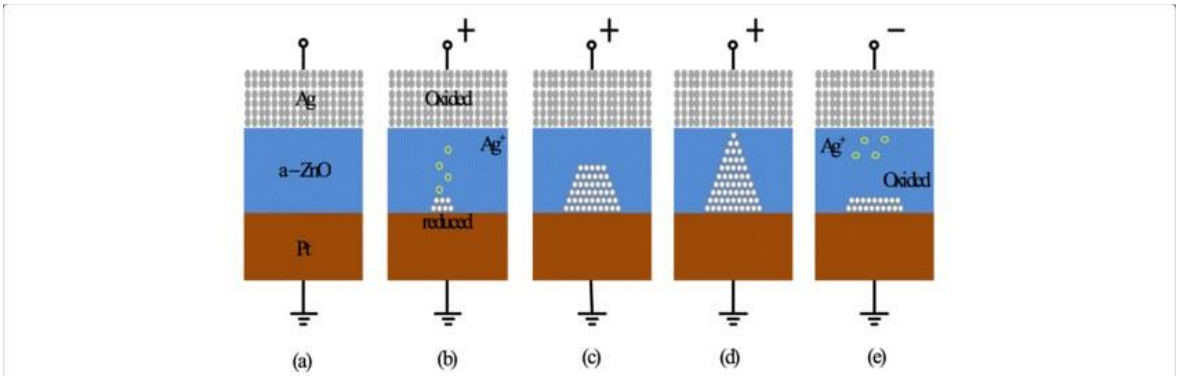


Figure 2.4:

Diagram of the conductive bridge RRAM's switching system. an RRAM device in its purest state. Ag is oxidised, and Ag + cations migrate to the cathode and are reduced there. d. The formation of a highly conductive filament is caused by the accumulation of Ag atoms and Pt electrode. e. Applying polarity-opposite voltage causes filament disintegration.

RRAM Memory Architecture

A. 1T1R

The simplest RRAM array construction is 1T1R (one transistor, one resistor). Each RRAM cell in this system is coupled to a single transistor and a single bit line. The bit line and transistor are used to read and write data into and out of the RRAM cell, respectively.

Low-density RRAM memory arrays, where there are few RRAM cells, frequently employ the 1T1R architecture. The simplicity of the 1T1R architecture has advantages such as low cost and simple CMOS technology integration. The 1T1R architecture does, however, have several drawbacks, including limited density and poor scalability.

B. Crossbar

For high-density memory arrays, the Crossbar design is a more intricate RRAM array architecture. Each RRAM cell in this architecture is coupled to two orthogonal sets of electrodes, resulting in a crossbar structure. The RRAM cell is chosen using the electrodes, which are also used to read and write data to the RRAM cell.

Compared to the 1T1R architecture, the Crossbar array has a number of benefits. One benefit is that a lot of RRAM cells may be crammed into a compact space due to its high density. Its scalability, which enables the creation of memory arrays with huge capacity, is another benefit.

The Crossbar architecture does have several difficulties, though. The sneak path problem, which happens when the current travels along undesired paths in the crossbar structure, is one difficulty. Data mistakes and decreased dependability of the memory array might result from the sneak path problem. Several solutions, including current limitation and diode insertion, have been put forth to deal with this issue.

The heterogeneity of the RRAM cells presents another difficulty for the Crossbar architecture. The performance and dependability of the memory array may be impacted by the RRAM cells' unpredictability. Many methods, including statistical analysis and redundancy, have been suggested to address this issue. Schematic and layout diagram of 1T1R array and crossbar array is shown in fig 2.5

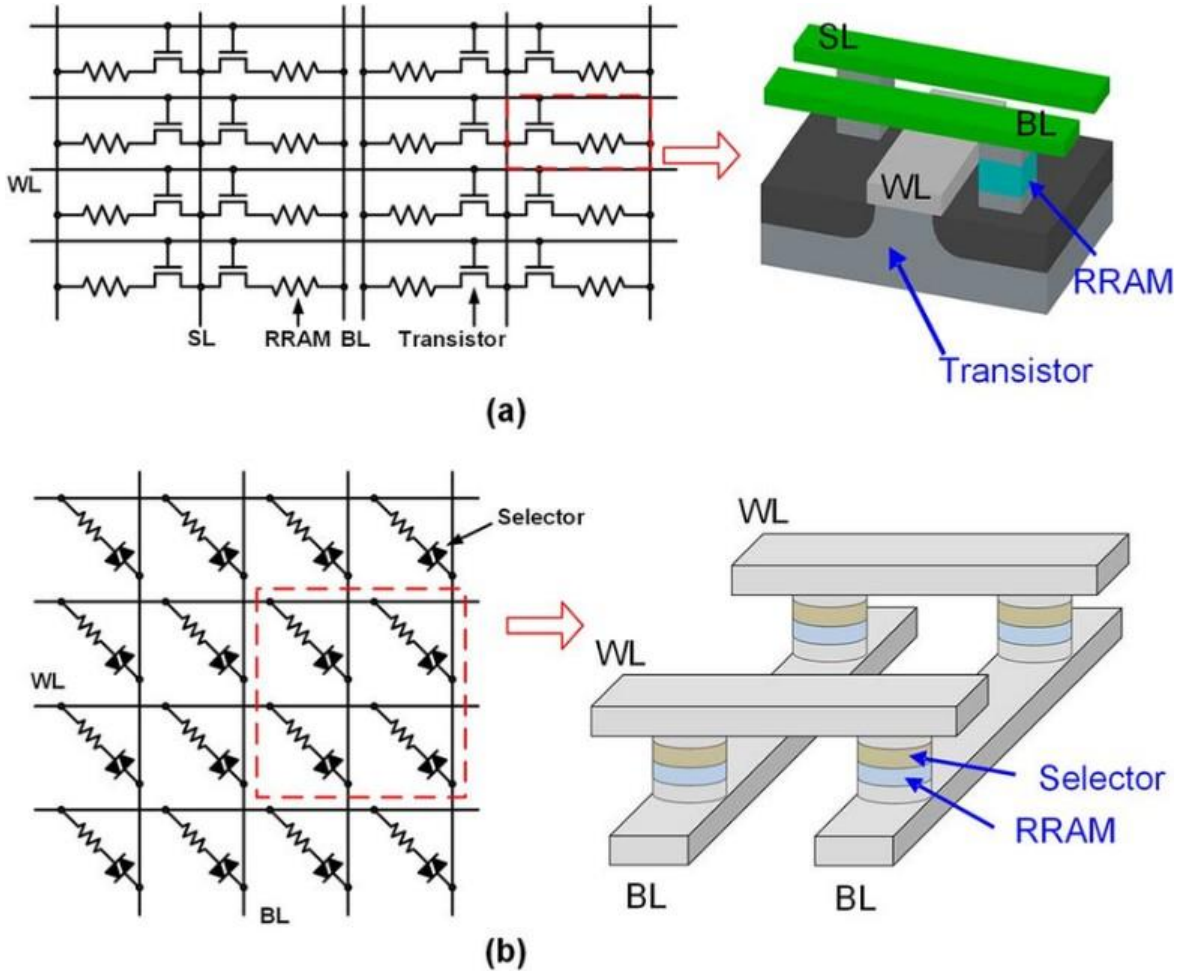


Figure 2.5:Schematic and layout diagram of (a) 1T1R array and (b) crossbar array.

In conclusion, the unique application and the intended performance and cost criteria determine which RRAM array architecture is best. While the

Crossbar architecture is appropriate for high-density memory arrays, the 1T1R architecture is best suited for low-density memory arrays. More study is required to increase the performance and dependability of these architectures, which each have their own advantages and difficulties.

2.1 Functional Block Diagram

In-memory computation is a computing architecture that stores and processes data in the same physical location, such as RAM. Key components include the ALU, cache, control unit, and in-memory computing blocks. In-memory computing blocks are small sections of memory used to store and process data efficiently and in parallel. This architecture can provide significant performance benefits by reducing data movement and improving processing speed. Block diagram of in-memory computation is shown in fig 2.6 .

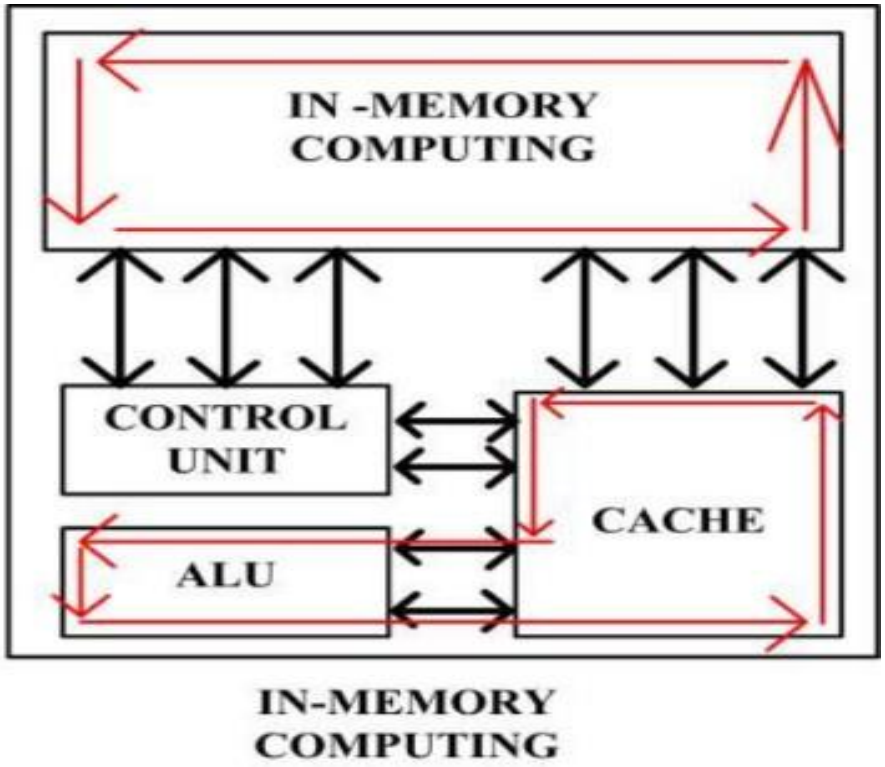


Figure 2.6 : Block diagram

Creation of RRAM symbol

Using specification of VTeam model on writing Verilog code , we created RRAM symbol. RRAM symbol is shown in fig 2.7 .

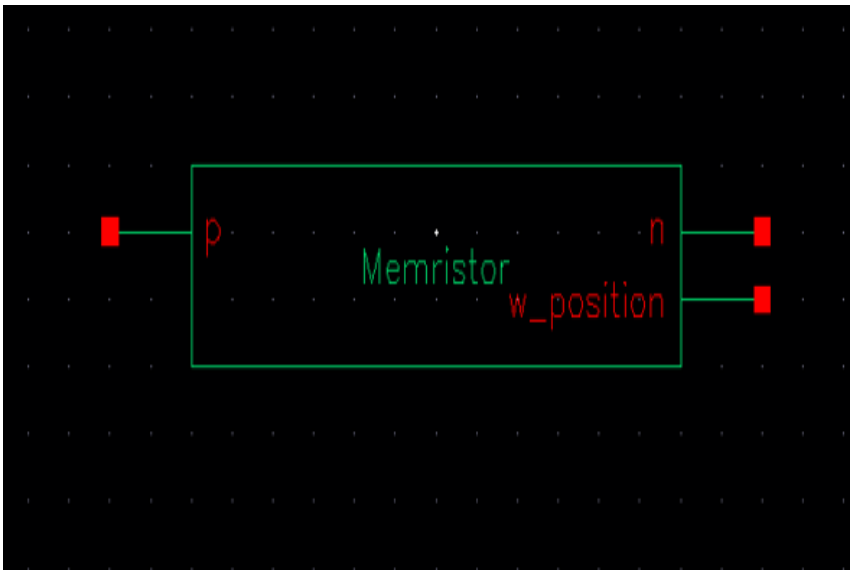


Figure 2.7 : RRAM Symbol

We tested VTeam model RRAM : Test circuit of RRAM is shown in fig 2.8 .

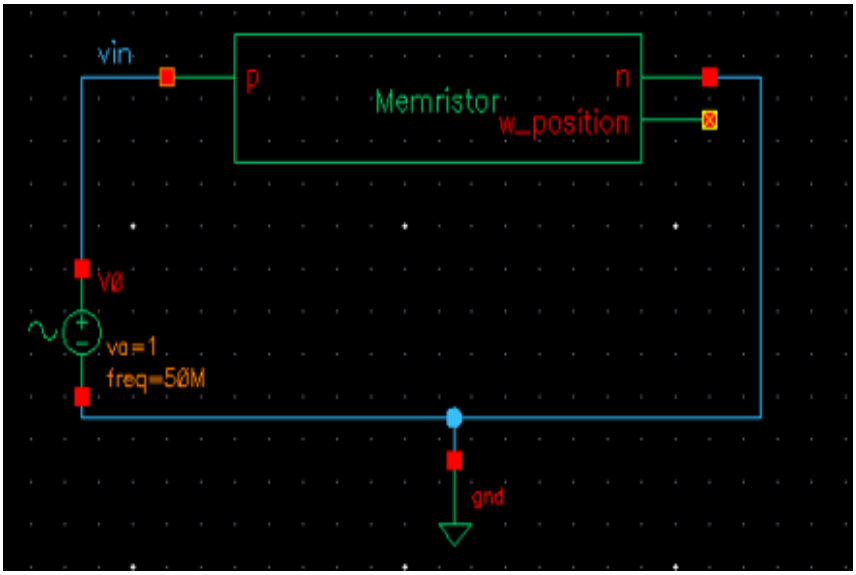


Figure 2.8 : Test Circuit Of RRAM

IV Graph of RRAM : IV Graph of RRAM is shown in fig 2.9 .

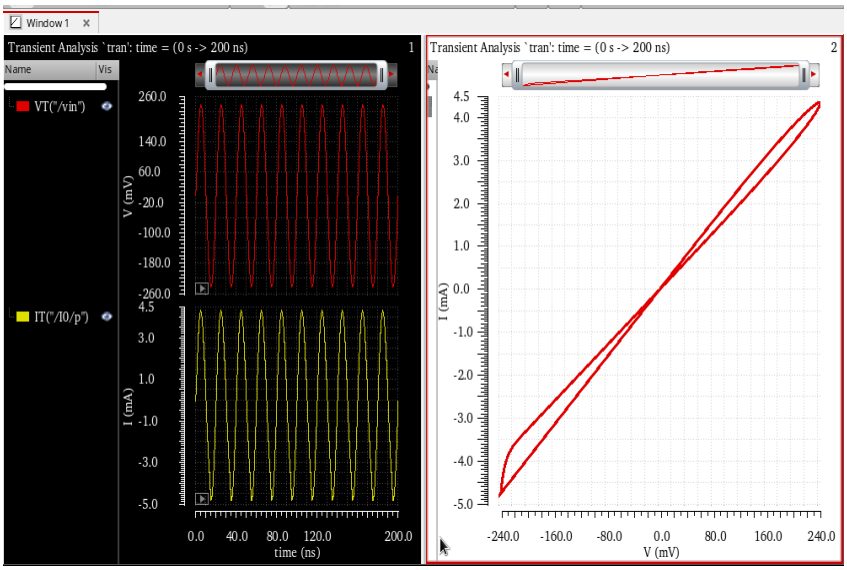


Figure 2.9 : IV Graph Of RRAM

Chapter 3

Implementation details

In this Chapter, we infer the detailed information about implementation. It also includes specifications used to design and propose the final system architecture.

3.1 Specifications and final system architecture

We have used VTeam RRAM Model. The specification table of this model is listed below in table 3.1

Table 3.1 : Design Specification

Name [Units]	**Description**	**VTEAM**
Frequency [Hz]	Source frequency (Sine input)	2
Source amp	Source amplitude	0.003 [A]
Ron [Ohm]	Memristor's minimum resistance	100
Roff [Ohm]	Memristor's maximum resistance	100k
D [m]	Physical width of the memristor	3e-09
V_threshold [V]	Threshold voltage	0
uv [m^2/Vsec]	Linear ion mobility	1e-10
P_coeff	Value of p in the window functions	2
Initial state	Initial state of the state variable	0.5
Alpha	Alpha in nonlinear ion drift	2
Beta	Beta in nonlinear ion drift	5
C	Chi in nonlinear ion drift	0.01
g	Gamma in nonlinear ion drift	4
n	n in nonlinear ion drift (odd positive integer)	14
q	q in nonlinear ion drift (odd positive integer)	13
a_on [m]	Upper bound of undoped region	2e-09
a_off [m]	Lower bound of undoped region	1.2e-09
i_on [A]	Threshold current in VTEAM	-8.9e-06
i_off [A]	Threshold current in VTEAM	0.0015
v_on [V]	Threshold voltage in VTEAM	-0.2
v_off [V]	Threshold voltage in VTEAM	0.02
c_on [m/s]	State derivative coefficient	3.5e-06
c_off [m/s]	State derivative coefficient	4e-05
b [A]	Normalized current	0.0005
X_c [m]	Normalized length	1.07e-11
k_on [m/sec]	kon in VTEAM	-10
k_off [m/sec]	koff in VTEAM	5e-4
x_on [m]	Lower bound of undoped region in VTEAM	0
x_off [m]	Upper bound of undoped region in VTEAM	3e-09
alpha_off	Nonlinearity power coefficient for VTEAM	1
alpha_on	Nonlinearity power coefficient for VTEAM	3
model	Required model	4
window_type	Required window function	0
dt	Numeric simulation time step (for virtuoso)	1e-10
W_multiplied	Normalization for the state variable (for virtuoso)	1e+08
P_window_noise	Small noise to avoid boundary problems in window functions (for virtuoso)	1e-18

System Architecture

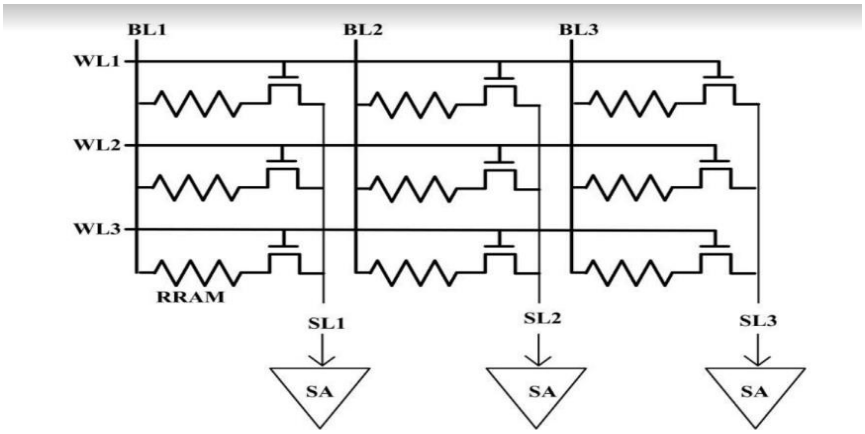


Figure 3.1 : System Architecture

Sense Amplifier Circuit:Data is read from the memory using the read circuitry, which includes a sensing amplifier.Its function is to detect the faint signals from a bitline that correspond to a data bit (1 or 0) stored in a memory cell and to amplify the faint voltage swing to recognisable logic levels so that the data can be correctly decoded by logic not contained in the memory.The structure of sense amplifier is shown in fig 3.2

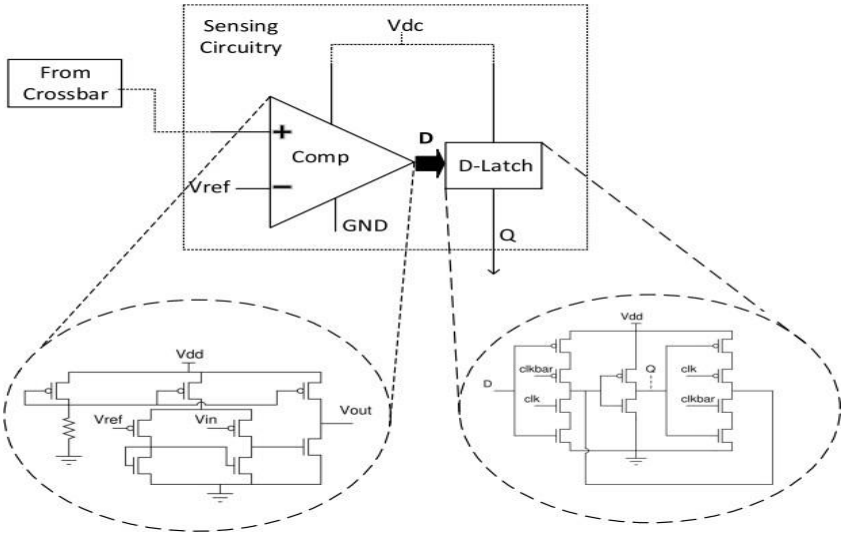


Figure 3.2 : Sense Amplifier Circuit

Realization of basics gates using RRAM

AND Gate:

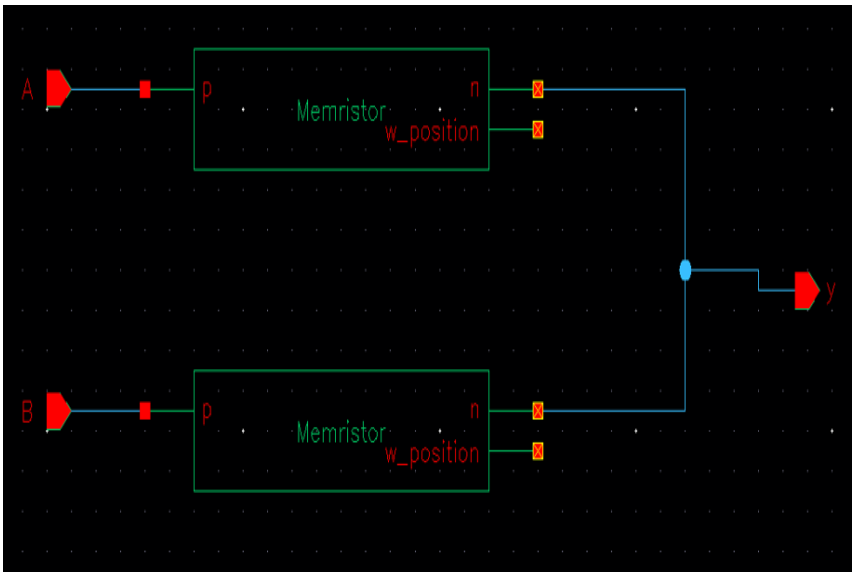


Figure 3.3 : And Gate Implementation Using RRAM

OR Gate:

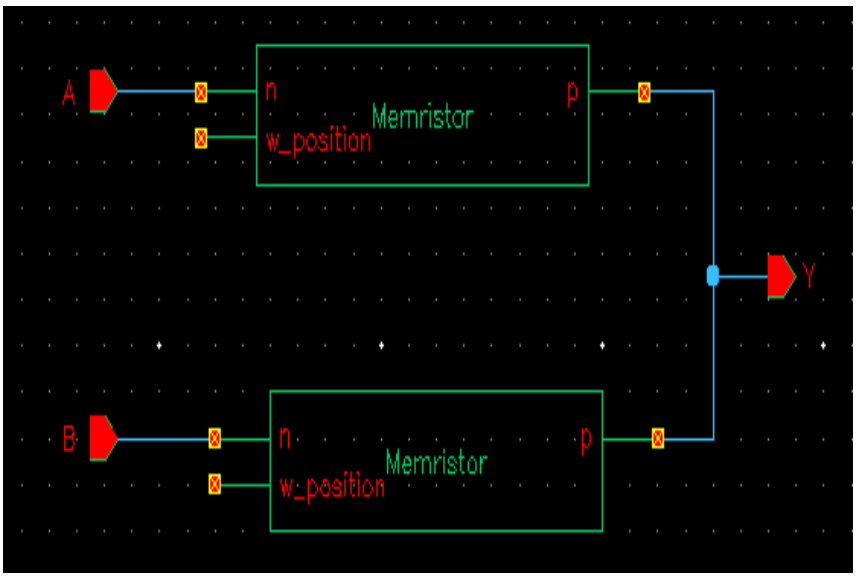


Figure 3.4 : OR Gate Implementation Using RRAM

EXOR Gate:

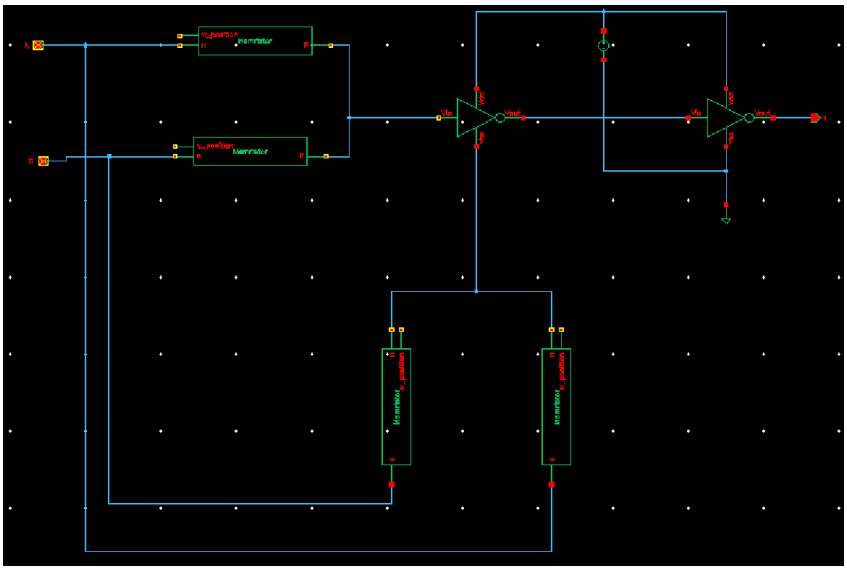


Figure 3.5 : EXOR Gate Implementation Using RRAM

Creation of 2-Bit multiplier:We created 2-bit multiplier using AND,OR and EXOR gate.

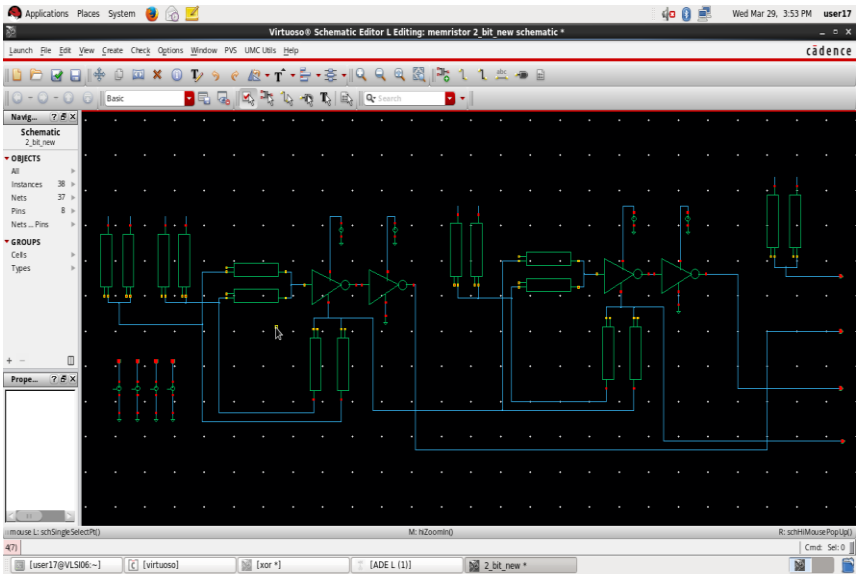


Figure 3.6 : Creation Of 2 Bit Multiplier

Waveform of 2-bit multiplier:

Figure 3.7 : Waveform Of Two Bit Multiplier

Truth table of 2-bit multiplier:

Table 3.2 : Two Bit Multiplier Truth Table

INPUT A		INPUT B		OUTPUT			
A_1	A_0	B_1	B_0	C_3	C_2	C_1	C_0
0	0	0	0	0	0	0	0
0	0	0	1	0	0	0	0
0	0	1	0	0	0	0	0
0	0	1	1	0	0	0	0
0	1	0	0	0	0	0	0
0	1	0	1	0	0	0	1
0	1	1	0	0	0	1	0
0	1	1	1	0	0	1	1
1	0	0	0	0	0	0	0
1	0	0	1	0	0	1	0
1	0	1	0	0	1	0	0
1	0	1	1	0	1	1	0
1	1	0	0	0	0	0	0
1	1	0	1	0	0	1	1
1	1	1	0	0	1	1	0
1	1	1	1	1	0	0	1

3.2 Algorithm

1. Creation of RRAM Symbol.
2. Perform transient analysis on RRAM.
3. Creation of Crossbar array(4x4)(8x8).
4. Simulation of crossbar array.
5. Creation of 1T1R array (4x4)(8x8).
6. Simulation of 1T1R arrays.
7. Perform in-memory Computation.
8. Compare Von-Neuman and in-memory Computation.

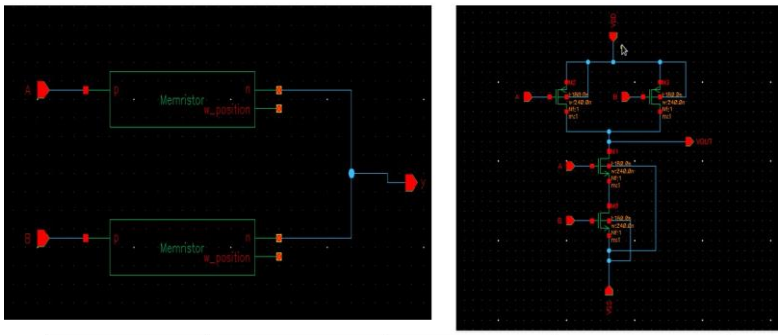
Chapter 4

Results And Analysis

4.1 Comparison between RRAM and CMOS logic:

The follwing figures compares the rise time, fall time,dealy and power of basic gates.

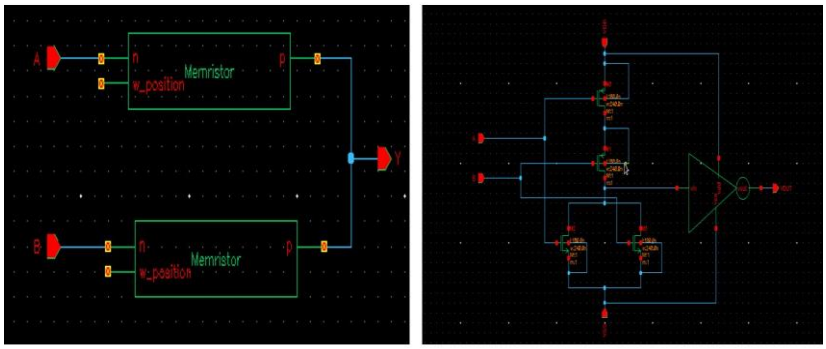
COMPARISION BETWEEN RRAM(AND) AND CMOS (AND)



RRAM (AND)	Value	CMOS (AND)	Value
Rise time	1.81ns	Rise time	2.804ns
Fall time	70.79ps	Fall time	556.6ps
Delay	55.4ps	Delay	117.9ps
Power	593.4mW	Power	564.9mW

Figure 4.1 : AND Gate Comparision

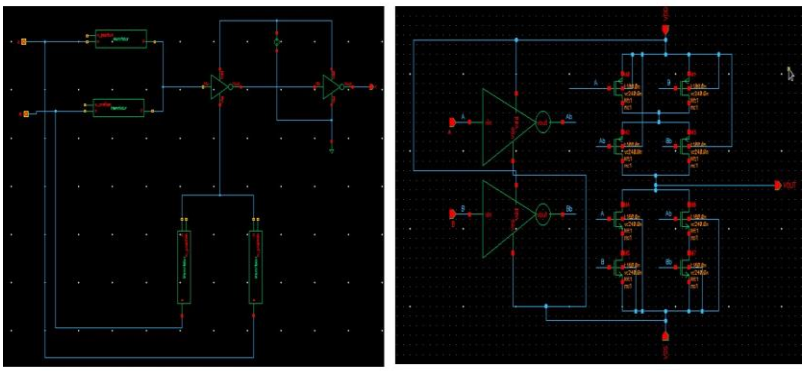
COMPARISION BETWEEN RRAM(OR) AND CMOS (OR)



RRAM (OR)	Value	CMOS (OR)	Value
Rise time	87.07ps	Rise time	180.6ps
Fall time	108.4ps	Fall time	569.6ps
Delay	30.7ps	Delay	115ps
Power	1.321mW	Power	1.453mW

Figure 4.2 : OR Gate Comparision

COMPARISION BETWEEN RRAM(XOR) AND CMOS (XOR)



RRAM (XOR)	Value	CMOS (XOR)	Value
Rise time	561.9ps	Rise time	3.596ns
Fall time	211.3ps	Fall time	948.5ps
Delay	121.170ps	Delay	158.77ps
Power	816.1mW	Power	781.9mW

Figure 4.3 : EXOR Gate Comparision

Transient Analysis Of 1T1R:

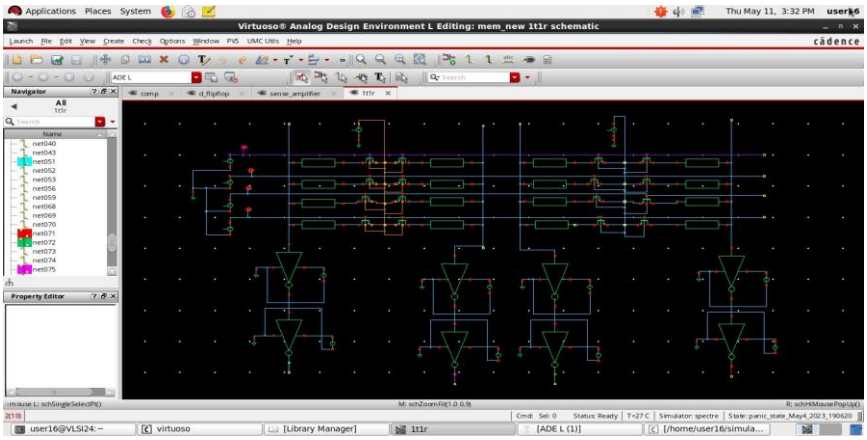


Figure 4.4: 1T1R Circuit Transient Analysis

4.2 Read/Write Test cases:

The following waveforms shows different read and write test cases

Case 1:Write 1

Figure 4.5: Write 1

Case 2: Read 1

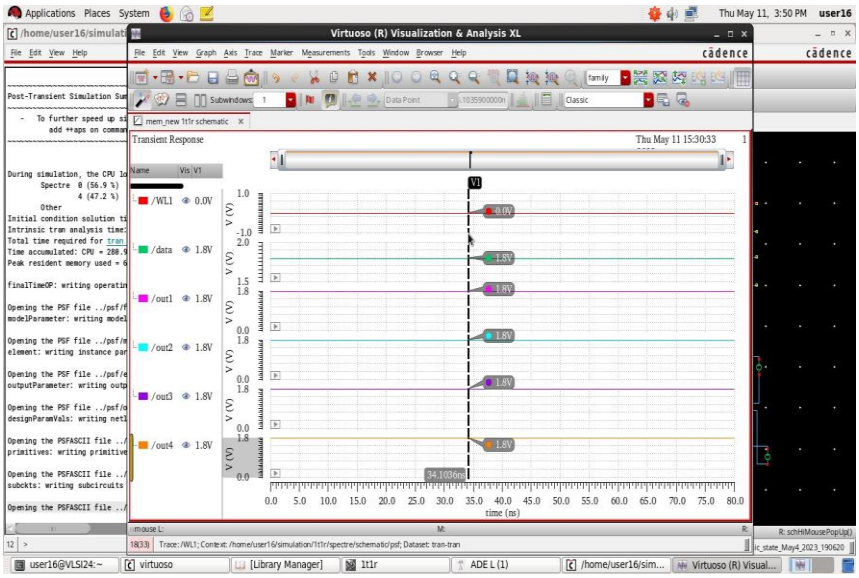


Figure 4.6: Read 1

Case 3: Write 0

Figure 4.7: Write 0

Case 4:Read 0

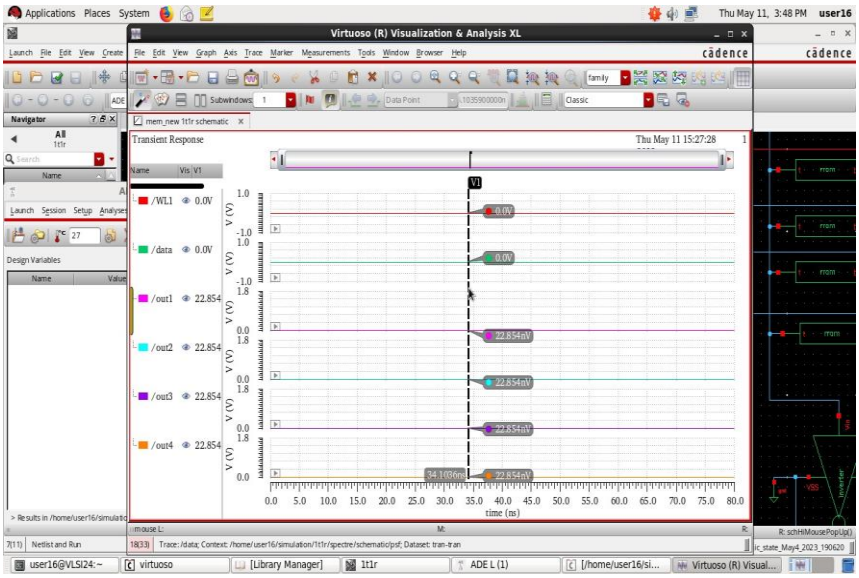


Figure 4.8: Read 0

1T1R Waveform:

Figure 4.9: 1T1R Waveform

Implementation Of Sense Amplifier:

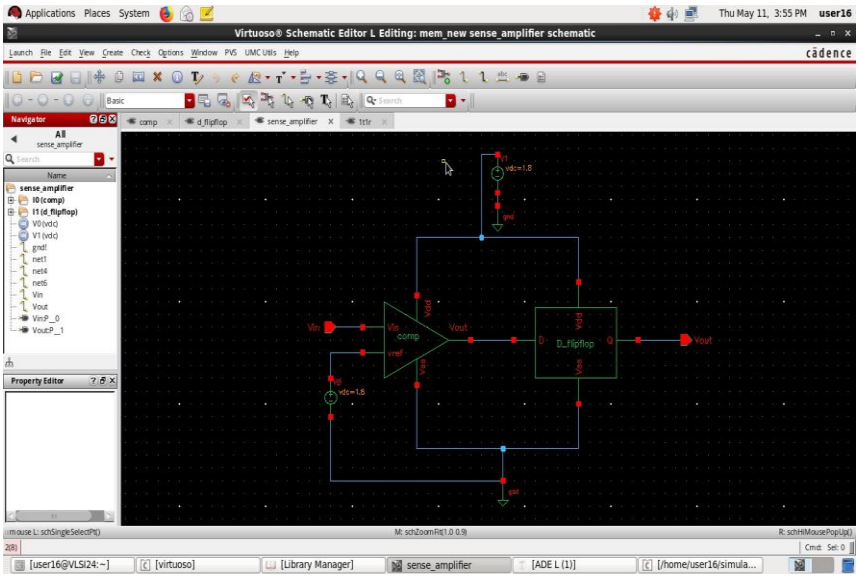


Figure 4.10 :Final Sense Amplifier Circuit

4.3 Analysis

- The delay of RRAM gates is also less when comparable to CMOS gates.
- This makes RRAM a promising technology for future generations of memory devices, especially for applications that require high-density and low-power consumption
- RRAM has many advantages over CMOS for certain applications, including non- volatility, scalability.

Chapter 5

Conclusions and future scope

This is the concluding chapter that includes project closure and epilogue along with the future scope of our project.

5.1 Conclusion

The project aimed to explore the potential of resistive random access memory (RRAM) for in-memory computation. To achieve this, the project objectives included creating RRAM symbols in Cadence using Verilog-A models, realizing basic gates using RRAM, simulating basic gates, constructing RRAM arrays (crossbar and 1T1R), simulating RRAM arrays for read and write operations, and performing in-memory computation.

Through the project, it was found that RRAM has the potential to perform in-memory computation, which can significantly improve the efficiency of memory and computing systems. The construction of RRAM arrays and the realization of basic gates using RRAM proved to be feasible and efficient. The simulations of RRAM arrays demonstrated the ability of RRAM to perform both read and write operations, indicating its potential as a non-volatile memory storage device.

The project results suggest that RRAM can be a promising alternative to traditional memory and computing systems. It can provide faster and more energy efficient memory computation by performing computations in the memory itself. However, further research is needed to optimize the design and performance of RRAM-based memory and computing systems for practical applications. Overall, the project provides a basis for future studies and applications of RRAM in memory computation.

5.2 Future scope

The project results suggest several potential future directions for research and applications of RRAM in memory computation. Some of the future scope includes:

1. Optimization of RRAM-based memory and computing systems for practical applications: Further research is needed for the design optimization and performance of RRAM-based memory and computing systems for practical applications, such as artificial intelligence, image and speech recognition, and data analytics.

2. Improvement of RRAM technology: There is a need for continued research to improve the RRAM technology, such as increasing the endurance and reliability of RRAM devices and reducing their power consumption.

3. Development of new algorithms: As RRAM can perform in-memory computation, new algorithms need to be developed to take advantage of this feature, leading to faster and more efficient computations.

4. Integration with other technologies: RRAM can be integrated with other emerging technologies, such as quantum computing and neuromorphic computing, to improve their performance and energy efficiency.

Overall, the future scope of RRAM in memory computation is promising, and further research and development in this area can lead to significant improvements in memory and computing systems' efficiency and performance.

5.2.1 Application in Societal Context

Resistive Random Access Memory (RRAM) has numerous potential applications in various societal contexts. Here are some examples:Medical diagnosis and treatment can be performed using RRAM-based sensors. They can be combined with wearable technology to track patients health and aid medical professionals in making precise diagnosis. RRAM-based memory devices can be used to store data from smart energy meters In self-driving automobiles, RRAM-based memory devices can be used to store and process information on driving performance, safety, and navigation. Agricultural soil moisture, temperature, and other environmental conditions can be monitored with RRAM-based sensors, which can help farmers increase crop output and decrease waste. Overall,RRAM has the potential to increase productivity, accuracy, and sustainability across a range of industries, having a positive influence on society as a whole.

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