School

of

Electronics and Communication Engineering

Senior Design Project Report

on

Single-Event Upset on Content Addressable Memory

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SCHOOL OF ELECTRONICS AND COMMUNICATION ENGINEERING

CERTIFICATE

This is to certify that project entitled **" Single-Event Upset on Content Addressable Memory"** is a bonafide work carried out by the student team of **Harsha S Hiregoudar (01FE20BEC183), Kiran Hanamagoudar(01FE20BEC214), Sneha Kumari (01FE20BEC272), Sneha S Anchekar(01FE20BEC291). The project report has been approved as it satisfies the requirements with respect to the senior design project work prescribed by the university curriculum for BE (VII Semester) in School of Electronics and Communication Engineering of KLE Technological University for the academic year 2023-2024.**

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ABSTRACT

Modern integrated circuits need close monitoring of the soft-error rate (SER) caused by bit upsets, which are often produced by alpha particle or neutron strikes. These incidents, also known as single-event upsets (SEUs), will become more troublesome in future technology.In this project, we demonstrated the results of SEU on Content Addressable Memory. First, we used Cadence to methodically design various CAM cells, including NOR, EXOR, and EXNOR type. We got insight into the behaviour and properties of each cell type through comprehensive simulations. We found that NOR type CAM cell has less delay and low power consumption,so we built the CAM array using NOR type cell. We modelled the impact of SEU by injecting a double exponential current pulse (DECP) into CAM array.The addition of a DECP improved our understanding of the system's robustness to varied stimuli. Finally, this project not only provided valuable insights into the reliability and vulnerability of CAM in the face of Single-Event Upsets, but also a thorough assessment of its power consumption and delay characteristics, paving the way for future advancements in radiation-hardened memory technologies.

Contents

Chapter 1

Introduction

Content Addressable Memory (CAM) is a type of computer memory that allows data to be accessed based on its content rather than a specific memory address. In CAM, the memory is organized in such a way that the data itself serves as the input and the memory returns the address where that data is stored.The fig 1.1 shows simple content addressable memory[1].

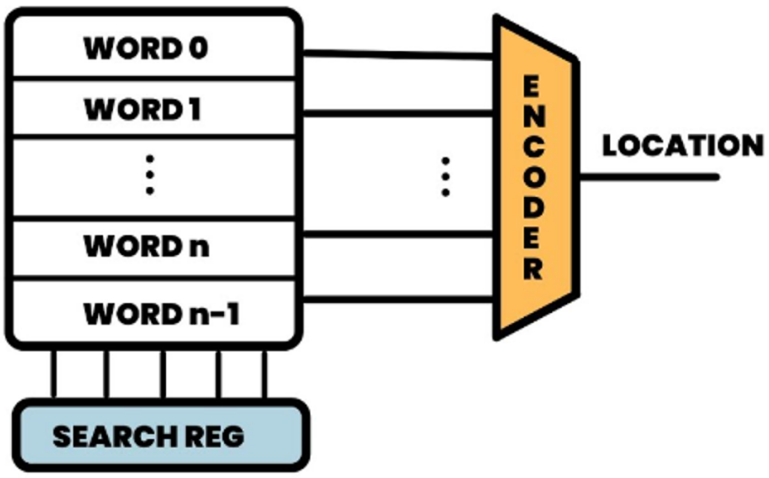


Figure 1.1: Simple content addressable memory array

CAM, on the other hand, is sensitive to a phenomena known as Single-Event Upset (SEU). The random alteration of a bit in memory induced by a single energetic particle or electromagnetic radiation contacting the memory cell is referred to as SEU. These particles, which are frequently cosmic rays or radiation from natural and man-made sources, can deposit enough energy to temporarily change the state of a memory cell, resulting in mistakes in data stored.

1.1 Motivation

The requirement for quicker and more efficient data retrieval in specialised computing applications drove the development of Content-Addressable Memory (CAM). Traditional memory systems need a precise memory address to access data, which can be time-consuming for associative searching and pattern matching applications. This constraint is addressed by CAM, which allows data to be retrieved depending on its content rather than a fixed address. This makes CAM especially useful in applications like as networking, databases, and artificial intelligence, where rapid and concurrent searches are critical for performance optimisation. The aim for CAM is to improve data access speed and efficiency, particularly in cases where standard memory architectures may fall short of satisfying the needs of associative and content-based retrieval

Traditional Memory (SRAM and DRAM) has the following disadvantages:

• High Power Consumption: In comparison to Content Addressable Memory (CAM), Static Random Access Memory (SRAM) and Dynamic Random Access Memory (DRAM) can consume a lot of power.
• Slower Access Times: DRAM has slower access times than other types of memory because it requires periodic refreshing to maintain the stored data.
• Volatility: DRAM is volatile memory, which means that it loses its stored data when the power is turned off.
• Complex Addressing: In order to access specific data in SRAM and DRAM, a memory address must be provided, which can be more complex and time-consuming than the content-based addressing used in CAM.

The advantages of CAM over SRAM and DRAM are as follows:

• Content-Based Addressing (CAM): CAM enables data retrieval based on content, removing the requirement for memory addresses. This feature makes it ideal for applications that require searching and matching patterns.
• Quick Search and Retrieval Operations: CAM excels at quick search and retrieval operations, providing real-time access to stored data. This speed is useful in networking devices, databases, and applications that require quick access to data.
• Lower Latency: CAM's associated nature results in lower latency for specific tasks when compared to traditional memory types. As a result, CAM is well suited for applications requiring low latency.

• Improved Data Integrity in Certain Applications: CAM's content-based addressing can improve data integrity, particularly in applications requiring exact matches or detection of patterns, such as network management.

Applications of Content Addressable Memory (CAM) :

1. Networking Devices
2. Database Systems
3. Pattern Matching and Recognition
4. Security Systems
5. Telecommunications

Device Characteristics of various memory technologies shown in Table 1.1[2].

Table 1.1 : Comparing SRAM, DRAM, CAM, and TCAM characteristics:

Feature	**SRAM**	**DRAM**	**CAM**	**TCAM**
Read Access Time	Fast	Slow	Very Fast	Very Fast
Write Access Time	Fast	Slow	Very Fast	Very Fast
Cost	Expensive	Inexpensive	Expensive	Very Expensive
Power Consumption	Low	High	Low	High
Applications	Cache memory, CPU registers	Main memory	Networking routers, firewalls	Networking routers, firewalls, network accelerators

1.2 Impact of Radiation on Semiconductor Memory

The charged particles produced by solar flares have an impact on the digital circuits foundin the space environment. A circuit becomes more radiation sensitive as its performance increases. Each of these actions increases the device's ra diation susceptibility, making low-charge particles that previously posed little threat to disruption or damage now considerably more likely. When creating Very Large-Scale Integrated (VLSI) circuits intended to be used in space missions, two groups of radiation effects must be taken into account.

1. Total Ionizing Dose (T.I.D.)
2. Single Event Effects (S.E.E.)

T.I.D. is caused by the cumulative charge accumulated in a material, which leads to the long-term deterioration of electronics. Electron and protons are mostly to blame for the long-term radiation effects on electronic gadgets. Solar Energetic Particle Events are the primary generators of these particles.

S.E.E. is a momentary effect brought on by a single charged particle entering the silicon. A single charged particle impinges on the substance, ionises it, and causes a current pulse that may or may not cause harm. Protons trapped in space, solar protons, neutrons, and heavy ions from galactic cosmic rays are significant sources of SEE exposure.

Single Event Upset and Latchup:

When a charged particle collides with a substance, it produces a transient pulse that causes soft errors known as Single Event Upsets (SEU). This short pulse can change the status of a memory cell. The impacts of SEUs are device-specific and depend on the impact of the erroneous information in the system. A trans sient pulse in a combinational logic or analog-to-digital converter caused by a charged particle impact may indicate a possible SEU, depending on the functionality of the circuit. A transient pulse, on the other hand, will constitute a SEU since the transient current pulse will change the value of the memory cell. The influence on the SEU system is determined by the nature, location, and design of the effect. Because SEE has a functional impact on a device, functional analysis allows for the evaluation of impacts. Instead of analysing the design by box or physical subsystem, it is analysed by intended usage. Functions are classified into "criticality classes," or SEE severity divisions. The most common hard fault is the Single Event Latchup (SEL), which occurs as a result of a short between ground and power and permanently impacts functioning. Single Event Latchup (SEL) is a potentially dangerous event involving parasitic circuit components. During a SEL, the device current exceeds the maximum allowable for the device. If power is not turned off, the device will eventually be harmed by thermal action.
A micro latchup happens when the device current is greater than the maximum allowed but less than the recommended maximum. In this case, a power reset is also required to return the gad to its original state. When one of these parasitic transistors is engaged by a spurious current spike, such as that induced by a powerful cosmic ray, the other one is activated, resulting in

a circuit with significant positive feedback. This is referred to as latchup. As a result, the circuit fully activates, causing a short across the device until it burns out or is turned off.

1.3 Objectives

Content-Addressable Memory (CAM) is used because of its special capacity to allow quick searches based more on content than specific addresses.Compared to conventional memory structures, CAM works well in situations where it is not possible to determine the search key, allowing for parallel searches.More elaborate and procedural objectives in order are as followed:

1. Analyze different CAM architecture.

2. To model the double exponential current pulse(DECP) in Cadence.

3. To study the impact of single-event upset on CAM.

4. To determine the threshold of DECP which causes single event upset

1.4 Literature survey

1.Low Energy Metric Content Addressable Memory (CAM) with Multi Voltage Matchline Segments.
A specific kind of memory known as Low Energy Metric Content Addressable Memory (CAM) with Multi Voltage Matchline Segments maximizes both power usage and retrieval and search performance.With CAM memory, data can be directly retrieved based on its content instead of its address, which speeds up specific tasks[3]. By using various voltage levels inside the memory's circuitry, Multi Voltage Matchline Segments increase the efficiency of this memory. It reduces power consumption during search operations by using multiple voltage segments, making sure that only necessary memory is used when looking for data. The result presents a promising option for power-efficient computing systems where energy optimization is critical because it not only lowers energy consumption but also increases the

memory's overall speed and efficiency.

2.Content Addressable Memory—Early Predict and Terminate Precharge of Match-Line

This paper probably refers to a theory of study that aims to maximize Content Addressable Memory's (CAM) effectiveness. This strategy probably focuses on optimizing the match-line precharge procedure in CAM systems. In order to compare stored data with incoming search data, match-lines are essential in CAM. In order to enable the prompt termination of precharge cycles upon the prediction of a match or mismatch, the suggested approach may use predictive algorithms or techniques for predicting match results early in the process[4]. This technique seeks to enhance the memory system's overall speed, energy economy, and performance by terminating unnecessary precharge cycles.It's probably an attempt to implement advanced methods to improve CAM's precharge processes, which could result in quicker and more effective memory retrieval.

3.Precharge-Free, Low-Power Content-Addressable Memory

Parallel lookup/search hardware is called content-addressable memory (CAM). Although it requires a lot of power, the parallel search scheme promises a fast search speed. Applications requiring high search speed and low power consumption are best suited for parallel NOR- and NAND-type matchline (ML) CAMs, respectively.Because the NOR-type ML CAM requires a lot of power, many reported designs aim to reduce that power consumption[5]. The short-circuit (SC) current that the NOR-type ML experienced during its precharge phase is reported and examined here. A unique precharge-free CAM is also suggested here. The disadvantages of the SC current in the NOR-type CAM and the charge sharing in the NAND are absent from the suggested CAM.A considerable decrease in the energy metric was shown by postlayout simulations using a 45-nm technology node:93 percent and 77 percent less than NOR- and NAND-type CAMs, respectively. To verify the stability of the suggested precharge-free CAM, a 500-run Monte Carlo simulation was run.

4.Content-Addressable Memory System Using a Nanoelectromechanical Memory Switch

The paper discusses a Content-Addressable Memory (CAM) system utilizing nanoelectromechanical memory switches. The system involves the use

of nanoelectromechanical devices as memory switches, providing a novel approach to content-based addressing in memory systems[6]. The authors explore the potential of this technology for CAM applications, emphasizing its advantages and contributions to the field.

1.5 Problem statement

This project aims to implement and simulate content addressable memory(CAM) and CAM array. Also study the impact of single event upset(SEU) in CAM array.

1.6 Organization of the report

• Chapter 1: Introduction
It includes motivation towards the project, objectives of project, litera ture survey done towards the problem statement, defining the problem statement

• Chapter 2: System design
This chapter includes the High level functional block diagram and description of the functional blocks.

• Chapter 3: Implementation details
This chapter contains detailed information about implementation. It also includes specifications used to design and propose the final system architecture. The algorithm and flowchart give the birds-eye view of the functionalities achieved.

• Chapter 4: Results and Analysis
This chapter includes the conclusion and results of implementation.

• Chapter 5: Conclusion
This is the concluding chapter that includes project closure and epilogue along with the future scope of our project and application to societal context.

Chapter 2

System design

In this Chapter, we infer the High level functional block diagram,description of the functional block diagram.

2.1 Operations of CAM

The operation of Content Addressable Memory (CAM) involves specific steps during both the search and write processes:

Search Operation:

1. Comparison:The CAM simultaneously compares the search data with the content of all entries in parallel.This is a content-based comparison, where the entire content of each entry is compared with the search data.
2. Match Detection:If a match is found during the comparison, the CAM detects it.Matching entries are identified based on the content, and this can happen in a single clock cycle, making CAM suitable for high-speed searches.
3. Output:The CAM outputs the address or identifier associated with the matching entry.This output provides a direct reference to the location of the matching data.

Write Operation:

1. Data Input:During a write operation, new data along with an associated tag or identifier is provided as input.
2. Write to Memory:The new data is written directly into the CAM memory array.Each entry stores both data and its associated tag.
3. Storage:The written data is stored at the location determined by its

content.CAM allows for random write access, meaning new data can be written to any location without affecting existing entries.

Types of CAM
It is categorised into two types
1. Binary Content Addressable Memory (BCAM)
2. Ternary Content Addressable Memory (TCAM)

1.Binary Content Addressable Memory (BCAM):
Binary Content Addressable Memory (BCAM) stores and retrieves binary data, which is normally made up of 0s and 1s. Each memory cell in BCAM compares an entire binary search word against stored binary words[7]. It is intended for situations requiring exact binary pattern matching. BCAM is widely used in networking devices, databases, and other situations where perfect binary matching are required for efficient data retrieval. Its simple matching method makes it suited for applications with stringent binary patterns, offering high-speed and reliable content-based addressing. The fig 2.1 shown in binary content addressable memory[6].

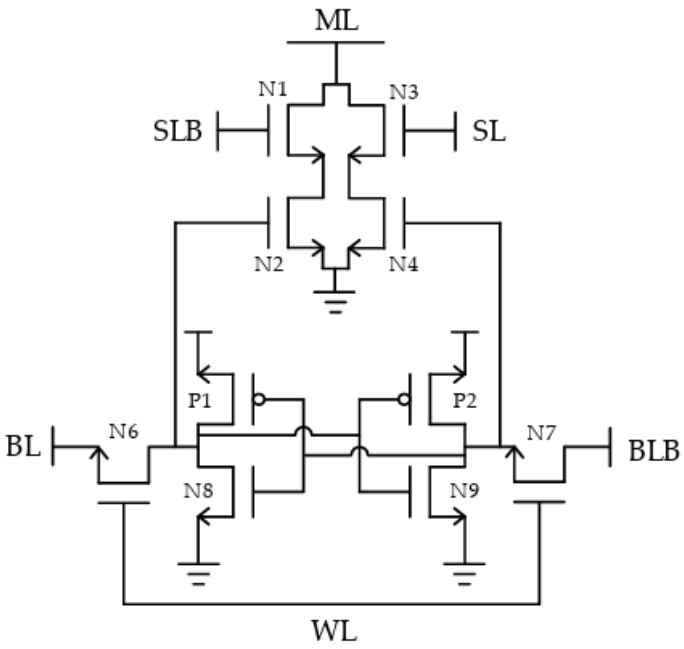


Figure 2.1: Binary content addressable memory

2.Ternary Content Addressable Memory (TCAM):
TCAM extends the capabilities of BCAM by allowing each memory cell to store one of three values: 0, 1, or X "don't care" status. TCAM's increased flexibility makes it appropriate for applications where some bits in the search key may not

be important for matching. TCAM may execute partial matches, allowing it to accommodate situations in which individual bits in the search key can have numerous values[7]. TCAM, which is commonly used in networking routers for fast variable-length prefix matching, provides adaptability in handling varied search criteria, making it useful in cases requiring more complex content-based addressing. The fig 2.2 shows Ternary content addressable memory[6].

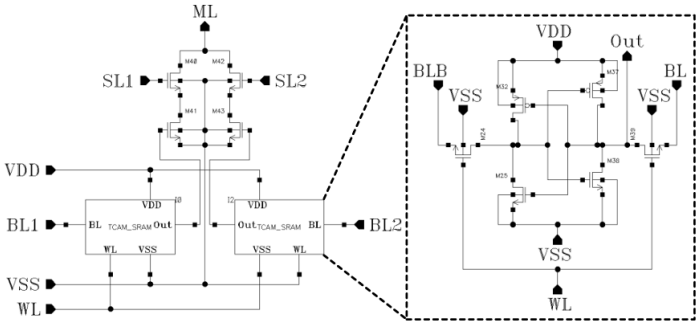


Figure 2.2: Ternary content addressable memory

2.2 Functional Block Diagram

Block diagram of CAM array is shown in fig 2.3.

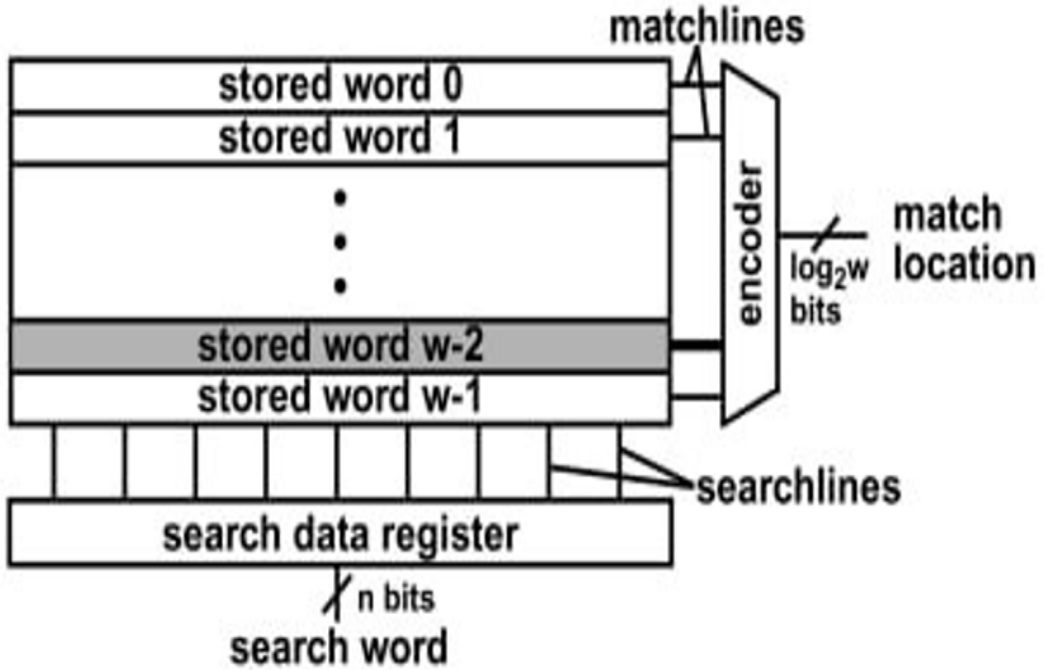


Figure 2.3 : Block diagram CAM array

- The input to the system is the search word.
- The search word is broadcast on the search lines.
- The input data to be searched is given as input in the CAM and loaded into the search data register.
- The input data broadcast by the search register their corresponding bits of data on each SL.
- Match line indicates if there was a match between the search and stored word.
- Encoder specifies the match location.
- If there are multiple matches, a priority encoder selects the first match.

Priority Encoder

Priority encoder is a digital circuit that converts multiple input signals into a unique binary code, representing the highest priority input[4]. Using OR and AND gate we build the 2:4 Priority Encoder . The schematic of priority encoder is shown in 2.4. The truth table of priority encoder is shown table 2.1.

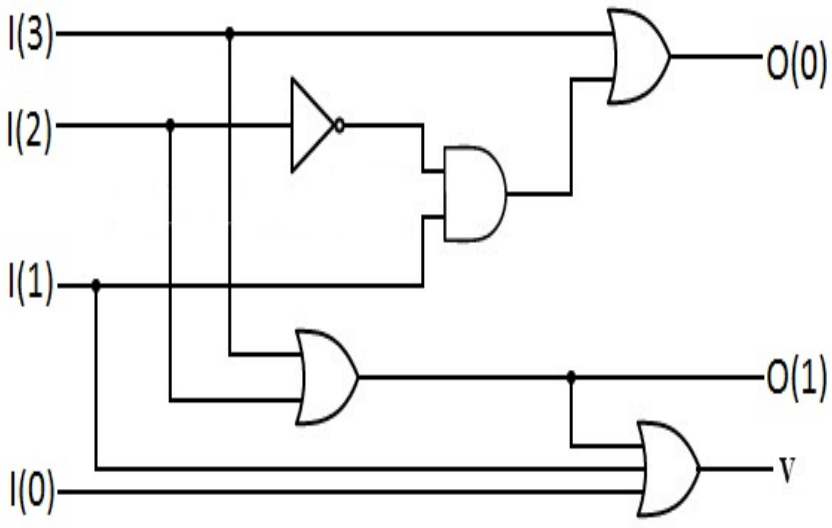


Figure 2.4 : Schematic of Priority Encoder

Table 2.1: 4-to-2 Priority Encoder Truth Table

I3	I2	I1	I0	O1	O0	V
0	0	0	0	x	x	0
0	0	0	1	0	0	1
0	0	1	x	0	1	1
0	1	x	x	1	0	1
1	x	x	x	1	1	1

2.3 Modelling of Single Event Upset

It is critical to test integrated circuits in a severe radiation environment before putting them into operational systems, as doing so reduces the likelihood of failure in future space applications. The following approaches can be used to determine a circuit's radiation sensitivity:

• The analysis of flight data issued from spacecraft operating in the actual environment: space projects,

• Ground testing,

• Fault injection.

1. Space Projects and Testing: Space projects play a vital role in understanding the behavior of devices in space, utilizing them in environments like space stations and research satellites. The initial type of test involves employing these devices for precise space testing of sub-micron generation electronics. This method surpasses the accuracy of ground testing and modeling programs, reducing risks in various applications[7]. The Microelectronics and Photonics Test Bed (MPTB) serves as an illustrative example, focusing on radiation exposure assessment. It has been orbiting since 1998, evaluating the impact of natural radiation on cutting-edge semiconductor and photonic components for a comprehensive understanding of functionality and performance.

2.Radiation Ground Test and SEU Testing: The radiation ground test represents the second category, exposing circuits to particle beams while performing specific tasks. This involves a comprehensive setup, including a particle beam, a defined test methodology, and electronic test equipment. The aim of Single Event Upset (SEU) testing is to calculate the cross-section vs. Linear Energy Transfer (LET) curve by irradiating the device under test with various particle species[9]. Particle accelerators and similar facilities generate the required particle beams for these tests. Additionally, fault injection methodology provides an alternative by injecting bit flips during program execution, aiding research decisions without using electron beams. This strategy involves creating a piece of code (CEU) to induce bit inversion, enhancing efficiency in subterranean tests.

3. Fault Injection Methodology and CEU Code: The fault injection methodology serves as a valuable technique for in-lab testing of electronic circuits, eliminating the need for electron beams. Results from fault injection contribute to research decisions, reducing costs and expediting subterranean tests. This approach involves injecting bit flips randomly during program execution. Crucially, the creation and storage of a specific piece of code, termed CEU (Code Emulating an Upset), play a pivotal role. This code, when executed, induces bit inversion in the chosen target (CEU target)[8]. Activation of an interrupt-like signal initiates CEU code execution if the processor is appropriately configured. The pseudo-random selection of the CEU target and interruption activation instant is facilitated by a temporary external mechanism. The resulting transient current waveform follows a double-exponential model, characterized by a quick rising time and a slow fall time. This is a regularly used approximation analytical model.The nature of DECP is shown in Fig 2.5.

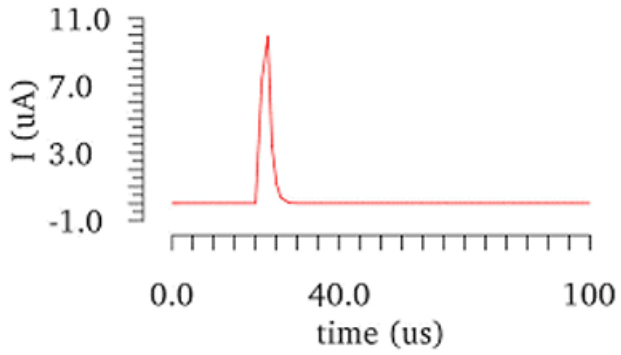


Figure 2.5: Simple content addressable memory array

$$I(t) = \frac{Q_{\text{coll}(e^{-t/\tau_\alpha} - e^{-t/\tau_\beta})}}{\tau_\alpha - \tau_\beta} \tag{2.1}$$

where $Q_{\text{coll}} = 10.8 \times L \times \text{LET}$.

The equation is a representation of the transient current waveform $I(t)$ resulting from ion track charge collection. Let's break down the components of this equation:

1. $I(t)$: This represents the transient current at time t, which is the quantity of interest in this context. It describes how the current changes over time.

2. Q_{coll}: This term denotes the collected charge due to ion track charge collection. It's calculated by multiplying three constants: 10.8, the length of the ion track (L), and Linear Energy Transfer (LET).

- 10.8: A constant multiplier.

- L: The length of the ion track. This parameter influences the amount of charge collected.
- LET: Linear Energy Transfer. It measures the energy transferred to the material per unit length by ionizing radiation. It plays a crucial role in determining the effect of radiation on the material.
3. $e^{-t/\tau_\alpha} - e^{-t/\tau_\beta}$: This part represents the difference between two exponential terms. Exponential terms are often used to model decay or growth processes over time.
- τ_α and τ_β: Time constants associated with the exponential terms. These constants influence the shape and duration of the transient current waveform. Putting it all together, the equation expresses the transient current ($I(t)$) as a function of time (t), taking into account the collected charge (Q_{coll}), and the exponential decay terms related to time constants (τ_α and τ_β).

Methods to overcome the Single Event Upset :

Soft error-tolerant methods fall into two main categories: prevention and recovery. Prevention techniques are implemented during microchip design to safeguard against soft errors, focusing on minimizing radiation sources. Recovery techniques, on the other hand, involve online procedures to address soft errors and ensure chip robustness. Several key strategies are employed:

1. Purification of Fabrication Material:
The reduction of alpha particle emissions in microelectronics is crucial for improving Soft Error Rate (SER) performance. High-purity materials and methods are employed during chip creation, minimizing uranium and thorium impurities to below 100 parts per trillion. Switching to ultra-low alpha packaging materials further reduces alpha emission. Additionally, alternative insulators without boron, replacing BPSG, help mitigate SER induced by 10B activation by low-energy neutrons.

2. Radiation Hardened Process Technologies: Modifying process technology is another approach to enhance SER performance. This can involve reducing the collected charge (Qcoll) or increasing the critical charge (Qcrit). Strategies include employing additional well isolation, such as triple-well or guard-ring structures, to hinder the funnelling effect and decrease the chance of parasitic bipolar collecting routes.

3. Redundancy in Design:
Redundancy is a fundamental design strategy to enhance system reliability

while optimizing time, space, or both. Traditional triple modular redundancy (TMR) with a majority voter remains a common practice, ensuring a reliable system through duplicated components.

4. ECC and Parity for Memory Protection:
Memory, particularly in large sizes, is more susceptible to ionized particles. To secure memory, including parity bits in each memory word is a straightforward method. A parity generator computes parity bits during write operations, and checking the parity code during read operations helps identify errors resulting from particle strikes affecting a single bit in a memory word.

Chapter 3

Implementation details

In this Chapter, we infer the detailed information about implementation. It also includes specifications used to design and propose the final system architecture.

3.1 System architecture

CAM—early predict mismatch of the ML to terminate the precharge.
The architecture of CAM array is shown figure 3.1[5]. Traditional NOR CAM precharges all the MLs (ML1 to MLm) when Pre signal is low and evaluates hit/miss of the search data when Pre goes high. Only the matching ML holds the charge to denote hit and remaining m-1; MLs drain their charge to denote miss. This brief reduces the voltage swing of the mismatching MLs to improve the CAM performance[4].It is unnecessary to charge the mismatching MLs to full swing level, since those MLs have to be discharged in the evaluation phase. Unlike conventional CAM architectures, which during the precharge phase merely charge the MLs, the proposed CAM also predicts the MLs that would mismatch early in the precharge phase. NOR and NAND CAM cells are the basic building elements of CAM architecture. NOR CAM is faster and less power efficient than NAND CAM. CAM constructed with NAND cells have charge sharing problems, and thus, they are not preferred by designers. As shown in Fig. 3.1, the proposed CAM is built with NOR CAM cell, and it creates a path between the nodes ML and MLP when any of the bits in the ML mismatches[5].

MLs are precharged through a precharge controller (inset in Fig. 3.1). The proposed CAM design dynamically varies the precharge time, so as to stop precharging of the mismatching MLs to full level. Pre is a fixed width precharge signal and CPre is a dynamically varying precharge signal. If the

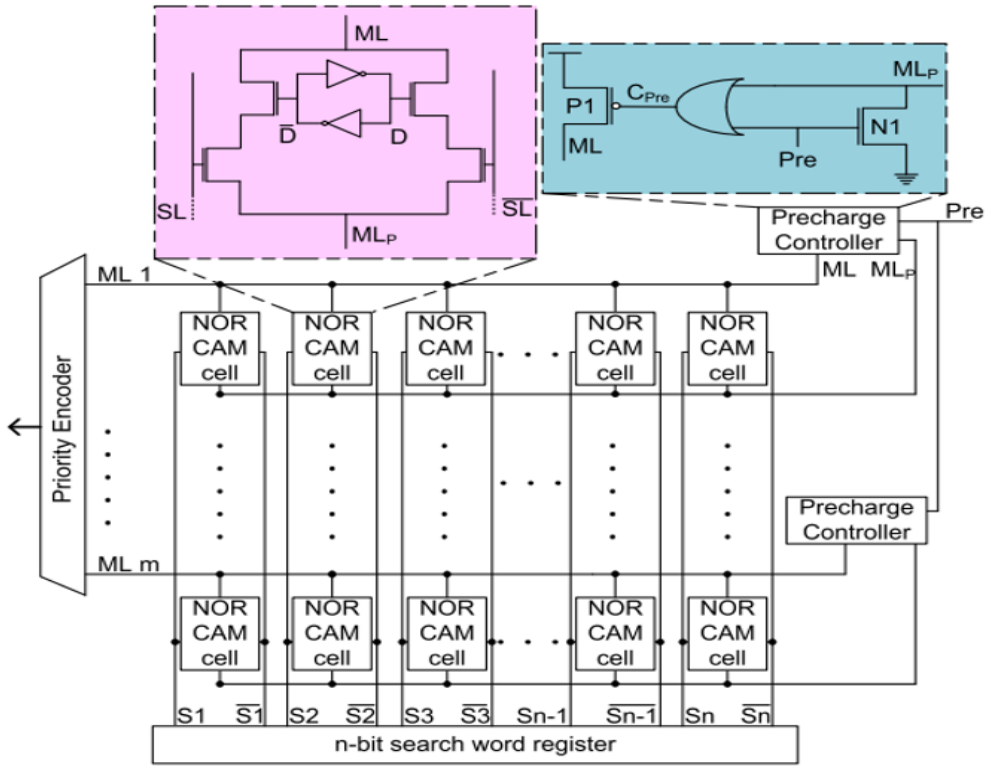


Figure 3.1: CAM—early predict mismatch of the ML to terminate the precharge.

search data mismatches with the word connected to ML, a path between the nodes ML and MLP is created. When the MLs start to precharge, node MLP gets charge through the mismatching XOR circuit of the CAM cell from the node ML. As node MLP reaches to threshold value of the parallel connected nMOS in the OR gate, CPre starts rising to halt ML from getting further charge[4].This reduces unnecessary charging of the mismatching ML by at least 45 percent of normal swing level. Since search delay directly depends on time taken to drain the mismatching MLs in the evaluation phase, the reduced voltage swing level on the mismatching MLs boosts search speed. During evaluation, Pre signal goes high to drain the ML (and node MLP) through MOS N1 to ascertain the mismatch. In the case of a match, nodes ML and MLP remain disconnected to replicate the pre-signal on CPre. The proposed CAM architecture charges ML to full swing level only if the search data matches the stored word.

Low Energy Metric Content Addressable Memory (CAM) with Multi-Voltage Matchline Segments.

CAM architecture is shown in fig 3.2. A hardware lookup table that conducts fast searches in a single clock cycle is called content addressable memory (CAM). Capacitive matchlines (MLs) are charged and discharged more frequently when search data is compared in parallel with all collected data [3]. We segment an ML and a wordline here.Improved energy metric is achieved by precharging the ML segments to varying voltage levels for the first time as reported. A low-voltage source is used to precharge one of the sub-ML segments in order to lower the power consumption related to ML. When the three segments line up, only then will the main Match Line discharge. In order to minimise power consumption without compromising search speed, careful voltage scaling is implemented in Match Lines where switching activity is high[4].

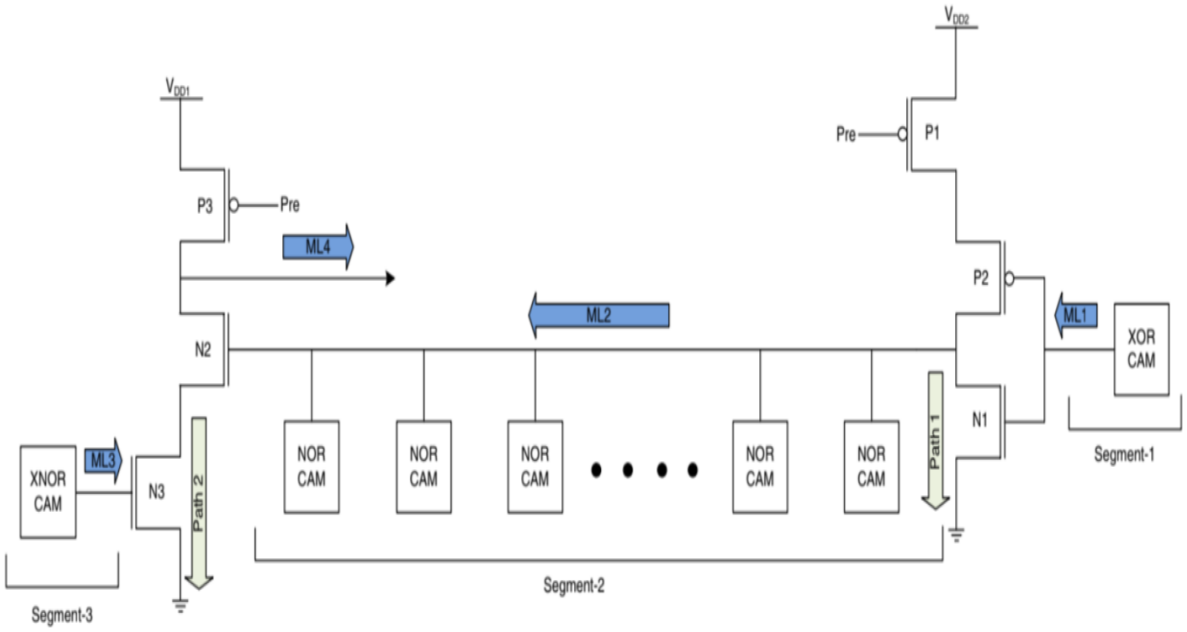


Figure 3.2 : Dynamic voltage matchline in the proposed CAM architecture. The figure depicts a single wordline's architecture, which must be repeated an equal number of times.

An array of CAM cells is usually used to build CAM. CAM cells use logic to compare the stored data with the search input and an SRAM structure to store data. In CAM, a match is indicated by keeping the high state on

the specific ML that matches the stored word with the search word; the remaining miss MLs are then released to the low state, or vice versa[3]. The CAM cell types utilised in our suggested architecture are briefly discussed in this section along with their comparison logic.

3.2 Implementation Of Different Content Addressable Memory Cells :

1) Precharge based Content Addressable Memory :

CAMs have three modes: write, read, and search. They operate in the same manner as SRAM s in the write and read modes. For example, to store a '1'in a memory cell, a'1' is written to the BL, and a high signal is applied to the WL. Here, the access transistors N6 and N7 are switched on, and the data written to the BL are stored in the cell. When a low signal is supplied to WL, the access transistor goes off, and a circuit comprised of two inverters saves[4]. To read the bit stored in the SRAM, a high signal is applied to the WL while the BL is precharged. If '0' is stored, BL is discharged to ground (GND) and indicates a low value. If "1" is stored in SRAM, the precharged high value is maintained.

In the CAM search operation, both search lines (SL, SLB) are precharged with GND, and the ML is precharged with the supply voltage (VDD) value. The data value being searched for is written to the SL. If the data value being searched for, using the N1-N4 transistors, and the data value stored in the SRAM are found to be the same, the pull-down path is kept 'off', and the ML has a high value, indicating a 'match'. Conversely, if the value being searched for and the stored data value differ, one of the pull-down paths connects the ML to GND and the ML is discharged to a low state, indicating a 'mismatch'.

In conventional CMOS-based CAMs, a precharge circuit is used to reduce the delay, as shown in figure 3.3. When the BL or ML voltage decreases in the precharged state during an operation, owing to the precharge circuit[4], the delay problem can be solved by using a sense amplifier to detect small changes.

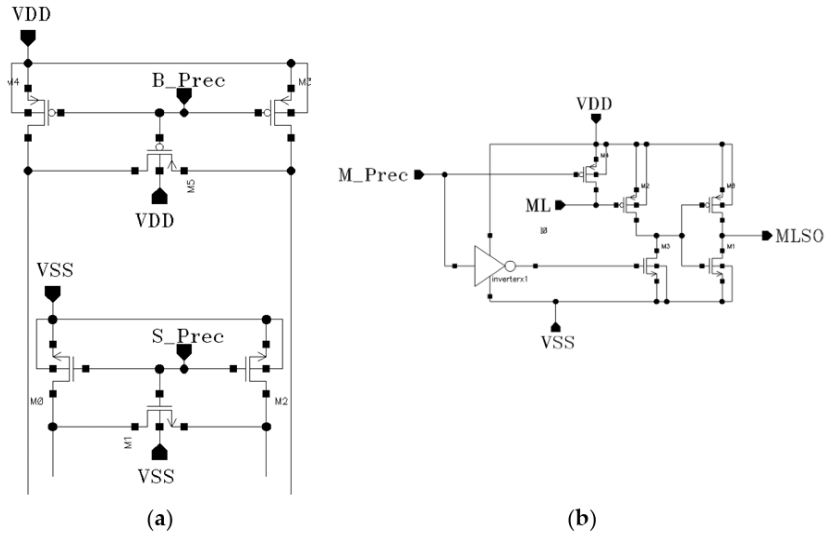


Figure 3.3 Precharge circuit of (a) bit line (BL) and search line (SL); and (b) match line (ML):

In addition, if the SL precharge is used, the two NMOSs connected in series in the matching circuit are turned off before a match operation is performed. Hence, the pull-down path that connects the ML to GND is blocked to prevent a discharge[4]. In addition to these tactics, studies have been conducted on various methods to reduce power consumption; for example, a precharge-free CAM circuit that eliminates the precharge circuit to reduce power consumption when a mismatch occurs [10] or a CAM circuit using an AND gate that yields "1" when all bits are '1" and yields '0', if even one bit does not match. A typical CMOS-based BCAM uses one SRAM to store a value of '0" or 1". A schematic diagram of the CMOS-based BCAM single-bit cell is shown in figure 3.4[6].

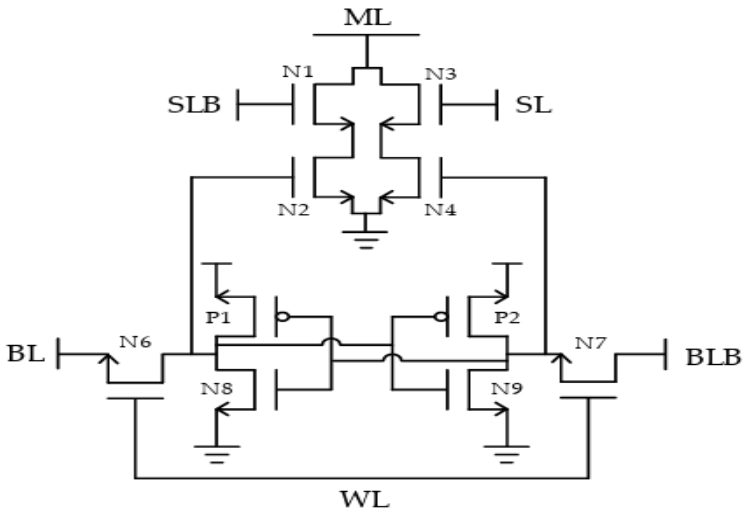


Figure 3.4 : Schematic of CMOS based BCAM cell

The working for the CMOS-based BCAM cell are summarized in table 3.1

Table 3.1: Truth table for BCAM cell

Q	QB	N2	N4	SLB	SL	N1	N3	ML
0	1	OFF	ON	0	1	OFF	ON	0
0	1	OFF	ON	1	0	ON	OFF	1
1	0	ON	OFF	0	1	OFF	ON	1
0	1	OFF	ON	1	0	ON	OFF	0

Simulation results of BCAM is shown in fig 3.5 :

Figure 3.5:Simulation results of BCAM

2)NOR based Content Addressable Memory:

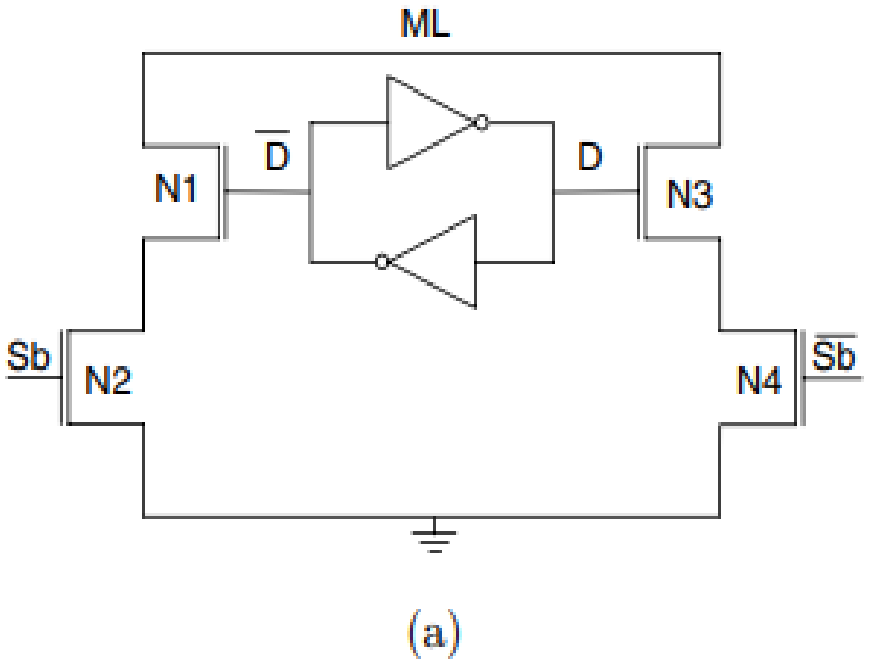


Figure 3.6 : NOR CAM Schematic

CAM has two states: precharge and evaluation.All of the MLs will be charged during the precharge phase[3]. The MLs either hold onto or release their charge while in the evaluation state, contingent on the type of CAM cell and the match/mismatch[4]. The NOR CAM Schematic is shown in fig 3.6. Truth table for NOR CAM is shown in table 3.2.

Table 3.2: Truth table of NOR CAM

D	**DB**	**N1**	**N3**	**SL**	**SLB**	**N2**	**N4**	**ML**
0	1	OFF	ON	1	0	ON	OFF	0
1	0	ON	ON	0	1	OFF	ON	0
0	1	OFF	ON	0	1	OFF	ON	1
1	0	ON	OFF	1	0	ON	OFF	1

Simulation results of NOR CAM is shown in fig 3.7.

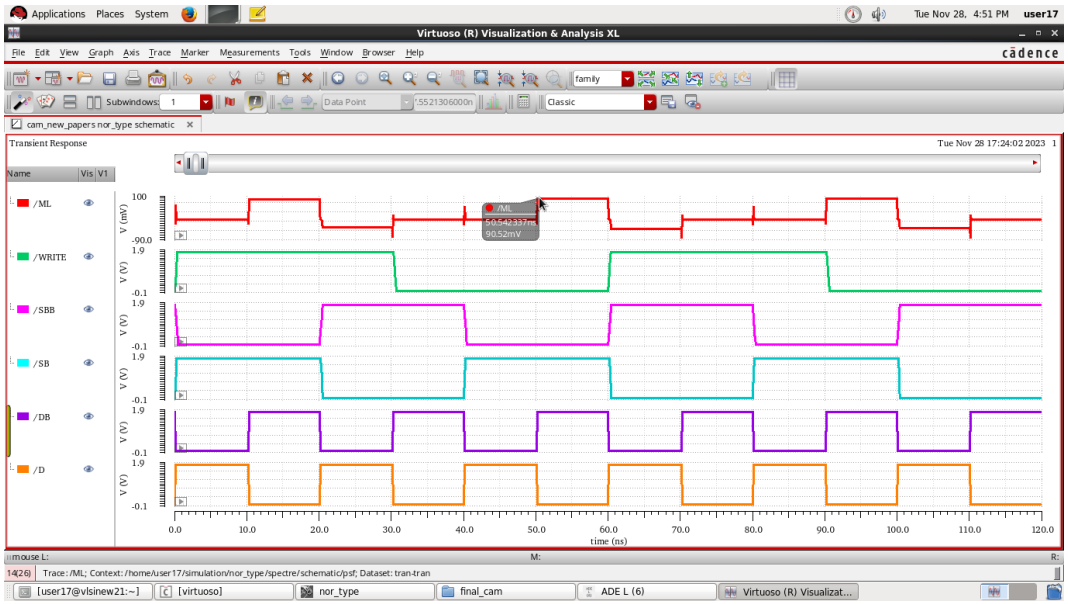


Figure 3.7:Simulation results of NOR CAM

3)EXNOR based Content Addressable Memory:

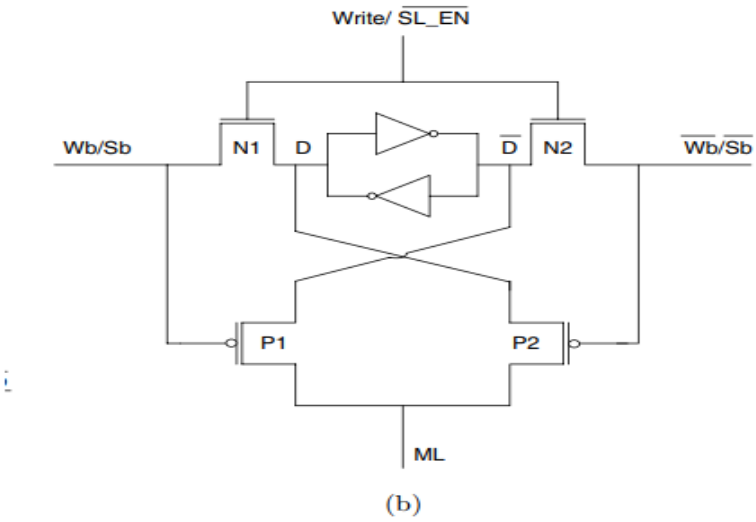


Figure 3.8 : Schematic of EXNOR CAM

In EXNOR type CAM cell, MLs will go high in case of match either through N1 and P2 or N2 and P1. If the stored and search bits do not match then MLs will remain low[3]. The schematic of EXNOR CAM is shown in fig 3.8. The truth table of EXNOR CAM is shown in table 3.3

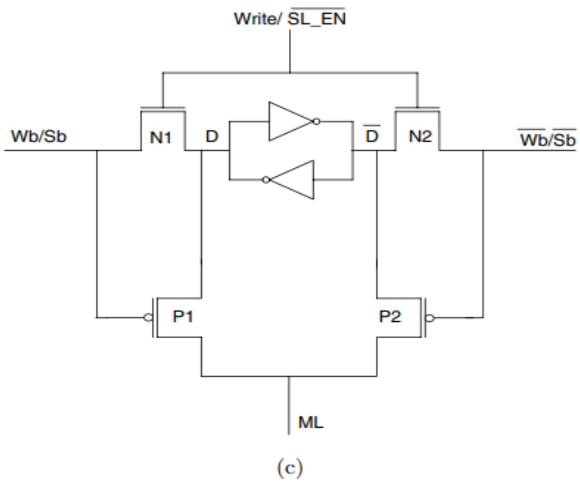
Table 3.3: Truth table of EXNOR CAM

WL	D	DB	N1	N2	SL	SLB	P1	P2	ML
0	1	0	OFF	OFF	1	0	OFF	ON	0
0	0	1	OFF	OFF	0	1	ON	OFF	0
1	1	0	ON	ON	1	0	OFF	ON	1
1	0	1	ON	ON	0	1	ON	OFF	1

Simulation results of EXNOR CAM is shown in fig 3.9.

Figure 3.9:Simulation results of EXNOR

4)EXOR based Content Addressable Memory:



(c)

Figure 3.10 : Schematic of EXOR CAM

In EXOR type CAM cell (Fig. 3.10), MLs will go high in case of mismatch either through N1 and P1 or N2 and P2[3]. If the stored and search bits match then MLs will remain low since no source is available to charge MLs.Truth table of EXOR CAM is shown in table 3.4.

Table 3.4: Truth table of EXOR CAM

WL	D	DB	N1	N2	SL	SLB	P1	P2	ML
0	1	0	OFF	OFF	1	0	OFF	ON	0
0	0	1	OFF	OFF	0	1	ON	OFF	0
1	1	0	ON	ON	0	1	ON	OFF	1
1	0	1	ON	ON	1	0	OFF	ON	1

Simulation results of EXOR CAM shown in 3.11.

Figure 3.11:Simulation results of EXOR

3.3 Modelling Of Double Exponential Current Pulse

We modeled Double Exponential Current Pulse with following specification shown in table 3.5. The simulation results of modeling of DECP is shown in fig 4.2

Table 3.5: Parameter Values

Parameters	Values
ZERO VALUE	0 A
ONE VALUE	1 A
RISE TIME START	10 ns
RISE TIME CONSTANT	5 ns
FALL TIME START	16 ns
FALL TIME CONSTANT	2 ns

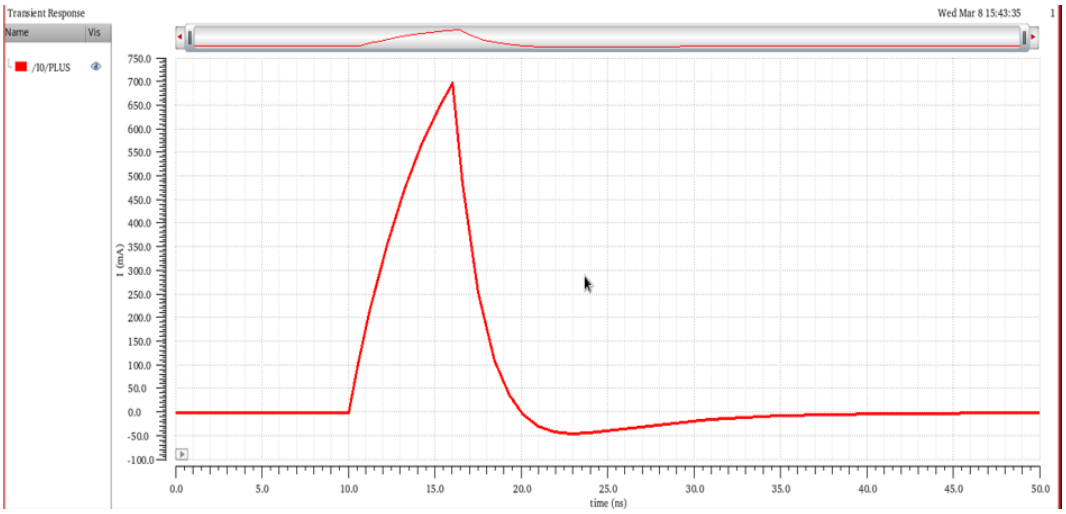


Figure 4.2: Simulation results of DECP modeling

3.4 Algorithm

1.Build different types of CAM cells like NOR,EXOR,EXNOR in Cadence.

2.Simulation of CAM cells.

3.Power and delay analysis of each cell.

4.Construct a array using the cam cells.

5.Simulation of the array.

6.To model the DECP and apply the same to the final circuit.

7.To study the impact of single-event upset on CAM.

8.Delay and power analysis of CAM array.

Chapter 4

Results And Analysis

4.1 Power and Delay Analysis of each cell:

The following table 4.1 compares the delay and power of CAM cells.

Table 4.1: Power and analysis of various CAM cells

Type of CAM cell	**Power(W/Search)**	**Search Delay(ns)**
NOR Based CAM	1.261 W	9.93 ns
EXNOR Based CAM	1.196 W	30.13 ns
EXOR Based CAM	1.207 W	19.65 ns

4.2 Results of CAM array:

We constructed a 4x4 array using NOR type CAM cell. We write data into the array, and we are searching for data in the array. Here we did two different cases to show how decp affects data stored and search mechanisms. The figure 4.1 (a) shows a 4x4 cam array, and figure 4.1 (b) shows a 4x4 cam array with a decp included.

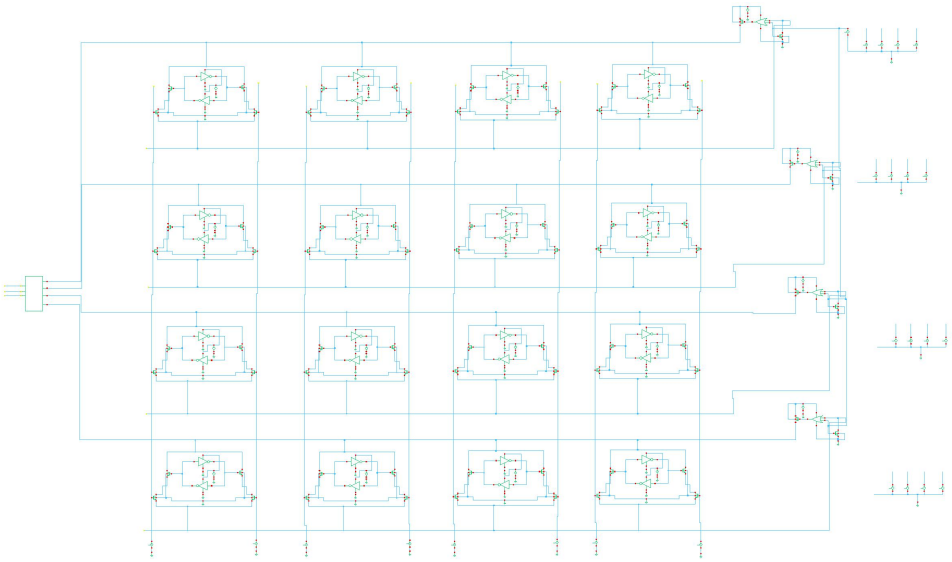


Figure 4.1(a):4x4 cam array Without DECP

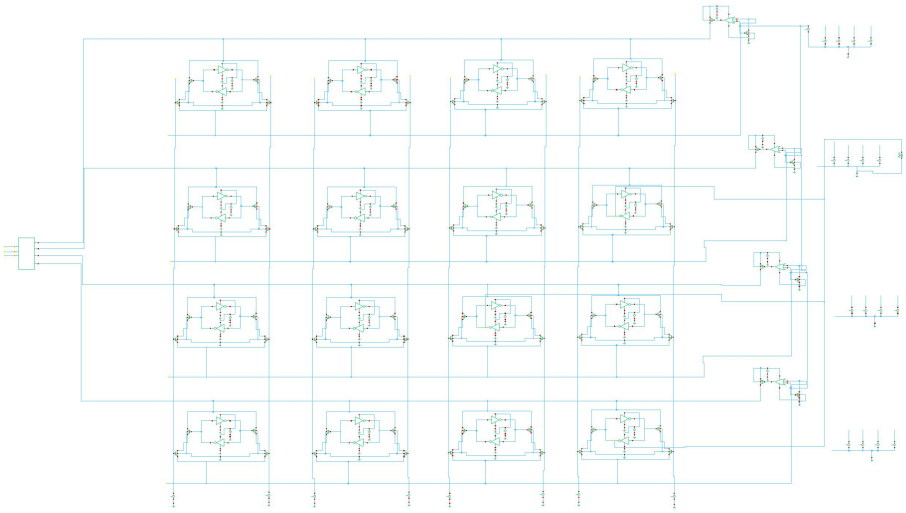


Figure 4.1(b):4x4 cam array With DECP

Case 1 : We stored data and the corresponding results are shown in table 4.2 and 4.3 respectively.The simulation results of the CAM array in fig 4.1 (a) and fig 4.1(b) are shown in fig 4.2 and fig 4.3 respectively. The red circle in fig 4.2 shows the effect of DECP in the CAM array.

Table 4.2: Data stored in array for case-1

Row	**Data**	**Data**	**Data**	**Data**
R1	0	0	0	0
R2	0	0	1	0
R3	0	1	0	1
R4	0	1	1	1

Table 4.3: Truth table of CAM array for case-1

S1	S2	S3	S4	M1	M2	M3	M4	A	B	V
0	0	0	0	1	0	0	0	1	1	1
0	0	0	1	0	0	0	0	0	0	0
0	0	1	0	0	1	0	0	1	0	1
0	0	1	1	0	0	0	0	0	0	0
0	1	0	0	0	0	0	0	0	0	0
0	1	0	1	0	0	0	1	0	1	1
0	1	1	0	0	0	0	0	0	0	0
0	1	1	1	0	0	0	1	0	0	1

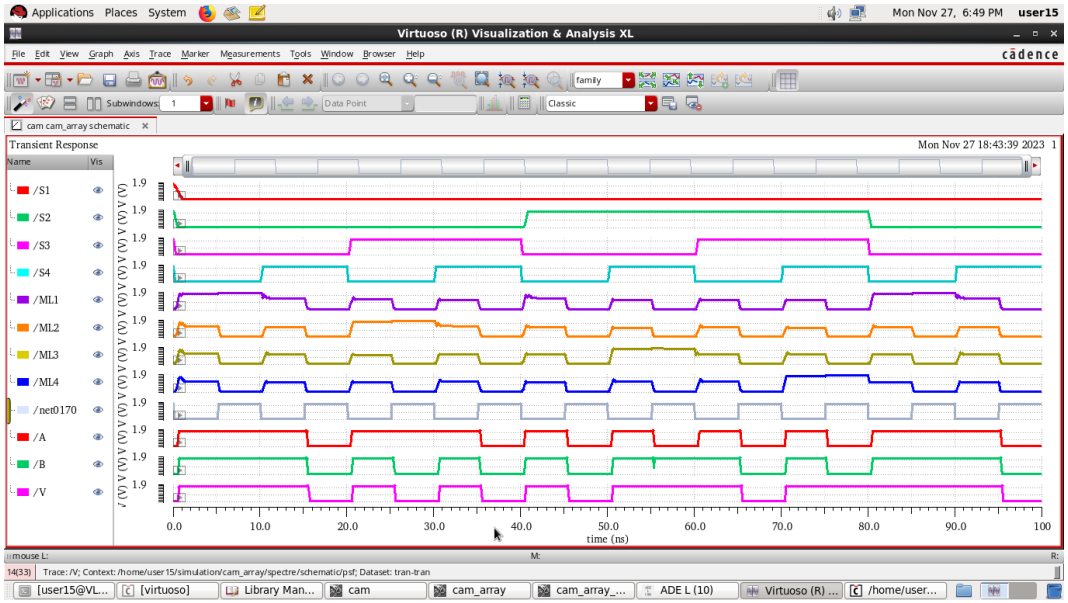


Figure 4.2: Simulation results of CAM array for case 1 without DECP

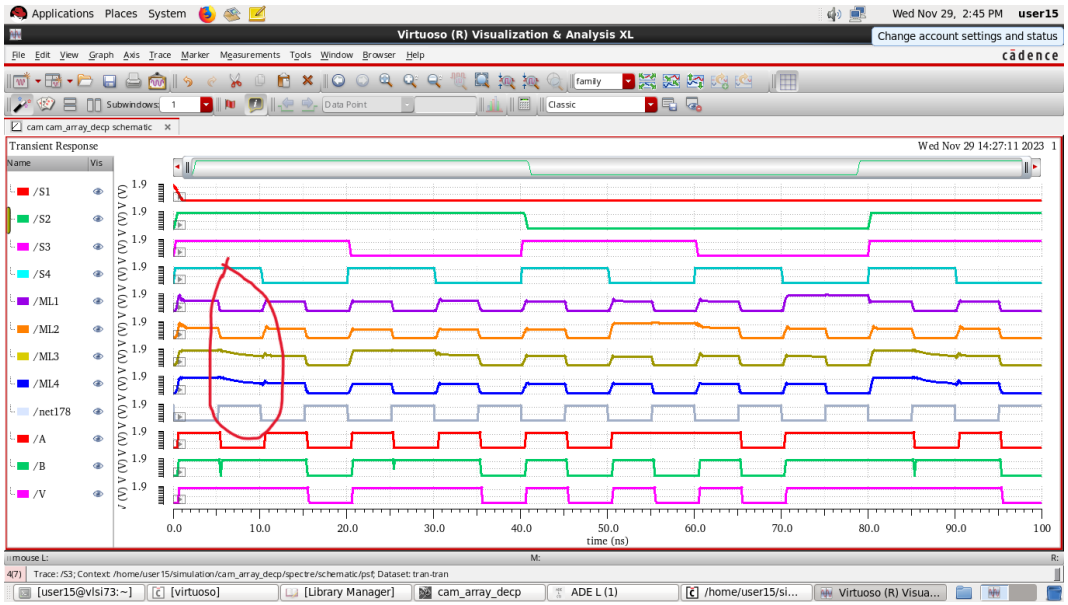


Figure 4.3: Simulation results of CAM array for case 1 with DECP

Case 2:We stored data and Corresponding Results are shown in table 4.4 and 4.5 respectively.

Table 4.4: Data stored in CAM array for case 2

Row	Data 1	Data 2	Data 3	Data 4
R1	1	0	1	0
R2	1	0	1	0
R3	1	1	0	1
R4	1	1	1	1

Table 4.5: Truth table of CAM array for case 2

S1	S2	S3	S4	M1	M2	M3	M4	A	B	V
1	0	0	0	0	0	0	0	0	0	0
1	0	0	1	0	0	0	0	0	0	0
1	0	1	0	1	1	0	0	1	1	1
1	0	1	1	0	0	0	0	0	0	0
1	1	0	0	0	0	0	0	0	0	0
1	1	0	1	0	0	1	0	0	1	1
1	1	1	0	0	0	0	0	0	0	0
1	1	1	1	0	0	0	1	0	0	1

The results of cam array in fig 4.1 are shown in fig 4.4 and fig 4.5. The red circle in fig 4.5 indicates the effect of DECP in CAM array.

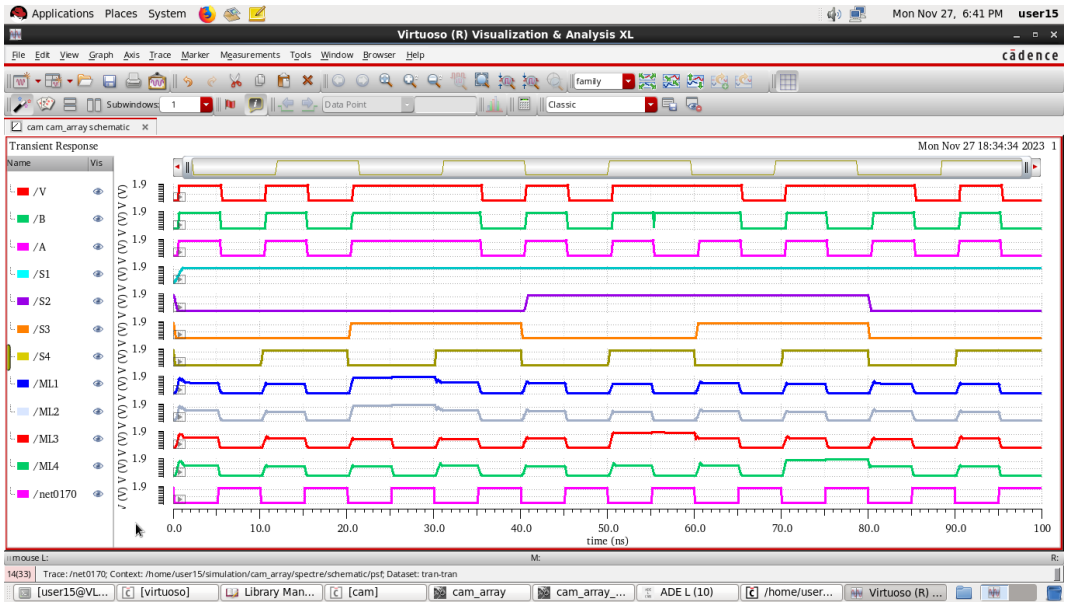


Figure 4.4:Simulation results of CAM array for case 2 without DECP

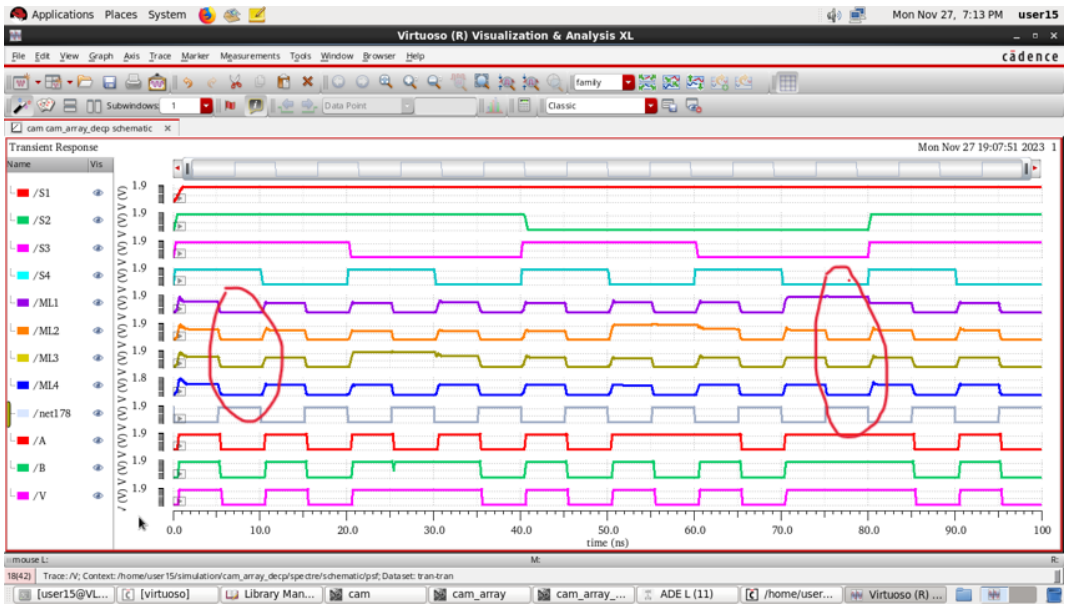


Figure 4.5:Simulation results of CAM array for case 2 with DECP

Results of Architecture shown in Fig 3.2

Truth table for CAM array in fig 3.2 is shown in table 4.6. Simulation results of CAM array in fig 3.2 is shown in 4.6 and 4.7.

Table 4.6: Case Table

Case	Segment-1	Segment-2	Segment-3	ML1	ML2	ML3	ML4
I	Match	Match	Match	Low	High	High	Low
II	Match	Match	Mismatch	Low	Low	Low	High
III	Match	Mismatch	Match	Low	Low	High	High
IV	Match	Mismatch	Mismatch	Low	Low	Low	High
V	Mismatch	Match	Match	High	Low	High	High
VI	Mismatch	Match	Mismatch	High	Low	Low	High
VII	Mismatch	Mismatch	Match	High	Low	High	High
VIII	Mismatch	Mismatch	Mismatch	High	Low	Low	High

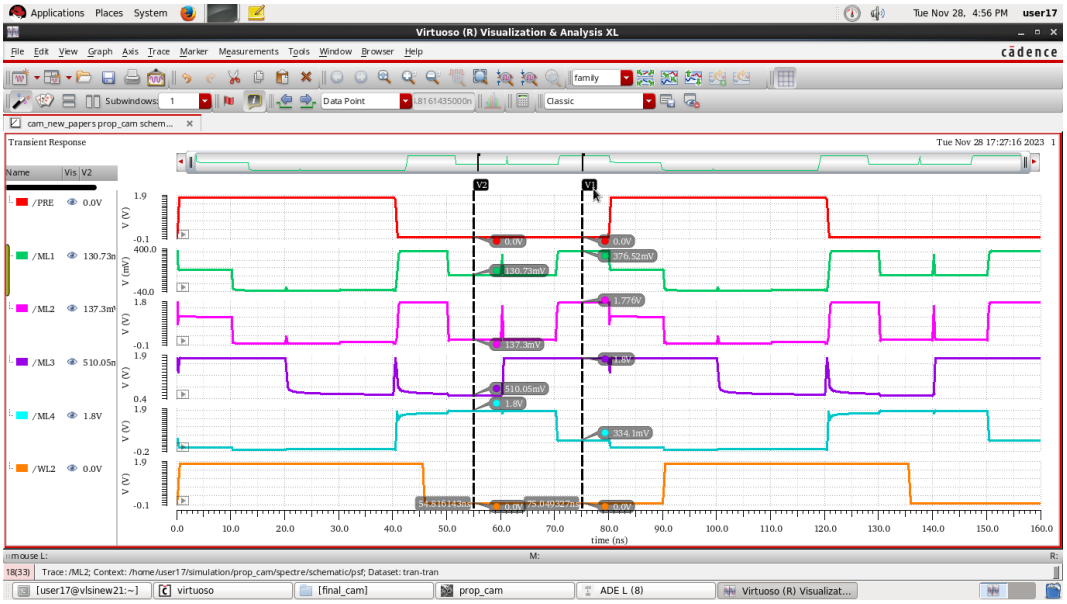


Figure 4.6: Simulation results without DECP

Figure 4.7: Simulation results With DECP

4.3 Power and Delay Analysis of CAM

Table 4.7 and 4.8 shows the power and delay analysis of the two different cam arrays.

Table 4.7: Power and delay analysis of CAM array(fig 3.1)

Match lines	Power(mW/Search)	Search Delay(ns)
Match-Line 1	814.6 mW	20.64 ns
Match-Line 2	681.1 mW	5.96 ns
Match-Line 3	672.7 mW	17.54 ns
Match-Line 4	672.4 mW	12.65 ns
Total ML	2840.8 mW	56.79 ns

Table 4.8: Power and delay analysis of CAM array(fig 3.2)

Match lines	Power(mW/Search)	Search Delay(ns)
Match-Line 1	137.7 mW	30.13 ns
Match-Line 2	616.2 mW	9.938 ns
Match-Line 3	663.6 mW	19.65 ns
Match-Line 4	662.7 mW	-
Total ML	2080.2 mW	59.718(60.13 ns)

4.4 Finding threshold value of DECP

When we inject the current pulse into CAM memeory, it alters the data stored in cam array. So this leads to incorrect results in search mechanism. Single event upset in cam array occurs at minimum of 30mA. The event upset is shown in fig 4.8.

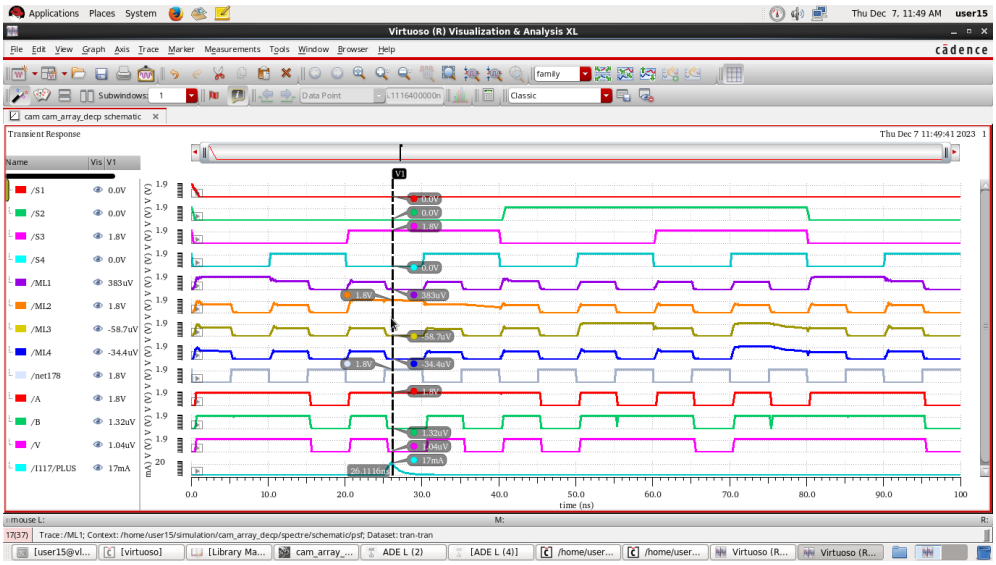


Figure 4.8: Event upset

Chapter 5

Conclusions and future scope

This is the concluding chapter that includes project closure and epilogue along with the future scope of our project.

5.1 Conclusion

In this thorough project on Single-Event Upset (SEU) on Content Addressable Memory (CAM), we methodically tackled many elements of CAM cell design, array construction, and SEU impact analysis. First, we used Cadence to methodically design various CAM cells, including NOR, XOR, and XNOR. We got insight into the behaviour and properties of each cell type through comprehensive simulations.

Following that, we built a CAM array by combining these CAM cells, emphasising the importance of array-level performance. The CAM array simulations allowed us to evaluate its functionality, providing a comprehensive view of the system's capabilities. We modelled the impact of Single-Event Upsets as part of our investigation into potential vulnerabilities, mimicking the occurrence of unanticipated mistakes caused by external radiation.

We measured the energy efficiency and speed of the CAM system by doing power and delay evaluations at both the cell and array levels. Furthermore, the addition of a double exponential current pulse (DECP) improved our understanding of the system's robustness to varied stimuli. Finally, this project not only provided valuable insights into the reliability and vulnerability of CAM in the face of Single-Event Upsets, but also a thorough assessment of its power consumption and delay characteristics, paving the way for future advancements in radiation-hardened memory technologies.

5.2 Future scope

In the future, we would like to analyze the impact of SEU on CAM arrays of various size. Also we would like to propose radiation hardening techniques to protect CAM arrays from Single-event upset

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