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PIN DIAGRAM OF 8051

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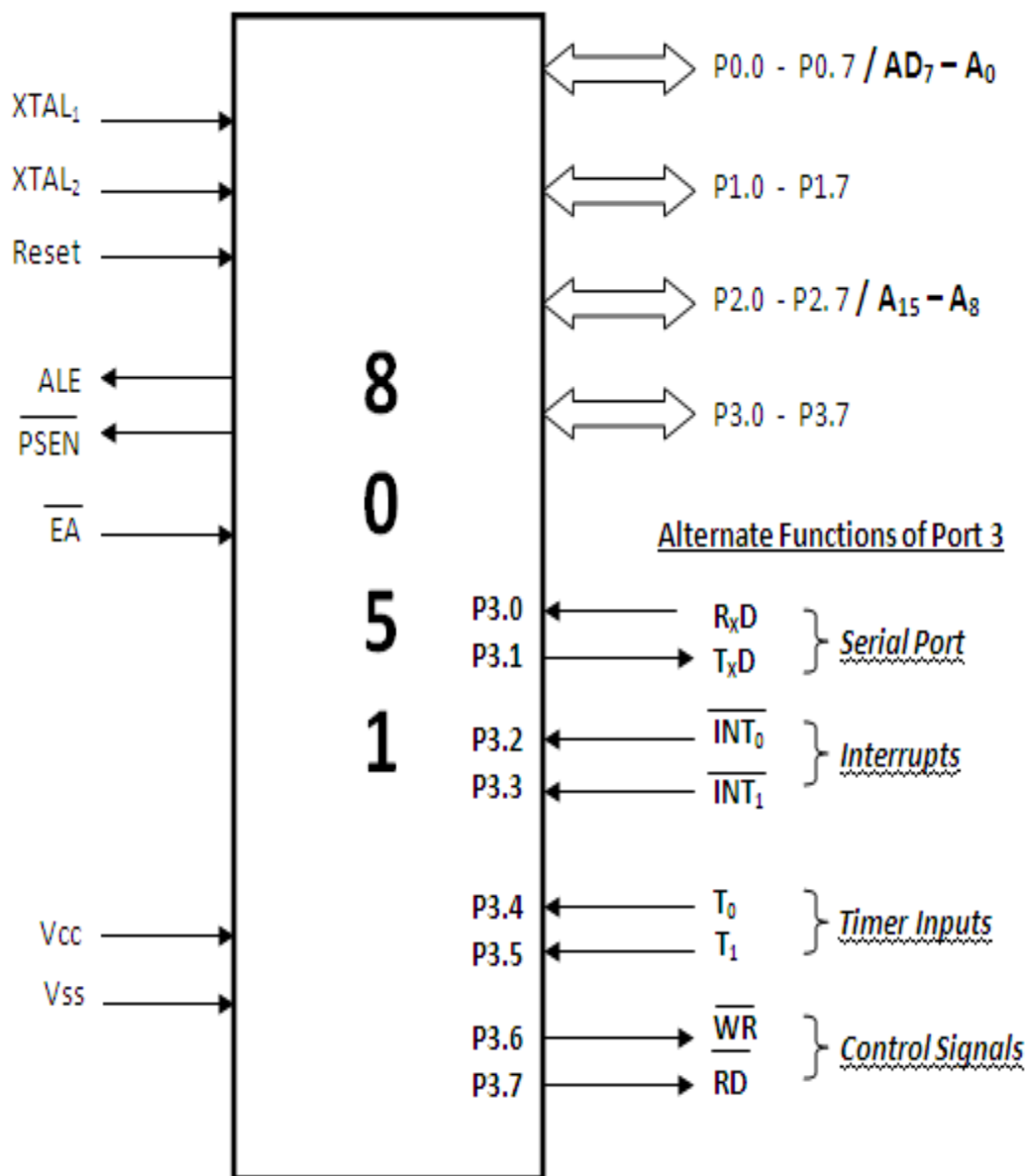E: bharatsir@hotmail.com
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8051 has 40 pins.
The function of these pins is briefly explained as follows.

**XTAL1
&
XTAL2**

These are connected to the **crystal oscillator**.
The **typical operating frequency is 12 MHz**.
In **Serial communication** based applications, the operating frequency is chosen to be **11.0592 MHz**, in order to derive the standard universal baud rates. This will be discussed in detail in the further chapters.

Reset

It is used to **reset** the 8051 microcontroller.
On reset **PC becomes 0000H**.
This address is called the **reset vector address**.
From here, 8051 executes the **BIOS program** also called the Booting program or the monitor program. It is used to **set-up the system** and make it **ready**, to be used by the **end-user**.

ALE
Address
Latch Enable

It is used to **enable the latching of the address**.
The **address and data buses are multiplexed**.
This is done to **reduce the number of pins** on the 8051 IC.
Once out of the chip, address and data **have to be separated** that is called **de-multiplexing**.
This is done by **a latch**, with the **help of ALE signal**.
ALE is **"1"** when the bus carries **address** and **"0"** when the bus carries **data**.
This informs the latch, when the bus is carrying address so that the latch captures only address and not the data.

$\overline{EA}$
Enable External
Access

It decides whether the first 4 KB of program memory space (0000H… 0FFFH) will be assigned to internal ROM or External ROM.
If $\overline{EA}$ = 0, the External ROM begins from 0000H.
In this case the Internal ROM is discarded.
8051 now uses only External ROM.

If $\overline{EA}$ = 1, the External ROM begins from 1000H.
In this case the Internal ROM is used. It occupies the space 0000H… 0FFFH.
In modern **FLASH ROM versions**, this pin also acts as **VPP** (12 Volt programming voltage) to write into the FLASH ROM.

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$\overline{PSEN}$
Program Status Enable

8051 has a **16-bit address bus** ($A_{15} - A_0$).
This should allow 8051 to access **64 KB of external Memory** as 2^{16} = 64 KB.
Interestingly though, 8051 can access **64 KB of External ROM and 64 KB of External RAM**, making a total of 128 KB.
Both have the same address range **0000H to FFFFH**.
This does not lead to any confusion because there are separate control signals for External RAM and External ROM.

$\overline{RD}$ **and** $\overline{WR}$ **are control signals for External RAM.**

$\overline{PSEN}$ **is the READ signal for External ROM.**

It is called Program Status Enable as it allows reading from ROM also known as Program Memory.
Having separate control signals for External RAM and External ROM actually **allows us to double the size of the external memory** to a total of 128 KB from the original 64 KB.

Vcc & GND

These are **power supply** pins.
8051 works at **+5V / 0V** power supply.

P0.0... P0.7

These are **8 pins** of Port 0.
We can perform a **byte operation** (8-bit) on the whole port 0.
We can also **access every bit of port 0 individually** by performing **bit operations like set, clear, complement** etc.
The bits are called **P0.0... P0.7**.
Additionally, Port 0 also has an **alternate function**.
It carries the **multiplexed address data lines**.
A0-A7 (the lower 8 bits of address) and **D0-D7** (8 bits of data) are **multiplexed into AD0-AD7**.
In any operation address and data are not issued simultaneously.
First, address is given, then data is transferred.
Using a common bus for both, **reduces the number of pins**.
To identify if the bus is carrying address or data, we look at the ALE signal.
If **ALE = 1**, the bus carries **address**,
If **ALE = 0**, the bus carries **data**.

P1.0... P1.7

These are **8 pins** of Port 1.
We can perform a **byte operation** (8-bit) on the whole port 1.
We can also **access every bit of port 1 individually** by performing bit operations like set, clear, complement etc. on **P1.0... P1.7**.
Port 1 also has NO alternate function.

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P2.0… P2.7	These are **8 pins** of Port 2.

These are **8 pins** of Port 2.
We can perform a **byte operation** (8-bit) on the whole port 2.
We can also **access every bit of port 2 individually** by performing bit operations like set, clear, complement etc. on **P2.0… P2.7**.
Additionally, Port 2 also has an **alternate function**.
It carries the **higher order address lines A8-A15**.

P3.0… P3.7

These are **8 pins** of Port 3.
We can perform a **byte operation** (8-bit) on the whole port 3.
We can also **access every bit of port 3 individually.**
The bits are called **P0.0… P0.7**.
The various pins of Port 3 have a lot of alternate functions.

P3.0 (**Rxd**) and P3.1 (**Txd**):   They are used to **receive and transmit serial data**.
This forms the **serial port of 8051**.

P3.2 ($\overline{\text{INT0}}$) and P3.3 ($\overline{\text{INT1}}$):   They are external **hardware interrupts of 8051**.
If they occur simultaneously, INTO is by default higher priority.

P3.4 (**T0**) and P3.5 (**T1**):   They are used **timer clock inputs**.
They provide external clock inputs to Timer 0 and Timer 1.

P3.6 ($\overline{\text{WR}}$) and P3.7 ($\overline{\text{RD}}$):   They are used as **control signals for External RAM**.
8051 can access 64 KB External RAM from 0000H to FFFFH..