



PRIORITY MODES OF 8259

Fully Nested Mode (FNM)

It is the **default mode** of 8259.

It is a **fixed priority** mode. (priorities won't change, will remain as it is)

IR₀ has the **highest** priority and **IR₇** has the **lowest** priority.

It is preferred for "Single" 8259. (not cascaded)

Special Fully Nested Mode (SFNM) (not the default mode)

This mode can be **used for** the **Master 8259 in a cascaded configuration**. (main difference)

Its **priority structure** is fixed and is the **same as FNM** (IR₀ highest and IR₇ lowest).

➤ **Additionally**, in SFNM, the **Master would recognize a higher priority interrupt from a slave, whose another interrupt is currently being serviced**. This is **possible only in SFNM**.

In SFNM the master will recognize a new interrupt from a slave whose another interrupt is already being serviced

Rotating Priority Modes

There are **two** rotating priority modes:
Automatic Rotation and Specific Rotation

the moment any interrupt is serviced it automatically becomes the lowest priority and all interrupts below it come up in the order.
this defies "dominance and starvation"

Automatic Rotation Mode

This is a rotating priority mode.

It is **preferred** when **several interrupt** sources are of **equal priority**.

In this mode, **after** a device receives **service**, it **gets** the **lowest priority**.

All other priorities rotate subsequently. ☎ For doubts contact Bharat Sir on 98204 08217

Eg: If IR₂ is has just been serviced, it will get the lowest priority.

Specific Rotation Mode

It is **also** a **rotating** priority mode, **but here** the **user can select any IR level for lowest priority**, and thus fix all other priorities. (only one IR level)

Special Mask Mode (SMM)

Usually 8259 **prevents interrupt requests lower or equal** to the interrupt, which is **currently** in service.

- 2) In **SMM** 8259 **permits interrupts of all levels** (lower or higher) **except** the one **currently** in service.
- 3) As we are **specially masking the current interrupt**, it is called **Special Mask Mode**.
- 1) This mode is preferred when we don't want priority



Poll Mode (polling simply means asking) (Here, polling is the exact opposite of interrupting)

Here the **INT line** of 8259 is **not used** hence 8259 cannot interrupt the **μP**.

Instead, the **μP will give Poll command** to 8259 using OCW3. → asks microprocessor weather there are any interrupts or not

In **return**, **8259 provides a Poll Word** to the **μP**.

The Poll Word **indicates the highest priority interrupt**, which requires service.

Poll Word

I	x	x	x	x	w ₂	w ₁	w ₀
1 = Valid Interrupt 0 = No valid interrupt					0	0	0 IR0
					0	0	1 IR1
					0	1	0 IR2
					0	1	1 IR3
					1	0	0 IR4
					1	0	1 IR5
					1	1	0 IR6
					1	1	1 IR7

Level No of the highest priority
interrupt to be serviced

Thereafter the **μP services the interrupt**. For doubts contact Bharat Sir on 98204 08217

Advantage: The **μP's program** is not disturbed. It can be used when the ISR is common for several interrupts. It can be used to increase the total number of interrupts beyond 64.

Drawback: If the polling interval is too large, the interrupts will be serviced after long intervals. If the polling interval is small, lot of time may be wasted in unnecessary polls.

Buffered Mode

In this mode **SP / EN** becomes **low** during **INTA** cycle.

This signal is used to enable the buffer.

EOI – (End Of Interrupt)

When the **μP responds** to an interrupt request by sending the first **INTA** signal, the **8259 sets the corresponding bit** in the In Service Register (**InSR**).

This **begins the service** of the interrupt.

When this bit in the In Service Register is **cleared**, it is called as **End of Interrupt (EOI)**.

EOI Modes:

1) Normal EOI Mode:

Here an EOI Command is necessary. The EOI Command is given by the programmer at the end of the ISR. It causes 8259 to clear the bit from In Service Register. There are two types of EOI Commands:

Non Specific EOI Command:

Here the programmer doesn't specify the Bit number to be cleared. 8259 automatically clears the highest priority bit from In Service Register.

Specific EOI Command:

Here the programmer specifies the Bit number to be cleared from In Service Register.

2) Auto EOI Mode (AEOI):

In AEOI mode the EI command is not needed. Instead, 8259 will itself clear the corresponding bit from In Service Register at the end of the 2nd **INTA** pulse.

DRAWBACK: loses the track of in-service register, because even before the ISR has even started, the corresponding bit has become 0 in the register. it would even entertain the same fucking interrupt instead of discarding it.