Unit - IV

- Bipolar Junction Transistor: Physical operation, operating point, load line, self-bias circuit, single stage CE Amplifier configuration – 4 lectures

- Ideal Op- Amp, inverting, Non-inverting and Unity gain Amplifiers, integrator, Differentiator, Summer/ Subtractor – 4 lectures

Bipolar Junction Transistor (BJT)

- Bipolar Junction Transistor (BJT) is a 3 terminal semiconductor device having 3 layers and 2 junctions
- It can be either n-p-n type or p-n-p type
- Two p-n junction diodes cannot be joined together to form a pnp or npn transistor
- The terminals connected with each of the 3 layers are known as Collector (C), Base (B) and Emitter (E). All these three layers are different in thickness and doping level, hence not interchangeable.

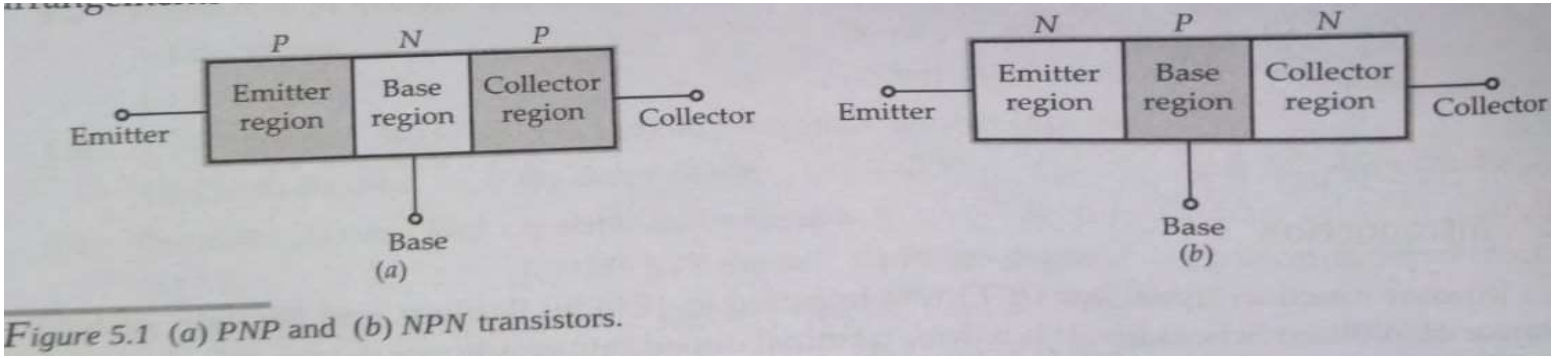


Figure 5.1 (a) PNP and (b) NPN transistors.

Bipolar Junction Transistor (BJT)

- Since Collector and Emitter are of same type semiconductor but not interchangeable. So, in order to differentiate among the two we put an arrow on the Emitter in the direction of p to n always irrespective of npn or pnp transistor.
- For a transistor $I_E = I_C + I_B$ always

	Base (B)	Collector (C)	Emitter (E)
Layer	Middle	Extreme end	Extreme end
Current	Minimum	Moderate	Maximum
Doping Level	Minimum	Moderate	Maximum
Thickness	Minimum	Maximum	Moderate

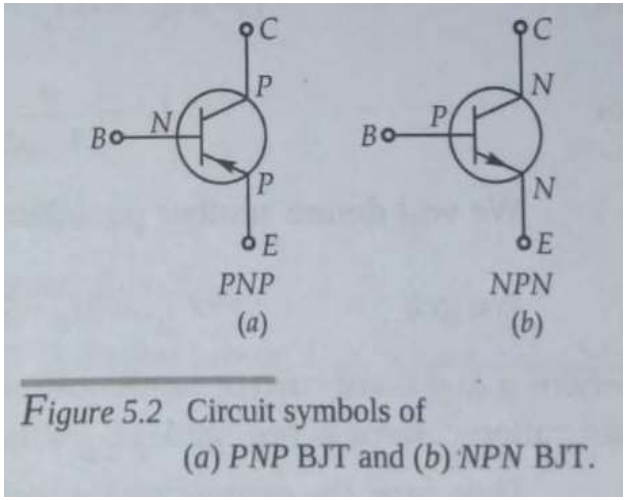


Figure 5.2 Circuit symbols of (a) *PNP* BJT and (b) *NPN* BJT.

BJT: Physical Operation

- A transistor operates in three regions Active, Cutoff and Saturation
- In Active region the transistor acts as an amplifier (Analog Electronics)
- In cutoff region it acts as off switch and in saturation region it acts as on switch. These two states can be understood as corresponding to logic 0 and 1 respectively (Digital Electronics)

BJT: As an Amplifier

5.7 Transistor as an Amplifier

If we compare different configured transistors in Table 5.2, we find that *CE* arrangement is most suited for signal amplification. Figure 5.16 shows the *CE, NPN* amplifier circuit. A dc voltage source (V_{BB}) is applied to the input circuit so that emitter-base (*E-B*) junction operates in the forward biased irrespective of polarity of input ac signal. A dc voltage source (V_{CC}) is connected to the output circuit in such a way that collector-base (*C-B*) junction operates in reverse biased.

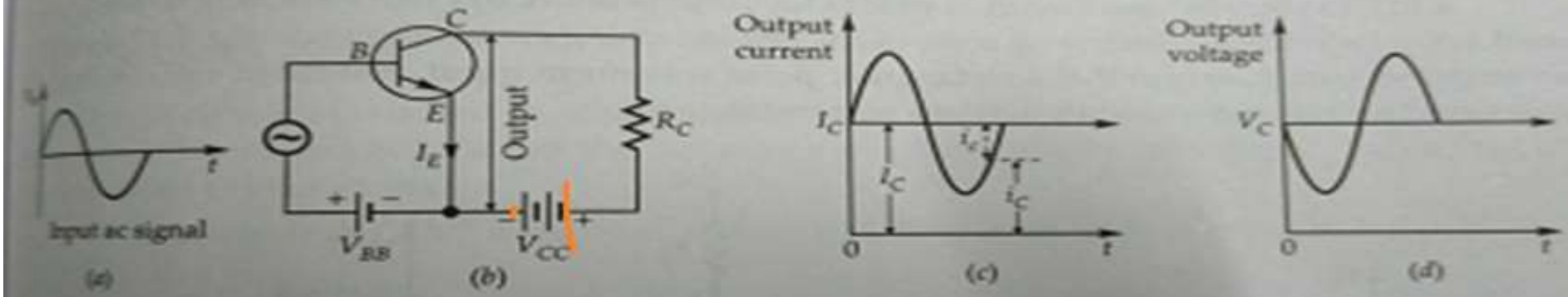
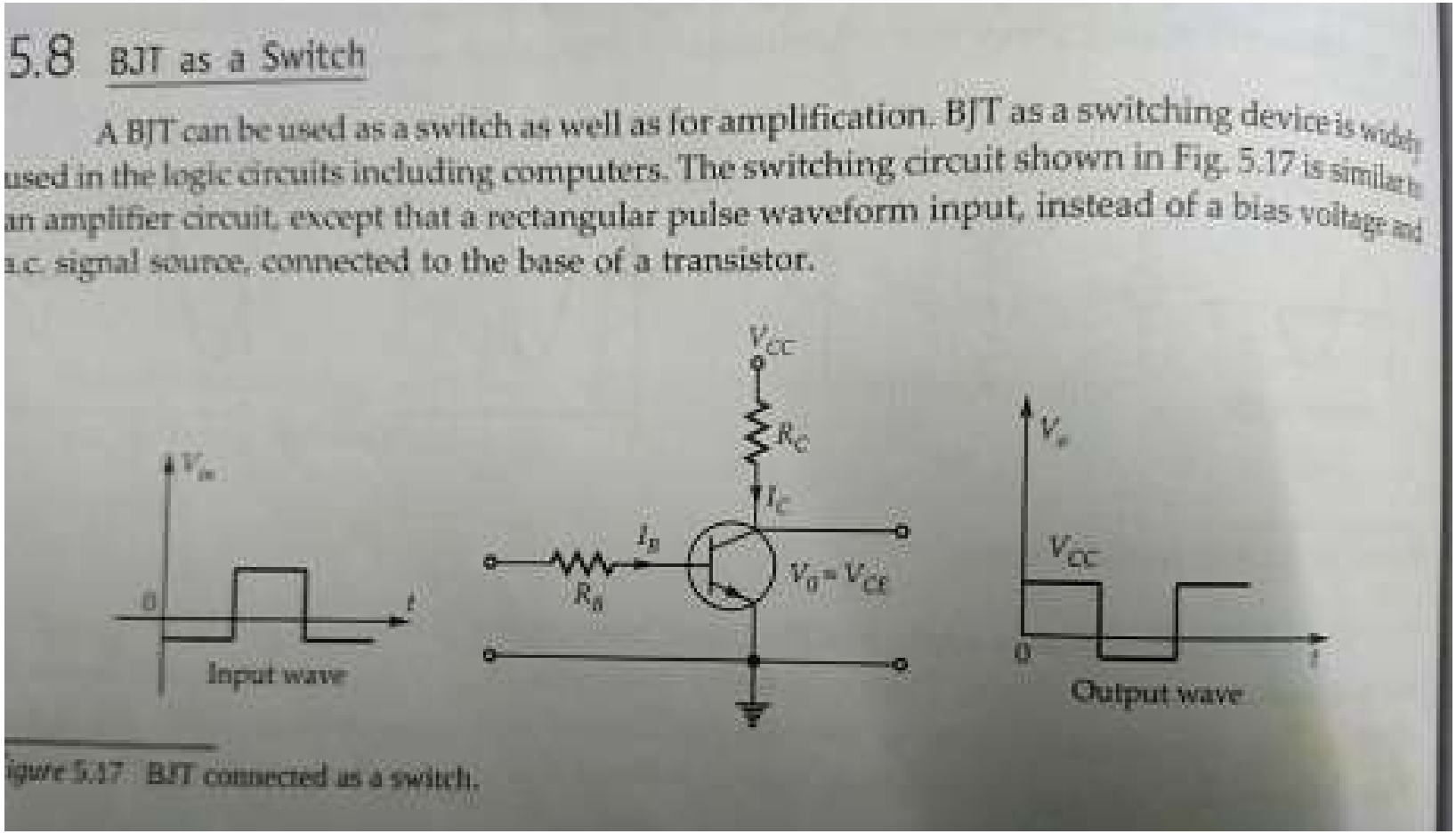


Figure 5.16 *CE NPN* Amplifier circuit.

When ac input signal is applied to the input, base-emitter voltage (V_{BE}) begins to oscillate with the polarity of the signal. During positive half-cycle, V_{BE} is increased which results I_B increases. This causes an increase in the collector current and larger voltage drop will appear across the load R_C. As V_{CC} is constant, output voltage V_{CE} (V_C, as *E* is grounded) decreases.

- In CE mode the BJT acts as an amplifier in the active region

BJT: As a Switch



5.8 BJT as a Switch

A BJT can be used as a switch as well as for amplification. BJT as a switching device is widely used in the logic circuits including computers. The switching circuit shown in Fig. 5.17 is similar to an amplifier circuit, except that a rectangular pulse waveform input, instead of a bias voltage and a.c. signal source, connected to the base of a transistor.

igure 5.17 BJT connected as a switch.

- Here output takes only 2 values V_{CC} or 0 (corresponding to logic 1 & 0) when the transistor is driven to cutoff and saturation states respectively

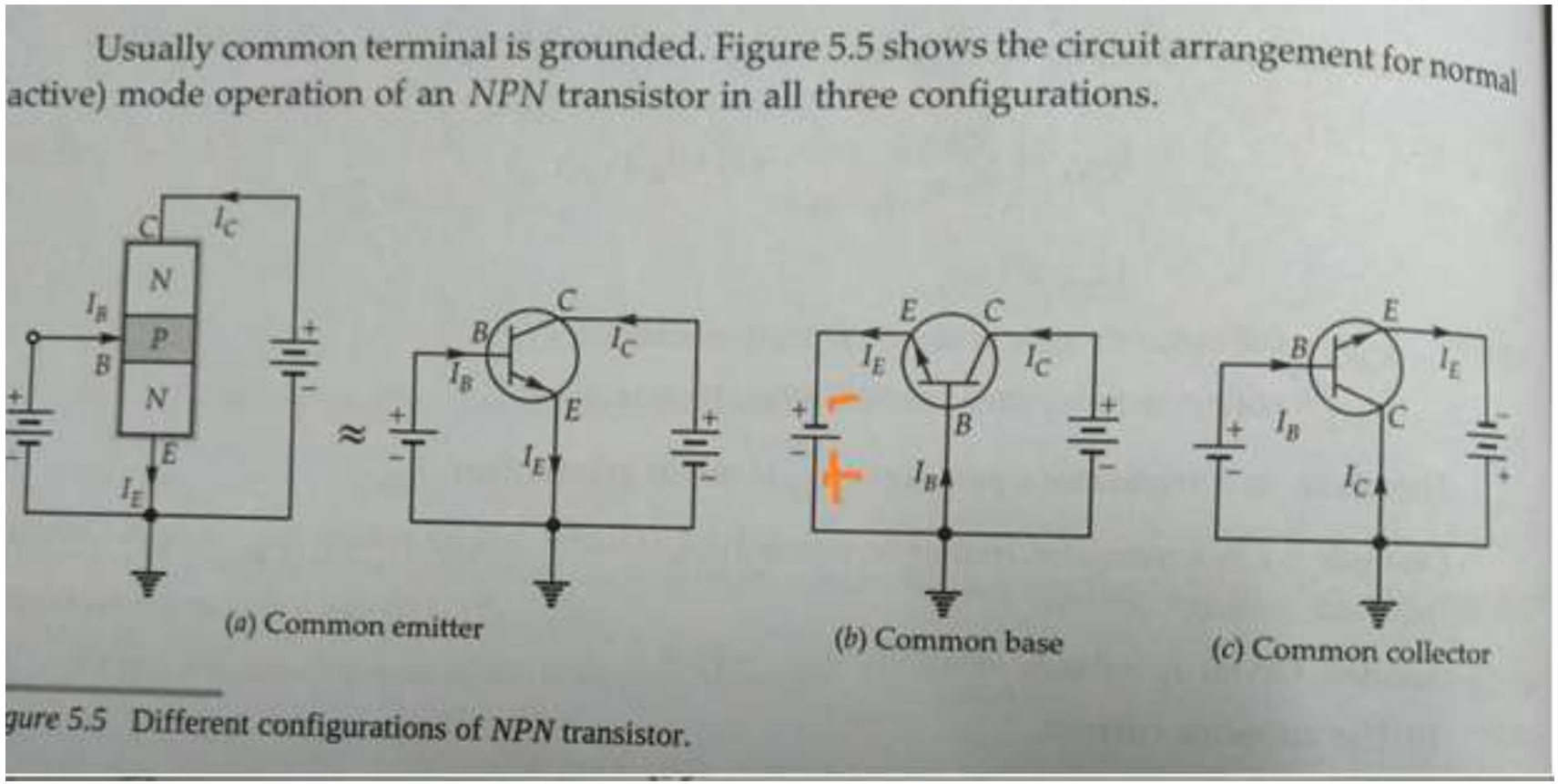
BJT: an Active element & Biasing

- Transistor is an active element as it is able to produce amplified high power replica of the input waveform at its output for a sufficiently long period of time, when operates in active region. It is able to do so by taking power from the DC sources and converting that DC power into the desired AC waveform.
- Connecting suitable DC power supply with desired polarity at the input and output side of Transistor is known as biasing of the Transistor

BJT: Different Operating modes

- Transistor is a 3 terminal device. But we need 4 terminals (2 for input side and another 2 for output side) to make an amplifier circuit. In order to achieve this we need to make one of the terminals of transistor common to both input and output side.
- Hence, a transistor can be operated in three different configurations viz. Common Emitter (CE); Common Collector (CC) and Common Base (CB)
- Out of these 3 modes CE mode is most commonly used. In this mode Emitter terminal is common to both input and output sides. Out of the remaining two terminals base is on input side and collector on output side.

BJT: 3 different Operating Modes



- The input output terminals and the polarity of the DC biases on the input and output sides for the 3 different modes of operation are as shown in the figure above

Transistor Reverse saturation currents

- There are 2 types of transistor reverse saturation currents I_{CBO} and I_{CEO} which flows due to minority charge carriers through the reverse bias junction. The reverse saturation currents flow due to the flow of minority charge carriers. Hence, they are independent of applied voltage and depends on temperature
- I_{CBO} is the reverse saturation current (collector current) flowing from collector to base when the third terminal (emitter) is open circuited. I_{CBO} is the output circuit current of CB mode when input circuit is open circuited.
- I_{CEO} is the reverse saturation current (collector current) flowing from collector to emitter when the third terminal (base) is open circuited. I_{CEO} is the output circuit current of CE mode when input circuit is open circuited.

BJT: current gains & Reverse saturation currents

- The CB configuration current gain is defined as the ratio of output current and input current in CB configuration such that $\alpha = I_C/I_E = 0.98 - 0.99$
- Also, CE configuration current gain is defined as the ratio of output current and input current in CE configuration such that $\beta = I_C/I_B = 99\text{-}100$
- $I_{CEO} > I_{CBO}$ such that $I_{CEO} = (1+\beta)\, I_{CBO}$ where β is the CE configuration current gain $\beta = I_C/I_B$
- Since, $I_E = I_C + I_B$
- Hence, $\alpha = I_C/I_E = I_C/(I_B+I_C) = \beta/(1+\beta)$
- Also, $\beta = I_C/I_B = I_C/(I_E-I_C) = \alpha/(1-\alpha)$

BJT: Junction bias for Operating regions

Operation Regions	Emitter- Base Junction	Collector- Base Junction
Active	Forward bias	Reverse bias
Cut-off	Reverse bias	Forward bias
Saturation	Forward bias	Forward bias

- For a transistor to operate as an amplifier, it should work in active region i.e. the Emitter-base junction should be forward biased and collector-base junction should be reverse biased for all the points of applied AC voltage.
- Hence, the DC operating point should be chosen carefully so that the transistor remains in active region and not driven to cutoff or saturation for all the points of applied AC input signal.

CE Mode : Connection of voltmeters and ammeters for input and output characteristics

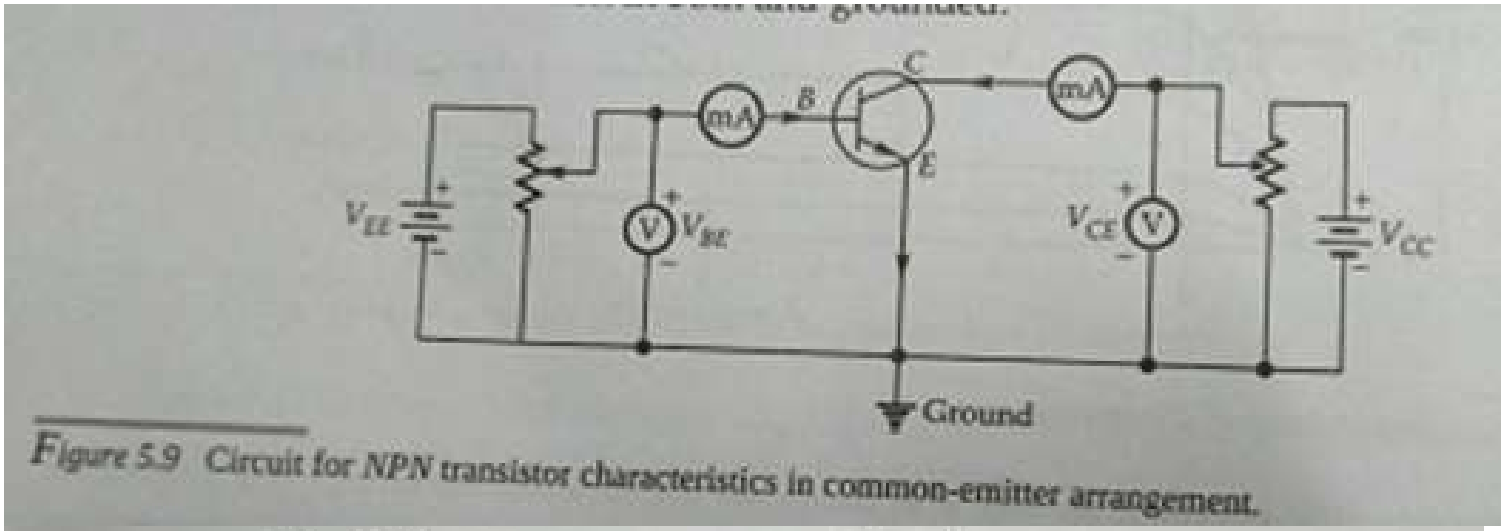


Figure 5.9 Circuit for NPN transistor characteristics in common-emitter arrangement.

Thus $V_{BE} = f_1(I_B, V_{CE})$ and $I_C = f_2(I_B, V_{CE})$

Figure 5.10 shows the curves between I_B and V_{BE} for different values of V_{CE}, known as input characteristic curves.

At $V_{CE} = 0$ V, emitter-base junction is forward biased, it acts as a forward biased diode. With higher values of V_{CE}, collector collects slightly more electrons due to decrease of effective width of the base, hence base current decreases. Therefore curve shifted towards the right on increasing V_{BE}.

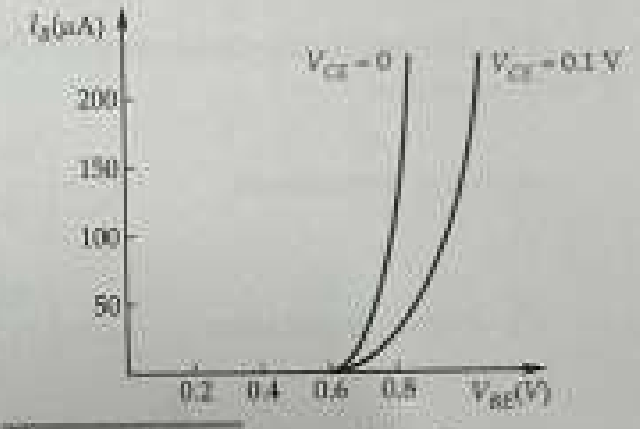
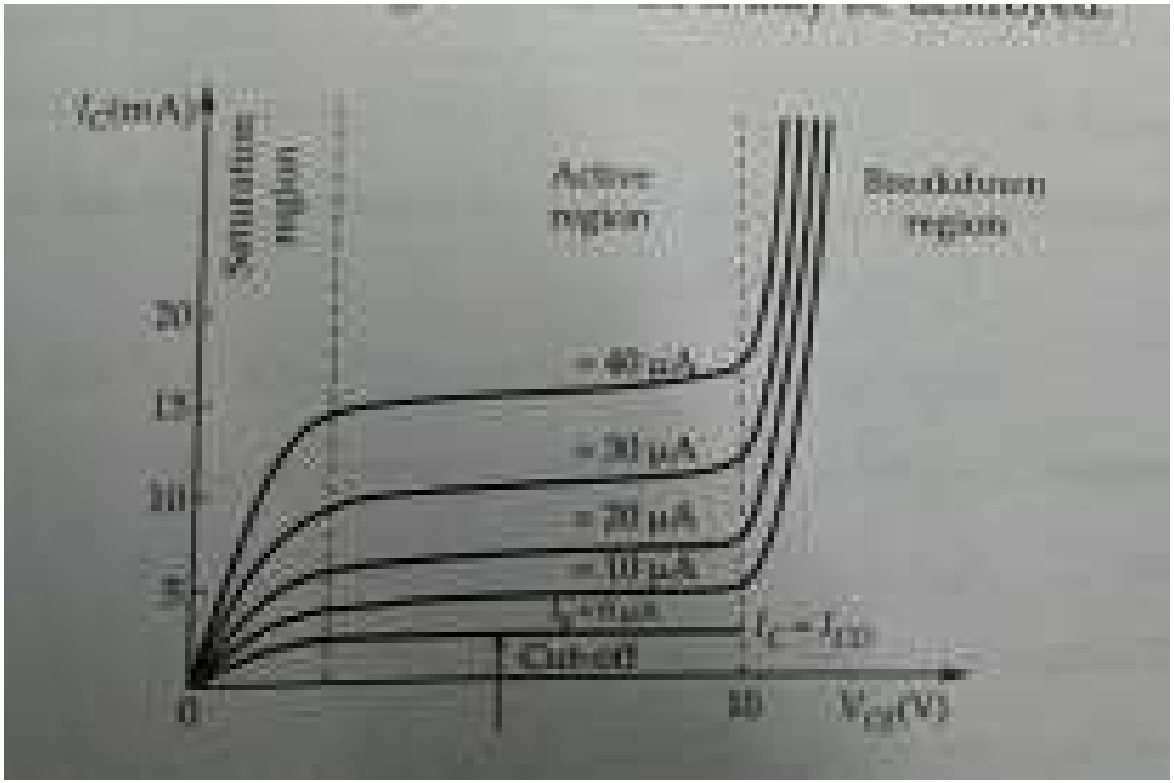


Figure 5.10 Input characteristics of CE arrangement.

- Input characteristics of CE mode is similar to the characteristics of a forward biased diode

CE Mode : output characteristics



- Output characteristics is drawn between V_{CE} and I_C. In active region I_C doesn't depend on V_{CE} and is fairly constant for a given value of I_B.
- The various lines are corresponding to the different values of input current I_B.
- The 3 regions Active, Cutoff and Saturation are clearly visible.

BJT: Load Line

dc Load Line

Let us consider a CE amplifier circuit ... base resistor R_B and collector resistor R_C ... visualised in Fig. 6.1.

In the output circuit, apply Kirchhoff's ... law (KVL),

$$V_{CC} = V_{CE} + I_C R_C$$

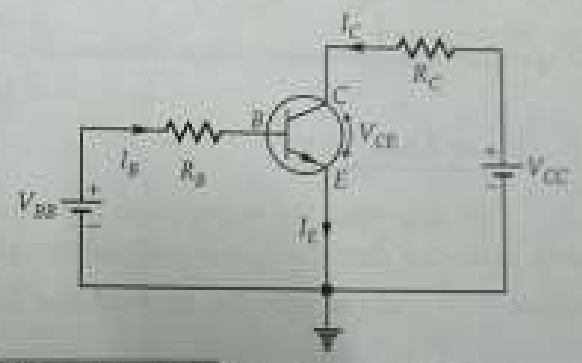


Figure 6.1 CE, NPN transistor amplifier circuit.

$$V_{CE} = V_{CC} - I_C R_C$$

or

$$I_C = \frac{-V_{CE}}{R_C} + \frac{V_{CC}}{R_C} \quad \text{...(6.1)}$$

As V_{CC} and R_C are fixed values *i.e.*, $\frac{V_{CC}}{R_C}$ is a constant, therefore above equation is a straight line equation like $y = mx + C$, where m = slope of line $= -\frac{1}{R_C}$ and $\frac{V_{CC}}{R_C}$ is the intercept of line on the vertical current axis of the output characteristics. Consider the two extreme points on the straight line shown in Fig. 6.2.

(*i*) When $I_C = 0$, $V_{CE} = V_{CC}$; cut-off point *A*

(*ii*) When $V_{CE} = 0$, $I_C = \frac{V_{CC}}{R_C}$; saturation point *B*

- The load line is a straight line which comprises of all the points of output voltage and current (V_{CE} and I_C) corresponding to the variation in input signal
- The KVL in the output loop gives the equation of the load line and the 2 extreme end points are evaluated to draw the load line as shown

BJT: DC & AC load line and Q-point

The dc load line is obtained by joining points A and B. The intersection of dc load line and characteristic curve gives the *operating point* (or *quiescent point*) as shown in Fig. 6.2. The dc load line gives the dynamic behaviour of the circuit and Q-point provides the value of I_C and V_{CE} of the circuit. When signal is applied to the input, values of I_C and V_{CE} vary about the Q-point accordingly. Q-point is also known as *operating point*.

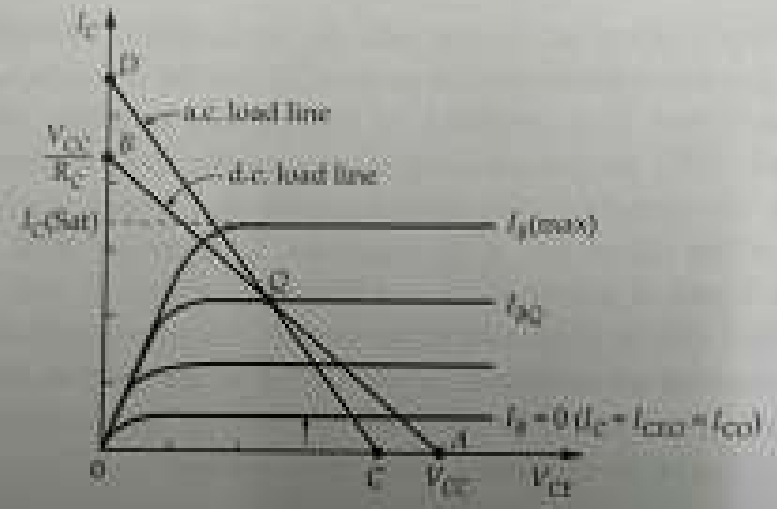
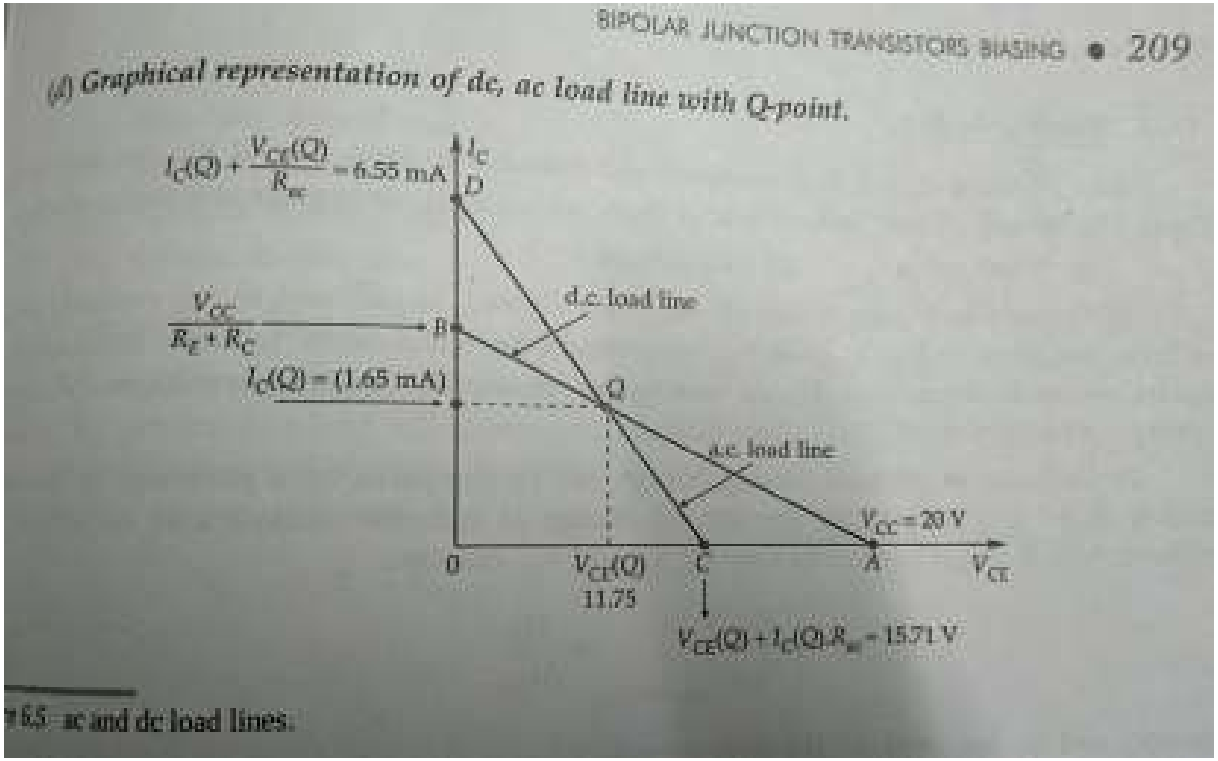


Figure 6.2 Common-emitter output characteristics and load lines.

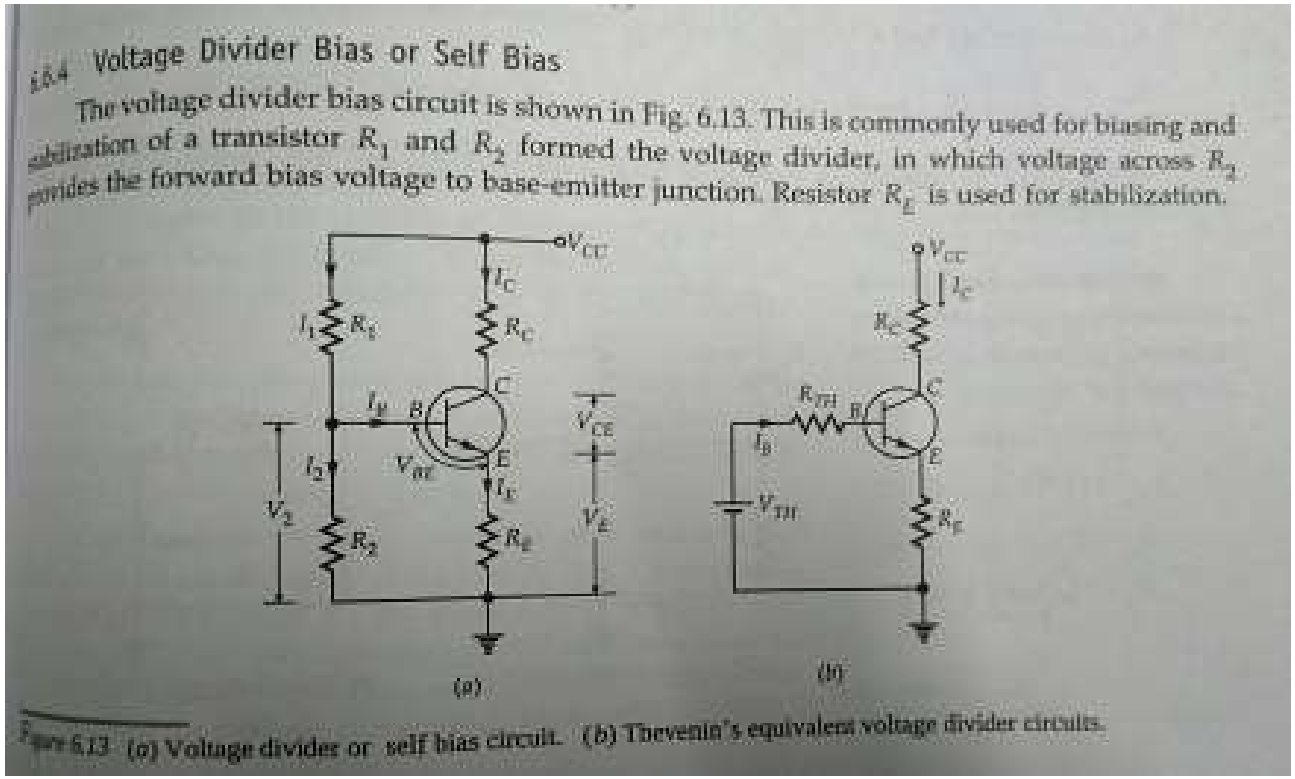
- The DC load line comprises of the points of output side corresponding to the variation in DC bias of input side, whereas the AC load line comprises of the points of the output side corresponding to the variation in AC signal at the input side.
- The AC load line has a steeper slope as compared to the DC load line as the equivalent resistance in case of AC is lower than in case of DC.
- The 2 load lines intersect at the operating point known as (**Q-point**)

BJT: Drawing AC load line from DC load line



- The AC load line can be drawn using AC resistance R_{ac} to the Q-point co-ordinate $V_{CE}(Q)$ and $I_C(Q)$ as shown in the figure above
- Once AC load line is drawn we can find the output side voltage and current for each and every value of the applied AC input

BJT: Voltage divider bias or Self Bias



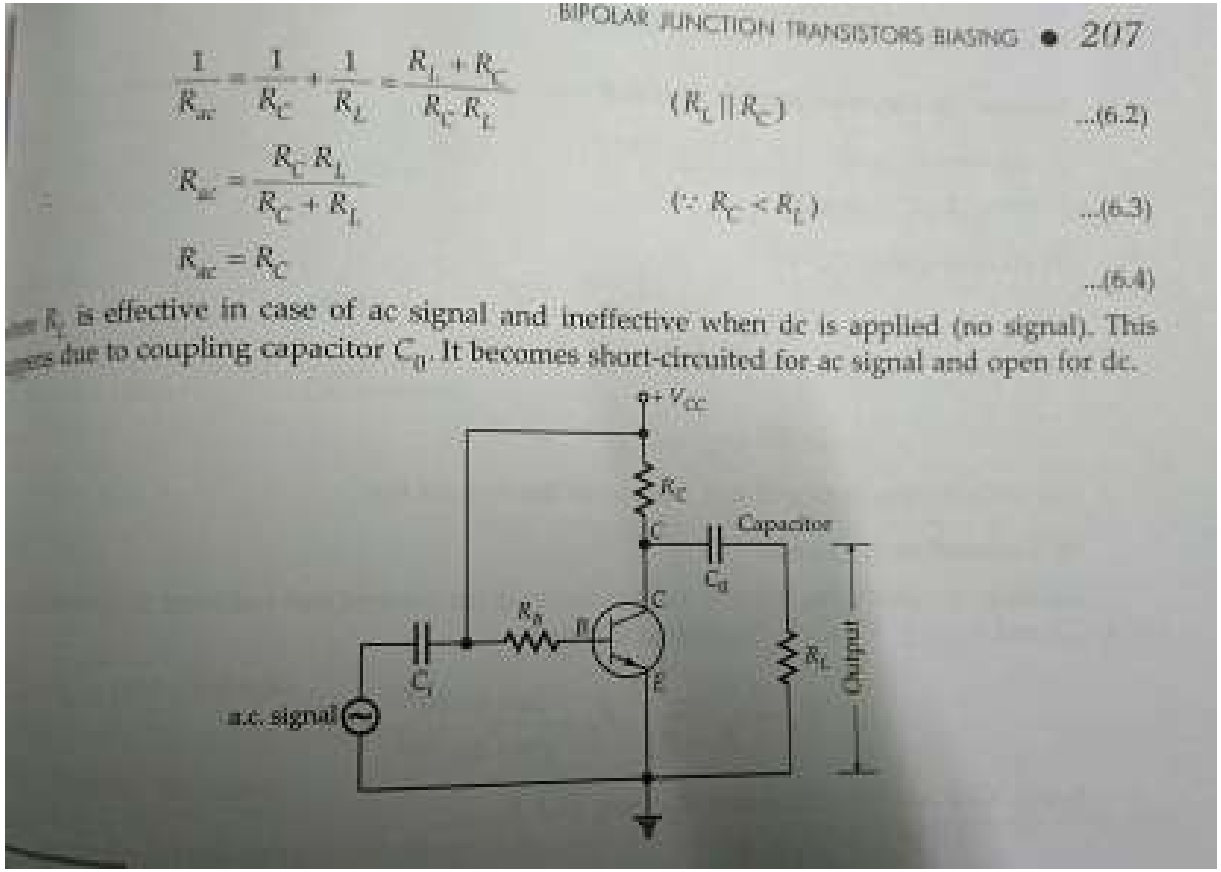
6.6.4 Voltage Divider Bias or Self Bias

The voltage divider bias circuit is shown in Fig. 6.13. This is commonly used for biasing and stabilization of a transistor R_1 and R_2 formed the voltage divider, in which voltage across R_2 provides the forward bias voltage to base-emitter junction. Resistor R_E is used for stabilization.

Figure 6.13 (a) Voltage divider or self bias circuit. (b) Thevenin's equivalent voltage divider circuits.

- In voltage divider bias, on input side 2 resistances are connected to create a voltage divider such that just one DC source is sufficient for both input and output side circuit.
- In order to solve this circuit we simply separate the input and output side of the circuit by connecting the DC source of same magnitude on input and output side.
- Then we find the equivalent Thevenin's circuit on input side as shown in the figure.
- Finally we apply KVL on both input and output sides to solve the circuit.

BJT: Single stage CE Amplifier Configuration



BIPOLAR JUNCTION TRANSISTORS BIASING • 207

$$\frac{1}{R_{ac}} = \frac{1}{R_C} + \frac{1}{R_L} = \frac{R_L + R_C}{R_C R_L} \qquad (R_L \| R_C) \qquad \ldots(6.2)$$

$$R_{ac} = \frac{R_C R_L}{R_C + R_L} \qquad (\because R_C < R_L) \qquad \ldots(6.3)$$

$$R_{ac} = R_C \qquad \ldots(6.4)$$

R_L is effective in case of ac signal and ineffective when dc is applied (no signal). This ...s due to coupling capacitor C_0. It becomes short-circuited for ac signal and open for dc.

- Coupling capacitors are used on both input and output sides to block the DC and pass on only the AC. The above circuit is an example of single stage amplifier.
- If two or more single stage amplifier circuits are connected in cascade then the resulting amplifier becomes multistage amplifier.

Numerical - 1

Example 5.3 *A transistor is connected in CE configuration as shown in Fig. 5.12. Use the silicon transistor. Determine (i) V_{BE} (ii) I_B (iii) I_C (iv) V_{CE} (v) I_E.*

Solution. Given $R_B = 470\,k\Omega$, $R_C = 3.6\,k\Omega$, $V_{in} = 15\,V$, $V_0 = 15\,V$ and $\beta_{dc} = 100$

(*i*) For ideal transistor, $V_{BE} = 0$.

(*ii*) I_B *determination.* Apply KVL in the input circuit (base circuit)

$$V_{in} = I_B R_B + V_{BE}$$

$$I_B = \frac{V_{in}}{R_B} = \frac{15}{470 \times 10^3} \quad (\because V_{BE} = 0\,V)$$

$$= 31.9\,\mu A$$

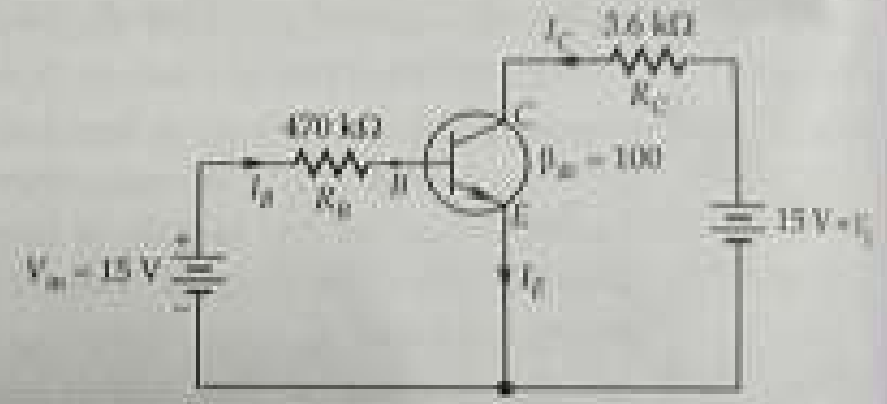


Figure 5.12

(*iii*) I_C *determination.* $\because I_C = \beta I_B$ $\therefore I_C = 100 \times 31.9\,\mu A = 3.19\,mA$.

(*iv*) V_{CE} *determination.* Apply KVL in the output circuit *i.e.*, collector circuit.

$$V_0 = I_C R_C + V_{CE}$$

$$\therefore V_{CE} = V_0 - I_C R_C = 15 - (3.19 \times 10^{-3}) \times 3.6 \times 10^3 = 15 - 11.48 = 3.52\,V$$

(*v*) I_E *determination.* Usually $I_E \approx I_C$, because I_B is very small.

In this case $I_E = I_C + I_B = 3.19\,mA + 31.9\,\mu A = 3.22\,mA$

- For ideal transistor VBE = 0 and for Si transistor VBE = 0.7 V

Numerical - 2

Problem 6.4 *In a transistor amplifier as shown in Fig 6.23(a), $R_C = 8\,k\Omega$, $R_L = 24\,k\Omega$ and $V_{CC} = 24\,V$. Draw the d.c. load line, determine the optimum operating point. Also draw the a.c. load line.*

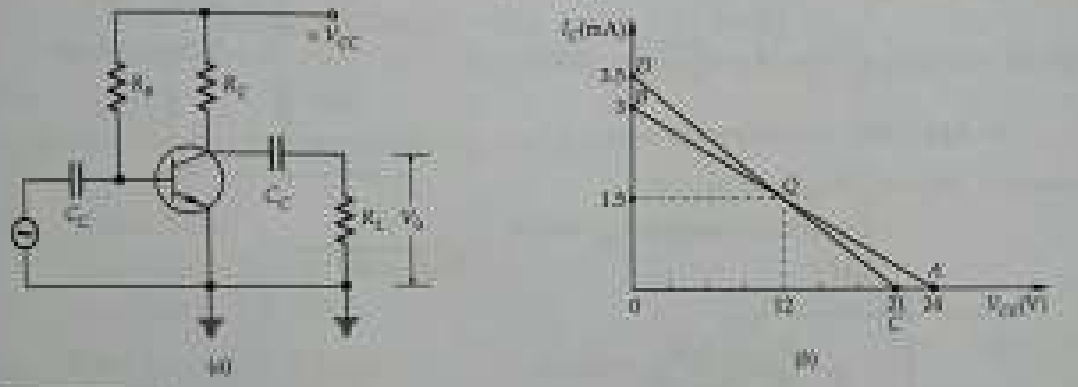


Figure 6.23

Solution. Given $R_C = 8\,k\Omega$, $R_L = 24\,k\Omega$ and $V_{CC} = 24\,V$

(a) (i) I_C (saturation), when $V_{CE} = 0$, is given by

$$I_C = \frac{V_{CC}}{R_C} = \frac{24}{8 \times 10^3} = 3\,mA \qquad \text{(Point } B\text{)}$$

(ii) V_{CE} (cut-off), when $I_C = 0$, i.e., $V_{CE} = V_{CC} = 24\,V$ (Point A)

$\therefore$ dc load line is a line connecting two points A and B on the output characteristic curves.

(b) *Optimum operating point.* Midway of the load line AB provides the optimum or maximum operating point $I_C(Q)$ and $V_{CE}(Q)$.

In this case $I_C(Q) = \frac{I_C}{2} = 1.5\,mA$ and $V_{CE}(Q) = \frac{24}{2} = 12\,V$

(c) *ac load line.* I_C (saturation) $= I_C(Q) + \frac{V_{CE}(Q)}{R_{ac}} = 1.5 + \frac{12}{6 \times 10^3} = 3.5\,mA$ (Point D)

and V_{CE} (cut-off) $= V_{CE}(Q) + I_C(Q) \times R_{ac}$

$= 12 + (1.5) \times 10^{-3} \times 6 \times 10^3 = 21\,V$ (Point C)

$$\left[\because \quad R_{ac} = R_C \| R_L = \frac{R_C \cdot R_L}{R_C + R_L} = \frac{8 \times 24}{8 + 24} = 6\,k\Omega\right]$$

Numerical - 3

Problem 6.5 *Determine the I_C and V_{CE} for the voltage divider bias configuration of Fig. 6.24.*

Solution. Given :

$V_{CC} = -18\,V$, $R_1 = 47\,k\Omega$,

$R_2 = 10\,k\Omega$, $R_C = 2.4\,k\Omega$ and $R_E = 1.1\,k\Omega$.

(*i*) From Fig. 6.24,

$$V_B = \left(\frac{V_{CC}}{R_1 + R_2}\right) R_2 = \frac{-18 \times 10}{47 + 10} = -3.16\,V.$$

(*ii*) Apply KVL in base-emitter loop :

$$V_E = V_B - V_{BE} = -3.16 - (-0.7)$$

(For silicon transistor $V_{BE} = 0.7\,V$)

$$= -2.46\,V$$

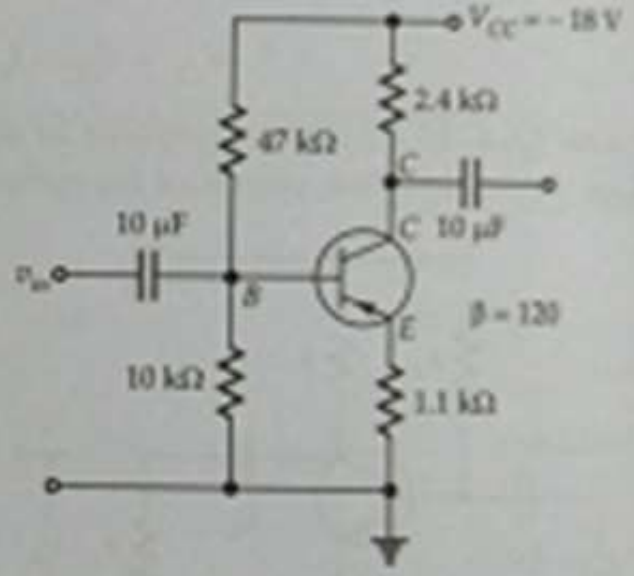


Figure 6.24

Therefore current in R_E,

$$I_E = \frac{V_E}{R_E} = \frac{2.46}{1.1 \times 10^3} = 2.24\,mA$$

(*iii*) Now consider collector-emitter loop for V_{CE} :

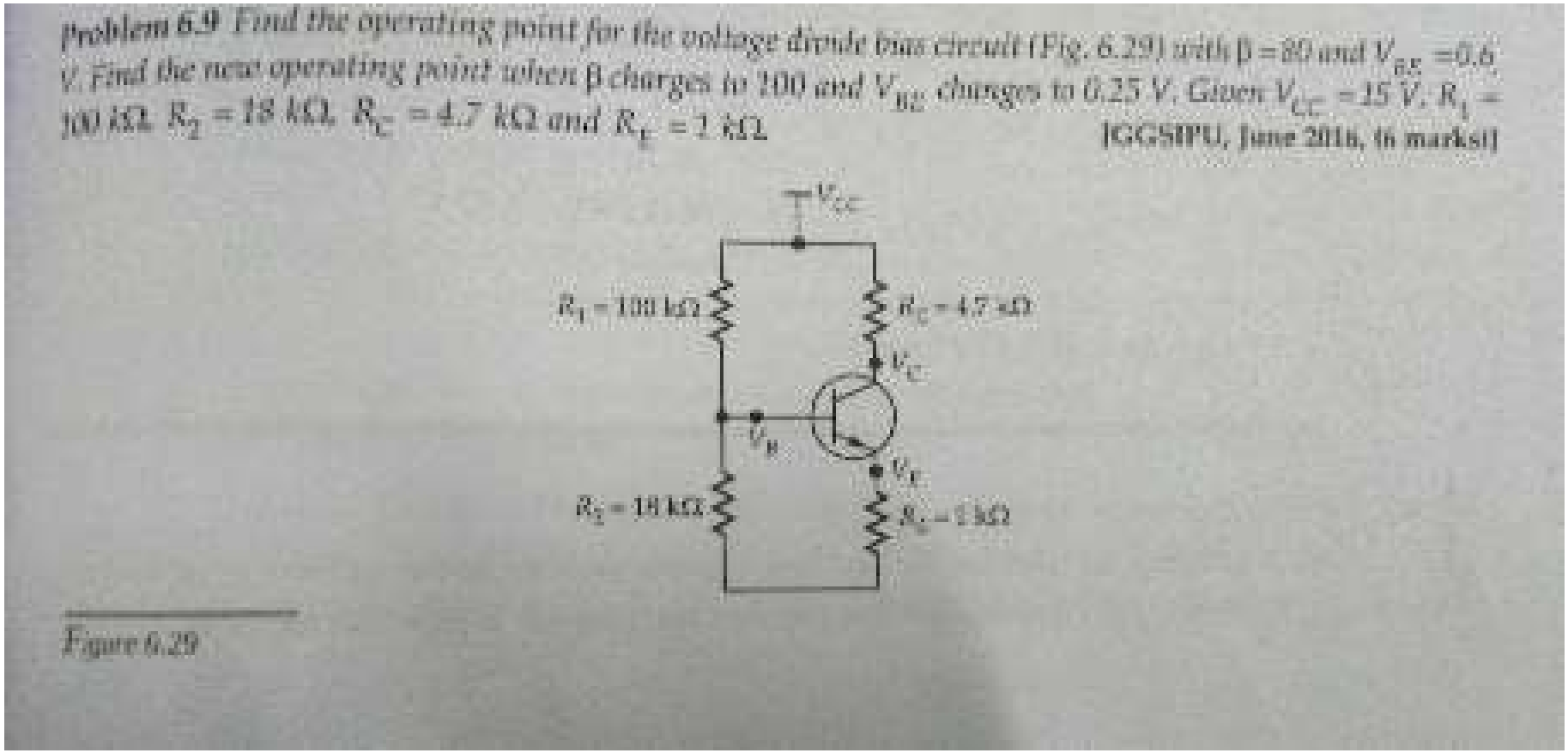
$$V_{CC} = I_C R_C + I_E R_E - V_{CE}$$

$$\therefore \quad V_{CE} = +(I_C R_C + I_E R_E) - V_{CC} = +I_C (R_C + R_E) - V_{CC} \qquad (I_C = I_E)$$

$$= +2.24 \times 10^{-3} \times (2.4 + 1.1) \times 10^3 - 18 = 7.84 - 18 = -10.16\,V$$

Thus $I_C = I_E = 2.24\,mA$ and $V_{CE} = -10.16\,V$

Numerical - 4



Problem 6.9 Find the operating point for the voltage divide bias circuit (Fig. 6.29) with β = 80 and V_{BE} = 0.6 V. Find the new operating point when β changes to 100 and V_{BE} changes to 0.25 V. Given V_{CC} = 15 V, R_1 = 100 kΩ, R_2 = 18 kΩ, R_C = 4.7 kΩ and R_E = 2 kΩ. [GGSIPU, June 2016, 16 marks]

Figure 6.29

- Here the lower point should be taken as reference at 0 V

Solution. Given values. $V_{CC} = 15$ V, $R_1 = 100$ kΩ, $R_2 = 18$ kΩ, $R_C = 4.7$ kΩ, $R_E = 1$ kΩ.

Figure 6.30 shows the Thevenin's equivalent circuit, where

$$R_{TH} = \frac{R_1 R_2}{R_1 + R_2} = \frac{100 \times 18}{100 + 18} = 15.25 \text{ kΩ}$$

$$V_{TH} = \left(\frac{V_{CC}}{R_1 + R_2}\right) R_2 = \left(\frac{15}{100 + 18}\right) \times 18 = 2.29 \text{ V}$$

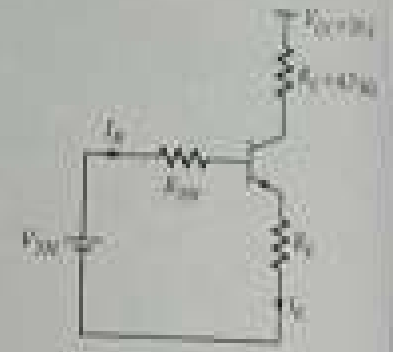


Figure 6.30 Thevenin's equivalent circuit

Case 1. When $\beta = 80$ and $V_{BE} = 0.6$ V

(i) I_B. Apply KVL to the base-emitter circuit

$$V_{TH} = I_B R_{TH} + V_{BE} + I_E R_E$$

$$\Rightarrow \quad I_B = \frac{V_{TH} - V_{BE}}{R_{TH} + (1 + \beta) R_E}$$

$$= \frac{2.29 - 0.6}{15.25 + (1 + 80) \times 1} = \frac{1.69}{96.25} = 0.0175 \text{ mA}$$

(ii) $I_C(Q) = \beta I_B = 80 \times 0.0175 = 1.40$ mA

(iii) $V_{CE}(Q) = V_{CC} - I_C(R_C + R_E) = 15 - 1.40\,(4.7 + 1) = 7.02$ V

Case 2. When $\beta = 100$ and $V_{BE} = 0.25$ V

(i) $I_B = \dfrac{V_{TH} - V_{BE}}{R_{TH} + (1 + \beta) R_E}$

$$= \frac{2.29 - 0.25}{15.25 + (1 + 100) \times 1} = \frac{2.04}{116.25} = 0.0175 \text{ mA}$$

(ii) $I_C(Q) = \beta I_B = 100 \times 0.0175 = 1.75$ mA.

(iii) $V_{CE}(Q) = V_{CC} - I_C(R_C + R_E) = 15 - 1.75\,(4.7 + 1) = 5.02$ V