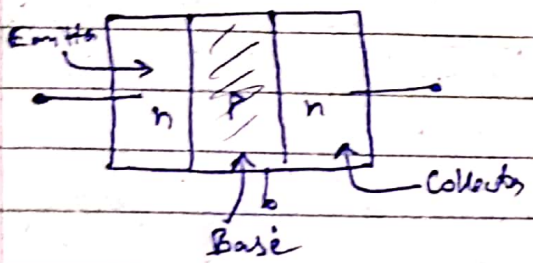
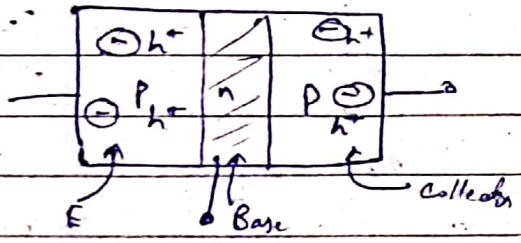
17th Jan 2022 **Bipolar junction Transistor (BJT)**

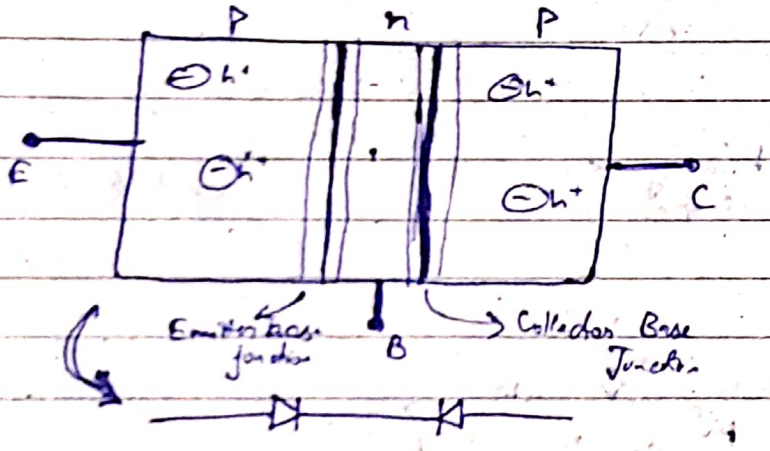
Date / Pg No.

* Invented in 1947 at Bell Telephone Lab.

BJT Construction:- Consist of 3 layers.

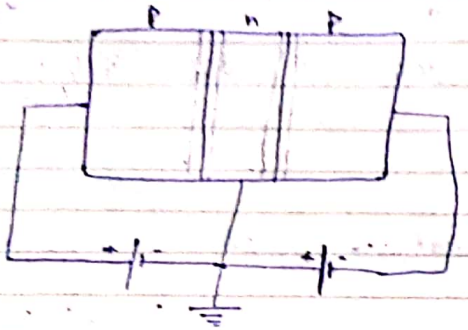






Mode of Operation	Emitter Junction	Collector Junction
Amplification ← Active	Forward	Reverse
for switching operation ← Saturation — On	Forward	Forward
for switching operation ← Cutoff — off	Reverse	Reverse
✗ Reverse active	Reverse	Forward

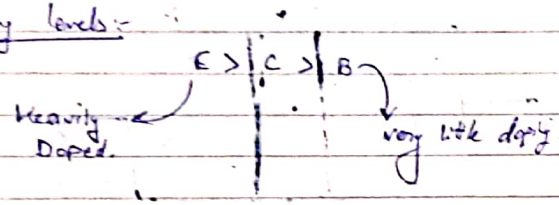
Notation :-



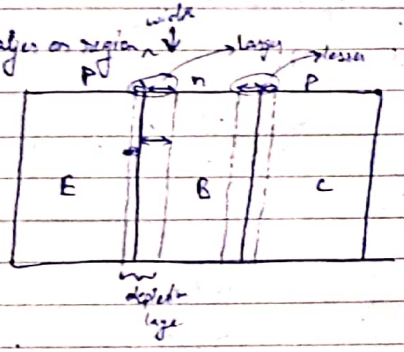
Size comparison :-

C > E > B

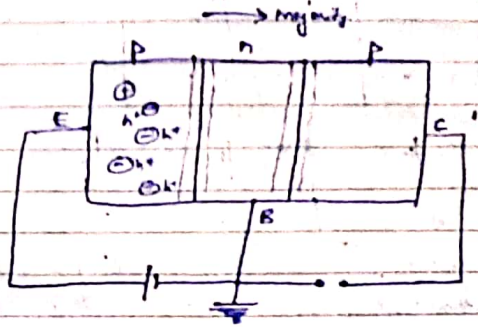
Doping levels :-



Doping ↑ depletion layer on region ↓ wide

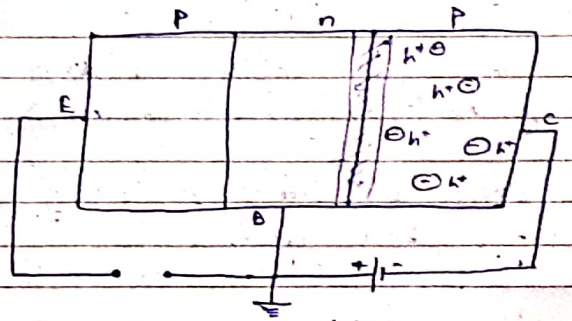


Transistor Operation :-



When E is +ve and B is -ve, it works as forward Biased diode, hence depletion region width ↓ with ↑ in biasing.

(a) Heavy flow of majority carriers from p to n-type material.

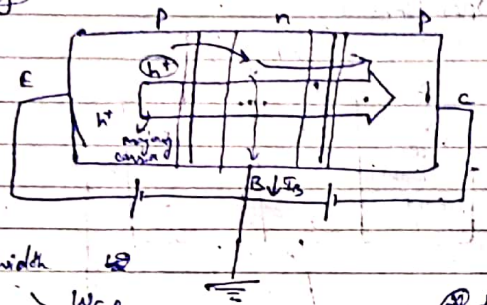


(b) Working as reverse biased diode.

(c) flow of majority carriers is 0, only minority carriers flow.

* Called Bipolar ⇒ as current is due to both (e⁻) and (h⁺)

Active region



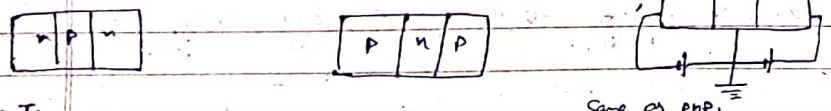
* dep width
$W_{B-C} > W_{E-B}$
due to different doping.

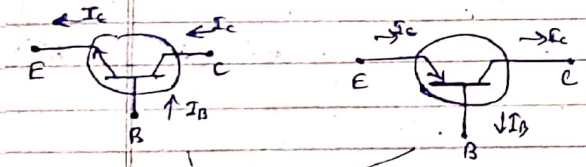
* the B region is very thin and hence the holes that diffuse from E to B passes mostly through B and reaches C.
Hence Base current is much low.

* Base current is very small. (μA or nA).

* large no. of majority carriers will diffuse across B-C junction and reached collector region.

* Majority carriers will works as minority carriers in n-type base region.



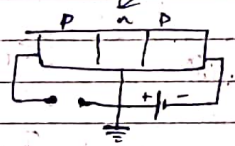


* arrow is towards E and shows the current direction

$I_E = I_B + I_C$ ⟹ always true.

$I_C = I_{C_{minority}} + I_{C_{majority}}$

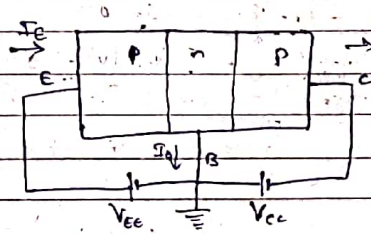
Reverse bias current. (I_C emitter is open)

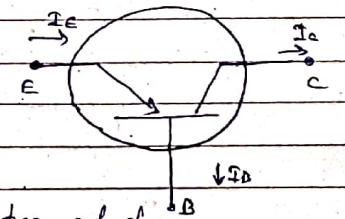


18th Jan 2022

Common Base Configuration :-

* Base is common to both input and output sides.



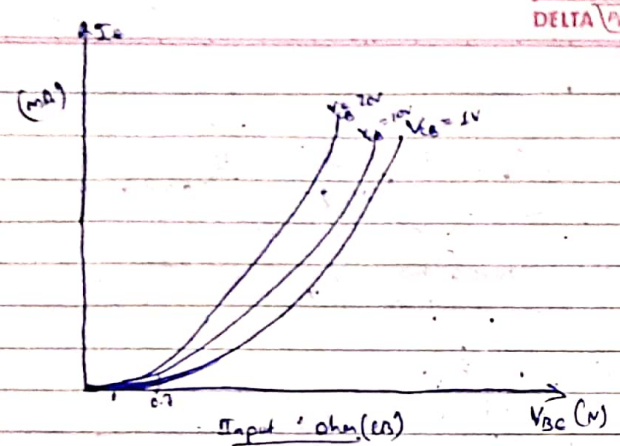


* To describe a 3-terminal device, two set of char. are required :-

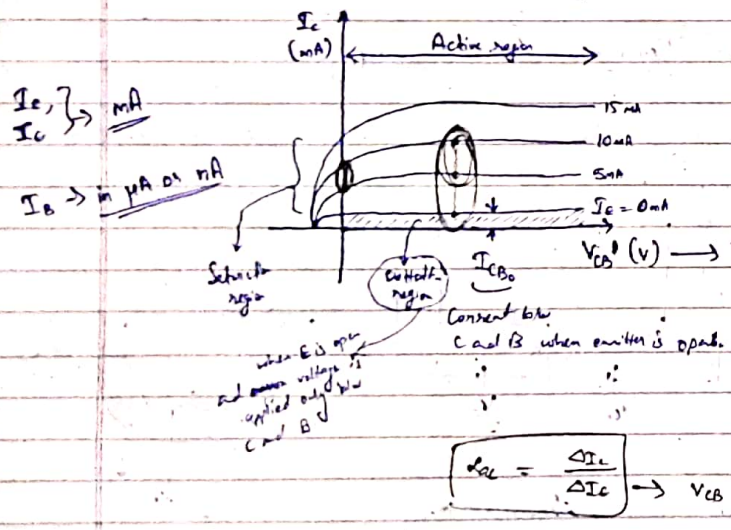
Input characteristic — Output CB

CB ⇒ voltage b/w collector and Base (V_{CC})

(Input current (I_E) to Input voltage (V_{BE}) for different values of (V_{CB}))



(*) Output char relates output current (I_C) and output voltage (V_{CB}) for different value of I_E



I_E, I_C → mA

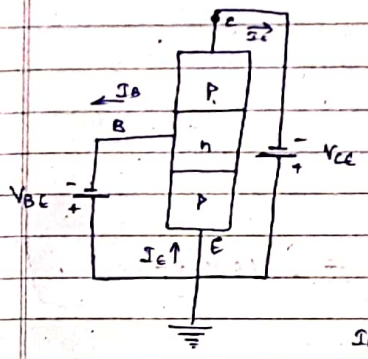
I_B → in μA or nA

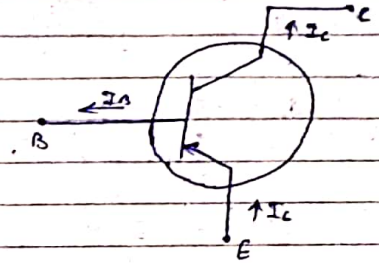
- Active → Amplifier
- Cutoff, Saturation → switching purpose

$$\alpha_{ac} = \frac{\Delta I_C}{\Delta I_E} \rightarrow V_{CB} \text{ is constant.}$$

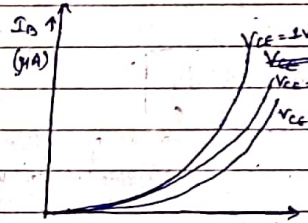
Common Emitter Config :-

* Emitter is common to both input and Output.



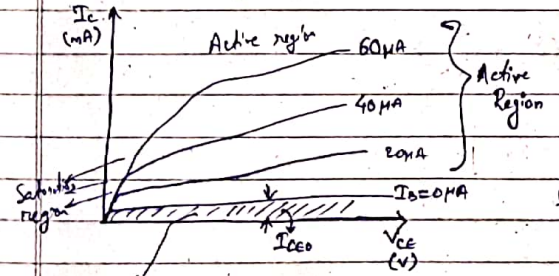


Input current (I_B) v/s Input voltage (V_{BE}) for a range of output voltage.



V_{CE} ↑ I_B ↓ as potential diff b/w C and E ↑, this gives rise to more current in E→C and hence E current I_B ↓.

Output char :-



I_{CEO} ⇒ C.I b/w C and B when E is open

Current gain in CB :- (common base)

$$\alpha = \frac{I_c}{I_E}$$

$I_E = I_B + I_c$ (very small)

$\Rightarrow I_E \simeq I_c \Rightarrow \alpha \simeq 1 \quad (0.90 \leq \alpha \leq 0.99)$

$$I_c = \alpha I_E + I_{CBO}$$

(I_{CBO} : minority current. (independent of V_{CB}) (μA or nA))

$\Rightarrow I_c \simeq \alpha I_c$ and $\alpha \simeq 1$

So, $I_c \simeq I_c$

Current gain in CE config :-

$$\beta = \frac{I_c}{I_B}$$

Since, $I_c \gg I_B \Rightarrow \beta \gg 1$

$$50 \leq \beta \leq 40$$

$$I_c = \beta I_B + I_{CEO}$$

$I_c = \alpha I_E + I_{CBO}$

$I_c = \alpha(I_c + I_B) + I_{CBO}$

$$\Rightarrow I_c = \frac{\alpha I_B}{1-\alpha} + \frac{I_{CBO}}{1-\alpha}$$

If $I_B = 0 \Rightarrow$ as in CE cutoff region

$$\Rightarrow I_c = \frac{I_{CBO}}{1-\alpha} = I_{CEO}$$

(from CE output char. graph)

$$I_c = I_{CEO} = (\beta+1) I_{CBO}$$

Relation b/w α and β :-

$I_E = I_c + I_B$

$$\frac{I_c}{\alpha} = I_c + \frac{I_c}{\beta} \quad \left(\because \alpha = \frac{I_c}{I_E},\ \beta = \frac{I_c}{I_B}\right)$$

$$\Rightarrow \frac{1}{\alpha} = 1 + \frac{1}{\beta}$$

$$\Rightarrow \alpha = \frac{\beta}{1+\beta} \quad \text{and} \quad \beta = \frac{\alpha}{1-\alpha}$$

19th Jan 2022

General char. of BJT :-

- Bipolar (majority and minority carriers present)
- $I_C = \beta I_B$
  - I_C : Output
  - I_B : Input
  - (*) Current control device
  - (*) Current controlled current source
- Two diodes connected back to back could not work as transistor
  - i) Base width large
  - ii) No Base current here

- $I_C = \beta(I_B) + I_{CEO}$
  $= \beta I_B + (\beta+1) I_{CO}$ → I_{CBO}
  $I_C = \alpha I_C + I_{CBO}$
- (*) Temp ↑ ⟹ β increases as significant change in minority carrier.
  (Though no of majority and minority ~~carrier~~ carriers generated + same but the ↑ in minority carrier is quite high)
- (*) Very small change in α ⟶ large change in β.

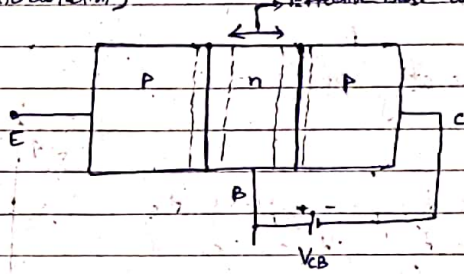
$$\beta = \frac{\alpha}{1-\alpha}$$

eg $\alpha = 0.95 \Rightarrow \beta = 19$
$\alpha = 0.99 \Rightarrow \beta = 99$.

Early effect (Base width modulation)

When V_{BC} ↑, Depletion region of C-B Junction widens.

⇒ Effective base width ↓.
(Base width modulation)



Base Punch through :-
when W becomes zero.
If R.Bias voltage at C-B junction ↑, a situation will arise when E-B & C-B depletion region touch each other & effective base width becomes '0'

Since Base width ↓, no. of Base charge carriers ↓. &
Therefore, I_B ↓
Hence, β ↑.

23rd Jan

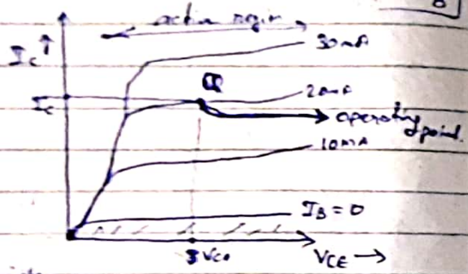
DC Biasing

$V_{BE} = 0.7V$

$I_E = I_B + I_C = I_B + \beta I_B = (1+\beta)I_B \approx \beta I_B$ (if β is very large)

and $\beta = \frac{I_C}{I_B}$

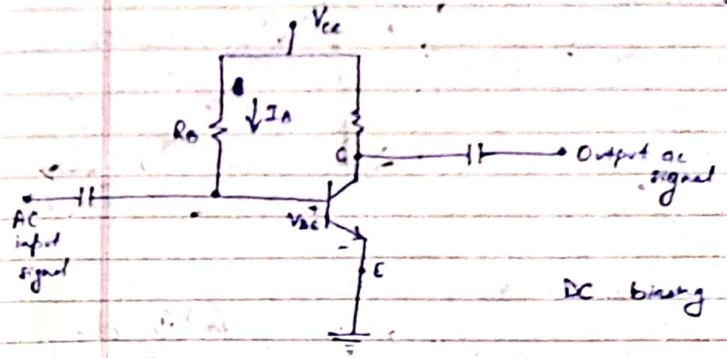
Operating points :-



* Operating point explains the operating voltage and current of transistor
* Operating point should lie in the active region. (else there will be distortion) → not amplification
  (in active region there is amplification)
  (to get amplified signal without any distortion)
* Also called Quiescent point (Q-point)
  → (Quiet, still and inactive)
* Biasing :- application of DC voltage to establish a fixed level of current and voltage

① Fixed-bias config. :-

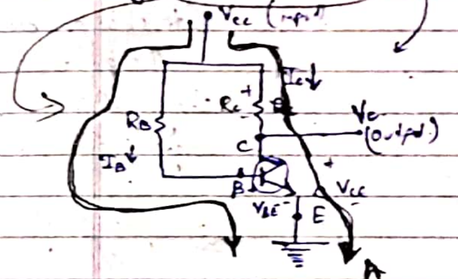
V_{CC} = input → Voltage Common Collector → voltage being given supply connected to the collector



DC biasing ⇒ f = 0 Hz

$X_C = \frac{1}{2\pi f C} = \infty$ (Capacitive reactance of capacitor)

Considering B-E (input) loop :-



Applying KVL,

$V_{CC} - I_B R_B - V_{BE} = 0$

$\Rightarrow \boxed{I_B = \frac{V_{CC} - V_{BE}}{R_B}}$

V_{CC} and V_{BE} are basically constant.

So, I_B depends on R_B.

Considering the output of (C-E) loop :-

$V_{CC} - I_C R_C - V_{CE} = 0$

$\Rightarrow \boxed{V_{CE} = V_{CC} - I_C R_C}$

④ V_{BE} is generally taken 0.7 V.

④ as E is grounded

$V_{CE} = V_C - V_E$ (→0) $= V_C$

$\Rightarrow \boxed{V_{CE} = V_E}$

and, $V_{BE} = V_B - V_E = V_B$

$\Rightarrow V_{BE} = V_B$

Load line analysis :-

$V_{CE} = V_{CC} - I_C R_C$

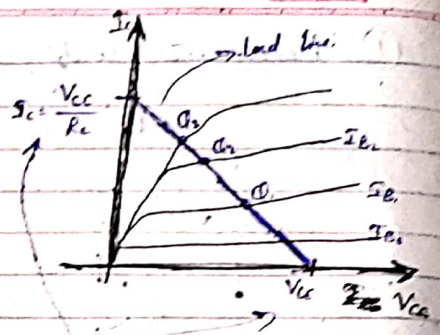
when when $I_C = 0$.

$\Rightarrow \boxed{V_{CE} = V_{CC}}$ @ $I_C = 0$

$\Rightarrow I_C R_C = V_{CC} - V_{CE}$

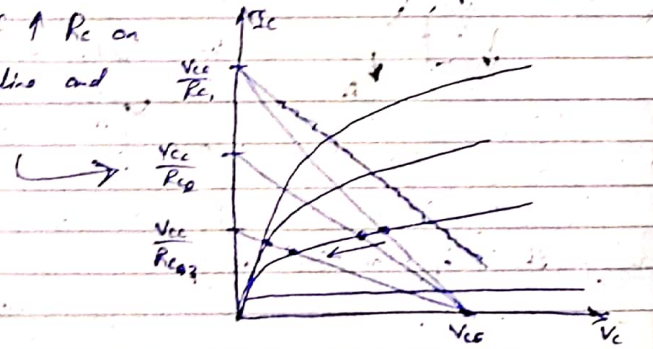
$\Rightarrow I_C = \frac{V_{CC}}{R_C} - \frac{V_{CE}}{R_C}$

$\boxed{I_C = \frac{V_{CC}}{R_C}}$ $V_{CE} = 0$



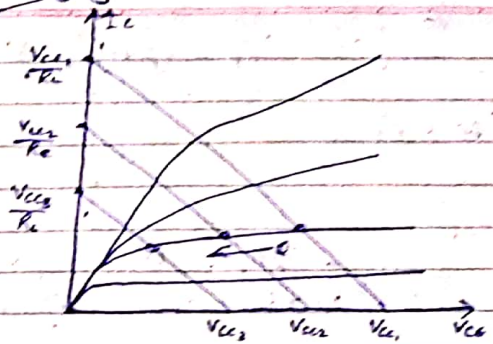
(a) To change the slope of load line (to change the Q-point point) change R_C to change I_C.

(b) Effect of ↑ R_C on load-line and Q-point.



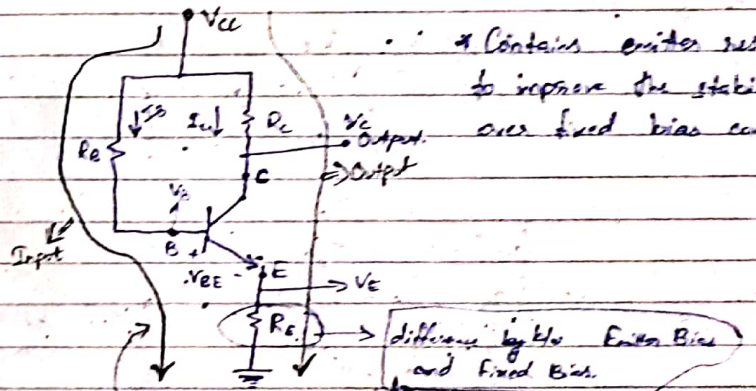
$R_3 > R_2 > R_1$

When changing V_{CC},



$V_{CC_1} > V_{CC_2} > V_{CC_3}$

Emitter-Bias config. :-



* Contains emitter resistance to improve the stability level over fixed bias config.

→ difference by the Emitter Bias and Fixed Bias.

all changes here are due to this resistor R_E as $V_E \neq 0$

Considering B-E loop (input) :-

By KVL,

$V_{CC} - I_B R_B - V_{BE} - I_E R_E = 0$

and we know, $I_E = I_C + I_B$

$= (\beta + 1) I_B$

$V_{CC} - I_B R_B - V_{BE} - (\beta+1) I_B R_E = 0$

$$I_B = \frac{V_{cc} - V_{BE}}{R_B + (\beta+1)R_e}$$

Considering Output (C-E)

$V_{cc} - I_c R_c - V_{ce} - I_E R_e = 0$

$V_{cc} - V_{ce} - I_c (R_c + R_e)$ Where $I_c \cong I_E$

$\Rightarrow \boxed{V_{ce} = V_{cc} - I_c (R_c + R_e)}$

also, $\boxed{V_E = I_E R_e}$ from circuit

$V_{CE} = V_C - V_E$ from KVL

$\boxed{V_C = V_{CE} + V_E}$

$\Rightarrow \boxed{V_C = V_{CC} - I_C R_C}$

$\boxed{V_B = V_{CC} - I_B R_B}$

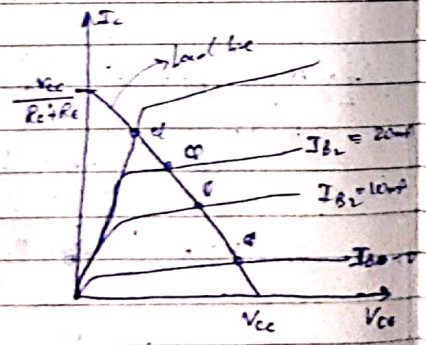
$\boxed{V_B = V_E + V_{BE}}$ can also be seen in the circuit

$I_B = \frac{V_B - V_{BE}}{R_B}$

Load line analysis :-

$V_{CE} = V_{CC} - I_C (R + R_E)$

$I_C = \frac{V_{CC}}{R_C + R_E}\Big|_{V_{CE}=0}$

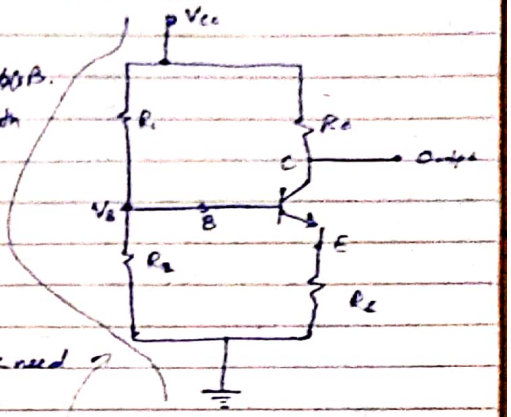


Voltage - divide config :-

(Less dependent on transistor's β. Hence, invariable with Temp. change.

$T \uparrow \beta \uparrow$ as $\beta = \frac{I_C}{I_B}$

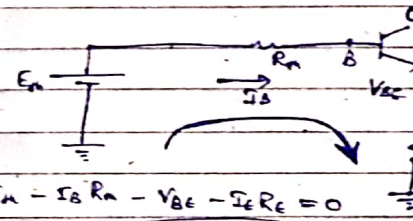
So, when $T \uparrow I_C \uparrow$ and hence $\beta \uparrow$, to save β from $\uparrow$ we need to control I_C



$R_{th} = R_2 \parallel R_1$ from this

$= \frac{R_1 R_2}{R_1 + R_2}$

$E_{th} = \beta V_{R_2} = \frac{V_{CC} * R_2}{R_1 + R_2}$ {By voltage divider}



$E_{th} - I_B R_{th} - V_{BE} - I_E R_E = 0$

and $\Rightarrow \boxed{I_E = (\beta+1) I_B}$

$\boxed{I_B = \frac{E_{th} - V_{BE}}{R_{th} + (\beta+1)R_E}}$

$\Rightarrow \boxed{V_{CE} = V_{CC} - I_C (R_C + R_E)}$ (Same as E-B config)

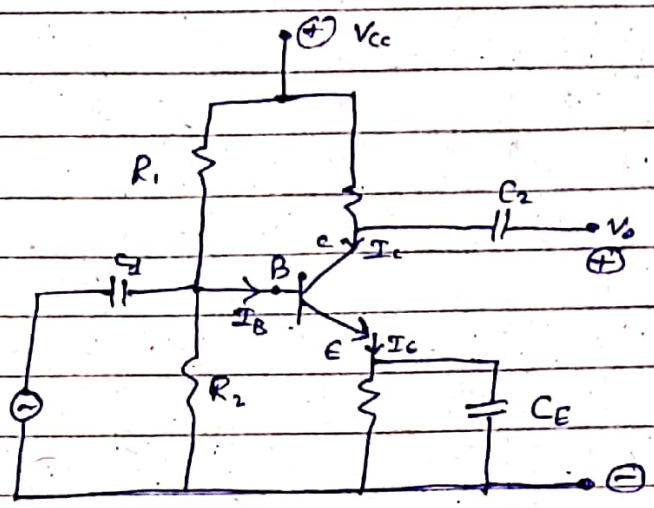
Single - stage CE Amplifier config :-

R_1, R_2, R_E, R_C = Biasing Resistance

C_1, C_2 ⇒ coupling capacitor

CE ⇒ Bypass cap.

coupling capacitor for input



$I_C = \beta I_B$, much larger AC current flows across R_C.

A weak signal is applied to Base, appears in amplified form in Collector. (as $I_C = \beta I_B$)

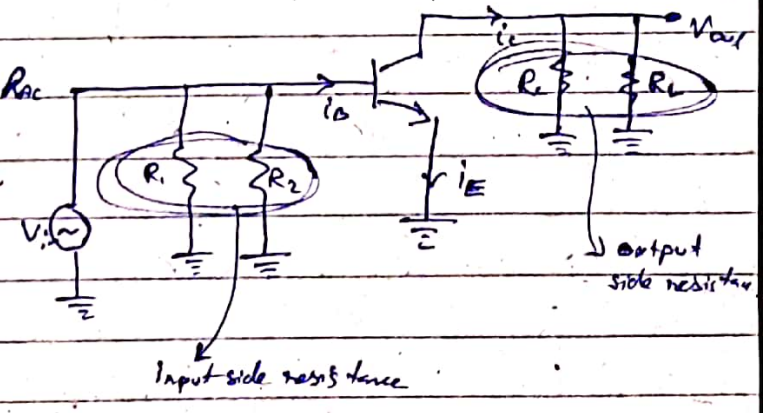
$$A_V = \frac{\text{Amplified Output Voltage}}{\text{Input Voltage.}}$$

Vcc is added to V_{in} and hence V_{out} is amplified

Removing Vcc or (grounding it)

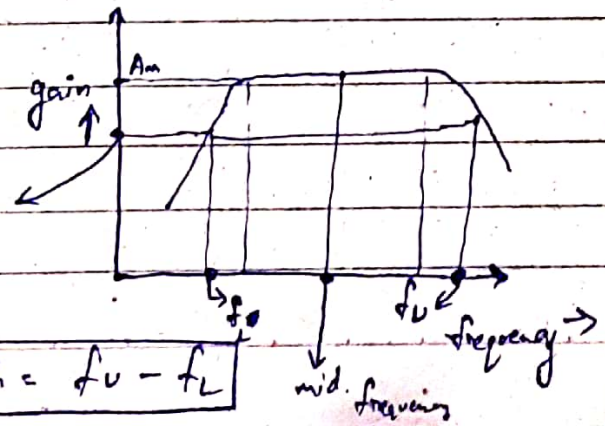
$R_{AC} = R_C \parallel R_L$ ⇒ equivalent of this is R_{ac}

= ac load



V_{out} = output volt.

f_L and f_U = $\frac{1}{\sqrt{2}} \times$ (gain at mid frequency)



Bandwidth = $f_U - f_L$