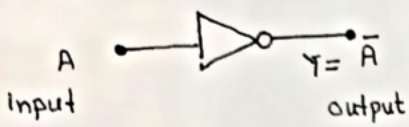
1. Logic Gates :

Logic gates are basic building blocks of digital circuits which are -

- Combinational Circuits : in which output(s) at any instant of time depends on the input(s) applied at the same instant of time.
- Sequential circuits : in which output(s) at any instant of time depends on not only the input(s) applied at the same instant of time but also on past input(s). Thus, sequential circuits have 'memory' and structurally, they have 'feedback'.

Various logic gates :

- NOT (inverter) gate :



Truth table

Input A	output Y
0	1
1	0

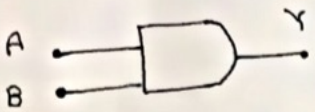
$Y = \bar{A}$

or

$Y = A'$

('_' or '/' represents 'compliment')

- AND Gate :

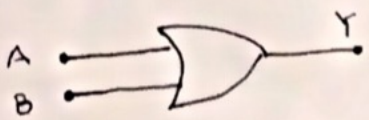


output Y is 1 when both inputs 'A AND B' are 1

A	B	Y
0	0	0
0	1	0
1	0	0
1	1	1

$Y = A.B$

- OR Gate :

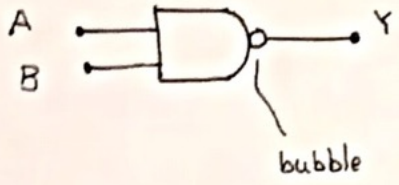


output is '1' when either A OR B is 1 (or both A, B are 1)

A	B	Y
0	0	0
0	1	1
1	0	1
1	1	1

$Y = A + B$

- NAND gate :



A	B	Y
0	0	1
0	1	1
1	0	1
1	1	0

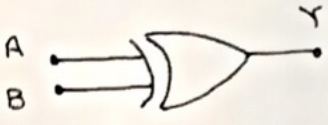
$$Y = \overline{A \cdot B}$$

- NOR Gate :

A	B	Y
0	0	1
0	1	0
1	0	0
1	1	0

$$Y = \overline{A + B}$$

- Ex-OR Gate :

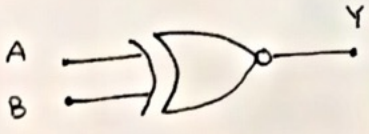


Y is 1 when A OR B is exclusively '1'.

A	B	Y
0	0	0
0	1	1
1	0	1
1	1	0

$$Y = A \oplus B$$

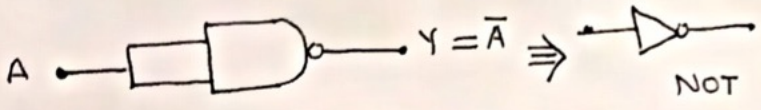
- Ex-NOR Gate :

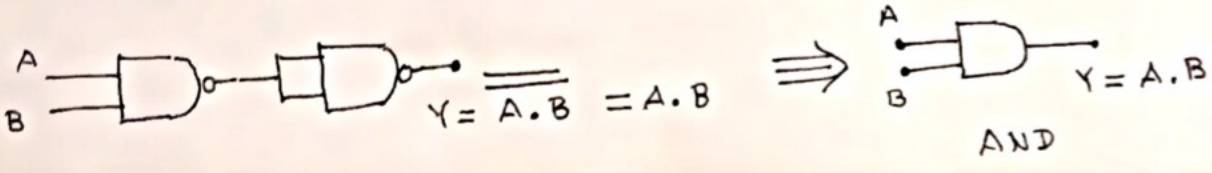


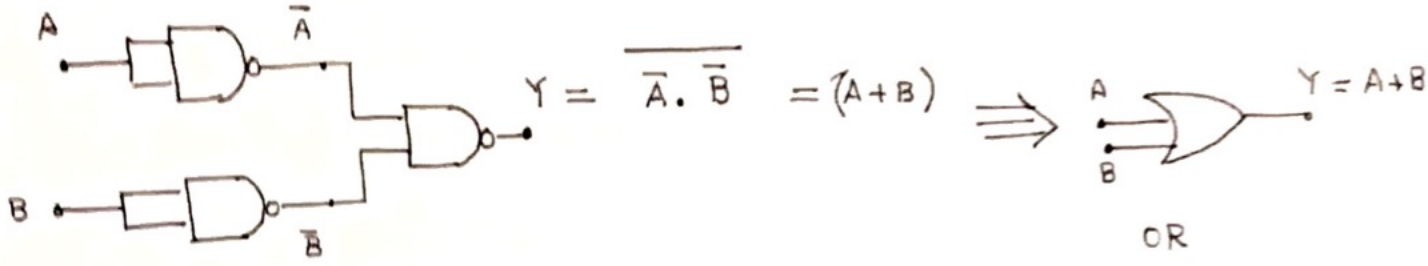
A	B	
0	0	1
0	1	0
1	0	0
1	1	1

$$Y = \overline{A \oplus B}$$

2. NOR and NAND as universal gates :







- De Morgan's Theorem :

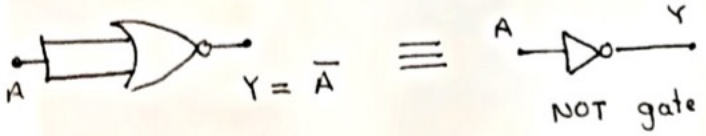
$$\overline{A+B} = \bar{A}.\bar{B}$$

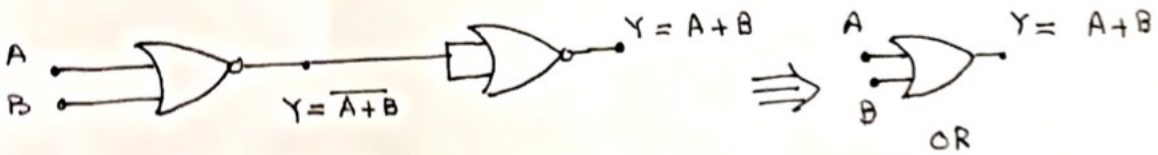
$$\overline{A.B} = \bar{A}+\bar{B}$$

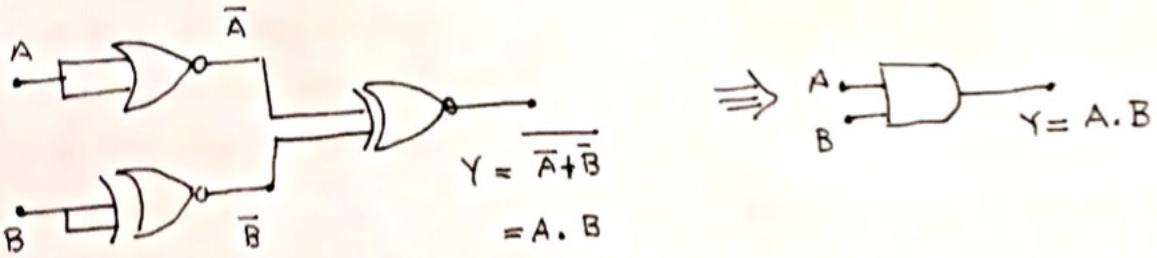
Proof :

A	B	$\bar{A}$	$\bar{B}$	A.B	A+B	$\overline{A+B}$	$\bar{A}.\bar{B}$	$\overline{A.B}$	$\bar{A}+\bar{B}$
0	0	1	1	0	0	1	1	1	1
0	1	1	0	0	1	0	0	1	1
1	0	0	1	0	1	0	0	1	1
1	1	0	0	1	1	0	0	0	0

Same Same







(using De Morgan's Theorem)

Prob. 1 (a) Write truth tables of 3-input AND, OR, NAND and NOR gates

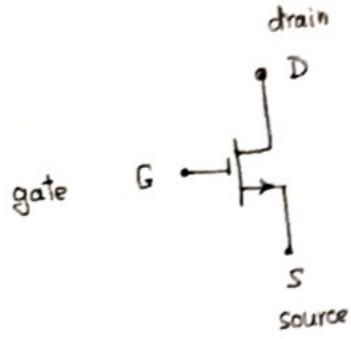
(b) Prove De Morgan's Theorem for 3 variables : i.e

$$\overline{A+B+C} = \bar{A}.\bar{B}.\bar{C}$$

$$\overline{A.B.C} = \bar{A}+\bar{B}+\bar{C}$$

3. Physical realisation of Logic gates :

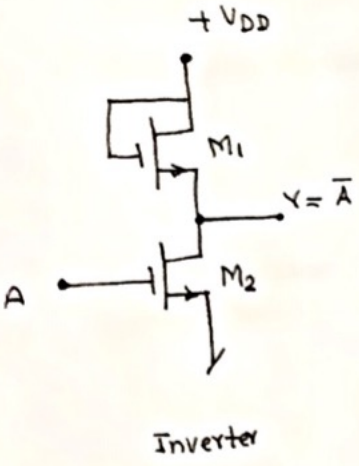
- Resistor - Transistor Logic (RTL)
- Diode - transistor logic (DTL)
- Transistor - transistor - logic (TTL)
- Emitter - coupled - Logic (ECL)
- Complementry - metal - oxide - semiconductor (CMOS) logic gates



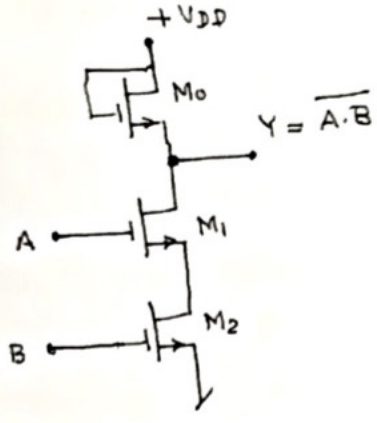
ON : SHORT when $V_{GS} > V_{th}$

OFF : OPEN when V_{GS} is zero (less than V_{th})

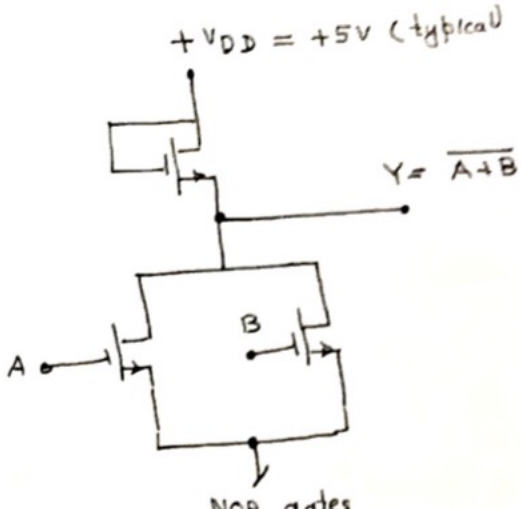
MOS field effect transistor (MOSFETs)



Inverter



NAND gate



NOR gates

n-channel mosfet conducts ("ON") when gate to source voltage is positive ($V_{GS} > V_{th}$) otherwise it is 'OFF'.

4. Logic '0' and Logic '1' levels :

An exemplary definition of logic 1 and logic '0' level is shown. These definitions change based upon how logic gates are implemented.