Reg. No. :

Question Paper Code : 90189

B.E./B.Tech. DEGREE EXAMINATIONS, NOVEMBER/DECEMBER 2019
Fifth Semester
Electronics and Telecommunication Engineering
EC 8552 – COMPUTER ARCHITECTURE AND ORGANIZATION
(Common to Electronics and Communication Engineering)
(Regulations 2017)

Time : Three Hours
Maximum : 100 Marks

Answer ALL questions

PART – A
(10×2=20 Marks)

1. List the registers that are available in the processor.

2. State and explain the performance equation.

3. What are the rules to perform addition on floating point numbers ?

4. What is sub word parallelism ?

5. Define processor clock.

6. What is imprecise and precise exception ?

7. Define hit ratio.

8. Differentiate USB and Firewire.

9. Name the interconnections used in a multi processor system.

10. What is meant by hardware multithreading ?

PART – B
(5×13=65 Marks)

11. a) i) If computer A runs a program in 10 seconds and computer B runs the same program in 15 seconds, how much faster is A than B ? (4)

ii) Describe the different kinds of addressing modes with an example. (9)

(OR)

b) i) A program runs in 10 seconds on computer A, which has a 2 GHz clock. Try to help a computer designer build a computer, B, which will run this program in 6 seconds. The designer has determined that a substantial increase in the clock rate is possible, but this increase will affect the rest of the CPU design, causing computer B to require 1.2 times as many clock cycles as computer A for this program. What clock rate should we tell the designer to target ? (8)

ii) State the advantages of multiprocessor system. (5)

12. a) i) Subtract $(11010)_2 - (10000)_2$ using 1's complement and 2's complement method. **(8)**

    ii) Differentiate arithmetic shift and logical shift. **(5)**

               (OR)

  b) Write down the Booth's algorithm. List the two attractive features of Booth's algorithm. Give an example for worst case of Booth's algorithm. **(5+4+4)**

13. a) Name and explain the two approaches used for generating the control signals in proper sequence. Differentiate the approaches. **(13)**

               (OR)

  b) List the reasons of pipeline conflicts in pipelined processor. How are they resolved ? **(13)**

14. a) What is virtual memory ? Describe the advantages of virtual memory. **(13)**

               (OR)

  b) What is Cache memory ? What are the two ways in which the system using cache can proceed for a write operation ? **(13)**

15. a) i) List the characteristics of Graphics Processing units. **(8)**

    ii) Differentiate in-order execution and out-of-order execution. **(5)**

               (OR)

  b) Explain in detail, the shared memory multiprocessor, with a neat diagram. **(13)**

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PART – C   **(1×15=15 Marks)**

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16. a) i) Use the Booth and bit-pair recording techniques to multiply $(-10 \times -10 = 100)_{10}$. **(10)**

    ii) List the rules to perform addition on floating point numbers. **(5)**

               (OR)

  b) i) Compare UMA and NUMA multiprocessors. **(5)**

    ii) A virtual memory has a page size of 1K words. There are eight pages and four blocks. The associative memory page table contains the following entries. **(10)**

Page	Block
0	3
1	1
4	2
6	0

Make a list of all virtual address (in decimal) that will cause a page fault if used by the CPU.