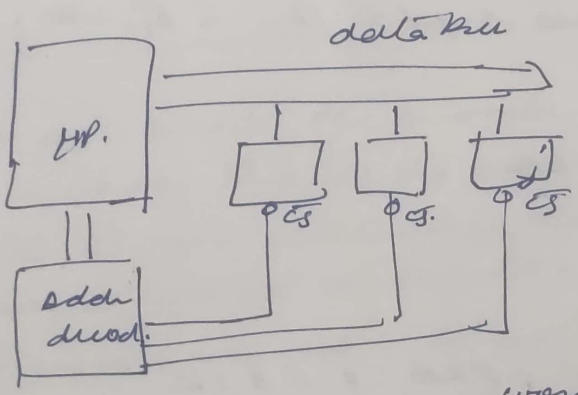
Memory Interfacing

Eg Design an 8085 system
8K EPROM using 4KB chips and 16KB RAM using 8KB chips

When µP generate an address only the chip whose address is given should be selected.

① When addr given by µP goes to decoder the decoder selects the chip and the data from the data bus enters into the selected chip



working at 3MHz.

Eg Design an 8085 system with 8K EPROM using 4KB chips and 16KB RAM. using 8KB chips

Memory calculation

EPROM: Required – 8KB
Available – 4KB.

No of chips – 2 required

Size of single chip – 4KB. = $4 \times 1KB$.
$= 2^2 \times 2^{10}$
$= 2^{12}$

∴ 12 address lines reqd.

Size of the address bus can be used to calculate the size of the memory.

If n addr lines then size of memory is 2^n.

Also from size of memory we can find no of address lines.

µP has 16 address lines but all are not reqd to go to the chip. Only the reqd address lines need to go to the chip.

In this case the size of the chip given = 4KB.

∴ No. of address lines reqd = 12. = $A_{11} - A_0$

RAM

Required. = 16 KB

Available - 8 KB.

No. of chips = 2.

Size of single chip = 8KB = $8 \times 1K$

$= 2^3 \times 2^{10} = 2^{13}$

∴ 13 addr lines reqd = $A_{12} - A_0$.

∴ Addr lines reqd in EPROM = 11

" " " for RAM = 13.

Addr Bus.

Chip	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0	Hex Addr
ROM 1 Begins	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0000H.
Ends.	0 0 0 0	1 1 1 1	1 1 1 1	1 1 1 1	0FFFH.
EPROM 2 Begins	0 0 0 1	0 0 0 0	0 0 0 0	0 0 0 0	1000H.
	0 0 0 1	1 1 1 1	1 1 1 1	1 1 1 1	1FFFH.
RAM 1	0 0 1 0	0 0 0 0	0 0 0 0	0 0 0 0	2000H.
	0 0 1 1	1 1 1 1	1 1 1 1	1 1 1 1	3FFFH.
RAM 2	0 1 0 0	0 0 0 0	0 0 0 0	0 0 0 0	4000H.
	0 1 0 1	1 1 1 1	1 1 1 1	1 1 1 1	5FFFH.

Whenever µP reset PC becomes 0000. So the 1st adder is 0000. This is the adder of the BIOS to load the OS and initialize the chips. This BIOS program is stored at location 0000. So this program should never be lost. So we have to store in EPROM and not write RAM.

BIOS program cannot be stored in RAM. as it can be erased and lost. In ROM in EPROM and ROM to RAM.

To calculate EPROM 1 ending adder :-

3 addr lines are going in the chip.

When you're calculating the ending adder. you are adding the addr lines calculated for EPROM to 0000H. Since last 4 bits are not taken the 15th to 12th bit 1111 + 0000 will be carried forward Also line A_{11} has a 0 + 1 = 1

If 1st step was 1 + 1 = 10 So 0 1 (A_{12})

0000 – 0FFF 4KB] 8KB
+1000 – 1FFF 4KB

So 2000 – 3FFF will be 8KB.

RAM → 2000 – 3FFF.

Next 8K → 4000 – 5FFF

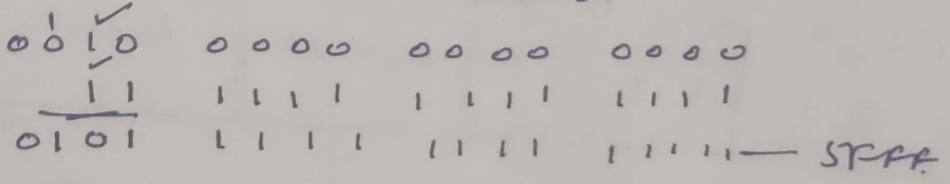
Eg for carry

Suppose it was 16 KB chip it should.

$16 \times 1K = 2^4 \times 2^{10} = 14$ lines.

↓

2000 – start addr.



Map is a plan.

Circuit for the implementation. is as follows

0000 – 0FFF 4KB] 8KB
+1000 – 1FFF 4KB]

So 2000 – 3FFF will be 8KB.

RAM → 2000 – 3FFF.

Next 8K → 4000 – 5FFF

Eg for carry

Suppose it was 16 KB chip it should.

$16 \times 1K = 2^4 \times 2^{10} = 14$ lines.

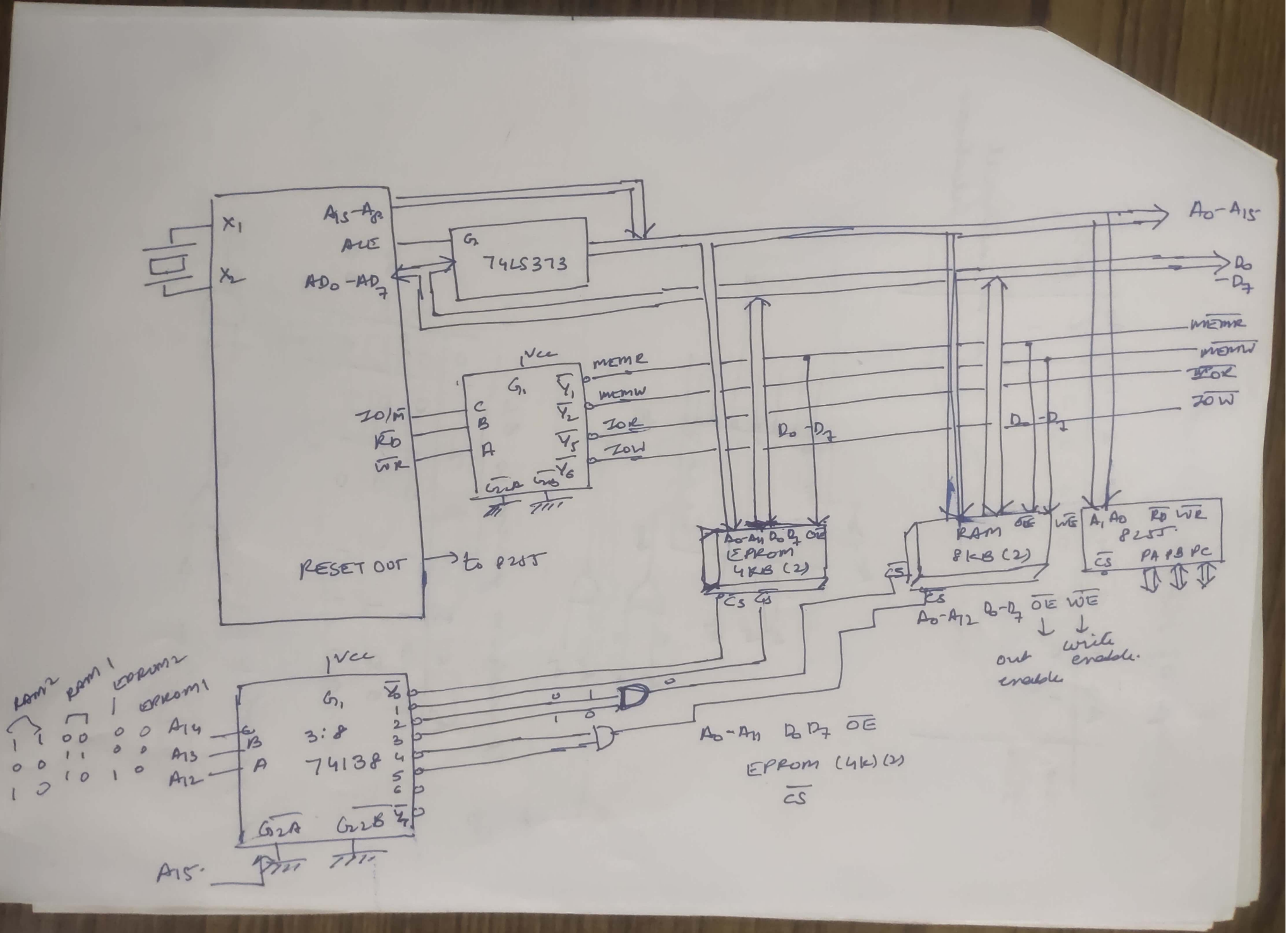
↓

2000 – start addr.

0010 0000 0000 0000
11 1111 1111 1111
0101 1111 1111 1111 — 5FFF

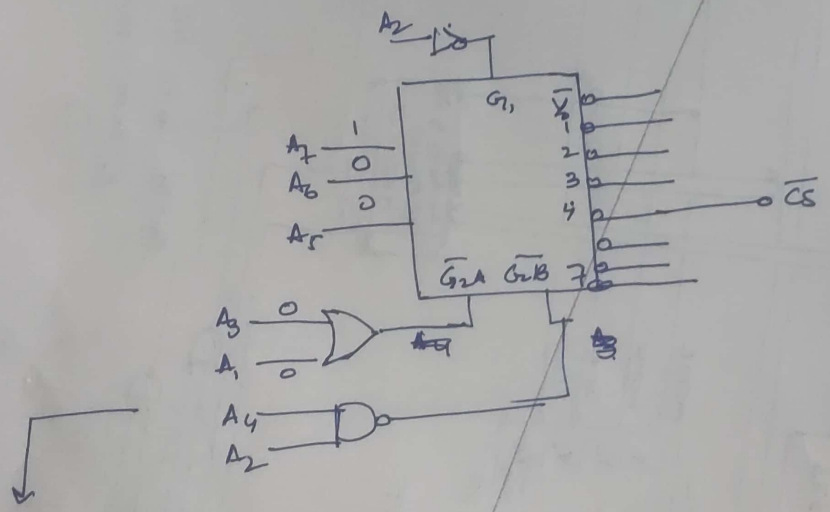
Map is a plan.

Circuit for the implementation is as follows


X1
X2
A15-A8
ALE
AD0-AD7
RESET OUT
to 8255
G2
74LS373
A0-A15
D0-D7
MEMR
MEMW
IOR
IOW
IO/M
RD
WR
Vcc
G1
C
B
A
Y1
Y2
Y5
Y6
G2A
G2B
D0-D7
A0-A10 D0 D7 OE
EPROM
4KB (2)
CS
RAM
8KB (2)
WE
A1 A0 RD WR
8255
PA PB PC
A0-A12 D0-D7 OE WE
out enable
write enable
RAM2
RAM1
EPROM2
EPROM1
A14
A13
A12
3:8
74138
Y0
Y7
A15
A0-A11 D0 D7 OE
EPROM (4K) (2)
CS

I/O Map of 8259.

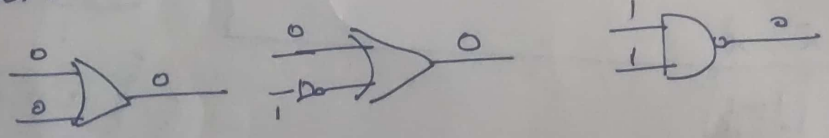
	A_7	6	5	4	3	2	1	A_0	
ICW1	1	0	0	0	0	0	0	0	80H
ICW2								1	
								1	Internal Selection
								1	



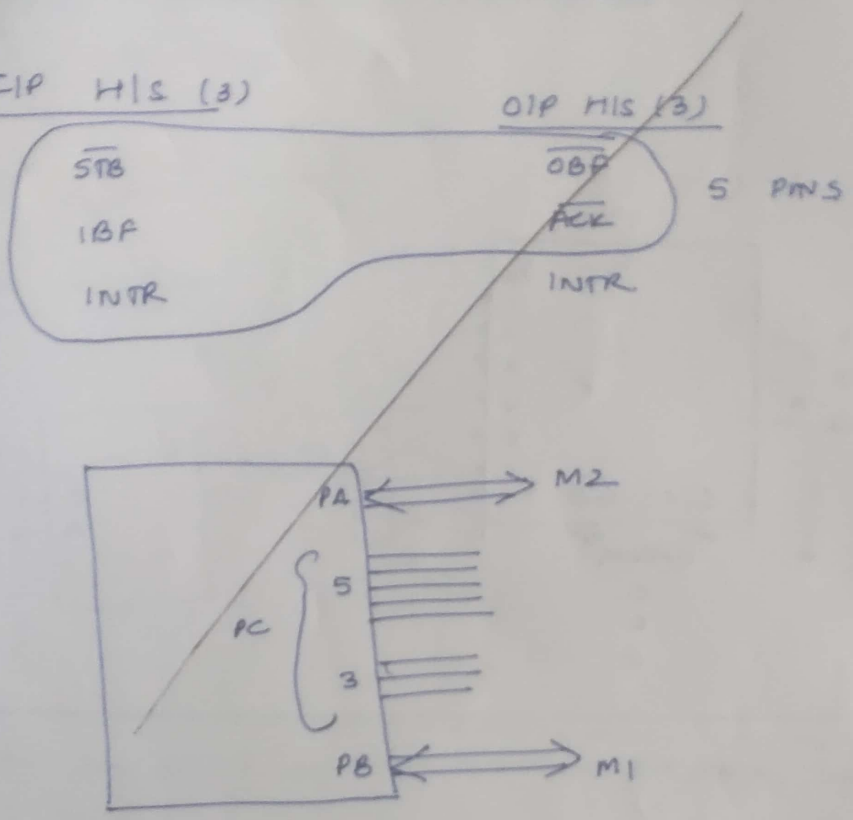
Eg If address given is 34.

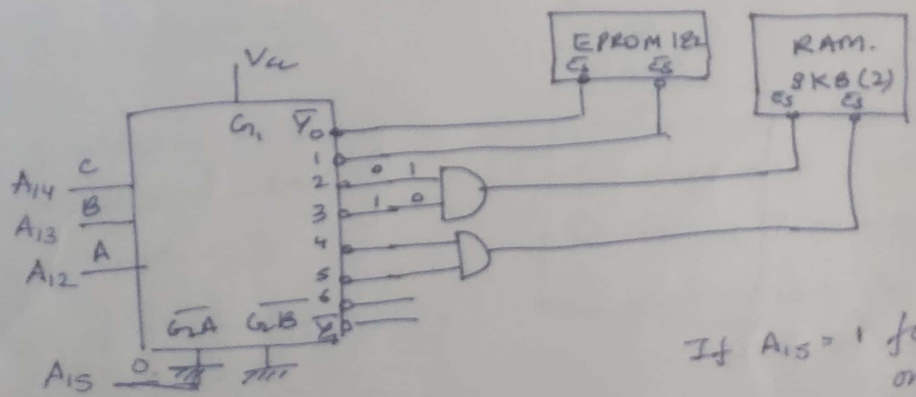
A_7	6	5	4	3	2	1	0	
0	0	1	1	0	1	0	0	– 34
0	0	1	1	0	1	0	1	– 35
0	0	1	1	0	1	1	0	36

In general.

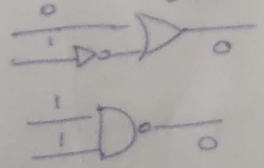


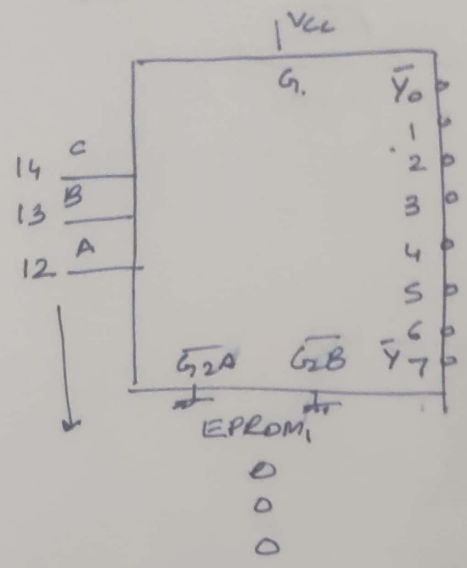
ODE 2 – BIDIRECTIONAL HANDSHAKE

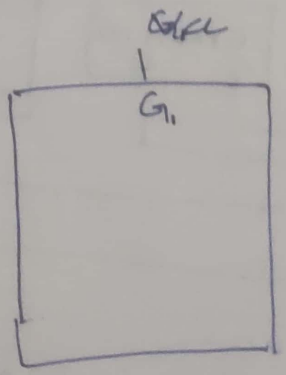




If A_{15} = 1 for any one chip then

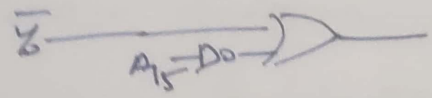



Vcc
G1
$\bar{Y}_0$
1
2
3
4
5
6
$\bar{Y}_7$
14 C
13 B
12 A
$\bar{G}_{2A}$
$\bar{G}_{2B}$
EPROM1

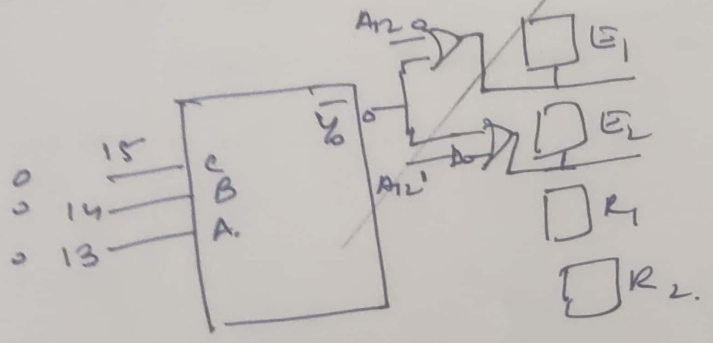

Vcc
G1

in this case happens to be 0 so can be connected to ground terminal of the decoder.

If $A_{15} = 1$ for any chip



Alternate Solution



Q. Design an 8085 system working on 3 MHz clock. with
8K EPROM using 4KB chips and
16 KB RAM using 8KB chips

Memory calculation

EPROM:

① Required = 8KB
② AVAILABLE = 4KB
③ No of CHIPS = 2
④ Size of Single chip
= 4KB = 4 × 1KB
= $2^2 \times 2^{10}$
= 2^{12}

∴ Addr lines reqd
= 12

RAM:

① Required = 16KB
② Available = 8KB chips
③ No. of chips reqd = 2
④ Size of single chip
= 8KB = 8 × 1KB
= $2^3 \times 2^{10}$
= 1^{13}

∴ Addr lines reqd
= 13.

MODES

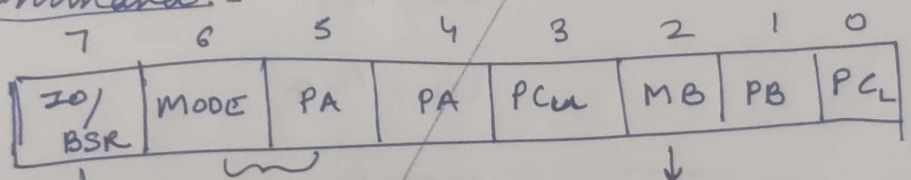
MODE 0 – SIMPLE I/O

MODE 1 – Handshaking

MODE 2 – Bidirectional handshake mode

	M0	M1	M2
	Simple	Handshake	Bidirectional
PA	✓	✓	✓
PB	✓	✓	M1 | M0
PC	✓	X → HS	X → HS.

I/O Command –



D_7 – I/O – 1 BSR – 0

$D_6 D_5$ – Mode 0 – 00 Mode 1 – 01 Mode 2 – 1x

D_4 – PA → I/P Port – 1 O/P Port – 0

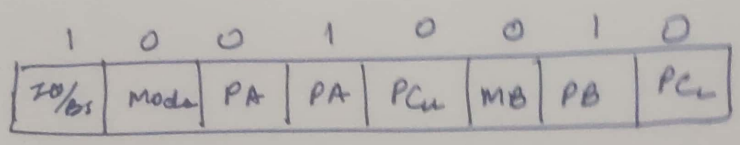
D_1 – PB → 1 – I/P 0 – O/P

D_2 – Port B mode 0 – 0 Port B mode – 1 – 1

PC_U – 1 – I/P 0 – O/P

PC_L – 1 – I/P 0 – O/P.

Eg



- 92H

PA - Mode - 0
PB - " 0
PC Mode 0 - O/P.

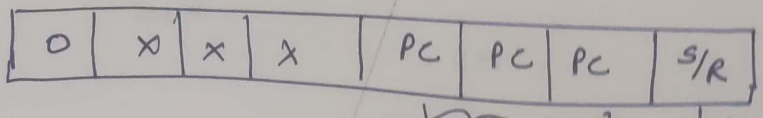
] INFERENCE

8086 - MOV AL, 92H
OUT 86H, AL

8085 - MVI A, 92H
OUT 83H

BSR Command :- Only for Port C

CW.



Select a bit
000 - PC_0
⋮
111 - PC_7

1 - Set
0 - Reset