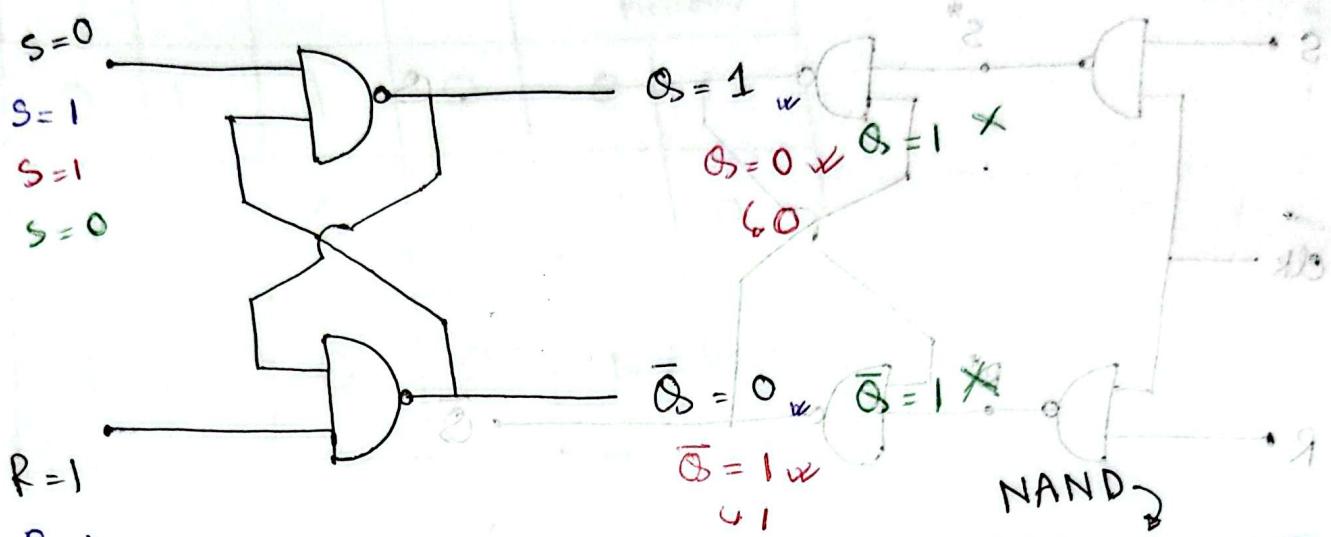
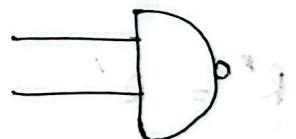


* SR Latch using Nand Gate



A	B	Output
0	0	1
0	1	1
1	0	0
1	1	0

S	R	Q	\bar{Q}
0	0	Not change Used X	
0	1	1	0
1	0	0	1
1	1	Memory / No change Not Used	

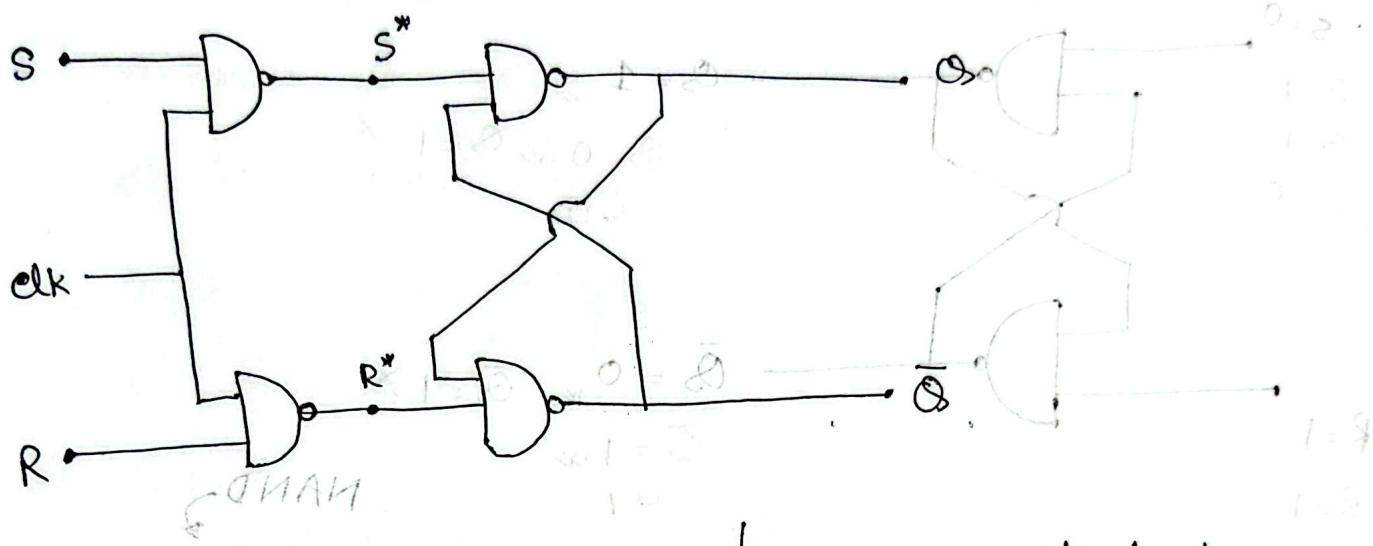


NAND GATE

S-R

S-R Flip-Flop

broad gates noted 92 *



Inputs	Q	Q̄
1 1	1	0
1 0	0	1
0 1	1	0

$= S'$

$$R^* = R'$$

STATE GUAR

} For a circuit to be a working flip-flop the clock pulse need to be 1

(also broad noted to 1)

	2	3	4	5
x	0	0	0	0
clock	0	1	1	0
Q	0	1	1	0
Q̄	1	0	0	1

$\therefore S^*_1 = S' / \bar{S}$

$\therefore R^* = R' / \bar{R}$

spuriously present
but off

Truth Table of SR flip-flop without Q1Q2Q3

S	R	S^*	R^*	Q	Q'
0	0	1	1	No change / Memory	
0	1	1	0	0	1
1	0	0	1	1	0
1	1	0	0	Not Used	

Ignore latch inputs

(SR Flip-Flop Table)

S	R	Q	Q'
0	0	1	Memory / No change
0	1	1	0
1	0	0	1
1	1	1	Not used

1	0	1	0
0	1	0	1
1	0	1	0
0	1	0	1
1	1	1	1

S-R Flip-Flop Truth + Characteristics Table

* S-R Flip-Flop Truth Table

S	R	Q	Q'
0	0	Memory	No Change
0	1	0	1
1	0	1	0
1	1	Not Used	

S	R	Q	Q'	Q _{old}	Q _{new}	Q _{old}	Q _{new}	Q _{old}	Q _{new}
0	0	0	1	0	0	1	1	0	0
0	1	0	1	1	0	1	0	1	0
1	0	1	0	0	1	0	0	1	1
1	1	Not Used		0	0	0	1	1	1

Excitation Table

Q	Q'	S	R
0	0	0	X
0	1	1	0
1	0	0	1
1	1	X	0

As values
are different
(0,1) so
don't care
X

Characteristics Table

$Q(t)$	S(t)	R(t)	$Q(t+1)$
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	Indeterminate
1	0	0	0
1	0	1	1
1	1	0	0
1	1	1	Indeterminate

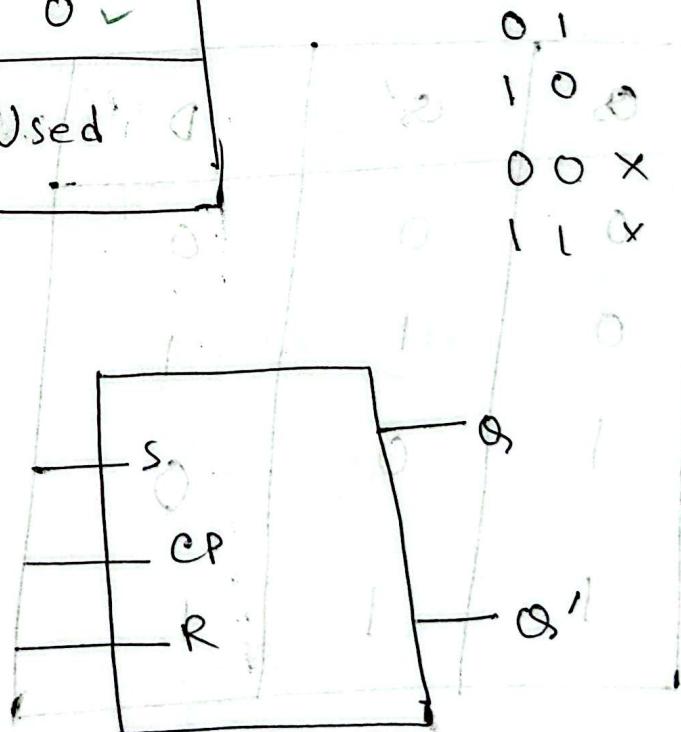
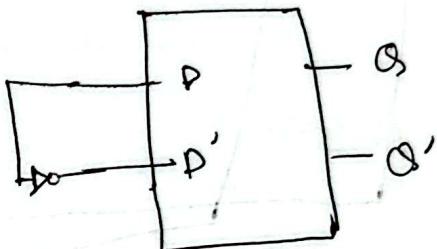
D Flip-Flop: 9/17/2023 9:00 AM

D	Q	Q'
0	0	1
1	1	0

For solving this problem we use D-Flip-Flop

SR Flip-Flop:

S	R	Q	Q'
0	0	Memory / No Change	
0	1	0 ✓	1 ✓
1	0	1 ✓	0 ✓
1	1	Not Used	



D-Flip-Flop Characteristic Table using D-Flip-Flop Truth Table

Table →

D-Flip-Flop Truth Table

D	Q	Q'
0✓	0✓	1
1✓	1✓	0

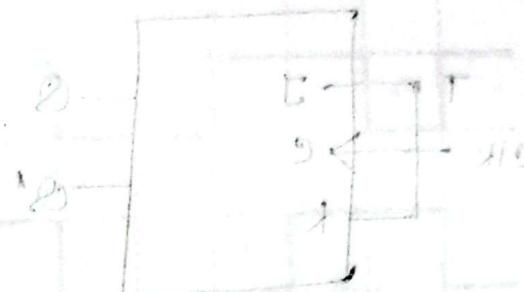
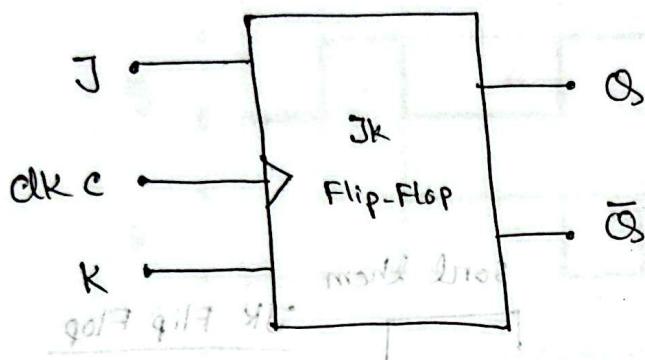
Characteristic Table

Q(t)	D	Q(t+1)
0	0✓	0✓
0	1✓	1✓
1	0✓	0✓
1	1✓	1✓

D-Flip-Flop Excitation Table:

Q _s	Q' _s	D	b1	b2	b3	b4	b5
0	0	0	0	0	0	0	0
0	1	1	1	1	1	1	1
1	0	0	0	0	0	0	0
1	1	1	1	1	1	1	1

J-K Flip-Flop



Characteristics Table:

Q_k	J	K	C	$Q_{(k+1)}$
0	0	0	1	0
0	0	1	1	0
0	1	0	1	1
0	1	1	1	1
1	0	0	1	1
1	0	1	0	1
1	1	0	0	0
1	1	1	0	0

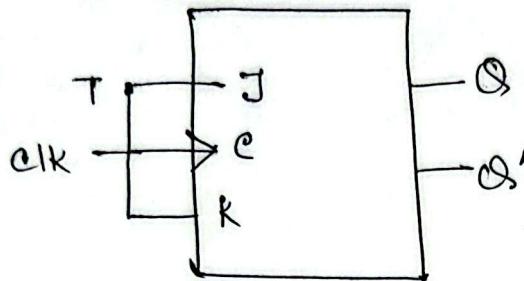
only this part is different from S-R flip-flop

J	K	Q_k	$Q_{(k+1)}$
0	0	0	Memory / No change
0	1	0	1
1	0	1	0
1	1	1	Toggle

Excitation Table

Q	Q^+	J	K
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

T - Flip-Flop



T-Flip Flop Table

T	Q	Q'
0	No Change	
1	Toggle	

Characteristic Table:

Q	T	Q(t+1)
0	0	0
0	1	1
1	0	0
1	1	0

Annotations: "No change" points to rows 1 and 3. "Toggle" points to rows 2 and 4.

sort them

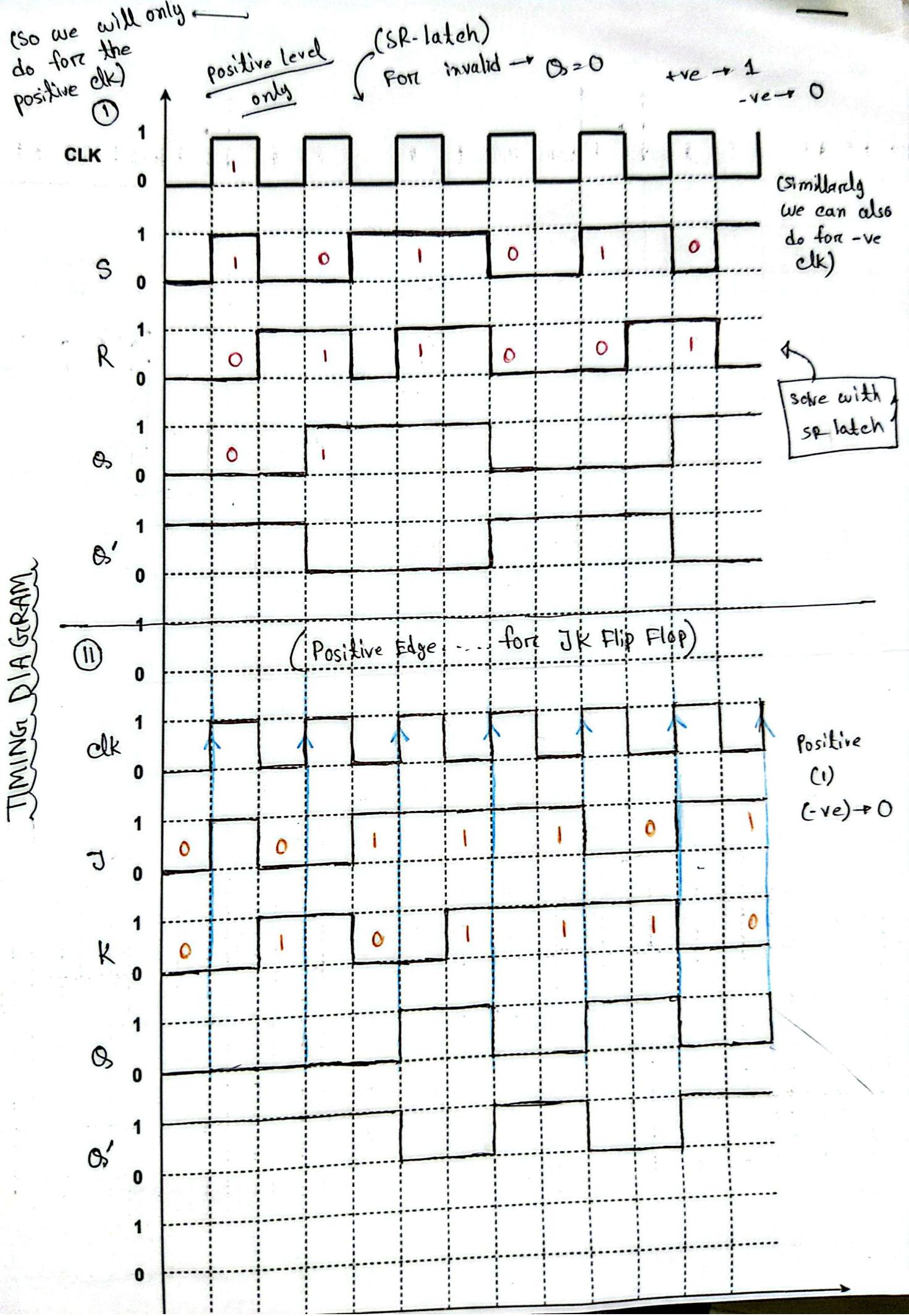
JK Flip Flop

J	K	Q	Q'
0	0	Memory/No change	
0	1	0	1
1	0	1	0
1	1	0	1

IT

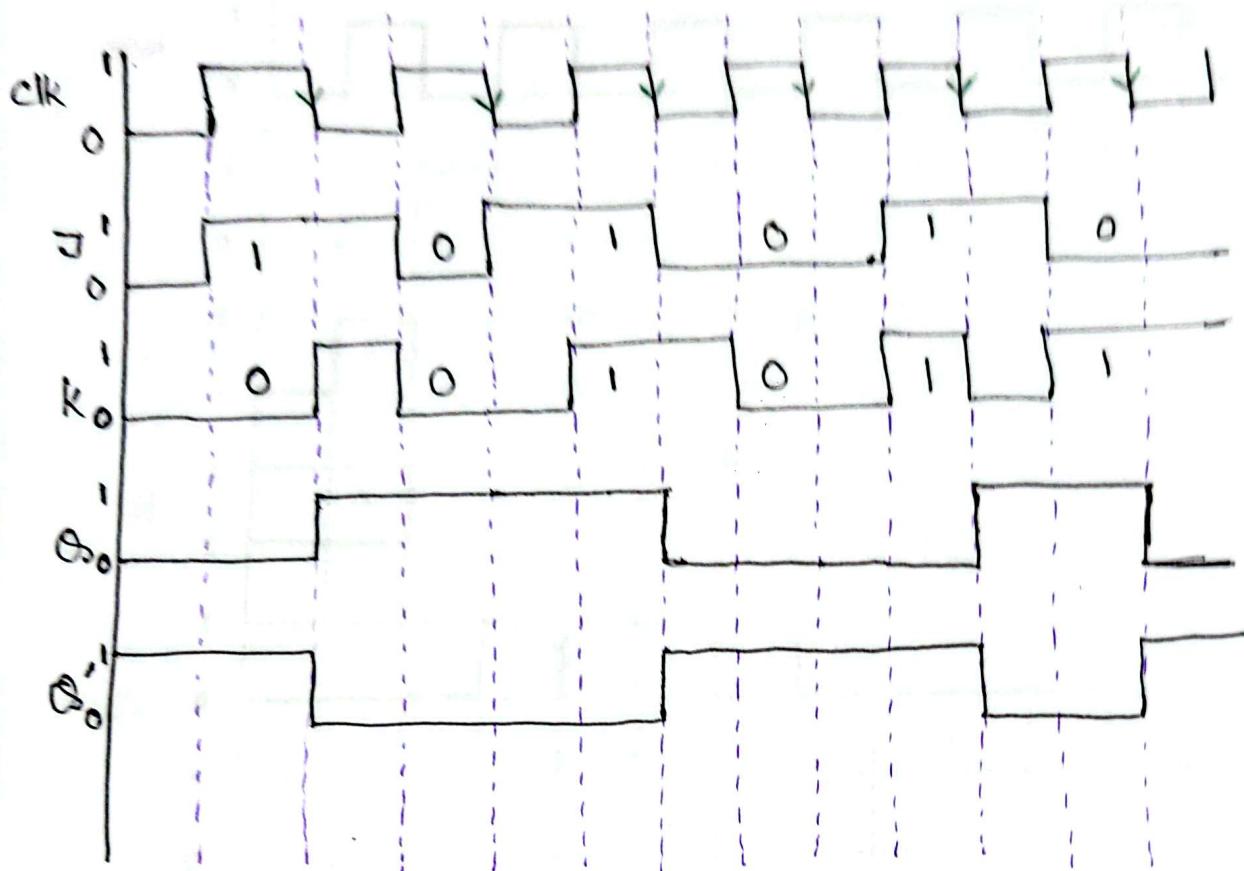
Excitation Table

Q	Q ⁺	T
0	0	0
0	1	1
1	0	1
1	1	0



TIMING DIAGRAM

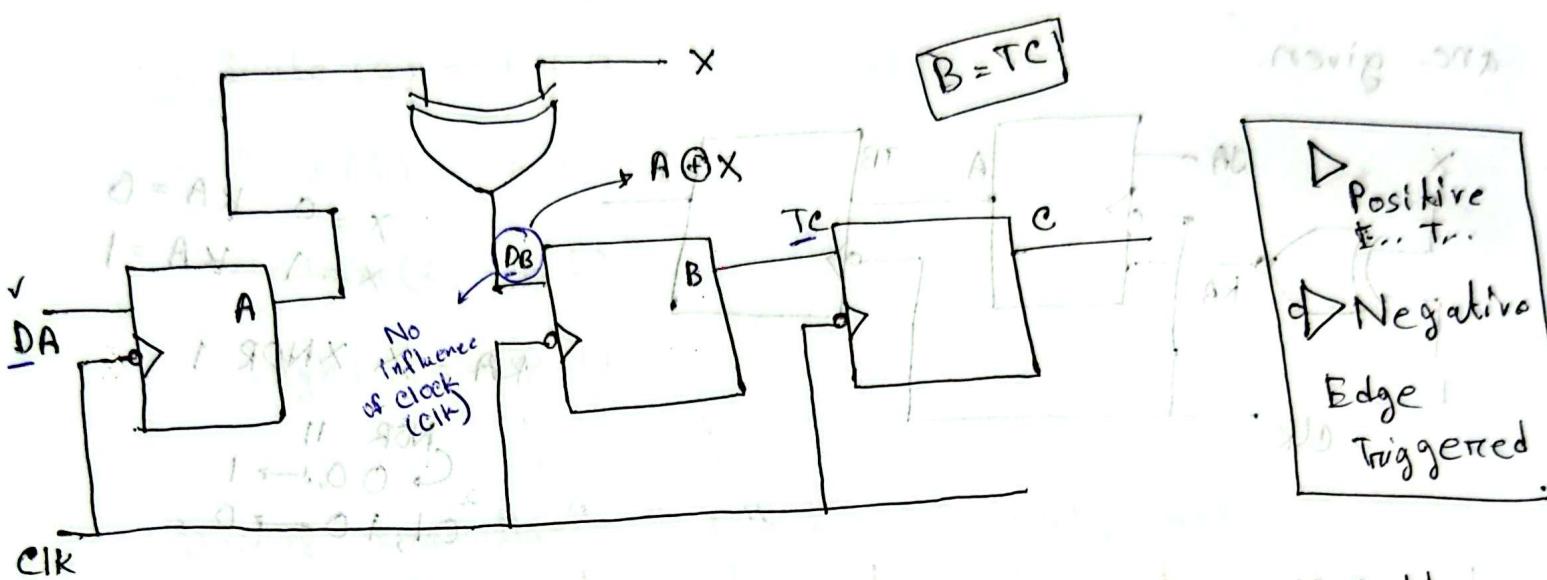
Negative Edge Triggered Diagram (JK flip flop)



JK FF Truth Table

J	K	Q	Q'
0	0	No change	
0	1	0	1
1	0	1	0
1	1		Toggle

DRAW Timing Diagram for A, DB, B and C.

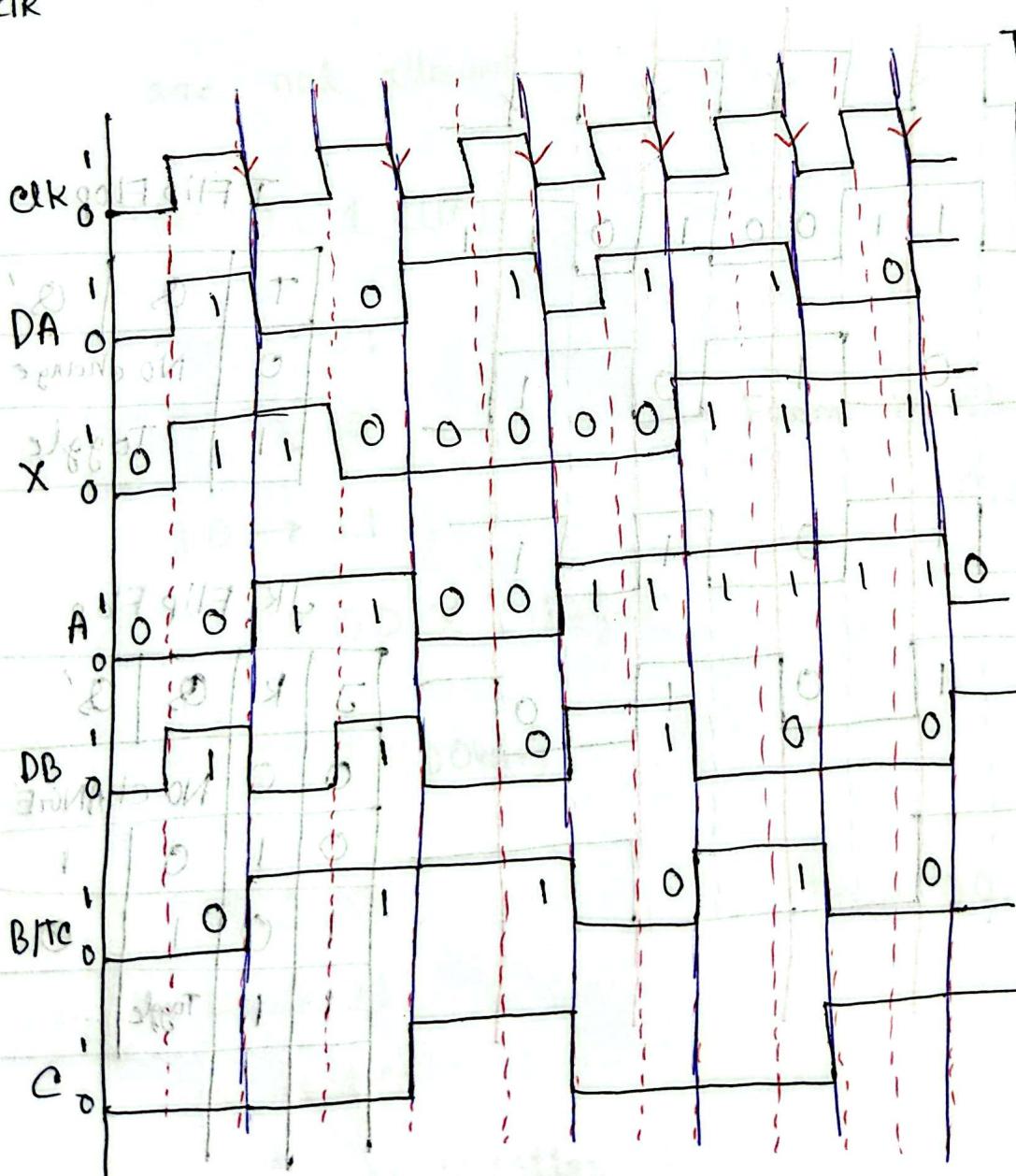


T-FF Truth Table

T	Q	Q'
0	No change	
1	Toggle	

D-FF Truth Table

D	Q	Q'
0	0	1
1	1	0



$$\begin{aligned} \text{XOR } 00, 11 &\rightarrow 0 \\ 01, 10 &\rightarrow 1 \end{aligned}$$

DRAW and Complete the Timing Diagram for the
following circuit. Clock Pulse (Clk), JA, and X waveforms
are given.

