SNEHA KATTEPURA CHANDRASHEKAR

+1 650-531-9050 | skattepu@ucsc.edu | Fremont, CA
https://www.linkedin.com/in/snehakchandrashekar | https://github.com/snehakchandrashekar

SUMMARY

MS Electrical and Computer Engineering student with expertise in Hardware ASIC design with strong academic and practical experience in digital systems and VLSI design. Seeking to apply expertise in hardware development and RTL design to innovative semiconductor projects, contributing to advanced technology solutions in a collaborative engineering environment.

EDUCATION

University of California Santa Cruz, USA Sept 2023 - May 2025
M.S, Electrical and Computer Engineering GPA: 4/4

The National Institute of Engineering, India Aug 2014 - May 2018
B.E, Electrical and Electronics Engineering GPA:8.87/10

TECHNICAL SKILLS

Programming and Scripting Languages: SystemVerilog, Verilog, Python, C++, C, Tcl, Perl

RTL Design: Static Timing Analysis, Clock Domain Crossing, FSM, FIFO depth, Clock divider, Clock gating

Verification: SystemVerilog Assertions, Functional Coverage, UVM

Protocols: AXI, AMBA

Operating Systems: Linux, Windows

Relevant Skills: Digital design, VLSI Design, RTL Design, FPGAs, Object-Oriented Programming, CMOS Transistors

WORK EXPERIENCE

Baskin Engineering, UC Santa Cruz, Teaching Assistant Jan 2024 - Present

- Led instructional lab sessions for the Analog Electronics Laboratory course, worked under professors to help frame coursework, provided hands-on guidance through projects and experiments, and assisted in managing and grading

Accenture Solutions Pvt. Ltd, Application Development Analyst June 2018 - Nov 2021

- Independently designed .NET-based utilities that decreased user workload by 40%, significantly improving performance and user experience
- Automated the file import/export process, reducing time by up to 70% by collaborating with cross-functional teams to reduce manual work, demonstrating strong teamwork

PROJECT EXPERIENCE

RTL Design and Functional Verification of FIFO in System Verilog

- Designed synchronous and asynchronous FIFO with memory blocks, and implemented elastic pipelines using SystemVerilog, integrating ready-valid handshake protocols to optimize data flow and transfer, ensuring seamless operation on FPGA platforms
- Conducted comprehensive functional verification for all designs by writing and executing detailed test cases, debugging errors, and ensuring protocol compliance while reducing data transfer errors

4x4 Multiplier Using Shift-and-Add Algorithm in Verilog

- Designed and implemented a 4x4-bit sequential multiplier using the shift-and-add algorithm, achieving optimal area utilization and efficient performance for small arithmetic operations
- Successfully verified the design through extensive simulation, ensuring correct functionality and timing across multiple test cases, with a focus on low-resource hardware environments

8-bit Arithmetic Logic Unit (ALU) Design in Verilog

- Designed and implemented an 8-bit ALU capable of performing fundamental arithmetic and logical operations, including addition, subtraction, AND, OR, XOR, and shift operations, optimized for performance and resource efficiency
- Verified the ALU through simulation, ensuring accurate operation across a range of inputs, with a focus on low latency and minimal area utilization

RELEVANT COURSES

- Logic Design with Verilog | Asic Systems Design (System Verilog)| Advanced VLSI Design | Computer Architecture