

Quiz 1

Submitted By:
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2016201

//quiz.v

`timescale 1ns / 1ps

//

// Company:

// Engineer:

//

// Create Date: 08/21/2017 12:36:32 AM

// Design Name:

// Module Name: quiz

// Project Name:

// Target Devices:

// Tool Versions:

// Description:

//

// Dependencies:

//

// Revision:

// Revision 0.01 - File Created

// Additional Comments:

//

//

module quiz(

input a1,

input a2,

input a3,

input a4,

```
input b1,  
input b2,  
input b3,  
input b4,  
output reg c,  
output reg d  
);
```

```
always@(*)  
begin  
if (a3 == 1 & b3 == 0)  
begin  
c=1;  
d=0;  
end  
else if(b3 == 1 & a3 == 0)  
begin  
c=0;  
d=1;  
end  
else if(a2 == 1 & b2 == 0)  
begin  
c=1;  
d=0;  
end  
else if(a2 == 0 & b2 == 1)  
begin  
c=0;  
d=1;  
end  
else if(a1 == 1 & b1 == 0)  
begin  
c=1;
```

```
d=0;
end
else if(a1 == 0 & b1 == 1)
begin
c=0;
d=1;
end
else if(a4 == 1 & b4 == 0)
begin
c=1;
d=0;
end
else if(b4 == 1 & a4 == 0)
begin
c=0;
d=1;
end
else
begin
c=1;
d=1;
end
end
```

endmodule

//cons.xdc

```
set_property PACKAGE_PIN F22 [get_ports {a1}]
set_property IOSTANDARD LVCMOS33 [get_ports {a1}]
set_property PACKAGE_PIN G22 [get_ports {a2}]
set_property IOSTANDARD LVCMOS33 [get_ports {a2}]
set_property PACKAGE_PIN H22 [get_ports {a3}]
set_property IOSTANDARD LVCMOS33 [get_ports {a3}]
```

set_property PACKAGE_PIN F21 [get_ports {a4}]
set_property IOSTANDARD LVCMOS33 [get_ports {a4}]
set_property PACKAGE_PIN H19 [get_ports {b1}]
set_property IOSTANDARD LVCMOS33 [get_ports {b1}]
set_property PACKAGE_PIN H18 [get_ports {b2}]
set_property IOSTANDARD LVCMOS33 [get_ports {b2}]
set_property PACKAGE_PIN H17 [get_ports {b3}]
set_property IOSTANDARD LVCMOS33 [get_ports {b3}]
set_property PACKAGE_PIN M15 [get_ports {b4}]
set_property IOSTANDARD LVCMOS33 [get_ports {b4}]
set_property PACKAGE_PIN T22 [get_ports {d}]
set_property IOSTANDARD LVCMOS33 [get_ports {d}]
set_property PACKAGE_PIN U14 [get_ports {c}]
set_property IOSTANDARD LVCMOS33 [get_ports {c}]