Lab 9
Submitted By:
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2016201

```
//top.v
`timescale 1ns / 1ps
//////////////////////////////////////////////////////////////////////////////////
// Company:
// Engineer:
//
// Create Date: 26.10.2017 01:44:22
// Design Name:
// Module Name: top
// Project Name:
// Target Devices:
// Tool Versions:
// Description:
//
// Dependencies:
//
// Revision:
// Revision 0.01 - File Created
// Additional Comments:
//
//////////////////////////////////////////////////////////////////////////////////


module top(
    input Clock,
    input Reset,
    input go,
    input [5:0] A,
    input [5:0] B,
    output [6:0] cathode,
    output anode,
    output [3:0] anode1,
    output [7:0] cathode1,
    output Done
    );
    wire [5:0] out_ans;
    wire [3:0] ones,tens,num,ones1,tens1,ones2,tens2;
    clk_div CD1(.mclk(Clock),.clk190(clk_190));
```

```
    debounce D1(.clk_in(clk_190),.clr_in(Reset),.clr_out(clr_de));
    debounce D2(.clk_in(clk_190),.clr_in(go),.clr_out(btn));
    clk_pulse cp1(.inp(btn),.cclk(clk_190),.clr(clr_de),.outp(out_pulse));
    gcd(Clock,clr_de,out_pulse,A,B,Done,out_ans);
    binary2bcd(.number(out_ans),.ones(ones),.tens(tens));
    binary2bcd(.number(A),.ones(ones1),.tens(tens1));
    binary2bcd(.number(B),.ones(ones2),.tens(tens2));
    disp_sevenseg(Clock,ones1,tens1,ones2,tens2,anode1,cathode1);
    pmodco p1(.ones(ones),.tens(tens),.cathode(cathode),.anode(anode),.clock_in(Clock));
endmodule


//clk_div.v
`timescale 1ns / 1ps
module clk_div(
input wire mclk,
output wire clk190);
reg [18:0] q;
always @(posedge mclk)
begin
q <= q+1;
end
assign clk190 = q[18];
endmodule

//disp_sevenseg.v
`timescale 1ns / 1ps
//////////////////////////////////////////////////////////////////////////////////
// Company:
// Engineer:
//
// Create Date: 23.09.2017 02:17:04
// Design Name:
// Module Name: disp_sevenseg
// Project Name:
// Target Devices:
// Tool Versions:
// Description:
//
// Dependencies:
//
// Revision:
// Revision 0.01 - File Created
```

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// Additional Comments:
//
//////////////////////////////////////////////////////////////////////////////////


module disp_sevenseg(
    input clock_in,
    input [3:0] ones,
    input [3:0] tens,
    input [3:0] hundreds,
    input [3:0] thousands,
    output [3:0] anode,
    output [7:0] cathode
    );
    reg [17:0] count;
    always@(posedge clock_in)
    begin
    count <= count+1;
    end
    reg [6:0] sseg_temp;
    reg [6:0]sseg;
    reg [3:0] an_temp = 4'b1110;
    always @ (*)
     begin
      case(count[17:16])
       2'b00 :
        begin
         sseg = ones;
         an_temp = 4'b1110;
        end
       2'b01:
        begin
         sseg = tens;
         an_temp = 4'b1101;
        end
       2'b10:
        begin
         sseg = hundreds;
         an_temp = 4'b1011;
        end
       2'b11:
        begin
         sseg = thousands;
```

```
        an_temp = 4'b0111;
       end
     endcase
    end
   assign anode = an_temp;
   always @ (*)
    begin
     case(sseg)
      4'd0 : sseg_temp = 7'b0000001;
      4'd1 : sseg_temp = 7'b1001111;
      4'd2 : sseg_temp = 7'b0010010;
      4'd3 : sseg_temp = 7'b0000110;
      4'd4 : sseg_temp = 7'b1001100;
      4'd5 : sseg_temp = 7'b0100100;
      4'd6 : sseg_temp = 7'b0100000;
      4'd7 : sseg_temp = 7'b0001111;
      4'd8 : sseg_temp = 7'b0000000;
      4'd9 : sseg_temp = 7'b0000100;
      default : sseg_temp = 7'b1111110;
     endcase
    end
    assign cathode = {sseg_temp,1'b1};
endmodule


//debounce.v
`timescale 1ns / 1ps
//////////////////////////////////////////////////////////////////////////////////
// Company:
// Engineer:
//
// Create Date: 04.10.2017 16:46:57
// Design Name:
// Module Name: debounce
// Project Name:
// Target Devices:
// Tool Versions:
// Description:
//
// Dependencies:
//
// Revision:
// Revision 0.01 - File Created
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// Additional Comments:
//
//////////////////////////////////////////////////////////////////////////////////


module debounce(
    input clk_in,
    input clr_in,
    output clr_out
    );
    reg D1,D2,D3;
    always@(posedge clk_in)
    begin
    D1 <= clr_in;
    D2 <= D1;
    D3 <= D2;
    end
    assign clr_out = D1 && D2 && D3;
endmodule

//clk_pulse.v
`timescale 1ns / 1ps
//////////////////////////////////////////////////////////////////////////////////
// Company:
// Engineer:
//
// Create Date: 25.10.2017 21:11:14
// Design Name:
// Module Name: clk_pulse
// Project Name:
// Target Devices:
// Tool Versions:
// Description:
//
// Dependencies:
//
// Revision:
// Revision 0.01 - File Created
// Additional Comments:
//
//////////////////////////////////////////////////////////////////////////////////

module clk_pulse(
```

```
input wire inp,
input wire cclk,
input wire clr,
output wire outp);
reg delay1;
reg delay2;
reg delay3;
always@(posedge cclk or posedge clr)
begin
if(clr == 1)
begin
delay1 <= 1'b0;
delay2 <= 1'b0;
delay3 <= 1'b0;
end
else
begin
delay1 <= inp;
delay2 <= delay1;
delay3 <= delay2;
end
end
assign outp = delay1 & delay2 & delay3;
endmodule

//gcd.v
`timescale 1ns / 1ps
module gcd (
input Clock,
input Reset,
input go,
input [5:0] A,
input [5:0] B,
output Done,
output [5:0] Y);
reg A_lt_B, Done;
reg [5:0] A_New, A_cur, B_cur, Y;

always @(posedge Clock)
   begin
      if (Reset) begin
         A_cur = 0;
         B_cur = 0;
```

```
      end
      else if (go) begin
         A_cur = A;
         B_cur = B;
      end
      else if (A_lt_B) begin
         A_cur = B_cur;
         B_cur = A_New;
      end
      else
         A_cur = A_New;
   end
always @(A_cur or B_cur)
  begin
    if (A_cur >= B_cur) begin
      A_lt_B = 0;
      A_New = A_cur - B_cur;
    end
    else begin
      A_lt_B = 1;
      A_New = A_cur;
    end
    if (B_cur == 0) begin
      Done = 1;
      Y = A_cur;
    end
    else begin
      Done = 0;
      Y = 0;
    end
end
endmodule

//binary2bcd.v
`timescale 1ns / 1ps
//////////////////////////////////////////////////////////////////////////////////
// Company:
// Engineer:
//
// Create Date: 26.09.2017 17:01:34
// Design Name:
// Module Name: bcd_adder
// Project Name:
```

```
// Target Devices:
// Tool Versions:
// Description:
//
// Dependencies:
//
// Revision:
// Revision 0.01 - File Created
// Additional Comments:
//
//////////////////////////////////////////////////////////////////////////////////


module binary2bcd(
    number,hundreds,tens,ones
    );
    input[7:0] number;
    output reg [3:0]hundreds;
    output reg [3:0]tens;
    output reg [3:0]ones;
    // double dabble algorithm
    reg[19:0] shift;
    integer  i;
    always @(number)
    begin
        shift[19:8] =0;
        shift[7:0] = number;
        for (i=0;i<8;i=i+1)
        begin
            if(shift[11:8] >= 5)
                shift[11:8] = shift[11:8] + 3;
            if(shift[15:12] >= 5)
                shift[15:12] = shift[15:12] + 3;
            if(shift[19:16] >= 5)
                shift[19:16] = shift[19:16] + 3;
            shift = shift <<1;
         end

         hundreds = shift[19:16];
         tens     = shift[15:12];
         ones     = shift[11:8];
    end
```

```
endmodule

//pmodco.v
`timescale 1ns / 1ps
//////////////////////////////////////////////////////////////////////////////////
// Company:
// Engineer:
//
// Create Date: 26.10.2017 01:05:57
// Design Name:
// Module Name: pmodco
// Project Name:
// Target Devices:
// Tool Versions:
// Description:
//
// Dependencies:
//
// Revision:
// Revision 0.01 - File Created
// Additional Comments:
//
//////////////////////////////////////////////////////////////////////////////////


module pmodco(
    input clock_in,
    input [3:0] ones,
    input [3:0] tens,
    output [6:0] cathode,
    output anode
    );
    reg [6:0] sseg_temp;
    reg [6:0]sseg;
    reg an_temp=1'b0;
    reg [17:0] count;
        always@(posedge clock_in)
        begin
        count <= count+1;
        end
        always @ (*)
```

```
            begin
             case(count[17])
              1'b0 :
               begin
                sseg = ones;
                an_temp = 1'b1;
               end
              1'b1:
               begin
                sseg = tens;
                an_temp = 1'b0;
               end
             endcase
            end
    assign anode=an_temp;
    always @ (*)
        begin
         case(sseg)
          4'd0 : sseg_temp = 7'b0000001;
          4'd1 : sseg_temp = 7'b1001111;
          4'd2 : sseg_temp = 7'b0010010;
          4'd3 : sseg_temp = 7'b0000110;
          4'd4 : sseg_temp = 7'b1001100;
          4'd5 : sseg_temp = 7'b0100100;
          4'd6 : sseg_temp = 7'b0100000;
          4'd7 : sseg_temp = 7'b0001111;
          4'd8 : sseg_temp = 7'b0000000;
          4'd9 : sseg_temp = 7'b0000100;
           default : sseg_temp = 7'b1111110;
         endcase
        end
        assign cathode = ~sseg_temp;
endmodule

//const.xdc
set_property PACKAGE_PIN W5 [get_ports {Clock}]
set_property IOSTANDARD LVCMOS33 [get_ports {Clock}]
set_property PACKAGE_PIN T18 [get_ports {Reset}]
set_property IOSTANDARD LVCMOS33 [get_ports {Reset}]
set_property PACKAGE_PIN T17 [get_ports {go}]
set_property IOSTANDARD LVCMOS33 [get_ports {go}]
set_property PACKAGE_PIN V17 [get_ports {A[0]}]
set_property IOSTANDARD LVCMOS33 [get_ports {A[0]}]
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```
set_property PACKAGE_PIN V16 [get_ports {A[1]}]
set_property IOSTANDARD LVCMOS33 [get_ports {A[1]}]
set_property PACKAGE_PIN W16 [get_ports {A[2]}]
set_property IOSTANDARD LVCMOS33 [get_ports {A[2]}]
set_property PACKAGE_PIN W17 [get_ports {A[3]}]
set_property IOSTANDARD LVCMOS33 [get_ports {A[3]}]
set_property PACKAGE_PIN W15 [get_ports {A[4]}]
set_property IOSTANDARD LVCMOS33 [get_ports {A[4]}]
set_property PACKAGE_PIN V15 [get_ports {A[5]}]
set_property IOSTANDARD LVCMOS33 [get_ports {A[5]}]
set_property PACKAGE_PIN W14 [get_ports {B[0]}]
set_property IOSTANDARD LVCMOS33 [get_ports {B[0]}]
set_property PACKAGE_PIN W13 [get_ports {B[1]}]
set_property IOSTANDARD LVCMOS33 [get_ports {B[1]}]
set_property PACKAGE_PIN V2 [get_ports {B[2]}]
set_property IOSTANDARD LVCMOS33 [get_ports {B[2]}]
set_property PACKAGE_PIN T3 [get_ports {B[3]}]
set_property IOSTANDARD LVCMOS33 [get_ports {B[3]}]
set_property PACKAGE_PIN T2 [get_ports {B[4]}]
set_property IOSTANDARD LVCMOS33 [get_ports {B[4]}]
set_property PACKAGE_PIN R3 [get_ports {B[5]}]
set_property IOSTANDARD LVCMOS33 [get_ports {B[5]}]

set_property PACKAGE_PIN A14 [get_ports {cathode[3]}]
set_property IOSTANDARD LVCMOS33 [get_ports {cathode[3]}]
set_property PACKAGE_PIN A16 [get_ports {cathode[2]}]
set_property IOSTANDARD LVCMOS33 [get_ports {cathode[2]}]
set_property PACKAGE_PIN B15 [get_ports {cathode[1]}]
set_property IOSTANDARD LVCMOS33 [get_ports {cathode[1]}]
set_property PACKAGE_PIN B16 [get_ports {cathode[6]}]
set_property IOSTANDARD LVCMOS33 [get_ports {cathode[6]}]
set_property PACKAGE_PIN K17 [get_ports {cathode[5]}]
set_property IOSTANDARD LVCMOS33 [get_ports {cathode[5]}]
set_property PACKAGE_PIN M18 [get_ports {cathode[4]}]
set_property IOSTANDARD LVCMOS33 [get_ports {cathode[4]}]
set_property PACKAGE_PIN N17 [get_ports {cathode[0]}]
set_property IOSTANDARD LVCMOS33 [get_ports {cathode[0]}]
set_property PACKAGE_PIN P18 [get_ports {anode}]
set_property IOSTANDARD LVCMOS33 [get_ports {anode}]
set_property PACKAGE_PIN U16 [get_ports {Done}]
set_property IOSTANDARD LVCMOS33 [get_ports {Done}]
set_property PACKAGE_PIN U2 [get_ports anode1[0]]
set_property IOSTANDARD LVCMOS33 [get_ports anode1[0]]
```

```
set_property PACKAGE_PIN U4 [get_ports anode1[1]]
set_property IOSTANDARD LVCMOS33 [get_ports anode1[1]]
set_property PACKAGE_PIN V4 [get_ports anode1[2]]
set_property IOSTANDARD LVCMOS33 [get_ports anode1[2]]
set_property PACKAGE_PIN W4 [get_ports anode1[3]]
set_property IOSTANDARD LVCMOS33 [get_ports anode1[3]]

set_property PACKAGE_PIN V7 [get_ports cathode1[0]]
set_property IOSTANDARD LVCMOS33 [get_ports cathode1[0]]
set_property PACKAGE_PIN U7 [get_ports cathode1[1]]
set_property IOSTANDARD LVCMOS33 [get_ports cathode1[1]]
set_property PACKAGE_PIN V5 [get_ports cathode1[2]]
set_property IOSTANDARD LVCMOS33 [get_ports cathode1[2]]
set_property PACKAGE_PIN U5 [get_ports cathode1[3]]
set_property IOSTANDARD LVCMOS33 [get_ports cathode1[3]]
set_property PACKAGE_PIN V8 [get_ports cathode1[4]]
set_property IOSTANDARD LVCMOS33 [get_ports cathode1[4]]
set_property PACKAGE_PIN U8 [get_ports cathode1[5]]
set_property IOSTANDARD LVCMOS33 [get_ports cathode1[5]]
set_property PACKAGE_PIN W6 [get_ports cathode1[6]]
set_property IOSTANDARD LVCMOS33 [get_ports cathode1[6]]
set_property PACKAGE_PIN W7 [get_ports cathode1[7]]
set_property IOSTANDARD LVCMOS33 [get_ports cathode1[7]]
```