Lab3

Submitted By:
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2016201

//top.v

```
`timescale 1ns / 1ps
//////////////////////////////////////////////////////////////////////////////////
// Company:
// Engineer:
//
// Create Date: 28.08.2017 15:06:23
// Design Name:
// Module Name: top1
// Project Name:
// Target Devices:
// Tool Versions:
// Description:
//
// Dependencies:
//
// Revision:
// Revision 0.01 - File Created
// Additional Comments:
//
//////////////////////////////////////////////////////////////////////////////////


module top1(
    input clk,
    input clr,
    input sel1,
    input sel2,
    output reg[4:0] count1
    );
wire f1,f2,f4,f8,ind,clk_deb;
wire [4:0] ans1,ans2,ans4,ans8;
divideby10 zx(.clkin(clk),.clkout(f1));
divideby2 zc(.clk(f1),.out_clk(f2));
divideby2 zv(.clk(f2),.out_clk(f4));
divideby2 zb(.clk(f4),.out_clk(f8));
```

```
q2 zn(.inc(clk),.outp(ind));
debounce zm(.clock_in(ind),.clr_in(clr),.clr_out(clk_deb));
decounter al(.clock_in(f1),.clr_debounced(clk_deb),.count(ans1));
decounter am(.clock_in(f2),.clr_debounced(clk_deb),.count(ans2));
decounter aw(.clock_in(f4),.clr_debounced(clk_deb),.count(ans4));
decounter ar(.clock_in(f8),.clr_debounced(clk_deb),.count(ans8));
always@(*)
begin
if (sel1 == 0 & sel2 == 0)
count1=ans1;
else if (sel1 == 0 & sel2 == 1)
count1=ans2;
else if(sel1 == 1 & sel2 == 0)
count1=ans4;
else
count1=ans8;
end
endmodule
```

//divideby10.v

```
`timescale 1ns / 1ps
//////////////////////////////////////////////////////////////////////////////////
// Company:
// Engineer:
//
// Create Date: 05.09.2017 14:32:31
// Design Name:
// Module Name: divideby10
// Project Name:
// Target Devices:
// Tool Versions:
// Description:
//
// Dependencies:
//
// Revision:
// Revision 0.01 - File Created
// Additional Comments:
//
//////////////////////////////////////////////////////////////////////////////////
```

```
module divideby10(
    input clkin,
    output reg clkout
    );
reg [26:0] counter;
    initial begin
        counter = 0;
        clkout = 0;
    end
    always @(posedge clkin) begin
        if (counter == 50000000) begin
            counter <= 0;
            clkout <= ~clkout;
        end else begin
            counter <= counter +1;
        end
    end
endmodule
```

//divideby2.v

```
`timescale 1ns / 1ps
//////////////////////////////////////////////////////////////////////////////////
// Company:
// Engineer:
//
// Create Date: 05.09.2017 16:35:19
// Design Name:
// Module Name: divideby2
// Project Name:
// Target Devices:
// Tool Versions:
// Description:
//
// Dependencies:
//
// Revision:
// Revision 0.01 - File Created
// Additional Comments:
//
//////////////////////////////////////////////////////////////////////////////////
```

```
module divideby2(
    input clk,
    output out_clk
    );
reg m;
initial m=0;
always@(posedge clk)
begin
m <= ~m;
end
assign out_clk=m;
endmodule
```

//q2.v

```
`timescale 1ns / 1ps
//////////////////////////////////////////////////////////////////////////////////
// Company:
// Engineer:
//
// Create Date: 28.08.2017 14:59:33
// Design Name:
// Module Name: q2
// Project Name:
// Target Devices:
// Tool Versions:
// Description:
//
// Dependencies:
//
// Revision:
// Revision 0.01 - File Created
// Additional Comments:
//
//////////////////////////////////////////////////////////////////////////////////


module q2(
    input inc,
    output outp
    );
    reg [24:0] count;
```

```
    always@(posedge inc)
    begin
    if ( count == 33554431)
    count=0;
    else
    count=count+1;
    end
    assign outp=count[18];
endmodule
```

//debounce.v

```
`timescale 1ns / 1ps
//////////////////////////////////////////////////////////////////////////////////
// Company:
// Engineer:
//
// Create Date: 29.08.2017 14:36:39
// Design Name:
// Module Name: debounce
// Project Name:
// Target Devices:
// Tool Versions:
// Description:
//
// Dependencies:
//
// Revision:
// Revision 0.01 - File Created
// Additional Comments:
//
//////////////////////////////////////////////////////////////////////////////////


module debounce(
    input clock_in,
    input clr_in,
    output clr_out
    );
    reg D1,D2,D3;
    always@(posedge clock_in)
    begin
    D1 <= clr_in;
```

```
    D2 <= D1;
    D3 <= D2;
    end
    assign clr_out = D1 && D2 && D3;
endmodule
```

//decounter.v

```
`timescale 1ns / 1ps
//////////////////////////////////////////////////////////////////////////////////
// Company:
// Engineer:
//
// Create Date: 05.09.2017 16:01:57
// Design Name:
// Module Name: decounter
// Project Name:
// Target Devices:
// Tool Versions:
// Description:
//
// Dependencies:
//
// Revision:
// Revision 0.01 - File Created
// Additional Comments:
//
//////////////////////////////////////////////////////////////////////////////////


module decounter(
    input clock_in,
    input clr_debounced,
    output reg [4:0]count
    );
//parameter width=5;
//reg[width-1:0] count;
always@(posedge clock_in)
begin
if(clr_debounced == 1)
count=0;
else
count=count+1;
```

```
end
endmodule
```

//const.xdc

```
set_property PACKAGE_PIN Y9 [get_ports {clk}]
set_property IOSTANDARD LVCMOS33 [get_ports {clk}]
set_property PACKAGE_PIN T18 [get_ports {clr}]
set_property IOSTANDARD LVCMOS33 [get_ports {clr}]
set_property PACKAGE_PIN G22 [get_ports {sel1}]
set_property IOSTANDARD LVCMOS33 [get_ports {sel1}]
set_property PACKAGE_PIN H22 [get_ports {sel2}]
set_property IOSTANDARD LVCMOS33 [get_ports {sel2}]
set_property PACKAGE_PIN T22 [get_ports {count1[0]}]
set_property IOSTANDARD LVCMOS33 [get_ports {count1[0]}]
set_property PACKAGE_PIN T21 [get_ports {count1[1]}]
set_property IOSTANDARD LVCMOS33 [get_ports {count1[1]}]
set_property PACKAGE_PIN U22 [get_ports {count1[2]}]
set_property IOSTANDARD LVCMOS33 [get_ports {count1[2]}]
set_property PACKAGE_PIN U21 [get_ports {count1[3]}]
set_property IOSTANDARD LVCMOS33 [get_ports {count1[3]}]
set_property PACKAGE_PIN V22 [get_ports {count1[4]}]
set_property IOSTANDARD LVCMOS33 [get_ports {count1[4]}]
```