Lab Homework – (2nd Oct. & 4th Oct.)

ECE270 - Embedded Logic Design

Board: Basys 3 Board, Xilinx Artix – 7 FPGA (XC7A35T-1CPG236C)

Submission Guidelines: Submit the entire Verilog code with the detailed explanation of your state diagram in the readable format.

Question:

Design and Implement a door lock which uses three push buttons to enter a 4-digit code. You can use btn[2:0] on the FPGA board for the door lock buttons. For example, you might press buttons 2-0-1-2 to open the door. Write a Verilog code which uses switches as follows:

- The first correct button selected from btn[2:0] will be the switch setting sw[7:6] where valid setting are “00”, “01”, “10” corresponding to btn[0], btn[1] and btn[2] respectively.
- The second correct button selected from btn[2:0] will be the switch setting sw[5:4].
- The third correct button selected from btn[2:0] will be the switch setting sw[3:2].
- The fourth correct button selected from btn[2:0] will be the switch setting sw[1:0].

You must make four button pressings before you know if you were successful. If you enter the correct code the LED_CORRECT will light up. If you enter an incorrect code then LED_WRONG will light up.