ECE270: ELD

Assignment 2

Due Date: Oct. 18, 2017

Submission Guidelines:

1) On backpack, submit single pdf file with readable text format.
2) Include all Verilog codes except automated codes of IP.
3) Answers without in-depth explanation will not be evaluated.

1. Explain in detail the architecture of phase locked look (PLL) in 7-series FPGA. Explain how VCO output frequency affects the power consumption of FPGA.

2. Explain in detail “Clock Monitor” functionality of CMT of 7-series FPGA in detail.

3. Design BUF4MUX which allows glitch less switching between 2 clocks of distinct frequency/phase via 1-bit control signal. Show the behavioral simulation results with detailed explanation of various transition scenarios. Mention all the assumptions explicitly.

4. Using CORDIC IP of Vivado, design circuit which outputs the square root of any input integer number between 0-256. Explain the results using behavioral simulation waveforms or on-board display.