ECE270: ELD

Assignment 3

Due Date: Nov. 10, 2017

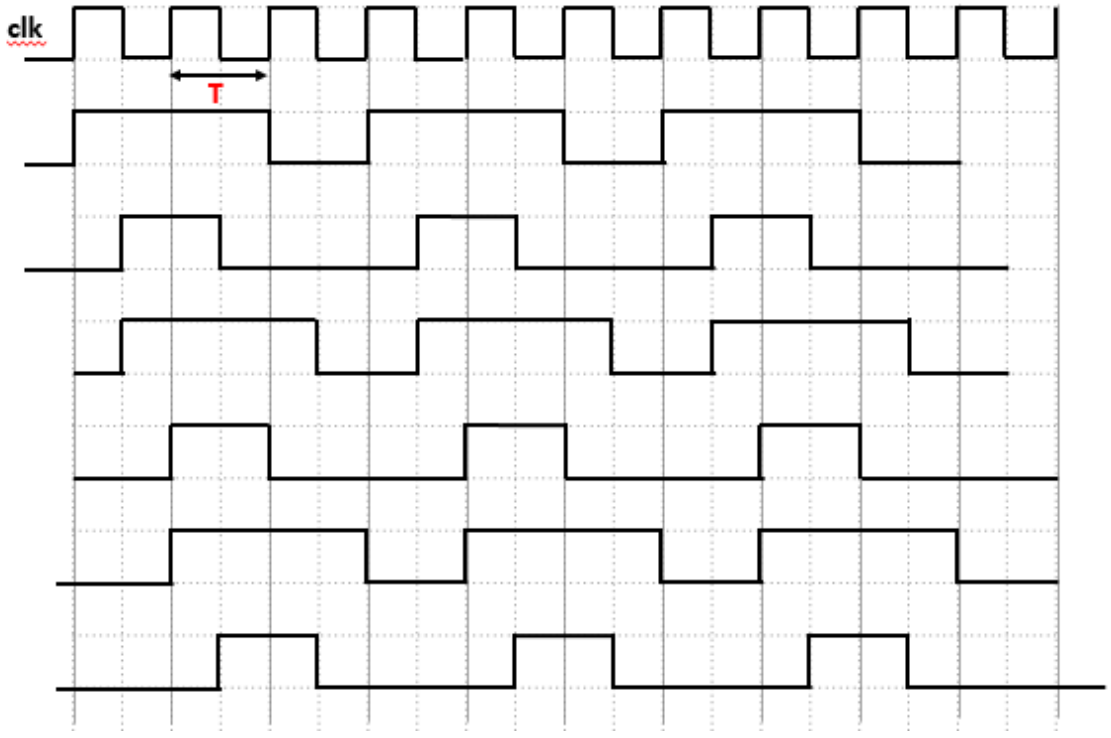
Submission Guidelines:

1) On backpack, submit single pdf file with readable text format.
2) Include all Verilog codes except automated codes of IP.
3) Answers without in-depth explanation will not be evaluated.

1. Design the clock divider circuit which has input clock, clk, and it produces the six output clocks shown below. Explain the answers in details with Verilog codes, testbench and simulation waveforms.

   (10 Marks)

   (Hint: Refer to DC lecture notes for frequency divider by odd number or pattern generation using FSM).



2. In AXI memory mapped interface, how the number of transactions and size of each transactions in a burst are determined?

   (2.5 Marks)

   Who determines it: Master or Slave?

   (0.5 Marks)

3. The timing diagram shown below indicate the Burst write operation in AXI memory mapped protocol. Modify this timing diagram to illustrate write operations in AXI Lite protocol.

(3.5 Marks)

Also, draw the timing diagram for read burst transaction in AXI memory mapped protocol with burst size of 2.

(3.5 Marks)