ECE270: ELD

Assignment 1

Due Date: Sept. 11, 2017

Submission Guidelines:

1) On backpack, submit single pdf file with readable text format.
2) For 2nd and 3rd answer, share the google drive link where the corresponding project folder (containing complete Vivado project) is located.
3) The link should be mentioned explicitly in the pdf file (one link for each answer). Otherwise, solution will not be evaluated.
4) Shared folder should be accessible to anyone with the link.
5) Don't modify the contents of the folder after submission deadline.

1. Explain in detail the HDL coding guidelines for making efficient use of: 1) CLB flip flops and 2) Shift register logic (SRL) using LUTs.

2. The pipelining approach involves use of flip-flops to improve the clock frequency at which the circuit can be clocked. For more details, refer to Lecture on August 31 and lab handout in week starting on Sept. 4.

   You need to design 3-bit multiplier circuit (for unsigned numbers) using full adder (and half adder, if needed). You can use only gate level modeling for full adder and half adder implementation. No such modeling restriction apply for multiplier circuit.

   Explain how the pipelining approach can be used to improve the clock frequency of multiplier circuit. Support your claims using data shown in Vivado reports.

3. Design 16:1 multiplexer with 2-bit inputs using gate level modeling, behavioral modeling and data flow level modeling. Compare and explain the FPGA resource utilization in each of them.

4. Design the following circuit using Verilog and verify it using testbench. Explain the circuit behavior as well as simulation results.