Lab 2

Submitted By :
Snehal Gupta
2016201

// Problem A
// Data flow

// problem_a.v

```
`timescale 1ns / 1ps
//////////////////////////////////////////////////////////////////////////////////
// Company:
// Engineer:
//
// Create Date: 14.08.2017 14:38:28
// Design Name:
// Module Name: problem_a
// Project Name:
// Target Devices:
// Tool Versions:
// Description:
//
// Dependencies:
//
// Revision:
// Revision 0.01 - File Created
// Additional Comments:
//
//////////////////////////////////////////////////////////////////////////////////


module problem_a(
    input T,
    input A1,
    input P,
    input A2,
    output H,
    output V,
    output A
    );
```

```
    assign H=( T & ~A1 & ~P)|(T & ~A1 & ~A2);
    assign V=( P & ~A2 & ~T)|(P & ~A2 & A1);
    assign A=( T & A1 & P & A2)|(T & ~A1 & P & ~A2);
endmodule
```

//const.xdc

```
set_property PACKAGE_PIN F22 [get_ports {A2}]
set_property IOSTANDARD LVCMOS33 [get_ports {A2}]

set_property PACKAGE_PIN G22 [get_ports {P}]
set_property IOSTANDARD LVCMOS33 [get_ports {P}]

set_property PACKAGE_PIN H22 [get_ports {A1}]
set_property IOSTANDARD LVCMOS33 [get_ports {A1}]

set_property PACKAGE_PIN F21 [get_ports {T}]
set_property IOSTANDARD LVCMOS33 [get_ports {T}]

set_property PACKAGE_PIN T22 [get_ports {H}]
set_property IOSTANDARD LVCMOS33 [get_ports {H}]

set_property PACKAGE_PIN T21 [get_ports {V}]
set_property IOSTANDARD LVCMOS33 [get_ports {V}]

set_property PACKAGE_PIN U22 [get_ports {A}]
set_property IOSTANDARD LVCMOS33 [get_ports {A}]
```

//Behavioral modelling

//behav_a.v

```
`timescale 1ns / 1ps
//////////////////////////////////////////////////////////////////////////////////
// Company:
// Engineer:
//
// Create Date: 22.08.2017 19:35:52
// Design Name:
// Module Name: behav_a
// Project Name:
// Target Devices:
// Tool Versions:
// Description:
```

```
//
// Dependencies:
//
// Revision:
// Revision 0.01 - File Created
// Additional Comments:
//
//////////////////////////////////////////////////////////////////////////////////


module behav_a(
    input T,
    input A1,
    input P,
    input A2,
    output reg H,
    output reg V,
    output reg A
    );
always@(*)
begin
if( (T == 1 & A1 == 0 && P == 0 )| (T == 1 & A1 == 0 & A2 == 0))
H=1;
else
H=0;
end

always@(*)
begin
if( ( P == 1 & A2 == 0 & T == 0) | ( P == 1 & A2 == 0 & A1 == 1))
V=1;
else
V=0;
end

always@(*)
begin
if((T == 1 & A1 == 1 & P == 1 & A2 == 1) | ( T == 1 & A1 == 0 & P == 1 & A2 == 0))
A=1;
else
A=0;
end
```

endmodule

//cons.xdc
set_property PACKAGE_PIN F22 [get_ports {A2}]
set_property IOSTANDARD LVCMOS33 [get_ports {A2}]

set_property PACKAGE_PIN G22 [get_ports {P}]
set_property IOSTANDARD LVCMOS33 [get_ports {P}]

set_property PACKAGE_PIN H22 [get_ports {A1}]
set_property IOSTANDARD LVCMOS33 [get_ports {A1}]

set_property PACKAGE_PIN F21 [get_ports {T}]
set_property IOSTANDARD LVCMOS33 [get_ports {T}]

set_property PACKAGE_PIN T22 [get_ports {H}]
set_property IOSTANDARD LVCMOS33 [get_ports {H}]

set_property PACKAGE_PIN T21 [get_ports {V}]
set_property IOSTANDARD LVCMOS33 [get_ports {V}]

set_property PACKAGE_PIN U22 [get_ports {A}]
set_property IOSTANDARD LVCMOS33 [get_ports {A}]

//Problem B
// Data flow

//problem_b.v
`timescale 1ns / 1ps
//
// Company:
// Engineer:
//
// Create Date: 22.08.2017 20:13:32
// Design Name:
// Module Name: problem_b
// Project Name:
// Target Devices:
// Tool Versions:
// Description:
//

```
// Dependencies:
//
// Revision:
// Revision 0.01 - File Created
// Additional Comments:
//
//////////////////////////////////////////////////////////////////////////////////


module problem_b(
    input C,
    input A1,
    input Q,
    input A2,
    input L,
    input B,
    output Z,
    output Y
    );
assign Z= (~Q & B) | (B & ~A1) | (B & ~C);
assign Y= (C & ~A1 & ~Q & ~B) | (Q & ~L & C & A1);
endmodule
```

//cons.xdc

```
set_property PACKAGE_PIN F22 [get_ports {C}]
set_property IOSTANDARD LVCMOS33 [get_ports {C}]

set_property PACKAGE_PIN G22 [get_ports {A1}]
set_property IOSTANDARD LVCMOS33 [get_ports {A1}]

set_property PACKAGE_PIN H22 [get_ports {Q}]
set_property IOSTANDARD LVCMOS33 [get_ports {Q}]

set_property PACKAGE_PIN F21 [get_ports {A2}]
set_property IOSTANDARD LVCMOS33 [get_ports {A2}]

set_property PACKAGE_PIN H19 [get_ports {L}]
set_property IOSTANDARD LVCMOS33 [get_ports {L}]

set_property PACKAGE_PIN H18 [get_ports {B}]
set_property IOSTANDARD LVCMOS33 [get_ports {B}]

set_property PACKAGE_PIN T22 [get_ports {Z}]
```

```
set_property IOSTANDARD LVCMOS33 [get_ports {Z}]

set_property PACKAGE_PIN T21 [get_ports {Y}]
set_property IOSTANDARD LVCMOS33 [get_ports {Y}]
```

// Behavioral modelling

// behav.v

```
`timescale 1ns / 1ps
//////////////////////////////////////////////////////////////////////////////////
// Company:
// Engineer:
//
// Create Date: 22.08.2017 21:14:14
// Design Name:
// Module Name: behav
// Project Name:
// Target Devices:
// Tool Versions:
// Description:
//
// Dependencies:
//
// Revision:
// Revision 0.01 - File Created
// Additional Comments:
//
//////////////////////////////////////////////////////////////////////////////////


module behav(
    input C,
    input A1,
    input Q,
    input A2,
    input L,
    input B,
    output reg Z,
    output reg Y
    );
always@(*)
begin
```

```
if ( (Q == 0 & B == 1) | (B == 1 & A1 == 0) | (B==1 & C==0))
Z=1;
else
Z=0;
end

always@(*)
begin
if( (C == 1 & A1 == 0 & Q == 0 & B == 0) | (Q == 1 & L == 0 & C == 1 & A1 == 1))
Y=1;
else
Y=0;
end

endmodule
```

//cons.xdc

```
set_property PACKAGE_PIN F22 [get_ports {C}]
set_property IOSTANDARD LVCMOS33 [get_ports {C}]

set_property PACKAGE_PIN G22 [get_ports {A1}]
set_property IOSTANDARD LVCMOS33 [get_ports {A1}]

set_property PACKAGE_PIN H22 [get_ports {Q}]
set_property IOSTANDARD LVCMOS33 [get_ports {Q}]

set_property PACKAGE_PIN F21 [get_ports {A2}]
set_property IOSTANDARD LVCMOS33 [get_ports {A2}]

set_property PACKAGE_PIN H19 [get_ports {L}]
set_property IOSTANDARD LVCMOS33 [get_ports {L}]

set_property PACKAGE_PIN H18 [get_ports {B}]
set_property IOSTANDARD LVCMOS33 [get_ports {B}]

set_property PACKAGE_PIN T22 [get_ports {Z}]
set_property IOSTANDARD LVCMOS33 [get_ports {Z}]

set_property PACKAGE_PIN T21 [get_ports {Y}]
set_property IOSTANDARD LVCMOS33 [get_ports {Y}]
```