Lab1

Submitted By :

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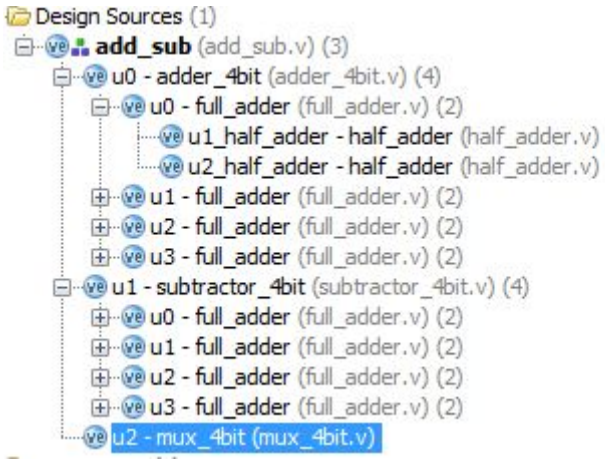
Hierarchy of my project :



// add_sub.v

```
`timescale 1ns / 1ps
//////////////////////////////////////////////////////////////////////////////////
// Company:
// Engineer:
//
// Create Date: 15.08.2017 13:47:52
// Design Name:
// Module Name: add_sub
// Project Name:
// Target Devices:
// Tool Versions:
```

```
// Description:
//
// Dependencies:
//
// Revision:
// Revision 0.01 - File Created
// Additional Comments:
//
//////////////////////////////////////////////////////////////////////////////////



module add_sub(
   input [3:0] a,
   input [3:0] b,
   input sel,
   output [3:0] dout,
   output ca
   );
   wire [3:0]m;
   wire [3:0]n;
   wire c;
   wire d;
   adder_4bit u0  (.a (a),.b (b),.sum (m),.carry(c));
   subtractor_4bit u1 (.a(a), .b(b),.diff (n),.borrow(d));
   mux_4bit u2 (.a(m),.b(n),.c(c),.d(d),.sel(sel),.dout(dout),.cd(ca));
endmodule
```

//adder_4bit.v

```
`timescale 1ns / 1ps
//////////////////////////////////////////////////////////////////////////////////
// Company:
```

```
// Engineer:
//
// Create Date: 14.08.2017 17:57:38
// Design Name:
// Module Name: adder_4bit
// Project Name:
// Target Devices:
// Tool Versions:
// Description:
//
// Dependencies:
//
// Revision:
// Revision 0.01 - File Created
// Additional Comments:
//
//////////////////////////////////////////////////////////////////////////////////


module adder_4bit(
   input[3:0] a,
   input[3:0] b,
   output[3:0] sum,
   output carry
   );


   wire [2:0]s;

   full_adder u0 (a[0],b[0],1'b0,sum[0],s[0]);
   full_adder u1 (a[1],b[1],s[0],sum[1],s[1]);
```

```
   full_adder u2 (a[2],b[2],s[1],sum[2],s[2]);
   full_adder u3 (a[3],b[3],s[2],sum[3],carry);
endmodule
```

//subtractor_4bit.v

```
`timescale 1ns / 1ps
//////////////////////////////////////////////////////////////////////////////////
// Company:
// Engineer:
//
// Create Date: 14.08.2017 18:25:19
// Design Name:
// Module Name: subtractor_4bit
// Project Name:
// Target Devices:
// Tool Versions:
// Description:
//
// Dependencies:
//
// Revision:
// Revision 0.01 - File Created
// Additional Comments:
//
//////////////////////////////////////////////////////////////////////////////////


module subtractor_4bit(
   input[3:0] a,
   input[3:0] b,
```

```
    output[3:0] diff,
    output borrow
    );



    wire [2:0]s;
    wire [3:0]l;

    xor(l[0],b[0],1'b1);
    xor(l[1],b[1],1'b1);
    xor(l[2],b[2],1'b1);
    xor(l[3],b[3],1'b1);

    full_adder u0 (a[0],l[0],1'b1,diff[0],s[0]);
    full_adder u1 (a[1],l[1],s[0],diff[1],s[1]);
    full_adder u2 (a[2],l[2],s[1],diff[2],s[2]);
    full_adder u3 (a[3],l[3],s[2],diff[3],borrow);
endmodule
```

//mux_4bit.v

```
`timescale 1ns / 1ps
//////////////////////////////////////////////////////////////////////////////////
// Company:
// Engineer:
//
// Create Date: 15.08.2017 13:35:50
// Design Name:
// Module Name: mux_4bit
// Project Name:
// Target Devices:
// Tool Versions:
```

```
// Description:
//
// Dependencies:
//
// Revision:
// Revision 0.01 - File Created
// Additional Comments:
//
//////////////////////////////////////////////////////////////////////////////////


module mux_4bit(
    input [3:0] a,
    input [3:0] b,
    input c,
    input d,
    input sel,
    output [3:0] dout,
    output cd
    );

    assign dout = sel ? b : a;
    assign cd = sel ? d : c;
endmodule
```

//full_adder.v

```
`timescale 1ns / 1ps
//////////////////////////////////////////////////////////////////////////////////
// Company:
// Engineer:
```

```
//
// Create Date: 14.08.2017 16:35:30
// Design Name:
// Module Name: full_adder
// Project Name:
// Target Devices:
// Tool Versions:
// Description:
//
// Dependencies:
//
// Revision:
// Revision 0.01 - File Created
// Additional Comments:
//
//////////////////////////////////////////////////////////////////////////////////


module full_adder(
   input a,
   input b,
   input c,
   output sum,
   output carry
   );
   wire w_sum1;
   wire w_carry1;
   wire w_carry2;
   assign carry = w_carry1 | w_carry2;
   half_adder u1_half_adder(.A(a), .B(b),.Sum(w_sum1),.Carry(w_carry1));
   half_adder u2_half_adder(.A(w_sum1),.B(c),.Sum(sum),.Carry(w_carry2)
```

```
   );
endmodule
```

//half_adder.v

```
`timescale 1ns / 1ps
//////////////////////////////////////////////////////////////////////////////////
// Company:
// Engineer:
//
// Create Date: 14.08.2017 16:14:30
// Design Name:
// Module Name: half_adder
// Project Name:
// Target Devices:
// Tool Versions:
// Description:
//
// Dependencies:
//
// Revision:
// Revision 0.01 - File Created
// Additional Comments:
//
//////////////////////////////////////////////////////////////////////////////////


module half_adder(
   input A,
   input B,
   output Sum,
```

```
    output Carry
    );
    assign Sum = (~A & B)| (~B & A);
    assign Carry = A & B;
endmodule
```

//constr.xdc

```
set_property PACKAGE_PIN F22 [get_ports {a[0]}]
set_property IOSTANDARD LVCMOS33 [get_ports {a[0]}]
set_property PACKAGE_PIN G22 [get_ports {a[1]}]
set_property IOSTANDARD LVCMOS33 [get_ports {a[1]}]
set_property PACKAGE_PIN H22 [get_ports {a[2]}]
set_property IOSTANDARD LVCMOS33 [get_ports {a[2]}]
set_property PACKAGE_PIN F21 [get_ports {a[3]}]
set_property IOSTANDARD LVCMOS33 [get_ports {a[3]}]

set_property PACKAGE_PIN H19 [get_ports {b[0]}]
set_property IOSTANDARD LVCMOS33 [get_ports {b[0]}]
set_property PACKAGE_PIN H18 [get_ports {b[1]}]
set_property IOSTANDARD LVCMOS33 [get_ports {b[1]}]
set_property PACKAGE_PIN H17 [get_ports {b[2]}]
set_property IOSTANDARD LVCMOS33 [get_ports {b[2]}]
set_property PACKAGE_PIN M15 [get_ports {b[3]}]
set_property IOSTANDARD LVCMOS33 [get_ports {b[3]}]

set_property PACKAGE_PIN T18 [get_ports {sel}]
```

```
set_property IOSTANDARD LVCMOS33 [get_ports {sel}]
set_property PACKAGE_PIN T22 [get_ports {dout[0]}]
set_property IOSTANDARD LVCMOS33 [get_ports {dout[0]}]
set_property PACKAGE_PIN T21 [get_ports {dout[1]}]
set_property IOSTANDARD LVCMOS33 [get_ports {dout[1]}]
set_property PACKAGE_PIN U22 [get_ports {dout[2]}]
set_property IOSTANDARD LVCMOS33 [get_ports {dout[2]}]
set_property PACKAGE_PIN U21 [get_ports {dout[3]}]
set_property IOSTANDARD LVCMOS33 [get_ports {dout[3]}]
set_property PACKAGE_PIN U19 [get_ports {ca}]
set_property IOSTANDARD LVCMOS33 [get_ports {ca}]
```