# MODELSIM CODE FOR HALF ADDER

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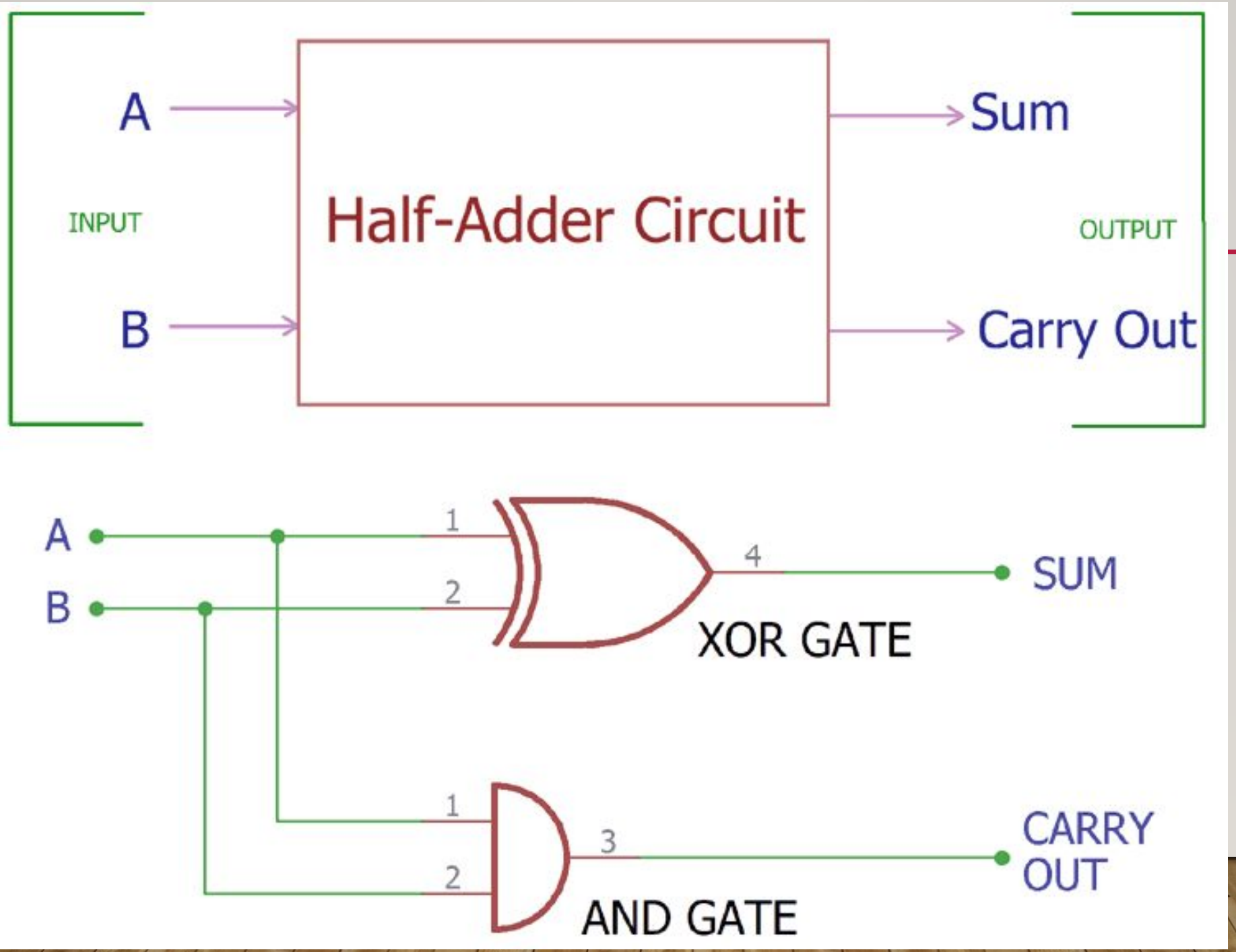
# BLOCK DIAGRAM


A
B
INPUT
Half-Adder Circuit
Sum
Carry Out
OUTPUT
A
B
1
2
4
SUM
XOR GATE
1
2
3
CARRY
OUT
AND GATE

# TRUTH TABLE OF HALF ADDER

| A | B | Sum | Carry Out |
|---|---|---|---|
| 0 | 0 | 0 | 0 |
| 0 | 1 | 1 | 0 |
| 1 | 0 | 1 | 0 |
| 1 | 1 | 1 | 1 |

# CODE FOR HALF ADDER

```
library IEEE;
use IEEE.std_logic_1164.all;
entity half_adder is
port(A,B: in std_logic;
sum,carryout: out std_logic
);
end half_adder;
architecture flow of half_adder is
begin
sum<= A xor B;
carryout<=A and B;
end flow;
```

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