Sukanya Maiti, Roll No.- 59, MCA_1_A, (Set: 04)

Write a VHDL Program for 8 x 1 multiplexer.

=>

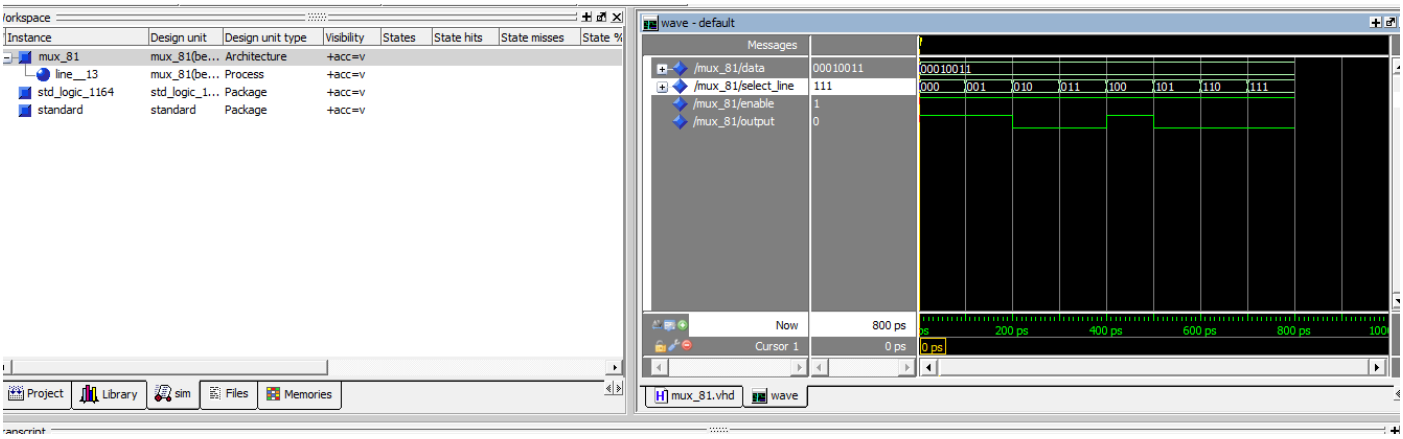
Truth table for 8 x 1 multiplexer: -

S2	S1	S0	Output(Y)
0	0	0	I0
0	0	1	I1
0	1	0	I2
0	1	1	I3
1	0	0	I4
1	0	1	I5
1	1	0	I6
1	1	1	I7

Source code:

```
library IEEE;
use IEEE.std_logic_1164.all;
entity mux_81 is
port(data : in std_logic_vector(7 downto 0); -- 8 data inputs
       select_line : in std_logic_vector(2 downto 0); -- 3 select lines
       enable : in std_logic; -- Enable signal
       output : out std_logic -- Output signal);
end mux_81;
architecture behavioral of mux_81 is
begin
  process(data, select_line, enable)
  begin
    if enable = '1' then
      case select_line is
         when "000" => output <= data(0);
         when "001" => output <= data(1);
         when "010" => output <= data(2);
         when "011" => output <= data(3);
         when "100" => output <= data(4);
         when "101" => output <= data(5);
         when "110" => output <= data(6);
         when "111" => output <= data(7);
         when others => output <= 'X'; -- Undefined behavior for safety
      end case;
    else
      output <= 'X'; -- Output is undefined if enable is not active
  end if;
 end process;
end behavioral;
```

Output: -


Instance
Design unit
Design unit type
Visibility
States
State hits
State misses
mux_81
mux_81(be...
Architecture
+acc=v
line__13
mux_81(be...
Process
+acc=v
std_logic_1164
std_logic_1...
Package
+acc=v
standard
standard
Package
+acc=v
Project
Library
sim
Files
Memories
wave - default
Messages
/mux_81/data
00010011
/mux_81/select_line
111
/mux_81/enable
1
/mux_81/output
0
000
001
010
011
100
101
110
111
Now
800 ps
Cursor 1
0 ps
200 ps
400 ps
600 ps
800 ps
mux_81.vhd
wave