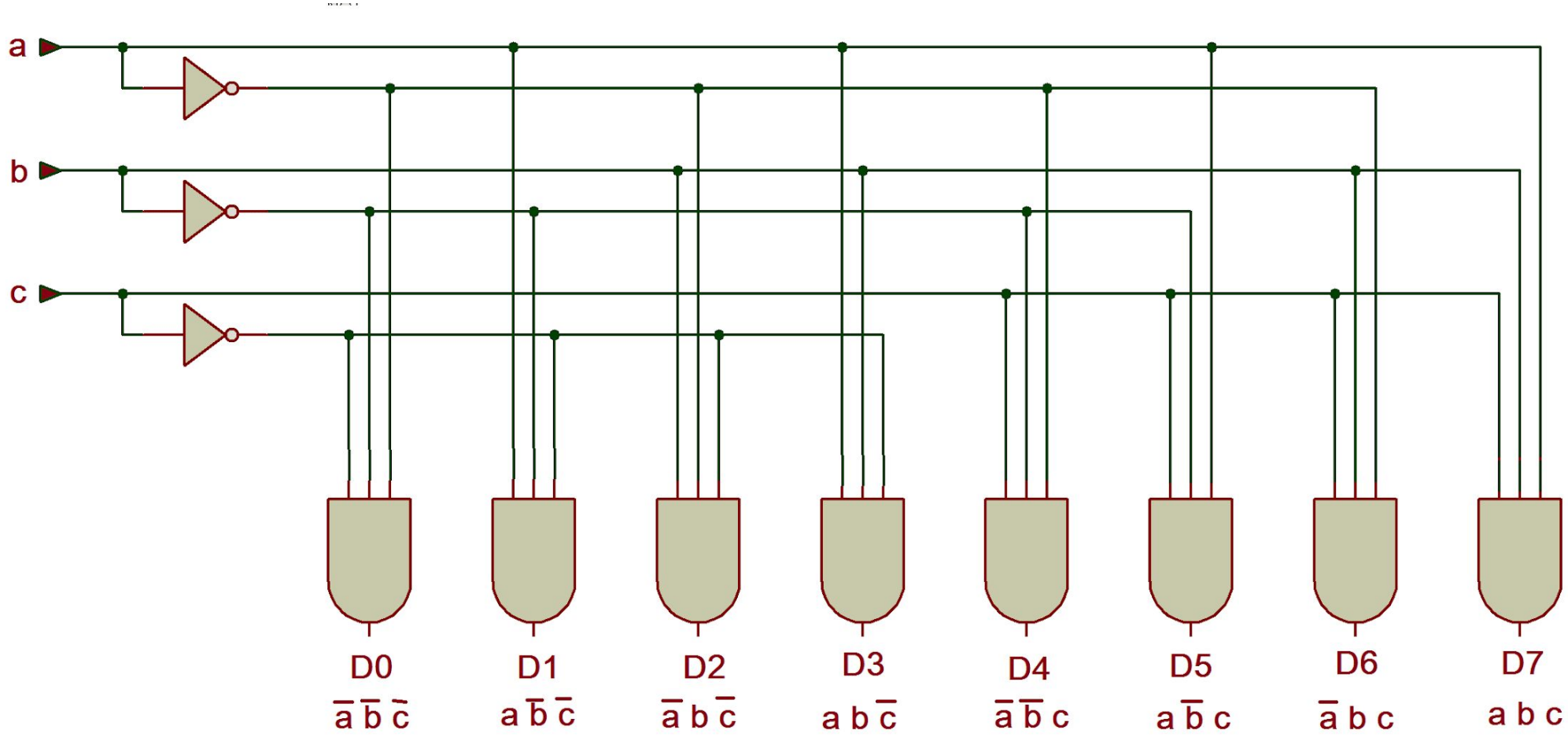
3×8 decoder VHDL Code

c	b	a	D0	D1	D2	D3	D4	D5	D6	D7
0	0	0	1	0	0	0	0	0	0	0
0	0	1	0	1	0	0	0	0	0	0
0	1	0	0	0	1	0	0	0	0	0
0	1	1	0	0	0	1	0	0	0	0
1	0	0	0	0	0	0	1	0	0	0
1	0	1	0	0	0	0	0	1	0	0
1	1	0	0	0	0	0	0	0	1	0
1	1	1	0	0	0	0	0	0	0	1


a
b
c
D0
$\bar{a}\,\bar{b}\,\bar{c}$
D1
$a\,\bar{b}\,\bar{c}$
D2
$\bar{a}\,b\,\bar{c}$
D3
$a\,b\,\bar{c}$
D4
$\bar{a}\,\bar{b}\,c$
D5
$a\,\bar{b}\,c$
D6
$\bar{a}\,b\,c$
D7
$a\,b\,c$

```
library ieee;
use ieee.std_logic_1164.all;
entity decoder_3x8 is
port (a : in std_logic_vector(0 to 2) ;
      d : out std_logic_vector (0 to 7));
end decoder_3x8;
architecture decoder_arch of decoder_3x8 is
 begin
  process (a)
   begin
     case a is
         when "000" => d <= “00000001”;
         when "001" => d <= “00000010”;
         when "010" => d <= “00000100”;
         when "011" => d <= “00001000”;
         when "100" => d <= “00010000”;
         when "101" => d <= “00100000”;
         when "110" => d <= “01000000”;
         when "111" => d <= “10000000”;
         when others => d<= "00000000";
   end case;
  end process;
end decoder_arch;
```