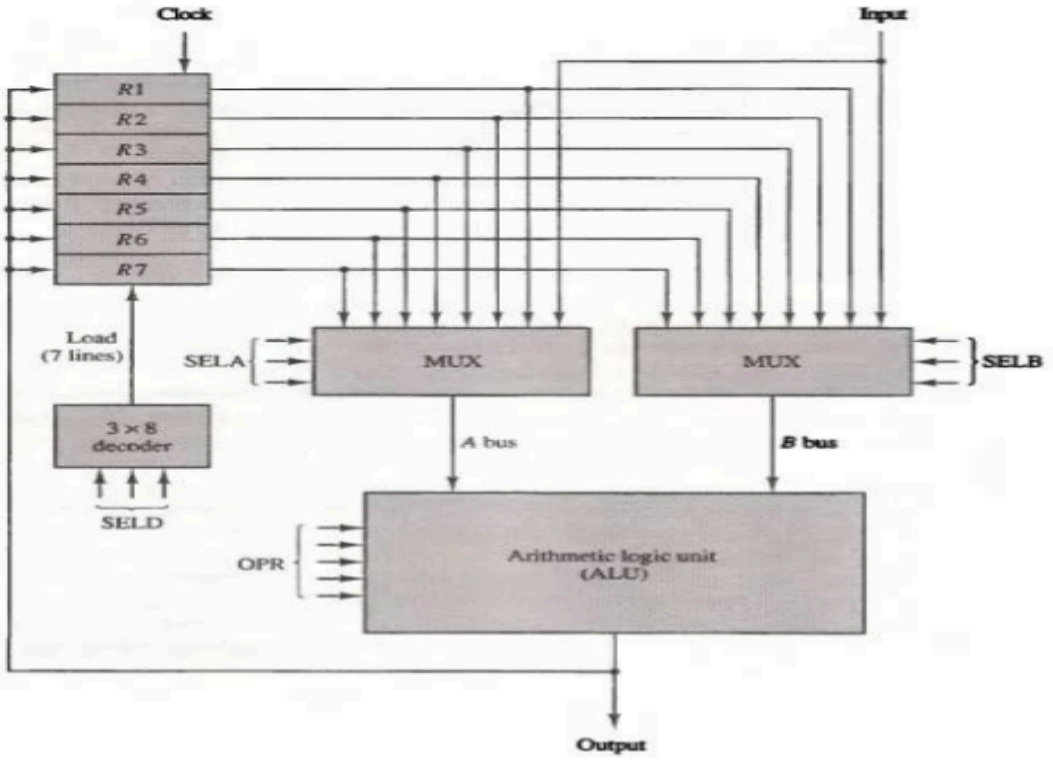
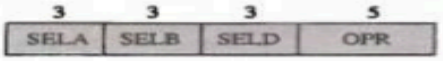
8-1. A bus-organized CPU similar to Fig. 8-2 has 16 registers with 32 bits in each, an ALU, and a destination decoder.

a. How many multiplexers are there in the *A* bus, and what is the size of each multiplexer?
b. How many selection inputs are needed for MUX A and MUX B?
c. How many inputs and outputs are there in the decoder?
d. How many inputs and outputs are there in the ALU for data, including input and output carries?
e. Formulate a control word for the system assuming that the ALU has 35 operations.

8-2. The bus system of Fig. 8-2 has the following propagation delay times: 30 ns for the signals to propagate through the multiplexers, 80 ns to perform the ADD operation in the ALU, 20 ns delay in the destination decoder, and 10 ns to clock the data into the destination register. What is the minimum cycle time that can be used for the clock?



(a) Block diagram



(b) Control word

Figure 8-2 Register set with common ALU.

8-3. Specify the control word that must be applied to the processor of Fig. 8-2 to implement the following microoperations.

a. $R1 \leftarrow R2 + R3$
b. $R4 \leftarrow R4$
c. $R5 \leftarrow R5 - 1$
d. $R6 \leftarrow \text{shl } R1$
e. $R7 \leftarrow \text{input}$

8-4. Determine the microoperations that will be executed in the processor of Fig. 8-2 when the following 14-bit control words are applied.

a. 00101001100101
b. 00000000000000
c. 01001001001100
d. 00000100000010
e. 11110001110000

8-5. Let SP = 000000 in the stack of Fig. 8-3. How many items are there in the stack if:

a. FULL = 1 and EMTY = 0?
b. FULL = 0 and EMTY = 1?

8-6. A stack is organized such that SP always points at the next empty location on the stack. This means that SP can be initialized to 4000 in Fig. 8-4 and the first item in the stack is stored in location 4000. List the microoperations for the push and pop operations.

8-7. Convert the following arithmetic expressions from infix to reverse Polish notation.

a. $A * B + C * D + E * F$
b. $A * B + A * (B * D + C * E)$
c. $A + B * [C * D + E * (F + G)]$
d. $\dfrac{A * [B + C * (D + \text{E})]}{F * (G + H)}$

8-8. Convert the following arithmetic expressions from reverse Polish notation to infix notation.

a. $A\ B\ C\ D\ E + * - /$
b. $A\ B\ C\ D\ E * / - +$
c. $A\ B\ C * /\ D - E\ F\ /\ +$
d. $A\ B\ C\ D\ E\ F\ G + * + * + *$

8-11. A computer has 32-bit instructions and 12-bit addresses. If there are 250 two-address instructions, how many one-address instructions can be formulated?

8-12. Write a program to evaluate the arithmetic statement:

$$X = \frac{A - B + C*(D*E - F)}{G + H*K}$$

a. Using a general register computer with three address instructions.
b. Using a general register computer with two address instructions.
c. Using an accumulator type computer with one address instructions.
d. Using a stack organized computer with zero-address operation instructions.

8-13. The memory unit of a computer has 256K words of 32 bits each. The computer has an instruction format with four fields: an operation code field, a mode field to specify one of seven addressing modes, a register address field to specify one of 60 processor registers, and a memory address. Specify the instruction format and the number of bits in each field if the in instruction is in one memory word.