SET – 3

Write a VHDL program for Full Subtractor.

```
Library IEEE;
    use IEEE.std_logic_1164.all;
    entity full_sub is
        port(A,B,brr_in: in std_logic;
            diff,brr_out: out std_logic);
         end full_sub;
         architecture flow of full_sub is
            component half_sub is
                port(A,B: in std_logic;
                    diff,brr: out std_logic);
                end component;
                component OR_gate is
                    port(A,B: in std_logic;
                        Y: out std_logic);
                 end component;
                 signal T1,T2,T3:std_logic;
                 begin
                     half_sub1: half_sub port map
(A=>A,B=>B,diff=>T1,brr=>T2);
                     half_sub2: half_sub port map
(A=>T1,B=>brr_in,diff=>diff,brr=>T3);
```

```
                    OR_gate1: OR_gate port map
(A=>T3,B=>T2,Y=>brr_out);
                end flow;
```

Truth table: -

Inputs			**Output**	
A	B	Brr(In)	Diff	Borrow
0	0	0	0	0
0	0	1	1	1
0	1	0	1	1
0	1	1	0	1
1	0	0	1	0
1	0	1	0	0
1	1	0	0	0
1	1	1	1	1

Wave: -