CREATING A NEW PROJECT IN MODELSIM

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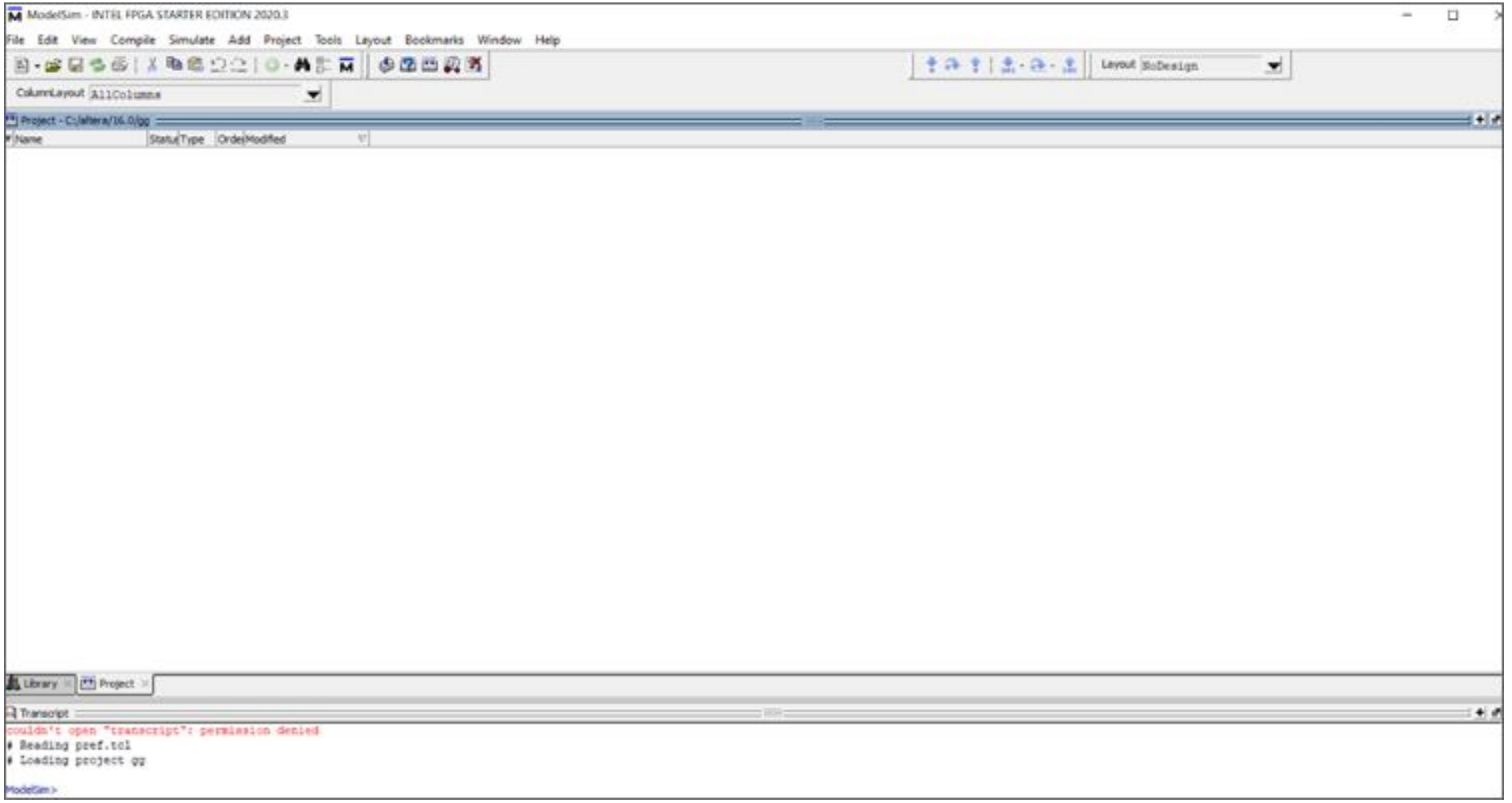
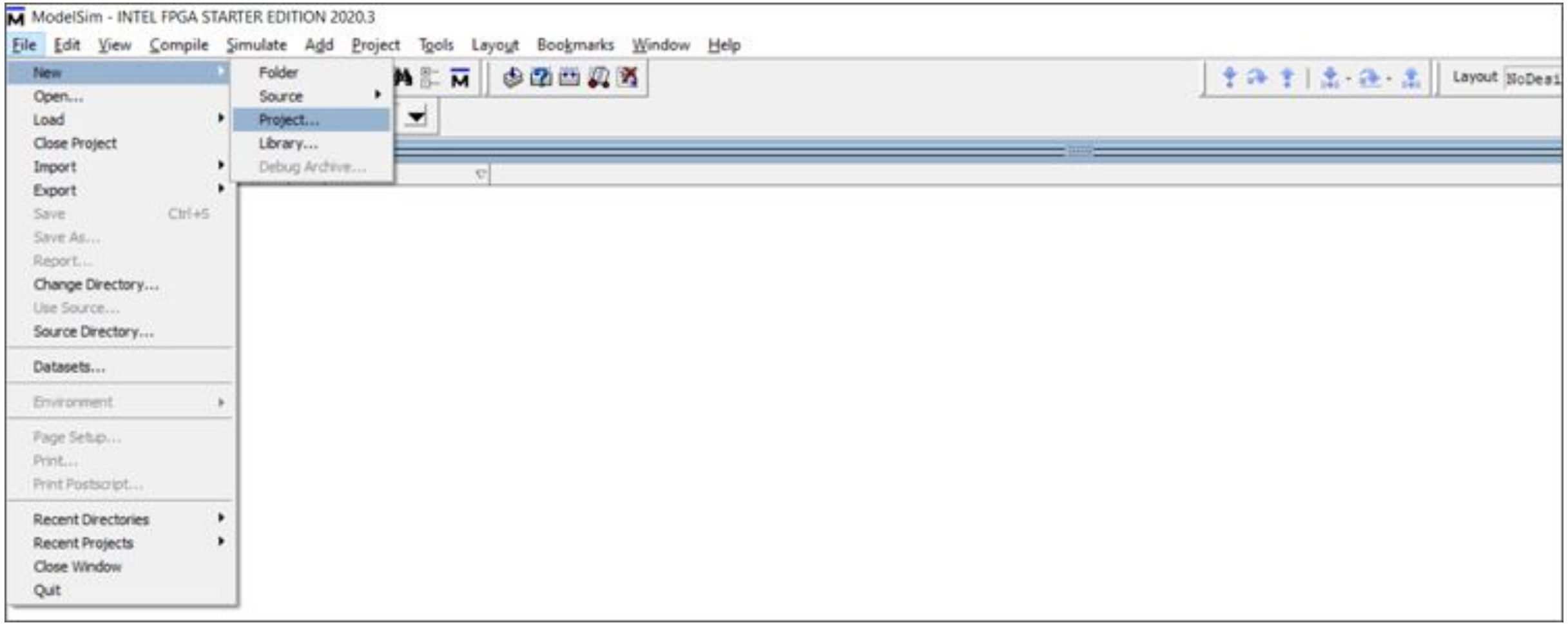
Before scripting the VHDL program, first, we need to create a project in the ModelSim. The steps to create the project are given below.

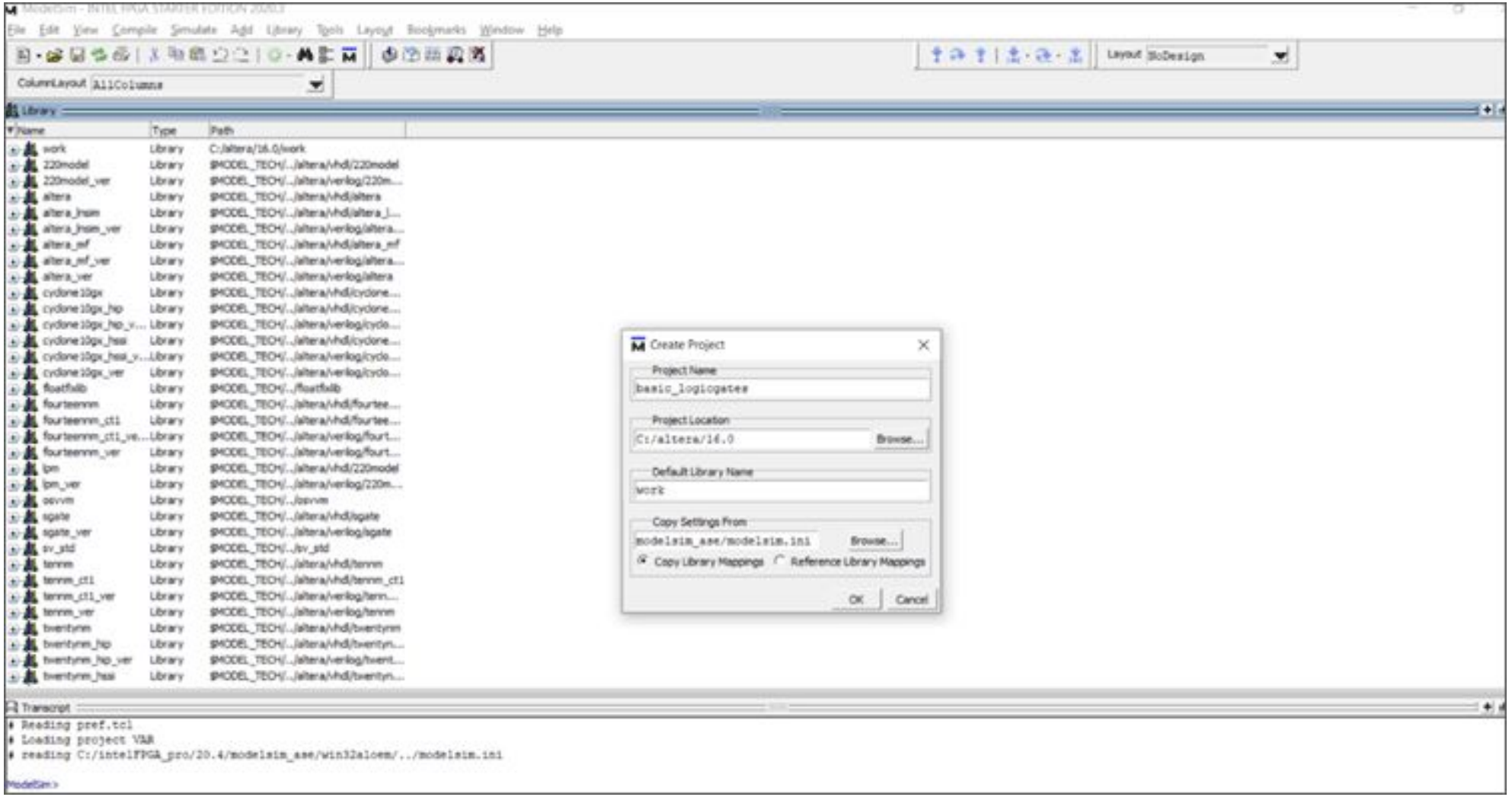
Step 1: Open ModelSim



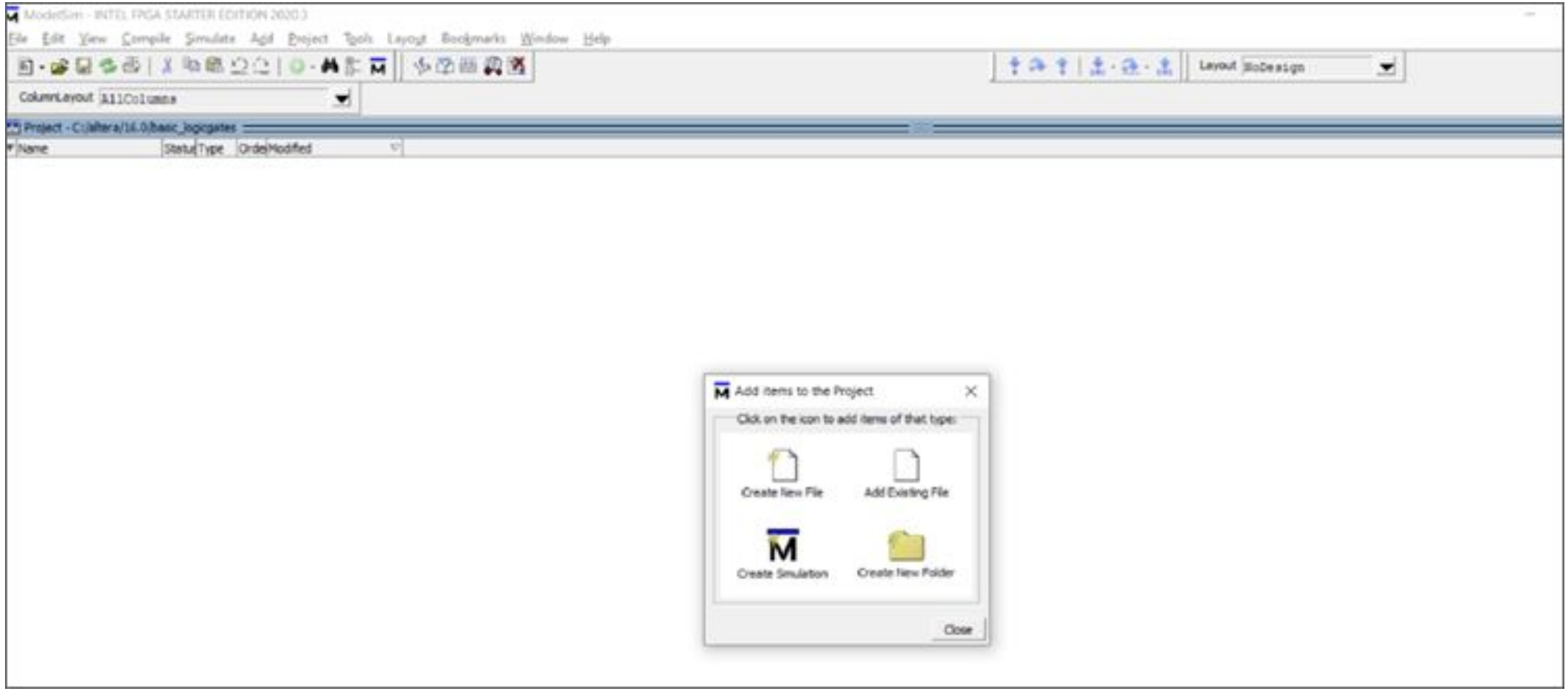
Step 2: Click File---->New---->Project



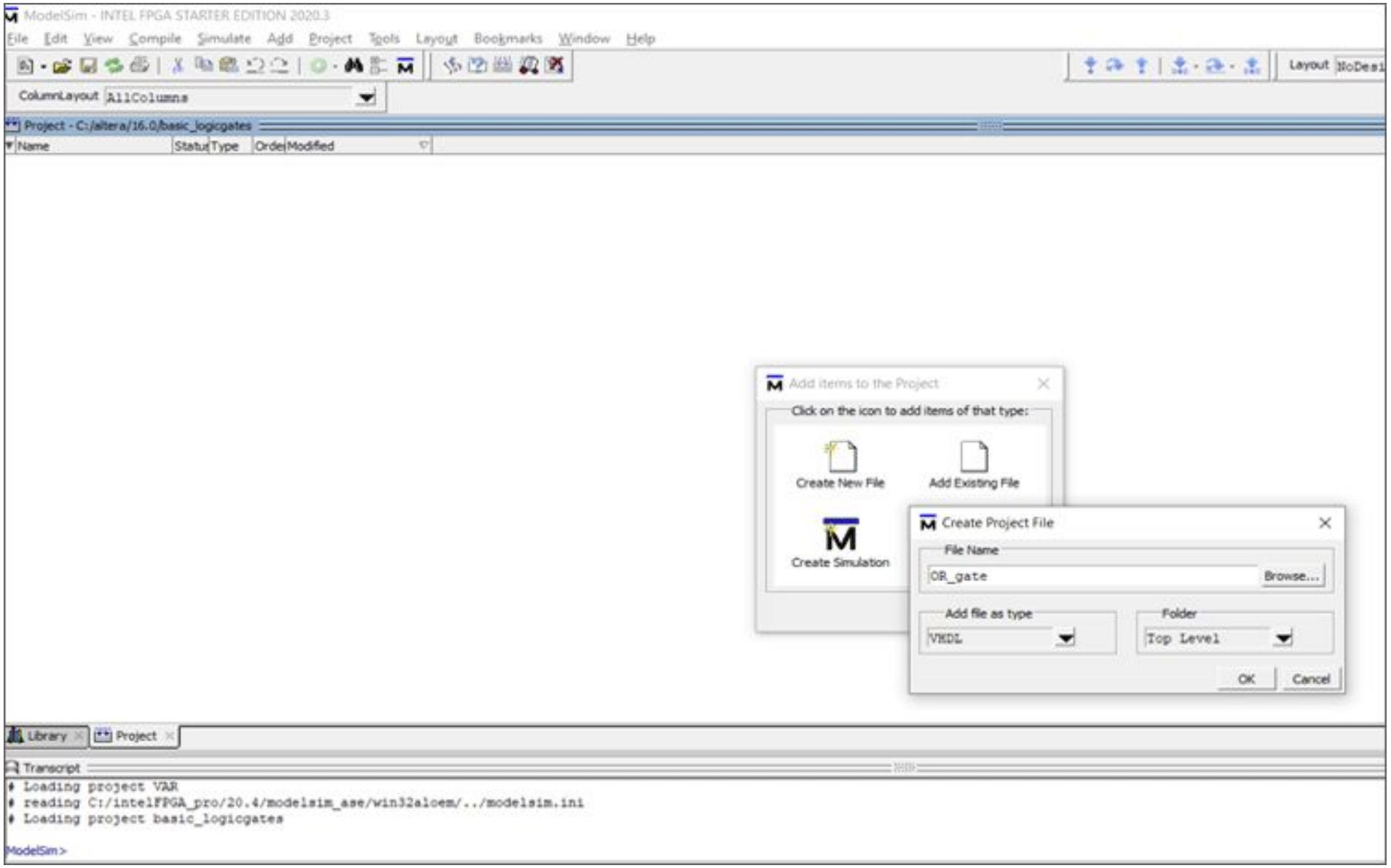
Step 3: The create new project dialog box opens up. Enter the name for your project and click OK as shown below. For example, the project name given below is **“basic_logicgates”**



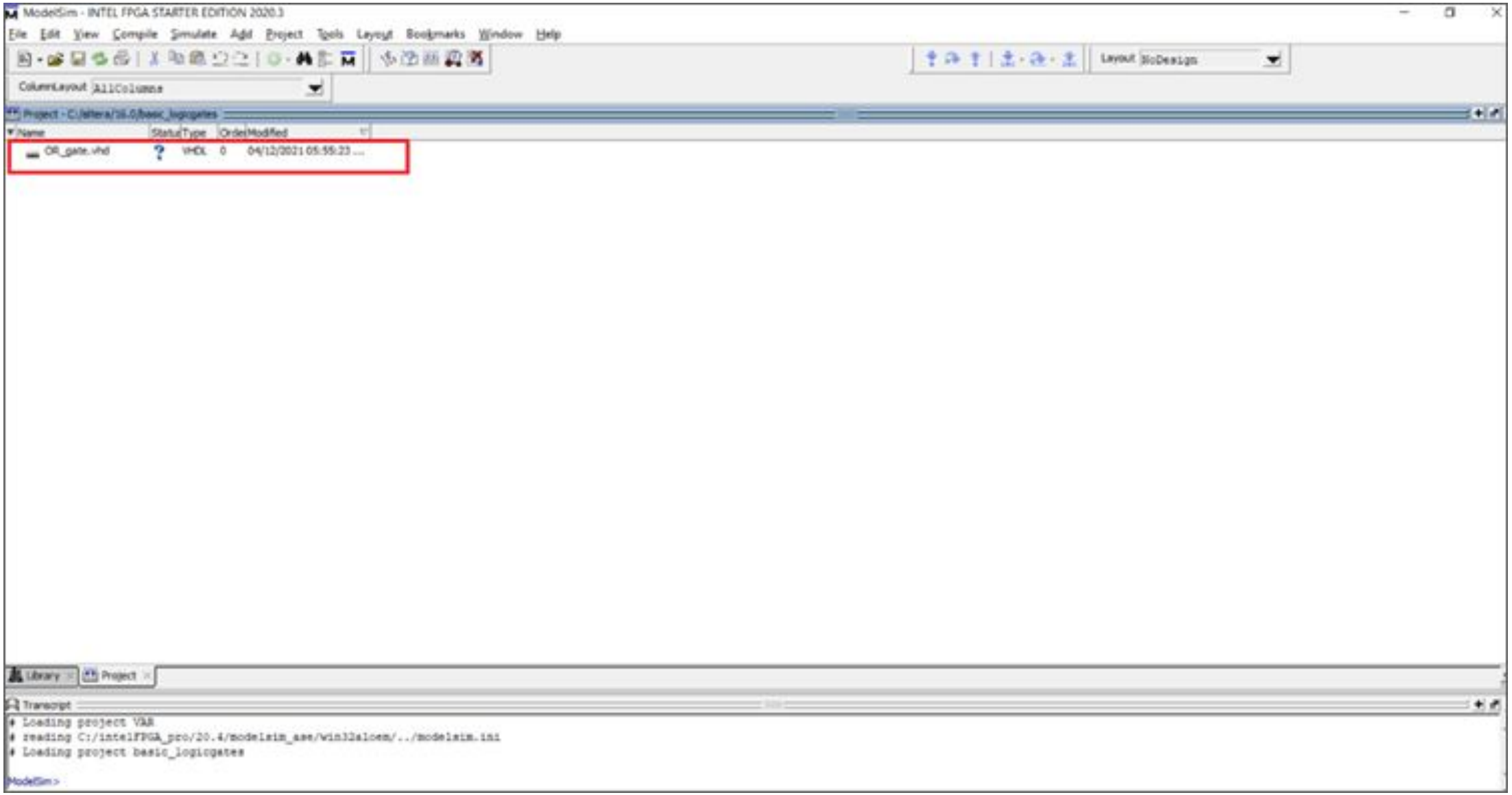
- **Step 4:** The project will be created and the **"Add Items to the project"** dialog box opens. Click on Create New File.



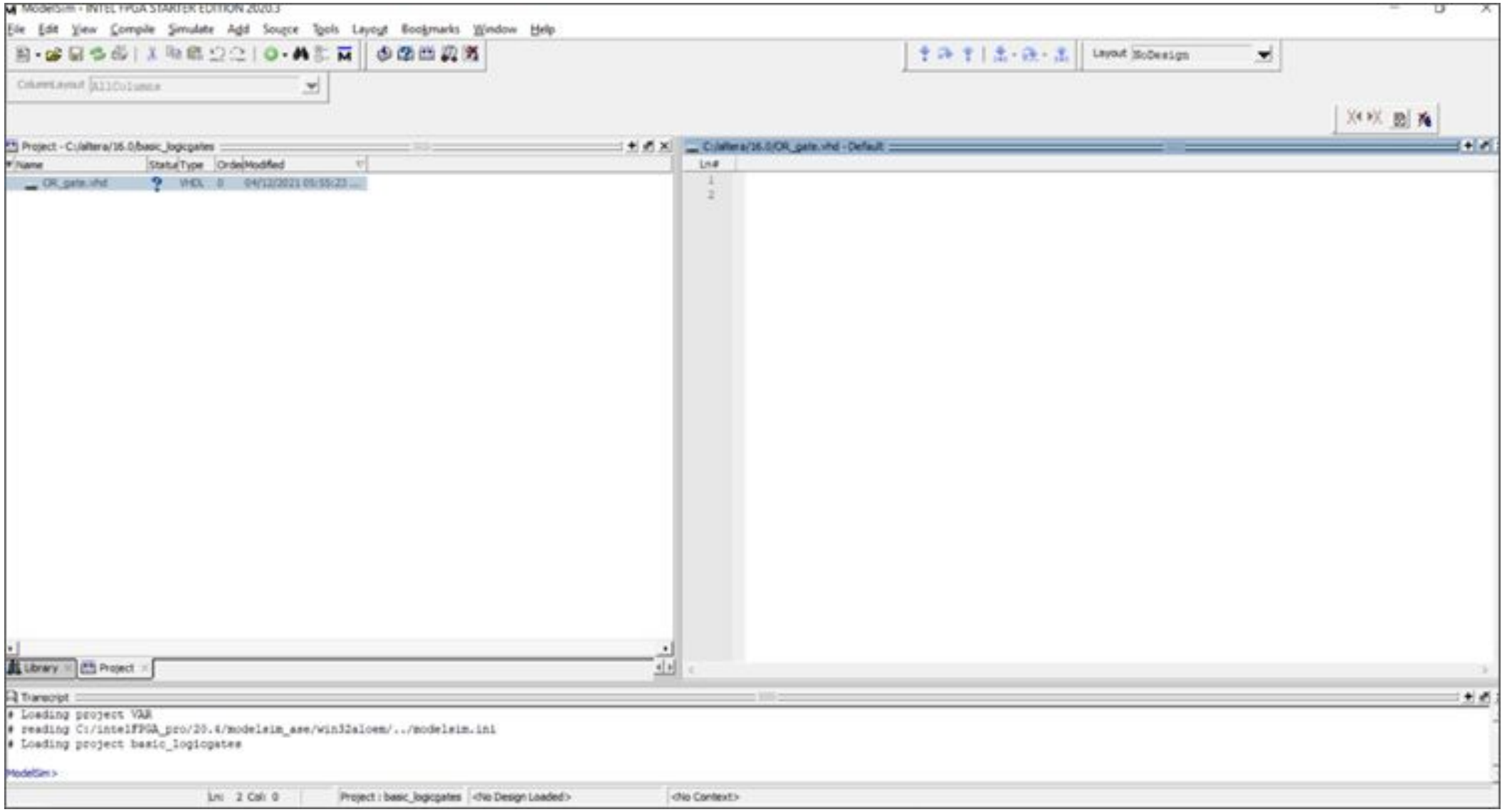
Step 5: 'Create a new project file' opens up. Give a file name and choose the file type as VHDL and click OK. Here, for example, the file name is given as OR_gate.



Step 6: The project will be created and the file **OR_gate** will be added as shown below.



Step 7: Now that the file is added, we can start scripting our first VHDL program. Double click the ***OR_gate.vhd***, an editor will open up on the right side of the window.



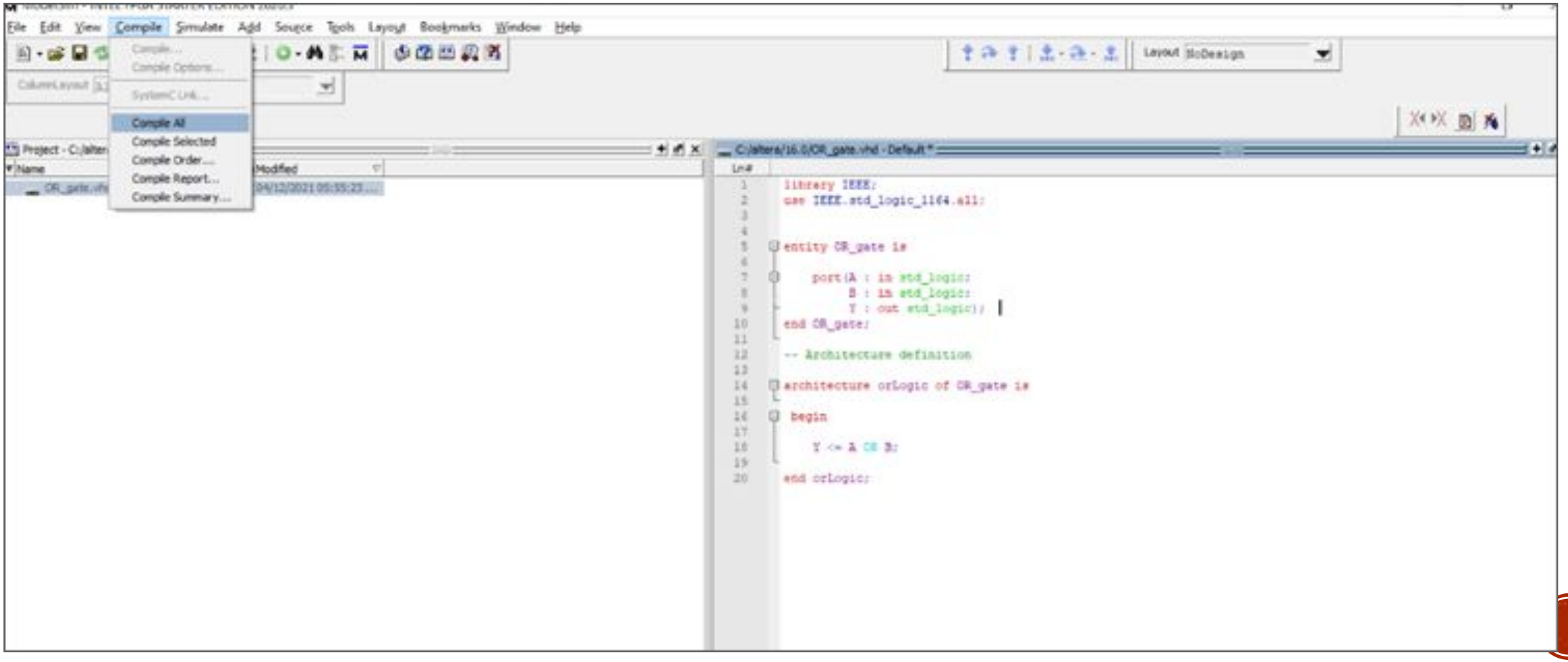
VHDL OR GATE

```
Library IEEE;
use IEEE.std_logic_1164.all;
entity OR_gate is
    port(A : in std_logic;
         B : in std_logic;
         Y : out std_logic);
end OR_gate;
architecture orLogic of OR_gate is
 begin
    Y <= A OR B;
end orLogic;
```

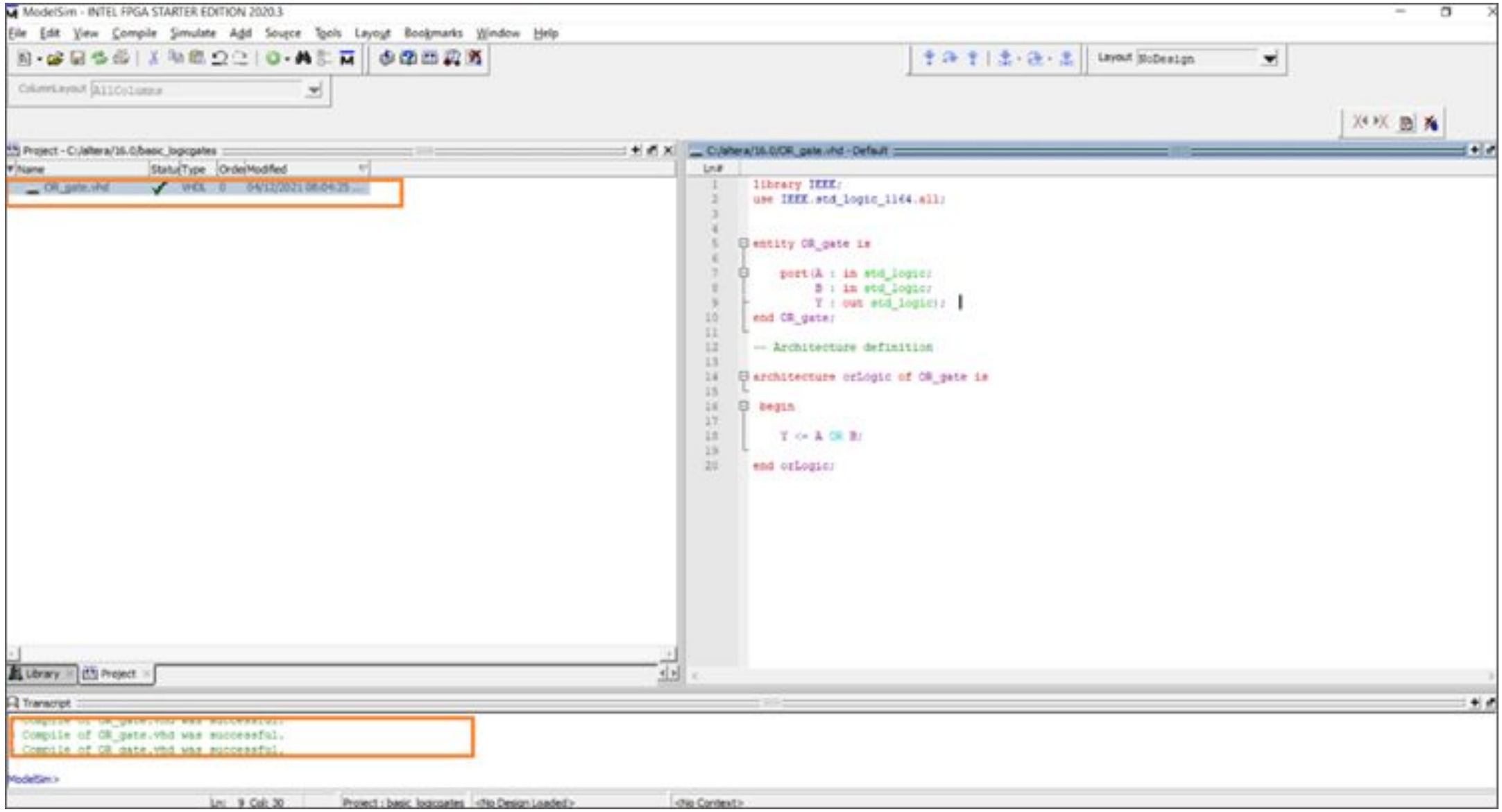
- First the Libraries are imported.
- Since A and B are the inputs, variables A and B are mapped to “in std_logic”. Here “in” refers to the input and std_logic refers to the standard signal/waveform. Similarly Y is mapped to “out std_logic” which refers to the output. Finally, the entity declaration is terminated by “end OR_gate”.

HOW TO COMPILE AND SIMULATE CODE ON MODELSIM?

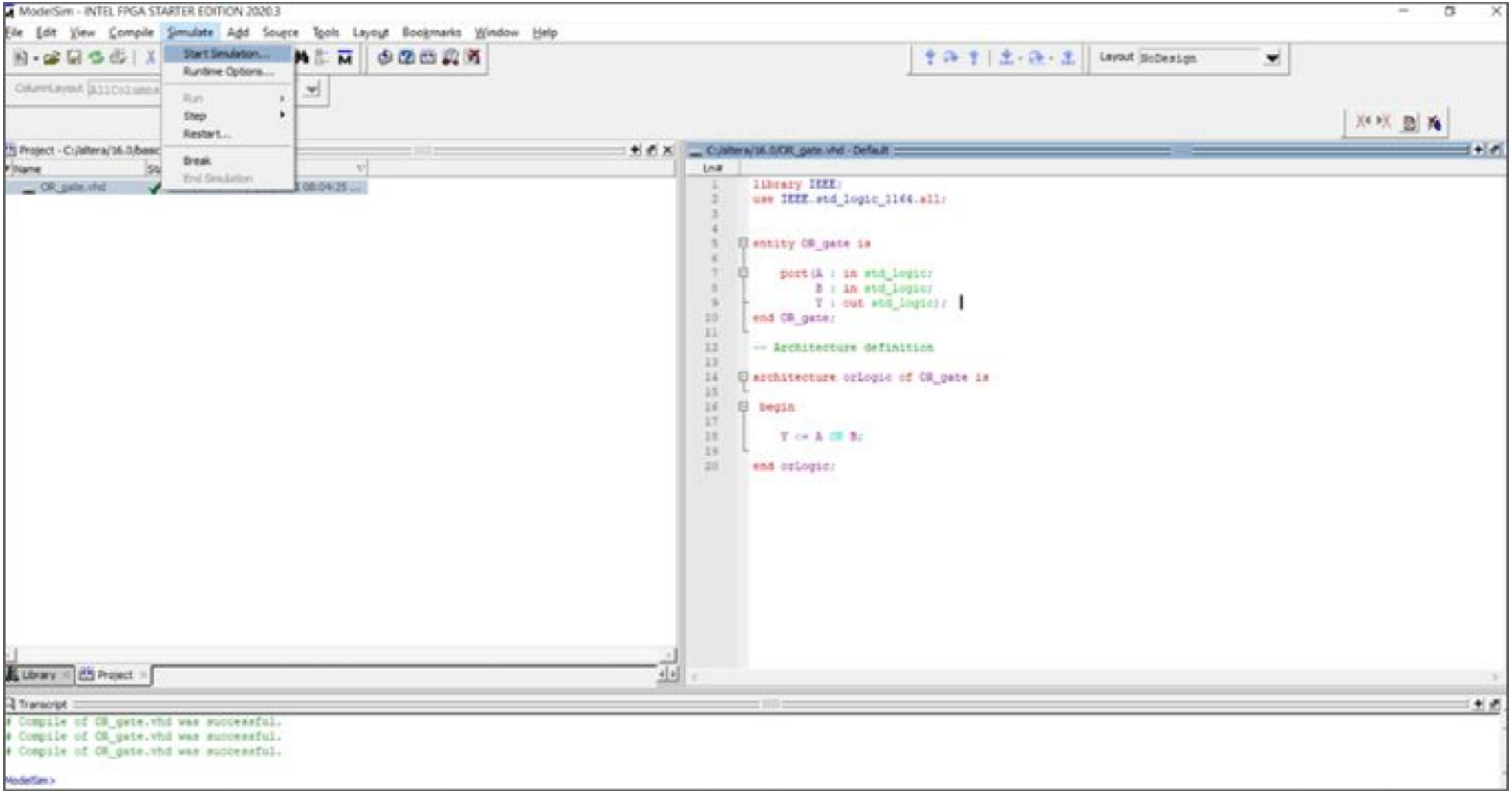
Step 1: First save the File by ***Ctrl+S.*** On the Tool Bar of the ModelSim, there is an option called “Compile”. Click **Compile>>>Compile All**.



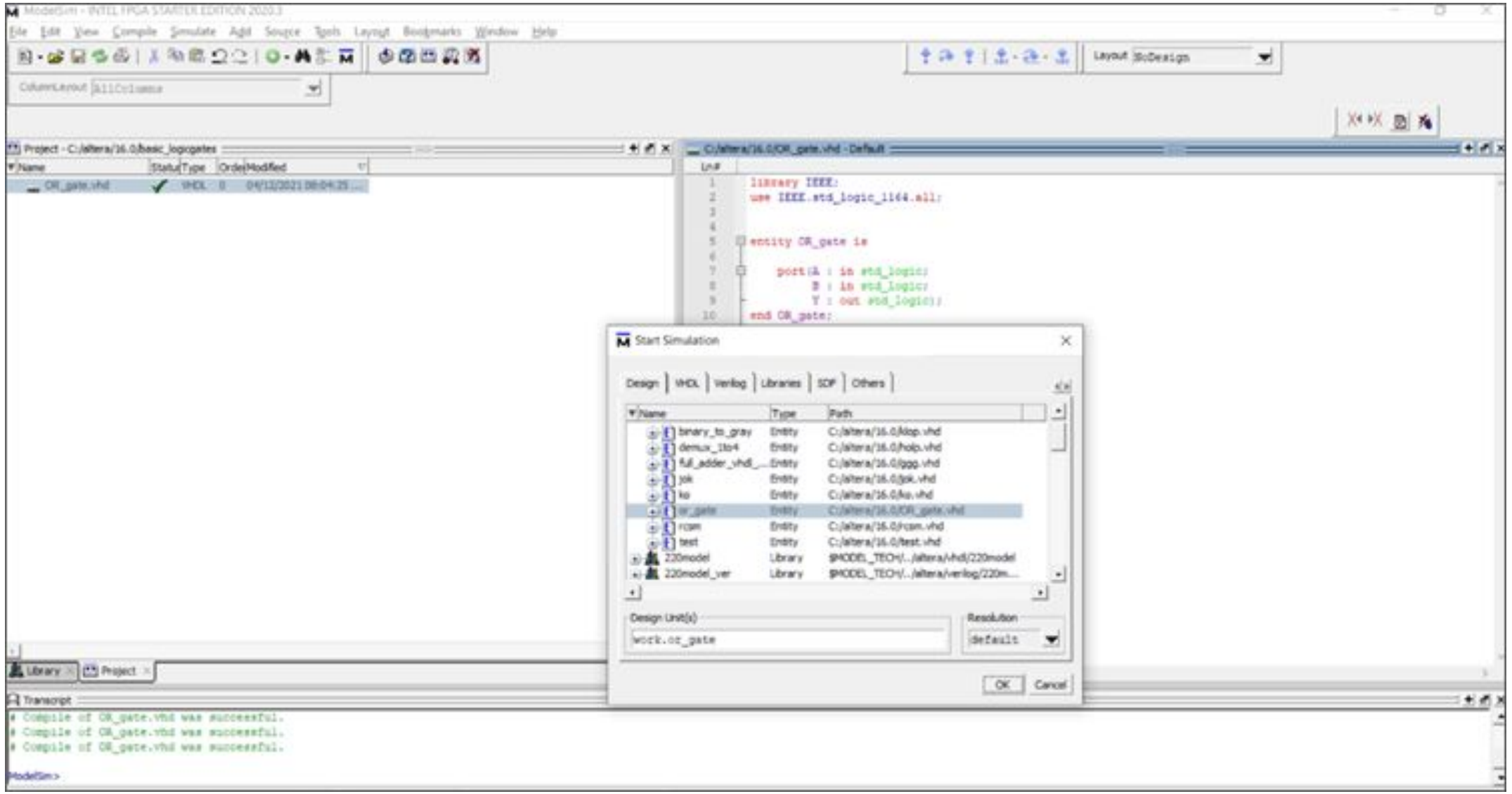
Step 2: Once Compiled All is clicked. The files are compiled and we can see a green tick mark “ü” and “Compile of entity name.vhd was successful” as shown below.



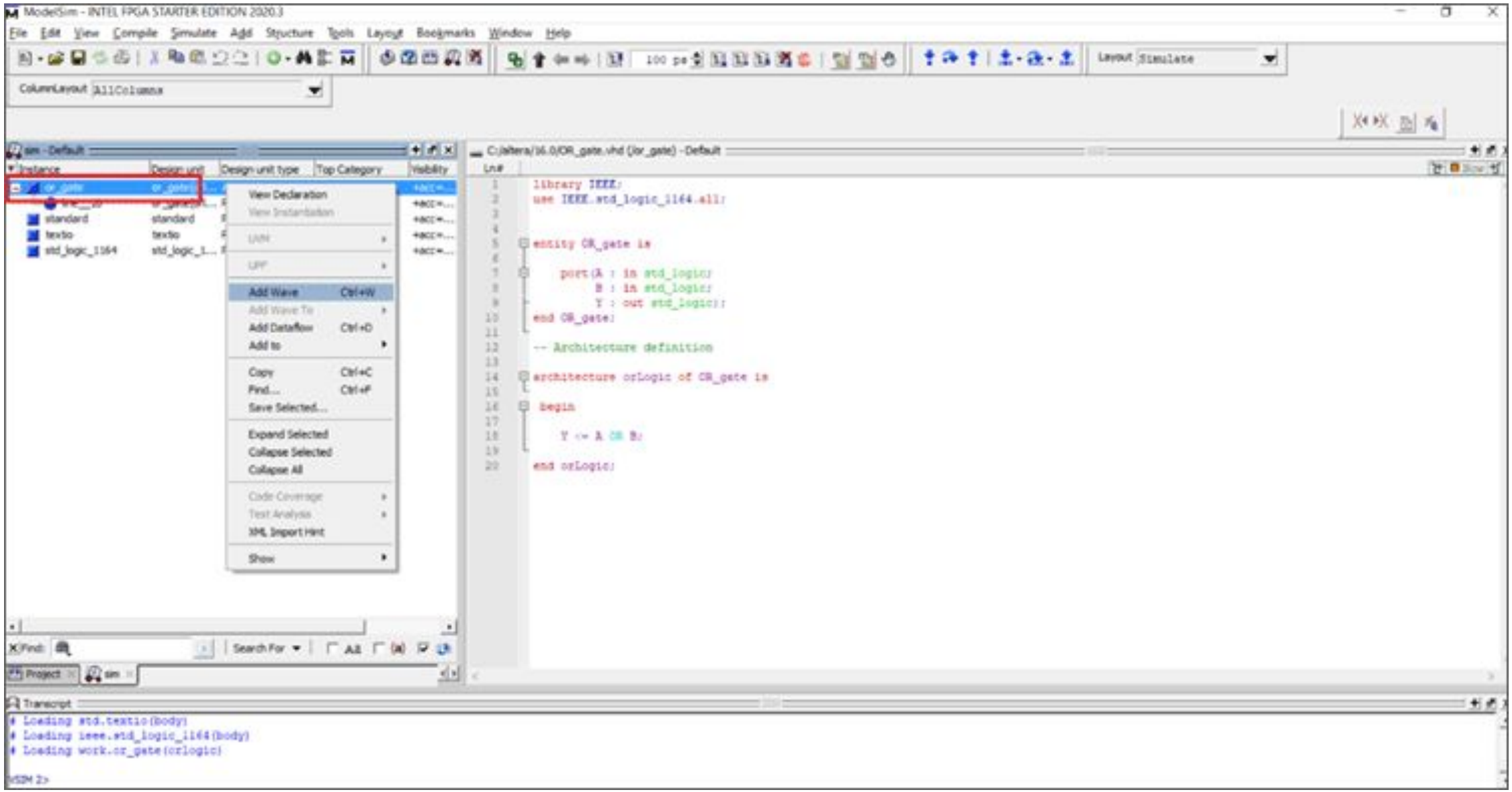
Step 3: If you find a red mark or unsuccessful please check your code if it has errors. Now that the compilation is successful. Let's simulate the designed circuit. On the ToolBar, there is an option called ”Simulate” as shown below. Click **Simulate>>>Start Simulate.**



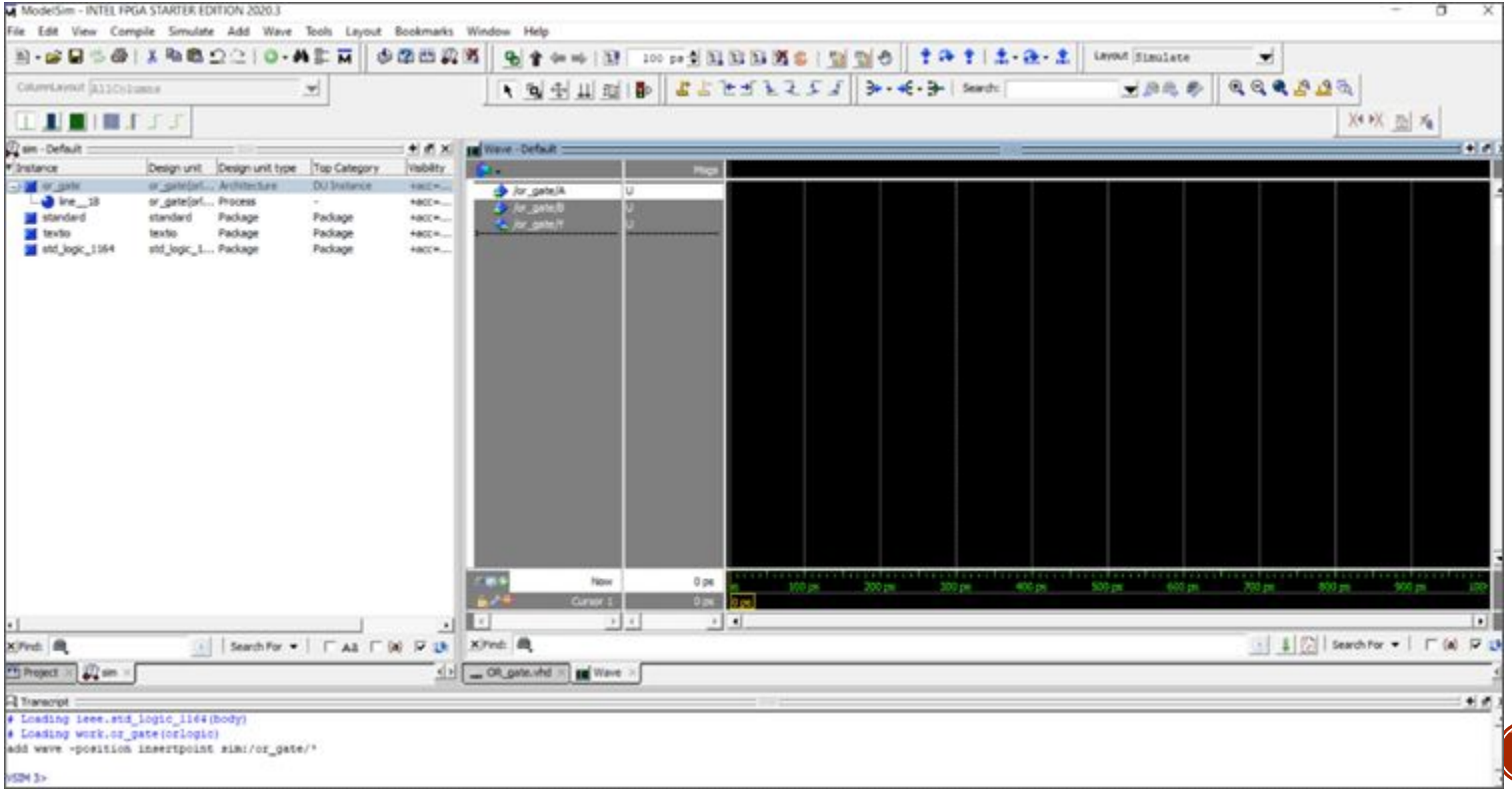
- **Step 4:** Once you select Start Simulation, a dialog box opens, and there is a folder called “Work”. Click Work Here, we can see our entity name (OR_gate). Select the “OR_gate” and click OK.



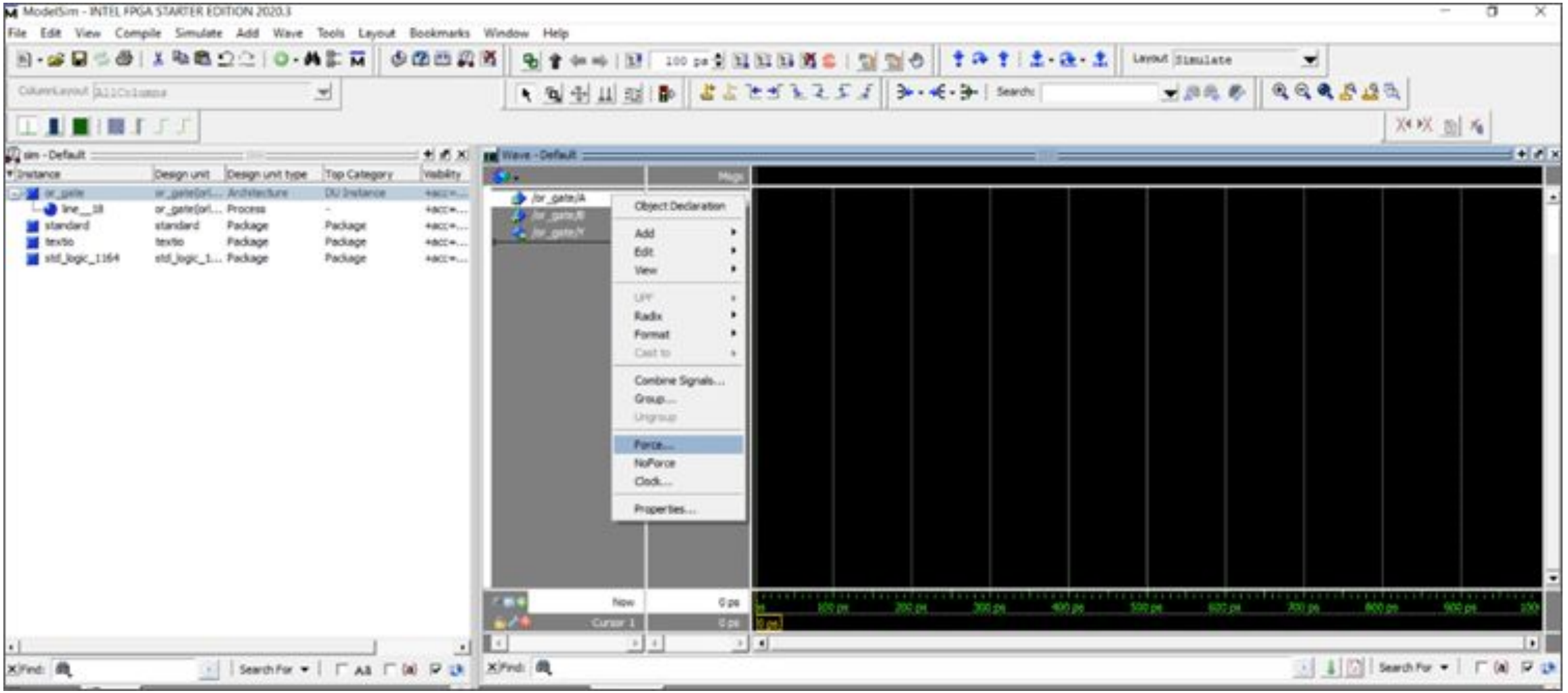
Step 5: The Simulation Window Opens. Right Click on the entity name (OR_gate) and click Add Wave as shown below.

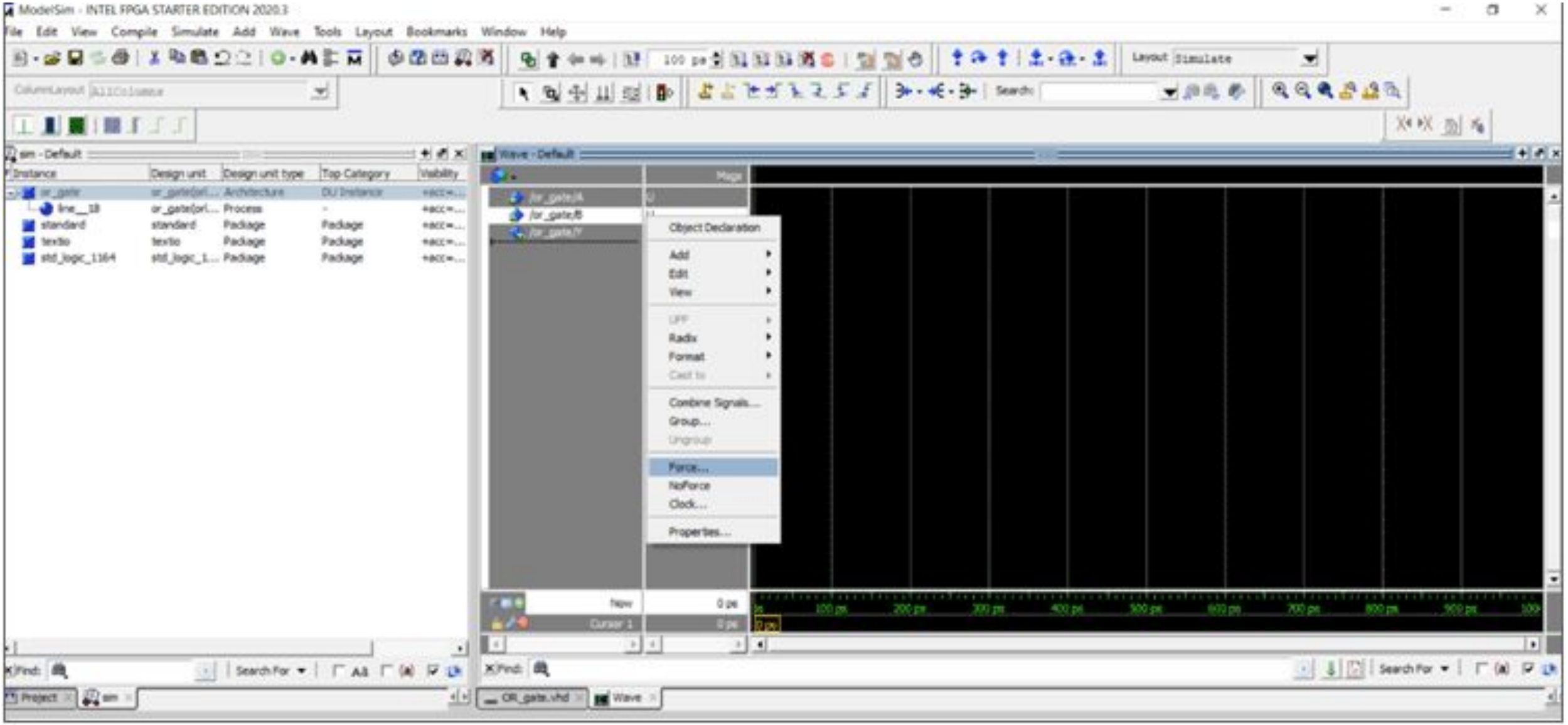


Step 6: The waveform window opens with declared inputs and outputs on the right side of the window as shown below.

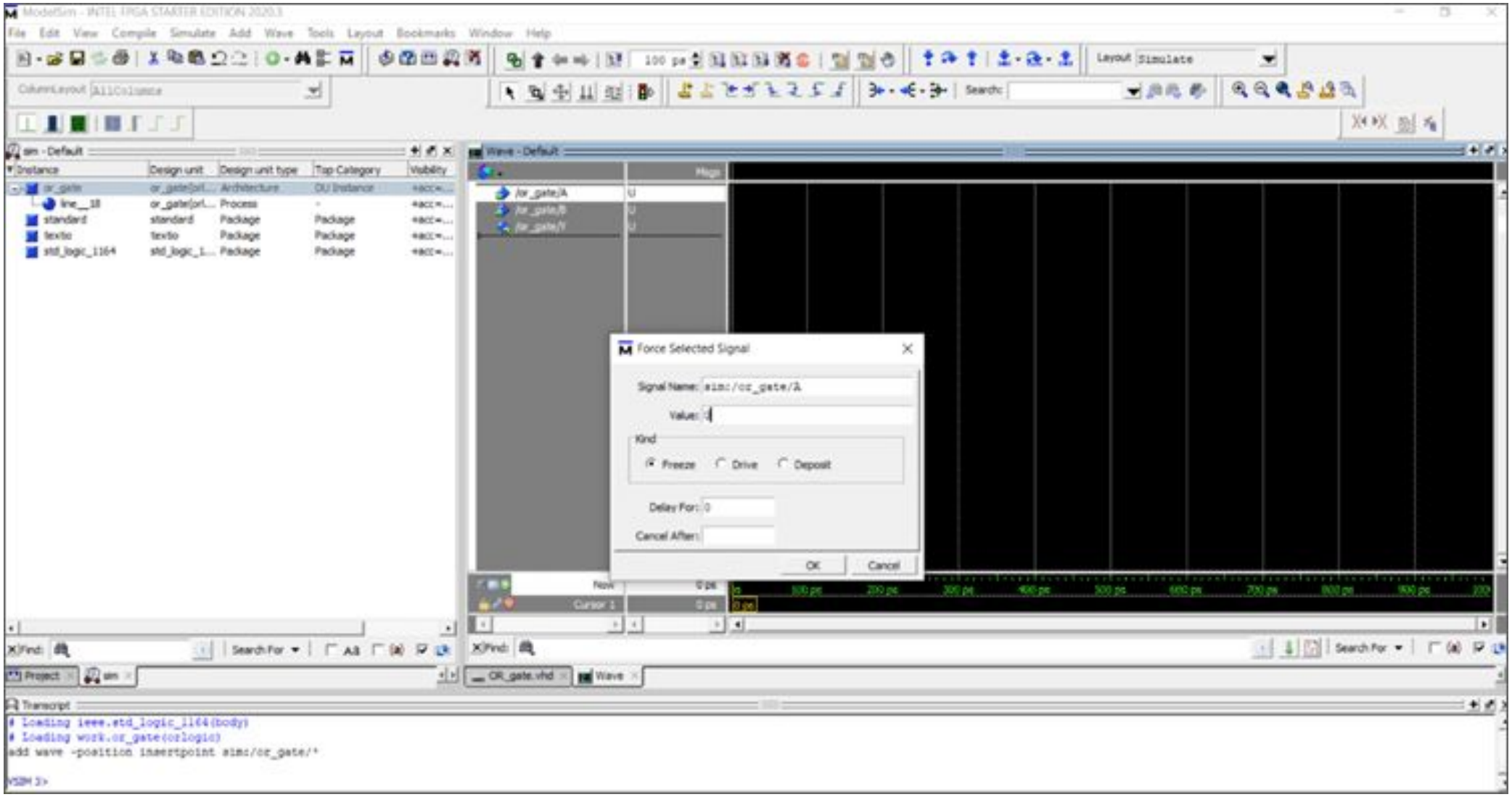


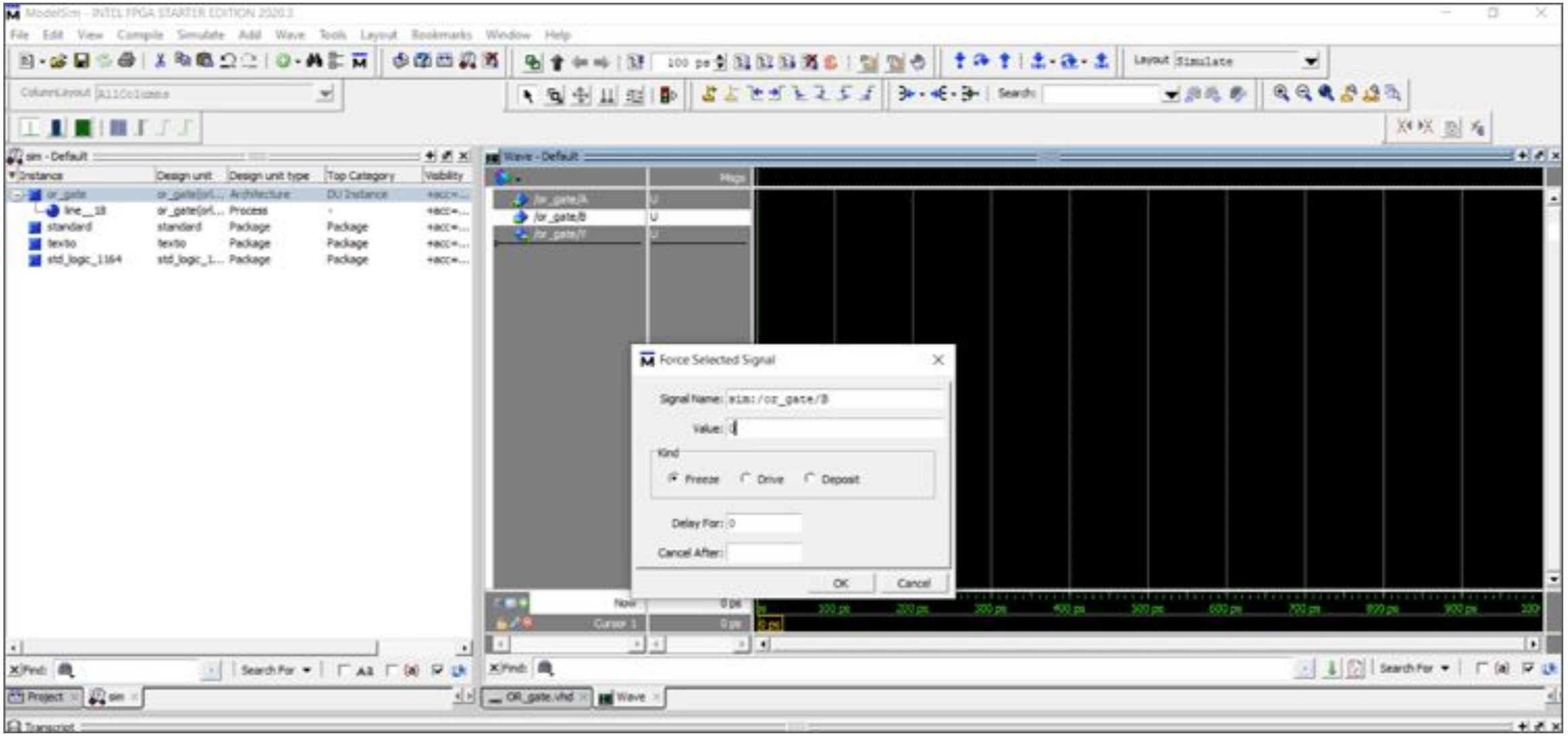
- **Step 7:** Now, let us simulate the circuit by giving the inputs. Right Click on the Inputs A and B. A menu pops up from that choose “Force” option.



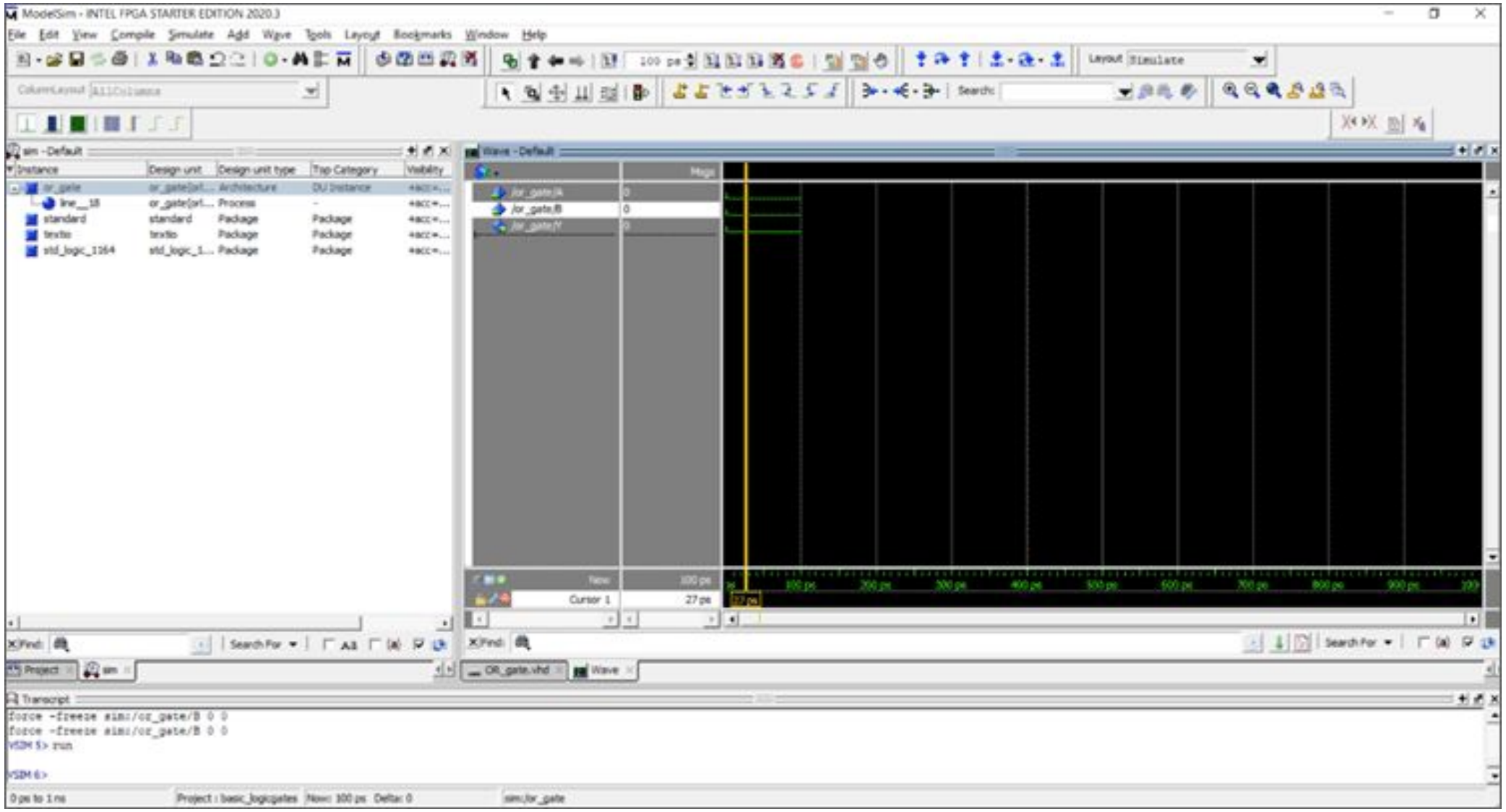

ModelSim - INTEL FPGA STARTER EDITION 2020.3
File Edit View Compile Simulate Add Wave Tools Layout Bookmarks Window Help
sim - Default
Instance
Design unit
Design unit type
Top Category
Wave - Default
Object Declaration
Add
Edit
View
Radix
Format
Combine Signals...
Group...
Ungroup
Force...
NoForce
Clock...
Properties...
Now
Cursor 1
Project
sim
OR_gate.vhd
Wave

- **Step 8:** Now a dialog box opens up. Set the Value to 0 for A and similarly for B set the value 0 and click OK.




ModelSim - INTEL FPGA STARTER EDITION 2020.3
File Edit View Compile Simulate Add Wave Tools Layout Bookmarks Window Help
sim - Default
Instance
Design unit
Design unit type
Top Category
Visibility
or_gate
or_gate(arl...
Architecture
DU Instance
line__18
or_gate(arl...
Process
standard
standard
Package
Package
textio
textio
Package
Package
std_logic_1164
std_logic_1...
Package
Package
Wave - Default
Msgs
/or_gate/A
/or_gate/B
/or_gate/Y
Force Selected Signal
Signal Name: sim:/or_gate/B
Value: 1
Kind
Freeze
Drive
Deposit
Delay For: 0
Cancel After:
OK
Cancel
Now
Cursor 1
Project
sim
OR_gate.vhd
Wave
Transcript

Step 9: Now that the inputs are given, let's Run the simulation. There is a Run icon in the toolbar near the timer as shown below. Click the run icon, we can see the waveforms on the graph for 100 ps. There is a yellow colour cursor on the waveform, move the cursor so that the corresponding inputs and outputs are shown.



Now, we can see that for A=0, B=0, Y=0, which verifies with Truth Table of OR Gate. Similarly, the other four input combinations are given and their outputs are verified as shown below.